AD-A193 225 VERY HIGH SPEED INTEGRATED CIRCUITS (VHSIC)(U) OFFICE OF THE UNDER SECRETARY OF DEFENSE (ACQUISITION) WASHINGTON DC VHSIC P ROGRAM OFFICE 31 DEC 87 1/2

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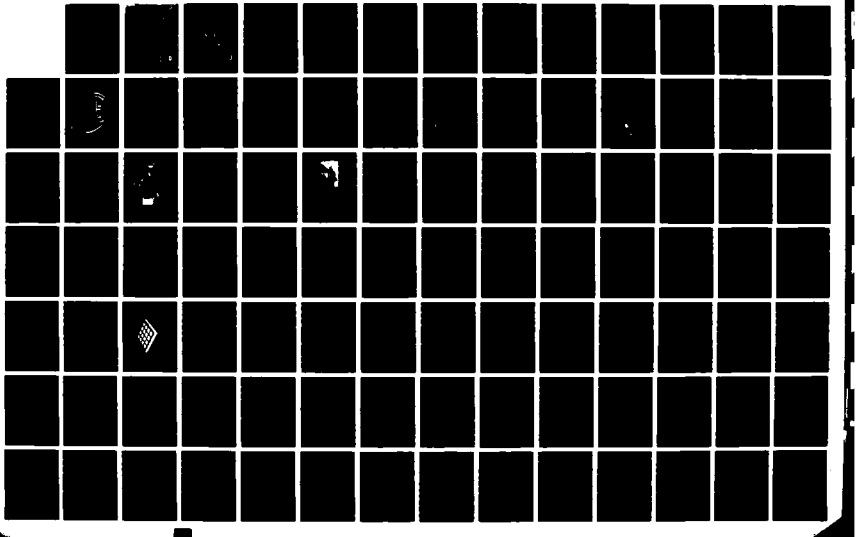

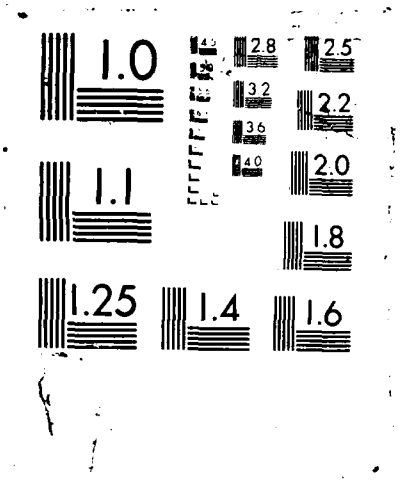
1.0
1.1
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1.6
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2.0
2.2
2.5
2.8
3.2
3.6
4.0

VERY HIGH SPEED INTEGRATED CIRCUITS

-VHSIC-

ANNUAL REPORT FOR 1987

VERY HIGH SPEED INTEGRATED CIRCUITS

- VHSIC -

ANNUAL REPORT FOR 1987

VHSIC PROGRAM OFFICE

OFFICE OF THE UNDER SECRETARY OF DEFENSE FOR ACQUISITION

31 December 1987

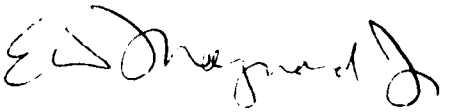
FOREWORD

The VHSIC Program is currently in its seventh year, with only a few more challenging years to go. DoD and the Services have made tremendous strides in all of the related digital microelectronics technology areas, and we are not through yet. Furthermore, we are already seeing substantial payoffs - and, I might add, ahead of schedule.

Our primary goal at the start of the VHSIC program was to reduce the relative time from the introduction of a microelectronic technology into the commercial market until the technology is first applied in our deterrent and warfighting systems. Specifically, we wanted to reduce this from around 10 to 12 years to less than 5 years with Phase 1 technology and to less than 2 years with Phase 2 technology. VHSIC 1, or 1.25 micrometer feature size integrated circuit (IC) technology, was first available in the commercial market in 1986. Therefore, all the 1.25 micrometer technology applications that will be operational before 1991 demonstrate that both the VHSIC technology development initiative is ahead of schedule, and it is feasible to insert advanced technology in our systems within 2 to 5 years from when it first becomes available in the commercial market.

VHSIC is not just a finite number of chips nor a few pilot production lines; rather, the VHSIC initiative has developed advanced processes, new manufacturing equipment and tools, new materials, new qualification requirements and procedures, new levels of radiation hardening, new interface standards and specifications, and improved techniques for built-in-test and maintainability to support a system design framework which exploits advanced technology. The successful developments of the VHSIC Program to date have spurred many other companies on the periphery of the "VHSIC family" to establish, independently, their own VHSIC design and fabrication centers as well as to undertake additional system insertion projects. These activities are all highlighted in this report.

The VHSIC program has successfully met the Phase 1 challenge; and, as highlighted in this report, is well on its way to developing and applying the next generation of IC technologies. The microelectronics technology has, over the past four decades, steadily grown from a mere aid to military operations, to being the "eyes and ears" and now, also, the "brains" of our deterrent systems. The ultimate capabilities available through the application of advanced microelectronic integrated circuits are limited only by our imagination, and it is our responsibility to obtain the greatest deterrent capabilities through the aggressive application of this new technology. The VHSIC Program Office is dedicated to making sure that the technologies and supporting tools are available when needed for use in our systems of the future.



E.D. Maynard, Jr.
Director
Computer and Electronics Technology

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CHAPTER I

SUMMARY

Very High Speed Integrated Circuits (VHSIC) is the name of the Department of Defense program to develop two new generations of the silicon integrated circuits which are needed to provide higher performance electronics for DoD weapon systems.

I.1 BACKGROUND

The defense posture of the United States is increasingly based upon the concept of a military force that is technologically superior to any potential adversary. Technology is expected, wherever possible, to leverage our ability to defend against numerically greater forces. The integrated circuit, which is the basic device for doing signal processing in any modern electronic system, has become one of the most effective force multipliers for our Nation's defense. The technology for making the device is a very demanding one. Complex and expensive equipments are required to produce it, advanced skills and knowledge are required to practice it, and very large investments are required to maintain its progress. The United States pioneered the introduction of the IC industry and still retains a very strong position in the development and application of new products.

In the past we were able to maintain a comfortable lead in the military applications of integrated circuits. However, by the late 1970s it became apparent that our "comfortable" lead had seriously eroded. Our ability to maintain a superior military force through the conventional application of advanced electronic technology was in question. The result was that the security and integrity of our future military capabilities were jeopardized. It became necessary to restore a more assured lead through earlier implementation of that technology.

One of the major causes of this erosion of technological leadership was that it was taking longer and longer for the DoD to move high performance ICs from the development laboratory into military systems. Commercial use of a given level of IC technology, by contrast, often preceded military applications by as much as eight to ten years as illustrated in Figure I.1. This also meant that the electronic components in some military weapon systems were becoming technologically obsolete before the systems had completed their expected logistic life span. More recently, obsolescence of electronic parts has sometimes occurred even before final production runs. Five major factors have contributed to this situation.

- By 1978, increasing commercial application of ICs had reduced the military share of the IC industry market to approximately 7%. Manufacturers thus were giving higher priority to commercial markets rather than to military orders.

- The requirements for reliable, real-time processing under military environmental conditions imposes unique requirements on ICs which cannot generally be met by even the best commercial products.

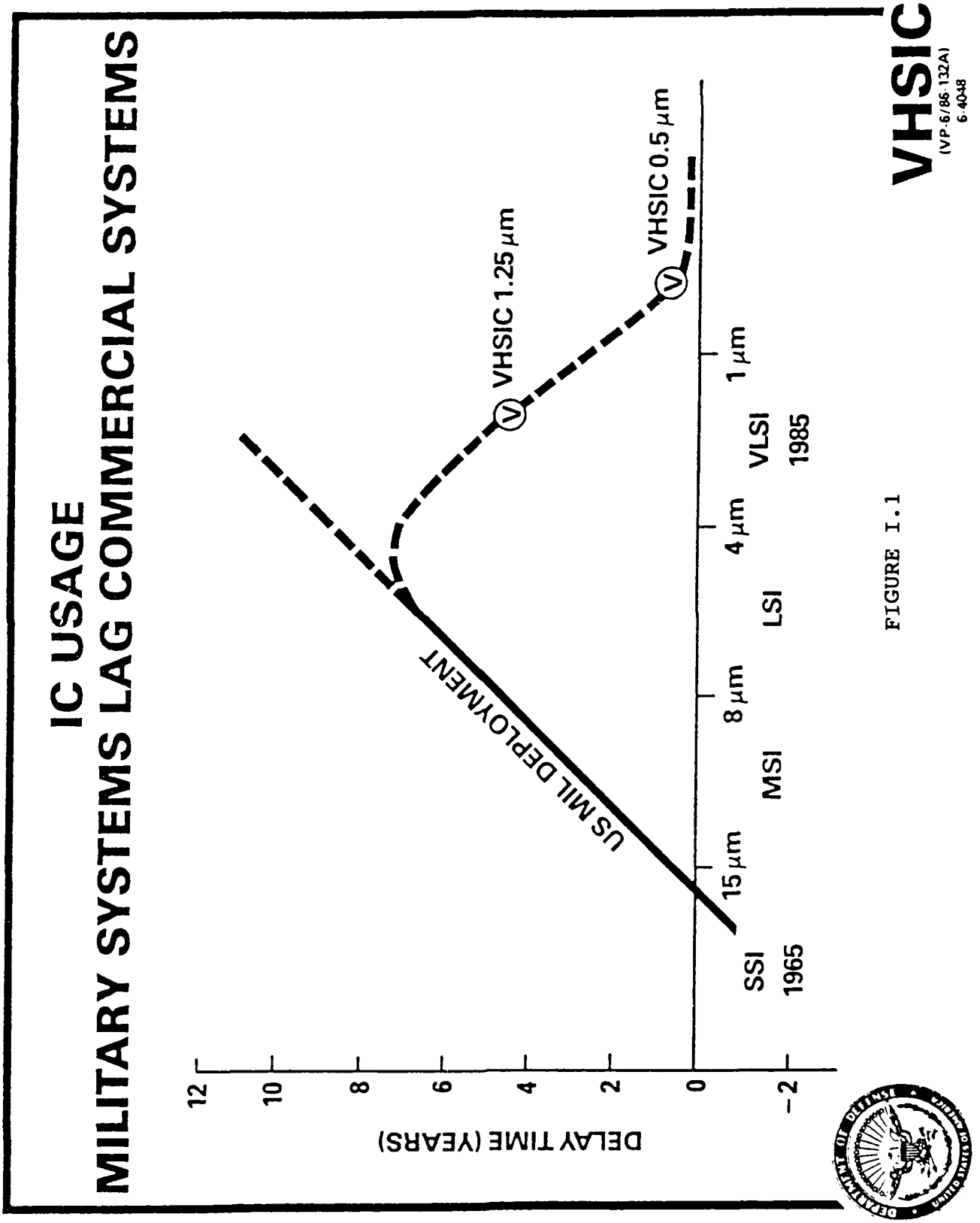

IC USAGE
MILITARY SYSTEMS LAG COMMERCIAL SYSTEMS
DELAY TIME (YEARS)
12
10
8
6
4
2
0
−2
US MIL DEPLOYMENT
VHSIC 1.25 μm
VHSIC 0.5 μm
15 μm
8 μm
4 μm
1 μm
SSI
MSI
LSI
VLSI
1965
1985
VHSIC
(VP-6/86-132A)
6-4048

FIGURE I.1

- o The cost of designing and producing ICs had increased sharply with complexity. The small production runs involved in many military procurements, however, did not provide a large enough base for absorbing the higher fixed costs. This resulted in much higher unit costs for military ICs compared to the commercial market.

- o The rapid evolution of new IC designs and production technologies resulted in early obsolescence of many specific parts and the facilities that produced them. This caused severe logistics repair and replacement problems for systems already in the field.

- o Military system program managers were cautious about inserting new IC technology in system developments which were subject to limited program funds and fixed time schedules.

Additional background information on the origins and progress of the VHSIC programs can be found in the "VHSIC Annual Report for 1986", reference I.1, and in references I.2 through I.9.

I.2 INSERTION HIGHLIGHTS

Success in designing VHSIC into systems has already been achieved, starting with the demonstration of a VHSIC circuit board in the AN/ALQ-131 airborne countermeasures pod in December 1985 and with the production, in 1987, of retro-fit spares for operational F-111 aircraft by the Air Logistics Center in Sacramento using gate arrays. These VHSIC system insertions have shown that the DoD can put state-of-the-art electronic technology into military systems at least as quickly as it is put into commercial systems.

There have been other notable insertion demonstrations. In September 1986, a VHSIC signal conditioner was installed in an operational AN/UYS-1 signal processor and demonstrated in a series of P-3 aircraft flights. In December 1986, the Army demonstrated a VHSIC version of a portion of the Enhanced Position Locating and Recording System (EPLRS). In September 1987, the Navy demonstrated a significant improvement for the AN/SRS-1 Combat D/F system using a combination of chips from four different VHSIC contractors. Also in September, the Navy also demonstrated VHSIC circuit boards in its new standard signal processor - the AN/UYS-2 Enhanced Modular Signal Processor. On December 10, 1987, the Army successfully demonstrated an automatic target tracking system for the Abrams M1A1 tank which will substantially improve the fire control system in the tank. Details on the current insertion projects are found in Chapter II.

The first generation of VHSIC technology, developed under Phase 1, is now being produced and being used in operational aircraft. VHSIC is FLYING!

I.3 PROGRAM OBJECTIVES

The goal of the VHSIC program is to develop an advanced semiconductor technology for military use and to sharply reduce the delay experienced by the DoD in getting that technology into systems. Ideally, the introduction of new IC technology in

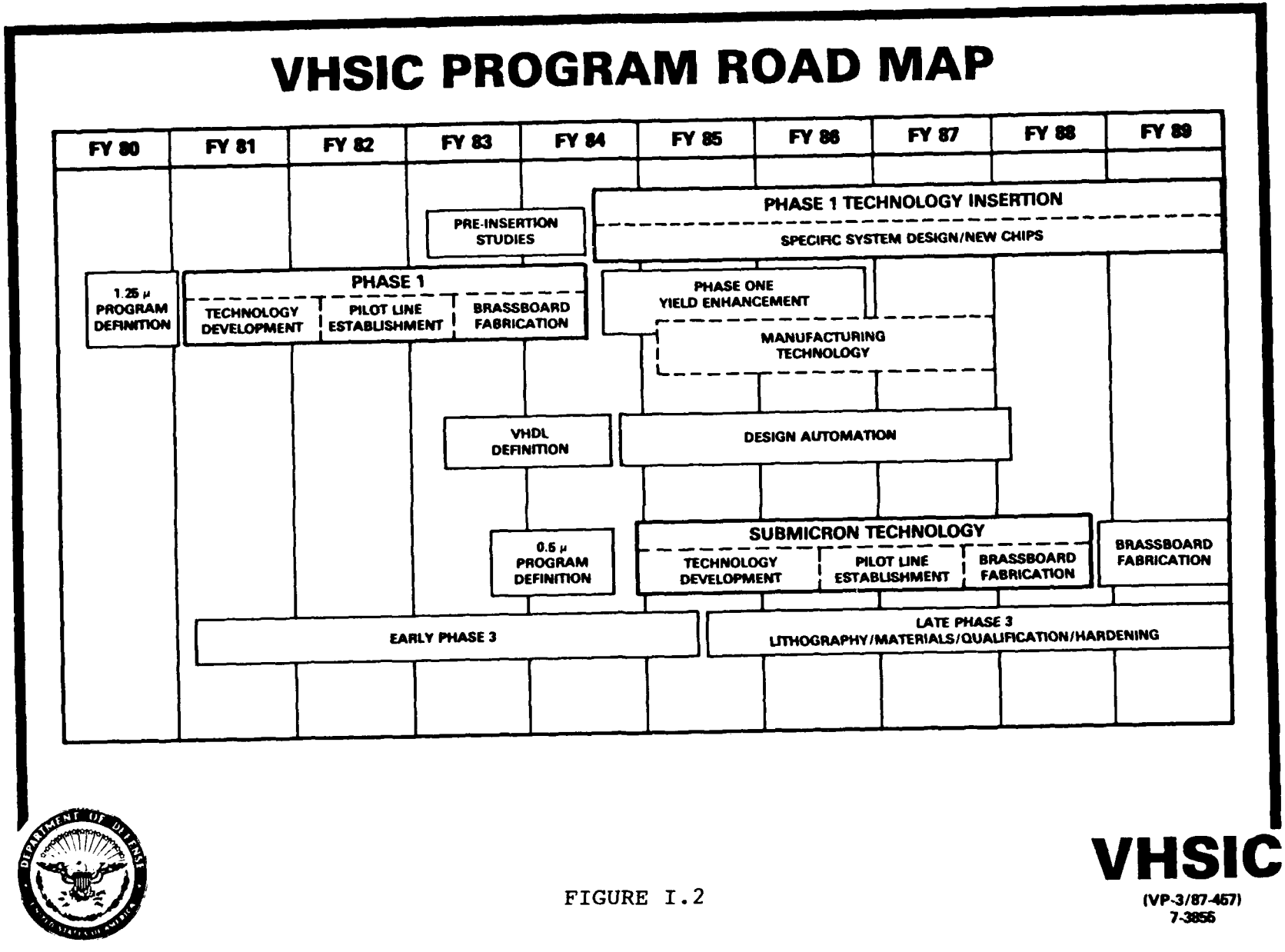

VHSIC PROGRAM ROAD MAP
FY 80
FY 81
FY 82
FY 83
FY 84
FY 85
FY 86
FY 87
FY 88
FY 89
PRE-INSERTION STUDIES
PHASE 1 TECHNOLOGY INSERTION
SPECIFIC SYSTEM DESIGN/NEW CHIPS
1.25 μ PROGRAM DEFINITION
PHASE 1
TECHNOLOGY DEVELOPMENT
PILOT LINE ESTABLISHMENT
BRASSBOARD FABRICATION
PHASE ONE YIELD ENHANCEMENT
MANUFACTURING TECHNOLOGY
VHDL DEFINITION
DESIGN AUTOMATION
0.5 μ PROGRAM DEFINITION
SUBMICRON TECHNOLOGY
TECHNOLOGY DEVELOPMENT
PILOT LINE ESTABLISHMENT
BRASSBOARD FABRICATION
BRASSBOARD FABRICATION
EARLY PHASE 3
LATE PHASE 3
LITHOGRAPHY/MATERIALS/QUALIFICATION/HARDENING
VHSIC
(VP-3/87-457)
7-3856

FIGURE I.2

the DoD should be such that its deployment coincides with, or even precedes, its appearance in the commercial market place.

In order to reach this goal the DoD must do more than solve the "catch-up" problem for one or two generations of new ICs. It is a permanent fact of life that the DoD will have only a small share of the total semiconductor market, whether measured in chips or in dollars. It is also understandable that system program managers are reluctant to commit to a system based on a new technology. The DoD has, therefore, determined that it must modify the acquisition process to recognize the short life span of a given generation of IC products by requiring system technology choices that will assure that the system has the most advanced, mature technologies when fielded and that technology upgrades are economically feasible during the lifetime of the system.

The VHSIC program has therefore placed a high priority on developing a capability within the U.S. semiconductor industry to maintain technological currency for military integrated circuits on a continuing basis.

In order to achieve the above goals, the products of the VHSIC program must meet at least the following criteria:

- o be available for procurement at least as soon as comparable commercial products,
- o have lower projected life cycle cost than current technologies,
- o have higher reliability for the same function,
- o be producible to military standards and specifications, and
- o have a short design/fabrication cycle time.

The efforts of a significant portion of the U.S. electronics industry have been marshaled to achieve these goals. The technical efforts are focused on using the best available materials, techniques, and equipment to make advanced silicon ICs. These are the only devices currently available which can solve the demanding problems of electronic signal processing, data transfer, and weapon control that arise in the operation of modern military systems. The VHSIC approaches to solving the problems of IC technology, production, and acquisition for military use are described in Chapters III, IV, and V.

I.4 PROGRAM STRUCTURE

The program activities are shown in the VHSIC Road Map in Figure I.2, and are divided into the following major areas.

- o Phase 1: In May 1981, a primary effort began with six prime contractors on the development and pilot production of VHSIC-1 silicon chips with 1.25 micron minimum feature sizes. They were also to be demonstrated in subsystem brassboards. This phase was later expanded with the addition of programs for technology insertion, yield enhancement, and for qualifying VHSIC-1 chips. The technology insertion efforts have been continued as separate programs.

- o PHASE 2: In November 1984, the program for the development and pilot line production of VHSIC-2 silicon chips with 0.5 micron minimum feature size was started. This program also called for their demonstration in subsystem modules. Three prime contracts for this phase were awarded.

- o PHASE 3 AND OTHER SUPPORTING EFFORTS: Throughout the VHSIC program, starting in 1980, a variety of efforts have been supported dedicated to building and infrastructure to support the full life cycle of VHSIC technology. Specific efforts have been undertaken to deal with advanced materials, lithography, fabrication tools, design automation software, packaging, test automation, pilot line certification, chip qualification, and radiation hardening.

Under the management of the VHSIC Program Office, a vigorous training and awareness program is being conducted. In addition, there is a growing activity in the transfer of VHSIC information and products to weapon system developers in the industrial and Government defense community. A number of companies outside of the VHSIC funded efforts have developed design and manufacturing facilities for the production of VHSIC chips.

I.5 PROGRAM STATUS

By the end of 1986, all VHSIC-1 chip development activity under the Phase 1 contracts was completed. The remaining efforts needed to make the 1.25 micron technology more readily availability for system use were production line certification and chip qualification. These Phase 1 activities have continued throughout 1987 and are discussed in Chapter II.

Technology development emphasis, during 1987, has focused on the Phase 2 submicron efforts and on the tools and software for automated design systems. Efforts leading to the insertion of VHSIC-1 products into military systems have also continued as a major activity. In addition to the insertion of VHSIC-1 products into the F-111 operational aircraft, a second major milestone was achieved when the VHDL (VHSIC Hardware Description Language used in computed aided design tasks) was adopted as an industry wide design language (IEEE Standard 1076).

The current status of the Phase 1, Phase 2, Phase 3, and the VHSIC Technology Insertion programs of the three Services is presented in the following sections of this report.

Appendix A contains DoD policy documents on technology insertion and technology security. The technical reports issued thus far and other documents pertaining to the program are referenced in Appendix B. Appendices C and D provide points of contact within the DoD and industry for different parts of the program and identifying information on all of the current and past major contracts for the various phases of the VHSIC program. The companies that have exhibited products at VHSIC conferences are listed in Appendix E. The glossary in Appendix F explains most of the acronyms used in this report.

CHAPTER II

VHSIC TECHNOLOGY INSERTION

VHSIC TECHNOLOGY INSERTION

"Technology Insertion" is the term used to describe the application in systems of any of the products developed under the VHSIC program - hardware, software, design tools, or standards. The VHSIC products can be used in the design of a new system, in the redesign of an older one, or in the maintenance and improvement of an existing one. Technology insertion constitutes one of the basic goals of the VHSIC program. Since it necessarily involves the linking of "high tech" with real military applications that will become operational systems, it also constitutes one of the more difficult problems that confronts the DoD.

System managers are faced with the necessity of staying within acceptable bounds of risk to their program budget and schedule even though they are aware that by introducing a new technology into their systems they could gain substantial benefits in performance and life cycle cost. In addition, system procurement regulation and military standards may directly or indirectly discourage the use of new technology. As one major system program manager has recently put it,

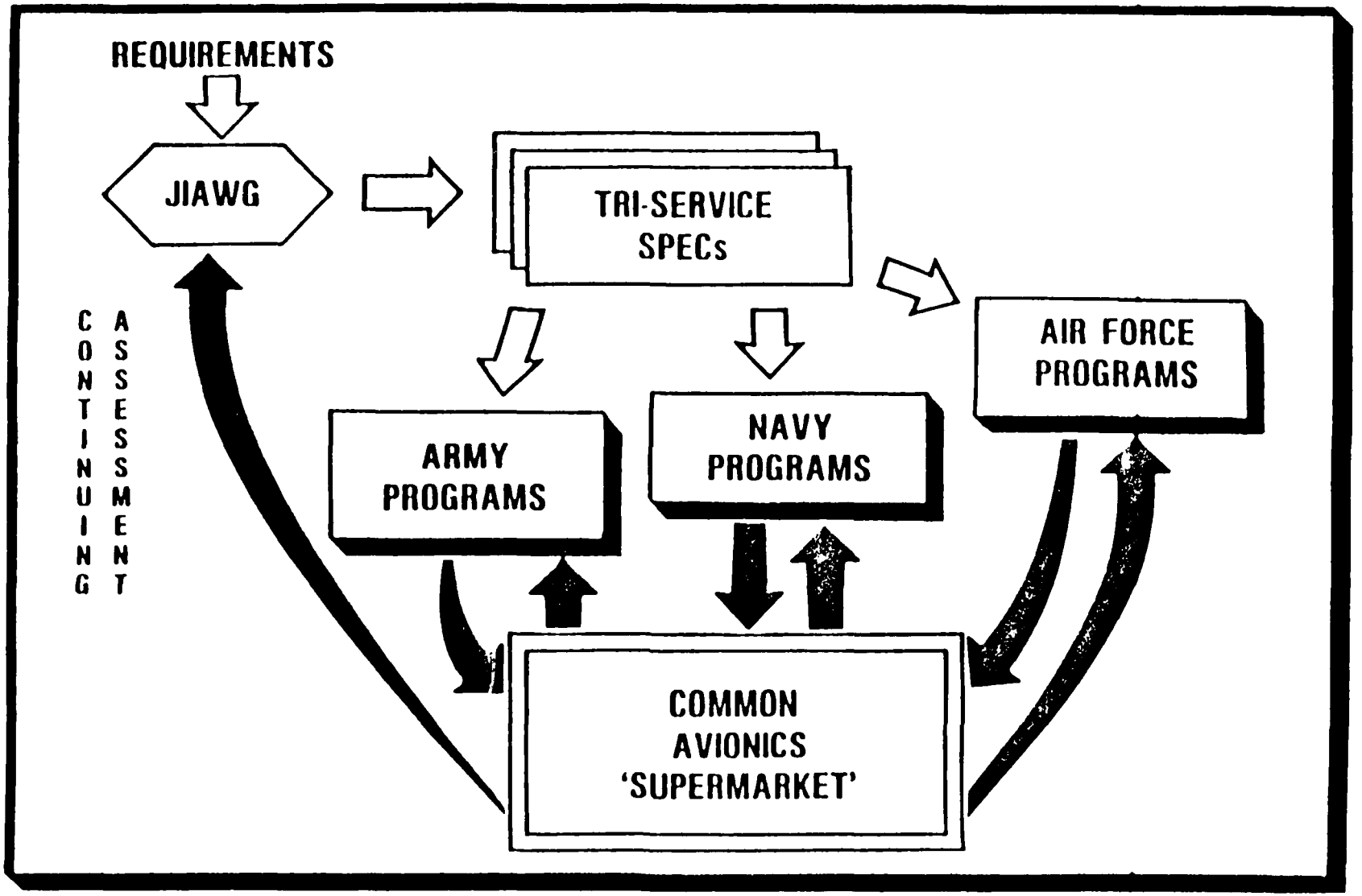
> "If such technology had been available in 1983, we could have designed a lighter, less expensive (system). Because of the potential cost benefits, (our system) application should be strongly considered for the brassboard VHSIC demonstration scheduled for 1989. . . . . In addition to developing sophisticated devices, the VHSIC . . . . program must develop reliable, stable processes for producing the devices. . . . . Qualified processes must be in place at the time the device designs are committed to production! "

The VHSIC program has met this problem by supporting a substantial number of insertion projects described below. These projects have been selected by the three Services to demonstrate that VHSIC works, that VHSIC is available, that VHSIC is beneficial. The benefits become manifest in different ways depending on the application: increased performance, increased reliability, enhanced maintainability, reduced acquisition costs, or reduced life cycle costs.

The Congressional/DoD initiative for common avionics development will provide a strong stimulus for the insertion of VHSIC products into aircraft systems. This initiative is being carried out under the Joint Integrated Avionics Working Group (JIAWG). As shown in Figures II.1, II.2, and II.3 the result will be a coordinated avionics specification for all three Services, a common avionics architecture, and a family of common VHSIC modules for all avionics functions.

Sections II.1 - II.3 summarize the VHSIC insertion programs in the three Services which are co-funded by the VHSIC Program Office. Section II.4 lists additional insertion programs, which are not directly funded by the VHSIC Program Office, but are applying the advanced VHSIC microelectronic technology in system developments. Collectively they reflect only a small fraction of the growing activity by DoD contractors in the introduction of VHSIC products and technology into military systems.

COMMON AVIONICS DEVELOPMENT



JOINT INTEGRATED AVIONICS WORKING GROUP (JIAWG)

FIGURE II.1

ADVANCED AVIONICS ARCHITECTURE

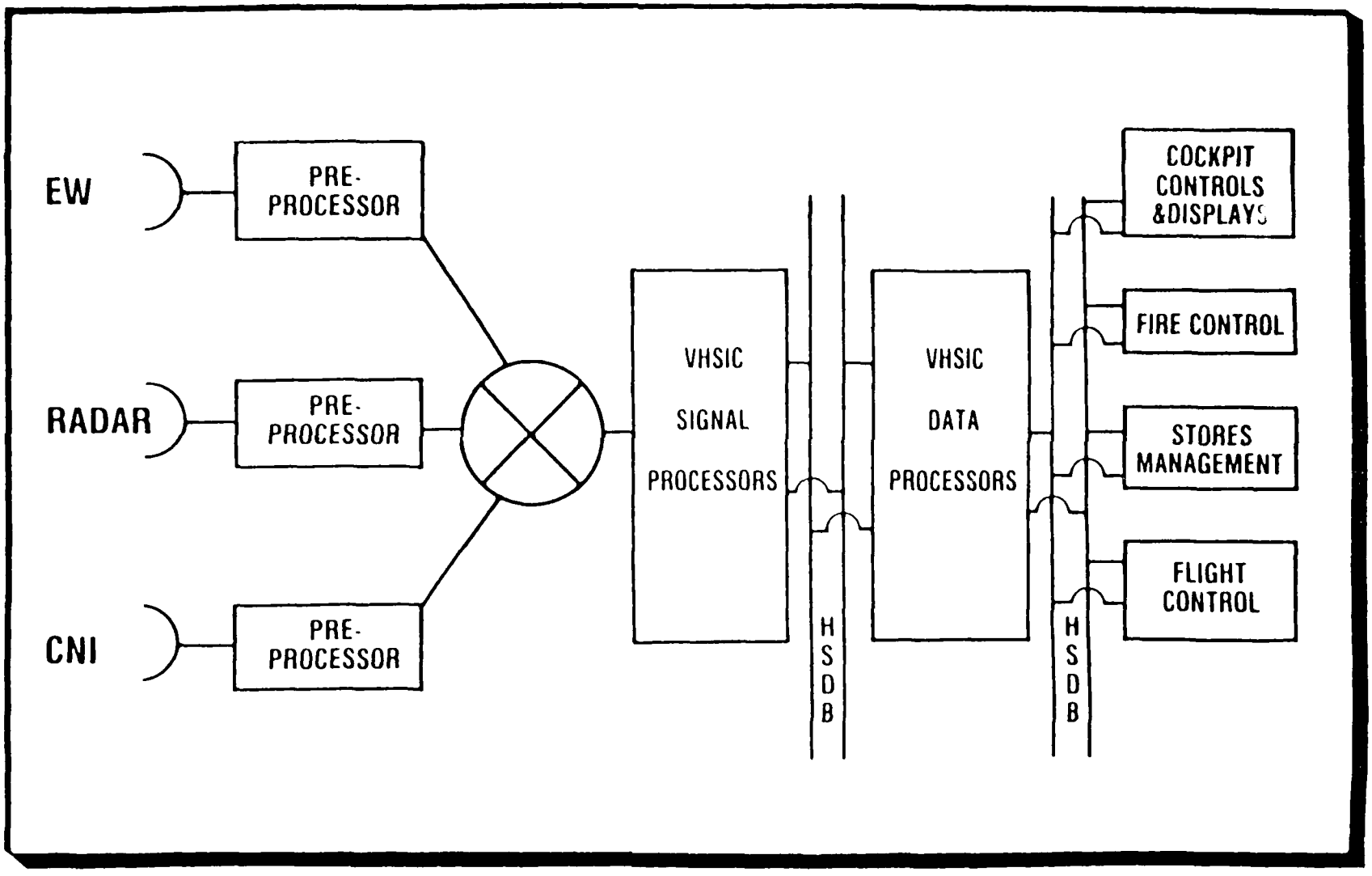


FIGURE II.2

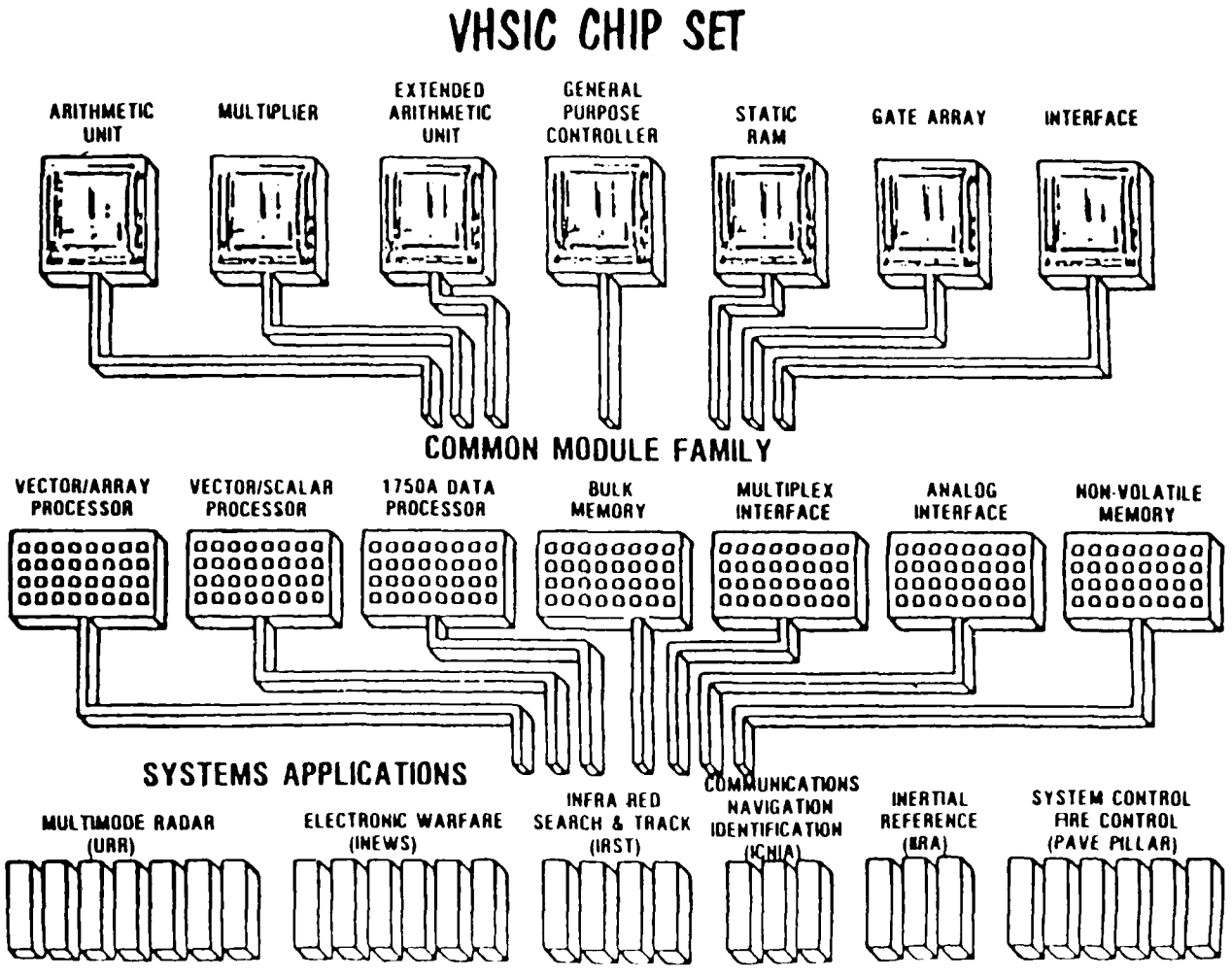

VHSIC CHIP SET
ARITHMETIC UNIT
MULTIPLIER
EXTENDED ARITHMETIC UNIT
GENERAL PURPOSE CONTROLLER
STATIC RAM
GATE ARRAY
INTERFACE
COMMON MODULE FAMILY
VECTOR/ARRAY PROCESSOR
VECTOR/SCALAR PROCESSOR
1750A DATA PROCESSOR
BULK MEMORY
MULTIPLEX INTERFACE
ANALOG INTERFACE
NON-VOLATILE MEMORY
SYSTEMS APPLICATIONS
MULTIMODE RADAR (URR)
ELECTRONIC WARFARE (INEWS)
INFRA RED SEARCH & TRACK (IRST)
COMMUNICATIONS NAVIGATION IDENTIFICATION (ICNIA)
INERTIAL REFERENCE (IRA)
SYSTEM CONTROL FIRE CONTROL (PAVE PILLAR)

FIGURE II.3

II.1 ARMY

II.1.1 Enhanced PLRS User Unit (EPUU)

The PLRS (Position Location and Reporting System) will provide Army ground troops with a system for battlefield tactical data transmission. A VHSIC version of the EPUU is being developed which will have a three-fold increase in signal throughput. The increased capacity is needed to meet the growth anticipated in the volume of battlefield data. Hughes Aircraft has designed and fabricated a VHSIC chip set that will update the Signal Message Processor (SMP) module in the EPUU. There are also plans to design a second chip set for a second module. These two VHSIC modules would also reduce both the logistics and acquisition costs associated with the planned production of more than 20,000 EPUUs. Preliminary Government estimates indicate that approximately $100 million can be saved in acquisition and life cycle cost by using VHSIC components.

On December 11, 1986, the Army demonstrated fully functional VHSIC-1 devices which transferred messages between a brassboard VHSIC EPUU and standard units.

During 1987, the VHSIC encoder/decoder chip was successfully demonstrated and became available for system integration (reference II.1). All VHSIC and non-VHSIC components developed for the brassboard EPUUs were completed, tested for functionality, and integrated into the brassboards. Two of the three cards required for the SMP module were fabricated and tested. Initial firmware and software development has been completed and final firmware/software upgrading is planned for 1988.

The VHSIC prototype modules are scheduled for field testing starting in November 1988. These modules will then be integrated into fifteen prototype VHSIC EPUUs and will be field tested in early 1989.

II.1.2 Advanced Tactical Helicopter (ATH) Mission Computer

During 1985 and 1986, system design work on advanced cockpit and mission equipment for the LHX helicopter (now called the Advanced Tactical Helicopter) included a task to provide preliminary designs for a VHSIC Mission Computer. These design efforts were jointly funded by the LHX Program Office and the VHSIC Program Office. See references II.2 through II.6.

Using five preliminary VHSIC Mission Computer designs as a base, each of two ATH contractor teams has, during 1987, continued to design the VHSIC Mission Computer. The two teams are headed by Boeing and McDonnell-Douglas. These efforts include formal laboratory demonstrations of selected computer features, e.g., 1750A data processor, signal processor, sensor data distribution, high speed data bus, video processor, etc.

The detailed VHSIC Mission Computer design efforts are expected to reduce technical risk to an acceptable level so that contracts for ATH DEM/VAL can be awarded in 1988 now that the program has been reviewed and redefined. Development and demonstration of the ATH VHSIC Mission Computer will continue in DEM/VAL through formal system integration and flight testing.

II.1.3. TOW Automatic Target Tracker

The requirements and goals of the TOW (Tube Launched, Optically Tracked, Wire Guided) program are:

a. dual, simultaneous, fully automatic flight demonstration using a brassboard VHSIC launcher,
b. increased rate of fire, greater accuracy, simplified training, and
c. demonstrated readiness for FSED.

The guidance set will perform both the existing missile tracking and guidance function and a new automatic multiple target tracking function.

Two early VHSIC trackers were built and tested by Texas Instruments and Hughes Aircraft. The brassboard phase was awarded to Texas Instruments in 1985. System design and some fabrication and software development were completed by the end of 1986.

During 1987, the TI VHSIC components have been delivered, and the brassboard fabrication has been completed. The system is now being simulated and tested. Software development and integration was 95% complete by December 1987 and is expected to be finished by March 1988.

The final system integration, preliminary tests, and ten missile flight demonstrations are scheduled for the first half of 1988. After successful demonstration, the automatic target tracker technology will be available for use in the TOW, the Advanced Anti-Tank Weapon System, and the tri-Service Hyper-Velocity Missile projects. See reference II.7.

II.1.4 FIREFINDER Radars

This program will develop a high performance VHSIC signal processor for the FIREFINDER radar systems. The processor will permit a significant reduction in size and improvement in performance and survivability of the FIREFINDER radar systems.

The FIREFINDER radars detect sources of hostile mortar, artillery, and rocket fire and accurately compute their location for the direction of counterfire. The use of VHSIC technology in the signal processor will significantly improve the performance of the weapon location computation, provide classification of the weapon type, and enhance the system performance against EW threats. The VHSIC processor reduces the power and parts count by 60%, which makes it a key subsystem in evolving toward a single vehicle FIREFINDER system. Reconfiguration of the radar on a single vehicle will reduce the crew size from eight to four personnel for the AN/TPQ-36 version of the radar and result in a projected life cycle cost savings of $430 million.

At the beginning of 1987, the processor architecture was being designed, and its performance was being analyzed using computer simulation. Four new VHSIC chips are being designed to implement the architecture. Fabrication has begun on the processor brassboard assembly.

During 1987, the processor module design was completed and simulated. The design and simulation of the four new VHSIC chips (a multiplier/accumulator, a registered arithmetic logic unit, an array element controller, and an external interface unit) were completed. These CMOS ICs have from 25,000 to 38,000 gates, and were fabricated by LSI, Inc. Software for the processor is being written and validated. Four VHSIC modules were fabricated and integrated along with ten other non-VHSIC modules in a demonstration brassboard which is presently in operational testing.

In 1988, it is planned to integrate the brassboard into an existing FIREFINDER radar for test and evaluation.

II.1.5 Combat Vehicle VHSIC Processor

The Armament Research and Development Center (ARDEC) is developing a VHSIC fire control processor to improve the performance and simplify the life cycle management of combat vehicle data processors. This fire control processor will consist of standardized processing modules which will perform all of the data processing, input/output, communication, and power conditioning functions required for future fire control applications. The modularity of the processor provides the needed flexibility for insertion into all combat vehicles. Applications include the Armored Vehicle Family and block improvements to the M1A1 tank and the Bradley Fighting Vehicle. Texas Instruments is the VHSIC brassboard contractor with General Dynamics as the system integrator. A block diagram of the system is shown in Figure II.4.

In June 1987, the VHSIC brassboard was successfully demonstrated in the laboratory. The brassboard has been integrated into an M1A1 tank gunner's sight by General Dynamics and was demonstrated in the field on December 10, 1987.

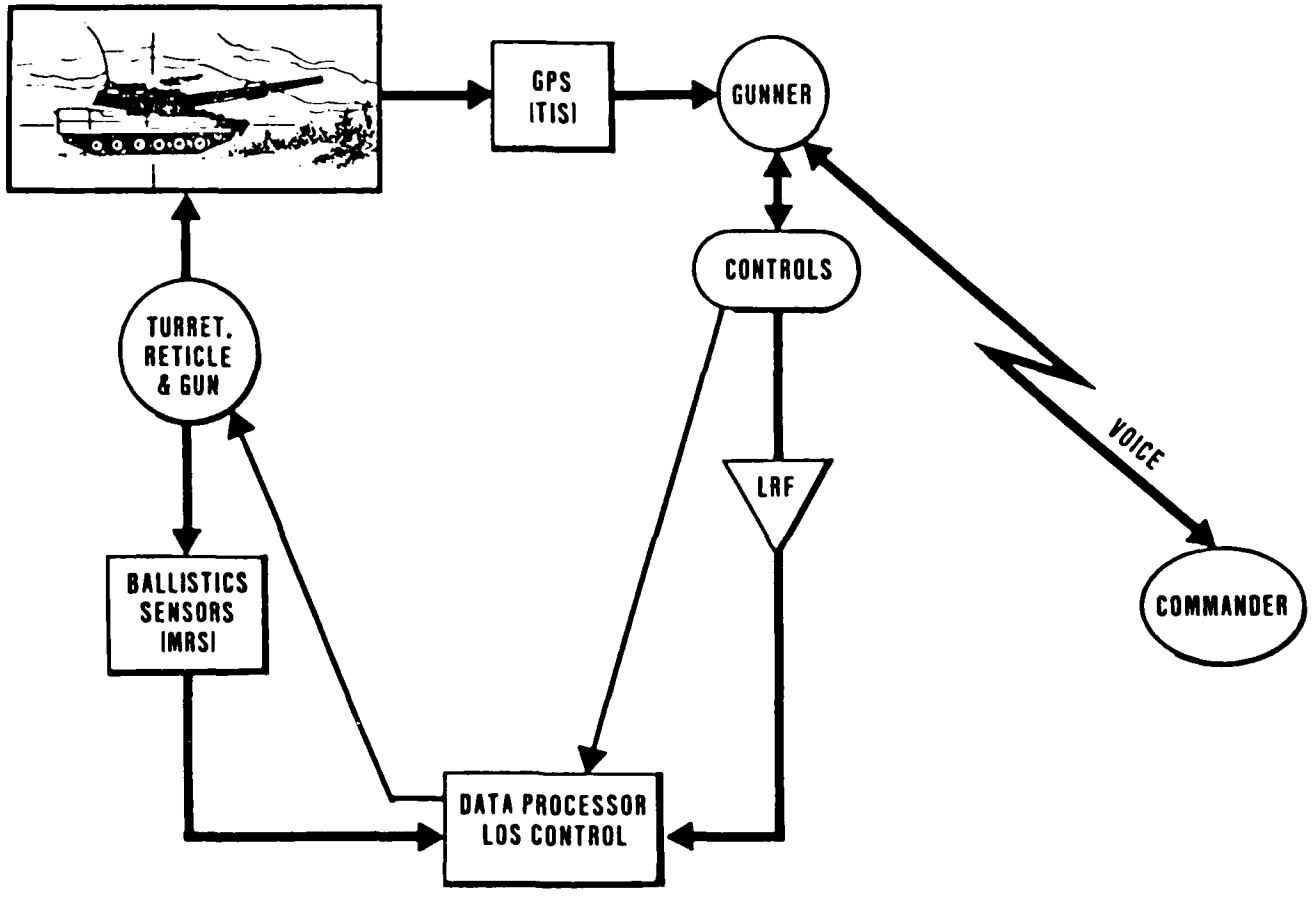
In September, 1987 a contract was awarded for development and fabrication of a Combat Vehicle Integrated Processor based on the positive results of this VHSIC insertion program.

II.1.6 Miniaturized Electronic Direction Finder Location Indicator (MEDFLI)

The goal of the MEDFLI program is to produce small, lightweight EW payloads for airborne and ground applications that can handle the severe threat emitter environment of the 1990s and beyond. The contractors for this program are ESL Corporation and RCA. The goal of this insertion project is to improve the throughput and reliability of the MEDFLI signal processor and to develop a special purpose Threat Association Module (TAM) for unique EW processing applications. See references II.8 and II.9.

Fabrication of the TAM began early in 1986. During 1987, the TAM Module was completed and successfully demonstrated, and a contract for fabrication of the VHSIC Modular Adaptive Signal Sorter (VMASS) was awarded.

Plans for 1988 and beyond are to complete the VMASS fabrication, then test and integrate the VMASS with the TAM and evaluate the total system performance.



COMBAT VEHICLE PROCESSOR - M1A1 TANK

FIGURE II.4

II.1.7 HELLFIRE Imaging Infrared Seeker

The Imaging Infrared (IIR) seeker for the HELLFIRE Fire and Forget missile system requires a high data throughput with a low power, small, light weight processor. The use of VHSIC technology in the seeker and processor will result in a reliable, low cost seeker with a long shelf life and a built-in test capability. The programmable/modular nature of the VHSIC components will accommodate future upgrades of missile capability. Development contracts for a VHSIC processor for the seeker were awarded in September 1985 to Texas Instruments and Ford Aeronutronics.

At the beginning of 1987, development of the VHSIC processor hardware for insertion into the HELLFIRE IIR seeker was well under way. However, the Joint Service Seeker program, which was to furnish the sensor hardware for insertion into the HELLFIRE system, had been terminated.

The HELLFIRE contracts are being modified to include the fabrication of a seeker head utilizing residuals from the terminated Joint Service Seeker program. The resulting seeker and processor will make full utilization of VHSIC technology and are expected to be completed during 1988. See references II.10 through II.12.

II.1.8 Multirole Survivable Radar (MRSR)

The Multirole Survivable Radar is being designed to make the operation of air defense artillery more effective in a combat environment that includes anti-radiation missiles and electronic countermeasures.

Westinghouse Corporation and Raytheon Company, are designing pre-production prototypes of a ground based radar to handle the Forward Area Air Defense requirements. VHSIC offers advanced signal processing performance within the limited space and power available in a single ground vehicle. Such a configuration can be quickly deployed with minimum manpower and has significantly improved reliability.

The MRSR VHSIC technology insertion effort was started in January 1987. Raytheon and Westinghouse are currently analyzing the reductions in cost, chip count, module count, and improvements in reliability.

Plans for 1988 and beyond are to complete the system analyses and start to assemble, test, and demonstrate VHSIC hardware. The MRSR will be delivered in 1989 with production following as soon as possible.

II.1.9 Army Command and Control System (ACCS)

The insertion of VHSIC technology into the ACCS project was started in October 1987 with a contract to TRW. The first six months of effort are being devoted to a study and set of recommendations for the application of VHSIC technology to the product improvement of the ACCS common hardware. A final report on the study is expected in September 1988.

II.2 NAVY

II.2.1 AN/UYS-2 Enhanced Modular Signal Processor (EMSP)

The EMSP is the Navy's next generation standard signal processor. This system is being designed to meet the Navy's air, sea, and shore signal processing requirements through the 1990s in sonar, radar, electronic surveillance, and communications systems. The AN/UYS-2 is constructed of Standard Electronic Modules (SEM) and is designed to be interoperable with other standard Navy computers.

AT&T performed the system integration effort for VHSIC insertion. Honeywell, as subcontractor, has developed the chips, circuit card assemblies, and SEM modules for the demonstration model.

VHSIC-1 (1.25 micron) technology was used in the development of a floating point arithmetic unit (FPAU). Three chips were developed for the FPAU: a floating point multiplier with 10,030 gates, a register file arithmetic logic unit (RALU) with 12,863 gates, and a 32-bit FIFO memory with 7,142 gates. Functional verification of the chip set was completed in July 1986, and the brassboard was then assembled. There are five chips per set, and each EMSP will use up to twenty sets.

In April 1987, the interoperability and signal processing capabilities of the system were demonstrated to the Navy EMSP team. In September 1987, SEM cards were inserted into the EMSP environmental prototype model and demonstrated while the system processed a sample of tactical data. A detailed analysis shows that the floating point AU has 46% more throughput than the fixed point AU on a comparable task basis.

EMSP laboratory development models incorporating the VHSIC chip set will be delivered to the Navy beginning in January 1988. See references II.13 and II.14.

II.2.2 MK-50 Advanced Lightweight Torpedo (ALWT)

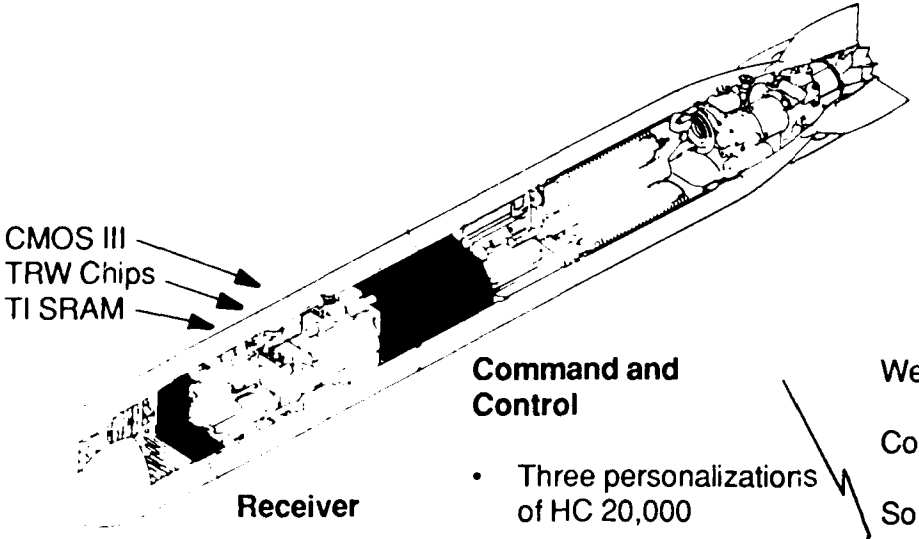
The MK-50 ALWT is being developed by Honeywell as the Navy's next generation torpedo designed to counter the continually evolving Soviet submarine threat. It will be the primary ASW weapon for air and surface platforms as well as the principal submarine standoff weapon.

As illustrated in Figure II.5, VHSIC insertion provides significant benefits to the MK-50 system: a saving of 5 inches in length and 40 pounds in weight which could be allocated to a larger warhead; increased reliability by having 1,300 fewer components and 15,000 fewer solder joints; power reduction of 16 watts; and 540 square inches less circuit board area. The overall result is a reduction in life cycle costs because of better reliability and maintenance characteristics with the same or better performance parameters. By adding the increased capability of a single board embedded AN/AYK-14 computer (which is a separate VHSIC insertion program described below) the size and weight of the electronics section of the torpedo would be reduced even more.

A variety of VHSIC Phase 1 chips from different manufacturers are being used in the digital receiver and in the command and control subsections. The TRW microcontroller chip, the TRW address generator chip, the TI SRAM, and a number of ETA/Honeywell gate array personalizations are being used.

VHSIC Payoff to MK-50

Honeywell



Command and Control

- Three personalizations of HC 20,000

Receiver

- VHSIC A/D converter
- Two personalizations of HC 20,000
- TRW chips (two)
- TI SRAM

Weight	16 lb	Benefit Reduction
Component Count	1,300	
Solder Connections	15,000	
Electronic Packaging Length	2.2 in.	
Power	16W	

Weight	40 lb	Benefit Reduction with Repackaging
Electronic Packaging Length	5 in.	

FIGURE II.5

87-CRV-4364

During 1987, all the required gate arrays were designed and fabricated. A multilayer board for the memory functions was completed and tested. A multilayer board for the remaining command and control functions is being designed. The receiver breadboard will be evaluated in 1988. Technical and operational evaluation of the Honeywell hardware has been scheduled for 1988-89.

II.2.3 HF/EHF Communications: VHSIC Terminal Brassboard (VTB)

The VHSIC Terminal Brassboard (VTB) is a joint Navy/Air Force effort to assess the ability of VHSIC technology to meet the requirements for complex signal processing for communications. The Air Force VTB effort is further discussed in section II.3.5. The Navy units being produced will process EHF and High Frequency Anti-Jamming (HF/AJ) communication signals to determine the potential benefits of VHSIC technology in future terminal designs. The new MILSTAR EHF satellite system will use complex, highly robust waveforms to provide the U.S. with minimum essential survivable communications capability. The HF/AJ subsystem uses improved HF waveforms for increased anti-jam performance.

VTB demonstrates the combination of these two complex systems into a single, common, processing architecture. The VTB system is designed to simultaneously support various combinations of EHF and HF/AJ channels. Projections for production versions of the VTB architecture indicate reductions of up to 75% in size, weight and prime power over current EHF and HF/AJ designs. Significant improvements in reliability, maintainability, and long-term system costs are also expected. These benefits will make it possible to have EHF and HF/AJ communications on platforms such as submarines and manpack terminals where very limited resources are available.

The VTB is being developed by TRW. The design and fabrication of the chips for the VTB were completed during 1987, making extensive use of the TRW Phase 1 chip set and VHSIC chips developed under the VCP insertion program discussed below. The chips include a FFT set, a convolutional decoder, and a configurable gate array.

Fabrication of the first VTB unit will be complete in early 1988. Demonstration and delivery are scheduled for late 1988. The VTBs will then be further evaluated for insertion opportunities at a testbed facility under development at NOSC, San Diego.

II.2.4 AN/AYK-14(V) Standard Airborne Computer

The AN/AYK-14 is the Navy standard airborne computer. It is a general purpose computer that is comprised of a family of modules; the newest of these is the VHSIC Processor Module. This computer is functionally and physically partitioned into replaceable modules to provide wide operational flexibility. The AN/AYK-14 is used in most Navy aircraft as well as in shipboard and land based applications. Major users include the MK-50 torpedo and the E-2C, EA-6B, P-3C, F-14D, A-6F, EP-3E, AV-8B, F/A-18, and SH-60B aircraft. Production of 12,000 to 14,000 units is expected by 1995.

Control Data Corporation was awarded a contract in 1986 to develop the VHSIC Processor Module (VPM). Unisys is the planned second source supplier. The module will plug into existing fleet equipment replacing as many as seven existing modules. Performance is increased over existing units by 5-10 times and memory capacity by 2-4 times. The mean time to failure of the module is expected to be 9000 hours. This will

significantly increase the reliability of the entire AN/AYK-14. The module features a 32K by 16 bit word high performance cache memory and 1 megabyte of local memory. The maximum throughput rate is 6 MIPS. Two modules can operate simultaneously in a dual processing mode on a single problem at a 10 MIP rate.

During 1987, five VHSIC 20,000 gate CMOS chips using standard cells have been designed. One of these chips - the I/O Adapter - accommodates a variety of bus interface types with minor modification. The module has been designed both in the SEM-E format and the 3/4 Air Transport Regulation (ATR) format for new applications and for retrofit into existing full ATR or SEM-E chassis. With this flexibility the VPM can meet the requirements of existing platforms and yet be compatible with evolving DoD standard module and bus interface requirements (i.e. SEM-E and PI-Bus).

Twenty two modules will be delivered to the Navy for land based brassboard testing and for testing on board an EA-6B aircraft commencing in December 1988. Baseline production will start in 1990, and full production is expected to begin in 1991. The F-18 and F-14 program offices are scheduling VPM production to phase in with their expanding requirements in the early 1990s.

II.2.5 VHSIC Communications Processor (VCP)

The objective of this program is to demonstrate VHSIC performance in a communications processor. The VCP consists of a signal processor in SEM-E format board technology and a preprocessor using universal matched filters also in SEM-E format. The architecture of the signal processor being developed under this program is common to that of the TRW VHSIC Phase 1 EW brassboard signal processor. In addition, the planned production version is common with that of the HF/EHF terminal and ICNIA programs. Each of the modules makes use of the TRW VHSIC Phase 1 chips.

In the VCP, the preprocessor will digitize baseband analog waveforms from the HF radios and the signal processor will perform the digital filtering functions. In addition, the VCP preprocessor brassboard, common to the tri-Service ICNIA program's brassboard preprocessor, will also demodulate GPS and JTIDS wideband signals and transfer the compressed bandwidth data to the signal processor for demodulation and tracking.

Navy and Air Force versions are being assembled for delivery in 1988.

II.2.6 AN/SRS-1 Combat Direction Finder

This program was based on a Sanders Associates IR&D study which demonstrated a vector product calculator (VPC) using VHSIC components. It was initiated in November 1985 with the objective of production in 1988.

In February 1987, the initial phase was completed (thirteen months after the start of the contract) with the design, development, and demonstration of a brassboard model of the Vector Product Calculator (VPC). It showed that the selected Phase 1 VHSIC chips from IBM, TRW, TI and Motorola can be integrated with conventional logic components to perform the design goals. A second phase of the program was initiated in March 1987 to replace all non-VHSIC components with four different gate array designs plus three conventional chips. Three conventional chips, six gate arrays, and thirty-six VHSIC components will then comprise the pre-production VPC circuit card.

The construction, laboratory testing, and at-sea testing of this card for insertion in the AN/SRS-1 system is scheduled for 1988 and initial production for 1989.

II.3 AIR FORCE

II.3.1 AN/ALQ-131 Electronic Countermeasure Pod

The AN/ALQ-131 is an airborne pod-mounted system capable of countering threat radars. A VHSIC Transmit Control Assembly (VTCA) is being developed for retrofit into this electronic warfare (EW) pod. The major goals are to improve the system MTBF by 25%, reduce the mean time to repair (MTTR) by 50%, provide up to 50% growth space for future capabilities by reducing the printed wiring assembly board count, provide a common VTCA for all RF bands, and provide an extensive maintenance and diagnostics system (MADS) capability for each VTCA.

Development of the VTCA by TRW began in September 1983, and prototype specifications were delivered in March 1984. The first insertion of VHSIC into an operational system took place in December 1985 with a demonstration of the VTCA in the AN/ALQ-131.

Accomplishments for 1986 included the delivery, flight testing, and laboratory testing of the Block I prototype. Initial flight test of the pod occurred on July 17, 1986 on an A-10 aircraft at Eglin AFB.

During 1987, the Air Logistics Center at Warner Robins AFB assumed management of this program. It is currently planning to contract for the development and qualification of a "preferred spare" VHSIC TCA that is compatible with both the Block I and Block II AN/ALQ-131 pods. The details of the prototype VHSIC TCA design were used to develop the specification. Contract award is anticipated by the 4Q88. Operational capability of the AN/ALQ-131 with a VHSIC TCA preferred spare is projected for 1992.

II.3.2 Autonomous Guided Weapon

The Autonomous Guided Weapon is a standoff weapon which employs an infrared seeker for high value target acquisition (IRHVTA) and tracking. It uses techniques which provide an autonomous acquisition and tracking capability, thus eliminating the need for designation and data link information throughout the flight of the missile. The VHSIC technology needed to do this includes a 1750A general purpose computer and the Multimode Fire and Forget signal and array processor.

A design study began at Texas Instruments in September 1983 and ended in April 1984. The brassboard development was contracted with TI in September 1984, and the IRHVTA high speed test effort began in January 1985. Work continued in 1986 on the brassboard fabrication and demonstration effort, and also on the IRHVTA high speed testing.

During 1987, the work has continued on the brassboard design and fabrication. A brassboard laboratory demonstration is scheduled for the 1Q88. Infrared seeker data

will be fed into the VHSIC processor brassboard in real time to perform the same algorithms that have been demonstrated on a similar processor using LSI technology.

Along with the reduction in weight, power, and volume, there is an anticipated 4 to 5 times increase in system computational speed. Competitive award for the Autonomous Guided Weapon FSD program is anticipated in the 3Q88 using VHSIC technology.

II.3.3 Common Signal Processor

IBM started in November 1984 to develop a modular common signal processor (CSP) based on VHSIC technology. It can be configured and programmed to satisfy a wide variety of applications such as high performance radars, secure communication, anti-submarine warfare, and electronic warfare. The program will demonstrate the feasibility of a common signal processor using VHSIC and furnish test results on issues of functional partitioning, module definition, standardization, and packaging software development.

The eleven VHSIC chips needed to meet the CSP requirements include a 1750A computer, static RAMs, and a number of custom chips designed from the IBM standard cell library. A 1.0 micron CMOS technology was chosen for the fabrication technology. A logistics support analysis was completed in September 1986. A demonstration/validation effort for the CSP began in mid 1986.

During 1987, work continued on the design, fabrication, and testing of the eleven 1.0 micron chips and of the demonstration modules. Brassboard deliveries are scheduled for July 1988.

II.3.4 MIL-STD-1750A Computer

This program, also referred to as the VHSIC Avionics Modular Processor or VAMP Program, will result in processor modules implementing the MIL-STD-1750A instruction set architecture. The computer is designed to operate at 3 million instructions per second and is based on the Pave Pillar common module concept. The VHSIC chip set includes static RAMs and VHSIC gate arrays. There are a total of 21 new chip designs proposed.

The program began with parallel contracts with TRW/DELCO and Westinghouse. During 1987, Westinghouse was selected to continue the effort to demonstrate an advanced development module.

Breadboard modules for functional verification were delivered in 1987, and all of the final design VHSIC chips are in various stages of fabrication and testing. Delivery of the advanced development module is scheduled for October 1988.

II.3.5 MILSTAR Terminal/Modem Processor

MILSTAR is an EHF satellite communication system. The use of VHSIC technology will provide improved performance with reduced life cycle cost. It will become possible to install the MILSTAR terminal on platforms with space and weight restrictions that otherwise preclude such installation. This is a joint effort with the Navy's HF/EHF program discussed in Section II.2.3.

The program started at TRW in 1984. The processor uses the preprocessor portions of the EHF on-board brassboard plus additional Phase 1 convolutional decoder, Fast Fourier Transform, and multiplier/accumulator chips. Detailed hardware design was completed early in 1986.

The detailed software design was completed in February 1987, and the brassboard fabrication was completed in December. Integration of the hardware and software will be done in February 1988. Demonstration of the brassboard is scheduled for June 1988, with delivery to the Services for testing and evaluation in July and August 1988.

II.3.6 Speech Enhancement Unit

The Speech Enhancement Unit (SEU) is an advanced development speech processor that removes tone, impulse, and wideband noise from speech channels. The SEU greatly improves the intelligibility of voice communications for both human operators and speech recognition equipment. VHSIC technology is critical to the implementation of SEUs of a practical size and affordable price. The increased throughput and speed of VHSIC will also provide better performance.

The design of a brassboard was begun in 1985 by Westinghouse and Queens College (City University of New York). Fabrication will begin when the design is completed and approved. The brassboard is scheduled to be completed, tested and evaluated by March 1988. Design of the field model will follow.

II.3.7 VHSIC Programmable Signal Processor (VPSP)

The AN/APG-68 is an airborne fire control radar which provides air-to-air target detection and tracking on the F-16 aircraft. A VHSIC PSP will greatly improve the operational characteristics of the radar such as tracking range, target discrimination, and multiple target tracking. The VHSIC technology being designed into the VPSP includes a 1750A chip set, 64K static RAMs and numerous personalizations of a Westinghouse 10K gate array. A contract was awarded to Westinghouse in 1985.

During 1986 and 1987, nineteen different gate array personalizations were fabricated. The VHSIC chips are being supplied by National Semiconductor and one or more second source suppliers. The brassboard and the hardware descriptions are scheduled to be completed in May 1988. Full scale engineering development with production options is expected to start in late 1988.

II.3.8 E-3A Signal Processor

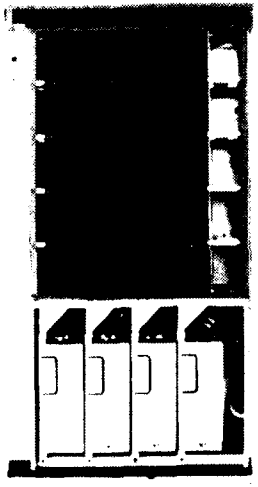
The E-3A Sentry aircraft is the Air Force Airborne Warning and Control System (AWACS). This insertion effort is aimed at improving the performance and logistics characteristics of the signal processor used in the surveillance radar on board the SENTRY. The benefits of using VHSIC are shown in Figure II.6.

A system insertion study was completed in 1983 by Westinghouse. The design phase was completed in 1985. A contract award for the hardware phase was made in August 1986.

Impact of Electronics on Warfare

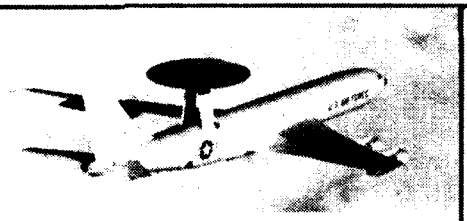
Airborne Surveillance

Present E-3 Processor



Performance	35 MCOPS
Power	3.4 kW
Boards	220
MTTR	22 min

86-3463-1



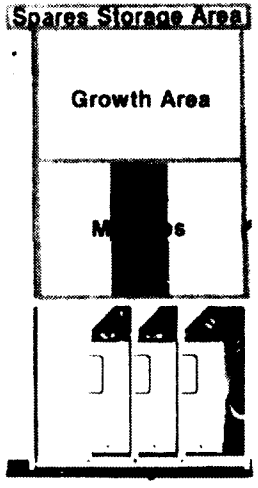
Improvements

Mission Adaptability
- Programmable

Fewer Parts
- Higher Reliability

Facilitates
- Longer Range Detection
- Detect Smaller Targets

VHSIC E-3 Processor



Performance	80 MCOPS
Power	1.1 kW
Board Pairs	7
MTTR	10 min

VHSIC

FIGURE II.6

The interface design was completed in March 1987. Westinghouse plans to merge the hardware and software by the end of 1988 and complete testing of the brassboard in March 1989.

II.3.9 VHSIC TTL Gate Array

Numerous Air Force systems contain older transistor-transistor-logic (TTL) devices which are rapidly becoming unavailable. The result is a generation of front line weapon systems that will soon be unsupportable. A majority of the TTL microcircuits can be replaced by a custom VHSIC TTL gate array.

A contract was awarded to Honeywell in September 1986. During 1987, the gate array design was completed and sample devices have been fabricated including a number of personalizations. The initial personalizations will be evaluated early in 1988.

II.3.10 F-15 Central Computer

The F-15 Central Computer controls pilot displays, weapon launch solutions, and the aircraft G-load warning system. The VHSIC 1750A computer will form the basis for this program.

The project was originally approved by the VHSIC Program Office in February 1985 as a candidate program for VHSIC insertion funding. Several management options and alternate acquisition strategies have been identified. Service funding levels and the acquisition strategy will be decided in FY88.

II.3.11 Logistics Retrofit Engineering For Microelectronics

The Logistics Retrofit Engineering (LRE) program was initiated by the Air Force to solve the growing problem of replacing special ICs that are out of production. One approach being followed is to re-engineer the system with VHSIC technology which improves logistics support through decreased procurements cost and increased reliability.

Design, fabrication, and testing were completed this year on the Rockwell VHSIC replacement for the F-111 Digital Signal Transfer Unit (DSTU). The mean time between failure (MTBF) of the original F-111 DSTU card was 40 hours, and many of the components on this card were no longer being produced. The new VHSIC F-111 DSTU card not only costs less to acquire ($2000 compared to $24,000 for the old card), but now incorporates built-in-test features and has an improved reliability of 5000 hours MTBF. The form, fit, function VHSIC replacement is currently operational as a preferred spare in the F-111 D aircraft.

II.3.12 Generic VHSIC Spaceborne Computer (GVSC)

The goal of this program is to develop a high reliability, radiation hardened VHSIC Phase 1 MIL-STD-1750A computer that is qualified for space applications. Harris, Honeywell, IBM, and RCA were selected in July 1985 for the Phase 1 GVSC program. Early in 1987, the GVSC program office selected Honeywell and IBM to continue into Phase 2. Breadboard designs began during the last quarter 1987. GVSC demonstrations are planned for July 1989.

II.3.13 Advanced Onboard Signal Processor (AOSP)

The AOSP is a general purpose array of signal processing elements which are interconnected through a multiple bus network. The AOSP is a critical system for future space applications such as onboard communications signal processing, radar processing, and electro-optical signal processing. VHSIC technology is required to meet the size, weight, and power constraints of space platforms.

Contracts were awarded to IBM and TRW in September 1986 for the development of two of the basic building blocks in the AOSP. Brassboards with VHSIC technology will be developed for the Mono Function Signal Processor and the System Input/Output Subsystem. Brassboard demonstration of the AOSP with these two building blocks is scheduled for July 1989.

II.4 INDEPENDENT TECHNOLOGY INSERTIONS

The following partial list of companies with insertion programs indicates the degree to which the VHSIC-1 is being designed into military systems, such as the sea-going Tartar weapon system shown in Figure II.7. The list includes active, awarded contracts, mostly for hardware developments and is only a sample of similar activity which is underway at many other DoD contractors.

In almost all cases, DoD systems contractors are including VHSIC-1 technology and products extensively in their proposals for system updates and new system developments. Many of the new VHSIC-1 chips being developed will meet the VHSIC interoperability standards.

General Dynamics

- o 1750A processor for Aquila (AF)

Honeywell

- o Boost surveillance tracking system (AF)
- o Multi-function target acquisition processor (Army)
- o Video display processor for ATF (AF)

Hughes Aircraft

- o Dipping sonar - ALFS (Navy)
- o Timing bus monitor development (Delco)
- o LEAP (SDIO)

IBM

- o AN/UYK-20 upgrade for Cutty Sark (Navy)
- o Integrated processor unit for LHX - study (Boeing-Sikorsky)
- o AN/MLQ-34 TACJAM communications (Sanders)

Raytheon

Tartar

- VHSIC Insertion
  - — Radar Signal Processing
- VHSIC Chips — Semi-Custom
  - (2) FFT
  - (2) CFAR
  - (1) Cordic
- Increased Throughput Performance By a Factor of 30 for FFT and Monopulse Calculations
- Projected Production Quantity of 27 Systems with 3000 Devices

NAVY
NAVAL SEA SYSTEMS COMMAND
(NAVSEA)

TARTAR MISSILE SYSTEM - VHSIC INSERTION

FIGURE II.7

Raytheon

- o Tartar missile (Navy)
- o Advanced processor technology for air-air missiles (AF)
- o Advanced on-board signal processor AOSP (AF/DARPA)
- o Terminal imaging radar (Army)
- o MILSTAR (AF)
- o AMRAAM producibility enhancement (N/AF)
- o IR Maverick AGM-65D (AF)
- o AIM-54C Phoenix missile (Navy)
- o Aegis standard missile (Navy)
- o Sparrow missile (Navy)
- o AN/SLQ-32 (Navy)
- o TSPAN - Trident sonar processor/analyzer (Navy)

Texas Instruments

- o ATF 1750A computer module (AF)
- o ATF mission data processor (AF)
- o AGWP - advanced guided weapons program (AF)

TRW

- o Common signal processor ATF (AF)
- o INEWS (AF)

Unisys

- o Common modules for ATF (AF)

Westinghouse

- o Guidance instruction set architecture (AF)
- o ATF array processor (AT&T/AF)
- o Joint STARS insertion (AF)
- o 1750A computer for space station (NASA)
- o Wafer scale integration (CSC/AF)
- o INEWS (AF)

CHAPTER III

PHASE 1

PHASE 1

The initial effort to develop and establish a pilot production capability for producing silicon chips with 1.25 micron minimum feature sizes began in May 1981. The contractors participating in this phase were Honeywell, Hughes, IBM, Texas Instruments, TRW (with Motorola), and Westinghouse (with National Semiconductor). This phase was later expanded with the addition of a technology insertion program and a yield enhancement program. The technology insertion efforts have been continued as a separate program; the remaining activity in Phase 1 has been to qualify representative VHSIC-1 chips to JAN specifications. Details of the chip development results of Phase 1 are contained in references III.1 through III.36.

III.1 VHSIC INDUSTRIAL BASE

In addition to the six VHSIC Phase 1 contractors, an increasing number of other companies are now designing and manufacturing VHSIC-1 products. The companies listed below have provided information on their fabrication processes, devices and products for sale, design, fabrication, and packaging capabilities, and points of contact for additional details. All of these companies are working toward fully meeting the VHSIC-1 requirements listed in section VII.1.2. Abstracts of the information provided are presented in this section.

A similar list of companies doing VHSIC design tool development is included in Chapter V.

III.1.1 AT&T

Fabrication Processes:
- o CMOS bulk 1.25 micron
- o CMOS bulk 1.25 micron, radiation hard, available 4Q88

Devices:
- o DSP16 - 16 bit fixed point signal processor, available 3Q88
- o DSP 32100 - 32 bit microprocessor, available 4Q88

Form:
- o Single chip, pin grid array

Design Facility:
- o Standard cell library, logic synthesis, layout; supported on Mentor Graphics, Daisy, and Valid workstations; available for external use
- o Custom logic design at 1.25 micron up to 50K gates and 100 MHz
- o Custom design to 0.9 micron available 1Q88

Point of Contact:
- o Claude Lumpkin (919-279-3604)
  AT&T, Guilford Center
  P.O. Box 20046
  Greensboro, NC 27420

III.1.2 General Electric/RCA Microelectronics Centers

Fabrication Processes:
- o CMOS bulk 1.25 micron, radiation harden, DESC certified
- o CMOS SOS 1.25 micron, radiation hard
- o Butterfly chip in qualification process for JAN-QPL
- o Bulk gate array chip to be submitted for generic qualification under MIL-M-38510/605

Devices (partial list):

	Size (mils)	Transistors	Yield (%)
Bulk CMOS			
Butterfly	248x248	39,500	25
Correlator	305x305	80,000	16
Signal Processor	371x368	40,000	39
13.7K gate array			
CMOS/SOS			
GVSC test vehicle	280x280	20,000	20
10K gate array	309x307	40,000	in debug
64K rad hard RAM	In development		

Form:
- o Packaged and tested to quality levels as high as Class S.

Design Facility:
- o Full service
- o Standard cell
- o Silicon compiler

Point of Contact:
- o E. Douglass (919-549-3304)
  GE Microelectronics Center
  PO Box 13049, 3026 Cornwallis Road
  Research Triangle Park, NC 27709
- o J. Saultz (609-866-6402)
  GE/RCA Microelectronics Center
  Route 38, Bldg. 145-3
  Moorestown, NJ 08057

III.1.3 Harris Corporation

Fabrication Process:
- o CMOS 1.25 micron; radiation hardened, 5 V

Devices:
- o Viterbi Coder/Decoder
- o Communication Switch

Form:
- o Single chip package

Design Facility:

- o Hurricane Silicon Compiler using parametric macrocells and glue cells
- o Daisy workstations, CADAT, Zicad accelerators

Point of Contact:
- o R. Quinn (305-729-5862
  Harris Corporation
  Government Systems Sector
  P.O. Box 37
  Melbourne, Florida 32902

III.1.4 Honeywell Solid State Electronics Division

Fabrication Processes:
- o Bipolar 1.25 micron; DESC audit October 1987
- o CMOS 1.25 micron; DESC audit scheduled for June 1988
- o RICMOS 1.25 micron; radiation hardened CMOS; DESC audit scheduled June 1988

Devices:
- o CMOS gate array family; to 40,000 gates
- o Bipolar gate array family; 12,000 gates
- o RICMOS memories

Form:
- o Bare chip and single chip packages to 284 pins.

Design Facility:
- o Front end logic design, physical design, operating with Mentor, Daisy, VAX.
- o VHDL interface in 1988.
- o Custom, gate array, standard cell design service available to customers

Products:
- o PI-bus interface unit; available mid-1988
- o Test-bus interface unit; available September 1988

Point of Contact:
- o Bruce Grieshaber (303-577-3559)
  Honeywell, Inc.
  Solid State Electronics Division
  1150 East Cheyenne Mountain Boulevard
  Colorado Springs, CO 80906

III.1.5 Hughes Microelectronics Center - Carlsbad and Newport Beach

Fabrication Process:
- o CMOS/SOS 1.25 micron, radiation hard; self-audit for certification 1Q88; Process to be DESC certified by 3Q88 and the complete CMOS SOS product line DESC qualified by 1990
- o HCMOS 1.1 micron/ 0.9 micron. DESC certification is planned for completion in 1989. Radiation hard versions are in development.
- o Foundry services as well as turn-key design services.

Devices:
- o Multi-channel correlator
- o Single channel correlator
- o Signal tracking subsystem
- o Configurable gate arrays

Form:
- o Tested chip, multichip packaging, or a variety of single-chip packages, including pin grid arrays, leaded and leadless chip carriers and quad flatpacks. Packaging includes pin grid arrays to 180 pins and flat pack to 196 leads.

Design Facility:
- o Standard cell library, parametrized cell, gate array, and full custom design service; Mentor Graphic workstations

Point of Contact:
- o R. W. Dodge(619-931-3196)
  Hughes Aircraft Company
  Bldg. 743, MSG630
  6155 El Camino Real
  Carlsbad, CA 92009

III.1.6 IBM Federal Systems Division

Fabrication Processes:
- o CMOS 1.0 micron 5V; DESC certified August 1987
- o CMOS 1.0 micron 5V, radiation hard
- o CMOS 0.5 micron 3.3V; baseline available 2nd Qtr 1988
- o CMOS 0.5 micron 3.3V, radiation hard; available 2nd Qtr 1988

Devices:
- o Configurable Static Ram (CSR)
- o Bus Interface Unit (BIU)
- o Systolic Processor (SP)
- o Address Generator (AG)
- o Signal Processing Element (SPE, MIL-M-38510/620)

Form:
- o Chips
- o Single Chip Package (SCP)
- o Multi Chip Package (MCP)

Products:
- o 64K, 256K radiation hardened SRAM; engineering samples 4th Qtr 1988
- o Fourier Transform Module; boards available 1st Qtr 1988
- o Common Signal Processor; breadboard demo 2nd Qtr 1988

Design Facility:
- o Chip design - custom design, master image
- o Subsystem design
- o System level design

Point of Contact:
- o Philip B. Johnson (703-367-5547)
  IBM Federal Systems Division
  9500 Godwin Drive
  Manassas, VA 22110

III.1.7 INTEL Corporation:

Fabrication Processes:
- o CMOS 1.0 micron 5V; DESC certified

Devices:
- o 64K SRAM MIL-M-38510/613; to be qualified 2Q88

Form:
- o Single chip surface mount packages

Design Facility:
- o Standard product designs only

Point of Contact:
- o Neil Carey (602-961-2825)
  INTEL Corporation
  5000 W. Chandler Blvd.
  Chandler, AZ 85226

III.1.8 LSI Logic Corporation

Fabrication Processes:
- o CMOS, 1.0 micron, 5V
- o CMOS, 1.2 micron, 5V

Devices:
- o Gate array, 60, 80, 100K estimated usable gates, 1.0 micron, bare chip, single chip package
- o RISC microprocessor chip set (available 4Q88), 1.2 micron, bare chip, single chip package

Products:
- o CPU (Central Processing Unit)
- o FPA (Floating Point Accelerator)
- o Write Buffer

Design Facility:
- o Complete design facilities available
- o Foundry Services

Points of Contact:
- o J. Ferro (408-433-4228)
  LSI Logic Corporation
  1551 McCarthy Blvd.
  Milpitas, CA 95035

III.1.9 National Semiconductor

Fabrication Processes:
- o CMOS 1.25 micron, radiation hard, 5V and 3.3V versions
- o Fabrication line certified in accordance with MIL-M-38510; assembly and test certification expected 1Q88
- o Qualification for 64K memory expected 3Q88
- o Qualification of 10K gate array has begun
- o Foundry services available

Devices:
- o 16K Static RAM
- o 64K Static RAM, MIL-M-38510/610

Form:
- o Standard DIP, surface mount package, wafer, or die

Design Facility:
- o Custom designs accepted from customer's CAD, from silicon compilers (Genesil or Concord)
- o Gate array personalizations, standard cell library

Points of Contact:
- o R. Cassidy (408-721-7200)
  National Semiconductor Corp.
  2900 Semiconductor Drive
  P.O. Box 58090
  Santa Clara, CA 95052-8090

III.1.10 Performance Semiconductor

Fabrication Processes:
- o CMOS 1.25 micron, 5V
- o CMOS 1.0 micron, 5V

Devices:
- o 1750A microprocessor
- o MMU/COMBO unit
- o Processor interface chip
- o SRAM, 16K
- o SRAM, 64K

Form:
- o CERDIP, sidebrazed DIP, and plastic DIP, all 300 mil wide standard. Non-standard widths also available.

Point of Contact:
- o L. G. Wellborn (408-734-8200)
  Performance Semiconductor Corp.
  610 E. Weddell Drive
  Sunnyvale, CA 94089

III.1.11 Raytheon Microelectronics Center

Fabrication Processes:
- o CMOS 1.25 micron, radiation hard, 5.0 volt process; DESC pre-audit in January 88; DESC audit in April 88; MIL-M-38510/606 qualification in June 89
- o Chip foundry through packaging and screening capability

Devices:
- o Up to 20K gate array family
- o Floating-Point Multiply Accumulate Kernel, available 2Q88.

Form:
- o Both chip and single package form

Products:
- o 10K, 15K and 20K gate arrays with complete software and library support
- o 40-bit, 25MHz, Floating-Point Processor

Design Facility:
- o Complete software and library support with a broad range of interface media to handle both component and system designs.

Points of Contact:

- o David Beadling - Component design (415-966-7705)
  Raytheon Company
  Semiconductor Division
  350 Ellis Street
  Mountain View, CA 94039

- o John Maxfield - System design (617-470-9048)
  Raytheon Company
  Microelectronics Center
  358 Lowell Street
  Andover, MA 01810

III.1.12 Texas Instruments

Fabrication Processes:

- o STL bipolar 1.25 micron (standard products)
- o NMOS 1.2 micron (SRAM)
- o CMOS 1.0 micron (standard products/ASIC), compliant to 883C
- o CMOS 0.8 micron (SRAM/ASIC/standard products)
- o Foundry services available for ASIC, gate array, and standard cell.

Devices:

- o 1.25 micron *VHSIC STL single chip, 2 MIPS MIL-STD-1750A data processor.*
- o 1.25 micron VHSIC NMOS 50-60 nanosecond static RAM with address latch and built-in parity
- o 1.0 micron CMOS gate array family to 15.3K gates
- o 1.0 micron CMOS standard cell family for designs to 40K gates

Form (standard packages):

- o 44 and 84 Pin LCCC (50 mil centers)

- o Gate Array/STD cell products
  - 28, 40 pin DIP
  - 28, 44, 68, 84 pin LCCC
  - 84, 100, 132, 144, 180, 208 pin PGA
  - 84, 100, 132, 16 pin Quad Flat Pack

Module Products:

- o VHSIC 1750A Data Processor Module - SEM-E format, MIL-STD1750A computer.
- o MIL-STD-1553B Bus Interface Module - SEM-E format, dual channel remote terminal/bus controller 1553B interface
- o System Maintenance Module - SEM-E format interface to VHSIC integrated environment workstation.
- o High Density Power Supply Modules - SEM-E format, 50 to 200 watt power supplies with choice of 2, 3, 5, and $\pm$15 volt outputs.
- o ARIES (Artificial Intelligence Embedded Processor) - SEM-E format LISP based symbolic processor.

Design Facility:
- o Chips - custom, ASIC (gate arrays or standard cells) for Daisy Mentor workstations, and silicon compiler design services.
- o Modules - embedded processor designs for 1750A and symbolic processors, memory, and peripherals plus array or signal processors.

Point of Contact:
- o Dennis R. Best (214-480-1321)
  Texas Instruments, Inc.
  P.O. Box 660246, MS 3145
  Dallas, TX 75266

III.1.13 TRW

Fabrication Processes:
- o Bipolar 1.0 micron, 5V, radiation harden; DESC qualification of AG expected 4Q88

Devices:
- o Window Addressable Memory (WAM),
- o Content Addressable Memory (CAM)
- o Four Port Memory (4PM) - CMOS available 12/88
- o Matrix Switch (MS) - CMOS available 8/88
- o Address Generator (AG), MIL-M-38510/616 qualification projected 4Q88
- o Microcontroller (MC)
- o Register Arithmetic Logic Unit (RALU) - CMOS available 8/88
- o Multiply Accumulate (MAC)
- o Convolutional Decoder (CD) - CMOS available 8/88
- o Fast Fourier Transform Arithmetic Unit (FFTAU) - CMOS available 8/88
- o Fast Fourier Transform Control Unit (FFTCU) - CMOS available 8/88
- o Convolver

Form:
- o Bare chips, single chip packages

Design Facility:
- o Entry points are anywhere from the specification to the design tape or the mask set.

Point of Contact:
- o Brad Byk (213-535-4069)
  TRW
  One Space Park
  Bldg. M5/1492
  Redondo Beach, CA 90278

III.1.14 Unisys - Microelectronics Center (UTMC)

Fabrication Processes:
- o CMOS 1.25 micron at UTMC

Devices:
- o 32-Bit RISC processor
- o 32-Bit floating point co-processor

Form:
- o Single chip package; pin grid array or surface mount

Products:
- o Single module demonstration computer

Point of Contact:
- o Neil F. Hahn (612-687-1714)
  Unisys Defense Systems
  Computer Systems Division
  P.O. Box 64525
  St. Paul, MN 55164

III.1.15 VTC Incorporated

Fabrication Processes:
- o CMOS 1.0 micron 5V P-well
- o CMOS 1.0 micron radiation hard 5V

Devices:
- o 16K radiation hard RAM, V1608-B

Form:
- o 24 pin DIP
- o 32 pin LCC

Products:
- o 1.0 micron foundry services on the Genesil silicon compiler. Designation VL8000

Design Facility:
- o Support for standard cell and Genesil silicon compiler developments.

Point of Contact:
- o Craig Carrison (612-851-5210)
  VTC Incorporated
  2401 East 86 Street
  Bloomington, MN 55420-3381

III.1.16 Westinghouse

Fabrication Processes:
- o CMOS 1.25 micron line, radiation hard, 5V and 3.3V versions
- o Foundry service (at National Semiconductor)

Devices:

Devices:
- o 16K static RAM, DIP/bare chip
- o 64K static RAM, DIP, leaded chip carrier, bare chip
- o 10K gate array, pin grid array, leaded chip carrier, bare chip
- o Gate array family to 54K gates, pin grid array, leaded chip carrier, bare chip

Modules:
- o 1750A processor
- o Non-volatile memory
- o Mil-STD-1553B Interface
- o High speed data bus interface
- o Clock/terminator/monitor

Design Facility:
- o Gate array routing from Daisy or CAE/Tektronix net list
- o Masks made from CALMA database

Points of Contact:
- o D. Sartorio (301-765-6744)
  Westinghouse Electric Corp.
  P.O. Box 1521, MS 5210
  Baltimore, MD 21203
- o J. Fagan (301-796-2280)
  Westinghouse Chesapeake Group
  7240 Parkway Drive, Suite 360
  Hanover, MD 21076

III.2 QUALIFICATION OF VHSIC DEVICES

The migration of VHSIC technology into military systems is having a profound impact on the process by which DOD acquires its weapon systems. New procedures are emerging for specifying microelectronic hardware and software components. The standards by which these components are manufactured, tested, and qualified for military use are being modified to take account of the new levels of technology introduced by VHSIC. The hardware components are being documented in the VHSIC Hardware Description Language (VHDL - a DoD and industrial standard which is more fully described in Chapter V). This standard language ensures an accurate and full technical description of the chip in such a form that second sourcing and/or re-procurement is much easier under than current procedures. All of these changes are forcing a re-examination of the specification and control of the logistics pipeline from the chip specification, to the manufacturer, to the supply depot, to the fielded system, to the repair facilities, and back.

III.2.1 Qualification Status

VHSIC devices are being qualified to MIL-M-38510 to demonstrate that VHSIC technology is capable of supporting system design with reliable, testable, and well-documented devices. The JAN qualification of VHSIC devices has been partially

supported by contracts to National Semiconductor, Motorola, TRW, IBM, Westinghouse, and Honeywell. To meet JAN qualification requirements a number of specific steps must be carried out.

- o characterization and documentation of the device in a dated specification (slash sheet) in accord with MIL-M-38510,
- o certification of the fabrication line to assure a controlled process in accordance with MIL-STD-976,
- o testing of a qualification lot in accord with MIL-M-38510 and MIL-STD-883C.

By the end of 1987 the following qualification actions had been taken by the VHSIC contractors.

Honeywell
- o Draft of specification sheet submitted to DESC for controller chip, MIL-M-38510/625
- o DESC audit of CML fabrication line (Colorado Springs) completed October 1987

IBM
- o SPE chip specification MIL-M-38510/620, dated December 1987
- o SPE scheduled for JAN qualification, September 1988
- o CMOS fabrication and assembly line (Federal Systems Division), certified August 1987

Motorola
- o Four port memory chip specification MIL-M-38510/615, dated November 1987
- o CMOS fabrication and assembly line (MICARL), certified February 1987

National
- o 64K SRAM chip specification MIL-M-38510/610, dated February 1987
- o CMOS fabrication line (Santa Clara), certified November 1986

Texas Instruments
- o Draft Standard Military Drawings (SMD) submitted to DESC for multi-path switch and 72K SRAM chips. SMDs describe existing commercial parts which could be used in a military environment.

TRW
- o Bipolar fabrication line (LSI Products), certified March 1987
- o Assembly and test process (Microelectronics Center), certified March 1987
- o Address generator chip specification MIL-M-38510/616, dated November 1987
- o Address generator scheduled for JAN qualification, September 1988

In addition to the above actions, Westinghouse and Hughes Aircraft have developed plans for qualification of their respective VHSIC gate arrays to MIL-M-38510/605, a generic qualification approach for CMOS gate arrays.

III.3 TEST AND EVALUATION

III.3.1 Army In-House Test and Evaluation

Two VHSIC device types were tested during 1987 at the Electronics Technology and Devices Laboratory (ETDL), US Army LABCOM, Ft. Monmouth, NJ.

Functional and parametric electrical tests were performed successfully on 95 VHSIC Texas Instruments static RAMs in accordance with TI specifications based on a preliminary Standard Military Drawing. These devices were furnished to Hughes for insertion into the FIREFINDER system. The SRAM is a fast, NMOS, 32 pin, LCC packaged device. Typical measured access time was 45ns. The design goal is 35 ns. Devices delivered to Hughes were selected for access times less than 50 ns. ETDL test data showed good correlation with TI data. Tests included functional tests in non-pipelined and pipelined modes, and DC parametric and access time measurements, all conducted at 25 and 85 degrees C. The electrical tests were performed on the Tektronix S3270 test system.

The second VHSIC device tested was the Texas Instruments VHSIC multipath switch. The test sample consisted of bipolar, LCC packaged devices. DC parameter measurements and functional self-test were performed using the Tektronix S3270 test system. Extensive functional tests were conducted using the Hilevel TOPAZ 50 test system. The TOPAZ tests included functional scan-path and self-test, crossbar tests, data set-up time, propagation delay time, and maximum frequency measurements. Device tests were performed successfully in accordance with a preliminary Standard Military Drawing. Measured maximum frequency was 13 MHz. The TOPAZ tests were developed by Texas Instruments using the TOPAZ 50 test system and device test data later verified at LABCOM's ETDL.

ET&DL has evaluated test chips from TI and IBM to determine process control and reliability of submicron technology. Devices were tested for DC characteristics and for hardness against hot electron effects. Over 10,000 DC tests were performed on transistors, resistors and contact chains. Results of these tests were correlated with the contractor's results and reported back to the contractor. IBM devices tested early in 1987 showed a severe roll off in transistor threshold voltage versus channel length. Process changes were made to correct the problem. All other test results correlate well with both contractors, and the test data indicate good process control.

ET&DL has also verified the elimination of device failure caused by hot electron effects. TI and IBM devices were stressed with overvoltage at $-10^{O}C$ for over 100 hours. The 0.8 micron TI devices, which normally operate at 5 volts, were stressed with 7.2 volts. The IBM devices, with 0.5 micron geometry, which normally operate at 3.3 volts, were stressed with 3.6 volts. No significant change in device performance was noticed. These results confirm the contractor data and no degradation of system reliability is expected under field conditions.

III.3.2 Navy In-House Test and Evaluation

Functional tests were performed at the Naval Ocean Systems Center on parts from three VHSIC Phase 1 Contractors: IBM, TRW, and National, and a part from Raytheon.

Devices and test programs were given to NOSC for evaluation. Automatic test equipment at non-VHSIC companies was leased and used to implement the test. Table III.1 lists the company, parts, and testers used.

The IBM, National, and Raytheon parts passed the functional tests over the frequency range 1-25 MHz at room temperature. The TRW parts were functional at 1 MHz, but defects in the tester adapter board prevented testing at higher clock frequencies.

NOSC also performed parametric tests on test chips from IBM, TRW, Motorola, and Honeywell. Measurements included transistor parameters (Vth, K1, mobility, etc), contact resistance, and resistivity.

The Signal Processing Staff of the Radar Division at the Naval Research Laboratory has developed a physical model of the TRW VHSIC MAC chip on their workstations manufactured by Daisy systems. The model runs on Daisy's Physical Modeling eXtension (PMX). Under this technique, the physical chip to be modeled is entered into the PMX, and the chip provides its own simulation. The input signals are actually sent to the chip. Its response is captured and fed back into the simulation. This technique circumvents the time-consuming and error-prone task of developing a software model of a new device. The PMX model only provides the functional behavior of the device. In order to be complete, the designer must also provide a graphical model, which determines how the device appears on the graphics terminal, and a timing model.

TABLE III.1

Company	Part	Tester
IBM	CMAC SPE	Takeda Riken T3340
TRW	CAM WAM	GenRad 16
National	16K SRAM	Teradyne 386J
Raytheon	FPMAK	Hilevel Topaz (NOSC)

The model was required in order to fully simulate a VHSIC Sidelobe Canceler design, which incorporated the MAC and two personalizations of the Motorola VHSIC V6000 gate array. The gate array designs were created and simulated on the Daisy. The addition of the PMX model of the TRW MAC allowed NRL to simulate the total design before fabrication. The gate arrays are currently in fabrication.

The Daisy PMX was also used by Naval Avionics Center to provide a physical model of the IBM VHSIC CMAC chip. The model was used to simulate their design of a VHSIC Fast Fourier Transform Brassboard. This processor was built, and only minor changes were required after fabrication in order to make it operational.

III.3.3 Air Force In-House Test and Evaluation

During FY87, the Microelectronic Reliability Division at the Rome Air Development Center performed detailed tests and evaluations of VHSIC devices. The RADC facility houses the baseline VHSIC test system, the TISSS central host computer, a VLSI design workstation, and a scanning electron microscope.

Test program development and device characterization focused on four VHSIC device types including the Honeywell sequencer, TI 72K SRAM, National/Westinghouse 64K SRAM, and the IBM SPE chip. Several commercial advanced VLSI chips were also studied. These were the Motorola 68000 microprocessor, a Performance Semiconductor 64K SRAM and several 256K DRAMS.

Several additional commercial devices are scheduled for evaluation in FY88. Candidates include the 32C016 and 32C032 CPU chips (National Semiconductor), the 80286 and 86386 CPU chips (Intel), the 68020 CPU chip (Motorola), and any 1750A chips that appear ready for qualification.

Packaged devices were subjected to tests contained in MIL-STD-883 (Test Methods and Procedures for Microelectronics). This effort is directed towards assessing the package construction and packaging processes of the VHSIC contractors. The objective of is to establish the suitability of these packaged devices for qualification to military standards. The result of this evaluation is a Product Evaluation Report that is first shared with the manufacturer to aid in process improvement. It is then forwarded to the DoD VHSIC Program Office as a record of the contractor's progress toward achieving a qualifiable product.

During 1987, chips and packages from Honeywell, IBM, Texas Instruments, and TRW were evaluated. Each of these contractors has received guidance on improvements needed in their products to be qualified for military use. Tests are currently underway on a total of 142 packaged devices from potential VHSIC suppliers.

CHAPTER IV

PHASE 2 - SUBMICRON TECHNOLOGY

PHASE 2 - SUBMICRON TECHNOLOGY

IV.1 TECHNICAL GOALS AND TASKS

In October 1984, Phase 2 contracts were awarded to Honeywell, IBM, and TRW for the development of the second generation of VHSIC technology. The VHSIC Program Office required the IC technology to meet, among other requirements, the specifications in Table IV.1.

TABLE IV.1

Feature size	0.5 micron
Functional throughput rate	10^{13} gate-Hz/cm^2
On chip clock rate	100 MHz
Failure rate	0.006%/1000 hours
Radiation hardening (total dose)	$5X10^4$ rads(Si)

The program of activity during this development is very similar to that of Phase 1 except that the goals are much more ambitious, and the tools for doing the development are less readily available. New tools, new techniques, and more aggressive technical approaches are being used to work toward the desired goals.

The specific tasks which the contractors have been engaged in for the past three years are grouped into eight major areas:

(1) chip technology and fabrication,
(2) system architecture design,
(3) chip design,
(4) support software,
(5) interoperability (BIU) design,
(6) module design, fabrication, and demonstration,
(7) brassboard design and fabrication (option),
(8) design and simulation methodology.

The progress and current status of each of the contractors is separately described below. More detailed information can be obtained from the interim Phase 2 technical reports which are listed as references IV.1 - IV.16.

IV.2 HONEYWELL

Honeywell is developing a 0.5 micron current mode logic bipolar process. The process features a mixture of optical and e-beam lithography, groove trench isolation, and 4 layers of metal interconnects. Packages for the chips include 270 pin single chip

packages and multichip packages using thin film, multilayer copper conductors with polyimide dielectrics.

Two basic submicron chip types are being developed. The first is a 35,000 gate array designated HM35000 which is being used for the Bus Interface Unit to the PI-Bus. The second chip type is designated the HM70000 Configurable Gate Array. This type has 70,000 available gates and can also be configured with custom macrocells such as memories, register files, and multipliers. Over 80% of the gates in these arrays can be used and routed in any given design. Power dissipation of these parts is from 5 to 7 watts. Three submicron chips and a VHSIC Phase 1 technology chip are being designed for this program.

In the design automation area, activity has concentrated on increasing the capacity of existing tools, speeding up existing tools, adding performance biasing influence to existing tools for minimizing a chip's input to output path delays, minimizing the number of manual operations required, and evaluating new or better tools.

A Multimode Array Processor brassboard module will be used to demonstrate the effectiveness of the Phase 2 technology. The module will run Automatic Target Recognizer software in either Single Instruction-Multiple Data (SIMD) mode or Multiple Instruction-Multiple Data (MIMD) mode and will interface to a PI-Bus. An Ada to microcode compiler and debugger are being developed to support the brassboard module. VHDL models of the chips will be developed. Honeywell has teamed with Motorola as a major subcontractor for bipolar process development and second source services. Progress in the individual technology areas of the program for 1987 follows:

Process Technology: In 1987, submicron processing became the number one priority of Honeywell's Solid State Electronics Division's facility in Plymouth, MN, as most of the Phase 1 processing was moved to the AVLSI facility in Colorado Springs. Several major pieces of equipment were purchased and brought on-line including a third e-beam machine, a sputtering system, and a GENUS 8710 cold-wall Low Pressure Chemical Vapor Deposition reactor. Ring oscillators with 4027 stages were fabricated. Proximity correction software developed under subcontract by Harris Corporation and a new negative e-beam resist called ECX paved the way for 1.5 micron pitch metal patterning on dense circuits. Optical lithography with conventional G-line 10:1 direct wafer steppers is being used for five layers including the device isolation grooves and the upper two metal layers and their vias. HM35000 metalization test chips are being fabricated. Process enhancements are being incorporated which should meet all of the submicron enhanced radiation hard requirements except that for single event upset.

Packaging: In 1987, tab lead frames were designed and ordered for the 180 pin HM35000 gate array and the 270 pin HM70000 gate array. The tabs differ from those used in Phase 1 in that there is now a double row of bonding pads around each die. The 180 lead pin-grid array package which was developed during Phase 1 will be used for the Bus Interface Unit. A 270 lead pin-grid array has been designed for the other chips. Multichip package test vehicles for testing thermal, electrical, and yield factors have been built on pinned and unpinned ceramic substrates. Multichip package fabrication was moved into a Class 10 clean room and, although yield enhancement work will continue, the technology is ready for the brassboard multichip package.

Design: Design, layout, and verification of the basic HM35000 gate array plus a test metalization pattern for it have been completed. Design and layout of the Bus Interface Unit function using the HM35000 gate array have also been completed and verified. The design and layout of the HM70000 configurable gate array, and random access memory, register file, and multiplier custom macrocells for it, have been completed and verified. A test metal design for the HM70000 has been started. First pass structural design of the Array Processor Unit chip and the Array Processor Controller chip on the HM70000 configurable gate array has been completed. Table III.2 summarizes the characteristics of the three Honeywell submicron chips.

Honeywell completed the fabrication of the first two lots of the BIU chip in December 1987. This chip is an early deliverable in the program since it is intended to validate the 0.5 micron processing technology. The chip contains about 19,000 equivalent gates of logic in 0.16 square centimeters of gate array - a circuit density that is ten times greater than that demonstrated in Honeywell's Phase 1 technology at 1.25 microns.

The BIU chip complies fully with all of the VHSIC interoperability standards. It implements the 2.1 version of the PI-bus specification, the version expected to be adopted by the Joint Integrated Avionics Working Group for advanced avionics systems in ATF, ATH, and ATA applications.

TABLE IV.2

Honeywell 0.5 Micron Chip Set

	Size (mils/side)	Pkg (pins)	Power (watts)	Gates (equiv)	Memory (bits)
Bus Interface	280	180	4.5	18.3K	
Array Controller	370	270	6.5	25.9K	4K RAM 1.3K Reg File
Array Processor	370	270	7.2	31.5K	8K RAM 0.5K Reg File

Note: 100 MHz clocks on all chips

By the end of 1987 the testing of BIU chips had begun, and the initial results verified that all of the circuits required to perform automated scan-based testing operated correctly. Complete scan paths containing up to 9000 equivalent gates were functional on many of the dice. A more complete measurement of the entire BIU chip using a high speed tester is in progress.

Design Automation: Gate array placement and routing tools were improved from many standpoints including gate array size capacity, amount of computer time required, number of unconnected routes, number of usable gates, and a speed-up of critical nets. Performance driven layout tools were demonstrated. The DAMSEL timing analysis tool, IR drop calculation tools, and Integrated Test Generation tools went into production use. Work on structural design translators from Mentor workstation software to VHDL was begun. A hardware accelerator was brought on line to speed up gate level simulation.

E-O Application: Functional Design of the Bus Interface Unit, the Array Processor Controller, and the Array Processor Unit chips has been completed and verified. Design of the Functional Interface Unit, which is a Phase 1 technology chip used between the Array Processor and the Bus Interface Unit to complete the PI-Bus interface, has been completed and verification is in progress. All chip designs were simulated using the Silvar-Lisco Helix simulator. The Verdix Ada compiler and debugger have been integrated with the microcode compiler, and testing is underway.

Second Source: Test chips fabricated by Motorola in 1987 using I-Line 10:1 direct wafer stepper optical lithography showed good underlayer results and improving metal layer results. A Perkin-Elmer AEBLE 150 e-beam system has been brought on line and fabrication of Honeywell test chips using this tool has begun.

Interim technical reports for the Honeywell Phase 2 contract are listed as references IV.1 and IV.5.

IV.3 IBM

IBM is designing and fabricating four chips for Phase 2. These chips have already been fabricated at 1.0 micron CMOS to verify functionality and validate performance predictions. The designs have been migrated to 0.5 micron and are being fabricated. A 220 peripheral I/O single chip package and a 16 chip 625 I/O pin grid array multi-chip package are being developed. The brassboard is an acoustic beamformer that will provide a 20 fold increase in performance for submarine and surface ship ASW applications.

Processing Technology: The IBM baseline fabrication process uses e-beam lithography to define 0.5 micron polysilicon gates and 1.0 micron optical lithography for the remaining mask levels. This approach meets the performance, feature size, and environmental objectives of Phase 2. Key process features are listed in Table IV.3.

IBM has designed, built, and qualified a Class 1 clean room facility for the critical steps in the 0.5 micron process. The results of the clean room qualification showed 0.28 particles per cubic foot at 0.3 micron or less and 0 particles greater than 0.5 micron.

Results in the lithography area also demonstrate good consistency. Nominal image size was maintained within the 3 sigma limits on all critical masking levels. Overlay errors are also within the 3 sigma limit. It has also been shown that mixing of optical and e-beam exposure systems does not contribute significantly to the overlay error

budget of the lithographic system. Overall availability of the e-beam exposure tool has been 90 percent over a six months period.

The IBM approach for multilevel metal patterning is based upon lift-off processes. During 1987, 16 CMOS test chips and product chips with multilevel high density metalization have been processed. Film thickness, line widths, and via size are within the targets. Electrical test yields for metal wiring and interlevel vias have met or exceeded targets in the majority of lots.

Development of the radiation hardened 0.5 micron process has been accelerated during 1987. Outstanding results have been achieved. The current outlook is that the process will meet or exceed all of the radiation hardness goals.

TABLE IV.3

KEY PROCESS FEATURES

Process Feature	Technology Leverage
o Lightly doped p-type epitaxy on heavily-doped substrate	Radiation and latch-up immunity
o Ion implanted retrograde n-well	Radiation and latch-up immunity/circuit density
o Shallow arsenic junction	Salicide compatibility/hot electrons
o Salicides	Device performance/density
o Low temperature oxide/ phosphosilicate glass	Radiation immunity/reliability/ back end of line planarization
o Area array solder interconnection	High I/O count/multichip packaging/reliability

Packaging: The first chip designs in 1.0 micron CMOS have been packaged in a single chip package (SCP) and are being assembled into a prototype system module. The SCP is a surface mounted peripherally leaded military package with 220 external leads on 25 mil pitch.

During 1987, the emphasis has been on temperature cycle testing. A sample of 48 packages has completed over 2000 cycles at a rate of 8 cycles per day. The data indicates that the package will meet the military environment requirements.

A multi-chip package (MCP), with space for up to 16 chips, is shown in Figure IV.1. The MCP has 625 I/O pins, 498 of which are signal pins. During 1987, the MCP has been undergoing electrical and thermal tests. Computer models for the chip, substrate, connector, and board have shown good agreement with test results. Preliminary results of the environmental tests are extremely promising.

Design: During 1987, the translation of the macrocell library from 1.0 micron to 0.5 micron has been completed. A series of test site wafers was evaluated for assessment of device characteristics. The resulting device characteristics are acceptable, and in good agreement with the models. Test chips with the 0.5 micron macrocells have been released for fabrication. Translators between the VHSIC Hardware Description Language (VHDL) and the IBM design tool set are being developed. The translator from IBM design language to VHDL has been completed this year, and one of the 0.5 micron chips (CSR) has been trial coded in VHDL using this tool.

IBM is developing a core set of signal processing chips that can be used in a variety of high performance environments. The original set of four chips has been expanded to five and are listed in Table IV.4.

All of these chips have been fabricated at 1.0 micron CMOS. Performance testing has shown that these chips run at 25 MHz or faster at 125°C. The CSR, SP, VBIU, and AG chips are currently in fabrication at 0.5 micron. Testing of the first 0.5 micron chips will begin in the first quarter of 1988.

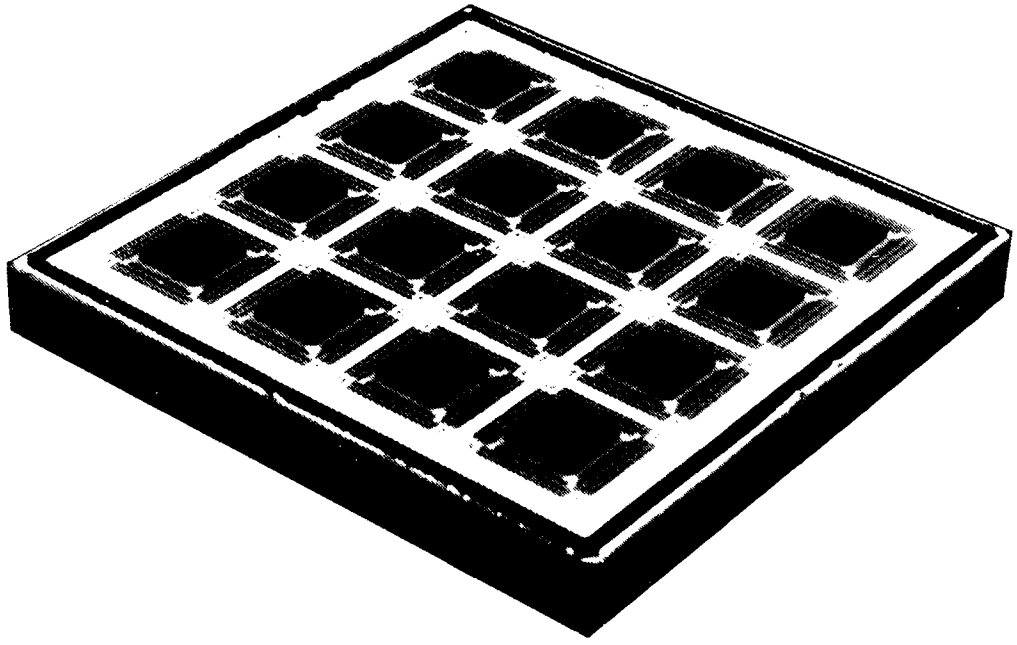
TABLE IV.4

IBM 0.5 Micron Chip Set

Systolic Processor Chip	Multiply/Accumulate Element
Configurable Static RAM	High Speed Configurable Memory
Address Generator Bus Interface Unit	Address Generator for CSR Standard PI-bus Interface
Signal Processing Element	High Performance Arithmetic Functions

Applications: The VHSIC acoustic beamformer brassboard module is part of an acoustic antenna array. It has been designed to perform the beamforming for large sonar arrays in future submarines and surface ships. The brassboard consists of a single standard electronic module (SEM) Format D card that can perform beamforming

MULTICHIP MODULE



- Number I/O Pins 625
  - — Signal I/O 498
  - — Power I/O 127
- I/O Pitch 2.54 mm (100 Mil)
- 50 MHz I/O
- Cap-Type Ceramic
- Thermal Enhancement-Grease
- Max Power Dissipation
  3W/Chip
  30W/Module

FIGURE IV.1

V3127

in a stand-alone or multiple module configuration. The 0.5 micron chips will be contained in two identical multi-chip packages mounted on the Format D module. During 1987, a prototype version of the module has been built using the first pass 1.0 micron chips and single chip packages. The prototype was demonstrated in the laboratory in December 1987.

Interim technical reports for the IBM Phase 2 contract are listed as references IV.6 through IV.11.

IV.4 TRW

The objective of the TRW Phase 2 effort is to develop a design and fabrication methodology capable of producing "superchips" - chips whose area, number of transistors, and functionality is up to two orders of magnitude greater than current state-of-the-art integrated circuits. To accomplish this, functional blocks called "macrocells", equal to or greater in complexity and size than VHSIC-1 chips, are fabricated on a silicon substrate and interconnected to form a superchip. This higher level of integration - wafer scale integration - results in:

- o increased signal and data processing functionality
- o increased reliability
- o increased speed

A key benefit of this approach is that the entire superchip can operate at the 100 MHz clock rate since the number of accesses to off-chip components is greatly reduced. The reduced number of chip to chip interconnects is expected to dramatically increase the reliability. To make the superchip approach viable, a variety of unique technical challenges must be overcome:

- o The yield of macrocell circuits on the wafer must provide a sufficient number of working circuits to assemble a fully functioning superchip.
- o Spare macrocells must be included in the initial design.
- o The interconnections between macrocells must be redundant to assure reliable data transfer.
- o The superchip must include a built-in capability to test each macrocell for functionality and to configure the good macrocells into a single functioning superchip.

An analysis of this design methodology indicates that one 1.0 inch by 1.5 inch size superchip can be obtained on each four inch silicon wafer if reasonable numbers of individual macrocells are utilized and a reasonable fabrication yield is achieved.

The higher risk of the superchip development required that objectives be prioritized in order to ensure that the key objectives of the program are accomplished. These objectives are:

- o a superchip functioning at 100 MHz clock rate
- o a 0.5 micron fabrication process capable of producing superchips

- o interoperability and testability via standard busses
- o an application of a superchip with the ability to detect faults in real time and reconfigure around them

A full-blown superchip requires the design and verification of a large number of different macrocell types. It is comprised of up to thirty million transistors and has built-in test circuitry to automatically check the functionality of all macrocells on power-up and re-configure them into a functioning superchip. The reconfigurability feature not only improves the probability of yielding a functioning superchip initially but also extends the life of the superchip because, as individual macrocells fail, the built-in test can automatically detect and replace the failed cells with functioning "spares". Triply redundant busses are used on the chip to ensure reliable connections between the various macrocells and I/O ports.

Processing Technology: A 0.5 micron CMOS process and a 0.5 micron bipolar process with triple level metallization were to be developed at Motorola and TRW, respectively, using an AEBLE-150 electron beam lithography machine for patterning the isolation trenches between the individual devices on the chip and for the other fabrication levels requiring minimum (submicron) dimensions. Motorola received Perkin-Elmer's first production AEBLE machine in September 1986.

The 0.5 micron CMOS process development at Motorola encountered two major problems: inadequate overlay accuracy of the AEBLE-150 e-beam machine and excessive current leakage with the trench isolation. To integrate the VHSIC process with Motorola's commercial technology plans, the CMOS process development has been transferred to APRDL in Austin, Texas, Motorola's premier commercial process development facility. The VHSIC process now uses LOCOS (Localized Oxidation of Silicon) instead of trench isolation and utilizes all optical lithography with an I-line step-and-repeat machine with a high numerical aperture lens.

Because a CMOS process appeared to be more in line with commercial and military trends, and because of continued technical problems in the development of the 0.5 micron bipolar process, the efforts by TRW to develop a 0.5 micron bipolar process were discontinued at the end of 1986. TRW plans to transfer and harden the Motorola CMOS process using mixed optical and e-beam lithography.

Design: The program originally included the design and fabrication of a signal processor superchip (SPS), a convolver superchip (CS), and a bus interface unit (BIU). Since the CS chip had been designed for the TRW bipolar technology, it was discontinued. The LOCOS technology requires a greater area for the same number of transistors and therefore increases the size of the superchip design. This area penalty jeopardized the probability of yielding an SPS superchip on a four inch silicon wafer without redesign and re-verification of the 29 macrocells which comprise the SPS - a task which could not be accomplished in the time remaining on the contract. As a risk reduction measure, TRW proposed to design and fabricate the CPUAX, the CPU portion of the SPS.

The current work is focused on the CPUAX. Eight macrocell types are required for this chip, most of which have already been designed at 0.5 micron. The re-sizing of the macrocells to conform to the LOCOS design rules is being done largely through computerized scaling of the original 0.5 micron designs.

The CPUAX design includes 64 active macrocells (out of approximately 150 available on the chip) which results in approximately one million active transistors (out of three million available on the chip) at any given time. The chip measures approximately 1.3 inches x 1.0 inch and dissipates 10 watts. The chip is designed to perform 200 million floating point operations per second.

Application: The brassboard module design was redirected from a cruise missile application to a communication satellite (MILSTAR) with a projected module demonstration date of September 1989.

Interim technical reports for the TRW Phase 2 contract are listed as references IV.12 through IV.16.

CHAPTER V

PHASE 3 AND OTHER SUPPORTING TECHNOLOGIES

PHASE 3 AND OTHER SUPPORTING TECHNOLOGIES

VHSIC Phase 3 is comprised of a group of tasks to develop various technologies needed to support the main objectives of the VHSIC program. In contrast to Phases 1 and 2, which are large, comprehensive, multi-technology programs, the Phase 3 projects are more sharply focused on the areas of key technologies, equipment, and design tools needed to transform VHSIC technology into a readily usable industrial capability. Many of the original contracts ran concurrently with Phase 1 and have been completed. Others have begun more recently and are continuing during the Phase 2 period.

The status of the current projects is described below. Appendix D contains a list of the projects in Phase 3, the contractors, and points of contact.

V.1 DESIGN TOOLS: INTEGRATED DESIGN AUTOMATION SYSTEM (IDAS)

The design automation portion of VHSIC technology is currently being developed under the Integrated Design Automation System (IDAS) program which grew out of a 1980 Phase 3 investigation of some design tools. The most notable of these were the Architectural Design and Analysis System by the Research Triangle Institute and a study of hardware description language requirements by Sperry.

The formal IDAS program began in late 1980 with plans for developing a VHSIC hardware description language (VHDL) and other tools for the efficient design, documentation, and management of VHSIC hardware and software. Another objective was to automate the design process at the system level and make it possible to assess the effects of various hardware/software tradeoffs very early in the design process. The designs could then be more responsive to system requirements.

The tools must not only be individually capable of handling designs of VHSIC complexity, but they must also be integrated into a smoothly working ensemble. This latter goal is achieved by requiring that all tools be capable of accepting designs expressed in the VHDL. If a tool operates at the algorithmic level, then, where feasible, the algorithms should be expressible in Ada as a common high order language.

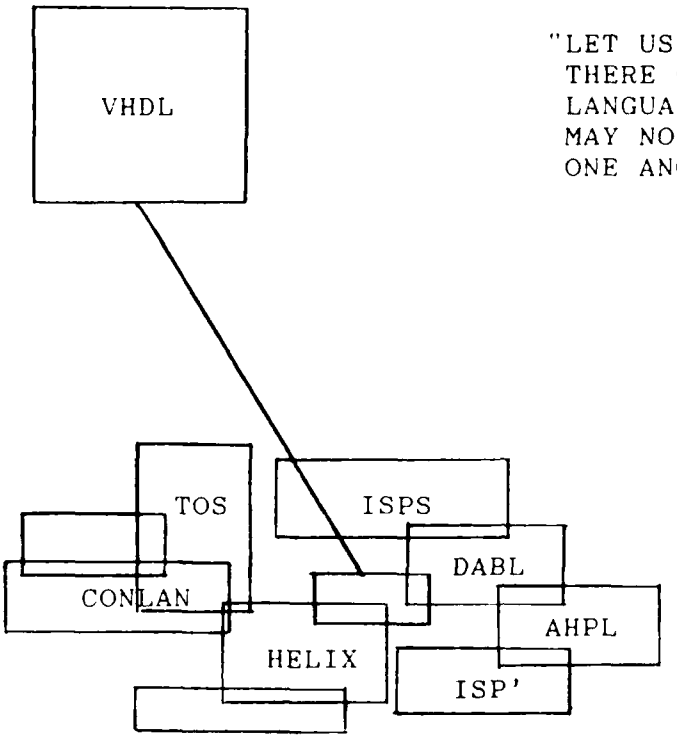
The use of these tools is being especially promoted at Service in-house design centers.

The IDAS program is organized into the four major task areas described below. The contractors active in the development of IDAS are listed in Appendix D.

V.1.1 VHSIC Hardware Description Language (VHDL)

The DoD faces the need to procure and maintain systems over a twenty year or more life cycle. The cycle starts in the initial design phase and so it is here that control over the procurement and logistics processes starts. Control has been very difficult and expensive in the past because of the many different record keeping systems into which the processes of acquisition and maintenance have been fragmented. Even with automated systems, the flow of information between different steps in the process is hindered by the same communication difficulties encountered millennia ago as described in Figure V.1. The VHDL program was initiated in order to establish a common DoD language with which all the elements of the design, acquisition, and

THE NEED FOR A COMMON LANGUAGE



"LET US GO DOWN AND
THERE CONFOUND THEIR
LANGUAGE THAT THEY
MAY NOT UNDERSTAND
ONE ANOTHER'S SPEECH"

GENESIS 11.7

VHDL BENEFITS

- A DOCUMENTATION TOOL FOR HARDWARE DESIGN
- A 'LINGUA FRANCA' FOR DESIGN DATA INTERCHANGE
- A DOD STANDARD LIKE ADA
- DOCUMENTATION FOR RE-DESIGN AND RE-PROCUREMENT

FIGURE V.1

logistics processes may communicate. As a first step, the VHSIC design tools are being created to produce full documentation automatically in the VHDL language during the design process. The following tasks are being pursued.

(a) VHDL Language Definition and Development

The definition and development of VHDL is the cornerstone of the IDAS program, and is being carried out under a contract with Intermetrics, Inc. A schematic description of VHDL is shown in Figure V.2. Implementation of software started in August 1984, and has continued into 1987. The software tool set being developed includes an Analyzer, Design Library Manager (DLM), Reverse Analyzer, Simplifier, and Simulator. Software releases of the tool set were made in February and August 1987. In September, a VHDL language version for IEEE standardization was released, and on December 10, the VHDL was approved as IEEE Standard 1076. This was a major VHSIC milestone, a step that ensures that VHSIC designs documented in the VHDL will be readily transportable throughout the commercial and military IC design communities. A final release of the tool set and the simulator for the full language is expected during 1988.

A VHDL newsletter is available from Intermetrics which regularly publishes information related to VHDL.

(b) VHDL Independent Validation and Verification

The purpose of the IV&V effort is to test the VHDL software in actual use in the field. The primary contract for this effort was awarded to the United Technologies Microelectronics Center (UTMC) in August 1985. The work is divided into two parts. The contractor performs an initial test of the VHDL software and then acts as a focal point for secondary testing at "beta" sites. The contract has been completed. User comments from the beta test sites have been incorporated into the IEEE 1076 version of the VHDL software.

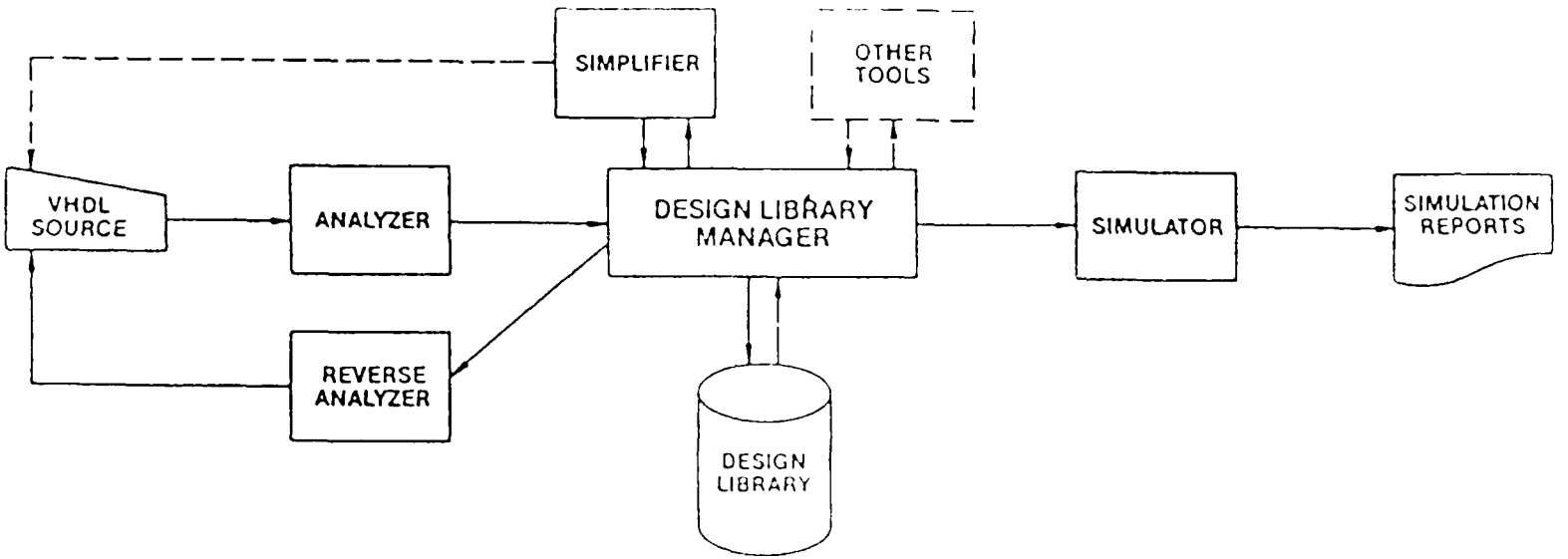
(c) Air Force Institute of Technology (AFIT) Support

The AFIT, at Wright Patterson Air Force Base, is serving as one of the beta sites as well as providing other support functions for the VHSIC program in relation to the VHDL. It is developing UNIX-based VHDL tools to distribute to universities, teaching VHDL in its CAD curriculum, providing consulting support on the IEEE standardization effort, and developing short courses on the VHDL for Government personnel. See Section VI.1 (TRAINING) for details.

AFIT also supported the standards discussions between the DoD and the IEEE Design Automation Standards Subcommittee (DASS) and the Standards Coordinating Committee 20 (SCC20) of the ATLAS language group. The VHDL (IEEE 1076) was balloted from May 20-July 10, 1987 and became an official IEEE Standard on December 10, 1987 by action of the Standards Certification Committee of the IEEE.

(d) Joint US/Canadian IBM Rehost

Under the Joint US/Canadian program started in July 1987, the VHDL tools are being adapted for use with IBM mainframes. The US is providing the VHDL



THE COMPONENT SOFTWARE BLOCKS OF VHDL

FIGURE V.2

software and technical consultation. The Canadian contractor, Bell Northern Research (BNR), will install the VHDL software in the IBM machines and integrate some of its own design tools into that VHDL environment. This contract will also provide for re-hosting on the DEC VAX and SUN 3 workstations which are of interest to universities and smaller users. The software delivery schedule to BNR is:

- o September 1987 - Version 8.0 of the VHDL environment (IEEE subset) completed on schedule
- o January 1988 - Full language Analyzer, Design Library Manager
- o April 1988 - Full IEEE 1076 simulator
- o July 1988 - Fully interactive simulator
- o October 1988 - Unix versions on VAX and Sun

V.1.2 VHDL Technology Insertion

The VHDL Technology Insertion program provides advanced design tools to support the designer using the VHDL. Beginning in August 1985, nine contracts have been awarded as listed in Appendix D.

(a) Workstations/Interfaces (GE, Gould, APL)

The purpose of these efforts is to develop terminals with interfaces which assist the designer using VHDL.

General Electric is developing a workstation suitable for production use. The first of five prototype workbenches using a Symbolics terminal was completed in November 1985. A complete chip design will be used to demonstrate the workstation environment.

Gould (via subcontractor Vista Technologies) is designing a generic workstation interface for VHDL using a SUN 3 workstation, which will automate the generation of VHDL code and check for internal consistency. The work has progressed successfully with the final software delivered in December 1987 to the Army at Ft. Monmouth and the Navy at the Naval Research Laboratory for evaluation. The new VHDL Workbench allows a designer to input schematic diagrams and have VHDL structural descriptions compiled in real time. If functional descriptions are desired, the system provides "hand holding" by means of a syntax directed editor. The user can create VHDL code even with limited knowledge of the language. This system should become the designer's entry into the world of VHDL. Since the DoD has recently chosen to adopt the new IEEE 1076 standard VHDL, it will be necessary to upgrade the VHDL Workbench to reflect this change.

The Johns Hopkins University Applied Physics Laboratory (APL) is developing software for translating between the VHDL and existing languages such as ADLIB/SABLE and ISP. APL is also integrating the tools around the VHDL intermediate form IVAN. The APL effort was completed in late 1986. Translators have been easily and quickly developed between the Mentor Graphics workstation and VHDL and between VHDL and ADAS (Architectural Design and Assessment System.

(b) Integration of VHDL and ADAS (Research Triangle Institute)

The goal of this contract is to integrate ADAS with VHDL in such a way that system designs may be captured (hierarchically) with ADAS and archived in VHDL. The net result will be an integrated environment for system level design supported by both ADAS and VHDL simulators. To achieve this capability, extensive enhancements in the graph editor, user interface, and ADAS simulator are being carried out.

During 1987, the detailed design and implementation of the project were completed. A prototype of the VHDL interface was delivered to the Air Force for integrating ADAS with the Genesil silicon compiler. Twenty DoD sites have received ADAS under this contract and, during 1987, training for personnel at these sites has been completed. System integration and testing will be completed in 1988.

(c) Synthesis Tools (Honeywell, JRS Research, Unisys)

The purpose of these efforts is to derive chip design data automatically from a VHDL behavioral description.

Honeywell uses the MIMOLA software system to determine a useful chip architecture from input that is algorithmic in nature and contains an implied structure. The output is an architectural description of a microprogrammed device in VHDL and the microcode to drive the device. Honeywell delivered a prototype of the software in June 1987 and the final version in November 1987.

JRS Research has developed an Automated VHDL/Microcode Compiler Synthesis and Design System (AMSDS) which synthesizes a microprogrammed processor architecture from an Ada program and a VHDL description of chips. Output from the program is a VHDL description of the processor and optimized microcode for the processor.

Most of the coding for AMSDS was completed during 1986 and tested in 1987. Microcode is the heart of many VHSIC chip designs. The ability to drive the compiler from VHDL machine descriptions and the ability of the microcode compiler to accept Ada source code are both important steps in breaking the bottleneck of laboriously hand coding microcode. Being able to quickly perform trade-offs between algorithms, hardware and microcode implementations (using the VHDL simulator) will also be extremely valuable in speeding up and optimizing the design process. JRS made the final delivery for this contract in June 1987. The system is in test and preliminary results are encouraging. To date, tests have shown that the automatically retargeted compiler produces better code without optimization than the baseline system did with optimization.

Sperry (now Unisys) was under contract to interface the VHDL analyzer to the MIXSIM interactive simulator. The contract was completed in May 1987. The VHDL interactive simulator is undergoing test in Government laboratories.

(d) Silicon Compiler Interfaces (RTI, National Semiconductor)

RTI is developing an interface between the VHDL and the Genesil compiler of Silicon Compiler Systems, Inc. As the chip is compiled by Genesil, a VHDL description is automatically written. The CMOS interface effort by National Semiconductor complements this by producing the chip designed with the Genesil compiler on the National Semiconductor CMOS VHSIC pilot line. This provides an experimental demonstration that the hardware output corresponds with the input design specifications.

V.1.3 System Design Tools

This program is developing advanced design tools aimed at making the higher (system) level of the design process more automated and more efficient. The contracts in this area will provide a variety of tools in fields such as design verification, design for test, advanced system synthesis, and life cycle cost modeling. These items are currently in procurement under an Air Force Project Research and Development Announcement (PRDA). Contract awards started in September 1986.

(a) Annotation Language for VHDL (Stanford)

This tool provides a designer with an English-like language in which the designer is able to write requirements. These requirements can be inserted into the VHDL design and extracted by a verification tool to insure that a design meets the set of specified requirements.

(b) Enhanced Automated VHDL/Microcode Compiler Synthesis and Design System (AMSDS) (JRS Research)

This contract effort is a continuation of development of the AMSDS system described in section V.1.2 (c).

The new efforts have focused on adding optimization and compaction capabilities to the compiler, increasing the scope and sophistication of the synthesizer process, and linking the synthesizer output (via VHDL) to the Concord silicon compiler (from Seattle Silicon Corporation). The link to the silicon compiler system will enable a complete end-to-end demonstration of an Ada specification being automatically compiled into a VHSIC chip. Major efforts are also being pursued to provide support for all Ada features, to add flexibility to the User Interface, and to add VHDL descriptions of various chip sets to the component libraries.

(c) System Level Tools for the ADAM (Advanced Design Automation System) (University of Southern California)

The long term goal of the ADAM system is to speed up the design process, to reduce design errors, and to produce designs which meet designers' goals and constraints. To achieve this goal, prototype design tools are being developed for experimental use by the Government and industry. These tools will allow a designer to specify the behavioral requirements for a design in VHDL, and to produce a register-transfer design automatically from the VHDL description. An

additional tool will provide an experimental natural language interface for entering system specifications into the ADAM System. This interface can be used for future higher-level tools.

In 1987, the following was achieved: synthesis of pipeline architectures from input data flow graphs to complete register-transfer data paths, definition of a VHDL subset for specifying behavioral requirements, and interfacing the synthesis procedures to a database of cells called CATALOG using the standard database query language SQL.

(d) Hierarchical Design for Testability (RTI)

This effort was started in September 1986 and will result in a set of knowledge based rules, using artificial intelligence techniques, for the ADAS system. It will help a designer automatically develop testable designs as the design process progresses.

(e) Analog Design with VHDL (Dartmouth University)

This effort will explore the utility of VHDL in analog component design and recommend extensions to the language which may be needed for analog design purposes. A prototype analog design system will also be constructed.

(f) Object Oriented Chip Design Using VHDL (Rensselaer Polytechnic Institute)

An advanced design tool will be developed that uses a novel way of producing a design. The designer will have available a set of "components", or building blocks, in a library from which he can build a chip. These blocks will be keyed like jigsaw puzzle pieces so that the design process will analogous to putting a jigsaw puzzle together. As the design progresses, the VHDL description and the chip physical layout will be produced automatically.

(g) Artificial Intelligence Interface to the ADAS System (RTI)

RTI was awarded a contract in September 1986 to develop the capability to map a set of software application programs onto a multiprocessor network with constraints. For example, if the set of programs must execute within a given time, this tool will determine all of the ways that the set of programs can be configured on the set of processors so that the execution time will be less than the constraint.

V.1.4 Engineering Information System (EIS)

Any design automation system requires a framework within which hardware and software information can be managed from the inception of a design through its complete life cycle. The EIS will allow data to reside in a heterogenous hardware environment but present a homogenous view of those data to the designer. The DoD is working with industry and the IEEE to obtain a common standard. A joint DoD/IEEE workshop was held at the University of Arizona in January 1986 to generate EIS requirements.

The EIS contract was awarded in July 1987 to Honeywell as the prime contractor and a team comprised of Computer Corporation of America, TRW, CAD Language Systems Inc., McDonnell Douglas Aerospace, and Arizona State University. The preliminary design review was held on November 13-15, 1987.

V.1.5 Independent Design Tool Development

The following list is a sample of the companies that are developing design tools which directly support the VHDL.

(a) Vantage Analysis

Description: VHDL analyzer and simulator for APOLLO workstation. Interfaced to Mentor software. Available April 1988.

Contact: B. La Porte (415) 659-0901
Vantage Analysis
42840 Christy St.
Freemont, CA 94538

(b) View Logic Systems

Description: Subset VHDL analyzer and simulator for IBM PC/AT class computers. Available June 1988.

Contact: L. Asher (617) 480-0881
View Logic Systems
275 Boston Post Rd. W
Marlboro, MA 01752

(c) CAD Language Systems

Description: VHDL integration platform targeted to a wide variety of hosts and operating systems; for integrating tools such as synthesizers, timing verifiers, and simulators. Available March 1988.

Contact: Dr. M. Shahdad (301) 424-9445
CAD Language Systems
51 Monroe St. Suite 606
Rockville, MD 20850

(d) Intermetrics

Description: VHDL analyzer and simulator targeted to UNIX and VAX VMS. Various parts available February - October 1988.

Contact: Rachel Rusting (617) 661-1840
Intermetrics, Inc.
7333 Concord Ave.
Cambridge, MA 02138

(e) Endot

Description: VHDL analyzer and simulator for general UNIX hosts and VAX/VMS interfaced to other Endot tools. Available May-September 1988.

Contact: C. Rose (216) 229-8900
Endot, Inc.
11001 Ceder St.
Cleveland, OH 44106

(f) VISTA Technologies

Description: Interactive workstation interface to VHDL. Available April 1988.

Contact: S. Swamy (312) 640-4712
Vista Technologies
50 Gould Center
Rolling Meadows, IL 60004

V.2 TEST AND MAINTENANCE

V.2.1 Built-In Test/Built-In Self Test (BIT/BIST)

The VHSIC Phase 1 Statement of Work required built-in test for VHSIC parts. The requirement was very general since neither the Government nor industry had a very clear picture of what was needed in circuits of VHSIC complexity. As a result of the initial work it became clear that the level of built-in test needed by military systems was much more extensive than that offered by the commercial market. IC manufacturers considered that the sole purpose of BIT was to verify the operability of a chip at the time of manufacture. The Government needed to be able to determine operability of the chip in real time, in a system installation.

In large systems, a built-in maintenance controller would perform a series of self checks when the system is turned on and then systematically test all the parts of the system. Any failures would be reported to the system controller. This controller would then be responsible for connecting the good parts into a functioning system based on available resources, maintaining error logs, and requesting subsystem repair when required. Tests would be run prior to shutting the system down to alert maintenance personnel to any failed or marginal parts which might require replacement before the next use of the system. This type of system philosophy is the heart of the proposed two-level maintenance system of the Air Force, the "minimally supported" systems of the Army, and the at-sea maintainability requirements of the Navy.

The information on testability gained through VHSIC Phase 1 contracts is reported under Phase 3 contracts on testability. See references V.1 through V.6.

The control of BIT/BIST in a VHSIC based system is built around a set of busses. The ETM-bus (Element Test and Maintenance) is used to interface directly between

chips; the TM-bus (Test and Maintenance bus) provides a second interface for communication at the board or module level. Details of these busses are covered in section V.3 on Interoperability.

V.2.2 Tester Independent Support Software System (TISSS)

The objective of this effort is to develop a system for the automated generation and maintenance of electrical test specifications and test programs for VHSIC devices. This will be accomplished through the development of a database centered software support system that is independent of both the CAD (computer aided design) and tester environments. The capability provided by TISSS will enable the Government to develop and maintain high reliability specifications in a standardized, transportable, and computer-accessible format and to automatically generate test programs. This will significantly reduce the time required to insert advanced technology microelectronics into operational systems. In addition, the data can be used for reprocurement of devices no longer being manufactured.

Full scale development of the TISSS was started by Harris Corporation in September 1985. The TISSS is now in the system integration and test stage of development. Software coding of all of the TISSS subsystems has been completed except for the modeling subsystem. A PDR (Preliminary Design Review) was held in July 1987.

The TISSS Build 1 was available and installed on the RADC TISSS computer in September 1987. The TISSS Build 1 is a fully integrated system, excluding the modeling subsystem, but is not system tested. A contract was awarded to Digicomp in April 1987 for the independent verification and validation (IV&V) of the TISSS software. The TISSS Build 2 (with system testing completed) is scheduled for delivery to the Government in May 1988. After installation, demonstration, and acceptance on the RADC TISSS computer, this initial operational capability (IOC) will be used for training and to eliminate any residual problems that may exist.

Insertion planning currently underway is addressing transition of the TISSS capability from development into an operational mode. To facilitate user acceptance, the TVL (TISSS Vector Language), a major feature of TISSS, is in the process of becoming an IEEE standard. Language has been recommended for inclusion into MIL-STD-454, Requirement 64, that references TISSS and its associated TVL as the means to provide microcircuit specification and test documentation for new system developments. Also, a VHDL Data Item Description (DID) is being written which may be referenced on procurements requiring microcircuit data deliverable to the Government in a format compatible with the TISSS.

The goal of this insertion phase is to transition to operational deployment within twelve months of the contract start, and to have a DoD TISSS operations center on-line by June 1989. This center will maintain the specification data for microelectronic devices used in Government developed electronic systems. Intermediate maintenance and preplanned product improvement (P3I) of the TISSS throughout the transitional IOC phase is critical to insure that the full operational capability performs as intended, and achieves the user acceptance essential to insure rapid use of the TISSS.

The TISSS concept is currently being extended to support LRM (line replaceable module) certification, test, and life cycle support as part of the Modular Avionics System Architecture initiative. The concept definition for the extension of the TISSS to support LRMs will be completed in May 1988 and development activities are to be initiated in October 1988.

V.2.3 Maintenance Concepts for VHSIC

Honeywell, under a 1985 contract with Rome Air Development Center, recently completed a study of the impact that advanced microelectronics technology will have on the development of appropriate maintenance concepts. The final technical report (RADC-TR-87-13) from this effort will be made available to U.S. Government agencies and their contractors through the DTIC (Defense Technical Information Center). See reference V.7

This study identifies and characterizes maintainability and diagnostic problems that might occur in advanced microelectronic systems. The guidelines are useful for specifying realistic maintenance requirements and for designing systems to meet those requirements. The guidelines are written for the system, module, and chip levels of assembly and generally provide options for the designer to choose which are most appropriate to the task. They were developed with the knowledge that VHSIC characteristics, such as built-in-test, might mitigate the problem.

System level guidelines include a discussion of maintainability as a primary system requirement, equal in importance to the mission requirements of that system. Diagnostic information management, packaging, fault diagnosis techniques, and VHSIC-1 and VHSIC-2 maintainability features are discussed.

Module level guidelines cover the electrical and mechanical characteristics associated with the maintenance features and the use of built-in test and automatic test equipment. The role of the module level diagnostics as a link between chip and system processes is stressed.

Chip level guidelines focus on methods used in the design of chips to implement a hierarchy of maintenance diagnosis throughout the system.

Particular insight into the techniques of good design for maintenance and the tradeoff between the level of maintainability achievable and its associated cost is provided. Several appendices are included which contain detailed examples of diagnostic techniques.

V.3 INTEROPERABILITY

The VHSIC Phase 2 Statement of Work, issued in 1984, stated the following requirements for interoperability.

> "3.5.1 Interoperability Standards: Interface and interoperability standards shall be established by agreement among all VHSIC Phase 2 Submicrometer Contractors and the Government COTRs to assure that all chips developed under the VHSIC Phase 2 Submicrometer Program are interoperable, both electrically and

physically. Standard voltage level(s) shall be established and utilized for all chips and input/output levels shall be equivalent for all chip interfaces, whether contained in a single or multi-chip package. A VHSIC half-micron Bus Interface Unit (BIU) chip shall be developed to facilitate module interoperability with a Standard Interconnect System Bus. The BIU and any other VHSIC chips developed under this Phase 2 VHSIC Submicrometer Program shall interface directly to a Standard System Maintenance Bus to be defined by agreement among all the VHSIC Phase 2 Submicrometer Contractors and the Government COTRs. All these standards shall be documented and delivered."

In accord with the above paragraph, the Government established a Tri-Service Interoperability Committee to coordinate this requirement. To date, the four standards listed below have been developed. The standards exist as copyrighted documents and may only be copied in their entirety. The purpose of the copyright is to prevent the reproduction of multiple unauthorized versions. Users must quote a document in full, and state any exceptions which exist in their implementation. See references V.8 through V.11.

Application to VHSIC-1 Technology. Although the interoperability effort was implemented and funded through the Phase 2 contracts, it is applicable to any device intended to be used in systems employing VHSIC technology, including 1 micron and 1.25 micron devices. It is expected that any Phase 1 parts which are redesigned after government acceptance of these specifications will adhere to them. For most contractors this may require the redesign of the maintenance node interface on their chips. *The interface between VHSIC-1 and VHSIC-2 chips is assured by the adherence* to the 25 MHz data interface specification in the Electrical Specification.

Progress. The contractors have "stabilized" the PI-Bus, TM-Bus, and the electrical interfaces, and are presently working on integrating the proposed Joint Test Action Group (JTAG)/IEEE chip test interface standard with the ETM-Bus. It appears feasible to merge the two standards.

The Joint Integrated Avionics Working Group (JIAWG) Backplane subcommittee has reviewed the busses and has recommended that both the PI-Bus and the TM-Bus be the standard backplane busses for the ATA, ATF, and LHX programs. These recommendations are awaiting approval by the JIAWG steering committee.

Description of Standards: The following is a summary of the provisions currently in the standards:

(a) Electrical Interface Specification (Version 2.2 dated June 10, 1987) defines the standard VHSIC chip I/O voltage levels and drive currents. In addition, it defines the standard power supplies and clocks to be used with VHSIC-2 chips. The standard VHSIC chip power supplies are +3.3 V (+/- 5%) and +5 V (+/- 10%). The clocking scheme adopted consists of a 0-100 MHz system clock and a reference clock which operates at 1/16th of the speed of the system clock. Any other clocks applied to a VHSIC chip are to have no phase relationship applied to them. This was done to provide a standard on-board clocking scheme. Finally, a pin drive specification has been adopted which allows interoperability between VHSIC and standard TTL parts. See reference V.8.

(b) The PI-Bus (Parallel Interface Bus) is a system interface bus and references the Electrical Interface Specification for consistency. The current specification (Version 2.1 dated September 26, 1986) will connect up to 32 modules on a backplane. Depending on the loading, it can run from 12.5 MHz (full load) up to 25 MHz (lightly loaded). The Bus provides a choice of 16- or 32-bit wide data paths, in either an "error detection" or a "single error correction, double error detection (SECDED)" mode. These modes may all exist simultaneously on the same backplane. See reference V.9.

(c) The Test and Maintenance Bus (TM-Bus) is a serial backplane bus for test and maintenance signals. Version 2.0 (dated December 31, 1986) includes definitions of message protocols, broadcast capability, multicast capability, and TM-Bus interrupts. It references the Electrical Interface Specification and the PI-Bus for consistency. The TM-Bus supports a full range of clock frequencies up to 6.25 MHz. See reference V.10.

(d) The Element Test & Maintenance Bus (ETM-Bus) is a second maintenance bus. Its purpose is to provide an interface by which any user may connect to a VHSIC chip's maintenance port in a standard and well defined manner. The actual test instructions issued to the chip are a function of the class of built-in-test provided by the chip manufacturer, and are not provided by the specification. The bus provides for ring, star, or tree configurations (depending on system requirements). Version 2.0 (dated December 31, 1986) references the Electrical Specification for consistency. See reference V.11.

V.4 RADIATION HARDENING

V.4.1 Status of Phase 1 Hardness Levels

Radiation tests have been performed by the six Phase 1 contractors in order to characterize the tolerance of Phase 1 chips to the five major nuclear and space radiation threats: total dose effects, neutron damage, ionizing dose rate for upset and latchup, ionizing dose rate for survivability, and single event upset (SEU) produced by alpha particles, protons, and heavy ions. The tests were conducted under the Defense Nuclear Agency (DNA) program on Transient Radiation Effects in Electronics (TREE) in support of the VHSIC Program. DNA's principal objectives in supporting VHSIC have been (1) to insure that the VHSIC Phase 1 radiation hardness requirements and goals are met and (2) to enhance the hardness of selected VHSIC technologies in order to extend radiation tolerances to levels suitable for satellite applications.

All radiation testing during the program was performed in accordance with a DNA test approach that required the use of standard test procedures, the use of common or similar test facilities, and testing to failure, where practical. Test procedures were developed to provide general as well as specific guidelines for testing in each environment without being unnecessarily restrictive or imposing nonessential test requirements that would increase program costs beyond available resources. For example, total dose testing was permitted over a relatively wide range of dose rates to enable use of Co-60 gamma cells at contractor facilities. Tests at low and high military specification temperature extremes (-55^{0}C and $+125^{0}$C) were not imposed

largely because of budgetary constraints. With the exception of total dose and SEU tests performed using contractor-owned radiation sources, all tests were conducted at common Government test facilities in order to minimize source and spectrum-related variations in test data.

In accordance with DNA's test guidelines, a test plan describing proposed test devices, parameters to be measured, and specific test procedures was submitted by each contractor to DNA for review and approval prior to each test.

Although one of the major objectives of this work was characterization of Phase 1 device hardness, much of the total dose test data for some technologies was developed in support of continuing process development and hardening activities and are not necessarily representative of the final VHSIC processes. Also, potential latchup fixes are currently being evaluated for both the CMOS and the bipolar technologies and, if successful, may eventually be incorporated into the main Phase 1 processes. Thus, further improvements in radiation hardness are possible in these areas.

Tests were conducted on representative samples. These included partially functional VHSIC chips, macrocells, and test circuits, as well as discrete devices and test structures. None of the VHSIC chips or macrocells evaluated were tested at the 25 MHz maximum clock rate specified for Phase 1 devices. However, some test circuits were evaluated at this frequency. The current hardness capability of each of the eight Phase 1 technologies is summarized in references V.12 and V.14.

V.4.2 Other Radiation Hardening Activity

In order to further harden Phase 1 and Phase 2 chips to the levels required for various military applications, the VHSIC Program Office has funded the efforts described below. A list of the contractors, contract numbers, and points of contact is included in Appendix D. See also reference V.13.

(a) Motorola - Bulk CMOS

Motorola has radiation hardened its bulk CMOS Phase 1 technology to meet space radiation requirements. Extensive modeling of radiation induced upset in the 6K gate array has been performed. Radiation hardened 6K gate arrays have recently been fabricated on the VHSIC line at MICARL. Radiation testing and evaluation of these arrays will be completed by July 1988.

(b) GE/RCA - CMOS/SOS

RCA has completed the design of the VHSIC 64K Static RAM and completed first pass in December 1987. RAMs are undergoing initial evaluation. The program will end in June 1988 with the delivery of 30 fully functional space hardened 64K CMOS/SOS (8K X 8) RAMs for Government evaluation.

(c) Westinghouse/National Semiconductor

With VHSIC funding, DNA has contracted WEC/NSC to radiation harden the VHSIC bulk CMOS process at National Semiconductor and at Westinghouse (Baltimore). Recent results show that Westinghouse should be able to demonstrate

space radiation hardness with the VHSIC 10K gate array by November 1988. These hardened arrays will be made available through Chesapeake Corporation with NSC and WEC both capable of fabricating the radiation hardened arrays.

National Semiconductor has demonstrated the feasibility of producing space hardened 64K static RAMs operating at 3.3 V on the VHSIC line. Work is continuing to achieve space hardness in 5 V VHSIC 64K SRAMs by November 1988. The major problem is radiation induced increases in standby leakage currents.

(d) Hughes Aircraft - CMOS Silicon-on-Sapphire

Hughes has radiation hardened its CMOS/SOS Phase 1 technology and will provide radiation hard CMOS/SOS foundry services. In addition to a custom VHSIC design capability, Hughes is offering CMOS/SOS gate arrays. Further improvements in radiation hardness are being made under the SDI SAT 8.1 program funded through the U.S. Army Strategic Defense Command (USASDC).

(e) Texas Instruments - STL Bipolar

Under a contract started in October 1986, TI is eliminating dose rate induced latch up and increasing the dose rate induced upset threshold in its Phase 1 STL bipolar technology. It will provide a foundry for radiation hard VHSIC bipolar chips. The latching macrocells have been identified. A set of layout/processing design rules to eliminate latch up have been developed and verified. The immunity of Array Controller/Sequencer (ACS) chips will be measured as a demonstration of the hardening results by March 1988.

(f) TRW - 3D Bipolar

Under a contract started in October 1986, TRW is hardening its 3D bipolar Phase 1 technology against radiation induced latch up. Design and layout changes using test chips have been investigated and the latch up immunity on the CAM chip under gamma pulse irradiation has been demonstrated.

(g) Booz-Allen - Electromagnetic Effects

The goal of this program, awarded in 1986, is to improve the survivability of VHSIC chips in a severe electromagnetic environment. Booz-Allen is reviewing the varieties of input/output protection used on VHSIC/VLSI chips for electrostatic discharge (ESD) protection. It will analyze and select those approaches which will offer the most chip protection against other electromagnetic threats, including EMP and SGEMP.

In FY88, VHSIC chips will be subjected to pulses from bench type EME simulators.

V.5 PACKAGING TECHNOLOGY

The programs with Martin-Marietta, Hughes Aircraft, and Honeywell to develop two families of chip packages to accommodate VHSIC Phase 1 chips have been completed

These two families are: (1) perimeter chip carrier with terminals on 20 mil centers for surface mounting and (2) pin grid array package with pins on 50 mil center for through hole mounting applications.

The chip carrier package family has been coordinated with the standardization efforts of the JEDEC-11 Committee and has been defined for I/O's from 104 to 304 leads. The pin grid array chip package has been defined with I/O's from 120 to 480 leads.

Three VHSIC Packaging Workshops/Conferences have been held and a fourth one is planned for 1989. See references V.15-17.

V.5.1 Texas Instruments - Multichip Packages

This program, begun in 1985, established a source for multichip packages and the techniques by which a number of VHSIC chips can be interconnected within the package. The multichip packages have been fabricated by the subcontractor, Interamics, and are now available from that company. Two sizes, 196 I/O and 308 I/O, of packages have been tooled. The units have distributed power and ground planes and have provision for decoupling capacitors. Chip-to-chip interconnection is incorporated in a multilayer tape automated bonding (TAB) system which is customized for each chip combination and will fit a standard I/O pattern in the package. The interconnection materials used were thick film ceramic and a copper-polyimide structure.

During 1988, the ceramic processing involved in fabrication of the multi-chip packages will be improved to increase yield and decrease cost. The resultant package and interconnect network will be evaluated to assure that the interconnect structure and package are suitable for VHSIC-2 chip applications.

V.5.2 General Ceramics - Perimeter Chip Carrier Package

This program, begun in 1986, established a source for leaded and leadless perimeter chip carrier packages for surface mount application. Using the design generated by the subcontractor, Martin-Marietta, chip carrier packages with I/O counts of 124, 204 and 264 have been fabricated.

V.5.3 Honeywell - Tape Automated Bonding (TAB)

This program, begun in 1985, established the interconnection techniques and methods along with a source for the copper interconnection tape. The subcontractor, 3M, has developed a 70 mm two layer tape which is now available for use with VHSIC chips. The processes for chip bumping, inner lead, and outer bonding have been established.

V.6 LITHOGRAPHY

V.6.1 E-Beam Lithography - Hughes/Perkin-Elmer

The development of an e-beam lithography equipment with a capacity for high wafer throughput was considered to be necessary for the fabrication of 0.5 micron

feature size VHSIC chips on a pilot line basis. The system consists of an electron-optical column, work chamber, stage, vacuum system, system software, deflection and exposure circuits, automated loading system, and a pattern data interface which is compatible with the VHDL design language. Wafer processing capacity (throughput) is specified to be at least four wafer levels per hour (with four inch wafers).

A three year contract was awarded to Hughes Research Laboratories in May 1981, with Perkin-Elmer Corporation (PE) as the major subcontractor. The contract continued until final tests in February, 1985. Perkin-Elmer is now marketing the machine as the AEBLE-150.

At the beginning of 1987, PE had completed the first phase of software control and support, column rework to improve resolution and reduce distortion, and the pattern modification software for converting CAD pattern data to hierarchical pattern software. Delivery of the first AEBLE 150 machine was made to Motorola in September 1986.

During 1987, commercialization has taken place for production and delivery of AEBLE-150 machines to several customers. Perkin-Elmer has improved all of their software, operating, and fabricating specifications, and their throughput has exceeded VHSIC requirements. Work is still continuing to improve the software and overlay accuracy.

V.6.2 X-Ray Lithography - Perkin-Elmer

The goal of this program is to develop an X-ray lithographic machine which would reduce the cost of producing submicron chips for moderate production volume. See reference V.18. The key features of the X-ray step-and-repeat (XSAR) machine development are:

- o 0.5 micron resolution
- o 20 wafer levels per hour throughput (with a 10 microJoule/cm^2 resist sensitivity) and four inch diameter wafers
- o development of a source for the fabrication of high quality masks
- o development of a pulsed plasma X-ray source for increased throughput.
- o installation and testing of the tool in a VHSIC Phase 2 pilot line.

The XSAR tool was assembled without the software for the automated feature of field-by-field alignment and wafer input-output handling. Test exposures and overlay accuracy were evaluated. Data limited by mask constraints showed that 0.1 micron overlay was achievable.

The boron nitride masks with 0.5 micron feature sizes were produced at the contractor's facility at a rate of about three per week.

The subcontractor, Maxwell, completed the fabrication of a high brightness plasma X-ray (HBX) source and demonstrated a 10 Hz pulse rate capability at one-third the required brightness.

During 1987, the software for automatic field-by-field alignment and wafer handling was completed. Full ten kilowatt operation of the tungsten rotating anode has been

accomplished with a source spot size of less than the required 1.5 mm. The contractor fabricated a complete XSAR second rotating anode source subsystem including a second XSAR base frame in preparation for the pilot line characterization effort. A subcontractor for this effort will be chosen in January 1988.

The X-ray mask fabrication problems of adhesion, absorber uniformity and wall slopes, membrane stresses, and defect control were solved. Selected masks were used in performing the XSAR acceptance performance tests to qualify the tool. Unexpected physical effects were discovered in evaluation tests of the HBX source which prevented further evaluation.

In 1988 and beyond, the XSAR tool will be operated in a pilot line environment. The X-ray mask development work will continue as part of the pilot line program.

V.6.3 Advanced Wafer Imaging System (AWIS) - GCA Corporation

The Advanced Wafer Imaging System (AWIS) is designed to meet the need for high resolution, high throughput lithography by extending optical lithography beyond its present limitations. The goal is to design a production prototype machine which can produce 0.5 micron chips of at least one square centimeter area and 0.1 micron alignment accuracy at a rate of 25 4-inch wafers per hour. The successful completion of the program would provide a cost effective production lithography for VHSIC/VLSI manufacturing. GCA has been designing a prototype optical stepper system (the AWIS Evaluator) by incorporating a laser/lens subsystem into a DSW 8000 frame.

At the beginning of 1987, lens qualification testing had been completed successfully. A 248 nm excimer laser source adapted to the lens and stepper frame provided sufficient illumination for throughput needs but required stabilization.

During 1987, stabilization of the illumination was achieved and the stepper system was brought within the focus control specification. The illumination system was incorporated into the DSW 8000 frame. The tool was accepted as a VHSIC 0.5 micron optical stepper. It was shipped and installed in the IBM facility in Manassas, VA to undergo characterization in the VHSIC-2 pilot line.

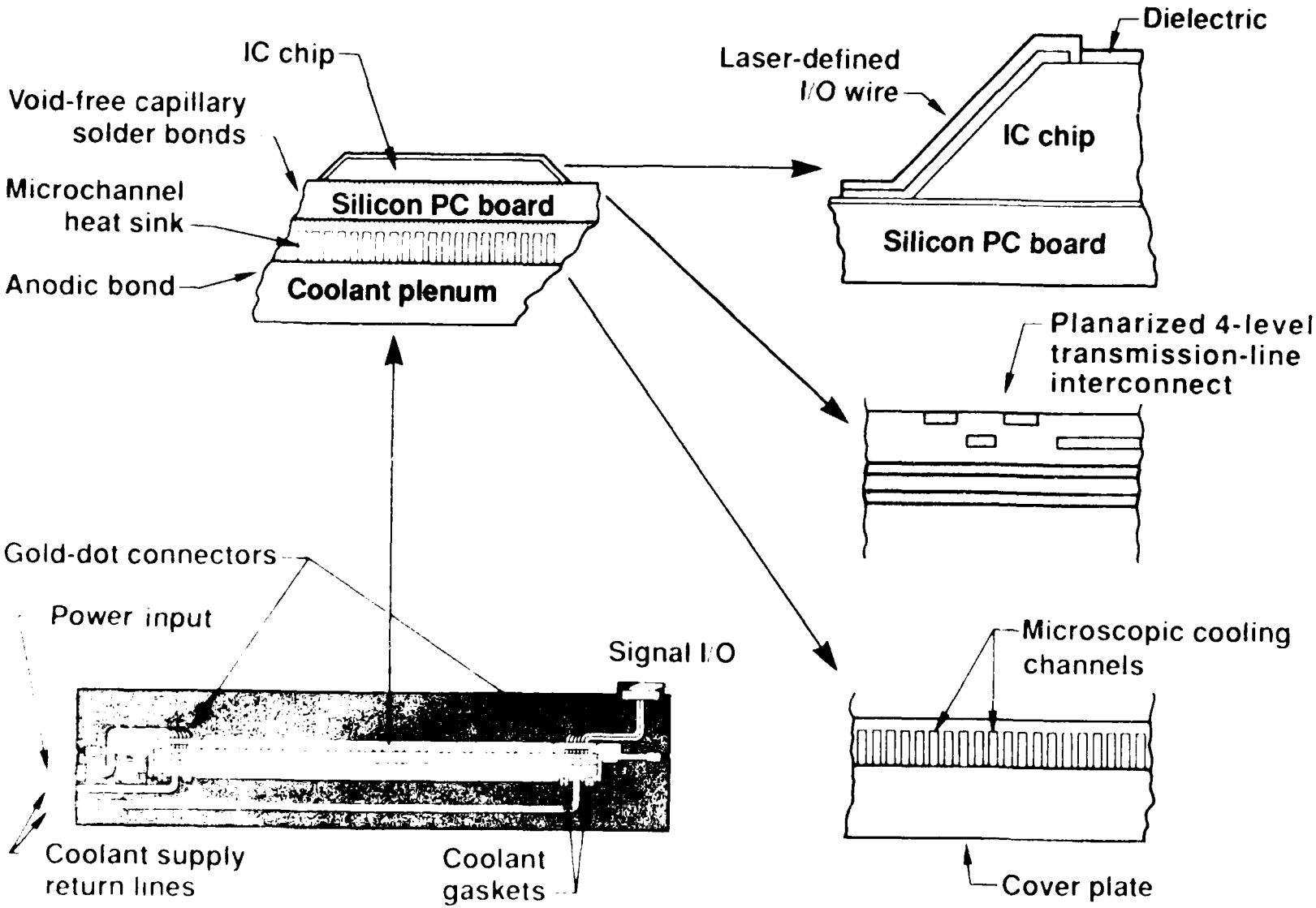
In 1988 and beyond, the AWIS Evaluator will be used in the IBM VHSIC pilot line for patterning of 0.5 micron devices. After twelve months of such effort, it will be shipped to the University of California, Berkeley, CA, for optical stepper modeling development work related to activities of the Semiconductor Research Corporation.

V.6.4 Laser Pantography - Lawrence Livermore National Laboratory (LLNL)

The goal of the Laser Pantography (LP) project is to develop advanced packaging and interconnection technologies which would make major improvements in military system performance, and significant reductions in the size and weight of such systems. Laser pantography processing is fast, flexible, and low cost. It can be used to provide interconnections on the chips and between the chips mounted on silicon wafers as substrates for hybrid wafer-scale integration.

A multi-step laser patterning process (see Figure V.3) has been developed which enables discretionary patterning of vias and metallization over 3-dimensional

Wafer-Scale Supercomputer Technologies



LASER PANTOGRAPHY TECHNIQUES

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FIGURE V.3

(non-planar) surfaces. The autofocusing capability of the LP equipment allows the lithographic process to follow the terrain of the surface and avoid the stringent requirement of planarization needed in conventional lithography in order to stay in focus. Using this technology, a chip-to-wafer interconnection technique has been developed with as many as 1600 gold thin-film wires around the edge of a 1-cm square chip.

To demonstrate this hybrid interconnect technology, LLNL has fabricated fully functioning 2-chip memory hybrids, employing VHSIC 64K static RAM chips. A more complex 10-chip memory hybrid is being developed for aerospace applications.

LLNL has also made significant progress on non-laser processing. Using enhanced reactive-ion-etching, LLNL has successfully etched Al-Cu(2%) anisotropically in a single-wafer etcher. Experiments are also being conducted on in-situ planarization of the aluminum alloy during deposition.

Other accomplishments in 1987 include fabrication of four-level metallization structures using laser planarization and fabrication and testing of thin-film transmission lines for wafer-scale interconnect using laser pantography.

V.7 RELIABILITY AND QUALIFICATION

V.7.1 Introduction

The insertion of VHSIC technology requires an approach which results in earlier qualification of devices with a less costly and time consuming process while, at the same time, retaining the improvement in reliability offered by the new technology. VHSIC has funded several programs on "generic" qualification procedures and reliability enhancement and assessment to achieve these goals.

This approach relies to a large extent on the use of surrogate devices for controlling the process and revealing quality and reliability problems. CAD tools are fully integrated into the certification procedure, since performance is based on these tools. Chip families and packaging techniques which apply to more than one device are dealt with generically. Design specific information is reported in the specification. Qualification testing is performed on samples of the chip family on a periodic basis.

V.7.2 Qualification Procedures - GE, AT&T, Honeywell

A contract was awarded in September 1986, to General Electric, AT&T, and Honeywell to address microcircuit qualification issues. The cost, complexity and relatively low quantity production needs of high technology VHSIC devices suggest that it is no longer economical to individually qualify piece parts. The generic qualification concept is based on Statistical Quality Control and Statistical Process Control (SQC/SPC) procedures whereby a microcircuit design and manufacturing process is characterized and continually monitored to assess its quality. Alternate screens for high magnification precap visual, new in-process controls to replace some end-of-line screens, wafer acceptance, and SQC/SPC provisions in addition to modified qualification requirements for custom or complex microcircuits have been included. A certified design and process capability is listed on the Qualified Manufacturers List (QML). A

product built in a QML facility is qualified for insertion into DoD systems after passing MIL-STD-883 test procedures. The costly Qualification Conformance Inspection (QCI) requirements are reduced through the use of process-representative evaluation circuits. The key to the success of this procedure is the development of certification vehicles to be implemented on the design and process flow to determine certifiability. For the design procedures, software benchmarks to assess manufacturers' CAD systems are envisioned. In the fabrication procedure, the development of test structures is required. An Industry Coordinating Working Group (ICWG) provides a real-time critique of the newly developed procedures to implement the generic qualification concept. The initial draft procedures will be reviewed in 1988.

V.7.3 Reliability Assessment of Gate Arrays - GTE

A contract was initiated in August 1986 to focus on the generic qualification problems for gate arrays and to determine the reliability of representative products. RADC released two detailed specifications for gate arrays (MIL-M-38510/605 and /600 for CMOS and bipolar technologies, respectively) in February 1987. These documents employ novel "generic qualification" procedures. Basically, GTE will perform two main tasks: one will be to review the two slash sheets, and the second will be to obtain representative products of the process and design system (Standard Evaluation Circuits, or SECs) and subject these devices to stress-step testing and life-testing. The results of the life-testing will be used to modify the detail specifications where necessary in an attempt to strengthen these documents and insure higher quality, higher reliability gate array products.

V.7.4 Non-destructive Bond Testing

This effort is developing a method for testing the quality of metallurgical bonds formed in the process of connecting VLSI/VHSIC chips to their packages by means of tape automated bonds (TAB). The end item of this program will be a report detailing the test method developed.

Vanzetti Systems is developing a test method using infrared-thermal non-destructive techniques which will be submitted for coordination and implementation in MIL-STD-883. A non-destructive evaluation technique with the necessary resolution to assess these chip and package metallurgical bond sites will also be developed, and the parameters that distinguish an acceptable bond from a defective one will be established. The contract effort began in March 1986.

The recent growth of TAB technology has evoked broad industrial interest in automatic inspection methods for TAB bonds where lead widths can be as small as two mils. Under VHSIC funding, the Vanzetti is extending its present inspection methods to these smaller sizes. An experimental laser/thermal inspection system for TAB bonds has been in operation since the summer of 1986 and routinely reveals lifted and deformed leads, contamination, solder quality anomalies, and other deviations from normal. The laser heating spot is just two mils in diameter. Exposure durations as short as 60 msec raise the target surface temperature by some 50-100^{O}C above room temperature. With somewhat longer exposures, the solder can be reflowed. This phenomenon is being explored as a means of repairing lifted leads immediately after they are found during the inspection process and, indeed, as a possible method of restoring soldered TAB bonds in the first place. Combined with the continuous

thermal monitoring which is already available, it makes possible the precise control of solder temperature, joint by joint, followed by the automatic inspection process.

Sonoscan is developing a test method using acoustic non-destructive techniques that will be submitted for coordination and implementation in MIL-STD-883. The contract was awarded and work was started in March 1986. A matrix of TAB inner and outer lead devices with a built-in range of quality is being investigated. Each bond interface is being documented acoustically and then pull-tested to develop a database upon which to formulate a specific test method. Preliminary data demonstrate good correlation between the degree of bonding and correlative pull tests (destructive). Optical inspection of the bonds prior to the acoustic microscopy could not detect differences in the bonds. This investigation is being performed with a Scanning Laser Acoustic Microscope (SLAM) to produce real-time images at 30 frames per second. The speed of scan and the practicality of acoustic microscopy demonstrated in other non-destructive testing applications make the method potentially viable for non-destructive evaluation of TAB.

V.7.5 Reliability Prediction Modeling

A contract was awarded in September 1986 to an IIT Research Institute team to develop failure rate prediction models for CMOS VHSIC and advanced VLSI microcircuits. This effort involves the characterization of each possible failure mechanism and the statistical combining of probability density functions (PDF) describing each mechanism into a usable prediction model form.

The literature has been reviewed and identification of the failure modes and mechanisms has been completed. Honeywell has identified which test structures will be utilized in the model development. IIT Research Institute has developed preliminary PDFs for electro-migration, time dependent dielectric breakdown, and hot carrier effects.

The model(s) will be validated with field data accrued over the course of the model development. The final models will be available by September 1988 and will then be proposed for inclusion in MIL-HDBK-217, "Reliability Prediction of Electronic Equipment."

V.7.6 VHSIC Impact on System Reliability

One of the goals of the VHSIC program is to improve weapon system reliability. Improvement is expected because a few, very complex, high speed parts can replace a large number of less complex, slower parts. Under a contract awarded in April 1985, General Dynamics has assessed the impact of this change on system reliability. The study compared VHSIC designs with contemporary non-VHSIC designs. The characteristics reviewed and evaluated were: complexity, interconnections, packaging, derating, thermal design, fault tolerance, weight, and size.

The F-16 weapon system was used as the contemporary non-VHSIC baseline since General Dynamics had large volumes of data on the system. VHSIC component failure rates were estimated by using the primary failure mechanisms and the F-16 data for medium scale ICs as a starting point. Assumptions were then made for potential VHSIC susceptibility and technology improvement factors. The VHSIC functions evaluated

were: VHSIC Common Signal Processor (IBM), V1750A Processor (TRW), AN-ALQ-131 (TRW), and Multi-mode Fire and Forget Electronics (TI). According to these estimates the VHSIC failure rate goal of 0.06 failures per million hours may be achievable for a ground (benign) environment. This study indicates that VHSIC parts should have approximately 1.7 failures per million hours in a harsh, fighter aircraft environment.

System improvement estimates were based on replacement of a conventional signal processing system with a functionally equivalent VHSIC system. The result is an estimated 12 percent improvement in mean-time-between-maintenance for the entire weapon system. For the processing subsystem alone, the estimated improvement can be 10 to 1 if cooling, comprehensive testability, and quality screening are implemented. Thermal management is considered a primary area of concern due to the density and power levels for VHSIC parts. The report recommends that the average junction temperature for all VHSIC parts be limited to $55^{O}C$, which is about $30^{O}C$ less than the current trend.

CHAPTER VI

INFORMATION SOURCES

INFORMATION SOURCES

VI.1 TRAINING

The VHSIC Program Office, from the outset, recognized that the transfer of VHSIC technology and products to both the DOD contractor community and DOD acquisition managers is essential for program success. It also recognized that historically this had been a difficult task to achieve. Novel approaches were needed to ensure that system designers would not only have access to VHSIC technology but also to VHSIC software and devices as quickly as they became available. Part of this effort is being carried out in the military weapon system technology insertion projects. An additional part of this effort is the VHSIC training and information program.

A major source of information for the defense community is and will continue to be the Defense Technical Information Center (DTIC). DTIC has on file well over 1000 documents relative to VHSIC and VHSIC related technology. DTIC is accessible to qualified users, including U.S. Government agencies, their contractors, subcontractors, and potential contractors who have established a "need to know" at DTIC. The DTIC phone number is (202) 274-6871.

The VHSIC training program began in January 1984 in order to provide:

- o system managers and senior engineers with an awareness of the VHSIC products and design technologies being developed, and
- o working level engineers with instruction in the design of systems using VHSIC products through hands-on design workshops.

The primary techniques for accomplishing these objectives have been regional workshops, conferences, presentations, and brochures. For the hands-on workshops, special software has been developed for using VHSIC design tools, and detailed technical reference material has been prepared in the form of application notes, performance data sheets, and text books.

VHSIC Application Workshops were organized and held throughout the country on a regional basis. The workshops provided comprehensive training and education in VHSIC technology for defense contractor personnel for the purpose of accelerating the application of VHSIC technology in military electronics. More than 3000 engineers and technical managers have attended them. Over thirty such workshops were held from 1984 through 1986.

The scope and depth of coverage of VHSIC technology at these workshops have enabled each attendee to evaluate the feasibility of using VHSIC technology in specific military system applications. Attendees were given the opportunity to present both application and work-related problems which were discussed by the group in terms of how VHSIC can be applied. The attendees were provided with approximately three days of instruction using text material which they took with them for future use in electronic design and interface with the VHSIC community.

The instructional material (available from DTIC) included:

- Student Guide - a compilation of VHSIC design data and chip architectures
- VHSIC Specification Guide - an abbreviated version of all of the VHSIC chip specifications
- Interface Reference Guide - a collection of technical and management information about ICs, Computer Aided Design (CAD) availability, documents available, as well as key Government and industry personnel.

A number of similar workshops have been held for DOD and other Government personnel at such in-house facilities as the Naval Ocean Systems Center (San Diego), the Naval Weapon Center (China Lake), Eglin Air Force Base (Florida), and the NASA Johnson Spaceflight Center (Houston).

A major follow-on effort to the Applications Workshops was developed by the Johns Hopkins University Applied Physics Laboratory and was initiated in June 1985. Called "Applications II", it was intended for those system designers who had attended the regional workshops. It built on their knowledge from earlier workshops and concentrated exclusively on how to design electronic subsystems using VHSIC products. This two day training program allowed hands-on use of some of the CAD tools developed for the VHSIC Program. Four Applications II workshops were held during the summer of 1985. Further extensions of these workshops were "Applications III" held by JHU/APL in October 1986, and "The Advanced Hands-On Applications Workshop IV" (or VHSIC Tech-Fair) held in July 1987.

During 1987, several training workshops, seminars, and courses were held. These have included the following:

- VHSIC Tech-Fair, Advanced Hands-On Applications Workshop IV, cosponsored by the DoD VHSIC Program Office and the Johns Hopkins University Applied Physics Laboratory, Laurel, MD, June 30-July 2, 1987.
- IDAS Workshop, sponsored by the DoD VHSIC Program Office, held at University of Cincinnati, Cincinnati, OH, August 19-21, 1987
- VHDL Users Group Workshop, sponsored by the DoD VHSIC Program Office, held at Virginia Polytechnic University, Blacksburg, VA, October 20-22, 1987
- Seminar on VHSIC Technology and Applications Design, sponsored by Palisades Institute for Research Services, November 3-5, 1987
- VHDL Tutorial, sponsored by the IEEE, ICCAD, Santa Clara, CA, November 9, 1987

The following training courses and materials are now available:

- o VHDL course, offered by CAD Language Systems, Inc. Call (301) 424-9445.
- o VHDL training course, offered by Intermetrics. Call (301) 657-3775.
- o VHDL training tape (Version 7.2), available from the Air Force Institute of Technology. Capt Richard Linderman, (513) 255-3576.
- o "VHSIC: The Answer", a video tape for use in informing DoD and industry program managers of the capabilities and benefits of using VHSIC in weapon systems.
- o ADAS Training Course, offered approximately five times a year by Research Triangle Institute; at RTI or on-site. Contact Liz Bentley, (919) 541-6830

VI.2 CONFERENCES: 1987

In addition to the training workshops listed above, the following conferences or workshops were held during 1987:

- o 1987 VHSIC Packaging Conference, sponsored by the DoD VHSIC Program office, April 21-22, 1987
- o 1987 VHSIC Qualification, Reliability, and Logistics Workshop, sponsored by the DoD VHSIC Qualification Committee, August 25-27, 1987
- o 1987 VHSIC Conference, sponsored by the DoD VHSIC Program Office, held at the Johns Hopkins University Applied Physics Laboratory, Laurel, MD, November 17-19, 1987.
- o 1987 Government Microcircuit Applications Conference, sponsored by the DoD, October 27-29, 1987 (VHSIC Applications Session).

Proceedings of the 1987 and earlier conferences are listed as references VI.1 through VI.13.

VI.3 1988-89 WORKSHOPS AND CONFERENCES

For 1988 and 1989 the following workshops, meetings and conferences are now planned or are under consideration.

- o 1988 VHDL Workshop, cosponsored by the University of Virginia and the IEEE Computer Society/Design Automation Technical Committee, to be held at University of Virginia, Charlottesville, VA, April 18-20, 1988. For information, call (804) 924-6086
- o VHDL Users Group Workshop, April 1988. For information call Lt R. Miller, (513) 255-8662

- o VHDL Training Workshop for University Faculties, late summer 1988. For information call Lt Naclerio, (513) 255-8633

- o 1988 VHSIC Qualification, Reliability, and Logistics Workshop, sponsored by the DoD VHSIC Qualification Committee, to be held at Scottsdale, AZ, September 27-29, 1988. For information, call E. Hakim, Army ETDL, (201) 544-2185.

- o 1988 VHSIC Conference. For information call E.C. Urban, (202) 697-9216.

- o 1989 VHSIC Packaging Conference. For information call O. Layden, Army ETDL, (201) 544-2378

- o TISSS (Tester Independent Support Software System) Industry Review, May 24-25, 1988, Orlando, FL. For information call Capt. William Russell, Jr., (315) 330-3974., RADC/RBE-1.

- o TISSS System Training Course, June 1988, RADC, Rome NY

VI.4 VHSIC TECHNICAL DATABASE

A centralized information system to organize the technical database generated by the VHSIC system and to provide access to it by the entire defense community was developed. It resides on a Micro-VAX at the Naval Ocean Systems Center (NOSC), and runs under Unix 4.3. It contains information in the following categories: integrated circuits, applications, technical documents, projects and contracts, briefing materials, software tools, training, and personnel. In June 1987, the DoD security officer approved the procedure for granting contractors access to the database. A VHSICnet (database and Unix utilities) manual is being developed to familiarize users with the system. RADC has proposed that a VHSIC Information Analysis Center (VIAC) be established at RADC as an adjunct to the Reliability Analysis Center. It would be a central point for dissemination of VHSIC information. For further information, contact Dr. David Roberts at the NOSC, San Diego, California, (619) 553-4954.

VI.5 VHSIC POINTS OF CONTACT

In the course of learning about VHSIC, questions may arise which have not been covered in published documents. At other times, the kind of information required may be so loosely defined that a personal contact can be helpful in providing initial assistance, advice, and contacts. The people listed in Appendix C as System Design Experts and VHSIC Issue Experts have agreed to serve as initial points of contact to provide preliminary information in getting started in VHSIC.

Contacts for information about work on specific contracts may be found in Appendix D (VHSIC Contracts - Points of Contact).

CHAPTER VII

POLICY

POLICY

VII.1 THE USE OF VHSIC: SYSTEM INSERTION

This section discusses three policy items relating to the use of VHSIC in military systems:

- o VII.1.1 A (draft) directive emphasizing that DoD should exploit the advantages of VHSIC technology in all procurements containing components for signal processing, data processing, or electronic control functions
- o VII.1.2 A definition of VHSIC for use by the Defense Electronics Supply Center (DESC) in labeling VHSIC devices in the process of qualification
- o VII.1.3 Proposed revisions of Requirement 64 of MIL-STD-454, Standard General Requirements for Electronic Equipment to reflect advances in microelectronic technology resulting from the VHSIC program.

VII.1.1 "VHSIC in Defense Systems": DoD Directive (draft)

In January 1987, the Under Secretary of Defense distributed a draft DoD Directive, "Very High Speed Integrated Circuits (VHSIC) Technology in Defense Systems," to the Services for comment. The cover letter addressed the role of electronic technology as a "force multiplier" for DoD weapon systems.

The document stated that it is the policy of DoD to exploit the many advantages of VHSIC technology in all procurements of Defense systems having subsystems or components for signal processing, data processing, or electronic control functions. This includes both new systems and upgrades and retrofits. The advantages cited include life-cycle cost, speed, performance, power, reliability, size, testability, logistics supportability, and flexibility to meet changing threat environments.

The evolution of technology was recognized, and the draft addressed the issue of rapid obsolescence of integrated circuits relative to the lengthy system acquisition cycle. The document called for the following to further the benefits available with this technology:

- o VHDL descriptions of circuits being used in DoD systems,
- o DESC certification of fabrication lines,
- o Built-in test covering 95% of logic
- o Interoperability standards for interfaces, testing and maintenance, and
- o Design simulation at the behavioral and logic gate levels to verify design of the entire electronic subsystem.

Appendix A-1 is a complete copy of the draft directive. Separate actions taken by the Navy and the Army for the same purpose are shown in Appendix A-2.

VII.1.2 Definition of VHSIC

A general objective of the VHSIC program was to stimulate the U. S. semiconductor industry to provide a capability to design and manufacture technologically advanced electronic equipment for U. S. military systems. The VHSIC program also helped to define a framework for military system design which includes those features considered highly desirable - performance, test and maintainability, reliability, and ability to upgrade to meet new threats. The chips must be designed and manufactured to support this framework.

In July 1987, the VHSIC Office offered guidelines to the Defense Electronics Supply Center (DESC) for use in labeling VHSIC devices in the process of qualification. VHSIC devices will be identified as VHSIC in the tables of MIL-STD-1562 which lists qualified parts. The following excerpts from the letter of transmittal to DESC explain the reason for the guidelines:

> "Since the (VHSIC) Program was designed to increase the technological level of integrated circuit manufacturing available to DoD, it benefits DoD to have many qualified VHSIC manufacturers. The larger the variety of interoperable VHSICs available to military system designers, the more flexibility they will have to design the high performance systems required by our defense strategy.
>
> Manufacturers providing this technology are encouraged to qualify their products to MIL-M-38510 (JAN). The guidelines below shall be used to determine which devices meet VHSIC-1 requirements. The primary source of these guidelines is the VHSIC Phase 1 Statement of Work. During the course of the VHSIC Program, requirements were refined to reflect the needs of system insertion. We believe that newly designed and redesigned VHSIC's should meet these tighter requirements."

Requirements cover minimum feature size, functional throughput rate, clock speed, VHDL descriptions, JAN qualification, radiation hardness, testability, and built-in-test (BIT). Requirements for BIT coverage, interoperability, and temperature range are increased to Phase 2 levels for new chip designs and chip redesigns.

The full text of the guidelines is reproduced in Appendix A-3. Manufacturers may discuss the application of these criteria to specific devices with DESC/ECS. For further information, see Government Points of Contact, Appendix C.

VII.1.3 MIL-STD-454: Proposed Revisions to Requirement 64

An array of military standards influence the design and manufacture of systems for military use. Requirement 64 of MIL-STD-454 contains requirements and guidance on the use of microelectronic devices. As a prime reference for use of microelectronic components, this requirement reflects the objectives of DoD for military components as well as current technology and capabilities. In order to maintain currency, the requirements of MIL-STD-454 are reviewed twice yearly.

Amendments to Requirement 64 have been drafted which require use of advanced technology microcircuits to achieve system performance objectives and reduce the risk of obsolescence. Advanced technology microcircuits are defined in terms of

performance, technology, capability to include system level Built-in-Self-Test through standard test busses, and ease of documentation and specification. VHDL descriptions of devices used in systems were also required. These draft amendments were circulated for comment in November 1987 by the MIL-STD-454 Coordinator, Roger Faust, AFASD/ENES at Wright Patterson AFB. The technology issues, particularly VHDL and TISSS, are the subjects of discussion between the Government and various industry committees involved in reviewing Government standards.

Following review by the MIL-STD-454 Government-Industry Advisory Committee, the amendments to Requirement 64 may be incorporated in whole or in part. If they are incorporated, the Requirement will facilitate and encourage the use of VHSIC technology in systems.

The draft revision to MIL-STD-454, Requirement 64 is reproduced in Appendix A-4.

VII.2 TECHNOLOGY SECURITY

The development of VHSIC Technology and its subsequent insertion into weapons systems will enable the U.S. to maintain its technological advantage over the numerically superior Soviet Union. In order to guard against the overt or covert acquisition of advanced technology by the Soviet Union, the Department of Defense established internal controls to bridge the gap between existing Government regulations and open, commercial technology. The existing regulations include the International Traffic in Arms Regulations (ITAR) of the Department of State and the Export Administration Regulations (EAR) of the Commerce Department. The DoD internal controls of policy and procedures for the advanced technology (VHSIC) safeguards were promulgated in DoD Instruction 5230.26, "Very High Speed Integrated Circuit (VHSIC) Technology Security Program." While this instruction could be readily implemented within the Department of Defense, it was not easily to implement in solicitations or contractual agreements in a complete or consistent manner.

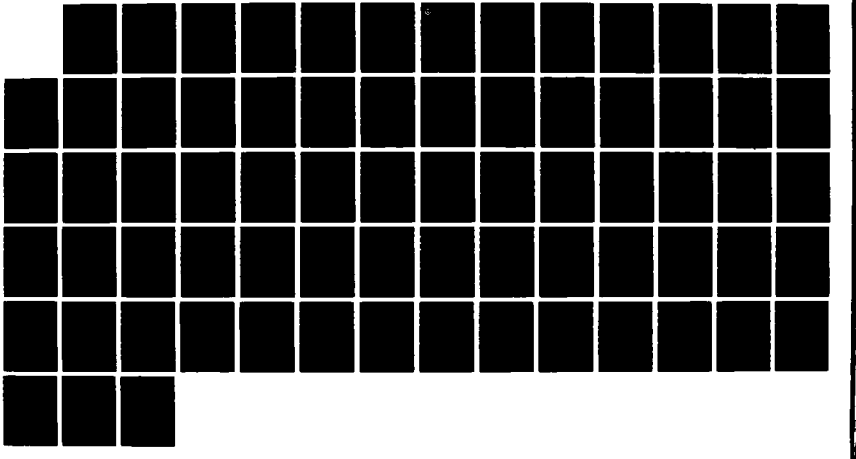
It has been determined that the best way to ensure some degree of dissemination [illegible] the information and maximize consistency in compliance would be to incorporate [illegible] requirements of DODI 5230.26 into the Defense Supplement to the Federal Acquisition Regulations (DFAR). Implementation of a particular DFAR still rests with individual program managers, but consistency of implementation would be improved.

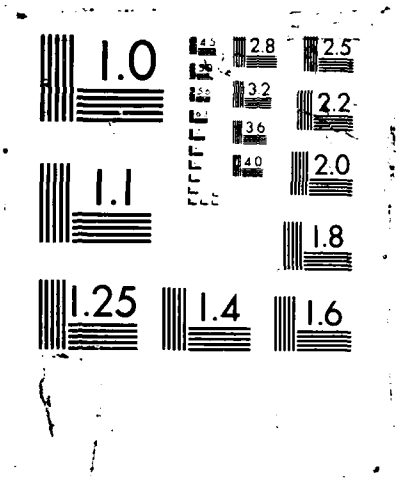
The requirements were proposed in the form of an amendment [illegible] and submitted for review. The Federal Acquisition Regulation [illegible] completed their review and authorized an interim rule [illegible] prescribes a contract clause for uniform use in all contracts [illegible] interim rule, which was published in the Federal Register [illegible] into effect immediately, and will expire on January [illegible]

In accordance with the interim rule, all [illegible] involving VHSIC must advise the contractor [illegible] of VHSIC-sensitive information [illegible] of Enclosures (2) and (4) to DoDI 5230.26 [illegible] interim rule have been implemented.

AD-A193 225 VERY HIGH SPEED INTEGRATED CIRCUITS (VHSIC)(U) OFFICE OF THE UNDER SECRETARY OF DEFENSE (ACQUISITION) WASHINGTON DC VHSIC P ROGRAM OFFICE 31 DEC 87 2/2

UNCLASSIFIED F/G 9/1 NL

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contracts are in the process of being modified to incorporate these new DFAR clauses. In a few other cases, contractors have been certified in accordance with these procedures, however, their contracts have not been renegotiated or modified to include these clauses.

Another security issue concerns the development and promulgation of a VHSIC export control policy. The USD Policy Memorandum (Reference I-09352/87) document, "Department of Defense Policy Regarding International Transfer and Export Control of Very High Speed Integrated Circuits (VHSIC) Technology, Goods, and Services," has an effective date of October 13, 1987. This policy is a major step toward striking a reasonable balance between the need for enhanced safeguards to protect this militarily critical technology and the economic imperative to share advanced VHSIC technology with our Allies.

The policy establishes guidelines for the release of VHSIC technical data and products under Foreign Military Sales, cooperative programs, and commercial exports. For the purposes of this policy, VHSIC devices are defined as "semiconductor devices which are specifically designed for military application" that have "a throughput rate of 1×10^{11} gate-hertz per square centimeter". VHSIC technology is defined to include "the VHSIC devices themselves, the technical data related to these devices, and the software specifically developed for the design, manufacture and test of VHSIC devices".

VHSIC devices incorporated in U.S. weapons systems could be exported to our allies and friends provided appropriate security measures are implemented to protect the technology. The policy authorizes the release of VHSIC products and technology for insertion into weapons systems of allied nations subject to specified minimum safeguard security measures. Release of VHSIC production technology, detailed design information, and specially designed software for VHSIC technology is prohibited to foreign sources.

A copy of the Federal Register announcement of the interim rule of the DFAR is shown as Appendix A-5 and the DoD VHSIC export policy document appears as Appendix A-6.

APPENDICES

APPENDIX A.1 - "VHSIC IN DEFENSE SYSTEMS": DOD (DRAFT) DIRECTIVE

ACQUISITION

THE UNDER SECRETARY OF DEFENSE

WASHINGTON, DC 20301

9 JAN 1987

(R&AT)

MEMORANDUM FOR CHAIRMAN, JOINT CHIEFS OF STAFF
UNDER SECRETARY OF DEFENSE (POLICY)
ASSISTANT SECRETARY OF DEFENSE (COMMAND, CONTROL, COMMUNICATIONS AND INTELLIGENCE)
ASSISTANT SECRETARY OF DEFENSE (COMPTROLLER)
GENERAL COUNSEL, DEPARTMENT OF DEFENSE
INSPECTOR GENERAL, DEPARTMENT OF DEFENSE
ASSISTANT SECRETARY OF THE ARMY (RESEARCH, DEVELOPMENT AND ACQUISITION)
ASSISTANT SECRETARY OF THE NAVY (RESEARCH, ENGINEERING AND SYSTEMS)
ASSISTANT SECRETARY OF THE AIR FORCE (RESEARCH, DEVELOPMENT AND LOGISTICS)
DIRECTOR, DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
DIRECTOR, DEFENSE COMMUNICATIONS AGENCY
DIRECTOR, DEFENSE INTELLIGENCE AGENCY
DIRECTOR, NATIONAL SECURITY AGENCY

SUBJECT: Review of Draft DoD Directive for Very High Speed Integrated Circuits (VHSIC) Technology in Defense Systems

The electronic technology of integrated circuits (IC) has become the foundation of our complex and sophisticated DoD weapon systems. Advanced electronics in weapon systems are our present "force multipliers." By the late 1970's, our lead in IC technology, both commercially and militarily, had seriously eroded. Hence, the VHSIC program was established with a goal to reverse this erosion of technology in weapon systems. The VHSIC program developed two new generations of advanced IC technology specifically designed to meet military system needs and provided the capability to support the weapon systems for their total operational life cycle.

To date, as a direct result of the VHSIC program effort, we are clearly leading IC technology commercially and militarily, both in IC computer-aided design and in IC fabrication technologies. The real success of this program is the ability of the DoD acquisition community to effectively employ and utilize the evolving advanced capabilities to maintain the "force multiplier" posture.

APPENDIX A.1

The impact of the enclosed Draft DoD Directive on our future weapon systems acquisition is significant, and as such, requires careful review, consideration, and comment by all. This draft Directive establishes policy for implementing VHSIC technology in the future. I request your review and comments be provided within 30 days. We will incorporate any necessary solutions or clarifications into the final DoD Directive. My point of contact is Dr. David Patterson, Defense Technology Analysis Office (VHSIC/ED), phone number (202) 697-4198, Room #3D139 (1211 S. Fern St.), The Pentagon, Washington, DC 20301.

Attachment

APPENDIX A.1

Department of Defense
DIRECTIVE

DRAFT

NUMBER

SUBJECT: Very High Speed Integrated Circuits (VHSIC) Technology in Defense Systems

References: (a) DoD Directive 5000.1, "Major System Acquisitions," March 12, 1986

(b) DoD Directive 5000.39, "Acquisition and Management of Integrated Logistic Support for Systems and Equipment," November 17, 1983

(c) VHSIC Hardware Description Language, version 7.2

(d) MIL-STD-976, "Certification Requirements for JAN Microcircuits," October 5, 1981 (or superseding version)

(e) VHSIC Interoperability Standards

(f) MIL-STD-883, "Test Methods and Procedures for Microelectronics," November 29, 1985 (or superseding version)

(g) MIL-M-38510, "General Specifications for Military Specification Microcircuits, October 31, 1983 (or superseding version)

A. PURPOSE

This Directive establishes DoD policy and provides guidance and direction for using Very High Speed Integrated Circuits (VHSIC) technology in all new Defense systems and system upgrades.

DRAFT

B. APPLICABILITY AND SCOPE

This Directive:

1. Applies to the Office of the Secretary of Defense (OSD), the Military Departments, the Organization of the Joint Chiefs of Staff (OJCS), the Defense Agencies, and the Unified and Specified Commands (here after referred to collectively as "DoD Components").

2. Applies to acquisition of new systems and system upgrades for all DoD weapon systems, training, and associated support systems, reference (a).

3. Applies to those subsystems used for signal processing, data processing, or electronic control functions.

C. DEFINITIONS

Very High Speed Integrated Circuits (VHSIC) Technology. That technology representative of the leading edge of digital integrated circuit technology, reference Enclosure 1.

D. POLICY

It is the policy of the Department of Defense to:

1. Exploit the many advantages of VHSIC technology in all procurements of Defense systems having subsystems or components for signal processing, data processing, or electronic control functions. These include all system new starts, on-going developments, and any and all upgrades and retrofits of existing systems. The advantages include system life-cycle cost, speed, performance, power, reliability, size, testability, and logistics supportability.

2. Use technology in each step of the acquisition and support process which reflects the advances in integrated circuit technology. Guidelines for use of this rapidly changing technology are given in Enclosure 1.

3. Use microelectronic devices which are fabricated, assembled, and tested in the U.S. and which meet or exceed the guidelines in Enclosure 1.

4. Apply advanced microelectronic technologies in accordance with the guidelines given in Enclosure 1.

E. RESPONSIBILITIES

1. The Under Secretary of Defense (Acquisition) (USD(A)) shall:

a. Be the DoD senior official for all activities related to this Directive.

b. Review system new starts, upgrades, and retrofits of all DoD components for compliance with this Directive.

c. Ensure that System Concept Papers (SCP), Decision Coordinating Papers (DCP), and Test and Evaluation Master Plans (TEMP) for major systems being reviewed by the Joint Requirements and Management Board (JRMB) contain adequate commitment to the use of technology as outlined in this Directive.

d. Ensure that the requirements of this Directive are implemented in all system acquisitions, including requests for proposals, new designs, and modifications to existing systems, and that acquisition strategies for all system new starts, upgrades and retrofits adequately address use of VHSIC technology and compliance with this Directive.

e. Ensure that the Military Standards are updated to reflect the requirements of this Directive.

f. Ensure the proper logistic support for systems using VHSIC technology.

g. Monitor compliance with this Directive.

2. The Under Secretary of Defense (Policy (USD(P)) shall develop a policy guidance consistent with rapid insertion of VHSIC chips into U.S. and NATO Defense systems.

3. The Head of each DoD Component shall:

a. Ensure that this Directive is implemented within the respective DoD Component.

b. Designate a VHSIC Technology Executive Official who shall oversee executing this Directive, monitor programs with respect to the use of VHSIC and serve as a focal point within the DoD Component for all activities related to VHSIC technology.

c. Develop a comprehensive Implementation Plan for using VHSIC technoglogy within the Component. This Plan shall include training, design support equipment, and logistics support to effect proper utilization of VHSIC technology in Defense systems. This plan shall be forwarded to the USD(A) 120 days from the effective date of this Directive. Periodic updates to this Plan shall be submitted when requested by USD(A) or as DoD Component Plans change.

F. PROCEDURES

Waivers. Authority for the issuance of waivers from the use of VHSIC technology as required by this Directive is delegated to each of the DoD Components only on a specific system or subsystem basis. For each proposed waiver, a full justification shall be provided and shall include, as a minimum, the following: a complete life-cycle cost analysis; a risk analysis; a schedule impact analysis. The life-cycle cost analysis shall include an assessment of the impact on the long term costs associated with both future upgrades and logistics support.

G. EFFECTIVE DATE AND IMPLEMENTATION

This Directive is effective immediately. Forward three copies of implementing documents to the Under Secretary of Defense (Acquisition) within 120 days.

DRAFT

APPENDIX A.1

ENCLOSURE 1

CHARACTERISTICS OF VHSIC TECHNOLOGY

1. Discussion.

The VHSIC Program has demonstrated advantages in the areas of system performance, reduced size and power, improved reliability and logistics supportability; improved life cycle costs are projected. Further, rapidly changing threat environments demand the flexibility available with the use of advanced technologies.

The integrated circuit industry is characterized by rapid progress, and thus rapid obsolescence. The five year life typical of an integrated circuit technology is considerably shorter than that of a typical DoD weapon system. The microelectronics in new systems are sometimes outmoded because of the time span from system conception studies to deployment. Thus, the system often has less than optimum performance and faces potential logistics problems of support of obsolescent parts within its planned life cycle.

System designers can minimize this by planning for the use of the newest technologies for the production of Defense systems. In the development phases of systems acquisition, system designers should anticipate technology evolution and use prototype parts. System developers should plan on concurrent development of integrated circuit technology and the system.

APPENDIX A.1

The advances of VHSIC technology offer improvements in many interrelated parameters associated with the integrated circuit. To simplify implementations of this Directive, the progression of technology will be characterized by the minimum feature size. However, integrated circuits selected for Defense systems should embody other capabilities such as those listed below.

2. Definitions.

a. Minimum Feature Size. The minimum lateral dimension of the integrated circuit as defined by the lithographic process in fabrication.

b. Functional Throughput Rate (FTR). The product of on-chip clock speed (Hz) and the gate density (logic gates per square centimeter).

3. Policy.

a. In the earliest phase of system acquisition, the concept definition designer should consider the technology referenced in the first column of Table 1. For the advanced development/demonstration/validation phase, the designer should use technology referenced in the second column of Table 1. Full-scale development will be implemented with technology described in the third column of Table 1. System production, modifications and product improvements will utilize the latest technology in production as shown in column four. Note that this requires the planning for future technology upgrades during the development phase of a weapon system.

DRAFT

TABLE I

MINIMUM FEATURE SIZES FOR INTEGRATED CIRCUITS IN THE SYSTEM ACQUISITION CYCLE

YEAR	MILESTONE I CONCEPT STUDIES	MILESTONE II ADVANCED DEVELOPMENT DEMONSTRATION	MILESTONE IIIA FULL SCALE DEVELOPMENT	MILESTONE IIIB PRODUCTION AND MODIFICATIONS
1986	0.8 micrometers	1.0	1.25	1.5
1988	0.5	0.8	1.0	1.25
1990	0.4	0.5	0.8	1.0
1992	0.3	0.4	0.5	0.8
1994	0.25	0.3	0.4	0.5

b. VHDL Description. Circuits being introduced into Defense systems after July 1, 1987, shall be described in VHSIC Hardware Description Language, reference (c).

c. Line Certification. The circuits being used for systems in production shall be fabricated on a line and process flow certified by Defense Electronic Supply Center according to MIL-STD-976, reference (d). At least one chip design from the technology must have been qualified to the requirements of MIL-STD-883, reference (f), and MIL-M-38510, reference (g).

d. Testability and Built-in Test. The circuit design shall facilitate the capability to fully verify the logic integrity of the chip from an external source. Built-in-test should cover at least 95% of logic gates. After July 1, 1987, new integrated circuit designs must have built-in test accessible from the standard VHSIC test and maintenance bus, reference (e).

e. Interoperability. After July 1, 1987 circuit designs shall adhere to the VHSIC Interoperability Standards, reference (e).

f. Use of Computer-Aided Design. A design simulation, at the behavioral and logic gate levels, shall be performed to verify the design of the entire electronic subsystem before new circuit designs enter fabrication. As a minimum, this should include timing analysis at the chip, board, and subsystem levels. The chip level analysis shall include modeling of dynamic performance and static modeling or simulation to fully verify logic integrity, logic-to-layout integrity and the effectiveness of built-in-test features. The subsystem level simulation shall verify design integrity and system fault detection/isolation effectiveness.

The following are goals for optimal design of integrated circuits to be used in Defense systems. Those characteristics which should improve with the advance in technology are noted.

g. Functional Throughput Rate (FTR). The integrated circuits should have a minimum FTR of 5×10^{11} gate-Hz/cm^2 for 1.25 micrometer technology; FTR should increase with decreasing feature size.

h. Clock Speed. The chip should operate with a minimum on-chip clock speed of 25MHz for 1.25 micrometer technology; clock speed should increase with decreasing feature size.

i. Gate Count. The chip should have a minimum gate count of 10,000 for custom logic with 1.25 um; gate count should increase for decreasing feature sizes.

j. Radiation Hardness. The chip should operate without failure in the following radiation environments:

Total dose - 10^4 Rads (Si)

Dose rate - 10^{10} Rads (Si)/sec without permanent failure

- 10^7 Rads (Si)/sec without logic upset

Neutron - 5×10^{12} n/cm^2

k. Reliability. After screening and burn-in, chip failure rates will be less than 0.006% per 1,000 hours at 60% confidence level, both while operating and stored over the -55°C to +125°C case temperature.

l. Temperature. The circuit shall operate at full rated specification over case temperature range -55°C to +125°C and worst case voltage variations.

m. Electrostatic Discharge Protection. Integrated circuits should withstand an electrostatic discharge of 2000 volts, as measured by MIL-STD-883, reference (f).

APPENDIX A.2 - VHSIC INSERTION POLICY MEMORANDA - ARMY AND NAVY

DEPARTMENT OF THE ARMY
OFFICE OF THE ASSISTANT SECRETARY
WASHINGTON, DC 20310-0103

16 NOV 1987

MEMORANDUM FOR: SEE DISTRIBUTION

SUBJECT: DOD VHSIC Program

The Department of Defense (DOD) Very High Speed Integrated Circuits (VHSIC) program has developed a new technology in microelectronics that promises significant benefits to the Army system development community. VHSIC offers the potential for improved performance, reduced size and weights, improved logistics and reduced life cycle costs. The products of Phase I of the VHSIC program are available now for application by developers to Army systems. I would like to lend my personal support and encouragement to everyone involved in the Army system development process, to take advantage of the products of the VHSIC program.

In this regard, I am endorsing the efforts of the OSD VHSIC office, COL W. Freestone, to provide information briefings to the Army system development community. The briefings will explain the VHSIC technology program and the types of products available to the materiel developer.

J. R. Sculley
Assistant Secretary of the Army
(Research, Development and Acquisition)

APPENDIX A.2

DEPARTMENT OF THE NAVY
OFFICE OF THE CHIEF OF NAVAL OPERATIONS
WASHINGTON DC 20350-2000

IN REPLY REFER TO

3900
098/Ser 6U356079
4 August 1986

MEMORANDUM FOR THE DISTRIBUTION LIST

Subj: POLICY ON VERY HIGH SPEED INTEGRATED CIRCUIT (VHSIC) TECHNOLOGY APPLICATIONS

Ref: (a) ASN(RE&S) memo of 21 Mar 86

1. Recent advances in VHSIC technology have created new opportunities to increase our mission effectiveness, while reducing weight, size, cost, and power requirements. It is our intent to exploit the benefits of VHSIC technology to enhance our warfighting capabilities in electronic warfare, fire control and guidance, command and control, surveillance, readiness, and supportability, while also striving to achieve cost reductions.

2. The Assistant Secretary of the Navy for Research, Engineering and Systems (ASN(RE&S)) has directed that VHSIC technology be considered for all newly initiated research and development programs for naval electronic equipment and systems, including preplanned product improvements, where VHSIC application will improve system performance, increase readiness and supportability at acceptable cost and schedule constraints (reference (a)). Consideration of the use of VHSIC technology is mandatory at Milestone I and Milestone II decision points for Navy acquisition programs. A request for VHSIC consideration and trade-offs should be included in future requests-for-proposals for design of new electronic systems.

ALBERT J. BACIOCCO, Jr.
Vice Admiral, U. S. Navy
Director
Research, Development & Acquisition

APPENDIX A.3 - DEFINITION OF VHSIC

OFFICE OF THE UNDER SECRETARY OF DEFENSE

WASHINGTON, DC 20301

ACQUISITION

21 JUL 1987

(R&AT)

Defense Electronics Supply Center
ECS
Att: Mike Frye
1507 Wilmington Pike
Dayton, OH 45444-5000

Dear Mr. Frye:

DESC/ECS has requested a definition of VHSIC for the purpose of determining when to classify a microcircuit "VHSIC" in labeling the MIL-M-38510 specification. The following paragraphs are intended as guidance in making this designation.

VHSIC is an acronym for Very High Speed Integrated Circuits. This acronym was developed to describe the Department of Defense sponsored program to develop very large scale integrated circuits applicable to DOD needs, particularly very high speed signal processing. The acronym is also used to describe the integrated circuits that were developed under that program. The contracted program has two phases, generally associated with designing with 1.25 micron feature sizes (VHSIC-1) and 0.5 micron feature sizes (VHSIC-2).

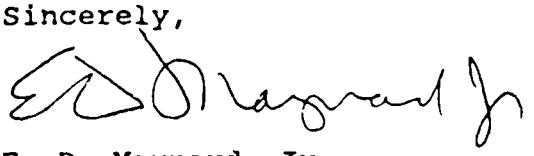
Since the program was designed to increase the technological level of integrated circuit manufacturing available to DOD, it benefits DOD to have many qualified VHSIC manufacturers. The larger the variety of interoperable VHSIC's available to military system designers, the more flexibility they will have to design the high performance systems required by our defense strategy.

Manufacturers providing this technology are encouraged to qualify their products to Mil-M-38510 (JAN). The guidelines below shall be used to determine which devices meet VHSIC-1 requirements. The primary source of these guidelines is the VHSIC Phase 1 Statement of Work. During the course of the VHSIC Program, requirements were refined to reflect the needs of system insertion. We believe that newly designed and redesigned VHSIC's should meet these tighter requirements.

APPENDIX A3

A performance matrix Mil-M-38510 specification has been established by DESC to accommodate the performance versus time progression of microcircuits along the normal maturation curve. Where this progression results in a VHSIC-1 device, the Scope paragraph of the specification may be annotated to indicate that the candidate device will meet VHSIC-1 requirements.

Sincerely,



E. D. Maynard, Jr.
Director
Computer and Electronics Technology

Attachment

APPENDIX A.3

1 VHSIC-1 Attributes

1.1 Minimum feature size

A VHSIC-1 technology shall have a minimum lateral dimension of 1.25 micrometers defined by the lithographic process in fabrication.

1.2 Operating Temperature Range

A VHSIC-1 shall operate at full rated specification over case temperature range -55 to +125 degrees Centigrade.

A VHSIC-1 for which a specification was submitted to DESC before July 1988 shall operate at VHSIC-1 frequency over case temperature range -55 to +85 degrees Centigrade and over the worst case voltage variations indicated in the specification. A full temperature range (-55 to +125 degrees Centigrade) version shall be available by January 1990.

1.3 Clock Speed

A VHSIC-1 shall operate with a minimum master clock speed of 25 MHz.

1.4 Functional Throughput Rate

The VHSIC-1 shall have a minimum Functional Throughput Rate (FTR) of 5x10 exponent 11 gate-Hz per square centimeter. Functional Throughput Rate is the product of on-chip clock speed (Hz) and the gate density (logic gates per square centimeter). FTR must be based on a reasonable minimum number of gates, e.g., 6,000.

1.5 VHDL Description

The VHSIC-1 logic structure and behavior shall be described in VHSIC Hardware Description Language (VHDL), ref(a). The VHDL description shall be delivered to the Defense Electronic Supply Center.

1.6 JAN Qualification (Mil-M-38510)

The VHSIC-1 shall be fabricated on a line and process flow certified by the Defense Electronic Supply Center according to MIL-STD-976, ref(b). The VHSIC-1 shall be qualified or in the process of being qualified to the requirements of MIL-M-38510, ref (c) and MIL-STD-883, ref (d); if in DESC's opinion qualification to Mil-M-38510 is not cost beneficial to DOD, DESC may recommend a Standardized MIL-Drawing (SMD).

1.7 Testability

The VHSIC-1 design shall include features to facilitate external testing to verify the integrity of the logic of the chip. These features shall reduce the burden of test vector generation, improve the achievable fault coverage of the test vector set, and reduce automatic test equipment requirements in terms of test vector storage and number of pins that must be driven and/or sensed. Manufacturing tests shall achieve at least 95% coverage of all detectable single stuck-at-zero and -one faults at the structural (logic) model level as determined by an approved fault simulator, e.g., HITS, LASAR, TEGAS, Hilo. Manufacturing level test vectors to meet these requirements shall be delivered to DESC in computer-readable form acceptable to DESC.

1.8 Built In Test

A VHSIC-1 shall incorporate built-in-test to verify the chip logic.

For detail specifications or new part types submitted to DESC after July 1989, the self test shall achieve at least 95% coverage of all detectable single stuck-at-zero and -one faults at the structural (logic) model level as determined by an approved fault simulator, e.g., HITS, LASAR, TEGAS, Hilo. The built-in test shall be accessible from the standard VHSIC Element Test and Maintenance Bus (ETM-BUS) or the VHSIC Test and Maintenance Bus (TM-BUS), ref (e).

1.9 Reliability

The reliability design goal for a VHSIC-1 is a failure rate, after specified screening and burn-in, less than 0.006% per 1,000 hours at 60% confidence level, while operating under specified conditions and while stored. A predicted failure rate, supported by reliability modeling data and/or test data, shall be provided to DESC.

1.10 Radiation Hardness

The VHSIC-1 shall operate

- without radiation induced failures in a radiation environment of 10,000 Rads (Si).
- without radiation induced permanent failures after a transient radiation dose of 10 exp 8 Rads (Si) per second for a ten nanosecond radiation pulse.
- without transient upset through a radiation pulse of 10 exp 7 Rads (Si)/second for a ten nanosecond radiation pulse.

1.11 ESD Susceptibility

A VHSIC-1 shall be capable of meeting the electrostatic discharge requirements of TM 3015, MIL-STD-883, ref (d), current at the time of the dating of the specification. For detail specifications or new part types submitted before January 1988, the VHSIC-1 shall meet an ESD requirement of 1000V when measured by TM 3015.

1.12 Interoperability

For specifications or new device types submitted after July 1988, the VHSIC-1 shall adhere to the VHSIC Interoperability Standards, ref (e).

2 References

a VHDL

VHSIC Hardware Description Language, version 7.2, IEEE standard after approval or superseding version.

b MIL-STD 976

MIL-STD-976, "Certification Requirements for JAN Microcircuits" October 5, 1981 (or superseding version).

c MIL-M-38510

MIL-M-38510, General Specifications for Military Specification Microcircuits, October 31, 1983 (or superseding version).

d MIL-STD 883

MIL-STD-883, "Test Methods and Procedures for Microelectronics," November 29, 1985 (or superseding version).

e Interoperability

VHSIC Interoperability Standards. Interim copies available from Naval Research Laboratory, Code 5305, Washington, DC 20375-5000.

APPENDIX A.4 - MIL-STD-454, REQUIREMENT 64 - PROPOSED REVISIONS

DEPARTMENT OF THE AIR FORCE
HEADQUARTERS ROME AIR DEVELOPMENT CENTER (AFSC)
GRIFFISS AIR FORCE BASE, NEW YORK 13441-5700

23 NOV 1987

REPLY TO ATTN OF: RBE-2 (V. Nivaggi, AUTOVON: 587-2101)

SUBJECT: Proposed Changes to Requirement 64, Microelectronic Devices

TO: See Distribution List

1. A proposed draft of Requirement 64 is attached for your review and comment.

2. The proposed changes, denoted by a bar in the left hand margin, establish requirements for employing, to the maximum extent practical, the advances made in integrated circuit technology in the design of new and re-engineered systems. Also included are coordinator's comments on Paragraphs 3.1, 4.6, 5.4, and Table 5.1.2 of the draft.

3. Please complete the reply sheet and forward per instructions thereon.

FOR THE COMMANDER

ANTHONY J. FEDUCCIA, Chief
Systems Reliability & Engineering Division
Directorate of Reliability & Compatibility

4 Atch
1. Distr List
2. Draft Rqmt 64, 21 Sep 87
3. Coordinator's Comments
4. Reply Sheet

APPENDIX A.4

DRAFT: Technology Revisions, Req. 64, 21 Sept 1987

REQUIREMENT 64

MICROELECTRONICS DEVICES

1.0 Purpose

This requirement establishes criteria for the selection and application of microelectronic devices for use in military systems. These criteria are based on the objectives of achieving technological superiority, quality, reliability, and maintainability in military systems.

2.0 Applicable Documents

MIL-M-38510: Microcircuits, General specification for
MIL-STD 785: Reliability Program for Systems and Equipment Development and Production
MIL-STD 883: Test Methods and Procedures for Microelectronics
MIL-STD 975: NASA Standard Electrical, Electronic and Electromechanical Parts List
MIL-STD 1547: Parts, Materials and Processes for Space and Launch Vehicles, Technical Requirements for
MIL-STD 1562: Lists of Standard Microcircuits
DOD-STD-1686: Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)
MIL-HDBK-217: Reliability Prediction of Electronic Equipment
VHDL: VHSIC Hardware Description Language, Version 7.2, or IEEE Standard 1076 after December 1987, or superseding version.
VHSIC Interoperability Standards: VHSIC Interoperability Standards. Includes specifications for the TM-bus, ETM bus. Pi Bus, and VHSIC Electrical Specification. Copies available from Naval Research Laboratory, Code 5305, Washington, DC 20375-5000.
TISSS: Tester Independent Support Software System (TISSS), TISSS Input Format (TIF), TISSS Vector Language (TVL), TISSS Design Language (TDL), TISSS version 3.0, IEEE standard after approval, or superseding version.

3.0 Definitions

3.1 Microelectronic Device: Monolithic, hybrid, rf and microwave (hybrid/integrated) microcircuits, multi-chip microcircuits, and microcircuit modules.

3.2 VHSIC: Very High Speed Integrated Circuits (VHSIC): a technology development program (1980-1989) for the design and manufacture of high speed digital integrated circuits with 1.25 and 0.5 micrometer feature sizes for military applications. Many VHSIC's incorporate Built-In-Test and later VHSIC's will incorporate interoperability features. Table 5.1.2 describes VHSIC characteristics.

3.3 MIMIC: Microwave/Millimeter Wave Monolithic Integrated Circuits (MIMIC): a program to establish the capabilities to design, develop, manufacture and test analog microwave/millimeter wave integrated circuits for use in military systems.

3.4 Advanced Microcircuit Technology: Microcircuit fabrication and design technology which is newly available for prototype designs and will be available for production in the near future (2-5 years). VHSIC and MIMIC are examples. For digital microcircuits, the performance capability can be approximately characterized by the minimum feature size, the clocking frequency, and the functional throughput rate. See para 5.1.

3.5 VHDL: VHSIC Hardware Description Language: A higher level computer language developed under the VHSIC program for describing the signal structure of electronic hardware (chips, modules, and subsystems). The language can describe the signal flow and the structure of the device in terms of the basic circuit models, fundamental logic blocks, and higher level functional assemblies of logic blocks.

4.0 Requirements

4.1 Selection

Technology

New and re-engineered system designs shall exploit advanced microcircuit technology to the maximum extent practical. At each stage in system design, i.e., concept studies, demonstration and validation, and full scale development, the microcircuit technology utilized shall ensure that the most advanced technology which meets the reliability, performance, and cost requirements of the application will be used in the production phase.

Reliability

Microelectronic devices in military systems in production shall, as a minimum, conform to MIL-M-38510, product assurance level class B. A plan to assure that microelectronic components meet this requirement shall be in place by Full Scale Development. Class S shall be used for space applications. Unless otherwise specified, the order of precedence shall be as follows:

a. Microcircuits listed in Table I of MIL-STD-1562.

b. Other MIL-M-38510 microcircuits not listed in Tables III, IV, and V of MIL-STD-1562.

c. Other microcircuits listed in Table II of MIL-STD-1562 as preferred for new design, subject to procuring activity approval.

d. Active Standardized Military Drawing (SMD) or DESC Drawing microcircuits not listed in Tables III, IV, and V of Mil-STD-1562, subject to procuring activity approval.

e. Other microcircuits (see 4.1.2), subject to procuring activity approval.

4.1.1 Qualified Devices

When the contract or purchase order for new design or redesign of military hardware specifies the use of MIL-STD-883 class B or S microcircuits, and there is a class B or S device on QPL-38510 of the required generic chip and package type or case outline, the qualified class B or S microcircuit shall be the only device authorized in that design.

4.1.1.1 Class S Device

For space applications, when class S parts per QPL-38510 are not available or cannot be qualified by the manufacturer, the requirements of MIL-STD-975 or MIL-STD-1547 shall apply in accordance with procuring activity direction.

4.1.1.2 Class B Device

When a qualified class B device does not exist and a active SMD (or DESC drawing) device of the required generic chip and package type or case outline does exist, the SMD (or DESC drawing) device shall be the preferred device authorized for that design.

4.1.2 Other Microcircuits

For other than QPL-38510 microcircuits, the following information shall be included in the non-standard part approval request (except where identification of a military detail specification, SMD or DESC Drawing number satisfies this requirement):

a. Device nomenclature, marking, configuration, functional requirements, parameters and limits sufficient to insure the required form, functions and interchangeability.

b. Required environmental, endurance (life) and other design capability tests.

c. Quality assurance requirements, including screening and lot quality conformance (acceptance) tests. As a minimum, devices shall be procured to all the requirements of MIL-STD-883 para 1.2.1. Hybrid and microwave microcircuits shall be procured to the requirements of MIL-M-38510, Appendix G. The applicable MIL-M-38510 detail specification, SMD, DESC Drawing or vendor/contractor document shall be specified for electrical performance, mechanical, and final electrical test requirements. Current and valid generic data may be substituted only for Groups C and D of Methods 5005, 5008, and 5010 of MIL-STD-883. Group C generic data must be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process, and from the same wafer fabrication area as the die represented. Group D generic data must be on date codes no more than one year old and on the same package type (see 3.1.3.12 of MIL-M-38510) and from the same plant as the package represented.

d. In the development or redesign phases, the projected availability and product assurance status for the time of production and through the projected life of the system shall be evaluated.

4.2 Programmable Devices

Use of programmable devices, regardless of type, requires approval of the procuring activity.

4.3 Fusible Link Devices

When fusible link devices (PROM's, PALs, EPLAs, etc.) are programmed by the user, parametric and functional electrical tests in accordance with MIL-STD-883, Method 5005, Group A, Subgroups 1,2, and 3, along with 7 and 8 at required access speeds, shall be performed after programming. This testing shall be done on a 100% basis.

4.4 Critical Items:

Custom microcircuits, hybrid or monolithic, are considered critical items and shall be treated in accordance with Task 208 of MIL-STD-785 when required by the contract.

4.5 Packages:

Microcircuit devices used in equipment shall be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. No organic or polymeric materials such as lacquers, varnishes, coatings, adhesives, or greases shall be used inside the microcircuit package, unless otherwise specified. No desiccants shall be contained in the microcircuit package, unless otherwise specified.

4.6 Device design documentation

Digital microcircuits, designed after _____, shall be documented with VHDL structural and behavioral descriptions from which independent redesign and manufacture of the microcircuits can be accomplished to meet multiple source or re-supply requirements. THE VHDL descriptions submitted shall be compatible with the TISSS Input Format (TIF). Fully developed electrical performance specifications, when required, shall be delivered in TISSS TDL (Test Description Language). The simulatable VHDL descriptions shall include a set of test vectors, compatible with TISSS Vector Language (TVL), which satisfy vector coverage requirements and which can be used to validate the functional description.

4.7 Cost Considerations (Moved from "Guidance", formerly Para. 5.7)

Microcircuit devices should be selected on the basis of overall life cycle cost rather than initial procurement cost alone.

APPENDIX A.4

5.0 Information for Guidance Only

5.1 General: Technology Progression

The use of advanced microcircuit technology shall be considered and evaluated in the design of all systems/equipment. For critical weapon systems applications, and for system development schedules projected to be longer than four years, the performance advantages provided by advanced technologies, such as VHSIC and MIMIC, shall be evaluated early in the system development phases for use in the procurement stage.

The projected availability of advanced digital (VHSIC) technologies for use in progressive stages of system development is provided in Table 5.1.1 to aid in performing this evaluation.

Table 5.1.1

Digital Technology Progression Prediction

Year	Concept	I	D&V	II	FSD	III	P&D
1987	.5 - 1.0	1.0 - 1.25		1.0 - 1.25		1.25 - 1.5	
1988	.5 - .8	.8 - 1.0		1.0 - 1.25		1.0 - 1.25	
1989	.5 - .7	.7 - 1.0		.8 - 1.0		1.0 - 1.25	
1990	.4 - .6	.5 - .8		.6 - 1.0		.8 - 1.0	
1991	.4 - .5	.5 - .6		.6 - .8		.7 - .8	
1992	.3 - .4	.4 - .6		.5 - .7		.6 - .7	
1993	.25 - .3	.3 - .5		.4 - .6		.5 - .6	
1994	.25	.3		.4		.5	

D&V: Demonstration and Validation
FSD: Full Scale Development
P&D: Production and Deployment
I, II, III : System Development Milestones

The numbers in the table represent the "minimum feature size" which generally characterizes the performance and characteristics of digital technology. (See Table 5.1.2.)

Table 5.1.2
Performance Characteristics
Digital Microelectronics

Characteristic	Units	Feature Size	Feature Size
Min feature size	micrometers	1.25	0.5
Temperature range	degrees Celsius	-55 to 125	-55 to 125
Min clock frequency	MHz	25	100 on chip
FTR	gate Hz/sq. cm.	5 exp 11	1 exp 13
Testability		95% coverage	95% coverage
BIT fault coverage			
stuck at	%	*95	95
stuck open (CMOS)	%		75
Test bus		*ETM or TM	ETM or TM
Interoperability		**yes	required

* Req'd after Jul 89
** Req'd after Jul 88

5.2 Class S

Class S is the highest product assurance level of MIL-M-38510 and is intended for space applications or other applications requiring the product assurance provisions of class S.

5.3 Reliability Prediction

When required, microcircuit reliability predictions shall be prepared in accordance with MIL-HDBK-217 for applicable technologies.

5.4 Electrostatic Sensitive Parts

Certain types of microcircuits are susceptible to electrostatic discharge (ESD) damage. Microcircuit susceptibility is classified in DOD-STD-1686 (and Test Method 3015 of MIL-STD-883). The least susceptible microcircuit class should be selected and a lower class microcircuit should not be used when a higher microcircuit class is available which meets performance requirements. The ESD susceptibility of microcircuits is listed in QPL-38510. When the device susceptibility information is not available, it can be determined using Test Method 3015 of MIL-STD-883 or Appendix B or DOD-STD-1686.

5.5 Microcircuit Obsolescence

Due to rapid technology advances, many military and commercial microcircuits listed in specifications and catalogs are either obsolete or are nearing obsolescence. The use of these devices will adversely affect the mission performance and logistic support of the using equipment.

Documentation of new microcircuit designs with VHDL which captures the design and performance of the microcircuit should be provided to reduce the cost of re-design and re-manufacture if early obsolescence occurs.

For Navy equipment current information on microcircuits that may be nearing obsolescence may be obtained from the Naval Avionics Center, Code 917, Indianapolis, Indiana 46219-2189, telephone (317) 353-3767, AV 369-3767.

5.6 Use of Non-hermetic Microcircuits

Upon specific request and approval by the procuring activity to waive the requirements of 4.1, non-hermetic microcircuits may be considered for use in ground fixed (GF) or ground benign (GB) environments as defined in MIL-HDBK-217, provided they meet all the requirements of the equipment specification, temperature and humidity are completely controlled in transit, storage, and application, and provisions have been made for logistic availability.

5.7 Testability

New and upgraded systems should exploit chip level built-in-test features to enhance the testability and operational availability of the module or system. When advanced digital modules or boards are developed, microcircuits incorporating the VHSIC ETM-BUS or VHSIC TM-BUS should be used. (See VHSIC Interoperability Standards.)

5.8 Life Cycle Cost Evaluation

The following factors shall be considered in estimating life cycle costs associated with selection of microcircuit devices or technologies: a) effect of built-in-test and use of TISSS on repair, maintainability, operational availability, and reconfigurability, b) value of VHDL descriptions of chips, modules, and boards in resupply, multiple source development, and design upgrade.

4318 Federal Register / Vol. 52, No. 28 / Wednesday, February 11, 1987 / Rules and Regulations

DEPARTMENT OF DEFENSE

48 CFR Parts 204 and 252

Department of Defense Federal Acquisition Regulation Supplement; Very High Speed Integrated Circuits Safeguards

AGENCY: Department of Defense (DOD).

ACTION: Interim rule and request for comments.

SUMMARY: The Defense Acquisition Regulatory Council has approved temporary revisions to the Defense Federal Acquisition Regulation Supplement (DFARS) which address requirements specified within DoDI 5230.26, entitled "Very High Speed Integrated Circuits (VHSIC) Technology Security Program," dated 17 March 1986. The DFARS revisions prescribed a contract clause for uniform use in all contracts involving VHSIC, which clause incorporates Enclosure (4) to DoDI 5230.26 by reference. Unless sooner rescinded or extended this coverage expires 31 January 1988, which period will allow sufficient time for conversion of the VHSIC safeguards within Enclosure (4) to DoDI 5230.26 to an appropriate military specification, military standard, or manual.

DATES: *Effective date:* The interim rule is effective February 4, 1987, and expires on 31 January 1988 unless sooner rescinded.

Comments: Interested parties are invited to submit written comments on or before April 13, 1987 to the Executive Secretary, DAR Council, at the address below. Please cite DAR Case *86-134* in all correspondence relating to this subject. Comments received will be considered in revising the interim rule which will be implemented by Departmental guidance. A Defense Acquisition Circular will not be issued in view of the temporary nature of the rule.

ADDRESS: Interested parties should submit written comments to: Defense Acquisition Regulatory Council, ATTN: Mr. Charles W. Lloyd, Executive Secretary, DAR Council, ODASD (P) DARS, c/o OASD (A&L) (M&RS) Room 3C841, The Pentagon, Washington, DC 20301-3062.

FOR FURTHER INFORMATION CONTACT: Mr. Charles W. Lloyd, Executive Secretary, (202) 697-7266.

SUPPLEMENTARY INFORMATION:

A. Background

The DFARS revisions approved by the DAR Council include a contract clause which incorporates Enclosure (4) to DoDI 5230.26 and includes in part (1) the requirement that contractors allow representatives of the Defense Investigative Service (DIS) access to facilities at reasonable times for compliance reviews, and (2) the requirement that subcontractors must also comply with Enclosure (4) to DoDI 5230.26 where subcontracts involve VHSIC. Pending conversion to a military specification, standard, or manual, contracting officers are directed by the revisions to provide a copy of Enclosure (4) to DoDI 5230.26 to contractors/offerors upon request.

B. Determination to Issue an Interim Rule

It is the desire of DoD to increase the use of VHSIC-sensitive information and/or program products within the Defense industry as quickly as possible. Disclosure of VHSIC-sensitive information and/or program products to potential adversaries has reduced and could continue to reduce the United States' technological advantage to the detriment of our national security. Contractor compliance with VHSIC safeguards is therefore essential. The DoD therfore concludes that compelling reasons require issuance of an interim rule without prior publication for public comment.

C. Regulatory Flexibility Act

The interim rule incorporates by reference, in standard contract format, requirements which are already being applied by VHSIC contractors on a voluntary basis with the costs thereof being reimbursable under Government contracts. Also, there currently are only ten small businesses with contracts involving VHSIC. Accordingly, the Department certifies that this rule will not have a significant economic impact upon a substantial number of small entities within the meaning of the Regulatory Flexibility Act of 1980, 5 U.S.C. 601 et seq. A regulatory flexibility analysis has therefore not been performed. Comments are invited from small entities and other interested parties.

D. Paper Reduction Act

This rule does contain information collection requirements which require the approval of OMB under 44 U.S.C. 3501 et seq. The collection of information requirements have been submitted to OMB for review under section 3504(h) of the Act.

List of Subjects in 48 CFR Parts 204 and 252

Government procurement.

Charles W. Lloyd,

Executive Secretary, Defense Acquisition Regulatory Council.

Therefore, 48 CFR Parts 204 and 252 are amended as follows:

1. The authority citation for 48 CFR Parts 204 and 252 continues to read as follows:

Authority: 5 U.S.C. 301, 10 U.S.C. 2202, DoD Directive 5000.35, and DoD FAR Supplement 201.301.

PART 204—ADMINISTRATIVE MATTERS

2. Section 204.202 is amended by adding to paragraph (c) paragraph (6) to read as follows:

204.202 DoD Distribution Requirements.

* * * * *

(c) * * *

(6) One copy or an extract to the cognizant Defense Investigative Service (DIS) office as listed in Enclosure (5) to DoDI 5230.26 Very High Speed Integrated Circuits (VHSIC) Technology Security Program whenever the clause prescribed at 204.7204 is included in the contract.

3. Subpart 204.4, consisting of section 204.471, is added to read as follows:

Subpart 204.4—Safeguarding Classified Information Within Industry

204.471 Very High Speed Integrated Circuits (VHSIC) Safeguards.

Policies and procedures regarding protection of technologies and products developed under the VHSIC program are addressed in Subpart 204.721.

4. Subpart 204.72, consisting of sections 204.7200 through 204.7204, is added to read as follows:

Subpart 204.72—Very High Speed Integrated Circuits Safeguards

Sec.

Subpart 204.72—Safeguarding Classified Information Within Industry

204.7200 Scope of subpart.

This subpart prescribes policy, procedures, responsibilities and requirements for establishing the Very High Speed Integrated Circuits (VHSIC) Technology Security Program for Defense contractors and subcontractors

in order to protect technology and products developed under the VHSIC program, in accordance with DoD Instruction (DoDI) 5210.75, "Very High Speed Integrated Circuits (VHSIC) Program Security Classification Guide."

204.7201 Definitions.

"VHSIC-sensitive Information and/or Program Products," as used in this subpart consist of unclassified technical information, subject to DoDI 5230.25, "Withholding of Unclassified Technical Data from Public Disclosure", that would significantly enhance the ability of a potential adversary to reduce the U.S. technological lead. Such information includes all unclassified information developed under DoD funding and listed in DoDI 5210.75 and excludes that information for which no special controls are required.

(a) *VHSIC-sensitive Information includes the following:*

(1) Internal reports dealing with technical details, particularly the solutions of problems common to VHSIC program contractors.

(2) Fabrication process data parameters and internal specification sheets.

(3) Detailed architecture and logic representations of chip and custom-macro cells, for example, hardware description language, system design language descriptions, and computer data base information unique to the VHSIC program.

(4) Recipe technology and other special technology developments.

(5) Design and layout ground rules when related to the VHSIC program.

(b) *VHSIC-Sensitive Program Products include the following:*

(1) VHSIC-sensitive chips, wafers and rejected parts created or received.

(2) Masks, reticles, pattern generation media (geometry information).

(3) Computer aided design, chip logic design, and chip integration tools unique to the VHSIC program.

(4) Special semiconductor process equipment.

(5) Modules of VHSIC hardware products.

(6) Military systems brassboards.

204.7202 General.

204.7202-1 Policy.

The VHSIC program is a technology initiative sharing roots with commercial microcircuit developments. The objective of the VHSIC program is to enhance the performance of U.S. military forces in relation to those of potential adversaries. The policy is to provide effective protection against disclosure to adversaries of the capabilities developed under the VHSIC program. This protection should neither impede the use of VHSIC products in *U.S. military systems nor intrude* into commercial microcircuit product design and production.

204.7202-2 Presward responsibilities.

In accordance with applicable Department and Agency procedures implementing DoDI 5230.28, technical or requirements organizations initiating purchase requests must identify to the contracting officer, the nature and extent of VHSIC-sensitive information and/or program products involved for each purchase request and provide a copy of Enclosures (2) and (4) to DoDI 5230.26.

204.7203 Notification to DIS.

Whenever the clause prescribed at 204.7204 is included in the contract, the contracting activity shall provide an extract or a copy of the contract to the cognizant DIS office (see 204.202(c)(6)).

204.7204 Contract clause.

The contracting officer shall insert the clause at 252.204-7006 Very High Speed Integrated Circuits Technology Security Program in all solicitations and contracts involving VHSIC-sensitive information and/or program products. The contracting officer shall provide a *copy of Enclosures* (2) and (4) to DoDI 5230.28 to each offeror/contractor upon request.

PART 252—SOLICITATION PROVISIONS AND CONTRACT CLAUSES

5. Section 252.204-7006 is added to read as follows:

252.204-7006 Very High Speed Integrated Circuits Technology Security Program.

As prescribed at 204.7204, insert the following clauses:

Very High Speed Integrated Circuits Technology Security Program (Jan 87)

(a) The Contractor shall comply with the applicable requirements of Enclosures (2) and (4) to DoDI 5230.28, entitled "Very High Speed Integrated Circuits (VHSIC) Technology Security Program," in effect on the date of award of this contract which is available from the contracting officer upon request.

(b) The Contractor shall allow representatives of the Defense Investigative Service (DIS) access, at all reasonable times, into its facilities for purposes of reviewing its compliance with the VHSIC safeguards applicable to this contract.

(c) The Contractor shall insert this clause, including this paragraph (c) with appropriate changes in the designation of the parties, in all subcontracts hereunder which involve VHSIC-sensitive information and/or Program Products as defined in section 204.7201 of the Department of Defense Federal Acquisition Regulation Supplement.

(d) The Contractor shall provide a copy of any subcontract involving VHSIC to the cognizant DIS office within ten (10) days after issuance of the subcontract.

(End of clause)

[FR Doc. 87-2864 Filed 2-10-87; 8:45 am]

BILLING CODE 3810-01-M

DEPARTMENT OF JUSTICE

48 CFR Parts 2804, 2807 and 2812

[Justice Acquisition Circular 86-1]

Amendments to the Justice Acquisition Regulations (JAR) Regarding Advance Procurement Planning, Procurement Lead Times and Rated Orders Under the Defense Production Act of 1950

AGENCY: Justice Management Division, Office of the Procurement Executive, Justice.

ACTION: Final rule.

SUMMARY: The Justice Acquisition Regulations, Parts 2804, 2807, and 2812 are revised to implement agency requirements under DOJ order 2300.5A, Advance Procurement Planning, and to provide JAR coverage of procedures for placing rated orders. The Department's Advance Procurement Planning order contains requirements for contract file documentation. This JAR amendment will add the documentation requirements to the existing contract file checklist in JAR 2804.803-70. A requirement to provide lead times and cut-off dates for receipt of requisitions is being added as an element of the procurement planning process and to reissue in the JAR previous implementation of OFPP Policy Letter 81-1. The former implementation was contained in the DOJ Directive System. Because major organizational components in DOJ have delegated procurement authority and their own particular needs and requirements, it will be left to the Bureaus to establish the lead times and cut-off dates within the broad guidelines established in the JAR. Finally, procedures are being implemented for review and coordination of rated orders under the Defense Production Act of 1950. DOJ infrequently has requirements for rated orders, however, past experience has shown that there is a need to increase awareness of the Procurement Executive's delegated responsibility to exercise this authority on behalf of the Department. Further FAR 12.3 requires

APPENDIX A.6

INTERNATIONAL TRANSFER AND EXPORT CONTROL OF VHSIC: DOD POLICY

THE UNDER SECRETARY OF DEFENSE

WASHINGTON D C 20301-2000

18 OCT 1987

POLICY

In reply refer to:
I-09352/87

MEMORANDUM FOR CHAIRMAN, JOINT CHIEFS OF STAFF
UNDER SECRETARY OF DEFENSE FOR ACQUISITION
ASSISTANT SECRETARY OF THE ARMY (RESEARCH, DEVELOPMENT AND ACQUISITION)
ASSISTANT SECRETARY OF THE NAVY (RESEARCH, ENGINEERING & SYSTEMS)
ASSISTANT SECRETARY OF THE AIR FORCE (ACQUISITION)
DIRECTOR, DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
DIRECTOR, NATIONAL SECURITY AGENCY
DIRECTOR, DEFENSE SECURITY ASSISTANCE AGENCY
DIRECTOR, STRATEGIC DEFENSE INITIATIVE ORGANIZATION
DIRECTOR, DEFENSE NUCLEAR AGENCY

SUBJECT: DoD Policy Regarding International Transfer and Export Control of Very High Speed Integrated Circuits (VHSIC) Technology, Goods and Services

The Department of Defense is spending considerable resources to improve advanced electronics for future weapon system programs. VHSIC, a successful "force multiplier", significantly improves our microprocessing capability and will have a synergistic effect when coupled with advanced sensor systems. The strategic advantage of VHSIC must be protected from unfriendly foreign acquisition. This policy provides DoD guidance on how to deal with requests for VHSIC.

Generally, the VHSIC policy permits transfer and export of VHSIC products which may be embedded in Western origin weapons systems to our friends and allies on a case-by-case basis when technology security is adequate. Production and detailed design technology and associated software will not be released.

Defense Technology Security Administration (DTSA) is responsible for management of the policy; DTSA's point of contact is Colonel Wendell Taylor, (202) 694-0961, should you have any questions regarding the implementation of this policy. My memorandum of 19 June 1986 on the release of VHSIC data and briefings to foreign entities is hereby rescinded

Fred C Ikle

APPENDIX A.6

COPY

Department of Defense
Policy Regarding
International Transfer and Export Control of
Very High Speed Integrated Circuits (VHSIC)
Technology, Goods and Services

13 October 1987

A. References

1. Arms Export Control Act
2. International Traffic in Arms Regulation, (ITAR)
3. Very High Speed Integrated Circuits (VHSIC) Program Security Classification Guide, DODI 5210.75
4. Very High Speed Integrated Circuits (VHSIC) Technology Security Program, DODI 5230.26

B. General

1. DoD recognizes that the U.S. semiconductor industry is a world leader in advanced integrated circuits and the leader in VHSIC technology. Furthermore, DoD recognizes that these technologies can provide a significant, critical military advantage to those nations who acquire them.

2. It is DoD policy to protect VHSIC technology to the maximum extent possible, utilizing procedures which are consistent with existing export control regulations.

3. DoD will consider foreign availability when evaluating requests for export of VHSIC technical data, goods and services.

C. Purpose

1. This policy establishes DoD guidelines as to the acceptability of transferring VHSIC technical data, goods and services under Foreign Military Sales (FMS) or Government-to-Government cooperative research, development or production programs or by export. This policy will be used by DoD to review proposed transfers and exports that may require DoD's recommendations and comments.

2. In addition, this policy may be useful to U.S. industry, foreign governments, and other exporters and foreign importers in furthering their understanding of DoD's responses to requests for exports or transfers of VHSIC technical data, goods and services.

D. Definition of VHSIC and VHSIC Technology

1. VHSIC devices are defined as semiconductor devices which are specifically designed for military applications and have a high-speed signal or data processing

capability that is equal to or better than a throughput rate of 1×10^{11} gate-hertz per square centimeter (gate density times clock frequency).

2. VHSIC technology consists of the VHSIC devices themselves, the technical data related to these devices, and the software specifically developed for the design, manufacture and test of VHSIC devices.

E. General Export and Transfer Policy. It is DoD policy to:

1. Treat defense-related technology as a valuable, limited national security resource to be invested in pursuit of national security objectives.

2. Control the export of technical data, goods and services that contribute to the military potential of any country that would prove detrimental to U.S. security interest; and

3. Facilitate the sharing of military technology only with NATo and other closely aligned and friendly nations that cooperate effectively in safeguarding technical data, goods and services from transfer to nations whose interests are inimical to the U.S.

F. VHSIC Security and Control

1. The policies, procedures and responsibilities contained in DODI 5210.75 and DODI 5230.26 are not superseded by this policy.

2. VHSIC technical data, devices and services, are controlled by the ITAR. The ITAR grants Canada certain exemptions. Requests to export or transfer VHSIC technology will be reviewed by DoD on a case-by-case basis.

G. Release Guidelines

1. VHSIC technology to be incorporated into specific weapons systems may be exported or transferred to our closest allies and friends on a case-by-case basis provided appropriate security measures are met.

a. Generally, the release of VHSIC technology devices will be favorably considered for NATO, and closely aligned and friendly nations, with whom the Department of Defense has established cooperative programs if the technology will be:

(1) incorporated into a U.S. weapon system; or
(2) incorporated into an allied/friendly, Western origin weapon system, provided:

(a) chip/board capability is appropriate for the stated requirements;
(b) the quantity of devices plus initial spares is appropriate for the application;
(c) additional spares are replaced on a one-for-one basis; and
(d) the foreign consignee and end-user execute the appropriate nontransfer and use certificate (Form DSP-83).

b. The exporter must provide a security plan under one of the following conditions:

(1) DOD VHSIC program exporters provide a VHSIC security plan in accordance with DODI 5230.26.
(2) Other exporters of VHSIC technology devices for military applications provide a security plan which conforms to the intent of DODI 5230.26.

2. Requisite accompanying data for inserting VHSIC devices, approved for export or transfer under a specific request, may be released. This data includes functional block diagrams, input/output data, application notes, and overall operating characteristics such as power requirements, packaging, size, weight, and other appropriate data necessary for system insertion.

3. Under the ITAR, a license is required for furnishing defense services. Therefore, a license is required to provide access to VHSIC Computer Aided Design (CAD) and Computer Aided Engineering (CAE) tools to facilitate the customized design of VHSIC devices. Applications for access to VHSIC CAD/CAE will be reviewed by DOD on a case-by-case basis. Access may be granted only in a controlled environment; i.e., one in which the user's access is limited to the design capability only while access to the methodology, source code, object code, and sensitive know-how within the system and detailed information on the data base are specifically prohibited. Approval of access to VHSIC CAD does not imply access to or release of any fabrication or production information.

4. There is a presumption of denial for any of the following requests connected with manufacturing technology:

a. Release of CAD, Computer Aided MAnufacturing (CAM), CAE, or Computer Aided Testing (CAT) software tools specifically developed for designing VHSIC parts.
b. Release of VHSIC detailed design data.
c. Release of VHSIC-unique processing technology, hardware and software.
d. Distribution or other bulk licenses for VHSIC devices.

H. <u>VHSIC Policy Management</u> Defense Technology Security Administration (DTSA), Technology Cooperation and Security Directorate is responsible for the management of this policy. Close coordination is required with the Computer and Electronics Technology Directorate of the Office of Deputy Under Secretary of Defense for Research and Advanced Technology.

APPENDIX B

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APPENDIX C

VHSIC POINTS OF CONTACT - GOVERNMENT

DoD Program Office

VHSIC Program Director	E.D. Maynard, Jr.	202-697-4198
Directors for Technology Insertion	COL W.H. Freestone, Jr.	202-697-0864
	D.G. Hayman	202-697-0864
	Lt Col H.R. Brown, III	202-697-0864
Qualification/ VHSIC Definition	Dr. S.E. Turnbach	202-697-4198
VHSIC Phase 2	Dr. D.O. Patterson	202-697-9216
Technology Security	D.G. Hayman	202-697-0864

Army Program Office

Program Director	Dr. C.G. Thornton	201-544-2541
Deputy Program Director	H. Borkan	201-544-2583
Program Manager	R.H. Sproat	201-544-3172

Navy Program Office

Program Director	LCDR P. Gariano, Jr.	202-692-6413
Deputy Program Director	J.P. Letellier	202-767-2937

Air Force Program Office

Program Director	W.J. Edwards	513-255-2911
Program Manager	R.M. Werner	513-255-6723

VHSIC System Design Experts

Communications		
A. Lukosevicius	Army CECOM	201-544-4133
R. Peterson	Navy NOSC	619-553-1164
Electro-Optics		
J. Pupich	Army CECOM	703-664-5207
Electronic Warfare		
J. Cervini	Army CECOM	201-544-3224

Radar/Sonar		
V. Organic	Army LABCOM	201-544-3477
J.P. Letellier	Navy NRL	202-767-2937
P. Rieml	Navy NADC	215-441-1933
D. Mukai	AF AFWAL/AARM	513-255-5359
Signal Processing		
K. Bromley	Navy NOSC	619-553-2353
J.P. Letellier	Navy NRL	202-767-2937
J. Holtkamp	Navy NAC	317-353-3249

VHSIC Issue Experts

Built-In-Test/Design for Test		
W. Debany	AF RADC	315-330-2047
P. McHugh	Army LABCOM	201-544-3501
M. Vineberg	Navy NOSC	619-553-4957
Design Automation/VHDL/ADAS		
C. Bosco	Army LABCOM	201-544-2912
D. Rooney	Navy NRL	202-767-2937
J. Hines	AF AFWAL	513-255-7142
Interoperability		
A. Bard	Army LABCOM	201-544-4469
J.P. Letellier	Navy NRL	202-767-2937
D. Barker	AF AFWAL	513-255-7142
Packaging		
O. Layden	Army LABCOM	201-544-2378
P. Speicher	AF RADC	315-330-4055
D. McKee	Navy NOSC	619-553-5396
Qualification: Line Certification, Procedure, Specifications		
M. Adams	DESC EQM	513-296-6258
T. Creek	DESC ECS	513-296-6023
TISSS		
W. Russell	AF RADC	315-330-3974
J. Haberer	AF RADC	315-330-2241
VHSIC Definition		
T. Creek	DESC ECS	513-296-6023
S. Turnbach	DoD CET	202-697-4198

APPENDIX D

VHSIC CONTRACTS - POINTS OF CONTACT

	Contractor	DoD
TECHNOLOGY INSERTION		
Enhanced PLRS User Unit Hughes Aircraft Company Contracts: DAAB07-84-C-K588 DAAB07-82-C-J096	L. Hersey 213-802-4344	A. Lukosevicus 201-544-4133
ATH Mission Computer Boeing/Sikorsky Contract DAAJ02-86-C-0016	D. Tinkham 316-526-3717	G. Tomlin 314-263-1810
ATH Mission Computer McDonnell Douglas/Bell Helicopter Contract DAAJ02-86-C-0017	R. Webb 602-891-7890	G. Tomlin 314-263-1810
TOW VHSIC Automatic Target Tracker Texas Instruments Contract DAAH01-85-C-1161	E. Mooty 214-480-1918	R. Mitchell 205-876-3672
FIREFINDER VHSIC Technology Insertion Demonstration Hughes Aircraft Company Contract DAAK20-84-C-0433	L. Burnett 714-732-3686	V. Organic 201-544-3477
Combat Vehicle VHSIC Processor Westinghouse Contract DAAA21-87-C-0281	J. McKindles 301-765-7777	L. Young 201-724-7051
Combat Vehicle VHSIC Processor General Dynamics Contract DAAA21-87-C-0287	P. Hetke 619-547-3787	L. Young 201-724-7051
MEDFLI-VTAM ESL Corporation Contract DAAK20-85-C-0648	D. Klaus 408-743-6455	D. Howson 201-544-4019
MEDFLI-VMASS RCA Corporation Contract DAAB07-87-C-P040	J. Springer 609-338-3505	L. Simon 201-544-4019
HELLFIRE IIR Seeker Ford Aerospace and Communications Contract DAAH01-85-C-A138	B. Vin 714-720-7118	T.J. Peacher 205-876-3484

HELLFIRE IIR Seeker Texas Instruments Contract DAAH01-85-C-A118	W. Sullivan 214-462-4872	T.J. Peacher 205-876-3484
HELLFIRE PA/VHSIC Chip Integration McDonnell Douglas Contract DAAH01-85-C-A104	D.M. Karnes 714-986-2176	T.J. Peacher 205-876-3484
Multirole Survivable Radar Raytheon Contract DAAH01-85-C-A034	L. Gallerani 617-274-3728	T.S. Tippit 205-876-1742
Multirole Survivable Radar Westinghouse	G. Hays 301-765-2114	T.S. Tippit 205-876-1742
Enhanced Modular Signal Processor (EMSP) AT&T/Honeywell Contract N00024-81-C-7318	L. Hooker 919-279-4740	D. Howard 202-697-2465
MK50 Advanced Lightweight Torpedo Honeywell Contract N00024-83-C-6254	S. Sivan 612-931-6995	T. Singleton 202-692-0637
HF/EHF VHSIC Terminal Brassboard (VTB) TRW Contract N00039-81-C-0414	C.M. Thomas 213-536-3104	K. Taylor 202-951-2188
AN/AYK-14(V) Standard Airborne Computer CDC/Unisys Contract N00019-86-C-0002	R. Balestra 301-468-8183	T. Schlegel 202-692-2514
VHSIC Communications Processor (VCP) TRW Contract N00019-82-C-0330	A. Schmitt 619-592-3472	T. Schlegel 202-692-2514
Combat Direction Finder Sanders Associates Contract: classified	J. Stowell 603-885-7074	D. Avery 202-692-2533
AN/ALQ-131 Electronic Countermeasure Pod Block I and II Production Specification TRW Contract F09603-85-C-0867	T. Ryan 912-929-7309	M. Duffey 912-926-5804
Autonomous Guided Weapon Texas Instruments Contract DAAK20-84-C-0437	J. Medding 214-462-5822	R. Jackson 904-882-3910
Common Signal Processor (CSP) IBM Contract F33615-84-C-1470	R. Estrada 703-367-4279	D. VanClave 513-255-7708

MIL-STD-1750A Computer Westinghouse Contract F33615-84-C-1465	D. Sartorio 301-765-6744	G. Konomos 513-255-3765
MILSTAR Terminal/Modem Processor TRW Contract N00039-81-C-0414	C.M. Thomas 213-536-3104	S.H. Talbot 315-330-3091
Speech Enhancement Unit Gould/Glen Burnie, MD Contract F30602-85-C-0266	J.N. Danoulakis 301-787-2880	J. Foelker 315-330-4024
F-16 VHSIC Programmable Signal Processor (VPSP) Westinghouse Contract F33657-81-C-0115	D. Sartorio 301-765-6744	D. Bernia 513-255-6461
E-3A Signal Processor No contract yet		
VHSIC TTL Gate Array Honeywell Contract F04606-86-C-0813	D. Burns 612-541-2066	T. Glum 916-643-6454
F-15 Central Computer ARINC Research Corporation Contract F09603-82-G-3866 CDRL-0031	L. Davis 301-266-4512	D. Fowler 912-926-6226
Logistics Retrofit Engineering 1750A Electronic Module General Dynamics Contract F04606-87-D-0034	T. Williams 916-920-3663	T. Glum 916-643-6454
Logistics Retrofit Engineering F-111 Pave Sprinter Study General Dynamics Contract F04604-84-D-0065 (completed)	T. Williams 916-920-3663	T. Glum 916-643-6454
Logistics Retrofit Engineering F-111 Digital Signal Transfer Unit Rockwell Contract F04606-84-D-0048, CET 87-10-313 (Completed)	R. Owens 916-920-1215	T. Glum 916-643-6454
Generic VHSIC Spaceborne Computer (GVSC) IBM Contract F29601-87-C-0006	R. Estrada 703-367-4279	R. Herndon 505-846-0855

Generic VHSIC Spaceborne Computer Honeywell Contract F29601-87-C-0018	D. Burns 612-541-2066	R. Herndon 505-846-0855
Advanced Onboard Signal Processor IBM Contract F30602-86-C-0151	R. Kettlekamp 703-367-3930	F. Schmandt 315-330-3091
Advanced Onboard Signal Processor TRW Contract F30602-86-C-0150	E. Yang 213-536-1431	F. Schmandt 315-330-3091

PHASE 1

Honeywell - Solid State Electronics Division Contract F33615-81-C-1527	D. Burns 612-541-2066	R. Werner 513-255-4557
Hughes Aircraft - Industrial Electronic Group Contract DAAK20-81-C-0383	R. Stone 619-931-5182	R. Sproat 201-544-3172
IBM - Federal Systems Division Contract N00029-81-C-0416	R. Estrada 703-367-4279	P. Gariano 202-692-3966
Texas Instruments - Equipment Group Contract DAAK20-81-C-03822	J. Wilson 214-995-2395	R. Sproat 201-544-3172
TRW - Military Electronics Division Motorola Contract N00039-81-C-0414	T. Zimmerman 213-535-3375 E. Daniels 602-962-3094	P. Gariano 202-692-3966
Westinghouse - Advanced Technology Lab National Semiconductor Contract F33615-81-C-1532	D. Sartorio 301-765-6744 J. Streb 408-721-5448	R. Werner 513-255-4557

PHASE 2

Honeywell - Solid State Electronics Division Contract F33615-84-C-1500	D. Burns 612-541-2066 G. Anderson 612-541-2045 D. Nielsen 612-541-2482	R Werner 513-255-4557
IBM - Federal System Division Contract DAAK20-85-C-0376	R. Estrada 703-367-4279 P. Johnson 703-367-5547	R. Sproat 201-544-3172

TRW - Military Electronics Division Motorola Contract N00039-85-C-0111	T. Zimmerman 213-535-3375 C. Meyers 512-928-6940	P. Gariano 202-692-3966

PHASE 3 - DESIGN AUTOMATION

VHDL Design Workbench Gould Defense Systems Contract DAAL01-85-C-0435	S. Swamy 312-640-4466	C. Bosco 201-544-2912
VHDL/MIXSIM Simulator Sperry Contract DAAL01-85-C-0436	L. Anderson 612-456-3871	C. Bosco 201-544-2912
VHSIC Hardware Description Language (VHDL) Intermetrics Contract F33615-83-C-1003	V. Berman 301-657-3775	J. Hines 513-255-4448
VHSIC/IDAS Microcode Compiler Demonstration JRS Research Labs Contract F33615-84-C-1422	E. Warshawsky 714-974-2201	J. Hines 513-255-4448
VHDL Independent Validation and Verification United Technologies Microelectronics Center Contract F33615-85-C-1760	J. Costentino 303-594-8237	J. Hines 513-255-4448
TISSS Independent Validation and Verification Digicomp Contract F30602-86-D-0025	J. Elkens 607-273-5900	W. Russell 315-330-3974
Processor Synthesis Tool for VHDL Honeywell Computer Science Lab Contract F33615-85-C-1261	S. Krolikosky 612-887-5701	J. Hines 513-255-4448
VHDL Designer's Workstation General Electric Research Center Contract F33615-85-C-1862	J. Sturman 518-387-5457	J. Hines 513-255-4448
VHSIC Silicon Compiler Research Triangle Institute Contract F33615-85-C-1863	J. Clary 919-541-6951 G. Frank	J. Hines 513-255-4448
Interface Between CMOS Process and Silicon Compiler National Semiconductor Corp Contract F33615-85-C-1867	J. Streb 408-721-5448	J. Hines 513-255-4448

Support To IEEE VHDL Standardization CAD Language Systems, Inc. Contract F33615-86-C-1050	M. Shahdad 301-424-9445	J. Hines 513-255-4448
Joint US/Canadian VHDL Rehost Bell Northern Research U.S. Participation Contract TBD	D. Agnew 613-726-4615	J. Hines 513-255-4448
VHDL Integration Johns Hopkins University/APL Contract N00024-85-C-5301	R. Slegel 301-953-5000 X4342	H.A. Alperin 301-394-2167
ADAS Integration into VHDL Support Environment Research Triangle Institute Contract N00039-86-C-0057	J. Clary 919-541-6951	P. Hunter 202-767-3517
Annotation Language for VHDL Stanford Center for Integrated Systems Contract F33615-86-C-1137	D. Luckham 415-723-1242	J. Hines 513-255-448
AMSDS JRS Research Laboratories Contract N00039-86-C-0056	E. Warshawsky 714-974-2201	H. Roth 301-394-1480
Enhanced AMSDS JRS Research Laboratories Contract N00039-87-C-0256	E. Warshawsky 714-974-2201	H. Roth 301-394-1480
System Level Tools for the ADAM System U. of Southern California Contract N00039-87-C-0194	A. Parker 213-743-5560	V. Anderson 619-939-3100
Hierarchical Design for Testability Research Triangle Institute/ University of Virginia Contract DAAL01-86-C-0039	J. Clary 919-541-6951	C. Bosco 201-544-2912
Analog Design With VHDL Dartmouth University Contract TBD	C. Hutchinson 603-646-2238	J. Hines 513-255-4448
Object-Oriented Chip Design Using VHDL Rensselaer Polytechnic Institute Contract F33615-87-C-1435	E. Rogers 518-783-8182	N. Noclerio 513-255-7142
Artificial Intelligence Interface to the ADAS System Research Triangle Institute/OCTY, Inc. Contract DAAL01-86-C-0040	N. Kanopoulos 919-541-7341	C. Bosco 201-544-2912

Engineering Information System Honeywell/CDC/TRW/CAD Language Systems/ McDonnell-Douglas/Arizona State University Contract F33615-87-C-1401	R. Kant 612-782-7322	J. Hines 513-255-4448 V. Anderson 619-939-3100

PHASE 3 - TEST AND MAINTENANCE

Maintenance Concepts for VHSIC Honeywell Contract F30602-85-C-0091	S.P. Divakaruni 612-782-7433	D. Richards 315-330-3476
Tester Independent Support Software System (TISSS) Contract F30602-84-C-0168	D. Lehtonen 305-729-4025	W. Russell 315-330-3974

PHASE 3 - RADIATION HARDENING

Radiation Hardened Bulk CMOS Motorola Contract DNA001-84-C-0403		LCDR L. Cohn 202-325-7016
Radiation Hardened CMOS/SOS RCA Contract DNA001-84-C-0404		J.M. McGarrity 202-394-3180
Radiation Hardened Bulk CMOS Westinghouse/National Semiconductor Contract DNA001-86-C-0134		LCDR L. Cohn 202-325-7016
Radiation Hardened CMOS/SOS Hughes Aircraft Contract DNA001-84-C-0407		LCDR L. Cohn 202-325-7016
Radiation Hardened STL Bipolar Texas Instruments Contract DNA001-86-C-0175		LCDR L. Cohn 202-325-7016
Radiation Hardened 3D Bipolar TRW Contract DNA001-86-C-0186		LCDR L. Cohn 202-325-7016
Electromagnetic Effects Chip Hardening Booz-Allen Contract DAAL02-86-C-0042		R. Garver 202-394-1403

PHASE 3 - CHIP PACKAGING

High Density Multilayer Packaging Development Hughes Aircraft Contract DAAK20-83-C-0429	R.P. Himmel 714-759-2893 R.I. Brown 714-759-2497	O. Layden 201-544-2379

High Density Multilayer Packaging Development Honeywell Contract DAAK20-83-C-0430	D. Gunderson 612-541-2040 R. Speilberger 612-541-2924	O. Layden 201-544-2379
High Density Multilayer Packaging Development Martin Marietta Contract DAAK20-83-C-0427	J. Fennimore 305-356-2086 G. Plite 305-356-7909	O. Layden 201-544-2379
Multichip Packages Texas Instruments Contract DAAL01-85-C-0442	R. Natali 214-995-3169	O. Layden 201-544-2379
Perimeter Chip Carrier Package General Ceramics/Martin Marietta Contract DAAL01-86-C-0001	K. Verma 714-630-6108	O. Layden 201-544-2379
Tape Automated Bonding (TAB) Honeywell/3M Contract DAAL01-85-C-0441	R. Maciolak 612-541-2914	O. Layden 201-544-2379
VHSIC Low Dielectric Constant Printed Wiring Boards Hughes Aircraft Contract F33615-84-C-1415	R.W. Siebold S. L. Oldhaus	A. Tewksbury 513-255-4557

PHASE 3 - LITHOGRAPHY

X-Ray Lithography Equipment Perkin-Elmer Contract DAAK20-84-C-0378	G. Ferrera 203-834-6610	R.J. Zeto 201-544-4872
Advanced Wafer Imaging System (AWIS) GCA Contract DAAL01-85-C-0460	P. Bachman 617-275-9000	R. Reams 202-394-3190
Laser Pantography Lawrence Livermore Laboratory National Laboratory Task Assignment	L. Wood B. McWilliams 415-422-7286	J.P. Letellier 202-767-2937
Optically Defined Submicron CMOS Texas Instruments DAAL01-86-C-0021	D. Mercer J. Salzman	R.J. Zeto 201-544-4872

PHASE 3 - RELIABILITY AND QUALIFICATION

VHSIC Generic Qualification Procedures GE/ATT/Honeywell Contract F30602-86-C-0172	P. Tracey 315-793-7491	C. Messenger 315-330-3766

Reliability Assessment of Gate Arrays GTE Contract F30602-86-C-0176	J. Meschi 312-681-7273	C. Windisch 315-330-2047
Non-Destructive Evaluation of Metallurgical Tape Bonds Vanzetti Contract F30602-86-C-0049	A. Traub 617-828-4650	P. Speicher 315-330-4055
Non-Destructive Package Screening Sonoscan Contract F30602-86-C-0050	L. Kessler 312-766-7088	P. Speicher 315-330-4055
Reliability Prediction Modeling IIT Research Institute/Honeywell Contract F30602-86-C-0261	W. Denson 315-330-4151 R. Maciolek	P. Manno 315-330-4635
VHSIC Impact on System Reliability General Dynamics Contract F30602-85-C-0007	S. Gray 817-763-3441	B. Dudley 315-330-2608

PHASE 3 - COMPLETED PROJECTS	DTIC NUMBER
1. Architectural Studies	
Signal Processing Algorithms on Chips Arizona State University Contract N00039-80-c-0511	AD-B072-124
Storage/Logic Arrays Boeing Contract F33615-80-C-1196	AD-B954-381L
A Hierarchical Design Approach for VHSIC Carnegie Mellon Contract N00039-80-C-0640	AD-B071-076
Study of VHSIC Applications in Naval Patrol Aircraft Lockheed Contract N00019-80-C-0610	AD-8074-271/2
Generalized Computer System Simulator for VHSIC Naval Air Development Center In-House	
Signal Processor Architecture Performance Evaluation Tool Research Triangle Institute Contract DAAK20-80-C-0275	AD-B102-719L

Memory Processor Study — AD-B068-519
Sanders Associates
Contract F33615-80-C-1192

Fault Tolerant Architecture for VHSIC — AD-B065-4998
Stanford Research Institute
Contract F30602-80-C-0303

Assignment Algorithms for Control of VHSIC Chips — AD-B067-642
Stanford Research Institute
Contract N00039-80-C-0571

Data Flow Architecture — AD-B071-864/5-7
Texas Instruments
Contract DAAK20-80-C-0276

Software Architecture Study — AD-B067-869
TRW
Contract F33615-80-C-1202

Architectures for Radar Signal Processing
University of Southern California
Contract N00039-80-C-0641

2. Lithography

Concentrating Collimating Illumination — AD-B067-869
for X-Ray Lithography
American Science and engineering
Contract N00019-80-C-0568

High Intensity Pulsed Plasma X-Ray Source — AD-B066-469L
AVCO Research
Contract F19628-80-C-0176

Ultra High Speed Submicron Direct Write
E-Beam System
EBC Corp.
Contract N00019-80-C-0618

Advanced Resist Materials and Processes
Hewlett Packard
Contract DAAK20-80-C-0264

Improved Resists for Electron-Beam Lithography
Hughes Research
Contract N00019-80-C-0616

E-Beam Lithography Components for Direct Writing — AD-B094-565L
Hughes Research
Contract DAAK20-80-C-0262

X-Ray and E-Beam Effects on MOS Devices
Naval Research Laboratory
In-House

Extension of X-Ray Lithography Technology — AD-B074-215
Perkin-Elmer
Contract DAAK20-80-C-0261

Intense Plasma X-Ray Source for
Submicron Lithography
Stanford Research Institute
Contract F33615-80-C-1194

Electron Beam System Software — AD-B078-420/421
TRW
Contract DAAK20-80-C-0263

Develop Direct Write E-Beam Lithography Components
Varian Associates
Contract F19628-80-C-0173

3. Processing

Coronaphoresis for Gas Purification — AD-B077-419
AVCO Research
Contract N00039-80-C-0589

Improved Crystal Quality of Silicon On
Insulated Substrates
Cornell University
Contract F33615-80-C-1197

Low Temperature Silicon Epitaxy
Hughes Research
Contract N00019-80-C-0616

Low Temperature Photochemical Processing — AD-B085-497L
For VHSIC Applications
Hughes Research
Contract DAAK20-80-C-0268

Laser Annealing
Hughes Research
Contract DAAK20-80-C-0269

Electron Beam Processing
Hughes Research
Contract DAAK20-80-C-0270

Extend Microlithography Technology Through Plasma Etching — AD-B085-912
Perkin-Elmer
Contract DAAK20-80-C-0265

4. Design Automation

Demonstrate Use of VLSI Design Rules Standards, and Interfaces — AD-B077-602/3/4
California Institute of Technology
Contract N00014-79-C-0924

CAD for Testable LSI — AD-B095-571L
General Electric
Contract F33615-80-C-1083

Critical VHSIC Design Tools
Sandia Laboratory
Contract P.O. 81-19638/39

Transportability of CAD Data — AD-B067-139
TRW Contract F33615-80-C-1198

Design Automation — AD-B075-616
University of Southern California
Contract DAAK20-80-C-0278

5. Materials and Characterization

Analytical Methods for Detecting Substrate Defects
Cornell University
Contract F33615-80-C-1197

VHSIC Silicon Starting Materials
Hughes Research Laboratory
Contract N00039-83-C-0725

Refractory Metal for Interconnection — AD-B082-339
Hughes Aircraft
Contract DAAK20-80-C-0273

X-Ray Diagnostic Techniques for VHSIC Silicon
Texas Instruments
Contract N00039-83-C-0722

VHSIC Starting Materials - Diagnostics
VTI, Inc.
Contract N00039-83-C-0723

Mobility/Drift Velocity Measurement In
Inversion Layers
Westinghouse
Contract DAAK20-80-C-0271

Improved SOS for VHSIC — AD-B078-171
Westinghouse
Contract F33615-79-C-1946

Low Defect Density Silicon Substrates — AD-B102-419L
for NMOS
Westinghouse
Contract N00039-80-C-0662

VHSIC Silicon Starting Materials
Westinghouse
Contract N00039-83-C-0724

6. Device Technology

Simple Submicron Device Models for — AD-B958-232L
Circuit Simulation
Cornell University
Contract F33615-80-C-1197

Submicron Devices: Exact Simulation and
Simple Models
Cornell University
Contract F33615-80-C-1197

Development of MESFET Silicon on Sapphire — AD-B068-304
For IC Gates
GE
Contract DAAK20-80-C-0272

Static Induction Transistor (SIT
Logic Technology
Hughes Aircraft
Contract N00019-80-C-0616

Low Resistivity Gates for CMOS ICs — AD-B066-109L
Rockwell
Contract DAAK20-80-C-0274

Industry Impact of VHSIC Program:
A Preliminary Analysis
The Analytical Science Corp.
Contract N00039-80-C-1199

7. Packaging

Improved Package for VHSIC — AD-B080-965
General Electric
Contract F33615-80-C-1191

Electronic Packaging for VHSIC — AD-B070-866
Honeywell
Contract DAAK20-80-C-0267

High Density, High Performance Hybrid — AD-B069-485
Circuit Technology
Raytheon
Contract F33615-80-C-1193

HCC-Compatible PWB Materials
Westinghouse
Contract F33615-82-C-5047

8. Testing and Reliability

VHSIC Yield Enhancement Test Structure
Aerospace Corp/JPL
Contract F4071-83-C-0084

Advanced High Speed Test System
Genrad
Contract F33615-84-C-5076

Failure Management Design System — AD-B074-223
Hughes Aircraft
Contract DAAK20-80-C-0277

Electron Beam Circuit Tester — AD-B073-808
Hughes Aircraft
Contract F30602-80-0321

Acoustic Microscopy for Inspection
of VHSIC Chips
Hughes Aircraft
Contract N00039-80-C-0625

Reliable, High Performance VHSIC System — AD-B089-167
University of Illinois
Contract N00039-80-C-0556

Measurement Technology for VHSIC
National Bureau of Standards
Contract N00019-79-IP-990003

Tester Independent Support Software System
Prospective Computer Analysts
Contract F30602-84-C-0167

Identify and Assess On-Chip Self Test and Repair Concepts — AD-B087-155
Research Triangle Institute
Contract N00039-80-C-0648

Signal Processor Architecture
Performance Evaluation Tool
Research Triangle Institute
Contract DAAK20-80-C-2075

Test Structure Development
Rockwell
Contract F33615-82-C-5110

Testing VHSIC Devices
Stanford University
Contract DAAK20-80-C-0266

Develop Test Technology for VHSIC
Texas Instruments
Contract F30602-81-C-0032

Design for Testability and Reliability — AD-B086-080
University of Southern California
Contract N00039-80-C-0641

APPENDIX E

EXHIBITORS AT VHSIC CONFERENCES

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Jay Harford
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703-367-1041

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National Semiconductor Corp. P.O. Box 58090 2900 Semiconductor Drive M.S. D3606 Santa Clara, CA 95051	Jerry Streb 408-721-5448
Naval Research Laboratory Code 5305 Washington, DC 20375	James J. Alter 202-767-3517
Performance Semiconductor 610 East Weddell Drive Sunnyvale, CA 94089	Les Wellborn 408-734-8900
Raytheon Company Microelectronics Center 358 Lowell Street Andover, MA 01810	John Maxfield 617-470-9050 Scott W. Stephen 617-470-9114
Research Triangle Institute Center for Digital Systems Research P.O. Box 12194 Herbert Building Research Triangle Park, NC 27709	James B. Clary 919-541-6951
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APPENDIX F

GLOSSARY OF ACRONYMS AND TECHNICAL TERMS

4PM	Four Port Memory
A-6F	Navy Attack Aircraft
AASP	Advanced Anti-Radiation Missile Signal Processor
ABBM	Acoustic Beamformer Brassboard Module
ACCS	Army Communications/Command System
ACE	Array Computing Element
ACS	Array Controller/Sequencer
ADAM	Advanced Design Automation System
ADAS	Architecture Design and Assessment System
ADB	Advanced Digital Bipolar (Honeywell technology)
AEBLE	Advanced Electron Beam Lithography Equipment
AEGIS	Advanced Electronic Guidance and Intercept System
AFIT	Air Force Institute of Technology
AG	Address Generator
AI	Artificial Intelligence
AJ	Anti-Jam or Jam Resistant
ALU	Arithmetic Logic Unit
ALWT	Advanced Lightweight Torpedo (MK-50)
AMAC	Add Multiply Accumulate
AMGS	Automatic Microcode Generation System
AMSDS	Automated Microcode Compiler Synthesis & Design System
AMTE	Automated Microcircuit Test Equipment
AN/ALQ-131	Airborne Pod-Mounted Electronic Countermeasure (ECM)
AN/ALR-56C,-74	AF Radars
AN/APG-65	Navy Coherent Multimode Pulse Doppler Radar
AN/APG-68	Airborne Fire Control Radar
AN/AYK-14(V)	Navy Embedded Standard Airborne Computer
AN/BQQ-5	Sonar System
AN/TPQ-36,-37	Army Radars (Firefinder)
AN/UYS-1,-2	Navy Standard Signal Processors
AOSP	Advanced Onboard Signal Processor
AP	Arithmetic Processor
APC	Array Processor Controller
APE	Asynchronous Processing Element
APIO	Array Processor Input/Output
APU	Arithmetic Pipeline Unit; Array Processing Unit
ARM	Anti-Radiation Missile
ASP	Advanced Signal Processor
ASW	Antisubmarine Warfare
ATE	Automatic Test Equipment
ATF	Advanced Tactical Fighter
ATR	Auto Target Recognition
AU	Arithmetic Unit
AV-8B	Marine Vertical Takeoff and Landing (VTOL) Aircraft
AWACS	Airborne Warning and Control System
AWIS	Advanced Wafer Imaging System
Ada	DoD High Order Programming Language
BEOL	Back End of Line

BIST	Built-In Self Test
BIT	Built-In Test
BIU	Bus Interface Unit
BOPS	Billion Operations Per Second
Brassboard	Field Demonstrable Electronic Model
Breadboard	Laboratory Demonstrable Electronic Model
C3I	Command, Control, Communications, and Intelligence
CAD	Computer Aided Design
CALMA	Graphics design system marketed by CALMA Corporation
CAM	Content Addressable Memory
CAM	Computer-Assisted Manufacturing
CAVP	Complex Arithmetic Vector Processor
CC-BUS	Chip to Chip Bus
CDP	Configurable Data Path (chip)
CDR	Critical Design Review
CDRL	Contract Data Requirements List
CGA	Configurable Gate Array
CMAC	Complex Multiply Accumulate
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CS	Convolver Superchip
CSP	Common Signal Processor
CSR	Configurable Static RAM
CTTC	Circuit Technology Test Chip (Honeywell)
DAST	Design, Architecture, Software, and Test
DESC	Defense Electronics Supply Center
DF	Direction Finder
DIFAR	Directional Frequency Analysis and Recording
DIU	Device Interface Unit
DNA	Defense Nuclear Agency
DOD	Department of Defense
DPU	Data Processor Unit
DRAM	Dynamic RAM
DSPE	Double Solid Phase Epitaxy
DTIC	Defense Technical Information Center
E-2C	Navy Airborne Warning and Control System (AWACS)
E-3A	SENTRY Air Force AWACS
E-BEAM	Electron-Beam
EA-6B	Navy EW Aircraft
EAR	Export Administration Regulations
EAU	Extended Arithmetic Unit
EAUM	Extended Arithmetic Unit Multiplier
EBL	Electron Beam Lithographic (Machine)
ECCM	Electronic Counter Countermeasures
ECM	Electronic Countermeasure
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHF	Extremely High Frequency
EIS	Engineering Information System
ELINT	Electronic Intelligence
EMC	Electromagnetic Compatibility

EME	Electromagnetic Effects
EMI	Electromagnetic Interference
EMP	Electromagnetic Pulse; Electromagnetic Potential
EMSP	Enhanced Modular Signal Processor
EO	Electro-Optic
EOSP	Electro-Optic Signal Processor
EOSPC	Electro-Optic Signal Processor Controller
EP-3E	Electronic Surveillance Aircraft
EPLRS	Enhanced Position Location and Recording System
EPUU	Enhanced PLRS User Unit
ESD	Electrostatic Discharge
ESM	Electronic Support Measure
ETM-Bus	Element Test and Maintenance Bus
EW	Electronic Warfare
F-14D	Navy Fighter Aircraft
F/A-18	Navy Fighter Attack Aircraft
FAR	Federal Acquisition Regulation
FEOL	Front End of Line
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FLIR	Forward Looking Infrared
FOG-11	Missile
FPAP	Floating Point Arithmetic Processor
FSED	Full Scale Engineering Development
FTR	Functional Throughput Rate
Firefinder	Army Target Locator System
GBU	General Buffer Unit
GFE	Government Furnished Equipment
GOMAC	Government Microelectronics Applications Conference
GPC	General Purpose Computer
GVSC	Generic VHSIC Spaceborne Computer
HBX	High Brightness X-ray
HDL	Hardware Description Language
HF	High Frequency
HOL	Higher Order Language
HSL	Hierarchical System Language
Hellfire	Anti-Armor Weapon System
Hercules	Hughes CAD system
I/O	Input/Output
IAC	Information Analysis Center
IAPU	Image Array Processing Unit
IC	Integrated Circuit
ICNIA	Integrated Communication, Navigation, Identification Avionics
IDAS	Integrated Design Automation System
IEEE	Institute of Electrical and Electronics Engineers
INEWS	Integrated Electronic Warfare System
IPS	Instructions Per Second
IRHVTA	Infra-Red (seeker for) High Value Target Acquisition
IRST	Infrared Search and Track
ISA	Instruction Set Architecture; Imaging Sensor Autoprocessor

ITAR	International Traffic in Arms Regulations
IV&V	Independent Validation and Verification
IVTM	Interconnect Verification Test Module
IVV	Independent Validation and Verification
JEDEC	Joint Electronic Devices Engineering Council
JTIDS	Joint Tactical Information Distribution System
LAMPS	Light Airborne Multipurpose System
LCCC	Leadless Ceramic Chip Carrier
LHX	Light Helicopter Experimental
LOFAR	Low Frequency Analysis and Recording
LP	Laser Pantography
LRE	Logistics Retrofit Engineering Program
LRM	Line Replaceable Module
LSI	Large Scale Integration
M2F2	Multimode Fire and Forget Missile
MAC	Multiplier/Accumulator
MADS	Maintenance And Diagnostics System
MC	Micro-Controller
MCC	Multiple Chip Carrier
MCP	Multichip Package
MEDFLI	Miniaturized Electronic Direction Finding Location Indicator
MICROMETER	Micron = 10(-6) Meter
MICRON	Micrometer = 10(-6) Meter
MIL-STD	Military Standard
MILSTAR	EHF Satellite Communication System
MIPS	Million Instructions Per Second
MK-50	Advanced Light Weight Torpedo (ALWT)
MMG	Multimode Guidance
MMS	Mass Memory Superchip
MMW	Millimeter Wave
MOPS	Million Operations Per Second
MOS	Metal-Oxide Silicon
MOSFET	Metal-Oxide Silicon Field Effect Transistor
MPS	Multipath Switch
MRSR	Multirole Survivable Radar
MS	Matrix Switch
MSI	Medium Scale Integration
MTBF	Mean-Time-Between-Failure; Mean-Time-Between-Fault
MTTR	Mean Time to Repair
NMOS	N-Channel Metal-Oxide Silicon
OPS	Operations per Second
OSD	Office of the Secretary of Defense
OUSDA	Office of the Under Secretary of Defense for Acquisition
OUSDR&E	Office of the Under Secretary of Defense for Research and Engineering
P3	Naval Patrol Aircraft
P3-C	Navy ASW Aircraft
P3I	Preplanned Product Improvement
PAVE SPRINTER	Modular Avionics Demonstration Program
PE	Processing Element
PGA	Pin Grid Array

PI-BUS	Parallel Interface Bus (designed during VHSIC-2)
PJH	PLRS/JTIDS Hybrid
PLA	Programmable Logic Array
PLAU	Pipeline Arithmetic Unit
PLRS	Position Locating and Reporting System
POC	Proof of Concept
PPP	Parallel Pipeline Processor
PRDA	Project Research & Development Announcement
PROM	Programmable Read-Only Memory
PSP	Programmable Signal Processor
PWB	Printed Wiring Board
QCI	Qualification Conformance Inspection
QML	Qualified Manufacturers List
QPL	Qualified Products List
RALU	Register Arithmetic Logic Unit
RAM	Random Access Memory
ROM	Read Only Memory
RPV	Remotely Piloted Vehicle
RTL	Register Transfer Language
RWR	Radar Warning Receiver
S3	Naval Early Warning Aircraft (including radar system)
SCM	Single-Chip Module (used interchangeably with SCP)
SCP	Single-Chip Package (used interchangeably with SCM)
SDI	Strategic Defense Initiative
SECDED	Single Error Correct, Double Error Detect
SEM	Standard Electronic Module
SEU	Speech Enhancement Unit
SEU	Single-Event Upset
SGEMP	System Generated Electromagnetic Pulse
SH-60B	(Sikorsky) Helicopter Aircraft
SI Chip	System Interface Chip (BIU + FIU)
SLAM	Scanning Laser Acoustic Microscope
SOW	Statement of Work
SP	Signal Processor
SPE	Signal Processing Element
SPEAR	Solid Phase Epitaxy and Regrowth
SPICE	Public Domain Integrated Circuit Simulation Program
SQC/SPC	Statistical Quality & Process Control
SPS	Systolic Processing Superchip
SRAM	Static RAM; Short Range Attack Missile
SSI	Small Scale Integration
STL	Schottky Transistor Logic
STS	Signal Tracking Subsystem
SubACS	Submarine Advanced Combat System
TAB	Tape Automated Bonding
TAM	Threat Association Module
TISSS	Tester Independent Support Software System
TM-BUS	Test and Maintenance Bus
TOW	Tube Launched, Optically Tracked, Wire Guided Missile
TREE	Transient Radiation Effects in Electronics
TTL	Transistor-Transistor Logic

VAG	Vector Address Generator
VALU	Vector Arithmetic/Logic Unit
VAX	DEC 32-Bit Commercial Computer
VBIU	VHSIC Bus Interface Unit
VCB	VHSIC Communications Brassboard
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuits
VID	VHSIC Insertion Demonstration for the EMSP
VLM	Very Large Memory
VLSI	Very Large Scale Integration
VPC	Vector Product Calculator
VPO	(DoD) VHSIC Program Office
VPSP	VHSIC Programmable Signal Processor
VSC	VHSIC Signal Conditioner
VTCA	VHSIC Transmit Control Assembly
WAM	Window Addressable Memory
WCL	Wireless Command Link
WSI	Wafer Scale Integration
XSAR	X-ray Step and Repeat Lithographic Machine
YE	Yield Enhancement
YVR	Yield Verification Run

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