AD-A191 891 COMPARING TESTABILITY MEASUREMENT TOOLS ON A VLSI BOARD 1/1
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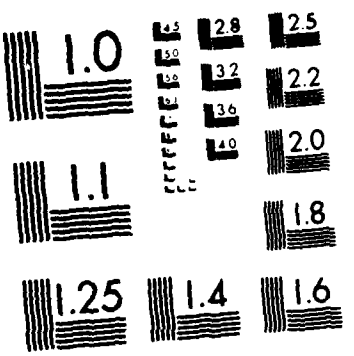

AD-A191 891

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution is unlimited.
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION Naval Ocean Systems Center 6b. OFFICE SYMBOL (if applicable)	7a. NAME OF MONITORING ORGANIZATION
6c. ADDRESS (City, State and ZIP Code) San Diego, CA 92152-5000	7b. ADDRESS (City, State and ZIP Code)
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Space & Naval Warfare Systems Command 8b. OFFICE SYMBOL (if applicable) SPAWAR	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State and ZIP Code) Washington, DC 20363-5100	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO: DMN; PROJECT NO: EE02; TASK NO: SPWR; AGENCY ACCESSION NO: DN213 123

11. TITLE (Include Security Classification)
Comparing Testability Measurement Tools on a VLSI Board

12. PERSONAL AUTHOR(S)
J.C. Bussert

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Journal Article	FROM _____ TO _____	September 1986	

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	complex module bit-slice microprocessors

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

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20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
☐ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☐ DTIC USERS	UNCLASSIFIED
22a. NAME OF RESPONSIBLE INDIVIDUAL J.C. Bussert	22b. TELEPHONE (Include Area Code) 619-225-6173
	22c. OFFICE SYMBOL Code 936

DD FORM 1473, 84 JAN

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COMPARING TESTABILITY MEASUREMENT TOOLS ON A VLSI BOARD

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ABSTRACT

There are three types of tools available to calculate a Testability Figure of Merit (TFOM) during the design process, in compliance with MILSTD-2165. These are checklists, logic models and workstation CAD enhanced Sandia Controllability/Observability Analysis Program (SCOAP) software. All of these TFOM tools are compared before and after design for testability (DFT) enhancements on a military microprocessor module.

INTRODUCTION

A complex module with severe testability problems was selected as the benchmark UUT. The module has four 2901 bit-slice microprocessors and five PROMs among the 44 ICs. With fourteen layers and 135 edge pins, this module from a modern fighter, is felt to be a representative state of the art design example. In contrast to an earlier small scale integrated circuit (SSI) UUT TFOM comparison, the more powerful tools in this evaluation were to provide DFT advice to the user and themselves drive the redesign. Next the modified UUT was rerun on all tools, and the final advantages and weaknesses of each tool's performance are noted.

CHECKLISTS

The MILSTD-2165 Appendix B is used and its subjective weighting and item selection are still worrisome. The lack of objectivity and contol, allow virtually any desired TFOM number to be achievable through gamesmanship. The good items could be a good core for a rule based TFOM expert system. Many of the items are logistic cradle to grave issues that do not even belong in an up-front TFOM content. Although checklists are crude, if properly used, the Appendix-B is better than many computer algorithms in bringing out the importance of clock lines, and crediting Built-in-Test (BIT) features. It also points out fan-in and fan-out nodes very well.

The Rome Air Development Center (RADC) digital PCB checklist was published in RADC-TR-79-327. This checklist was very poor for this module, due to its severe penalty on sequential and LSI devices, and no credit being given for BIT features. The RADC fan-out and fan-in sheet is very useful not only for this list, but also with the 2165 sheets. The RADC list has excellent grading objectivity and mandatory weighting, but due to its unforgiving penalties for sequential devices, it is useful only on combinational digital UUTs. The RADC list is the shortest and easiest TFOM tool around.

LOGIC MODELS

The DETEX Inc Logic Model (LOGMOD) tool has been around and been used on numerous systems over 15 years. It has greatly improved in the past two years since it was run on the SSI board.. It was especially strong in its feedback loop identification and recommended test point locations. Logmod relentlessly finds embedded feedback loops when the obvious ones are broken. It now has a very user friendly report format that augments the unweildy matrix graph that was relied upon previously. With available Detex training, the user can enter and interpret the results very easily. A logic model weakness is that all items and lines entered in the network are equal. This infers that a microprocessor is the same as a flip-flop or a resistor. It likewise says that a clock or tristate are of no more importance than a data line for the test programmer. Logmod had demonstrated fault isolation and logistic support features and has ILS utility other than TFOM. There is no upper node limit and VHSIC complexity has been modeled on Logmod. Logmod is a proprietary vendor tool to be leased for use.

The ARINC Research Corp System Testability And Maintenance Program (STAMP) has been upgraded from an earlier 200 node Apple program to a H-P A900 with over 2000 nodes capacity. STAMP has 23 different numerical TFOM measures that are obscure to the user and require contractor assistance in clarifying the results. The user friendly reports that were on the Apple program are not available on the H-P version. Arinc

CH 2299-6/86/0000-0171 $1.00 © 1986 IEEE

prefers to have its people retain possession of and run the proprietary STAMP program. Then Arinc personnel explain it for the customer, on a contractor deliverable basis. The same logic model assumption that all lines and items are of equal testability importance is in STAMP. There is a 2000 node upper limit, but this could be raised with additional memory. STAMP also has demostrated good logistic support experience and models from board to the system level.

CAE ENHANCED SCOAP

The CALMA workstation Controllability/Observability Predictability Testability Report (COPTR) is an enhanced top-down tool with a complete model library. Nodes difficult to observe or control had high number values, and a "-1" if impossible to see or toggle. The high observe/control numbers guide the user to circuit problem areas. One problem area that users should be aware of, is that non-gate level models in the library will not play on the COPTR. The 2901s and PROMs had to be jury-rigged with inserted gates to play on the COPTR. A problem was the CAD listing of device internal gate observe/control numbers not useful at the board level. Another was the printing of CAD assigned default gibberish numbers instead of the signal or pin labels that were keypunched in. Replacing software assigned default names and suppressing device internal nodes requires further vendor work for the user needs.

The DAISY Workstation Daisy Testability Analyzer (DTA) was the most powerful tool used, and included an automatic test point insertion by software mode. This is done by putting a test point at each node and analyzing the total circuit impact. This requires CPU time and is best done overnight. A manual test point placement mode like the CALMA, is also available.

The Daisy lack of menu format made it harder to use, since typing commands can be more error prone. Daisy also had a complete chip library, including microprocessors and memory devices, and they all ran on the DTA program.

CONCLUSIONS

The improvement in tools available and better features from 1983 and 1985 is impressive. Increased use of all of the testability tools will be incentive for improvements and more powerful tools in the future. Nearly all of the vendors were eager for user feedback and advice on improvements. Due to the proprietary vendor costs associated with available logic models, NOSC has contracted the development of a government-owned TFOM algorithm. This tool, called Computer Aided Fault Isolation Testability (CAFIT) model, should be available free for government design use in 1987.

There is no simple answer to the inevitable question, "Which tool is best?" Some are limited to digital, but 2165 and both logic models are suitable for analog or mechanical technology, and from board to top system level as well. If CAD workstations are available, the choice is two brands now. Although released too late for this evaluation, GenRad's HITAP is claimed to play on many workstation brands. Recommendations for CAD tool improvements include needed compatibility between CAD gate level testability tools, and functional library models. Hopefully, this paper will make designers and government agencies aware of the available TFOM tools, and help them decide on the optimum one for their particular module or system.

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