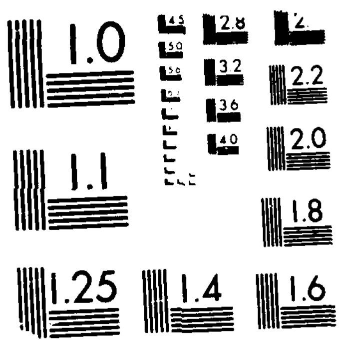
AD-A191 650 AUTOMATED TEST DEVICE FOR FASR (FIXED ARRAY SURVEILLANCE RADAR) BEAM STEERING COMPONENTRY(U) NAVAL RESEARCH LAB WASHINGTON DC R A SCOTT 10 FEB 88 1/1

UNCLASSIFIED NRL-MR-6143 F/G 17/9 NL



MICROCOPY RESOLUTION TEST CHART

Naval Research Laboratory

Washington, DC 20375-5000

(2)

NRL Memorandum Report 6143

AD-A191 650

Automated Test Device for FASR Beam Steering Componentry

RUSSELL A. SCOTT

Target Characteristics Branch
Radar Division

February 10, 1988

Approved for public release, distribution unlimited

88 3 14 013

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved OMB No 0704-0188

1a REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY 2b. DECLASSIFICATION / DOWNGRADING SCHEDULE	3 DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
4 PERFORMING ORGANIZATION REPORT NUMBER(S) NRL Memorandum Report 6143	5 MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION: Naval Research Laboratory 6b OFFICE SYMBOL (If applicable): 5346	7a. NAME OF MONITORING ORGANIZATION Naval Sea Systems Command
6c. ADDRESS (City, State, and ZIP Code) Washington, DC 20375-5000	7b ADDRESS (City, State, and ZIP Code) Washington, DC 20362-5101
8a. NAME OF FUNDING / SPONSORING ORGANIZATION: Naval Sea Systems Command 8b OFFICE SYMBOL (If applicable): NAVSEA	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State, and ZIP Code) Washington, DC 20362-5101	10 SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO: 62172N PROJECT NO: TASK NO: RS12-131-000 WORK UNIT ACCESSION NO: DN780-226

11 TITLE (Include Security Classification)

Automated Test Device For FASR Beam Steering Componentry

12. PERSONAL AUTHOR(S)
Scott, Russell A.

13a. TYPE OF REPORT	13b TIME COVERED	14 DATE OF REPORT (Year, Month, Day)	15 PAGE COUNT
Interim	FROM ______ TO ______	1988 February 10	16

16 SUPPLEMENTARY NOTATION

17 COSATI CODES			18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Automated testing; Radar; Microprocessor based; Phased Arrays

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

The Fixed Array Surveillance Radar System uses an automated test device known as the Axis Box Tester. An axis box serves as a distribution point connecting the horizontal and vertical busses of the array and monitors the rf of phase shifters and aids with beam steering. The tester diagnoses axis boxes and verifies proper operation. All digital circuitry is tested, including all data flow paths to and from the phase shifters, all control line information, and all circuitry to select rows and columns. The tester attempts to provide information that will aid, if not solve problems. The software is parsed into modules that perform various tests upon the axis box. The hardware, which uses a single-board computer with an Intel 8086 microprocessor, provides the interface between the microprocessor and the axis box. The tester provides very accurate diagnostics and can reduce debugging time by a factor of 100. Some problems prevent the tester from doing more than guessing at possible causes of a problem.

(continues)

20 DISTRIBUTION / AVAILABILITY OF ABSTRACT ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	21 ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED
22a NAME OF RESPONSIBLE INDIVIDUAL R. A.Scott/E. E. Maine	22b TELEPHONE (Include Area Code): 202 767-2301 22c OFFICE SYMBOL: 5346

DD Form 1473, JUN 86 Previous editions are obsolete SECURITY CLASSIFICATION OF THIS PAGE

S/N 0102-LF-014-6603

CONTENTS

AUTOMATED TEST DEVICE FOR FASR BEAM STEERING COMPONENTRY

INTRODUCTION

The Fixed Array Surveillance Radar system (FASR) uses an automated test device known as the Axis Box Tester. As Fig. 1 shows, the antenna subsystem includes units such as axis boxes, phase shifters, and computer controllers. Inside the radar system are 27 axis boxes and 297 phase shifter elements arranged in an array. A complete description of the architecture and beam steering process has already been presented*. The axis box is defined as "a multiport box containing logic that interconnects the horizontal backplane bus (axis box bus) to the vertical bus (phase shifter bus). The circuitry supports the beam steering function and has 11 monitor circuits to measure the RF performance for 11 phase shifters"*. An exterior view of FASR is shown in Fig. 2. The tester plays the role of a technician. Users can verify correct operation or diagnose and locate possible problems by hooking up the tester to an axis box through RS-232 cables (underlined terms are defined in glossary) and running the axis box diagnostic routines that are burned into programmable read-only memory (PROM). The axis box is comprised of both a digital and analog portion. The tester only checks the digital circuitry. The project is broken into two components: software and hardware. The software system will be discussed first.

SOFTWARE

The axis box tester's software shares space inside a PROM with two other test routines. These routines are the Phase Shifter Test and the Cable Select Test. All three programs share common resources of Input/Output (I/O) routines, which enable communications to the Cathode Ray Tube (CRT) monitor. All tests are accessed by the common menu for the FASR test routines.

The tester's software conforms to the numbering scheme established for the IC's on-board the axis box. Since each IC has its own number, a technician can quickly locate and replace a faulty IC.

The assembly computer programs were developed on the Textronix Microcomputer Development Lab's (MDL) 8540, 8550, and 8560. The software is broken down into various modules to increase efficiency and reduce extraneous code.

The software tasks were parsed into the Main Routine, Initialization Routine, Column Select Test, Row Select Test, Phase Shifter Read and Write Lines Test, Print Error Message Routine, and the Control Lines Test. The software tasks are summarized in Table 1.

*J. M. Willey, "An Architecture to Beam Steer and Monitor A Phased Array Radar Antenna", NRL Report 8965, June 12, 1986.

Manuscript approved October 27, 1987.

Fig. 1 — (The following radar components are visible: (1) two axis boxes are side by side; (2) a glimpse of a phase shifter; and (3) all computer controllers.)

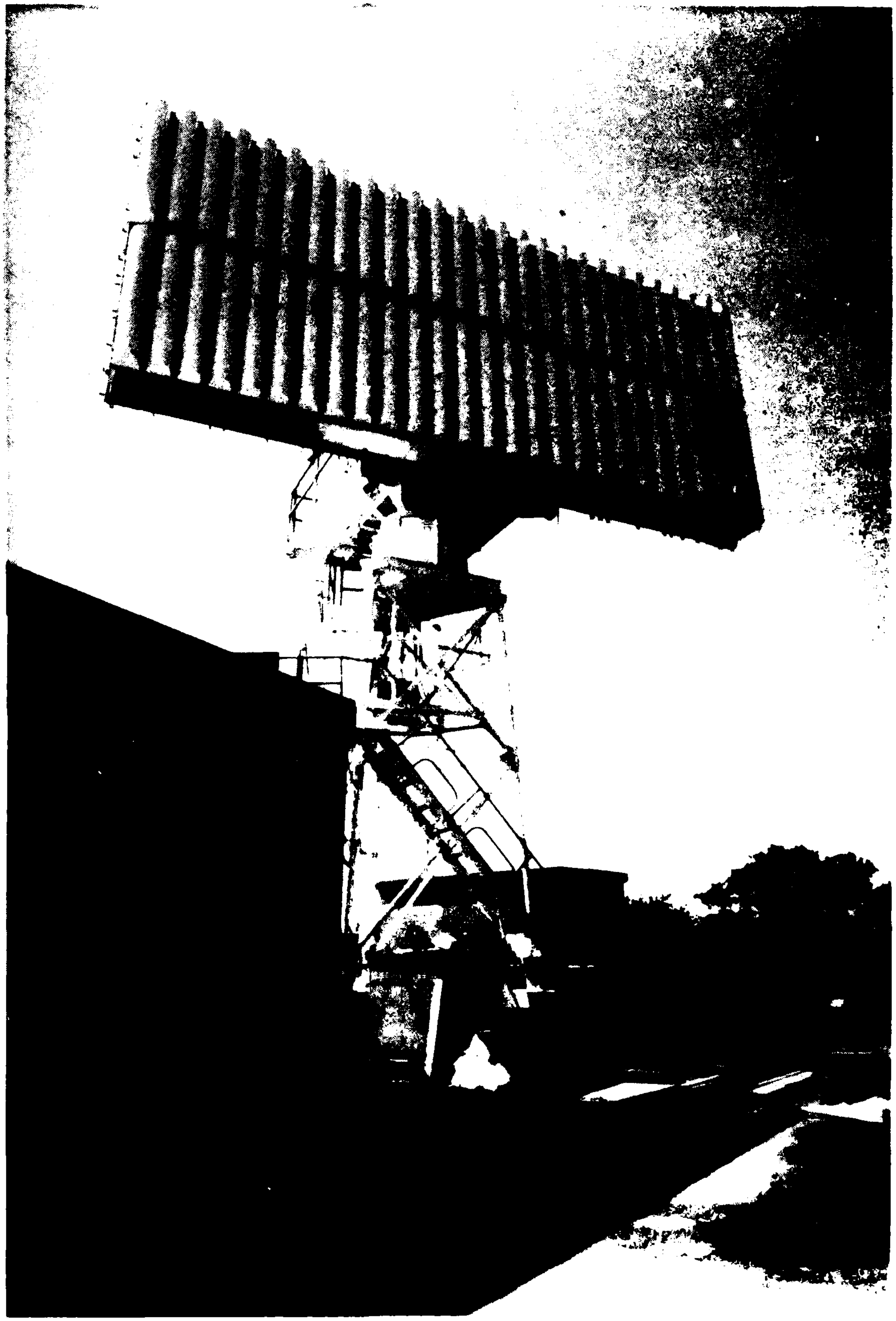


Fig. 2 ... FASR ... W ...

Table 1 - Summary of Tester's Software

Summary of Software Tasks		
Routine/Test	Purpose	Accuracy/Efficiency
Main	Calls all other modules, except Initialization Routine; Provides test menus; startup procedure	Modular organization decreases redundancy and increases speed
Column Select	Verify all Columns	Limited only by shared select circuitry
Row Select	Verify all Rows	Limited only by shared select circuitry
Initialization	Defines all constants, variables, macros, and look-up tables	Global data management maximizes efficiency
Phase S. R/W Lines	Verify all r/t circuitry	Limited only by two main ICs shared by all r/t circuitry
Control Lines	Verify control lines	Exact IC located except for few cases
Print Error Message	Output error message to the CRT	Look-up tables provide efficient transfer of messages to CRT

Main Routine

The Main Routine controls the tester's software. With one exception, the Initialization Routine, the Main Routine calls all other modules to complete the required tasks. The calling order is (1) Control Lines Test, (2) Row Select Test, (3) Column Select Test, and (4) Phase Shifter Read and Write Lines Test. This order uses the most efficient debugging scheme for the axis box.

Other tasks of the Main Routine are startup configuration, the tester's menus, and the diagnostic iteration display. The startup procedure sends control information to initialize the tester's hardware components. To access the tester's menu, the Axis Box Test must be selected from the FASR test routines' common menu. Once the Axis Box Test is selected, the tester's menu prompts for a selection between individual tests such as the Control Lines Test or the Row Select Test, as shown by Fig. 3. After an individual test is selected, another menu, as shown in Fig. 4, provides the option for the number of times that test is performed. Any section of the axis box can be tested once or indefinitely. Testing once provides a quick check on the axis box. Testing continuously, however, assures reliability and locates transient problems. The control character, control-C, terminates the continuous loop test. After the test routine and the type of test procedure are selected, a diagnostic menu is displayed at the bottom of the screen. This menu varies depending on the test selected. If only one test is selected instead of the Continuous Loop Test, diagnostic messages will be printed informing how well the axis box is working. With continuous testing, these diagnostic messages are suppressed and more general diagnostics informing the type of test, the number of iterations and the number of errors are displayed in a menu format at the bottom of the CRT. This menu format is especially useful when all the available tests are performed on the axis box. Debugging with this menu achieves maximum efficiency, because each test routine is monitored simultaneously, as shown in Fig. 5. More advanced techniques of debugging are documented in the tester's reference manual, an informal, unpublished document available to device operators.

```
   Test Options ( v2.0 ):

(A)ll Tests << default >>
(L)Control Lines
(R)ow Select
(C)olumn Select
(O)1&04 Lines
(B)ack to Menu
       Which Option?
```

Fig. 3 - Options available for axis box test

```
          Diagnostic Options:

(C)ontinuous Loop Test << default >>
(O)ne test only
            Which Option?
```

Fig. 4 - Options for number of times test is performed

#ITERATIONS	#ERRORS for: CONTR_LINES	ROW_SELECT	COL_SEL	OUT/PHASE S. R/W
001A	0000	0000	0000	0000

Fig. 5 - Diagnostic iteration display for all axis box tests

Column Select Test/Row Select Test

Column Select and Row Select Test are much alike. On-board the axis box is a decoder that selects a particular row and column to locate a specific axis box. Fully functional select circuitry are vital for communicating to a specific axis box within the radar array. The Column and Row Select Test use iterative routines to test the select circuitry. They start at the first column/row and write signals to the axis box decoder circuitry. The tester then reads the expected signals from the output of the axis box. Subsequently, the tester determines if the proper row/column was selected. These tests are iterative because a counter is initialized to a start location and incremented after each row/column position is tested. Each row/column is tested until the counter reaches its final value, the final row/column position. Both routines test circuitry sharing common logic gates so that pinpointing the faulty device is very complicated. Therefore, faulty select circuitry compound errors and limit the tester's debugging abilities. For this limiting case, these routines will indicate which select lines have failed and what possible Integrated Circuits (ICs) are at fault.

Initialization Routine

The Initialization Routine includes all variable declarations, look-up tables and constants that initialize the tester's hardware. This routine is not a subroutine since it is referenced and not called. Basically, the routine is a dictionary defining all values of variables and constants for the other test routines. The architecture of the software was established to make variables, constants and macros global quantities from their defined routines. Thus, any routine can use their values by declaring them as globals. This approach to data management reduces extraneous declarations of variables. Also, look-up tables, which use register index pointers to locate particular diagnostic messages, minimize code and increase efficiency.

Phase Shifter Read and Write Lines Test

The phase shifters within the radar array are physical devices that affect the direction of the radar beam. The phase shifters communicate to the axis box through its receiver/transceiver (r/t) ICs. Since each axis box links 27 phase shifters, there are 27 r/t ICs for the individual phase shifter lines. These ICs can be switched between transmitting or receiving depending upon the required task. Two main ICs on-board the axis box select between transmit or receive mode. Also, buffers direct the individual phase shifter lines down a selected path.

The Phase Shifter Read and Write Lines Test is responsible for assuring that the r/t circuitry are fully operational. Since all phase shifter lines intercept the two main ICs, precise debugging cannot be achieved. If one of the main ICs is faulty, then all the phase shifter read and write lines will be flagged as errors. Also, if the main ICs are working and one r/t IC fails, the tester will indicate the faulty line, r/t IC and, unfortunately, the main ICs. The tester cannot assure the main IC's proper operation unless all r/t ICs are working. However, the suspect ICs are ordered in most probable source of the error, so the technician can replace that IC first.

Control Line Test

The Control Lines Test supervises the path of control lines passing through the axis box to other hardware portions of the radar array network. These lines are easiest to debug since many are routed through two identical ICs. Thus, the outputs appearing at both ICs should be the same. If they differ, then precise narrowing down of a faulty IC can be achieved. Usually, this test indicates the specific IC that needs replacement. There are, however, situations where more than one IC is suspect.

Print Error Message Routine

The Print Error Message Routine prints errors on a CRT. When an error is located by a test routine, certain parameters are passed to this routine to print out the diagnostic error message. The test routine passes the base address of the main table. The main table contains the relative addresses of all the error messages. Locating a specific error message requires an index pointer value relative to the base address. Therefore, the index value is also passed. Using this system (base-indexed addressing), the error diagnostic messages can be located and written to the CRT. These look-up tables are optimal for efficiency of code and speed, at least in an iterative debugging process. Some of the tester's routines have built in diagnostic messages for working or faulty aspects that are too complicated to include in an organized look-up table scheme. After the error message is written, the Print Error Message Routine returns control to the calling routine. Macros are used to print messages to the CRT.

HARDWARE

The Axis Box Tester involves interfacing with two components: the Microcomputer System's (MCS-86) System Design Kit (SDK-86) and the Axis Box. The SDK-86 is a single-board computer and contains all the test software (burned in PROMs). The SDK-86 is responsible for starting up the test program. As shown in Fig. 6, the tester receives test codes from the SDK-86 to condition the axis box. The tester then conditions the axis box. Results from the axis box are sent through the tester to SDK-86, where they are diagnosed. Finally, diagnostic information appears at the terminal. Thus the tester is a peripherally oriented design. Its main purpose is to provide an interface between the axis box and the computer controller.

SYSTEM MODEL

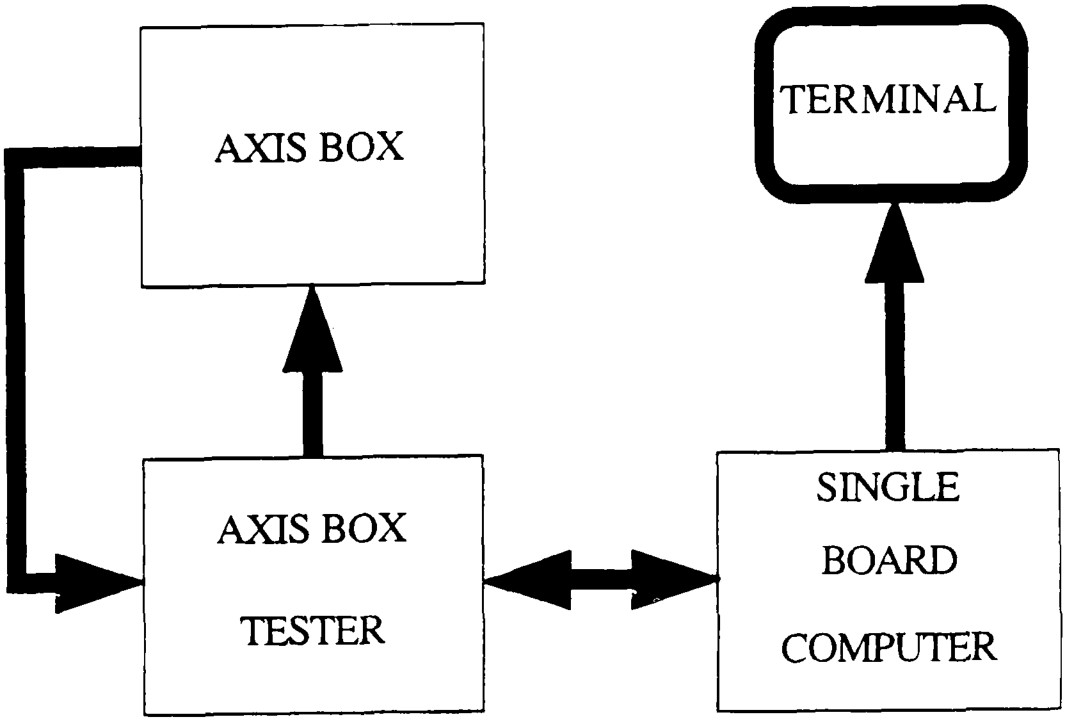


Fig. 5 - Summary of system operation: tester receives test codes from SDK-86; with these codes the tester conditions the Axis Box. Results are received and diagnosed; necessary information is displayed at terminal.

Interfacing

An information bus is needed to pass signals between boards. RS-232 cables are used because they are reliable, fast and energy efficient. There are six RS-232 cables connecting the tester and the axis box and two cables connecting the tester and the SDK-86 board.

Power Requirements/Housing

The power requirements for the SDK-86 board are a positive five volts, negative twelve volts and a ground. The tester requires a positive five volts and a ground terminal. The test bed scheme also provides more sophisticated power requirements to the axis box through a specially configured cable.

The tester is housed in the middle of a tri-connected metal chassis, which resembles a suitcase. Also sharing the middle is the Cable Tester. The top chassis contains the SDK-86 and the Phase Shifter Tester, which is mounted into a plastic cover. In the bottom chassis is a power supply that contains the necessary voltages and an adequate current load for the test equipment.

Hardware Components

The actual physical hardware of the axis box tester is comprised of two main parts: the control circuitry and the Programmable Peripheral Interface Units (PPIs-Intel's 8255 ICs). The control circuitry is basically a mirror image of the axis box. The tester has a receive network to match the axis box's transmit network. The converse is also true. Also, there are line drivers, which send control signals to the axis box. Decoders select various PPIs on the tester. The decode logic is prearranged so the proper PPIs are selected.

The heart of the tester is the PPI section. These devices enable all I/O processing between the computer controller on-board the SDK-86 and the axis box. These devices are programmable and the 24 I/O pins were configured into 3 8-bit I/O ports for the tester. Whenever a routine sends out test data, the tester's control circuitry (decoder) selects the appropriate PPI and its output port. Then the PPI sends this information to the axis box. The results from the axis box are intercepted by the tester's circuitry and routed to the appropriate PPI and its input port. Finally, these results are sent to the microprocessor board. The route between the PPIs and the tester is a bi-directional bus. The same is true for the tester and the axis box. The PPIs, latches, and receivers/transceivers are all previously assigned to hook-up to specific portions of the axis box through RS-232 cables.

LIMITATIONS/CONCLUSIONS

There are limitations with the axis box tester. The tester is subject to wear, therefore, it is always necessary to verify the tester with a working axis box before using it to debug a faulty board. Wirewraps, which provide connections for the tester, wear down after four to five years so this step is vital. Also, locating the exact problem is not always possible since several networks on the axis box share logic gates and processing ICs. The tester can only provide a list of suspects for these cases. Furthermore, in some cases the tester will attribute an error to an IC when in fact a wiring fault has developed or a IC socket has failed. These errors are inherent to the board and are independent of ICs. The ability to locate these problems is beyond the tester.

The axis box tester works well in most cases and provides reliability for a working axis box. Through the ability of exhaustive testing, boards with transient problems can be isolated, repaired and returned to the radar array. Also, the tester eliminates the time consuming process of removing the axis box from the array. The tester was designed to plug directly into an axis box hooked to the radar array. Thus, valuable time can be used diagnosing and repairing the axis box, instead of removing it and having a technician spend days isolating problems. The tester has already been used on the working radar array's axis boxes and has cut debugging time by a factor of 100.

ACKNOWLEDGMENTS

The author would like to recognize all who have contributed to the design and fabrication of the axis box tester. Considerable advice, time, assistance and humor were generously given by Jim Alter, Ron Beattie, and Tom Hively. Also, special thanks to Earl Maine and Jeff Willey who provided continuous support, advice, time, assistance and encouragement.

Special thanks are due to Jim Evins for the use of his macro print routines, and other software tools that reduced development time by several weeks. Additionally, he provided hours of help, ideas and endless patience.

REFERENCE

[1] J. M. Willey, "An Architecture to Beam Steer and Monitor A Phased Array Radar Antenna," NRL Report 8965, June 12, 1986.

GLOSSARY

buffer	An electronic device that amplifies an incoming signal.
global	A term used with software variables and constants allowing a routine outside the defining routine access to a defined resource.
IC	An integrated circuit is a compact arrangement of logic gates and electronic components performing a set function.
latches	An electronic device which keeps an incoming signal at its set value until the signal is read or until a new signal is received by the latch.
logic gates	Digital circuitry yielding results based upon set combinations of ones and zeroes.
look-up-tables	A software structure organizing information within a table that is accessed by a base and index pointer.
RS-232 cables	Industry standard cable. Ex: IBM-PC communication port uses an RS-232 cable.
PROM	Programmable Read Only Memory; this device allows a program to be burned into an IC and provides the flexibility of reprogramming the IC.
receiver/transceiver	ICs that transmit or receive data based upon the mode of operation selected for the r/t. The mode select is an on/off type switch.
select lines	The axis box select lines are the paths between the select circuitry to the output of the axis box. These lines are tied to the row and columns of the axis boxes and phase shifters.

END
DATE
FILMED
5-88
DTIC