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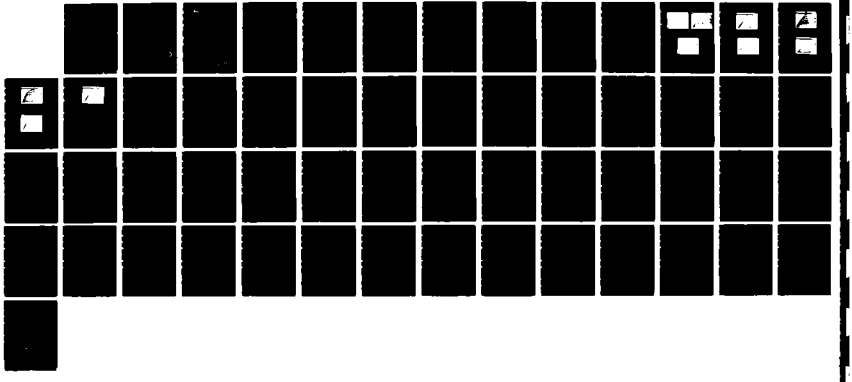

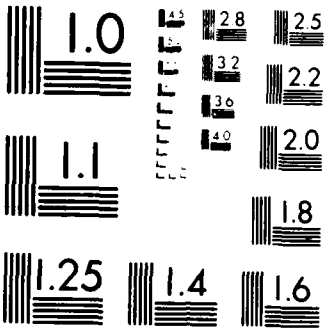
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COMPUTER AIDED DESIGN OF MONOLITHIC MICROWAVE AND MILLIMETER WAVE INTEGRATED CIRCUITS AND SUBSYSTEMS

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This interim technical report presents results of research on the computer aided design of monolithic microwave and millimeter wave integrated circuits and subsystems. A specific objective is to extend the state-of-the-art of the computer aided design (CAD) of the monolithic microwave and millimeter wave integrated circuits (MIMIC). In this reporting period, we have derived a new model for the high electron mobility transistor (HEMT). Based on a nonlinear charge control formulation which takes into consideration the variation of the 2DEG distance offset from the heterointerface as a function of bias. Pseudomorphic InGaAs/GaAs HEMT devices have been successfully fabricated at UCSD. For a lum gate length, a maximum transconductance of 320 mS/mm was obtained. In cooperation with TRW, Devices with 0.1t um and 0.25 um gate lengths have been successfully fabricated and tested. New results on the design of ultra-wideband distributed amplifiers using 0.15 um pseudomorphic InGaAs/GaAs HEMT's have also been obtained. In addition, two-dimensional models of the submicron MESFET's, HEMT's and HBT's are currently being develped for the CRAY X-MP/48 supercomputer

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ABSTRACT

This interim technical report presents results of research on the computer aided design of monolithic microwave and millimeter wave integrated circuits and subsystems. A specific objective is to extend the state-of-the-art of the computer aided design (CAD) of the monolithic microwave and millimeter wave integrated circuits (MIMIC). In this reporting period, we have derived a new model for the high electron mobility transistor (HEMT) based on a nonlinear charge control formulation which takes into consideration the variation of the 2DEG distance offset from the heterointerface as a function of bias. Pseudomorphic *InGaAs/GaAs* HEMT devices have been successfully fabricated at UCSD. For a 1 μm gate length, a maximum transconductance of 320 mS/mm was obtained. In cooperation with TRW, devices with 0.15 μm and 0.25 μm gate lengths have been successfully fabricated and tested. New results on the design of ultra-wideband distributed amplifiers using 0.15 μm pseudomorphic *InGaAs/GaAs* HEMT's have also been obtained. In addition, two-dimensional models of the submicron MESFET's, HEMT's and HBT's are currently being developed for the CRAY X-MP/48 supercomputer. Preliminary results obtained are also presented in this report.

1. Fabrication of HEMT Devices

1.1 Introduction

High electron mobility transistors (HEMT) have shown great potential for high speed and high frequency applications. Much progress has been made in the AlGaAs/GaAs HEMTs where the larger band gap highly doped AlGaAs supplies electrons to the two dimensional electron gas (2DEG) in the smaller band gap undoped GaAs. Recently, there has been increasing interest in pseudomorphic InGaAs/GaAs HEMTs[1,2,3] because of the higher mobility of InGaAs over GaAs and the elimination of the persistent photoconductivity problem associated with the AlGaAs.

Pseudomorphic InGaAs/GaAs HEMT devices with a gate length of 2 microns and transconductance of 120 mS/mm have been fabricated at UCSD. Using the fabrication facilities and process at TRW, a one micron gate length InGaAs/GaAs HEMT with a maximum transconductance of 320 mS/mm was successfully made. These results are comparable to those found in a 1 micron pseudomorphic InGaAs/AlGaAs HEMT. [4] These HEMTs have exhibited a transconductance of 540 mS/mm in a 0.1 micron device [5].

Material

The material system for these HEMT devices is pseudomorphic $In_{.15}Ga_{.85}As$/GaAs on GaAs substrate, grown by molecular beam epitaxy at UCSD. The advantages of this material over the conventional AlGaAs/GaAs is the higher electron mobility and peak electron velocity in the InGaAs and the avoidance of problems associated with the deep donor - vacancy complexes known as DX centers in the AlGaAs. These cause the threshold voltage to be dependent on temperature and illumination and also lead to a persistent photoconductivity at low temperatures. The lattice mis-match between the GaAs and InGaAs would normally create dislocations at the interface but by making the InGaAs layer thin, the mis-match can be taken up by elastic strain. Figures 1 and 2 show the material structures of the HEMTs reported here.

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[1] T.E. Zipperian, L.R. Dawson, C.G. Osburn, and I.J. Fritz, *IEDM Technical Digest*, 1983, pp. 696-698

[2] J.J. Rosenberg, N. Benlamri, P.D. Kirchner, J.M. Woodall, and G.D. Pettit, *IEEE Electron Device Letters*, EDL-6, pp. 491-493, 1985.

[3] T.E. Zipperian and T.J. Drummond, Electronic Letters, vol 21, pp. 823-824, 1985.

[4] A. Ketterson, et al., *IEEE Electron Device Letters*, EDL-6, no. 12, pp. 628-630, 1985.

[5] P.C. Chao, et al., *IEEE Electron Device Letters*, EDL-8, no. 10, pp. 489-491, 1987.

500 Å n^+ GaAs 2 × 10^{18} cm^{-3}
125 Åundoped GaAs spacer
200 Å $In_{.15}Ga_{.85}As$
2500 Åundoped GaAs buffer
Semi-insulating GaAs substrate

UCSD #348

Figure 1

300 Å n^+ GaAs 4 × 10^{18} cm^{-3}
200 Å n^+ GaAs 2 × 10^{18} cm^{-3}
25 Åundoped GaAs spacer
300 Å $In_{.15}Ga_{.85}As$
5000 Åundoped GaAs buffer
Semi-insulating GaAs substrate

UCSD #462

Figure 2

Device Fabrication

The HEMTs fabricated were split source devices with various gate lengths and widths. A new mask set was made for 2 micron discrete field effect transistors. It was determined that 2 micron geometries was the minimum dimension that could be reliably fabricated with the current HTG aligners at UCSD. The devices would serve as an initial step in the development toward smaller dimension devices and be useful as prototype devices for investigating various material systems. The total gate width was 300 microns and the source to drain spacing was 6 microns, allowing a 2 micron alignment tolerance in the mask set. The overall dimensions are shown in Figure 3a. In addition, a few 1 micron, 2.5 micron and 3 micron gate length devices with source to drain spacings of 5 micron, 7.5 micron and 9 microns, respectively, were included as test structures. The 1 micron gate length device mask set given us by TRW and shown in Figure 3b and 3c, has two split source devices with source to drain spacing of 3 microns and gate widths of 300 and 100 microns, respectively.

The HEMT fabrication process at UCSD consists of three sections, which are mesa isolation, ohmic contact and gate. The mesa isolation is accomplished by a wet etch consisting of phosphoric acid, hydrogen peroxide and water in a 1:1:25 mixture. For the ohmic contacts a AuGe alloy with a thin Ni cap layer is used. Furnace annealing is performed at 450°C. Much effort has been focused on the gate process, which is the most critical portion of the fabrication. The gate lithography involves fine geometries and alignment and the gate recess controls the threshold voltage. Thermally evaporated aluminum is the gate metal. An outline of the UCSD process is attached. The intention was to establish a consistent 2 micron gate process followed by work on a 1 micron gate process at UCSD. Toward this goal, there have been beneficial opportunities to visit and use TRW facilities in Redondo Beach, California.

A two micron photolithography process was developed for the new devices. An HTG aligner with mid - UV (300-320 nm) wavelength source was used. It became apparent that contact between the wafer and the mask is the most critical factor to achieving uniform, consistent and accurate resolution of the mask features. The best results come with use of vacuum contact, a chuck designed for the appropriate sample size, and a flat sample backside. As a result,

the backside of the sample needed to be cleaned and lapped to remove the In residue left after MBE growth. Difficulties arise with small piece samples because good contact is harder to achieve. Among the principle causes are mask bow and non-uniform resist thickness. Mask bow can be reduced with a mask holder and chuck designed for small pieces.

The alignment tools and microscope optics on the HTG are inadequate for alignment within 1 micron. Consistent resolution of 1 micron spaces has been difficult. The Karl Suss mask aligner is designed for use in the 1 micron and submicron range, and is more widely accepted and commonly used. The fabrication facility at TRW has Karl Suss aligners and these were used for the 1 micron InGaAs/GaAs HEMT devices fabricated there.

The gate recess etch is the most critical step in the processing of HEMT devices. It is necessary for the removal of the conduction path in the highly doped top layer and to adjust the threshold voltage. As a result, there was much development for this part of the process. A method was needed to determine the endpoint of the etch. This was accomplished by monitoring the saturation current between the source and drain by making contact to the ohmic pads through the resist. The sample would be etched for a certain time and measured until a pre-determined endpoint saturation current was reached. Two GaAs MESFETs and a InGaAs/GaAs HEMT with five micron gate lengths were fabricated as trial runs for using this technique. The results of these devices are seen in Figures 4,5, and 6. The gate recess allows the pinchoff in the depletion mode MESFET and the fabrication of enhancement mode devices. The depth of the gate recess may only be a couple of hundred angstroms so a very slow etch is necessary.

As a result, the next issued addressed was to improve the wet chemical etch system. An etch of phosphoric acid, hydrogen peroxide and water in a 1:1:25 ratio had been used. However, the etch rate of 30–40Å/sec was to fast for a shallow gate recess and resulted in a lack of control and uniformity. The citric acid etch system was investigated by Otsubo[6] and found to be an excellent stow and linear etch of GaAs. A mixture of 50% aqueous citric acid with hydrogen peroxide in a 40:1 ratio proved to have an constant etch rate of 10Å sec. This new etch provided more stability and by increasing the etch time improved the control of the gate recess depth.

Visits to TRW this summer and the opportunity to work in a well equipped facility with an established process was very helpful. Fabrication of InGaAs/GaAs HEMT's at TRW serve as a benchmark for improvements of the process at UCSD and help qualify portions of the process as well as identify problem or critical areas. The 2 micron HEMT devices, #348 A and #462C shown in Figures 7 and 8 had the gate portion of the process done at TRW using the resist and resist process from UCSD. The results indicated that the mesa isolation and the ohmic contact process as well as the gate resist process are adequate to successfully fabricate 2 micron devices at UCSD. The complete fabrication process was then done at UCSD resulting in working devices on #348C and #462D. However, as seen in Figures 9 and 10, the performance of these devices were not as good as those finished at TRW, indicating some improvement is needed, particularly in the gate metallizations.

Sample #462E and #348D were fabricated with the TRW ohmic and gate process. The results from the 2 micron devices on #462E were compared to devices either partially or

[6] M. Otsubo, T. Oda, H. Kumabe, and H. Miki, *J. Electrochemical Soc.* 124, 155 (1977).

completely fabricated at UCSD. The performance of these devices on #462E and the 1 micron devices on #348D serve as a target for future devices.

Results and Discussion

The best results for the pseudomorphic InGaAs/GaAs HEMTs are from the 1 micron devices on sample #348D. A short gate device (Figure 11) (gate width of 100 microns) exhibits a transconductance of 320 mS/mm, while the best value for the long gate device Figure 12 (gate width of 300 microns) is 225mS/mm. The I-V curves shown in Figures 11 and 12 show both positive and negative gate voltages with the peak transconductance occurring with positive gate voltage. They also show good saturation and pinch-off characteristics as well as good current values. These results are comparable to the 1 micron InGaAs/AlGaAs pseudomorphic HEMT by Ketterson et. al.[4] which had a transconductance of 270 mS/mm. The potential of the device is shown here and further improvements to the process should increase its performance. High frequency measurements will be made on these devices.

For the 2 micron devices, the highest transconductance, 183mS/mm for a 300 micron wide gate, was from sample #462E which was fabricated with the TRW process (Figure 13). As a comparison, #462C (Figure 8) and #348A, (Figure 7) which only had gate recess and metallization done at TRW, have transconductance of 135 mS/mm and 175 mS/mm. It was found that the ohmic contact resistance for #462E is half of that for #462C. Devices from the same material but completely fabricated at UCSD, #462D (Figure 10) and #348C (Figure 9), have transconductances of 80mS/mm and 120mS/mm. With some further development of the gate recess and metallization the performance of the devices fabricated at UCSD will improve and a 2 micron process will be finalized. This gives us the capability of initial evaluation of different material systems and with a few improvements to the processing equipment, allow us to establish a 1 micron process at UCSD.

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[4] A. Ketterson, et al., *IEEE Electron Device Letters*, EDL-6, no. 12, pp. 628-630, 1985.

1. APPENDIX A

UCSD

Mesa Isolation

Lithography

Solvent clean

Prebake (105 C. 20 min)

Hunt HPR 1182 photoresist

Spin (5000 rpm, 20 seconds)

Softbake (105 C. 30 min)

Exposure HTG aligner (~40mJ/cm^2)

Develop (1 min, no agitation)

Hardbake (110 C. 30 min)

Etch (45 sec, H_3PO_4:H_2O_2:H_2O, ratio1 :1:25)

Resist strip in acetone

Ohmic Contact

Lithography

(same as above)

Metal Evaporation

AuGe:Ni (1000Å, thermal evaporation

Liftoff, in acetone

Alloy

450° C, 30 sec in formine gas using

furnace with graphite boat

Gate

Lithography

(Same as above)

Recess etch

Preclean (NH_4OH:H_2O,ratio1:15)

Etch (citric acid : H_2O_2:H_2O, ratio 20:1:20)

Measure source to drain current

Metal evaporation

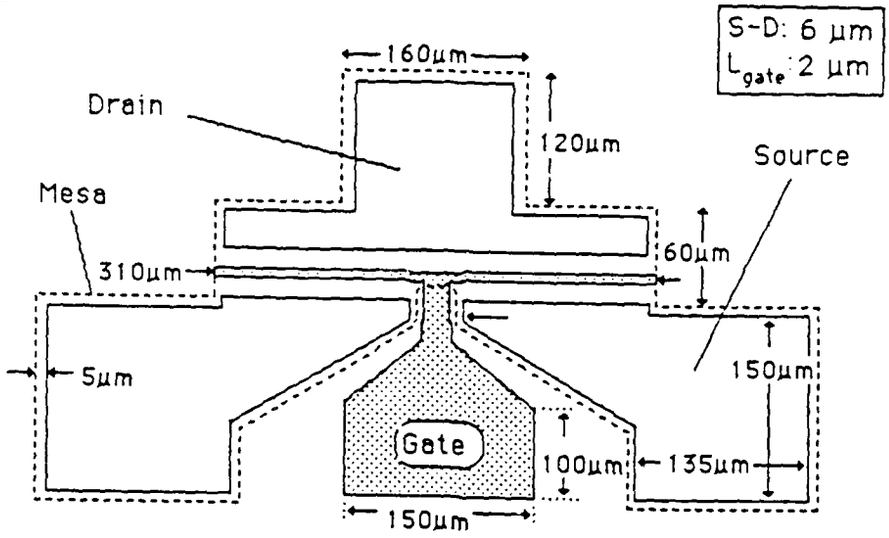
Preclean (NH_4OH:H_2O, ratio 1:15)

Al (1000Å thermal evaporation

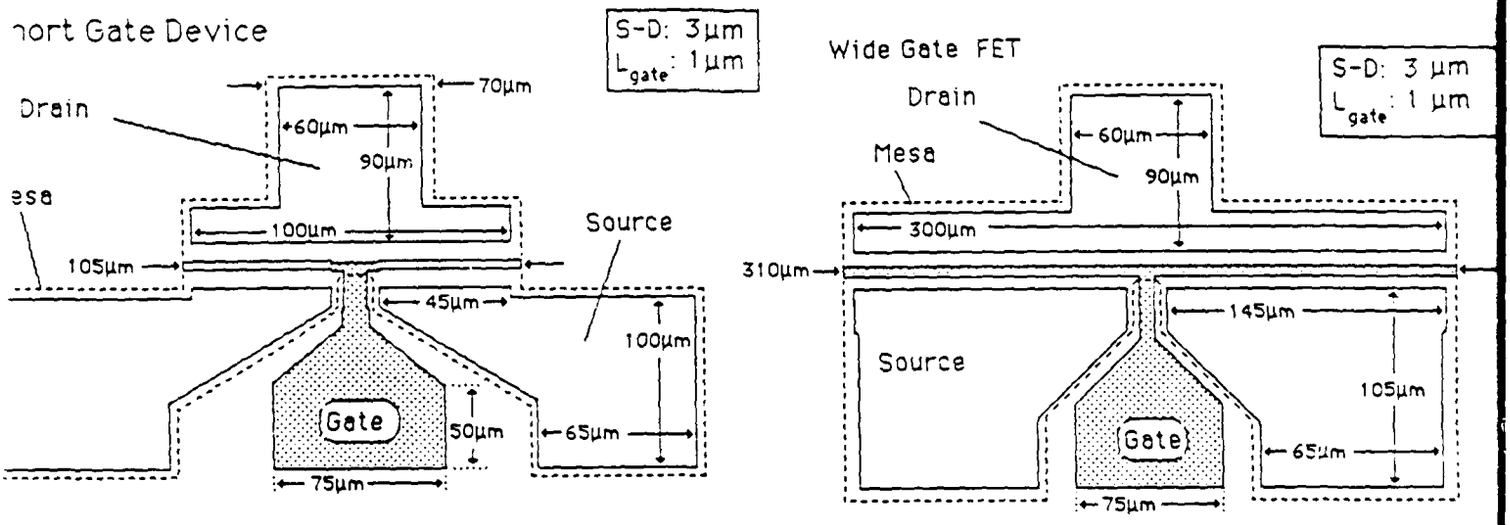
Liftoff in acetone

2. APPENDIX B

Figures



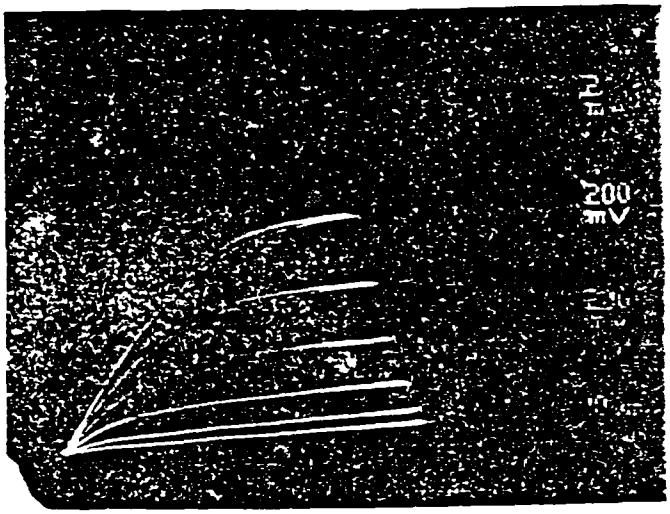
a) Schematic of the UCSD 2 µm gate FET



b) c)

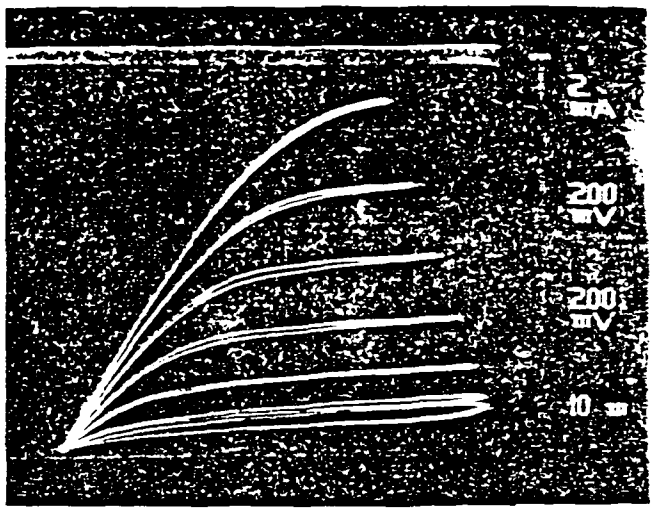
b), c) Schematic of the two devices on the 1µm gate FET mask set.

Figure 3



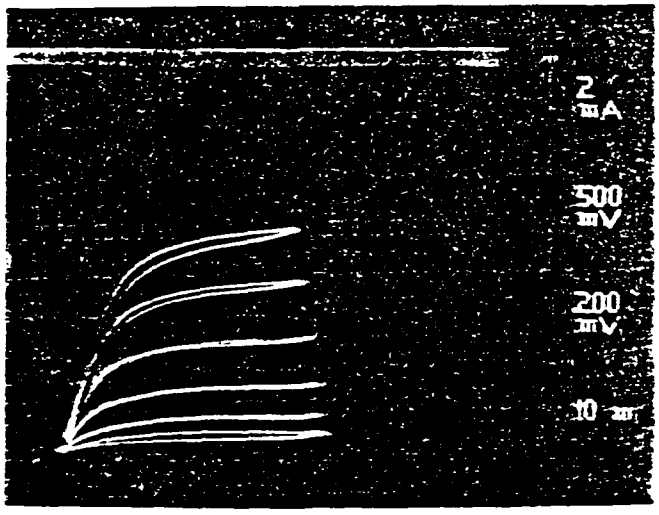
Enhancement mode GaAs MESFET A

Figure 4



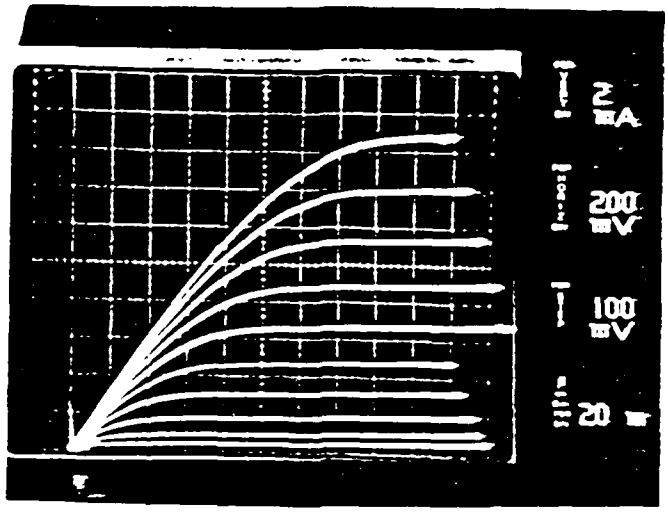
Depletion mode GaAs MESFET B

Figure 5



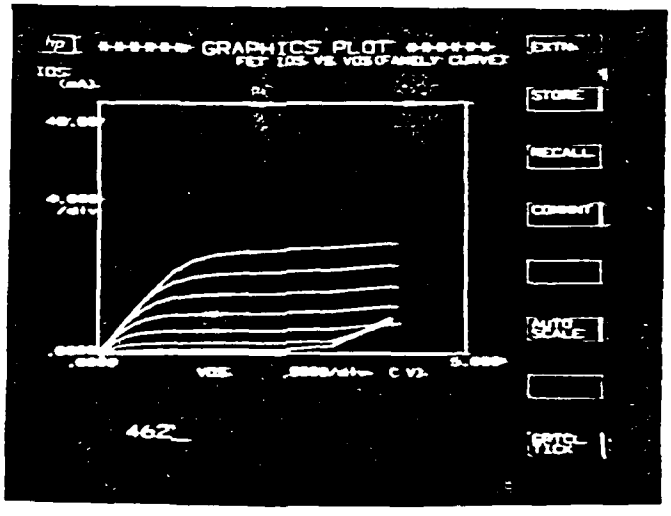
5 um gate enhancement mode InGaAs/GaAs HEMT

Figure 6



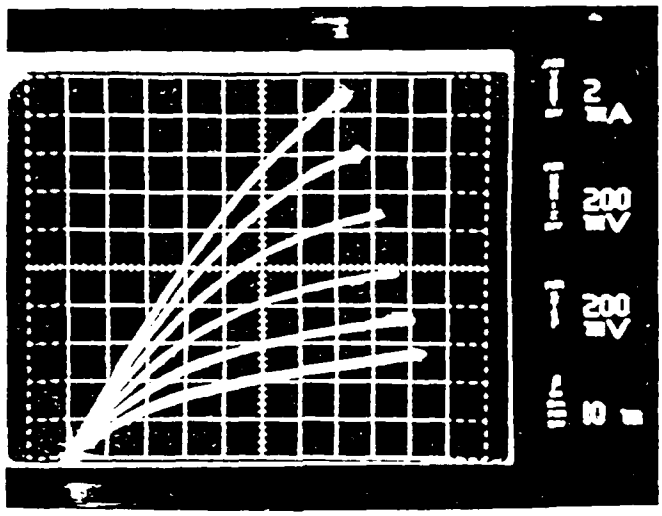
UCSD 348A InGaAs/GaAs 2μm HEMT with g_m = 175mS/mm

Figure 7

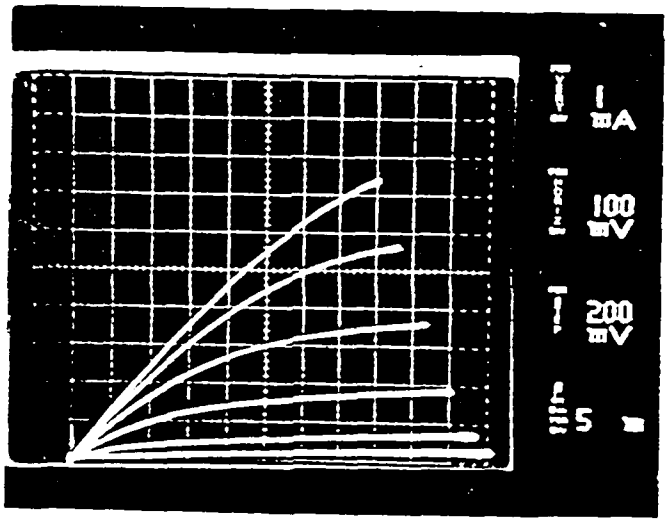


UCSD 462C InGaAs/GaAs 2μm HEMT with g_m =135 mS/mm

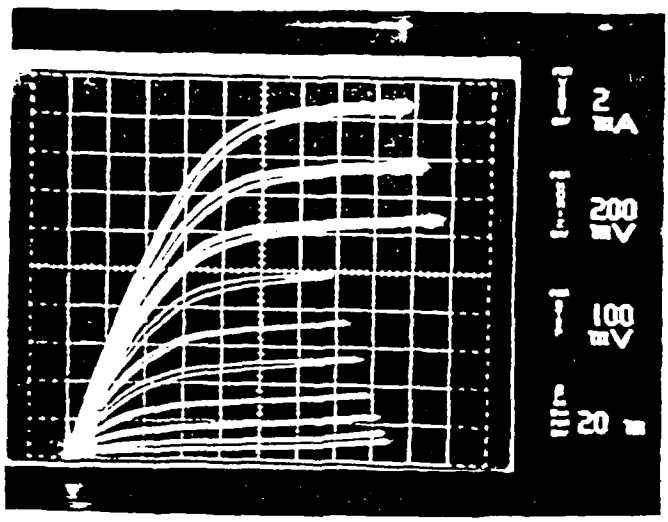
Figure 8



UCSD 348C InGaAs/GaAs HEMT with g_m = 120mS/mm
Figure 9



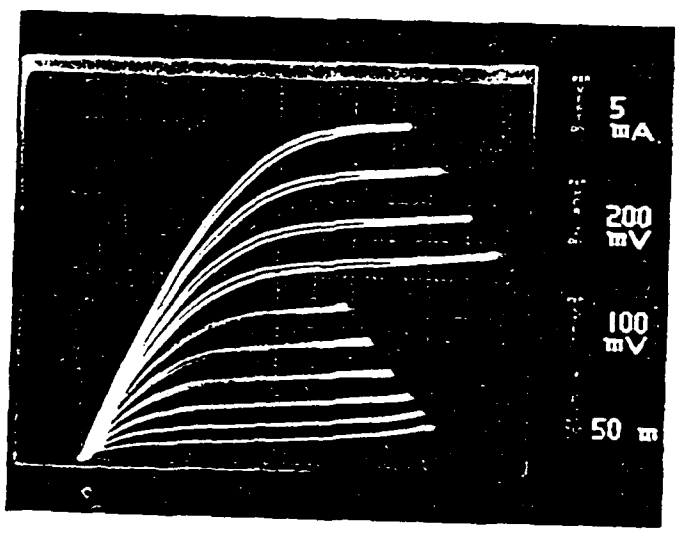
UCSD 462D InGaAs/GaAs HEMT with g_m = 80mS/mm
Figure 10



UCSD 348D InGaAs/GaAs 1μm HEMT (gate width = 100 μm)

g_m = 320mS/mm

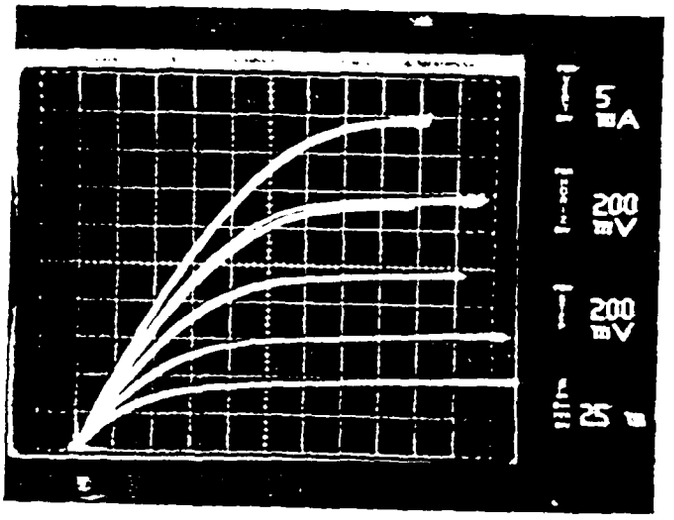
Figure 11



UCSD 348D InGaAs/GaAs 1μm HEMT (gate width = 300 μm)

g_m = 225mS/mm

Figure 12



UCSD 462E InGaAs/GaAs 2μm HEMT with g_m = 183mS/mm

Figure 13

2. Design of Distributed Amplifiers Using 0.15 μm Pseudomorphic *InGaAs/GaAs* HEMT's

2.1 Introduction:

Distributed amplifiers using 0.15 μm pseudomorphic *InGaAs/GaAs* HEMT's for 60 GHz and possibly 94 GHz frequency bands are being designed at UCSD. The potential of distributed amplification for obtaining gain over wide frequency bands has long been recognized.[1,2] Broadband distributed amplifiers using discrete *GaAs* MESFET's have been demonstrated at microwave frequencies.[3, 4,5,6,7] Better performance is expected with the use of HEMT due to its superior high frequency characteristics over MESFETs. The principle behind distributed amplifiers was based on the idea to separate the input capacitance of the active devices by means of artificial transmission lines, while adding their transconductances. As a result, it is possible to achieve extremely wide bandwidths up to very high frequencies with effectively very wide gates. The latter obviously has a beneficial impact on the amplifier's power handling capabilities.

For the distributed amplifier design, we will first develop the D.C. model and small signal equivalent circuit for HEMT. These will be initial steps toward developing a systematic approach to the circuit design of distributed amplifier. In the following sections, the small signal equivalent circuit will be discussed, and be applied to some distributed amplifier design.

3. Small Signal Equivalent Circuit

There are several sets of S-parameters measured on a 0.15μm pseudomorphic HEMT by TRW. One set labeled as HEMT C2 is listed in Table 1. Its frequency performance MAG/MSG, MUG, S_{21}, K vs. frequency are plotted in Fig. 1, and f_{max} can be projected to higher than 80 GHz. The current gain h_{21} vs. frequency is plotted in Fig. 2 and f_T is projected to 70 GHz.

---

1 E.L. Ginzton, W.R. Hewlett, J.H. Jasburg, and J.D. Noe, "Distributed Amplification," in *Proc. IRE*, Vol.. 36, pp. 956-969, 1948.

2 D.V. Payne, "Distributed Amplifier Theory," *Proc. IRE*, vol. 41, pp. 759-762, 1953.

3 W. Jutzi, "A MESFET Distributed Amplifier with 2 GHz Bandwidth," *Proc. IEEE*, vol. 57, pp. 1195-1196, 1969.

4 Y. Ayasli, R.L. Mozzi, J.L. Vorhaus, L.D. Reynolds, and R.A. Pucel, "A Monolithic GaAs 1-13 GHz Traveling-Wave Amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 976-981, 1982.

5 Y. Ayasli, L.D. Reynolds, J.L. Vorhaus and L. Hanes, "Monolithic 2 ~ 20 GHz traveling wave amplifier," *Electron. Lett.*, Vol. 18, No. 14, pp. 596-598, 1982.

6 Karl B. Niclas, Walter T. Wilser, Thomas R. Kritzer and Ramon R. Pereira, "On theory and performance of solid state Microwave Distributed Amplifiers," *IEEE Trans. Microwave Theory Tech.*, Vol. MTT-31, pp. 447-456, 1983.

7 James B. Beyer, S.N. Prasad, Robert C. Becker, James E. Nordman and Gert K. Houenwarter, "MESFET Distributed Amplifier Design Guidelines," *IEEE MTT-32*, pp. 268-275, 1984.

The small signal equivalent circuit of the active device is necessary to predict performance outside the measured frequency band. The circuit derived from the measured date includes many parameters, such as the parasitics associated with the fabrication process. Therefore, it is important to derive an exact equivalent circuit. The parasitic parameter resulting from measurement should be de-embedded out of the small signal equivalent circuit. This de-embedded model is used in the monolithic amplifier circuit design.

A small signal equivalent circuit proposed by Dr. Ahlgren is shown in Fig. 3(a) to fit the measured data listed in Table 1, and the deembedded model is shown in Fig. 3(b). An amplifier with lumped elements was designed and is shown in Fig. 3(c), and its performance is shown in Fig. 4.

Although the fit between the model and the measured data is very good, a more conventional model is derived based on the physical structure of the device and from the point of view of statistics.[8] In addition, the parasitic resistance R_g, R_s, and R_d can be obtained from dc measurements as detailed by Fukui.[9] A resulting small signal equivalent circuit is shown in Fig. 5.(a), and the de-embedded model is shown in Fig. 5.(b).

4. Verification of the Potential of Distributed Amplifier

The performance of distributed amplifier is examined to determine whether its potential warrants the development of a systematic approach for design. The de-embedded model derived by Ahlgren is shown in Fig. 3(b), and its performance is shown in Fig. 6. Transmission line sections, whose characteristic impedances are all 50 ohms, were introduced between gate ends and between drain ends of this de-embedded model to form a distributed amplifier, which is shown in Fig. 7. Its performance within the frequency band 0-30 GHz is shown in Fig. 8. Comparing the curves in Fig. 6 and Fig. 8, it is clear that the gain flatness is improved, and the return losses of input and output are much smaller.

An attempt was made to improve the performance of distributed amplifier by using tapered transmission lines.[10] These transmission line sections have different characteristic impedances from one another with linearly or exponentially tapered relations. The circuit topology is shown in Fig. 9, and its performance is shown in Fig. 10. It is clear that gain is 8.5 ± 0.5 dB, and return losses are below -10 dB.

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8 Rimantas L. Vaitkus, "Uncertainty in the Values of GaAs MESFET Equivalent Circuit Elements Extracted from Measured Two-port Scattering parameters," *Cornell Conference on High Speed Semiconductor Devices and Circuits*, pp. 301-308, 1983.

9 H. Fukui, "Determination of the Basic Device Parameters of a GaAs MESFET", *The Bell System Technical Journal* Vol. 58, pp. 771-797, 1979.

10 Walter H. Ku and J.Q. He, "Analysis and Design of Monolithic Distributed GaAs MESFET Amplifiers," *Cornell Conference on High Speed Semiconductor Devices and Circuits*, pp. 80-92, 1983.

Similarly, using the de-embedded model shown in Fig. 5(b), we designed another distributed amplifier with tapered transmission line, which is shown is Fig. 11, and its performance is shown in Fig. 12.

5. Systematic Design approach to be Developed

Knowing that the distributed amplifier has potential to increase the gain-bandwidth product, systematic study should commence to achieve a practical design guideline for distributed amplifiers. These guidelines will be established from examining the first order performance of distributed amplifier designs using the conventional simplified model rather than the de-embedded model. Then the small signal equivalent circuit and de-embedded model should be re-evaluated by comparison with the measured S-parameters and dc measurements.[8,9] This de-embedded model would be used to optimize the circuit design when running the Touchstone program.

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8 Rimantas L. Vaitkus, "Uncertainty in the Values of GaAs MESFET Equivalent Circuit Elements Extracted from Measured Two-port Scattering parameters," *Cornell Conference on High Speed Semiconductor Devices and Circuits*, pp. 301-308, 1983.

9 H. Fukui, "Determination of the Basic Device Parameters of a GaAs MESFET", *The Bell System Technical Journal*m Vol. 58, pp. 771-797, 1979.

6. References:

1. E.L. Ginzton, W.R. Hewlett, J.H. Jasburg and J.D. Noe, "Distributed amplification," in *Proc. IRE*, Vol. 36, pp. 956-969, 1948.
2. D.V. Payne, "Distributed amplifier theory," *Proc. IRE*, Vol. 41, pp. 759-762, 1953
3. W. Jutzi, "A MESFET distributed amplifier with 2 GHz bandwidth," *Proc. IEEE*, Vol. 57, pp. 1195-1196, 1969.
4. Y. Ayasli, R.L. Mozzi, J.L. Vorhaus, L.D. Reynold and R.A. Pucel, "A monolithic GaAs 1-13 GHz traveling-wave amplifier," *IEEE Trans. Microwave Theory Tech.*, Vol. MTT-30, pp. 976-981, 1982.
5. Y. Ayasli, L.D. Reynolds, J.L. Vorhaus and L. Hane, "Monolithic 2 - 20 GHz traveling wave amplifier," *Electron. Lett.*, Vol. 18, No. 14, pp. 596-598, 1983.
6. Karl B. Niclas, Walter T. Wilser, Thomas R. Kritzer and Ramon R. Pereira, "On theory and performance of solid state Microwave Distributed Amplifiers," *IEEE Trans. Microwave Theory Tech.*, Vol. MTT-31, pp. 447-456, 1983.
7. James B. Beyer, S.N. Prasad, Robert C. Becker, James E. Nordman and Gert K. Houenwarter, "MESFET Distributed Amplifier Design Guidelines," *IEEE MITT-32*, pp. 268-275, 1984.
8. Rimantas L. Vaitkus, "Uncertainty in the Values of GaAs MESFET Equivalent Circuit Elements Extracted from Measured Two-port Scattering parameters," *Cornell Conference on High Speed Semiconductor Devices and Circuits*, pp. 301-308, 1983.
9. H. Fukui, "Determination of the Basic Device Parameters of a GaAs MESFET", *The Bell System Technical Journal*m Vol. 58, pp. 771-797, 1979.
10. Walter H. Ku and J.Q. He, "Analysis and Design of Monolithic Distributed GaAs MESFET Amplifiers," *Cornell Conference on High Speed Semiconductor Devices and Circuits*, pp. 80-92, 1983.

7. Tables

TEM MILLIMETER & MICROWAVE TECHNOLOGY CENTER
WAFER: 404-1 DEV TYPE: UCSD 17:31:15 24-JUN-87
15 C-3 80 um.
Vds = 2.000 V Idss= 26.065mA Gm = 28.600mS Vth =-996.875mV
Idsoff= 706.850uA Idsp= 24.085mA Gmp= 35.700mS Vgsp= -75.000mV

Freq	S11		S21		S12		S22		S21
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang	dB
1.00	0.997	-2.8	2.670	176.1	0.003	84.1	0.719	-1.7	8.53
2.02	0.994	-5.6	2.668	172.5	0.007	83.2	0.719	-3.2	8.59
3.04	0.991	-8.5	2.684	168.7	0.010	81.7	0.718	-4.6	8.58
4.06	0.984	-11.4	2.658	164.9	0.014	76.5	0.716	-6.1	8.49
5.08	0.976	-14.0	2.644	161.6	0.016	74.4	0.714	-7.4	8.44
6.10	0.970	-16.8	2.647	157.9	0.020	74.9	0.715	-9.0	8.45
7.12	0.957	-19.6	2.598	153.9	0.024	69.2	0.709	-10.4	8.29
8.14	0.946	-22.1	2.561	151.1	0.027	66.4	0.707	-11.7	8.17
9.16	0.935	-24.7	2.565	147.9	0.030	65.3	0.705	-13.1	8.18
10.18	0.930	-27.3	2.530	143.7	0.033	61.1	0.701	-14.4	8.06
11.20	0.906	-29.7	2.462	140.6	0.036	58.5	0.697	-15.7	7.82
12.22	0.892	-32.1	2.438	138.1	0.039	56.5	0.694	-16.9	7.74
13.24	0.877	-34.5	2.416	134.2	0.043	53.0	0.691	-18.2	7.66
14.26	0.861	-36.6	2.341	130.9	0.043	49.8	0.686	-19.4	7.39
15.28	0.846	-38.8	2.290	128.3	0.047	48.7	0.683	-20.4	7.20
16.30	0.831	-40.9	2.290	125.9	0.048	45.6	0.680	-21.7	7.20
17.32	0.814	-42.9	2.223	121.5	0.051	42.8	0.675	-22.6	6.94
18.34	0.799	-44.7	2.142	120.1	0.051	41.1	0.672	-23.4	6.61
19.36	0.784	-46.6	2.142	118.0	0.055	39.1	0.669	-24.4	6.62
20.38	0.768	-48.3	2.117	114.0	0.055	36.5	0.665	-25.1	6.52
21.40	0.755	-49.9	2.021	111.6	0.056	34.1	0.665	-25.9	6.11
22.42	0.744	-51.4	1.986	110.9	0.057	35.1	0.665	-26.5	5.96
23.44	0.734	-53.1	2.039	107.5	0.061	31.3	0.667	-27.4	6.15
24.46	0.720	-54.9	1.924	103.1	0.060	32.5	0.667	-28.4	5.69
25.48	0.707	-56.4	1.884	103.2	0.064	29.1	0.667	-29.6	5.50
26.50	0.698	-57.9	1.938	100.0	0.065	29.2	0.666	-30.5	5.75

Table 1

TRW MILLIMETER & MICROWAVE TECHNOLOGY CENTER
WAFER: 404 1 DEV TYPE: UGSD 17:31:15 24-JUN-87
15 0.2 80 nm.
Vds = 2.000 V Idss= 26.065mA Gm = 28.600mS VTh =-996.175mV
Idsoff= 706.850uA Idsp= 24.085mA Gmp= 35.700mS VRsp= -75.000mV

Freq GHz	K	SIGN H1	MAX GAIN AVAILABLE dB	MAX GAIN STABLE dB	MAX GAIN UNILATERAL dB	H21
1.00	0.240	+		29.03	33.75	71.22
2.02	0.229	+		25.89	31.09	35.87
3.04	0.261	+		24.19	29.00	23.78
4.06	0.368	+		22.84	26.53	17.57
5.08	0.438	+		22.05	24.82	14.21
6.10	0.437	+		21.21	23.84	11.91
7.12	0.559	+		20.32	22.11	10.08
8.14	0.635	+		19.83	20.94	8.81
9.16	0.665	+		19.30	20.15	7.96
10.18	0.762	+		18.81	19.15	7.13
11.20	0.831	+		18.33	18.19	6.40
12.22	0.885	+		18.00	17.49	5.91
13.24	0.941	+		17.53	16.85	5.48
14.26	1.058	+	15.91		16.02	5.00
15.28	1.087	+	15.13		15.39	4.67
16.30	1.142	+	14.48		14.98	4.45
17.32	1.224	+	13.56		14.30	4.13
18.34	1.306	+	12.88		13.64	3.84
19.36	1.321	+	12.55		13.33	3.73
20.38	1.411	+	12.06		12.93	3.56
21.40	1.488	+	11.42		12.31	3.30
22.42	1.514	+	11.20		12.00	3.18
23.44	1.474	+	11.14		12.05	3.14
24.46	1.596	+	10.55		11.41	2.90
25.48	1.581	+	10.21		11.07	2.79
26.50	1.564	+	10.33		11.19	2.82

Table 1 (cont'd)

8. Figures

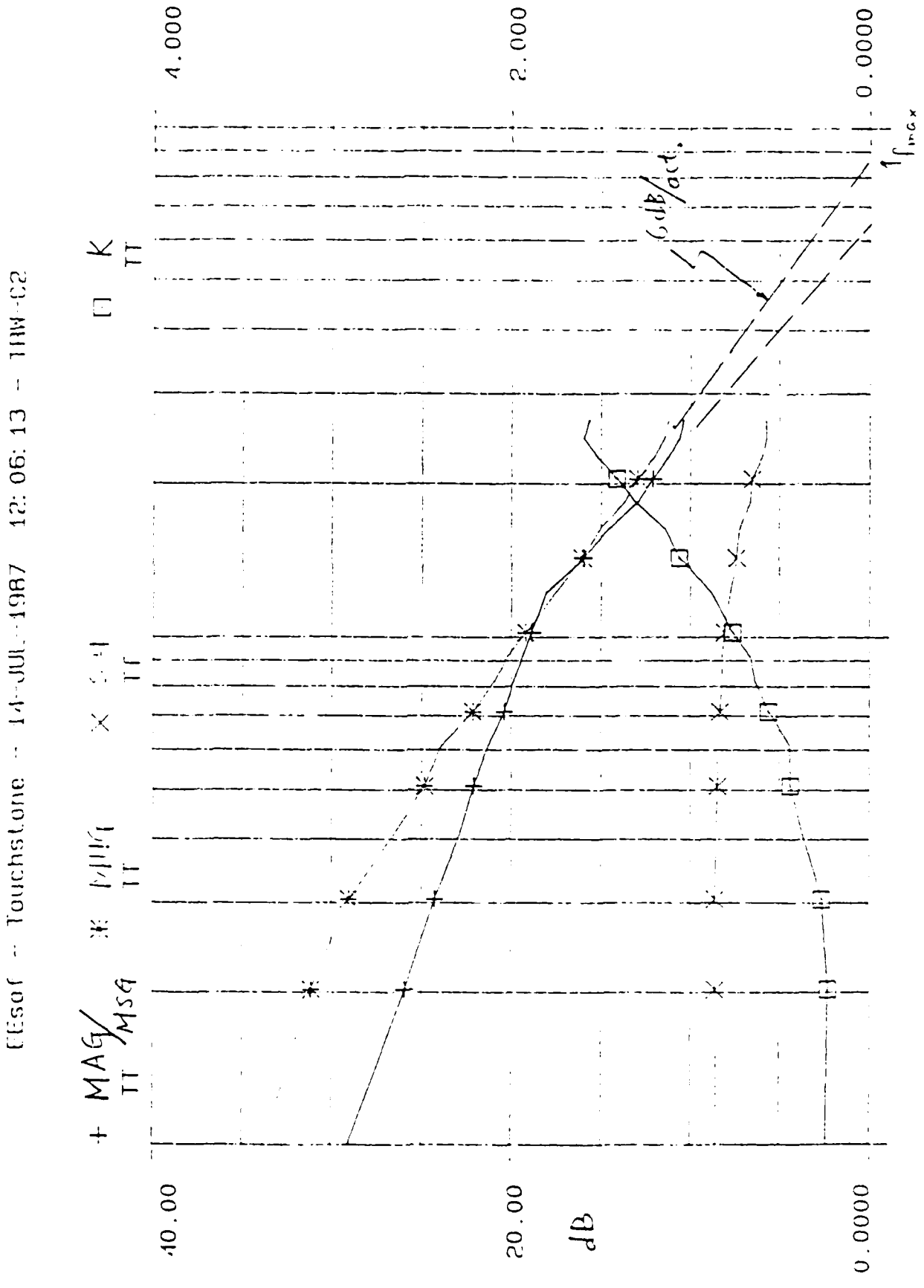
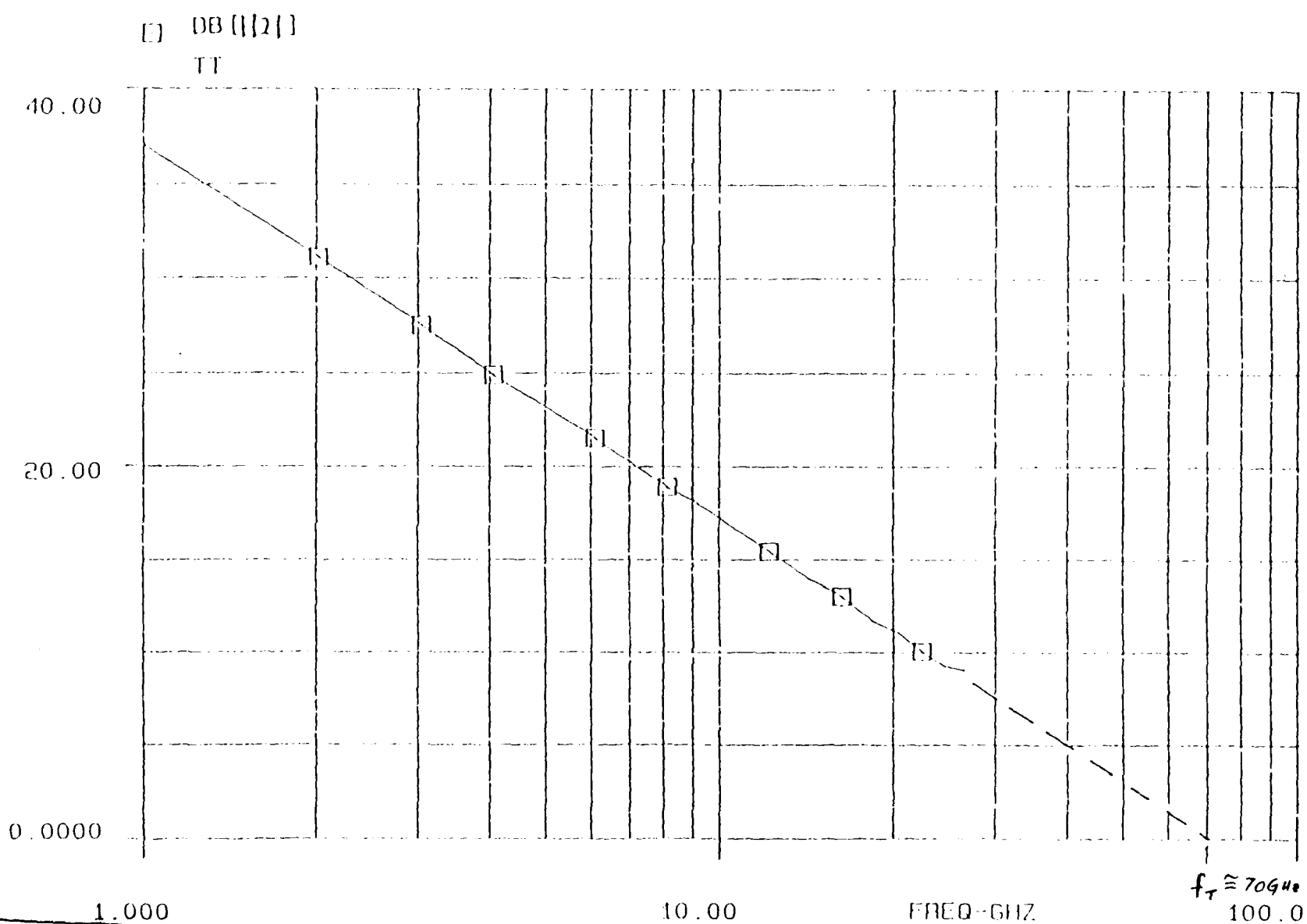


Fig. 1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[] DB[|2|]
TT
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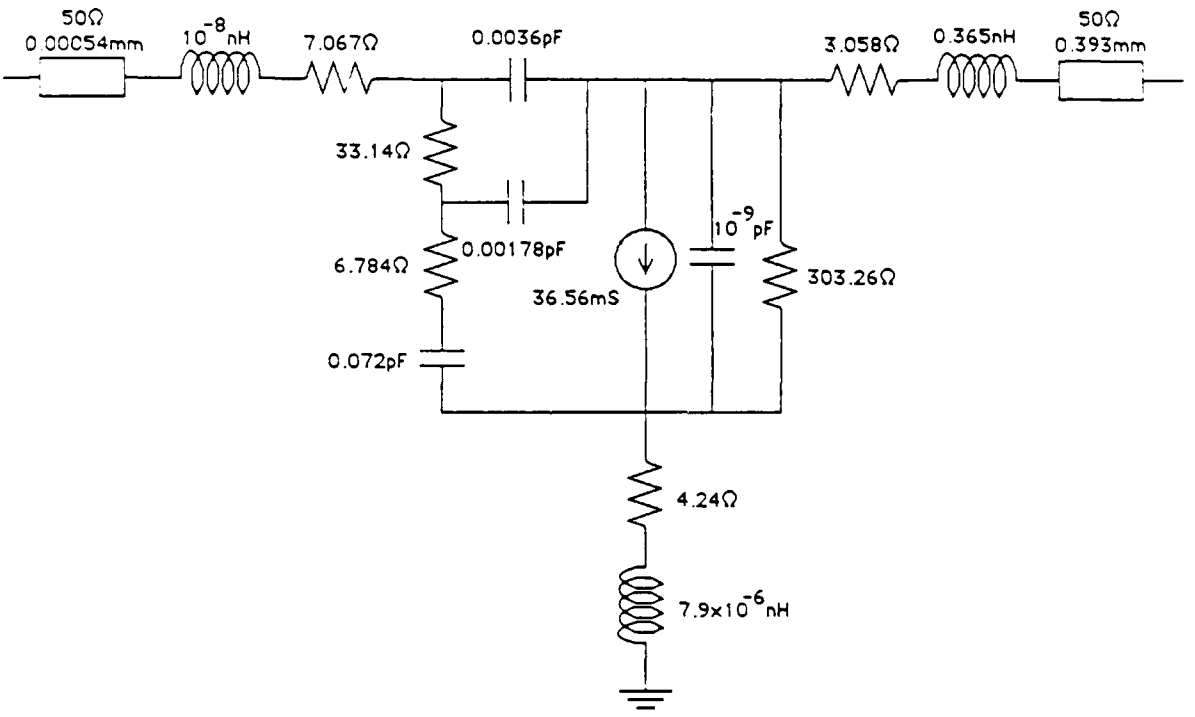
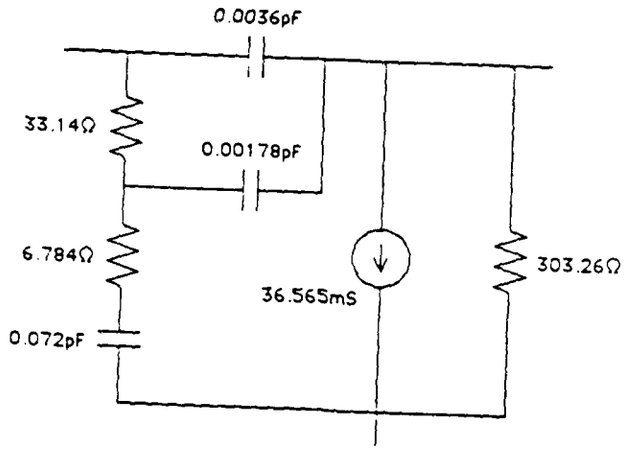
20.00
0.0000
1.000
10.00
FREQ-GHZ
100.0
$f_T \cong 70GHz$

Fig. 2


50Ω
0.00054mm
10^-8 nH
7.067Ω
0.0036pF
3.058Ω
0.365nH
50Ω
0.393mm
33.14Ω
0.00178pF
6.784Ω
0.072pF
36.56mS
10^-9 pF
303.26Ω
4.24Ω
7.9x10^-6 nH

(a)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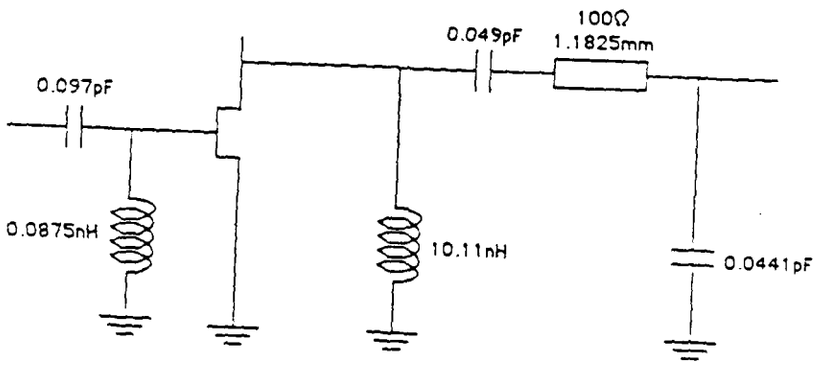
0.072pF

(b)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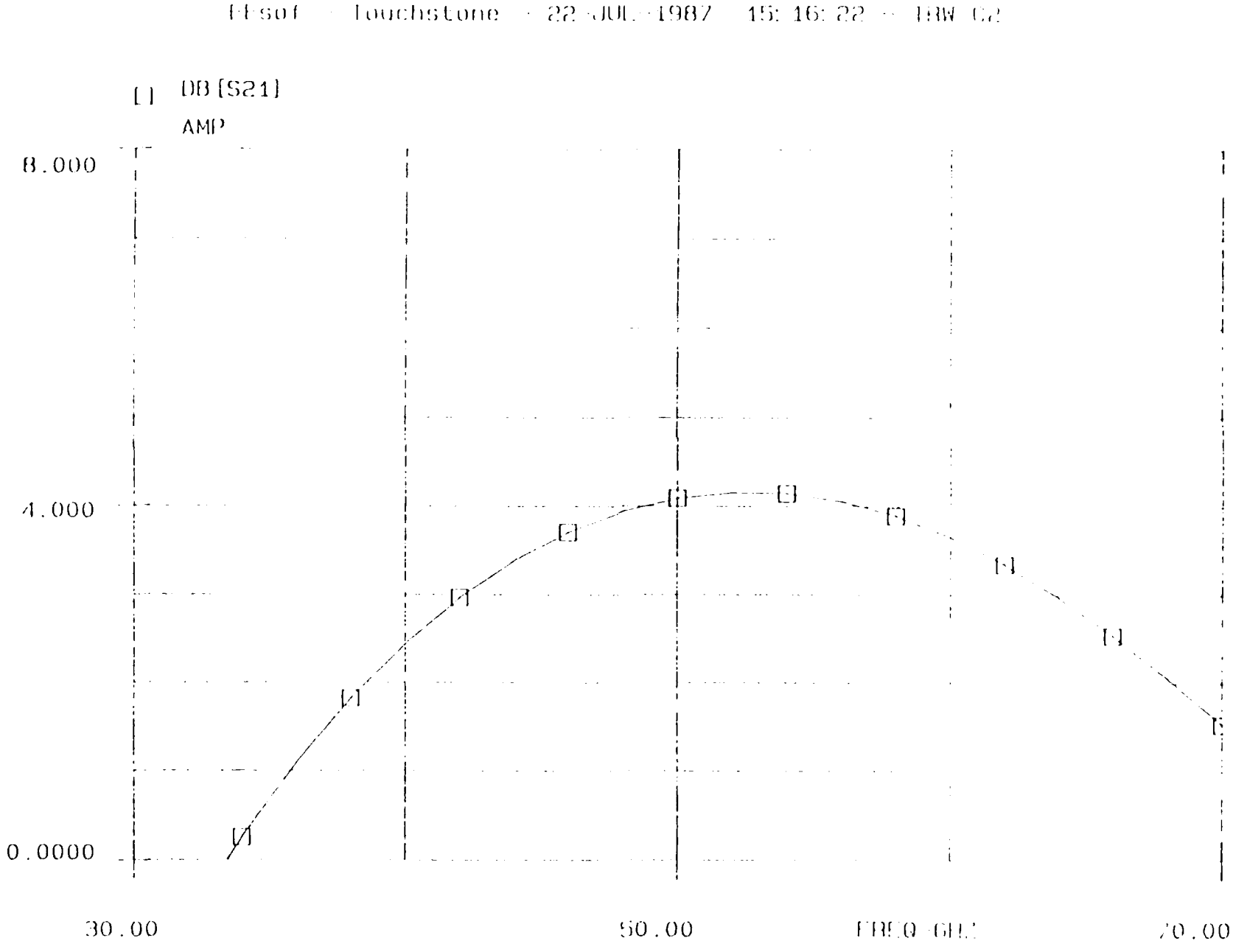
(c)

Fig. 3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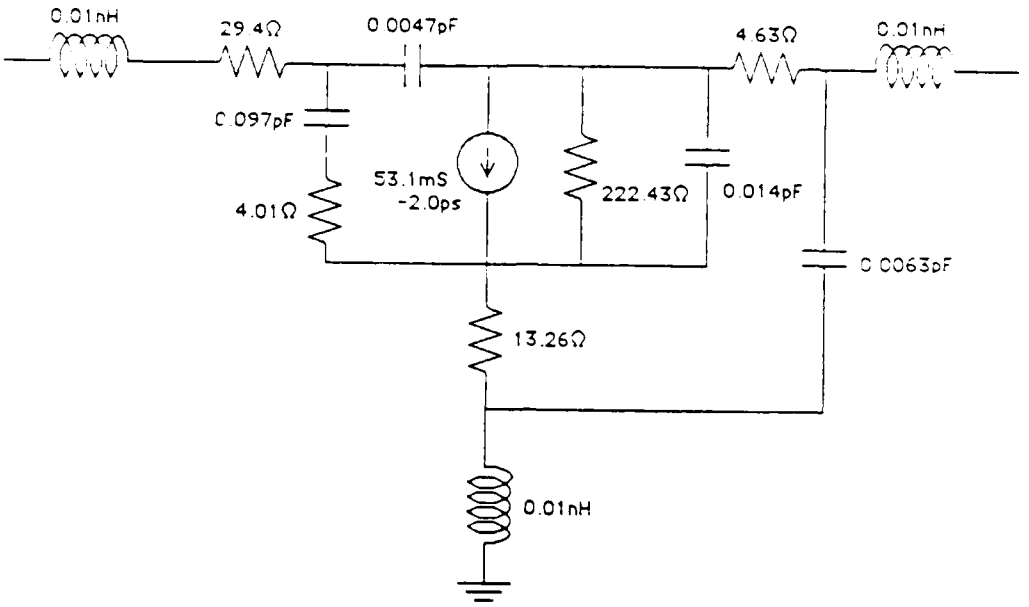
4.000
0.0000
30.00
50.00
70.00

Fig. 4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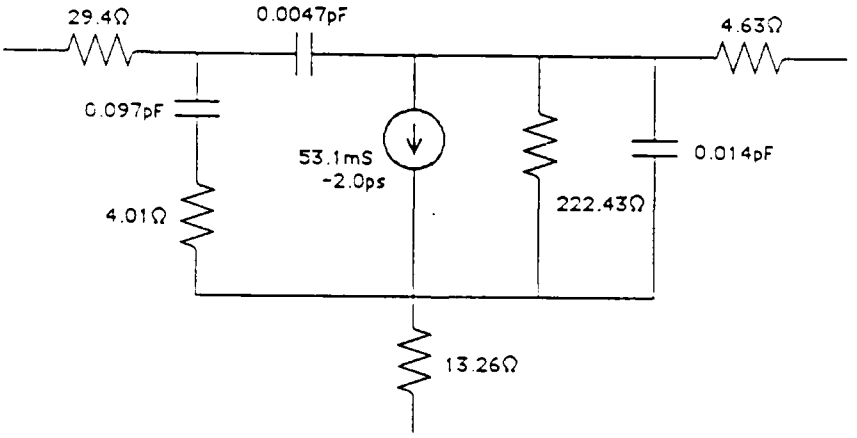
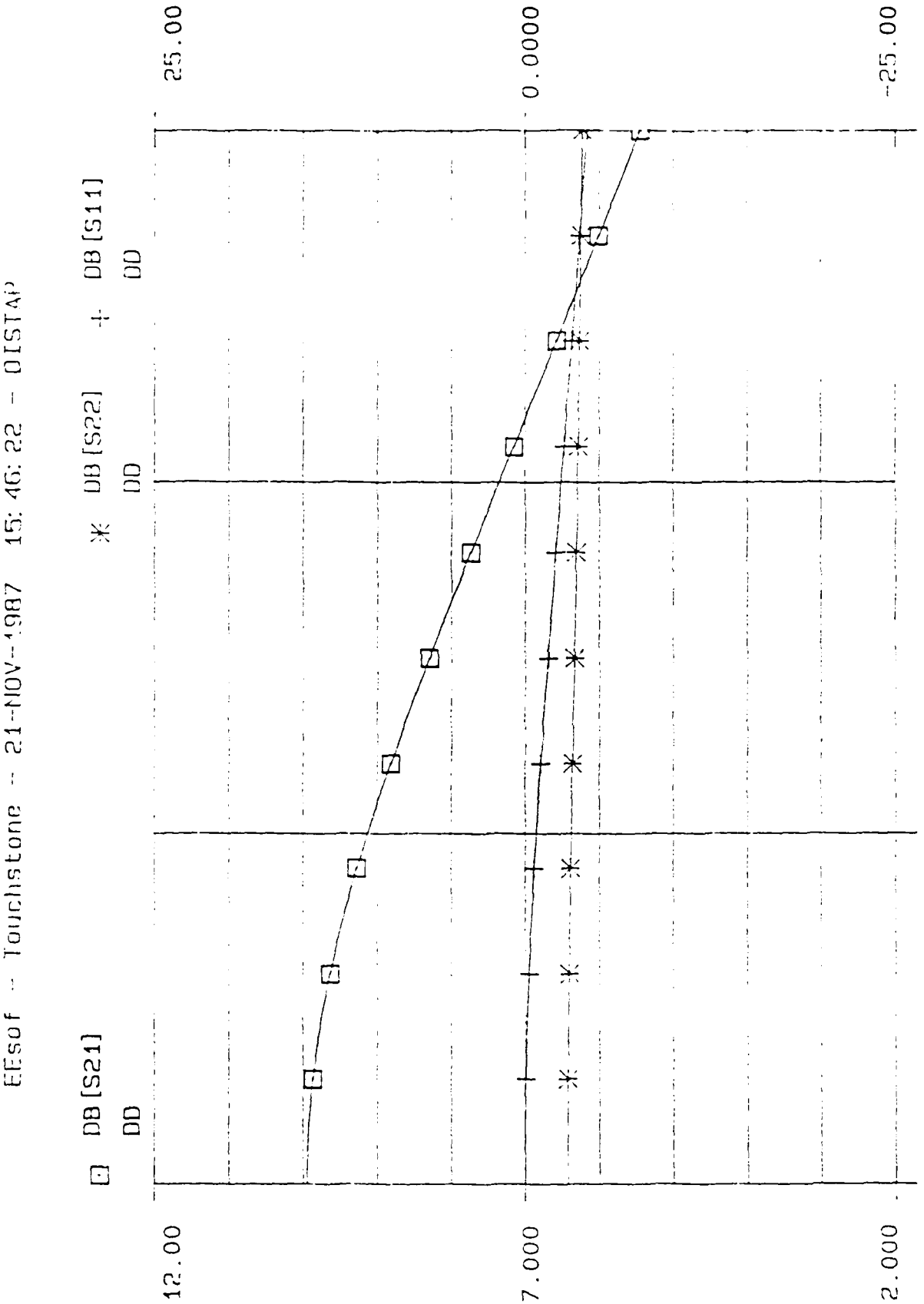
29.4Ω
0.0047pF
4.63Ω
0.01nH
0.097pF
53.1mS
-2.0ps
4.01Ω
222.43Ω
0.014pF
0.0063pF
13.26Ω
0.01nH

(a)


29.4Ω
0.0047pF
4.63Ω
0.097pF
53.1mS
-2.0ps
0.014pF
4.01Ω
222.43Ω
13.26Ω

(b)

Fig. 5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□ DB [S21]
DD
* DB [S22]
DD
+ DB [S11]
DD
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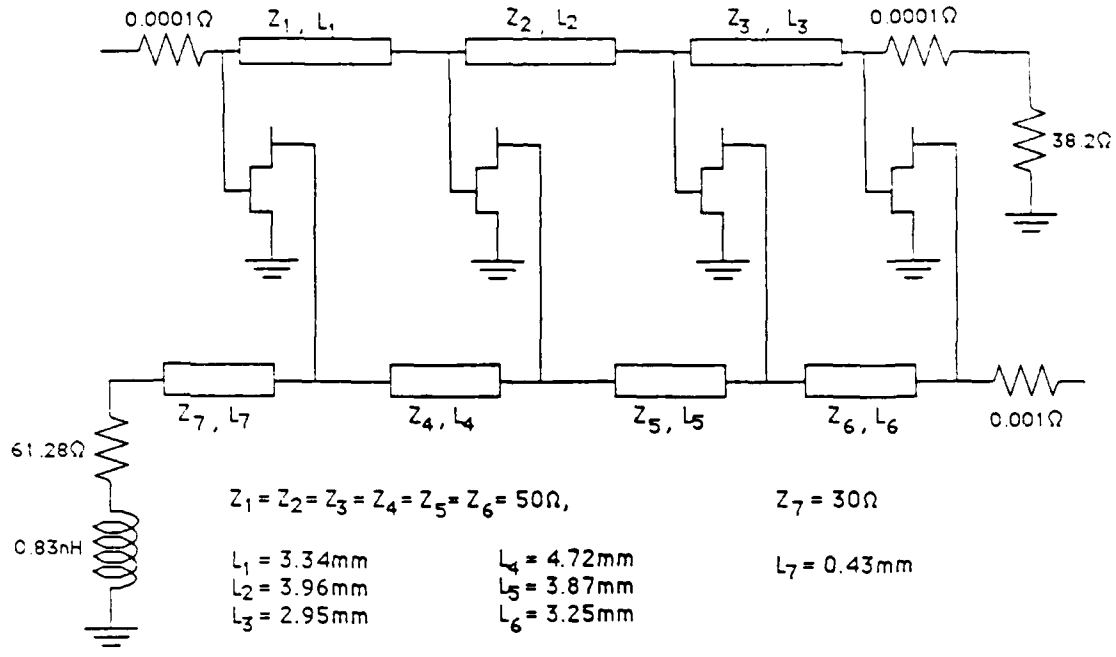
0.0000
-25.00
12.00
7.000
2.000
0.0100
10.01
30.01
FREQ-GHZ

Fig. 6

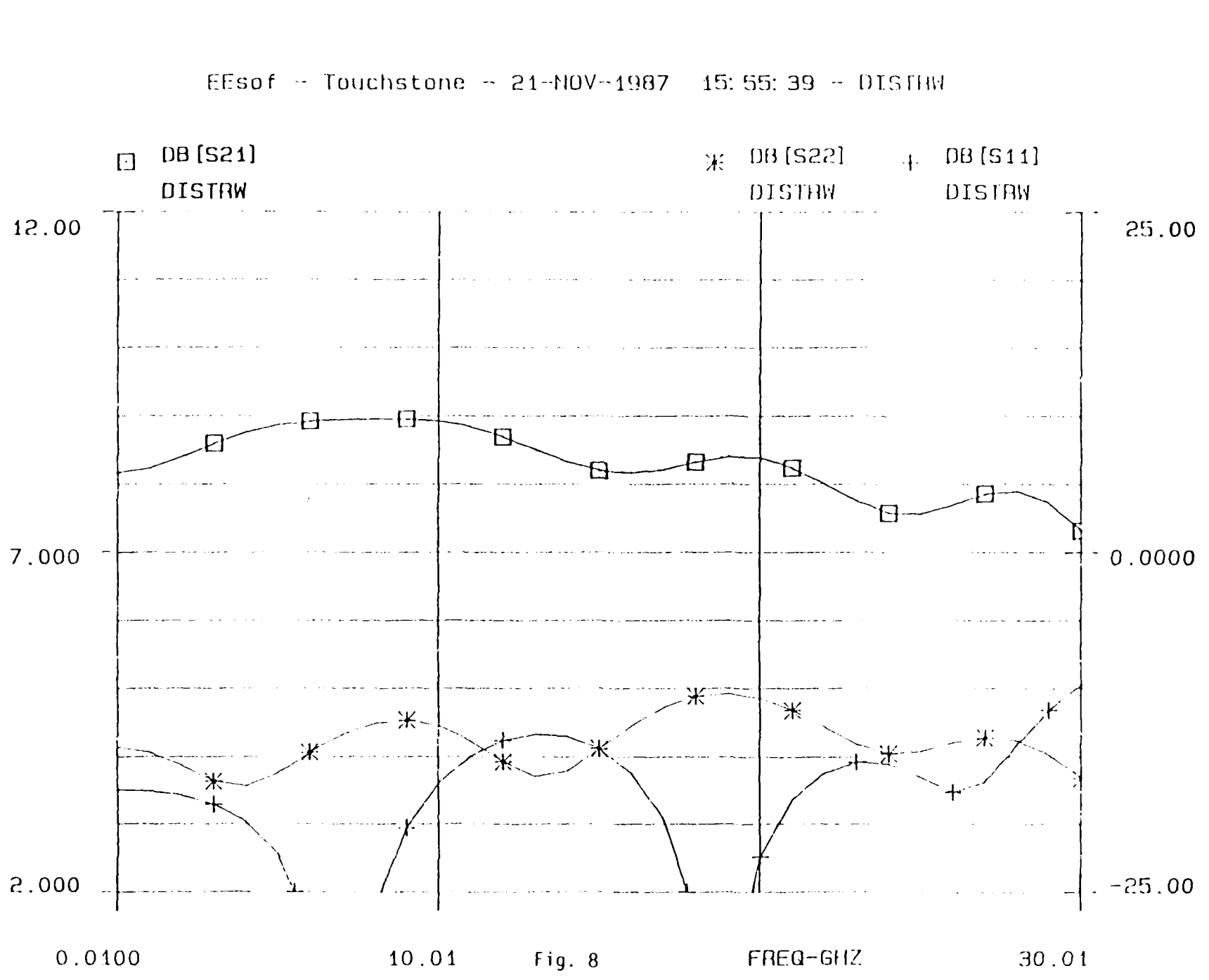


$Z_1 = Z_2 = Z_3 = Z_4 = Z_5 = Z_6 = 50\Omega$,

$Z_7 = 30\Omega$

$L_1 = 3.34mm$
$L_2 = 3.96mm$
$L_3 = 2.95mm$
$L_4 = 4.72mm$
$L_5 = 3.87mm$
$L_6 = 3.25mm$
$L_7 = 0.43mm$

Fig. 7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DB[S21]
DISTRW
DB[S22]
DISTRW
DB[S11]
DISTRW
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2.000
25.00
0.0000
-25.00
0.0100
10.01
FREQ-GHZ
30.01

Fig. 8

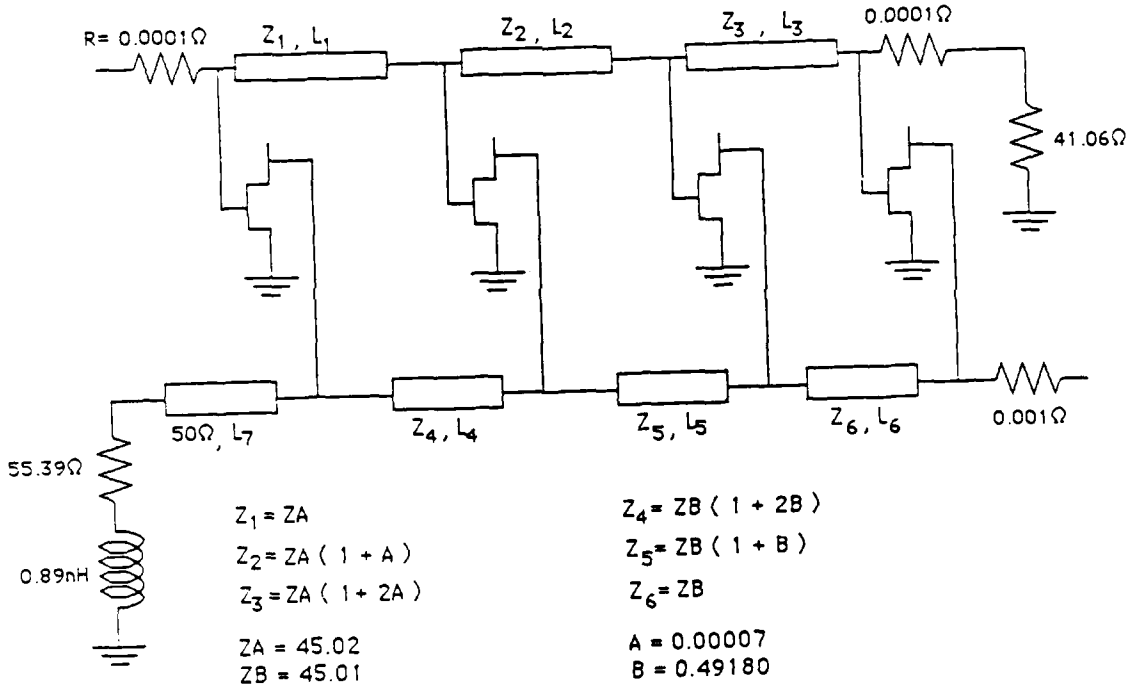
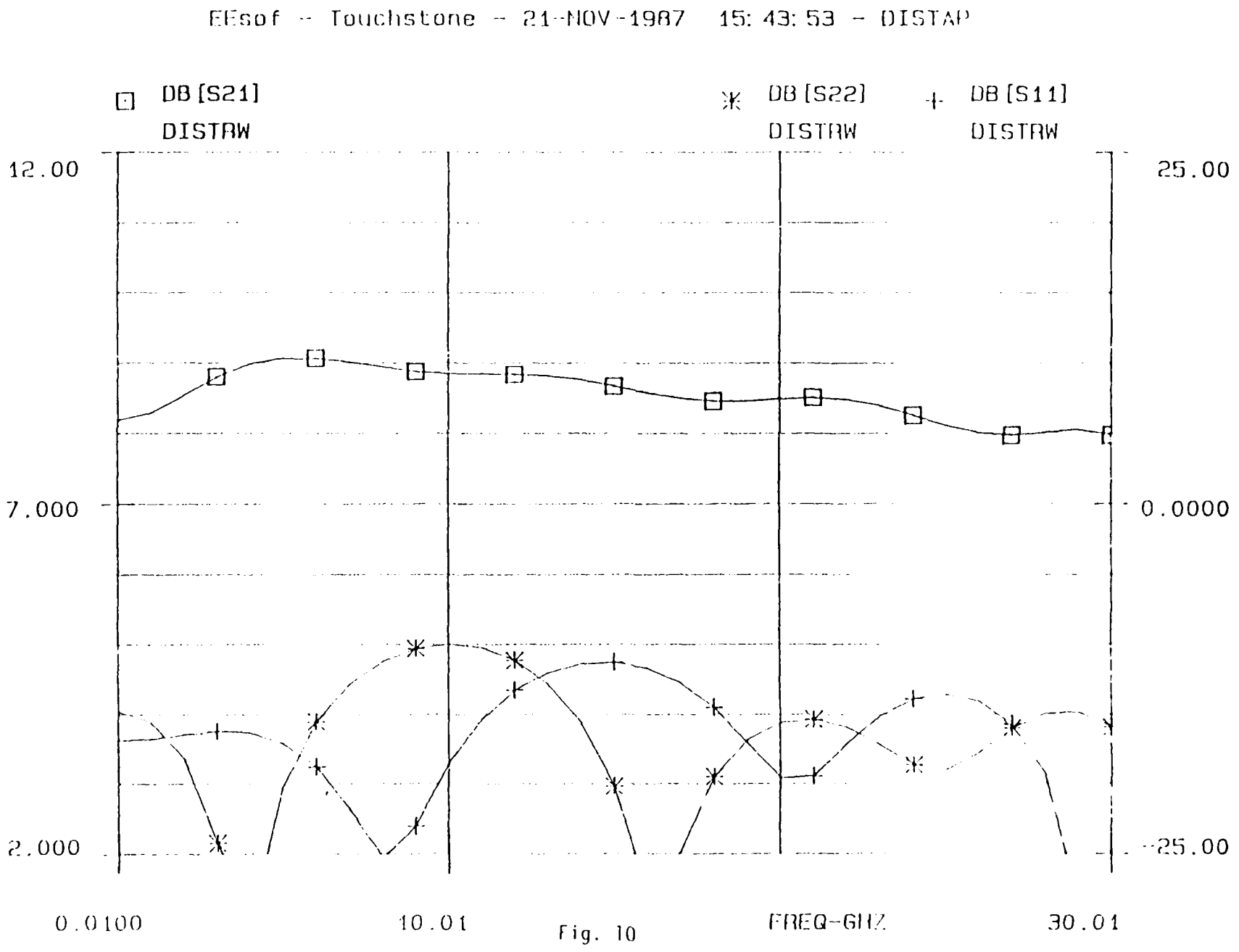

R= 0.0001Ω
Z1 , L1
Z2 , L2
Z3 , L3
0.0001Ω
41.06Ω
50Ω, L7
Z4 , L4
Z5 , L5
Z6 , L6
0.001Ω
55.39Ω
0.89nH
Z1 = ZA
Z2 = ZA (1 + A)
Z3 = ZA (1 + 2A)
ZA = 45.02
ZB = 45.01
Z4 = ZB (1 + 2B)
Z5 = ZB (1 + B)
Z6 = ZB
A = 0.00007
B = 0.49180

Fig. 9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DISTRW
DB[S22]
DISTRW
DB[S11]
DISTRW
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2.000
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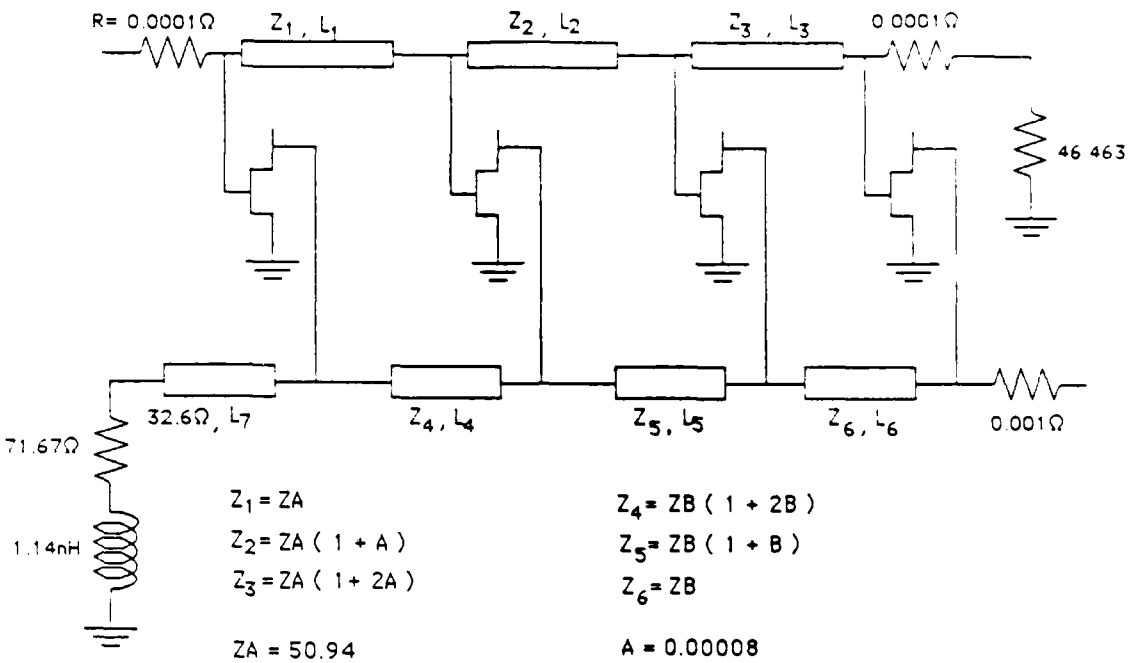
0.0000
-25.00
0.0100
10.01
30.01
FREQ-GHZ

Fig. 10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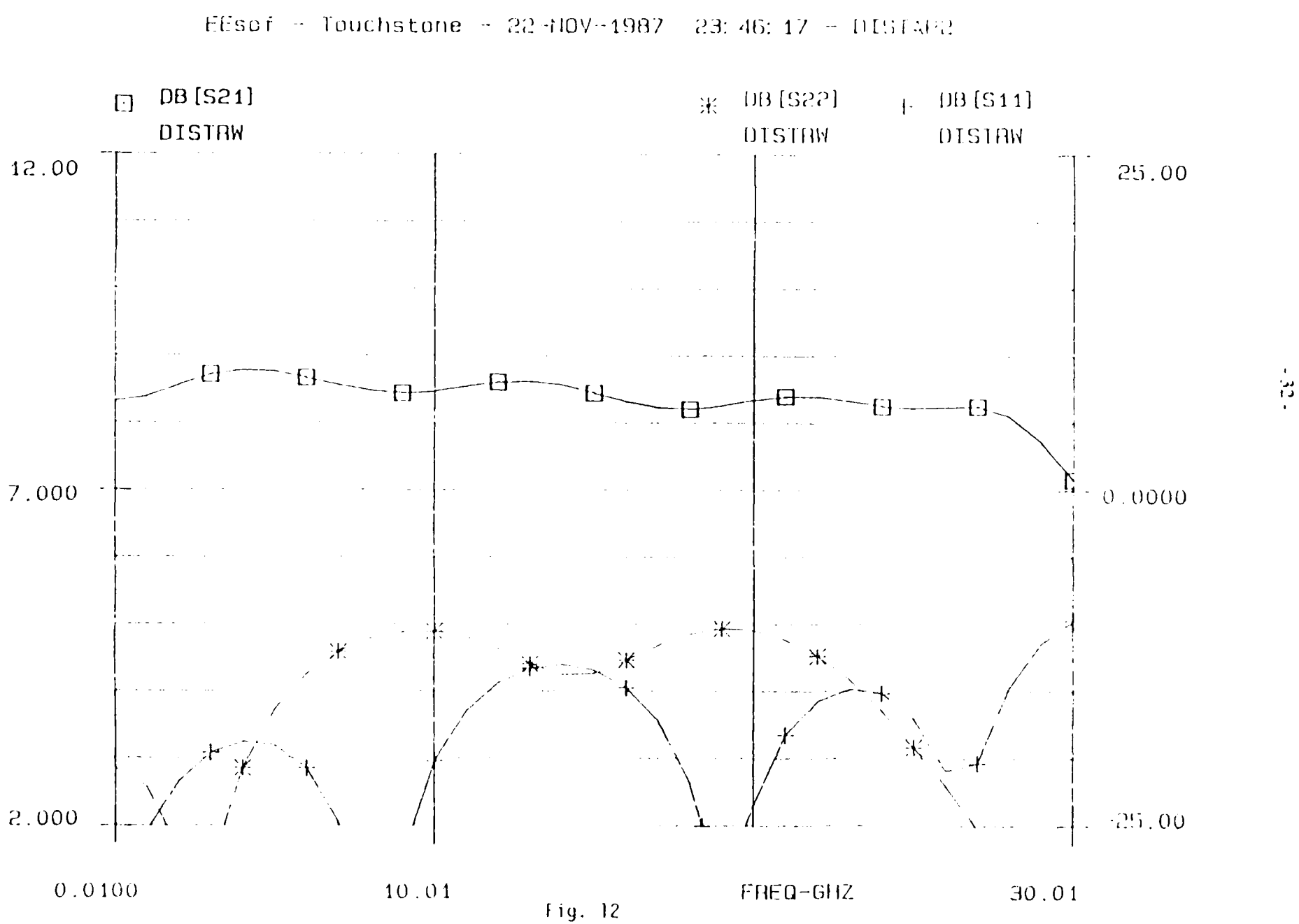
Z2 , L2
Z3 , L3
0.0001Ω
46 463
32.6Ω, L7
Z4 , L4
Z5, L5
Z6 , L6
0.001Ω
71.67Ω
1.14nH
Z1 = ZA
Z2 = ZA (1 + A)
Z3 = ZA (1+ 2A)
ZA = 50.94
ZB = 44.01
Z4 = ZB (1 + 2B)
Z5 = ZB (1 + B)
Z6 = ZB
A = 0.00008
B = 0.75478

Fig. 11


EEsof - Touchstone - 22-NOV-1987 23:46:17 - DISTAP2
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DB[S22]
DISTAW
DB[S11]
DISTAW
12.00
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2.000
25.00
0.0000
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0.0100
10.01
FREQ-GHZ
30.01

Fig. 12

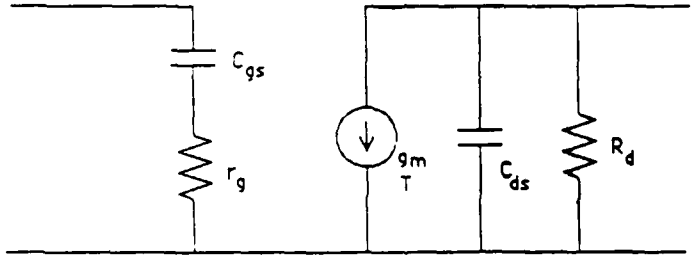

Fig. 13

3. An Analytical HEMT model based on nonlinear charge-control formulation

3.1 Introduction

The high electron mobility transistor (HEMT), a field-effect transistor that takes advantage of the novel properties of the two-dimensional electron gas at the heterointerface has shown promising performance in the of high-speed and high-frequency regimes since its demonstration in 1980. Many models for HEMT's based on a simple linear charge control model similar to that for conventional MOSFET's with only the gate insulator layer. The simulations of the I-V characteristics of these devices have shown fair agreement with experimental data within certain operation regions or in some respects [1]-[4]. Recently, Hughes et al., [5] has pointed out the importance of nonlinear effects on the charge control model and considered the nonlinear variation of Δd (the distance of 2DEG from heterointerface) utilizing a numerical method. These results led to a better fit of the calculated and measured transconductance characteristics. However, the physical mechanism cannot be easily recognized in the derivation of this model. Furthermore, the variation of charge density after current saturation was not considered.

An analytic I-V model of the HEMT, which can simulate the dc with the whole operation range of the dc characteristics through the whole range of operations is derived in this study. This model will be applied to conventional AlGaAs/GaAs HEMT's so that comparisons can be made to the models previously mentioned. In addition, the AlGaAs/GaAs HEMT material system has been much studied so information is available on many of the material parameters needed for the device analysis. This allows the models to focus on representing the basic characteristics and principles behind the operation of HEMT's. The models can later be readily adapted to HEMT's of new material systems, such as the pseudomorphic InGaAs/GaAs HEMT being developed at UCSD, as soon as material parameters become known.

3.2 Nonlinear Charge Control

The first proposed conventional charge control model for HEMT [1] derived from Poisson's equation neglected the Fermi-potential term.

$$qn_s = \frac{\varepsilon_l}{d_l + d_e}\left[V_G - V_T - V_F\right] \tag{1}$$

$$V_T = \phi_B - \frac{\Delta E_c}{q} - \frac{qN_{Dl}}{2\varepsilon_l} d_l^2$$

where n_s is the 2DEG sheet carrier concentration, ε_l and d_l are the permittivity and thickness of carrier supplying layer, respectively, q is the electronic charge, V_G is the gate-source biased voltage, ϕ_B is the barrier height of the Schottky-gate, ΔE_c is the conduction band discontinuity, N_{Dl} is the doping concentration in the top layer, d_e is the spacer layer thickness, and V_F is the Fermi-potential with reference to the conduction band edge of the 2DEG channel.

Drummond et al. [2] extended this model to include the variation of Fermi potential of the two-dimensional electron gas by a linear approximation with respect to sheet carrier concentration.

$$V_F = V_{Fo} + a\, n_s \tag{2}$$

which yielded

$$qn_s = \frac{\varepsilon_I}{d_I + d_e + \Delta d}\ [V_G - V_{Fo} - V_T] \tag{3}$$

where

$$\Delta d = \frac{\varepsilon_I\, a}{q} \tag{4}$$

This model was further modified [5] to take into account the nonlinear dependence of the position of 2DEG channel Δd from heterointerface on gate bias. The 2DEG offset is calculated from the weighted average of all energy levels.

$$\Delta d = \frac{\frac{2}{3}\sum_n n_{sn}\, d_n}{n_s} \qquad n = 0,\ 1,\ 2,\ 3,\ \cdots \tag{5}$$

where

$$n_s = \sum_n n_{sn} \qquad n = 0,\ 1,\ 2,\ 3,\ \cdots \tag{6}$$

Clearly, in the above derivation the computations are very complicated.

According to the triangular potential well approximation the relation between n_s and the Fermi-level can be established, only if the lower and the excited subband are being considered.

$$E_F = \frac{kT}{q}\ln\left\{ -\frac{1}{2}\left[e^{\frac{q}{kT}\gamma_0 n_s^{\frac{2}{3}}} + e^{\frac{q}{kT}\gamma_1 n_s^{\frac{2}{3}}} \right] + \sqrt{\frac{1}{4}\left(e^{\frac{q}{kT}\gamma_1 n_s^{2/3}} - e^{\frac{q}{kT}\gamma_0 n_s^{2/3}}\right)^2 + e^{\frac{q n_s}{DkT}}\, e^{\frac{2q}{kT}(\gamma_0+\gamma_1) n_s^{2/3}}} \right\} \tag{7}$$

As suggested by eq. (7), we can approximate E_F by

$$E_F = a(bn_s)^{\frac{2}{3}} \tag{8}$$

with a high accuracy. Substituting eq. (7) into eq. (1), further manipulations yield the 2DEG sheet carrier concentration

$$n_s = \frac{\varepsilon_I}{(d_I + d_e)\left[1 + \frac{p}{q} n_s^{-\frac{1}{3}}\right]} \left[V_G - \phi_B + \frac{\Delta E_c}{q} + \frac{qN_{D_I}}{2\varepsilon_I} d_I^2 \right] \tag{9}$$

where

$$p = \frac{\varepsilon_I\, a}{d_I + d_e}\, b^{\frac{2}{3}} \tag{10}$$

Eq. (9) indicates that Δd is proportional to $n_s^{-\frac{1}{3}}$. This corresponds to the results calculated from a variational method by Stern and Das Sarma [6].

3.3 Drain Current Characteristics

When a doped layer with wider band-gap is grown on top of an undoped layer with narrower band-gap, a two-dimensional electron gas will form at the heterointerface due to the charge transfer driven by the conduction band discontinuity. In normal operation mode, the depletion of the doped layer is attributed to the charge transfer and Schottky gate depletion. At thermal equilibrium the undepleted channel width of parasitic MESFET, h, as shown in Fig. 1, is

$$h = d_1 - \frac{n_s}{N_{D1}} - \left[\frac{2\varepsilon_1}{qN_{D1}}(\phi_B - V_n - V_G)\right]^{\frac{1}{2}} \tag{11}$$

where V_n is the potential difference between the conduction band edge and the Fermi-energy in the neutral substrate.

The threshold voltage of the parasitic MESFET's conduction where $h = \phi$ may be easily obtained, and can be written as

$$V_c = \phi_B - V_n - \frac{qN_{D_1}}{2\varepsilon_1}\left(d_1 - \frac{n_{so}}{N_{D1}}\right)^2 \tag{12}$$

If the gate applied voltage $V_G \geq V_c$, then the doped layer is not fully depleted and the conduction of parasitic MESFET should be taken into account.

Experimental measurement has shown the velocity saturation phenomenon existing in the high electric field regime for III - V compound material. For simplicity in mathematics manipulation, the field-dependent velocity model is approximated by the following model for both the parasitic MESFET Channel and the two-dimensional electron gas channel.

$$v(E) = \frac{\mu E}{(1 + \frac{E}{E_1})}, \qquad E \leq E_c \tag{13}$$

$$= v_{sat}, \qquad E \geq E_c \tag{14}$$

where μ is the low-field mobility, and E_c is the critical field at the onset of velocity saturation.

3.4 Normal HEMT Operation Mode

1. Linear Region ($V_D < V_{sat}$)

When the applied drain voltage is not high enough to accelerate carriers up to saturation velocity, the drain current can be evaluated.

$$I_D = \frac{\bar{w}\varepsilon_1\mu_2[V_G - V_T - V]}{(d_1+d_e)[1 + \frac{p}{q}\alpha(V_G - V_T - V)^{\frac{1}{3}}]} \quad \frac{E}{1+\frac{E}{E_2}} \tag{15}$$

where $\bar{w}$ is the gate width, α is the nonlinear charge control coefficient and V is the channel potential.

Integrating eq. (15) I_D can be written in terms of y_o and y_D:

$$I_D = \frac{-3\bar{w}\mu_2\varepsilon_1 \left\{ \sum_{n=1}^{6} \left[\frac{(-1)^n}{n} \left(\frac{p}{q}\alpha\right)^{6-n} (y_D^n - y_o^n) \right] + \left(\frac{p\alpha}{q}\right)^6 \ln \left[\frac{y_D + \frac{p}{q}\alpha}{y_o + \frac{p}{q}\alpha} \right] \right\}}{(d_1+d_e)\left[L + \frac{V_D}{E_{c2}}\right]} \tag{16}$$

where y_o and y_D are defined as

$$y_o = [V_G - V_T]^{\frac{1}{3}} \tag{17}$$

$$y_D = [V_G - V_T - V_D]^{\frac{1}{3}} \tag{18}$$

2. Saturation Region ($V_D \geq V_{sat}$)

In saturation, we make use of eq. (9) and (14). The 2DEG channel current in saturation region leads to the equation

$$I_D = \frac{\bar{w}\varepsilon_1\mu_2[V_G - V_T - V_{sat}]E_{c2}}{(d_1+d_e)\left\{1 + \frac{p}{q}\alpha(V_G - V_T - V_{sat})^{\frac{1}{3}}\right\}\left(1 + \frac{E_{c2}}{E_2}\right)} \tag{19}$$

To ensure continuous current transition from linear region to saturation region, we make use of the current continuity between these regions and obtain the following,

$$-6(y_s+\frac{p}{q}\alpha)\left\{ \sum_{n=1}^{6} \left[\frac{(-1)^n}{n} \left(\frac{p}{q}\alpha\right)^{6-n} (y_s^n - y_o^n) \right] + \left(\frac{p\alpha}{q}\right)^6 \ln \left[\frac{y_s + \frac{p}{q}\alpha}{y_o + \frac{p}{q}\alpha} \right] \right\}$$

$$= y_s^4 \left[E_{c2}L(1-K) + V_G - V_T - y_s^3 \right] \tag{20}$$

Channel length modulation factor K and y_s are defined as

$$K = \frac{L - L_c}{L} \tag{21}$$

$$y_s = \left[V_G - V_T - V_{sat} \right]^{\frac{1}{3}} \tag{22}$$

We might determine K and V_{sat}, by solving a set of two-dimensional Poisson equations by Laplace's method and keep the lowest space harmonic [7]. However, a simpler one-dimensional approximation to Poisson equation is adopted in the velocity saturation region, which assumes

$$\frac{\partial^2 V}{\partial X^2} = \beta I_D \tag{23}$$

where the variation of carrier concentration in the direction perpendicular to the current flow is assumed to be negligible.

Solving eq. (23) subjected to boundary conditions, $E(L_c) = E_{c2}$ and $V(L_c) = V_{sat}$, the voltage drop across the saturated channel region can be written in terms of K and V_{sat}.

$$V_{sat} = V_D - \frac{\beta L^2 K^2}{2} \frac{\bar{w}\varepsilon_1\mu_2[V_G - V_T - V_{sat}]\, E_{c2}}{(d_1+d_c)\left\{1+\frac{p}{q}\alpha(V_G - V_T - V_{sat})\right\}^{-\frac{1}{3}}\left[1+\frac{E_{c2}}{E_2}\right]} - E_{c2}LK \tag{24}$$

Note that Eq. (20) and Eq. (24) are functions of two dependent variables, y_s and K. Thus V_{sat} and K can be obtained by solving this set of coupled equations. Even though the equations are of high-order functions of y_s, the range in which the roots y_s and K are located is

$$0 \le K \le 1 \tag{25}$$

$$-\frac{q}{p}\alpha \le y_s \le y_o \tag{26}$$

This will restricts the number of reasonable roots to one.

Once the gate voltage becomes larger than V_c, a conduction channel forms in the parasitic MESFET, i.e., the carrier supplying layer is not fully depleted, causing to current contribution from 2DEG channel as well as a MESFET channel underneath the Schottky gate.

3.5 Parasitic MESFET Conduction Mode $V_G \ge V_c$

Consider the case where the MESFET channel is pinched off at $x = L_M$ by the gate bias. The channel potential at this point reads

$$V_M = V_p - (\phi_B - V_n) + V_G \tag{27}$$

where the pinch-off voltage is given by

$$V_p = \frac{qN_{D1}\left(d_1 - \frac{n_{so}}{N_{D1}}\right)^2}{2\varepsilon_1} \tag{28}$$

Within the conduction channel, the 2DEG will not be perturbed by gate and drain voltages, where the channel potential is lower than V_M, and will stay at thermal equilibrium values, n_{so}, which can be estimated self-consistently by

$$n_{s0} = \frac{\varepsilon_1}{q(d_1+d_e)\left[1+\frac{\rho}{q} n_{s0}^{-1/3}\right]} \left[\phi_B - V_n - V_p - V_T\right] \tag{29}$$

1. Linear MESFET Channel ($V_D < V_M$)

The current flowing through the MESFET channel can be derived as in the conventional MESFET model, which is given by

$$I_1 = \frac{\frac{\bar{w} q \mu_1 N_{D1}}{L}\left(d_1 - \frac{n_{s0}}{N_{D1}}\right)\left[V_D - \frac{2}{3}\frac{(\phi_B - V_n - V_G + V_D)^{3/2} - (\phi_B - V_n - V_G)^{3/2}}{\sqrt{V_p}}\right]}{\left(1+\frac{V_D}{LE_{c1}}\right)} \tag{30}$$

Since $V_D < V_M$, the whole 2DEG channel behaves like a linear resistor, the current flows through the 2DEG channel reads

$$I_2 = \frac{\bar{w}\varepsilon_1\mu_2[\phi_B - V_n - V_p - V_T]V_D}{(d_1+d_e)\left[1+\frac{\rho}{q} n_{s0}^{-1/3}\right]\left[L+\frac{V_D}{E_{c2}}\right]} \tag{31}$$

The total drain current I_D is

$$I_D = I_1 + I_2 \tag{32}$$

2. Pinched-off MESFET Channel ($V_M < V_D < V_{sat}$)

The 2DEG current due to equilibrium two-dimensional electron gas can be calculated as in the linear region.

$$I_2 = \frac{\bar{w}\varepsilon_1\mu_2[\phi_B - V_n - V_p - V_T]V_M}{(d_1+d_e)\left[1+\frac{\rho}{q} n_{s0}^{-1/3}\right]\left[L+\frac{V_D}{E_{c2}}\right]} \tag{33}$$

While the current flows through the MESFET channel it is evaluated with the boundary condition, $V(L_M) = V_M$, and can be expressed as

$$I_1 = \frac{\left[\bar{w}\mu_1 N_D\left(d_1 - \frac{n_{s0}}{N_{D1}}\right)\right]\left[V_M - \frac{2}{3}\left[V_p - \frac{(\phi_B - V_n - V_G)^{3/2}}{\sqrt{V_p}}\right]\right]}{\frac{\bar{w}\varepsilon_1\mu_2[\phi_B - V_n - V_p - V_T]V_M}{I_2(d_1+d_e)\left(1+\frac{\rho}{q} n_{s0}\right)} - \frac{V_M}{E_{c2}} + \frac{V_M}{E_{c1}}} \tag{34}$$

Similar to the formulation in the normal operation mode, the 2DEG current can be explicitly expressed as

$$I_2 = \frac{-3\bar{w}\mu_2\varepsilon_1\left\{-\frac{V_M[\phi_B-V_n-V_p-V_T]}{3[1+\frac{p}{q}n_{so}^{-1/3}]}+\sum_{n=1}^{6}\frac{(-1)^n}{n}\left(\frac{p}{q}\alpha\right)^{6-n}[y_D^n-y_M^n]+\left(\frac{p\alpha}{q}\right)^6\ln\left[\frac{y_D+\frac{p}{q}\alpha}{y_M+\frac{p}{q}\alpha}\right]\right\}}{(d_1+d_e)\left[L+\frac{V_D}{E_{c2}}\right]} \tag{35}$$

3. Saturated MESFET Channel ($V_{sat} < V_D$)

In this operation region, formulation of the current flowing through the MESFET channel is identical to eqn. (34). And the 2DEG current is very similar to that in the pinched-off region and can be derived as

$$I_2 = \frac{-3\bar{w}\mu_2\varepsilon_1\left\{-\frac{V_M[\phi_B-V_n-V_p-V_T]}{3[1+\frac{p}{q}n_{so}^{-1/3}]}+\sum_{n=1}^{6}\frac{(-1)^n}{n}\left(\frac{p}{q}\alpha\right)^{6-n}(y_D^n-y_M^n)+\left(\frac{p\alpha}{q}\right)^6\ln\left[\frac{y_D+\frac{p}{q}\alpha}{y_M+\frac{p}{q}\alpha}\right]\right\}}{(d_1+d_e)\left[L(1-K)+\frac{V_{sat}}{E_{c2}}\right]} \tag{36}$$

Similarly, the two dependent variables, y_s and K, can be solved from the following two equations, derived from current continuity requirement, and from a Poisson equation in the saturation region, separately.

$$-6\left(y_s+\frac{p}{q}\alpha\right)\left\{-\frac{V_M[\phi_B-V_n-V_p-V_T]}{3[1+\frac{p}{q}n_{so}^{-1/3}]}+\sum_{n=1}^{6}\left[\frac{(-1)^n}{n}\left(\frac{p}{q}\alpha\right)^{6-n}(y_D^n-y_M^n)+\left(\frac{p\alpha}{q}\right)^6\ln\left[\frac{y_D+\frac{p}{q}\alpha}{y_M+\frac{p}{q}\alpha}\right]\right\}\right.$$

$$\left.=y_s^4\left[E_{c2}L_c+V_G-V_T-y_s^3\right]\right. \tag{37}$$

$$\left[1-\frac{\beta L^2K^2\bar{w}\varepsilon_1\mu_2E_{c2}}{2(d_1+d_e)(1+\frac{E_{c2}}{E_2})}\right]y_s^4+\left(\frac{p}{q}\alpha\right)y_s^3+(V_D-V_G+V_T-E_{c2}LK)y_s+\left(\frac{p}{q}\alpha\right)(V_D-V_G+V_T-E_{c2}LK)=0 \tag{38}$$

3.6 Discussions

The performance of the model is evaluated with the data from from Drummond et al.[2], we have the model to evaluate its performance. Fig. 2 shows the drain I-V characteristics for the 1 μm device. The used parameters are listed in Table 1. This model gives a better agreement with the experimental I-V curves than does the two-piece model. In this simulation run, the parasitic source and drain resistance are not included so parasitic resistances are not taken into account. However, this kind of gain reduction can be covered by adding two parasitic resistances R_s and R_d to the equivalent circuit model externally.

In the deeper gate reverse bias region, the modeled results have a better fit to the experimental data than to existing models due to the more accurate nonlinear charge control model operating in the saturation region. There the carrier concentration in 2DEG channel shows high sensitivity to the variation of gate potential, because the scarce carriers are repelled further from the heterointerface by the gate field. This effect leads to the reduction in transconductance.

The next step to improving the accuracy of this model is further modification of the parasitic MESFET portion. The existing parasitic MESFET model can not describe its external behavior adequately from the view point of gate transconductance. The remedy being planned will include some appropriate terms in the formulation to take care of real space transfer effects. Those current components will be weighted to guarantee the smooth transition from 2DEG current dominated region to the transconductance compression region around the onset of parasitic MESFET conduction.

3.7 Conclusions

We have derived I-V characteristics model for the HEMT's based on a nonlinear charge control formulation which takes into consideration the variation of the 2DEG distance offset from the heterointerface as a function of bias. The model has been kept in a simple and analytical form, making it a possible module to be implemented in the circuit simulation program without adding too heavy of a computation load. Also, the modeled results are in fair agreement with experimental data, which demonstrates that the model could be applied to the optimization of device performance.

Table 1

Parameters Used for the HEMT

L	1 μm
W	145 μm
d_i	450 A
d_e	100 A
μ_2	4050 cm^2/Vs
v_s	1.0×10^7 cm/s
E_{c2}	3.0 KV/cm
ε_i	12.2 ε_0
ΔE_C	0.32 V
a	97.6 mV
b	1.0×10^{12} cm^{-2}
α	1.0×10^{-4}
β	3.2×10^8
ϕ_B	1.15 V
N_{D1}	6.5×10^{17} cm^{-3}
V_{F0}	0.0 V
T	300.0° K

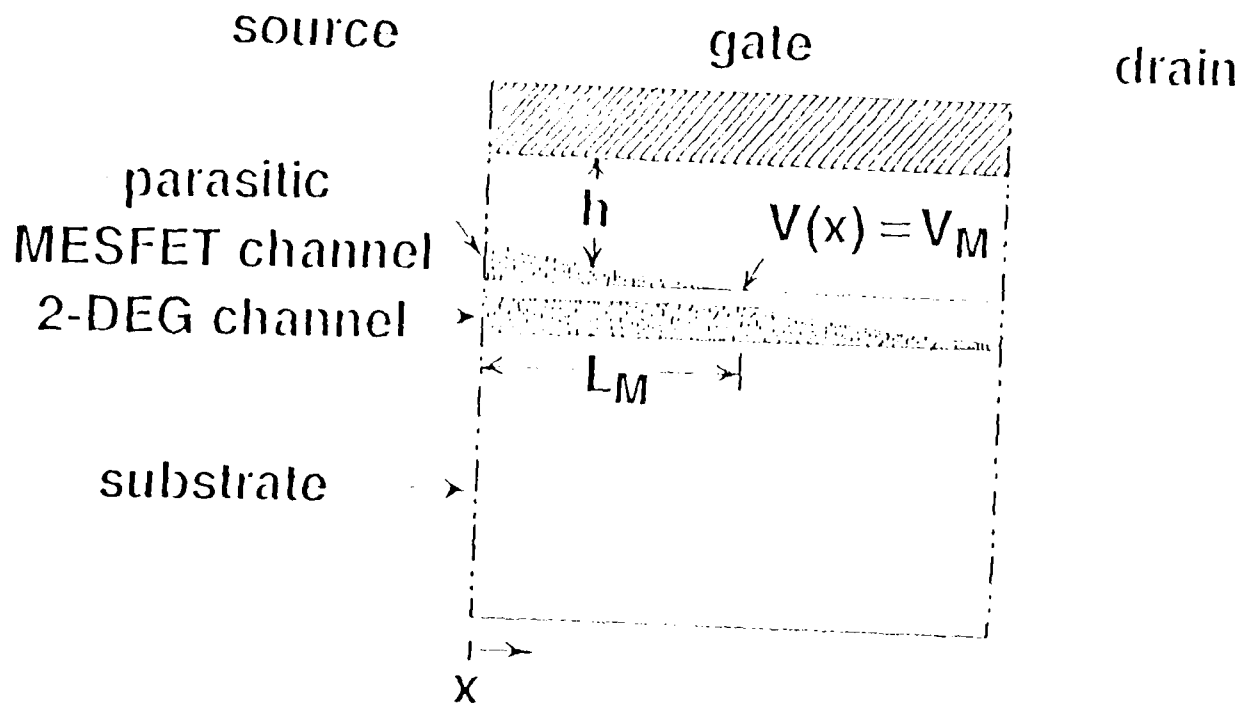

Fig. 1

Schematic diagram illustrating current in two-dimensional electron gas channel and parasitic MESFET channel

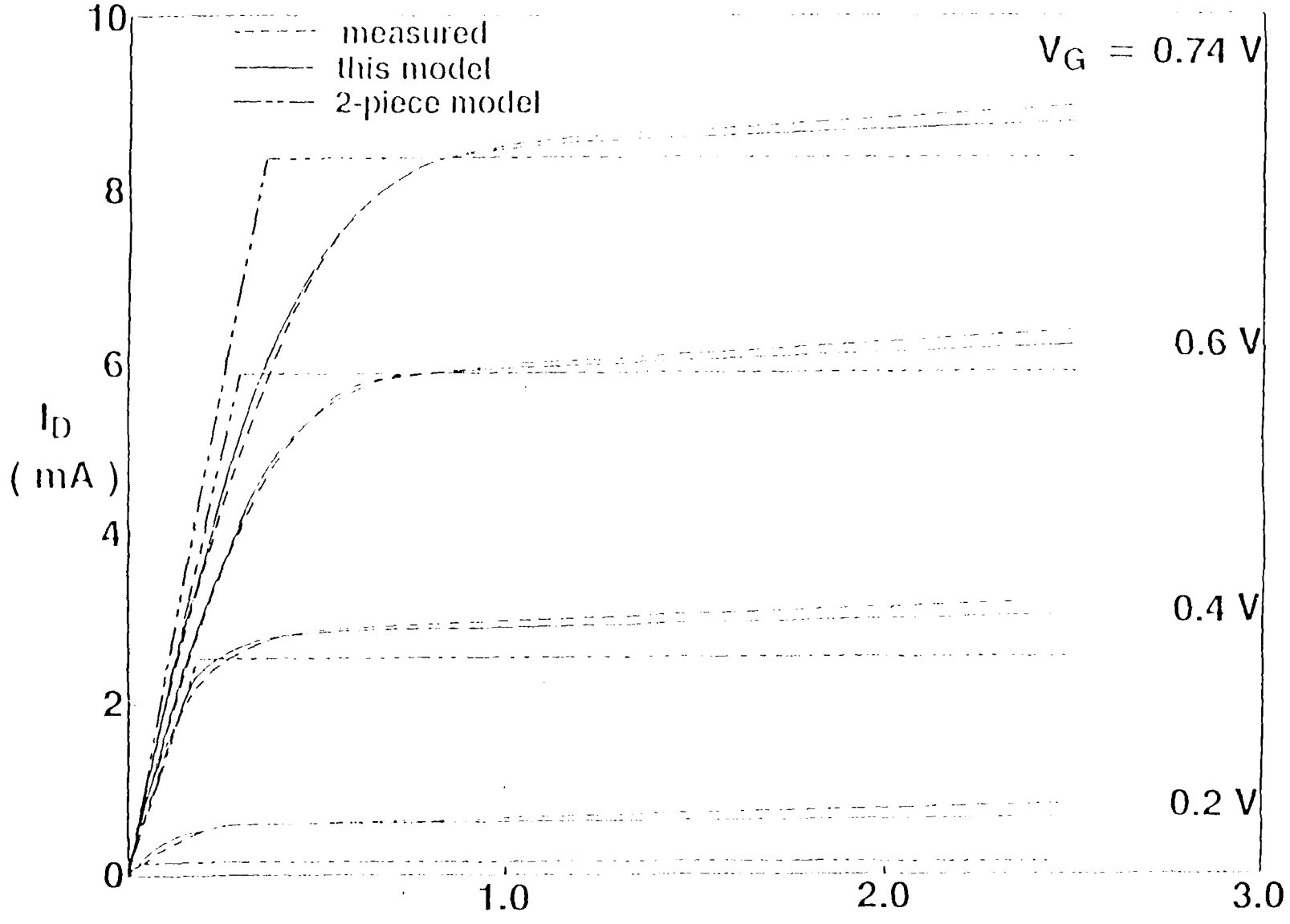

Fig.2

Comparison of this model with Drummond's two-piece velocity model [2]

3.8 References

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4. SDA: A Highly Efficient Two-Dimensional Finite-Element Simulator for Semiconductor Device Analysis

4.1 Introduction

The further reduction in geometrical dimensions of today's semiconductor devices and the advent of novel devices employing new materials, has highlighted the need for simulation, especially numerical simulation. This has become a powerful tool for providing insight into the functioning of devices by examining the distribution of various physical quantities in the interior of a device as well as external device behavior. In addition, the predictive capabilities of detailed numerical device simulations can be used to enhance device characterization techniques and to form a basis for the technological optimization of process, device and circuit designs.

A new approach to nonlinear finite element numerical analysis for semiconductor devices, developed by the VLSI Research Laboratory at UCSD, has been implemented in a general purpose two-dimensional finite element program for Semiconductor Device Analysis (SDA). In addition to the conventional finite-element algorithm constructed to carry out all types of linear and nonlinear finite-element analysis procedures, the following new features are incorporated to enhance computing capability, accuracy, and graphical interaction. In SDA, mesh generation for an arbitrary semiconductor device and the choice of an optimal solving algorithm can be done automatically by SDA or interactively through a dialogue with the user. By using high order error estimation and predictive techniques, a strategy for fully adaptive spatial grid generation and optimal choice of the time steps developed to find a balance between the reduction of discretization errors and the additional amount of computational efforts needed. The high computation speed of SDA is achieved by using simultaneously a modified Scharfetter-Gummel method to solve the two-dimensional Poisson's equation and the two-dimensional continuity equation on an optimal self-adaptive triangular mesh. New physical models have been derived for the analysis of and submicron devices and new III-V compound devices, such as the pseudomorphic InGaAs HEMT. These will be useful for investigating the device physics as well as suggesting new approaches for improvement.

This program can simulate GaAs MESFET and AlGaAs/GaAs heterojunction bipolar transistors as well as conventional silicon MOSFET and bipolar transistors. These devices can have arbitrary geometry and impurity distribution with a wide temperature range.

The program also considers incomplete ionization and variable band structure effects and can employ either Boltzmann or Fermi statistics. The graphics capability makes the graphic interpretation of simulation results very clear and attractive.

4.2 Basic Equations

The two-dimensional numerical model, SDA-1A, developed at UCSD for semiconductor device analysis first examines Poisson's equation

$$\nabla(\varepsilon\nabla\psi) = n - p + N_s \tag{1}$$

where n, p are electron, and hole concentration, respectively ψ is potential and N_s is net impurity concentration, which is defined as

$$N_s = N_D^+ - N_A^- \tag{2}$$

N_D^+ and N_A^- the ionized donor and acceptor concentration, respectively, are given by,

$$N_D^+ = \frac{N_D}{1 + g_d \exp\left[-\frac{E_D - E_{fn}}{k_B T}\right]} \tag{3}$$

$$N_A^- = \frac{N_A}{1 + g_a \exp\left[-\frac{E_{fp} - E_A}{k_B T}\right]} \tag{4}$$

where E_D is the donor energy level and E_A is the acceptor energy level. The electron and hole concentration can be represented as

$$n = n_{ie} e^{(-\phi_n + \psi + V_n)/V_t} \tag{5}$$

$$p = n_{ie} e^{(\phi_p - \psi + V_p)/V_t} \tag{6}$$

where ϕ_n and ϕ_p are the electron and hole quasi-Fermi potentials respectively, V_n and V_p are electron and hole band parameters respectively, n_{ie} is intrinsic carrier density for reference material and thermal potential is given by

$$V_t = \frac{k_B T}{q}$$

The equations for the electron and hole band parameters are as follows

$$\begin{cases} V_n = -\dfrac{Chi - Chi_r}{q} + \dfrac{k_B T}{q} \ln \dfrac{N_c}{N_{cr}} + \dfrac{k_B T}{q} \ln \dfrac{F_{\frac{1}{2}}(\eta_c)}{e^{\eta_c}} \\ V_p = -\dfrac{Chi - Chi_r}{q} - \dfrac{E_g - E_{gr}}{q} + \dfrac{k_B T}{q} \ln \dfrac{N_v}{N_{vr}} + \dfrac{k_B T}{q} \ln \dfrac{F_{\frac{1}{2}}(\eta_v)}{e^{\eta_v}} \end{cases} \tag{7}$$

The potential difference between the fermi levels and the conduction or valence band are defined as

$$\begin{cases} \eta_c = \dfrac{E_{FN} - E_c}{k_B T} = \dfrac{q(\psi - \phi_n) + (Chi - Chi_r) + \frac{1}{2} k_B T \ln\left[\dfrac{N_{vr}}{N_{cr}} e^{-E_g/k_B T}\right]}{k_B T} \\ \eta_v = \dfrac{E_v - E_{FP}}{k_B T} = \dfrac{q(\psi - \phi_p) + Chi - Chi_r) - E_g - \frac{k_B T}{2} \ln\left[\dfrac{N_{vr}}{N_{cr}} e^{-E_g/k_B T}\right]}{k_B T} \end{cases} \tag{9}$$

(10)

where χ is electron affinity, E_g is bandgap, N_c, N_v are effective density of states for the conductor band and valence band respectively. The subscript r represents the reference material, and $F_{1/2}$ is Fermi integral.

The second major equation for device analysis is the continuity equation.

$$\nabla \cdot \vec{J}_n = \frac{\partial n}{\partial t} + R \tag{11}$$

$$\nabla \cdot \vec{J}_p = -\frac{\partial p}{\partial t} - R \tag{12}$$

where R is the recombination rate which includes SRH bulk and surface recombination, Auger recombination and impact ionization. The recombination rate in turn is described by

$$R = \frac{(np-n_i^2)}{\tau_{po}(n+n_1)+\tau_{no}(p+n_1)} + (np-n_i^2)(C_p p + C_n n) - \frac{1}{q}(\alpha_n |J_n| + \alpha_p |J_p|) \tag{13}$$

and $\vec{J}_n$, $\vec{J}_p$ are the electron and hole current densities respectively are defined as

$$\vec{J}_n = -qn\mu_n \nabla \phi_n \tag{14}$$

$$\vec{J}_p = -qp\mu_p \nabla \phi_p \tag{15}$$

where μ_n and μ_p are electron and hole mobilities. For GaAs, the following empirical electron mobility model, which is a function of impurity concentration, temperature and field, is used

$$\mu(N_T, T) = \left\{ \frac{\mu_1 (N_T - 10^6 N_{ref})}{N_T + 10^6 N_{ref}} + \frac{\mu_{max} + \mu_{min}}{[1 + N_T/N_{ref}]^\alpha} \right\} \frac{T}{300} \tag{16}$$

$$\mu(N_T, T, E) = \frac{\mu(N_T, T) + \frac{V_{sat}}{|E|}\left[\frac{|E|}{E_o}\right]^4}{1 + (|E|/E_o)^4} \tag{17}$$

$$V_{sat} = V_{sat}(300K) - \beta T \tag{18}$$

where E is field and V_{sat} is saturation speed.

It should be emphasized that the model described above has taken into account incomplete ionization of impurities ($N_D^+ \neq N_D$, $N_A^- \neq N_A$ in (2), (3), (4)), and the different conditions which require either Fermi or Boltzmann statistics. In equations (7) and (8), with Fermi statistics $F_{1/2}(\eta_c) \neq e^{\eta_c}$, $F_{1/2}(\eta_v) \neq e^{\eta_v}$, and for Boltzman statistics $F_{1/2}(\eta_c) = e^{\eta_c}$, $F_{1/2}(\eta_v) = e^{\eta_v}$. Finally, for heterojunctions we find that $V_n \neq 0$, $V_p \neq 0$ in (5), (6).

4.3 Discretization Method Using Scharfetter-Gummel Scheme

The equations (1), (11), and (12) as described above can be expressed in a general form like

$$\nabla\cdot(a\nabla u) = f \tag{19}$$

where $\mu=(\psi,\ \Phi_n,\ \Phi_p)$,

$$f = (n-p+N_a,\ \frac{\partial n}{\partial t}+R,\ -\frac{\partial n}{\partial t}),\ a=$$

$$a = (\varepsilon,\ e^{\psi},\ e^{-\psi}).$$

After manipulation using a finite discretization scheme, the discretized equation set becomes

$$F_i = \int a\nabla u\phi_i\,d\Omega + \int f\phi_i\,d\Omega = 0 \tag{20}$$

This is a set of non-linear equations that can be solved by Newton method. The equation set in Newton iteration form is

$$\sum_j (K_{ij}+G_{ij})\,\nabla u_j = -\left(\sum_j K_{ij}u_j + f_i\right) \tag{21}$$

where

$$K_{ij} = \int a\nabla\phi_i\nabla\phi_j\,d\Omega \tag{22}$$

$$G_{ij} = \int \frac{\partial f}{\partial u}\phi_i\phi_j\,d\Omega \tag{23}$$

$$f_i = \int f\phi_i\,d\Omega \tag{24}$$

A seven point Gaussian quadrature method is used in eqs. (22)-(24), which reads as

$$\int_e F\,d\Omega = \sum_{i=1}^{7} w_i F_i \tag{25}$$

where w_i is weighting factor at the i^{th} point and F_i is the value of function F at the i^{th} point. The finite element mesh is comprised of triangular elements and so the 1st, 2nd and 3rd points are the vertices of the triangle, the 4th, 5th and 6th points are the mid-points of the edges and the 7th point is the center of the triangle.

Calculation of the values of n, p, e^{ψ}, $e^{-\psi}$ at the 4th, 5th, 6th, and 7th points is very important and critical because it has a significant effect on the accuracy of discretization and the convergence speed. First, we apply the Scharfetter-Gummel (S-G) formula into Poisson's equation as well as into the continuity equations using finite element methods, so that the computational effort required for convergence is reduced and the accuracy of solutions is improved significantly.

The S-G formulas assumed in SDA-1A are as follows:

$$n(x_i) = (1 - g(x_i, \Delta\psi_{ij}))n_i + g(x_i, \Delta\psi_{ij})n_j \tag{26}$$

$$p(x_i) = (1 - g(x_i, -\Delta\psi_{ij}))p_i + g(x_i, -\Delta\psi_{ij})p_j$$

$$(e^{\psi})_k = B(\Delta\psi_{ij})e^{\psi_i}$$

$$(e^{-\psi})_k = B(-\Delta\psi_{ij})e^{-\psi_i}$$

where

$$g(x, y) = \left(1 - \exp\left(y\frac{x - x_i}{h_{ij}}\right)\right) / (1 - \exp(y)) \tag{27}$$

$$B(x) = x / [\exp(x) - 1],$$

$$\Delta\psi_{ij} = \psi_j - \psi_i,$$

$$h_{ij} = \chi_j - \chi_i$$

To illustrate the effectiveness of this new scheme described above, which will be called method II, an abrupt n–P junction is simulated, and results are shown as Table 1 - Table 4. Method I is the classical finite element method, using low order polynomials to approximate n, p, e^{ψ}, and $e^{-\psi}$.

Table 1. Number of iterations required for convergence (NUM) versus impurity density (N_d) with method II (the number of mesh points N_p = 24, Na = 1×10^{15} cm^{-3}, zero bias)

N_d (cm^{-3})	5×10^{15}	5×10^{16}	5×10^{17}	5×10^{18}	5×10^{19}	1×10^{20}
N_p	24	24	24	24	24	24
NUM	6	6	7	8	8	7

Table 2. NUM and the fewest number of mesh points N_{pmin} required for convergence versus N_d with method I (classical method) ($Na = 1 \times 10^{15}\ cm^{-3}$, zero bias)

$N_d(cm^{-3})$	5×10^{15}	5×10^{16}	5×10^{17}	5×10^{18}	5×10^{19}	1×10^{20}
N_{pmin}	24	37	149	194	352	446
NUM	11	36	17	70	134	260

Table 3. A comparison of discretization errors of Poisson's equation with method I and with method II, as a function of minimum mesh size $\Delta X_{min}(\mu)$ ($Na = 1 \times 10^{15}\ cm^{-3}$, $N_d = 5 \times 10^{15}\ cm^{-3}$, zero bias)

$\Delta X_{min}(\mu)$		0.15	0.075	0.0375
ERR	I	46.07	21.30	9.30
%	II	13.68	8.23	1.58

Table 4. A comparison of discretization errors of continuity equations with method I and that with method II, as a function of ΔX_{min} ($Na = 1 \times 10^{15}\ cm^{-3}$, $N_d = 5 \times 10^{15}\ cm^{-3}$, $V_{app} = 0.6V$)

$\Delta X_{min}(\mu)$		0.15	0.075	0.0375		0.15	0.075	0.0375
ERR	I	n	34.19	19.86	10.58	p	24.19	12.21
(%)	II		20.20	5.53	2.01		12.01	5.76

From Tables 1 and 2, it is shown that method II is sufficiently accurate so that the convergence of the problem is almost independent of the impurity density and the grid size of mesh. This is in contrast to method I where the convergence is very sensitive to the impurity density and fineness and layout of the mesh. This is due to large integration errors, especially in highly doped regions. When $N_D = 10^{20}\ cm^{-3}$ and $N_a = 5 \times 10^{15}$, the new method only needs 7 iterations on a rather rough mesh (the number of points in the mesh ($N_p = 24$), while the classical method needs 246 iterations on a rather fine mesh. ($N_p = 446$). This shows the convergence rate increases by a factor of 37. The saved time is greater because the time per iteration on rough mesh is far less than on fine mesh.

From Tables 3 and 4, it is shown that with method II, we can obtain more accurate solutions than with method I on the same mesh particularly for Poisson's equation. In addition, the results indicate that applying method II to the continuity equations will be able to take the same advantage of the S-G scheme as those well known in the finite difference counterpart. When using the mesh whose minimum mesh size Δx_{min} 0.0375 μ the accuracy of solution of ψ, n, p for method II is increased by a factor of 5.8, 5.26, 3.20, respectively, over method I. The smaller Δx_{min}, becomes the higher the improvement of accuracy.

4.4 Non-Linear Iteration Algorithm

It is well known that decoupled methods have the advantage of higher speed and less storage requirements compared with coupled methods in the low and medium current regime. However, its speed is much lower than that of coupled method in the high current regime. This is due to a considerable increase in the number of relaxation iterations between equations needed for convergence when there is strong coupling among the equations. Therefore, we proposed the following schemes to overcoming the drawbacks of decoupled methods.

(1) Adaptive control of inner iteration number in solving a single equation.

The inner iteration is Newton iteration and the out iteration is S-G iteration. Because the error function per outer iteration usually decreases only by a factor of 0.3 - 0.5, it is not necessary to have the inner iteration reach convergence during the initial phase of outer iteration before the start of next outer iteration. Therefore, the following strategy is adopted:

If $\|F_\psi\| > C$, the inner iteration proceeds until its error function decreases by an order of two. Otherwise the iteration keeps going until the convergence is reached.

The computation shows that the desired computation quantity is decreased considerably by the method.

(2) Variable order prediction technique and adaptive control of the step for bias voltage.

A variable order and step method, which is similar to the auto-integration algorithm, but in terms of voltage step instead of time step, is presented. It is shown that the number of out relaxation iterations is decreased significantly by the method.

(3) The method to speed up convergence by using SOR and extrapolation in outer iteration is assumed.

4.5 The Self-Adaptive Mesh Refinement Technique

The initial mesh for finite element discretization is generated by the simulator according to device structures provided by the users, and the self-adaptive mesh refinement procedure will be invoked to optimize the mesh whenever the speed-up of convergence rate is possible. The self-adaptive mesh requirement technique employed in SDA has eliminated the tedious mesh specification and has enhanced the program's efficiency substantially.

4.6 Some examples of Device Analysis

For purposes of illustration, the SDA program has been used to simulate GaAs MESFET device. The device dimensions and refined grid are shown in Fig. 1. Contour maps of potential distribution and three dimensional electron density distribution at several biases under thermal equilibrium condition are plotted in Fig. 2 and Fig. 3, respectively. Fig. 4 illustrates the external I-V characteristics obtained in this sample run, which demonstrated that this SDA simulator can effectively model semiconductor devices of arbitrary structures within a wide range of bias conditions, and can satisfy any user requirement.

4.7 Further Work

Revisions to the SDA-1A program are underway to include new function and models, such as hot electron models which are pertinent to devices with small size, and quantum well and bulk electron effects which are needed for HEMT simulation.

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