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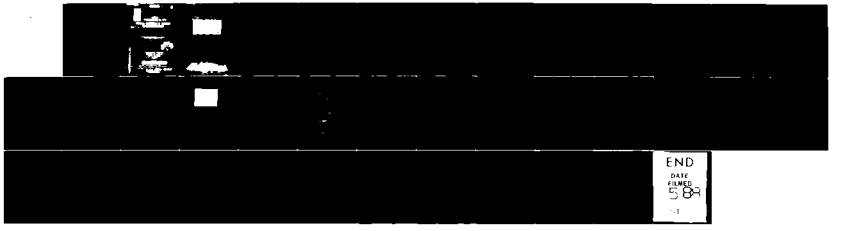

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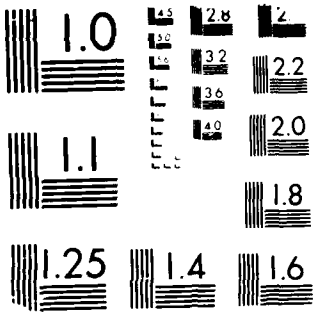

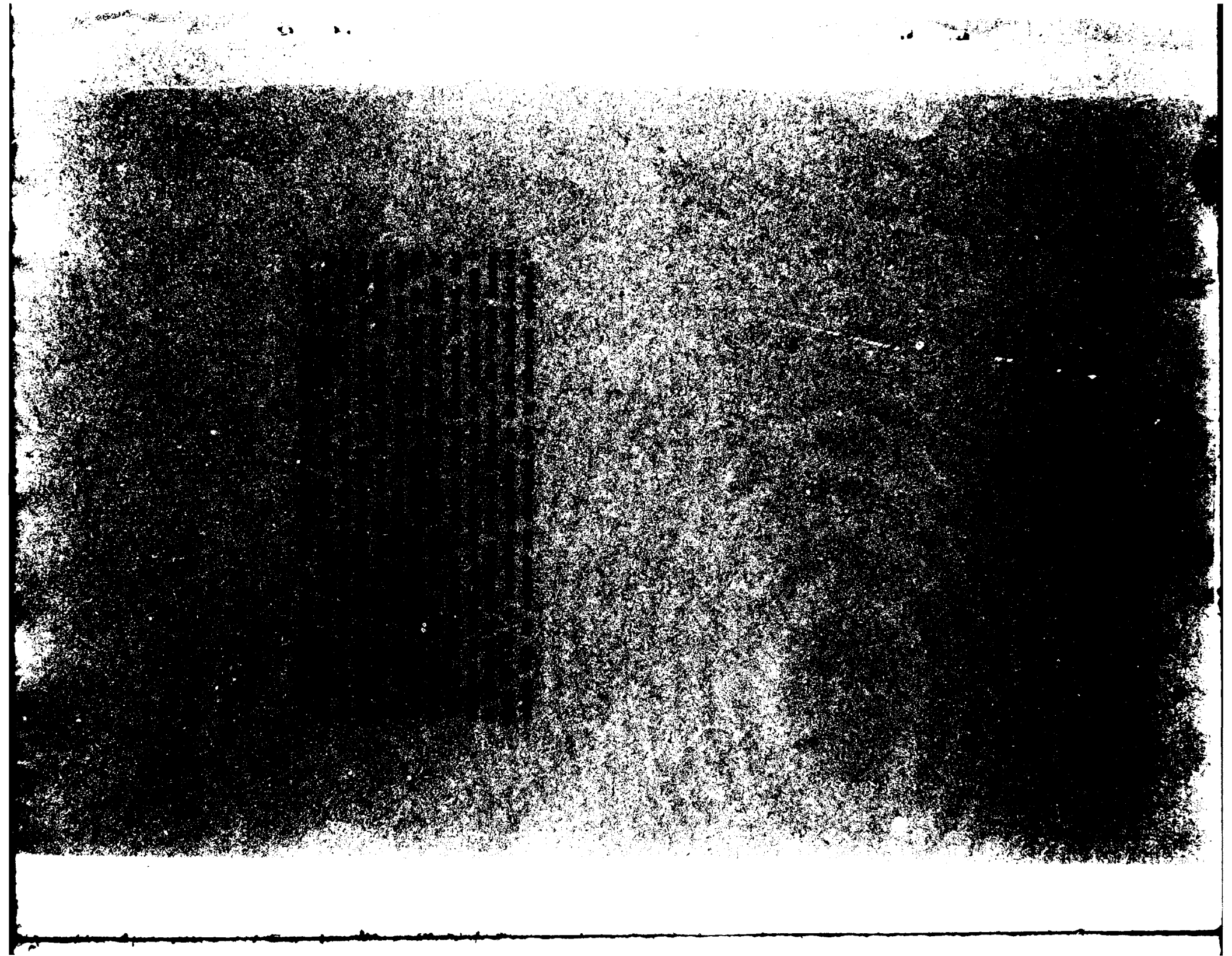

ROYAL SIGNALS AND RADAR ESTABLISHMENT

Memorandum 3672

TITLE: THE DESIGN, IMPLEMENTATION AND EVALUATION OF A FAST 100 MHz INTEGRATOR SYSTEM

AUTHOR: R D Edwards

DATE: October 1985

SUMMARY

A miniature unfocussed synthetic aperture radar has been designed at RSRE. The radar parameters required a video integrator with a high data rate capability. Plessey Research (Caswell) Ltd were engaged to design and develop a 100 MHz shift register based video integrator module. At RSRE a real time test and evaluation system has been developed in conjunction with a minicomputer. A special purpose high speed computer compatible buffer store was developed by Cambridge Consultants Ltd. At RSRE a design incorporating two integrators to provide phase and quadrature processing has been developed. Details of the systems operational concepts, performance and test results are discussed.

RSRE MEMORANDUM 3672

THE DESIGN, IMPLEMENTATION AND EVALUATION OF A FAST 100 MHz INTEGRATOR SYSTEM

R D Edwards

LIST OF CONTENTS

LIST OF FIGURES

LIST OF CONTENTS (Continued)

LIST OF FIGURES (Continued)

LIST OF APPENDICES

1 INTRODUCTION

A study of miniature high resolution synthetic aperture radars at RSRE[1] concluded that an unfocussed synthetic aperture radar (SAR) would meet a required specification. Such a radar is under design and construction. A narrow transmitted pulse with range sampling at 12.5 nanoseconds provides a range resolution of approximately 2 metres. Doppler analysis processing provides a similar azimuthal resolution by coherent integration of returned radar signals. The integration process gives a signal-to-noise ratio advantage to a radar which is peak power limited by a narrow pulse and high pulse repetition rate (prf). The first stage of the processing requires a video integrator capable of summing four successive radar returns for all 1024 range samples within each return. The integrator must be capable of continually integrating 4 radar returns but at the same time provide a bandwidth compressed output of each integrated result.

Three possible architectures for an integrator design were investigated with consideration given to compactness and low power consumption. The architectures were based on Charge Coupled Devices (CCD), Random Acess Memory (RAM) and Shift Register. From the three architectures two designs were followed up.

In the first instance a design based on CCD technology was chosen[3]. The complete integrator structure was contained on one integrated circuit. The analogue nature of the device dismissed the need for an analogue to digital converter. The design and fabrication of the CCD device was carried out "in house" at RSRE. Design and construction of suitable drive and control circuitry, together with suitable testing was carried out. The CCD device was found to be operable to the required data rate but problems with drift, poor linearity and a much higher than anticipated power consumption precluded its use in a real system.

The second architecture using RAM was not chosen because at that time devices were slow, had excessive power consumption and high speed addressing problems were envisaged.

Finally an elegant integrator design based around shift registers was chosen. A contract was placed with Plessey Research (Caswell) Limited[4] to design and develop the shift register based integrator consisting of an integrator module and logic control module.

The design was based around two custom designed integrated circuits, one, a fast adder implemented on a gate array, the other a 16 x 256 bit low power MOS shift register. The fast 8 bit adder is now available as a commercial integrated circuit.

Special facilities were provided at RSRE for test and evaluation of the digital integrator. Two methods of test and evaluation were designed and developed. The first method involved the design of the system control module (refer Figure 4). This provided a simple "stand alone" system to allow the integrators timing parameters to be checked and a variety of test waveforms to be examined. As a result of tests undertaken using this method modifications to the integrator system were necessary. The second method involved the design of an interface module (refer Figure 5) which, in conjunction with a special high speed buffer memory system designed by Cambridge Consultants Limited[2], has provided real time test and evaluation of the integrator using a NOVA 4X computer.

The computer test facility has allowed accurate assessment of the integrators performance and verified its operational specification. This led to the design of a dual integrator system. A new logic control module has been designed with the ability to drive two integrator moduels in parallel. This arrangement allows simultaneous processing of phase (I) and quadrature (Q) information necessary for complete processing of the radars data. This dual integrator is intended to be used in conjunction with the experimental miniature synthetic aperture radar system.

1.1 VIDEO INTEGRATOR ARCHITECTURES

Details including advantages and disadvantages of the three architectures are given below:

a. In the system based on high speed RAM (Figure 1a) three operations are required to take place in one clock period ie for a 100 MHz data rate then the period is 10 nS. The stages are as follows: the RAM must be addressed, then data read from the RAM must be added to the incoming data and finally the summed data written back to the RAM. This system is likely to require a high degree of multiplexing to achieve the required data rate. The complex addressing and probable multiplexing at high speed indicates a bulky power consuming system.

b. The shift register architecture provides a simple solution (refer Fig 1b) since only one operation is required per clock period. No complex addressing is required as with the RAM architecture. Providing the shift register is of the required length (1024 bits) and the input data blocks are the same length, then data clocked out of the register will automatically be added to the correct incoming data bits. When the required number of integrations are complete the data is transferred at the higher input data rate to a buffer register. Data can then be output at the slower rate during the integration period. Implementation requires a multiplexed system for speed and reduced power consumption.

c. The CCD architecture provides an ideal solution (refer to Figure 1c) with a large proportion of the processing carried out on-chip. There is no need for an A/D converter due to the inherent analogue design. Once the input buffer has been filled with data its contents can be transferred by a single parallel operation to the integrating register. After the required number of integrations, data accumulated in the integrating register is transferred to the output buffer. Data can now be read out at a slow rate from the buffer. An analogue to digital converter is provided for digital implementation of the integrated data. Multiplexing of three CCD devices is necessary to obtain the speed of operation. Although the CCD is a low power device, power is consumed in the drivers for the clock phases. The CCD and digital shift register technology are both MOS and the power consumption is proportional to the square of the voltage. The digital shift register has reduced operating voltage compared with 15V for the CCD giving a net reduction in power consumption. A further benefit of the digital register is the reduced number of clock phases, reducing power consumption and simplifying control logic design.

1.2 TIMING CONSIDERATIONS: SAR APPLICATION

For the unfocussed synthetic aperture radar application the required timing considerations are discussed as follows. Figure 2 shows that the integrator should be capable of adding 4 azimuthal returns for all ranges R_0 to R_n. Basic timing relationships for the radar application are given in Figure 3. A sample period of 12.5 nS (78 MHz) is required to maintain the specified range resolution ($\simeq$ 2 metres). 1024 range samples are therefore collected in 12.8 µs, range ambiguity being catered for by using a pulse repetition frequency (prf) of 16 KHz. Four integrations therefore take a total time of 250 µs. Allowing for data transfers within the integrator system then 205 µs is available for the slow readout of 1024 data samples ie 5 MHz data rate.

Evaluation of the shift register integrator by two methods is given in section 4. The "stand alone" test system emulates the radars timing (refer Figure 3) and operating conditions as described above. Experimentation has shown that by deriving all controls including the radar timing from a single master clock source (ie a synchronous system) provides stable, jitter free operating conditions. If asynchronous timing relationships are used, as with the computer test system (see Section 4), then problems occur and synchronising of all commands must be undertaken for a stable operating environment.

2 RSRE CCD VIDEO INTEGRATOR

The introduction of CCD devices at RSRE allowed an ideal architectural design for a high speed integrator. The architecture of the device is described in Section 1.2 with reference to Figure 1c. Sections 2.1 and 2.2 cover detials of the CCD design and peripheral circuitry necessary for its operation. Results of the integrators performance are discussed. Although an ideal design in theory, problems with devices and high power consumption in drive circuitry led to the implementation of the digital shift register approach.

2.1 THE CCD INTEGRATOR SYSTEM

The architecture has been previously described in Section 1. To attain the required data rate three CCD devices must be multiplexed together. Data is transferred within the device by a 3 phase clocking system. Therefore 3 sets of 3 phase clocks for controlling the input buffer, parallel transfer and output buffer for each of the CCD devices is needed (refer Fig 1a). A block diagram of the integrator system is given in Figure 6. The logic control board contains all the required functions for controlling the system in a "stand alone" mode enabling emulation of the system timing requirements as shown in Figure 3. All the necessary sets of clock phases are generated by the clock phase generation board which is under control of the logic control board. By correct phasing of the three devices A, B and C the input data is automatically demultiplexed. The same is true for multiplexing the slow readout from the devices. Due to mismatching between individual CCD devices variable gain and offset controls are provided to aid correction. The output signal is superimposed on one of the clock phases and this must be subtracted with the aid of an output sampling clock. For digital implementation a sample-and-hold and 8 bit A/D converter are provided.

2.2 INTEGRATOR EVALUATION AND PERFORMANCE

The integrator system has successfully operated up to data rates of 78 MHz. Some test waveforms are shown in the Appendix 2. Although the required operating speed has been met a number of problems exist, some of them are discussed below. The CCD devices themselves suffered from poor linearity and limited dynamic range. Poor charge transfer efficiency was noted with some devices. A large number of control voltages are needed for each CCD device, all of which must be individually set, these voltages need ocassional adjustment due to the poor temperature stability of the CCD devices. For a multiplexed system the CCD devices were required to be matched, this constraint was difficult to meet. The power consumption of the system was in the region of 23 watts, considerable power being consumed in the drivers necessary for the large number of clock phases each of which has a high capacitance. Second generations of the CCD showed no particular improvements in characteristics.

3 PLESSEY DIGITAL INTEGRATOR MODULES

The digital video integrator was contracted for design and development by Plessey Research (Caswell) Ltd. Two modules were constructed, each module is contained on a double eurocard printed circuit board. Details of these two modules are given in Sections 3.1 and 3.2.

3.1 DIGITAL VIDEO INTEGRATOR MODULE

With reference to Figure 7 the basic concept of the integrator can be observed. 1024 data samples pass via the adder to be stored in the summation shift register. The next 1024 data samples input to the adder are in turn added to data samples fed back from the previous data samples stored in the summation shift register. This process is repeated to give a summation of successive 1024 blocks of data samples. After the appropriate number of summations or integrations, clocking of the buffer shift register is made coincident with that of the summation shift register. The summed data samples stored in the buffer shift register

can be accessed by clocking the buffer at the required output data rate. A new integration sequence is performed by zeroing data fed back to the adder during the first 1024 new data samples.

Actual implementation is more complex then the basic concept described above. Demultiplexing of the input data allows high integration speeds to be achieved using slower, low power MOS shift registers. The demultiplexing arrangement is shown in Figure 8. Data is demultiplexed into 4 identical integrator channels, each operating at 25 MHz data rate, their operational concepts being similar to those described above. The adders are specially designed integrated ciruits based on gate array technology using emitter coupled logic families (now commercially available as SP9218 latched adder). Three sets of latches are provided within the adders which allow demultiplexing, de-skewing and re-timing of the input data. This makes all 4 channels identical, allowing common clocking and timing for integrator and buffer shift registers. Specially designed low power shift registers with a 16 x 256 bit format were used, sharing one register between two channels. On completion of the integration cycle the contents of the integrator are transferred at high speed to the buffer memory. Data is read from the buffers and multiplexed to provide an output data rate of 5 MHz, with a block length of 1024 and dynamic range of 8 bits. The multiplexing function is accomplished in the MOS shift register buffers which have the multiplex function built into their output. Data can be input in 4 bit digital form or via a Plessey SP9754 analogue to digital (A/D) converter. A power saving feature of the integrator is the ability to power down the ECL adders during inoperative periods, ie the dead times between data input cycles.

3.2 LOGIC CONTROL MODULE

The hardware to carry out the integration process is contained on the digital video integrator module. Various addressing and clocking signals are required for its operation, these are derived on the logic control module. Control of the integrator system is by a set of simple commands input to the logic control module (refer Figure 9).

The logic control module is described with the aid of Figure 10. The high speed section is designed using ECL devices, the rest of the circuitry using standard TTL series of logic components. A fast clock of 100 MHz is suitably delayed to allow precise timing relationships between addresses, system clocks and latch controls. The demultiplexing function shares the input data between four separate but identical channels, the demultiplexer address being produced from a 4 phase generator. A suitably delayed divide by 4 version of the 100 MHz input clock is translated to drive circuitry designed using TTL logic families. Each MOS shift register is capable of a 25 MHz data rate. The design of the shift register requires a 4 phase clocking system because a further 4 way demultiplexing takes place on chip.

The input data and output data commands are asynchronous, to reduce possible edge discrepancies they are synchronised with the system clock. The input data command causes 257 clock cycles to be counted, from this clock burst 4 phases are generated to form the integrator memory clocks. A separate 5 MHz clock controls the output data rate. The output data command causes 1024 clock cycles to be counted, a 4 phase control is generated from this clock burst to carry out the multiplexers tristate

commands. The buffer memory clocks are derived from a fast burst of 256 clock cycles of the integrator memory clock followed by a slow burst of 256 slow clock cycles derived from the 5 MHz clock input. The master reset command is asynchronous and is synchronised with the system clock before resetting the appropriate logic components of the logic control module. The three user commands are described below.

a. Input data - causes a new block of data to be read in.

b. Integrator reset - causes the first integration of a new block of data, at the same time the result of the previous integration is read into the buffer memory. This command must be coincident with the input data command.

c. Output data - causes a block of data to be read out.

4 RSRE MODULES AND CONFIGURATION

The test system has been constructed in a modular form allowing two different systems to be configured, namely "stand alone" and "computer testing". The "stand alone" test facility (refer to Figure 4) requires four modules for complete operation, full control is provided by the system control module. This test system is most suited for checking and evaluation of circuit detail using an oscilloscope and logic analyser. The computer test facility (refer Figure 5) provides a method for detailed evaluation of complicated data waveforms via control of the computer. Further details of the modules are given in Sections 4.1 to 4.3.

4.1 SYSTEM CONTROL MODULE

The system control module was designed to provide basic commands to operate the integrator system in a continuous mode. This mode of operation provides almost identical operating commands and data rates required for the SAR application. The inputs to this module are a fast (variable up to 100 MHz) continuous clock and a manually operated master reset command (refer Figure 11). The design derives its commands in a synchronous manner from the fast input clock. This provides the required stability for examination of data paths and timing parameters for the integrator system. A maximum of 16 integrations is allowed with this test system.

The design incorporates 10,000 series emitter-coupled-logic (ECL) for the fast counting section and transistor-transistor-logic (TTL) for the rest of the circuitry (refer Figure 12). A manually derived reset enables monostabled pulses for master resetting of the system. Once reset, the system should function without further attention but resetting at regular intervals would be a wise precaution. During the reset period the fast clock is disabled to allow for correct phasing of the systems ECL circuitry. The fast clock is divided by a synchronous counter chain from which the slow clock and a pulse at the data period (20.48 μs) are derived. These ECL derived waveforms are translated for TTL compatibility. The pulse at the input data period is divided by 16 and gated to produce the integrator reset command. A variable length counter allows "N" integrations to be performed via the input data command. The output data command is produced one input data period after the integrator reset (this allows time for data transfer

to the SR buffers). The nominal output data period is 205 μs although a maximum of 307 μs is available with this system. Data input trigger is an output command for synchronisation of externally generated data. For examination of results in analogue form a latch and 8 bit D/A converter are provided. Latch and converter commands are derived from the slow clock.

4.2 INTERFACE MODULE

The interface module links the integrator system to the fast buffer store. The interface module provides buffering/driving facilities, generation of user commands for control of the integrator and level shifting for incompatibilities in logic levels (refer Figure 13). A block diagram of the interface module is shown in Figure 14. The integrator system uses a common +5 V for both TTL and ECL, the buffer store uses +5 V for TTL and -5.2 V for ECL. This incompatibility was overcome by floating the system power supplies with respect to the buffer power supplies allowing the fast ECL families to be compatible. The slower TTL families were level shifted for compatibility. Buffers were used for both transmitting and receiving data channels between the buffer store and the integrator module. The three user commands, integrator reset, input data and output data are derived by gating the STRT, CLEAR and IOPLS controls from the buffer store. Timing relationships for these commands/controls are shown in Figure 15. Synchronisation of data is maintained by using a master clock which is common to both the integrator system and the buffer store.

4.3 FAST BUFFER STORE/NOVA 4X COMPUTER

The fast buffer store was custom designed by Cambridge Consultants Limited[2] and is housed in the main frame of the computer. Data may be written to or read from the buffer store via the computer, likewise data may be externally written to or read from the buffer store. The buffer store consists of a 2K * 8 bit block of high speed memory which is used for both read and write operations. The various modes of operation of the buffer store are controlled by a set of software subroutines, the subroutines were developed in assembler code and are presented as FORTRAN subroutines for easy incorporation into larger programs. The buffers mode may be set, for example, to read or write any number of samples from 1 to 2048 in a continuous or single block mode using analogue or digital data ports with an internal or external clock. Data may be output as 8 bit bytes up to 100 MHz rates or in analogue form via an 8 bit 10 ns D/A converter. Data may be intput as an 8 bit byte or via a 6 bit A/D converter at rates up to 100 MHz.

5 TEST AND EVALUATION OF THE DIGITAL INTEGRATOR

There are two specific test procedures, the first of these (bench testing) was devised to check timing relationships and evaluate the data path of a single input waveform. At this stage modifications and redesign were implemented before the second method of testing was undertaken. The second method of testing (with a NOVA 4X computer) provided the ability to implement complicated test waveforms and fast and accurate evaluation of results. Greater detail is covered in Sections 5.1 to 5.3.

5.1 BENCH TESTING

Bench testing was devised for checking timing parameters and data paths of simple input waveforms, whose configuration is shown in Figure 4. Basic timing relationships were examined and some fine adjustments were made using the 1 ns variable delay on the logic control module. The first simple test carried out was to fill all 1024 points within an integration block with a fixed value ie a number between 0 and 15. The results were checked with the aid of an oscilloscope and logic analyser. At this stage problems with the integrator system were evident. Modifications were made before a digital ramp that counted continuously from 0 to 15 was input to system. Further modifications and redesign were necessary before the integrator system could be made operational. Having achieved basic operation of the integrator the 4 bit A/D was commissioned. After some adjustments the A/D converter appeared to operate correctly. As a guide to correct operation the analogue output of the D/A converter, contained on the system control module, was examined for a variety of triggered input waveforms. The integrator system was now considered suitable for thorough testing in conjunction with the NOVA 4X computer. Some of the modifications and redesign are given in Appendix 3.

5.2 TESTING AND PROGRAMMING WITH THE NOVA 4X

The computer test facility has enabled real time evaluation of complicated test waveforms. The test system is configured as shown in Figure 5. A suite of programs has been developed using FORTRAN V programming language. Control of the buffer store is achieved using a set of FORTRAN subroutines which have been developed from assembler code. Two flow charts are shown in Figures 16 and 17, the first of these shows a simplified test procedure, the second indicates the form of the final test program. Four test waveforms, pulse, square wave, sine wave and ramp were software generated with the ability to set their periodicity, amplitude and DC offset parameters. A sequence of random noise points was generated as a test waveform with the ability to be added to the four waveforms above. Digital data was input to the integrator in 4 bit byte form. Results were verified by a software error check of the integrated result. Analogue data was generated from 8 bit bytes via the buffer stores D/A converter. This gave a very accurate analogue quantity for processing by the integrators 4 bit A/D converter. Further results are given in section 7.

6 DUAL INTEGRATOR DESIGN

For correct processing of the radar data both phase (I) and quadrature (Q) information must be catered for. This requires individual integrator modules for the I and Q channels. The integrators are identical and operate in parallel. The dual integrator design forms the basis of a system to be used in an experimental radar system. The dual integrator system consists of a dual logic control module and two integrator modules. For test and evaluation a system control module and test data module are added (Figure 18). Each module is built on a double eurocard printed board. Further details are given in sections 6.1 to 6.3.

6.1 DUAL LOGIC CONTROL MODULE

The dual logic control module is an extension of the existing logic control module but does include new design ideas. The basic design is similar to that of Figure 10 but includes extra circuitry to drive two integrator modules. This is in the form of buffering and duplication of clocks and control signals. A new PCB design for this module incorporates these changes. Included are modifications mentioned in Appendix 3. One of the design features has been to allow a reduced range swath to 256 samples. These 256 range samples may be windowed anywhere within the nominal 1024 range samples. This reduction in data swath by a quarter has similarly allowed the same reduction in output data rate. This temporary measure has been necessary for the experimental radar link which at present is unable to cope with the full data rate.

6.2 SYSTEM CONTROL AND INPUT DATA MODULES

The system control module is unchanged in design and can easily cope with the extra commands for the dual logic control module. The input data modules provide two sources of input data. Available is a 4 bit data ramp or a 4 bit wide pulse, both are generated from ECL counters which are clocked by the system clock.

6.3 TESTING THE DUAL INTEGRATOR

Whilst computer evaluation can be conducted on individual modules the dual integrator system cannot be simultaneously tested in conjunction with the computer. The dual system has therefore been constructed with individually tested modules. The waveforms generated by the input data modules have been used to give final checks on timing and speed of operation. Minor adjustments may be necessary in timing to allow for variations in propagation delays between the two channels.

7 RESULTS AND PERFORMANCE

The results and performance are presented in three sections. These sections cover the digital and analogue results of individual integrator systems and results of the dual integrator system.

a. 4 Bit Digital Input

The tests carried out in section 3.3 have proven the ability of the integrator to operate error free with input data rates of up to 92 MHz. The use of random noise as an input has also shown error free results. This frequency of operation was shown to be a maximum for error free operation with all variations of testing. Increasing the frequency of operation, hence increasing the input data rate, to 100 MHz produced LSB errors (under 1%). A detailed examination showed that LSB errors occurred on large negative transitions, this was shown by using pulsed and maximum amplitude square wave data inputs. This error due to the negative edge was shown to accumulate N times with N integrations indicating an input mismatch rather than an error in the integration process. System timing is very critical at these rates of operation, a mismatch in input data latches is the most probable source of error.

b. Analogue Input Data

Results using digital data showed error free operation to 92 MHz therefore analogue data was limited to this rate to be sure of error free testing. Initial tests showed noise in the order of LSB errors. Repeating the tests showed similar noise problems and evidence of a dc drift. Stabilisation and smoothing of the analogue to digital converter reference source has cured the noise and drift problems. Accurate setting of the analogue input range can now be accomplished. The resulting changes has allowed accurate results to be obtained with analogue data to 87.5 MHz data rates. Occasional errors are sometimes detected and are thought to be caused by noise on the analogue signal which are processed by the flash analogue to digital converter. The data rate may be increased to a maximum of 96 MHz with increased errors but above this rate complete failure is exhibited.

c. Dual Integrator

Due to reasons given previously the dual integrator system could not be simultaneously tested using the computer test facility. Tests using a digital ramp and pulse have shown satisfactory operation to data rates of 85 MHz. The input of analogue data provided satisfactory operation to data rates of 85 MHz. Timing parameters have been optimised for each integrator for simultaneous operation around a nominal 78 MHz data rate.

8 CONCLUSIONS

A high speed test and evaluation facility, with the ability to cope with data rates up to 100 MHz, has been successfully developed incorporating the use of a NOVA 4X minicomputer. The CCD video integrator has met the specified data rate of 78 MHz but problems, as described earlier in this Memorandum, prompted development of a digital video integrator system that has been developed and, with modification and redesign, proved to operate with both digital and analogue signals at data rates exceeding the nominal 78 MHz radar data rate. A dual integrator system has successfully been developed for use in an experimental radar system.

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3 R D Edwards et al, A CCD Video Integrator, 5th International Conference on Charge Coupled Devices, September 1979.

4 D Jarvis, A J Fryers, A Digital Integrator, Plessey Research (Caswell) Ltd, Contract No A54A/677 MOD.

APPENDIX 1

SPECIFICATIONS FOR CCD AND DIGITAL INTEGRATORS

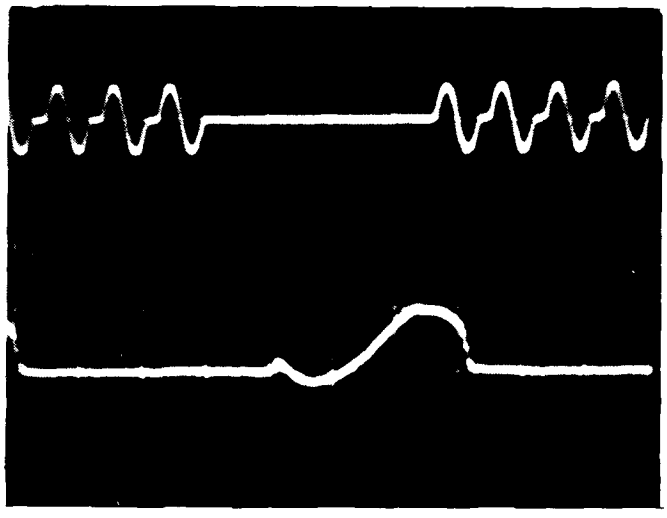
CCD System

Min No integrations	4
Max sample rate	100 MHz
Max output data rate	5 MHz
Data block length	765
Analogue input range	1 V
Analogue output range	1 V
Digital output	8 bit A/D
Power consumption	10 Watts
Power supplies	+5 V +10 V +11 V +5 V -5.2 V
Module format	Double Eurocards

Digital System

Min No integrations	4
Max input data rate	100 MHz
Max outut data rate	5 MHz
Data block length	1024
Input word length	4 bits
Max integrated word length	8 bits
Analogue input	4 bit A/D
Total power consumption	10 Watts
Power supplies	+15 V + 5 V
Module format	Double Eurocards

APPENDIX 2



Input/Output waveforms for 78 MHz input sample rate and
4.3 MHz output sample rate for CCD integrator system

APPENDIX 3

MODIFICATIONS AND REDESIGN

Testing procedures revealed necessary modifications and redesign, the main corrections are described below:

a. An intermittent count of 257 in the logic control board was traced to a glitch which was removed by the addition of a short delay.

b. The integrator master reset did not always work allowing the system to be reset into an illegal state. Synchronising the reset pulse with the system clock and extending its function to other logic components has produced a reliable reset command.

c. The MOS shift registers are of a dynamic type and only 1 ms is allowable before a refresh is needed. Although the operation of the registers was kept within these bounds a tendancy for the register to draw excessive currents from its 4 phase clocking system was noted if left in certain steady states of clock phase. The reason for this is not fully understood but the problem only occurs in the buffer stage and not in the fast integrator stage. Various avenues were investigated but has temporarily been cured by clocking data in the buffer 256 times rather than 257 hence keeping the stopped clock phase in a state in which the system is stable.

d. An error on the integrator PCB design had joined two output bits of an ECL adder together effectively giving a "wired" or "function", causing some integrations to be correct and others incorrect. A modification to the printed circuit board has resolved the error.

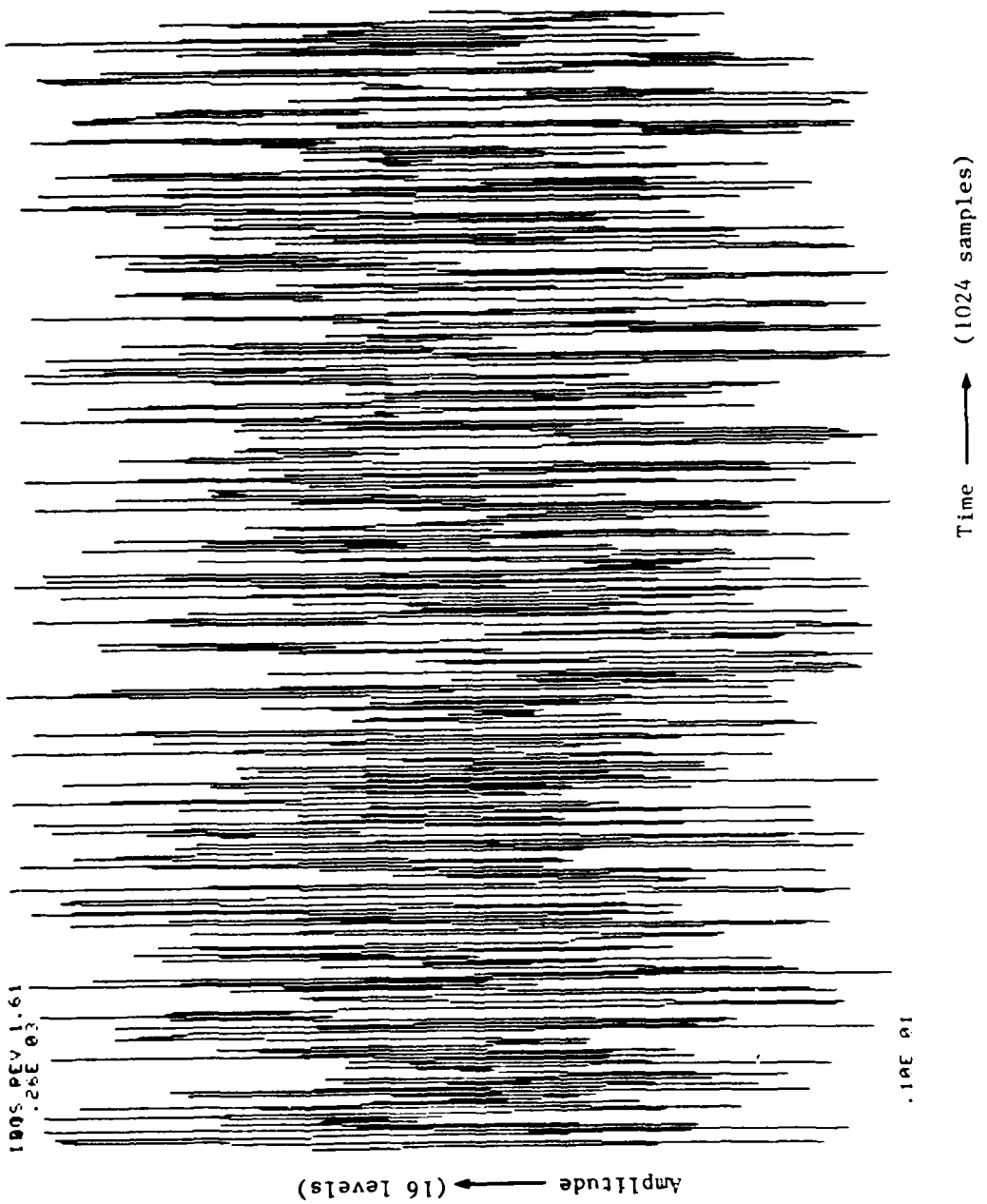
e. To allow the frequency of operation to be varied easily it was necessary to derive the demultiplex clocks, A/D convert control and A/D converter latch within the same 10 ns period.

f. Synchronisation of the master reset had been carried out but it was found after using the system with the computer that synchronisation of the asynchronous input data commands was necessary. This did not show up with bench testing due to their synchronous derivation from the system clock.

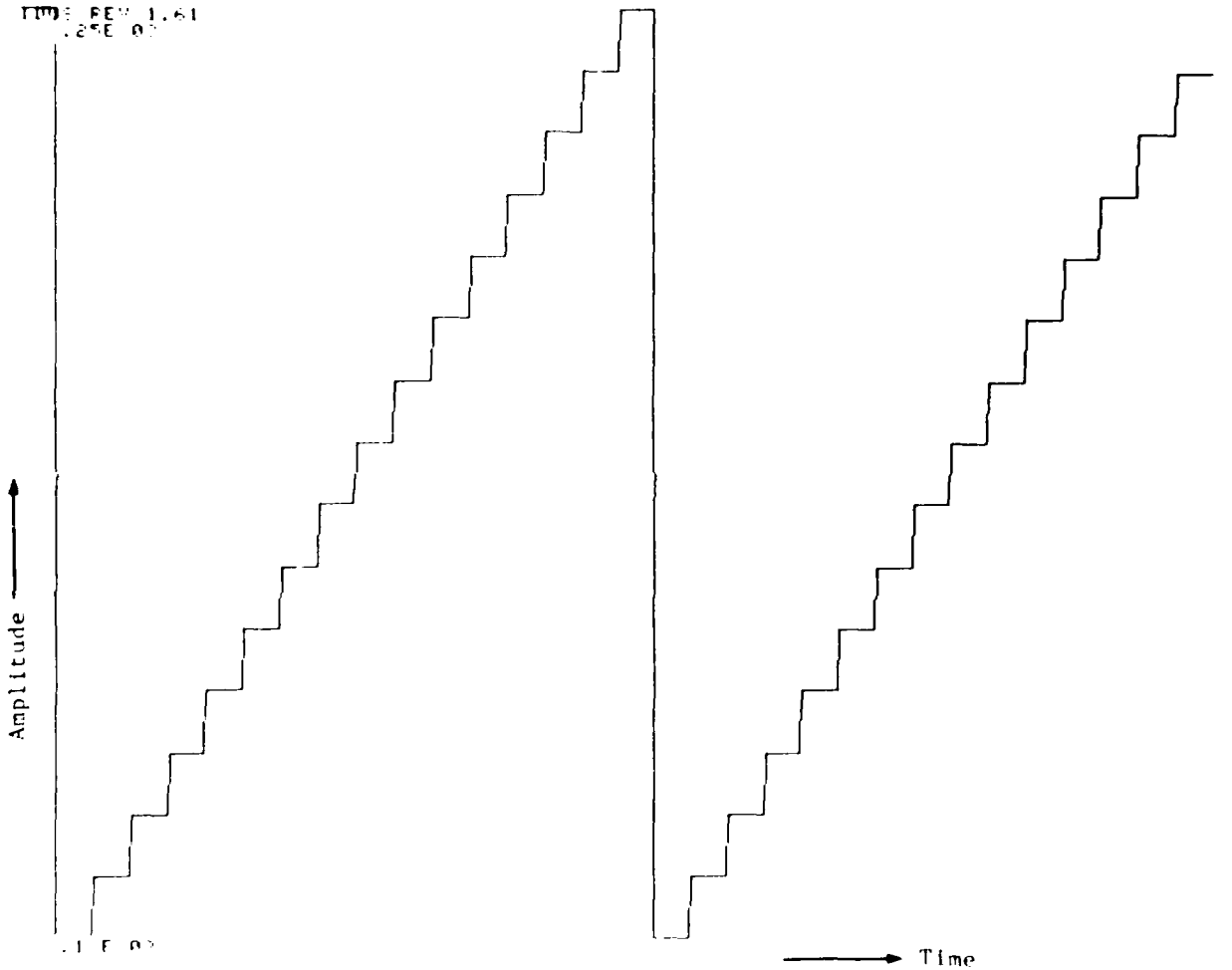
g. Problems with noise and drift with the A/D converter was noticed, this was cured by extra smoothing and deriving the voltage for the reference chain from special purposes stable reference voltage source.

h. Modifications and redesign has involved a new PCB for the integrator board. A new PCB board has been designed for the logic control module, this has included necessary modifications and redesign to allow operation of the dual integrator system and for coping with changes in data rates and fewer range samples.

APPENDIX 4



Noise Test Waveform for Digital Integrator



90 MHz input data rate, 4 integrations, period = 16

Ramp test result for digital input

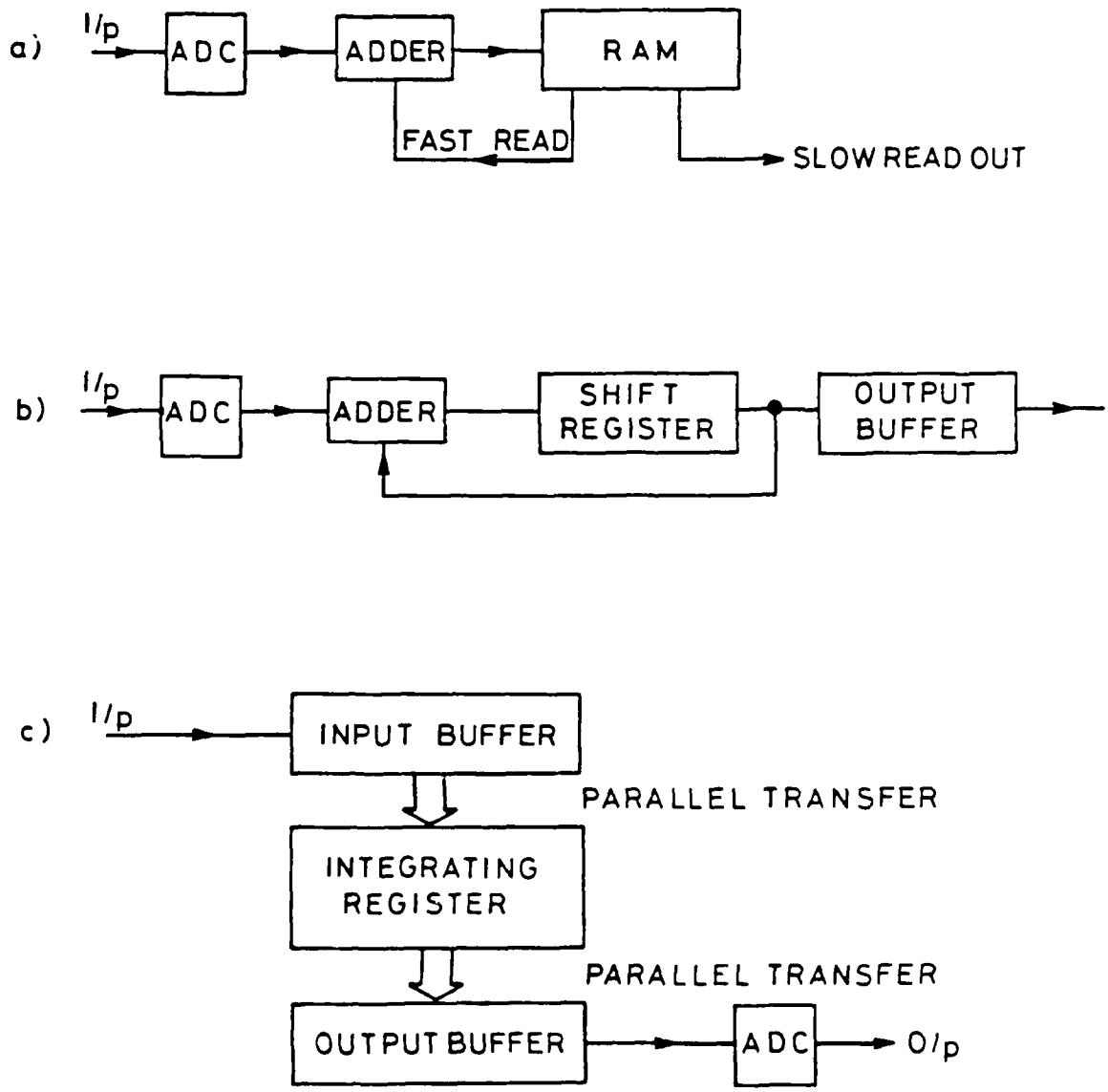
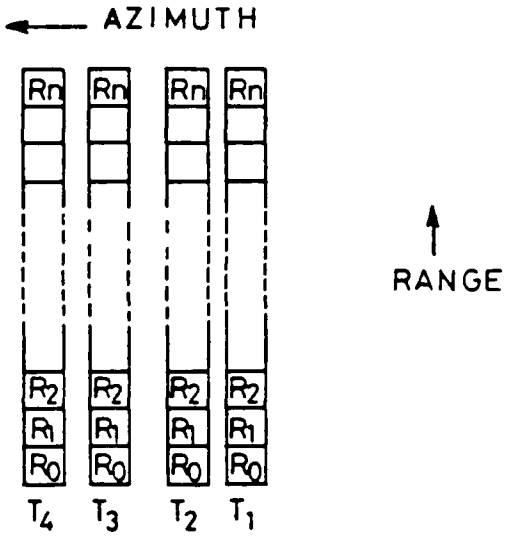


FIG.1 VIDEO INTEGRATOR ARCHITECTURES



THE INTEGRATOR SHOULD BE CAPABLE OF ADDING : —

$R_0(T_1) + R_0(T_2) + R_0(T_3) + R_0(T_4) = \text{RESULT } R_0$

$R_1(T_1) + R_1(T_2) + R_1(T_3) + R_1(T_4) = \quad " \quad R_1$

$Rn(T_1) + Rn(T_2) + Rn(T_3) + Rn(T_4) = \text{RESULT } Rn$

WHERE n = N° RANGE GATES

T_1 to T_4 RADAR RETURNS

FIG. 2 APPLICATION

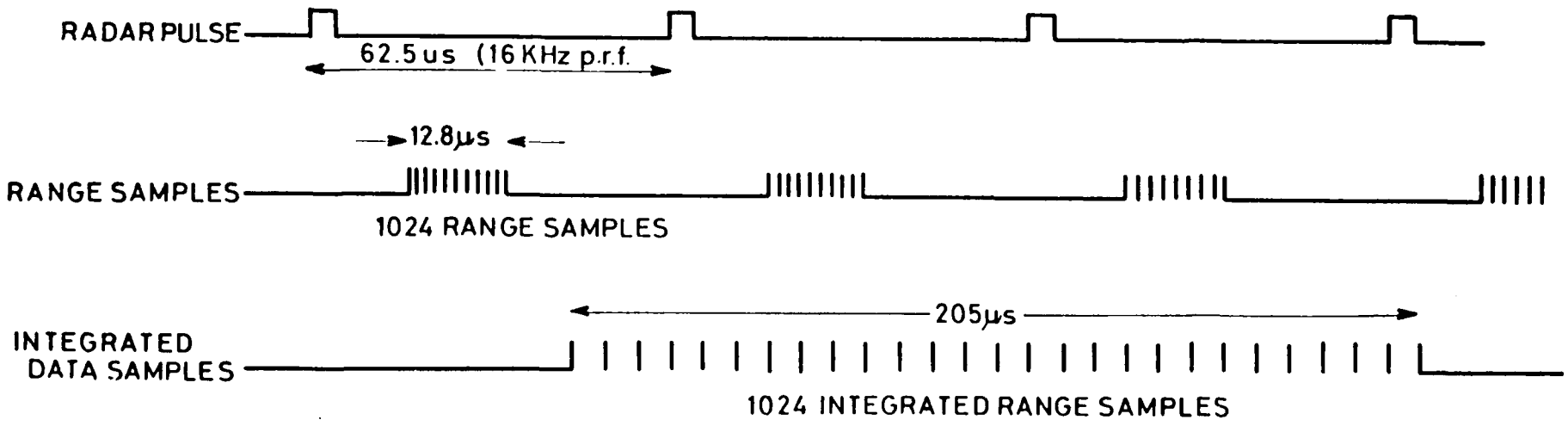


FIG.3 TIMING CONSIDERATIONS : SAR APPLICATION

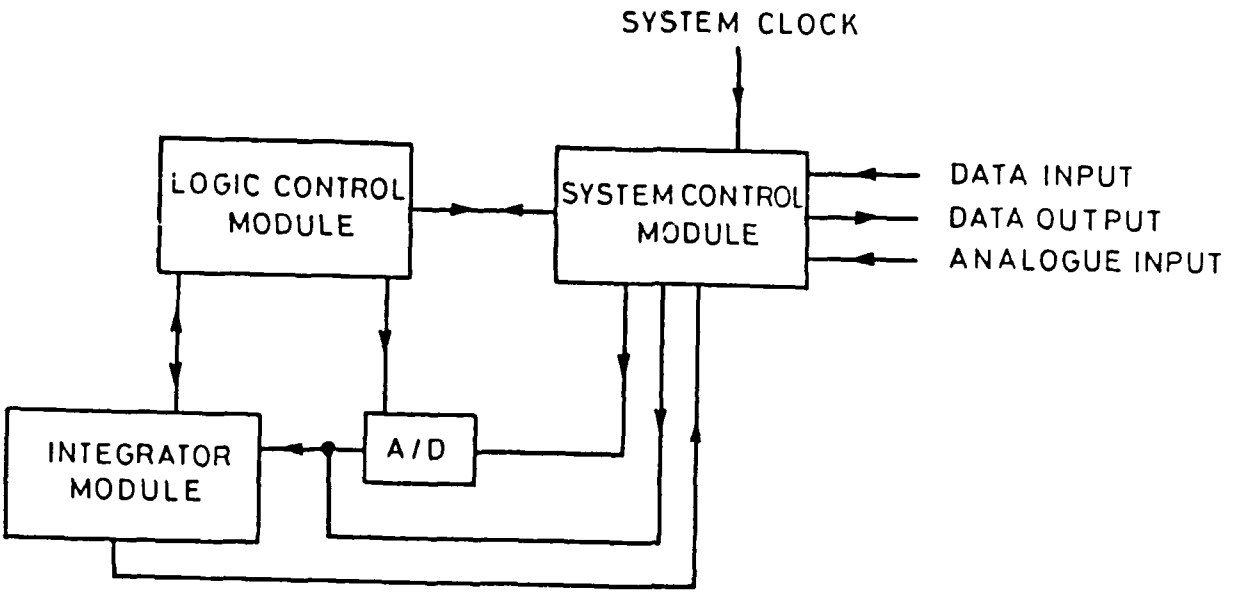


FIG. 4

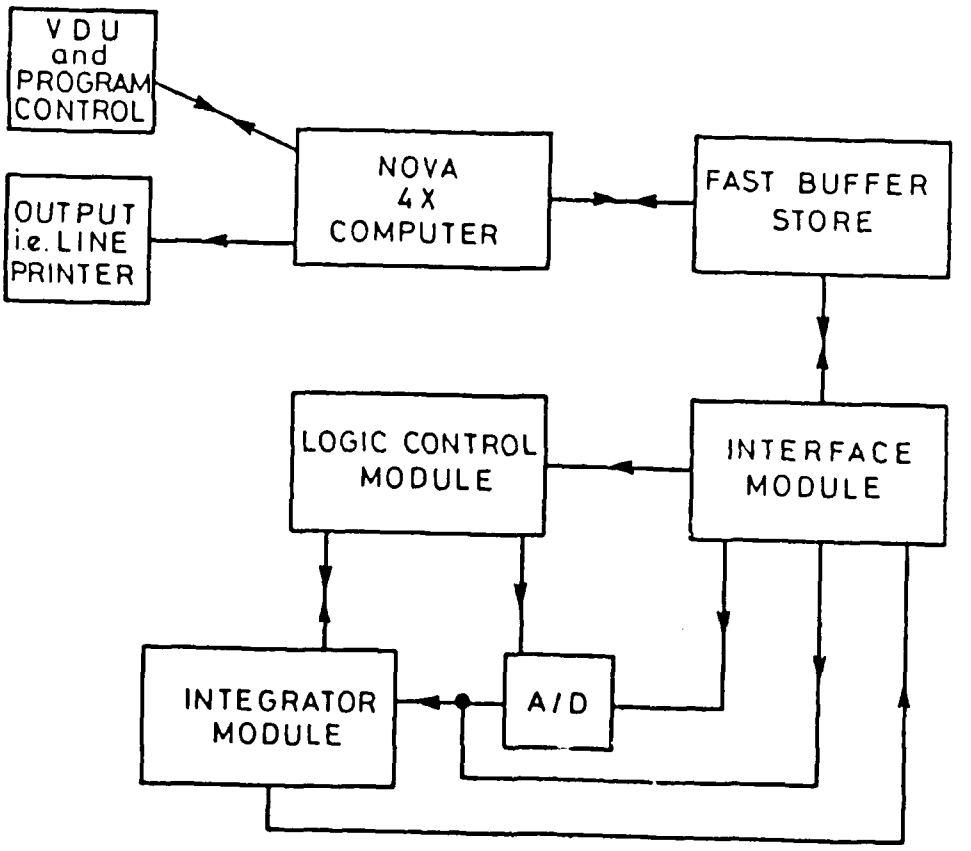


FIG. 5 COMPUTER TEST FACILITY

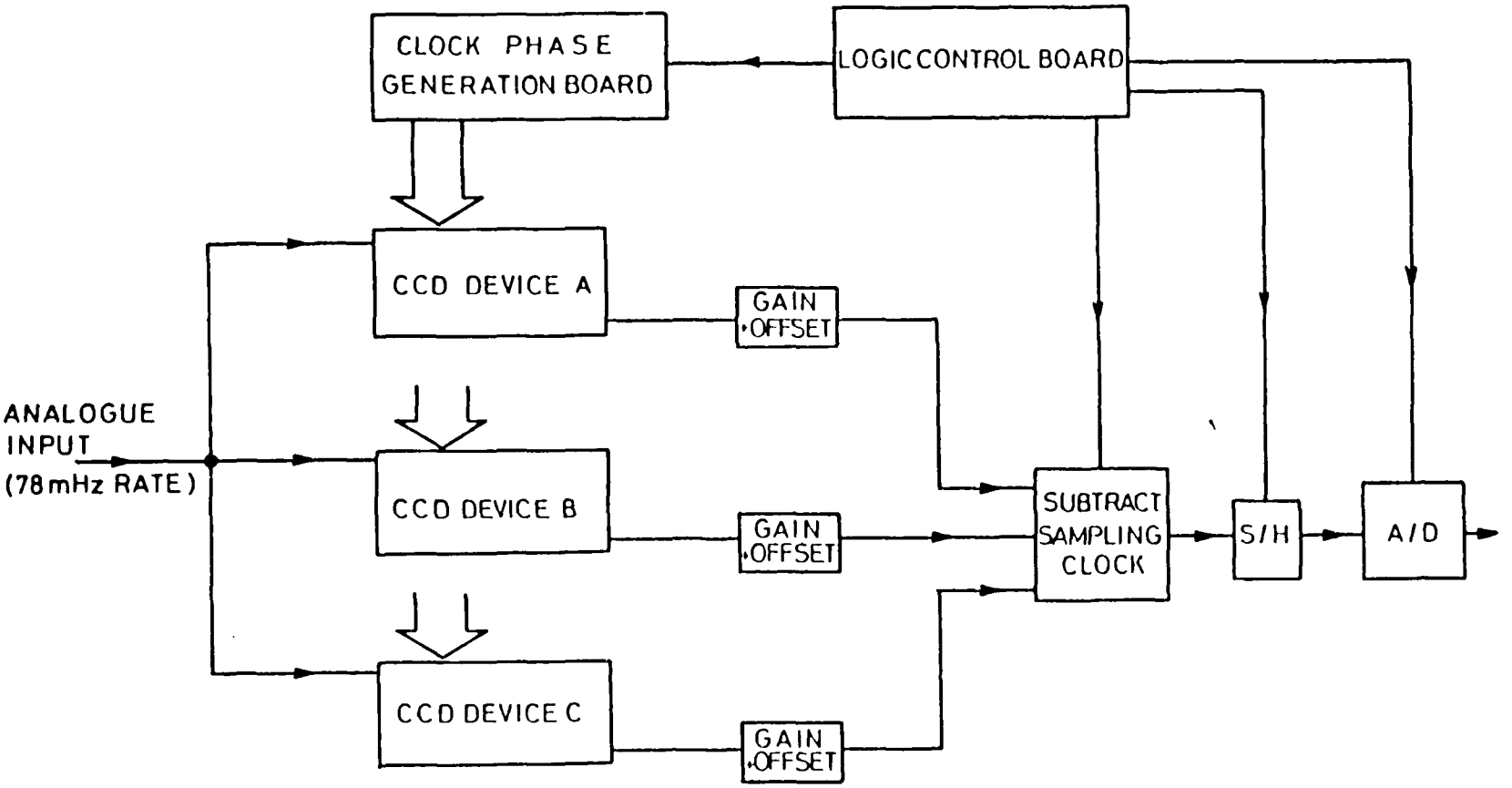


FIG.6 CCD INTEGRATOR SYSTEM CLOCK DIAGRAM

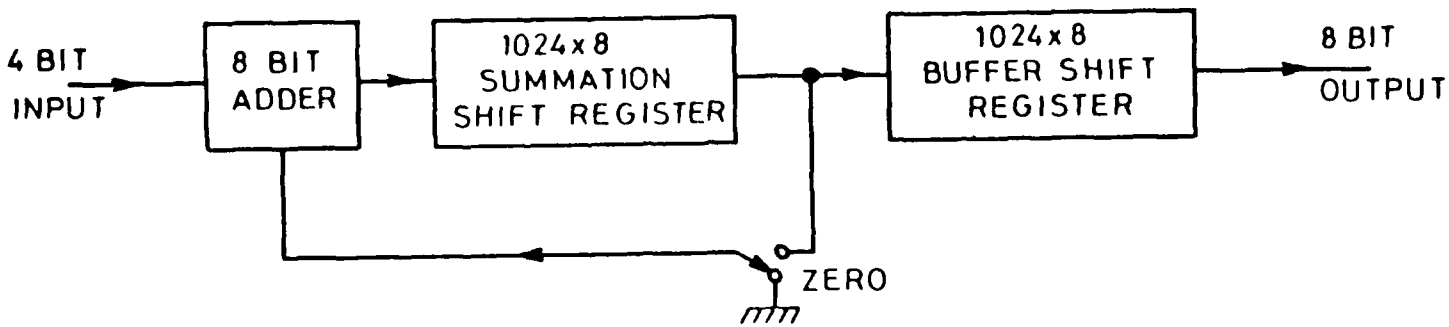


FIG.7 BASIC INTEGRATOR

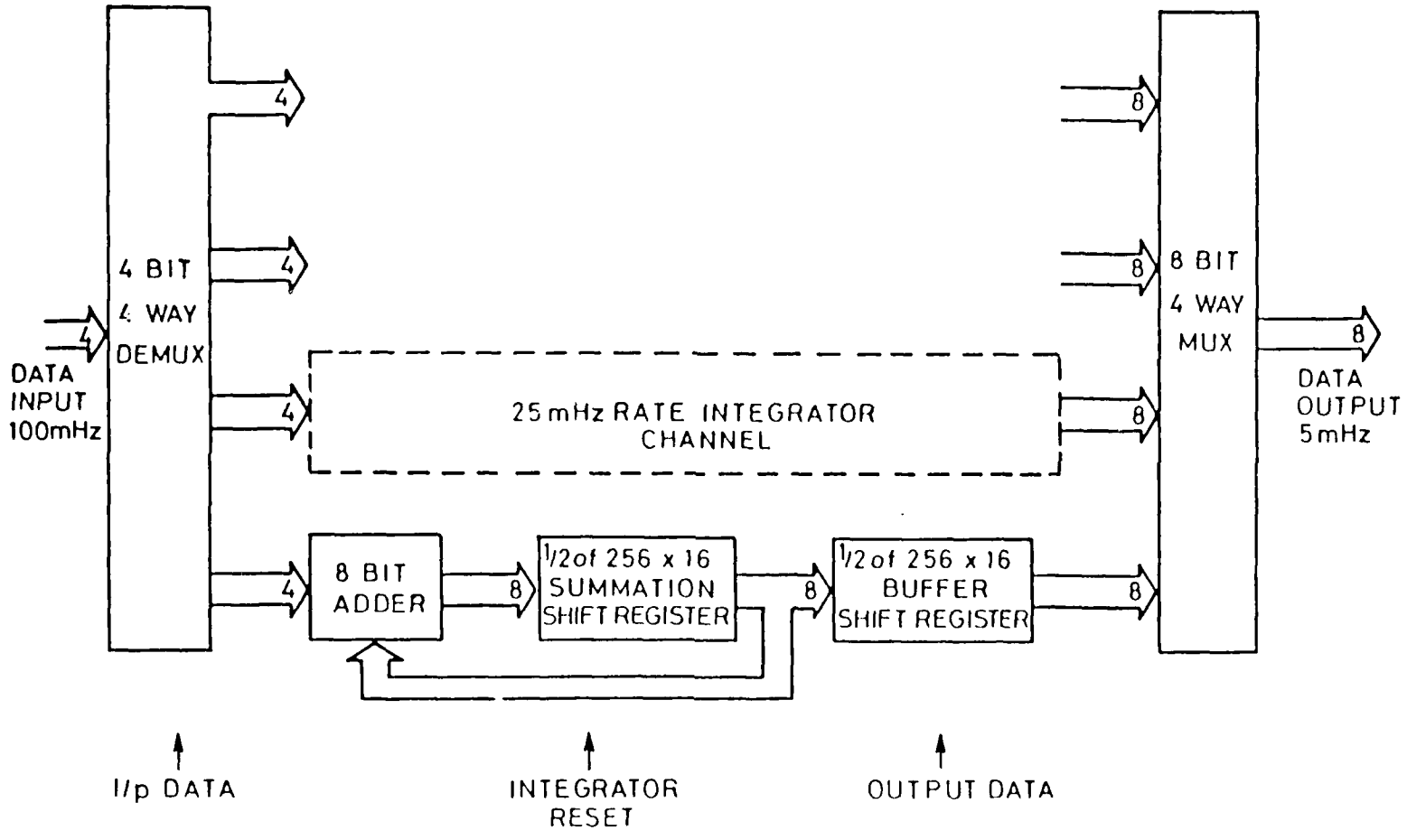


FIG.8 VIDEO INTEGRATOR BLOCK DIAGRAM

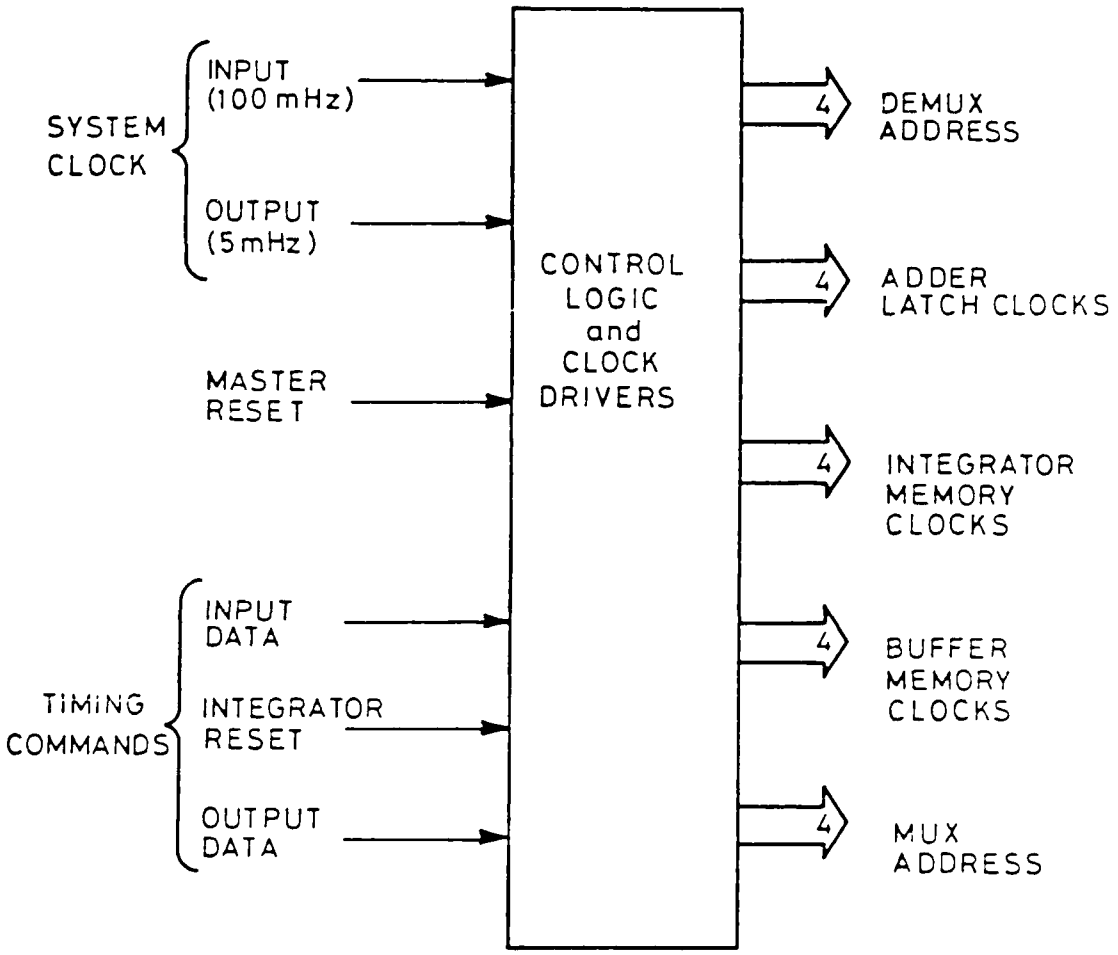


FIG. 9 LOGIC CONTROL MODULE COMMANDS

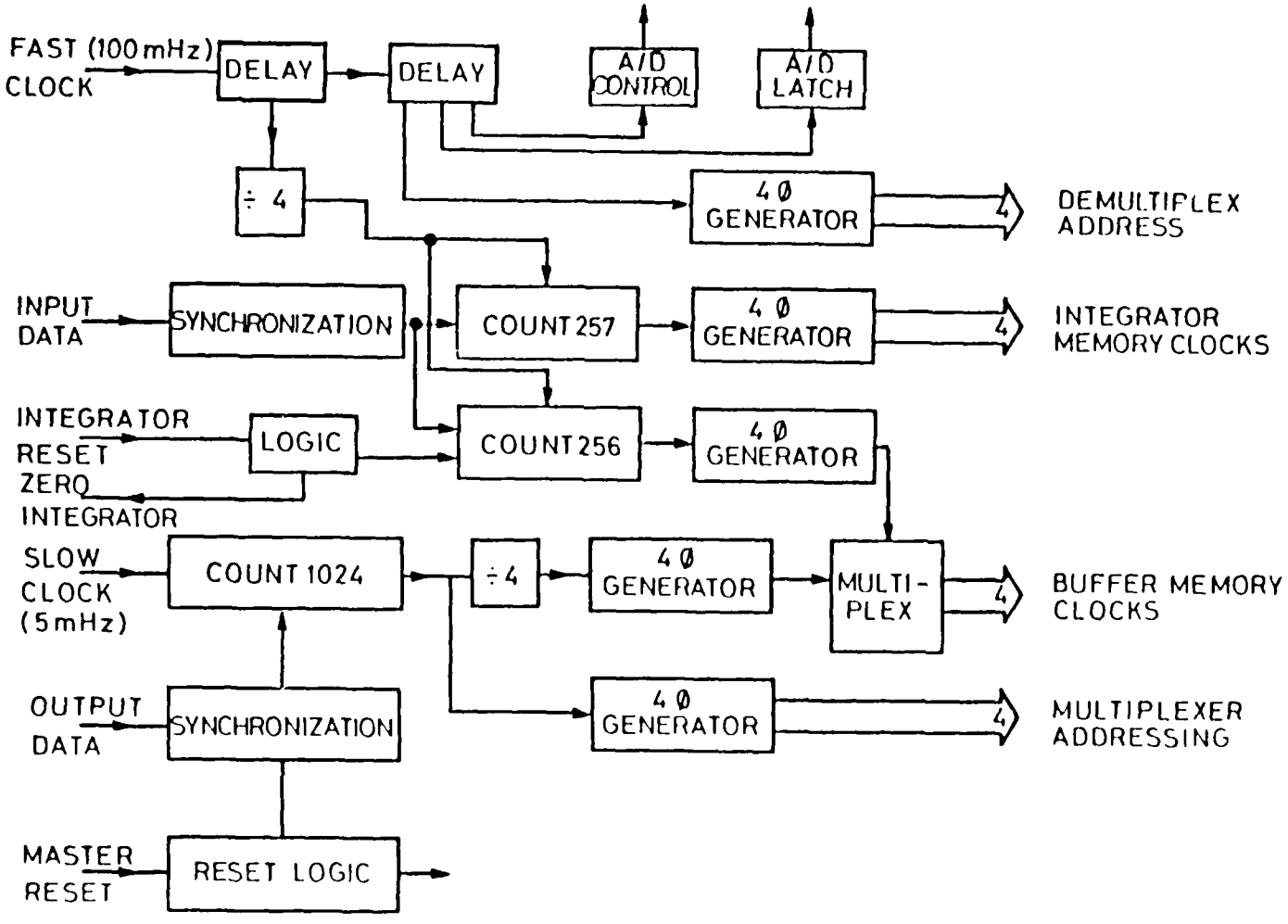


FIG 10 LOGIC CONTROL MODULE BLOCK DIAGRAM

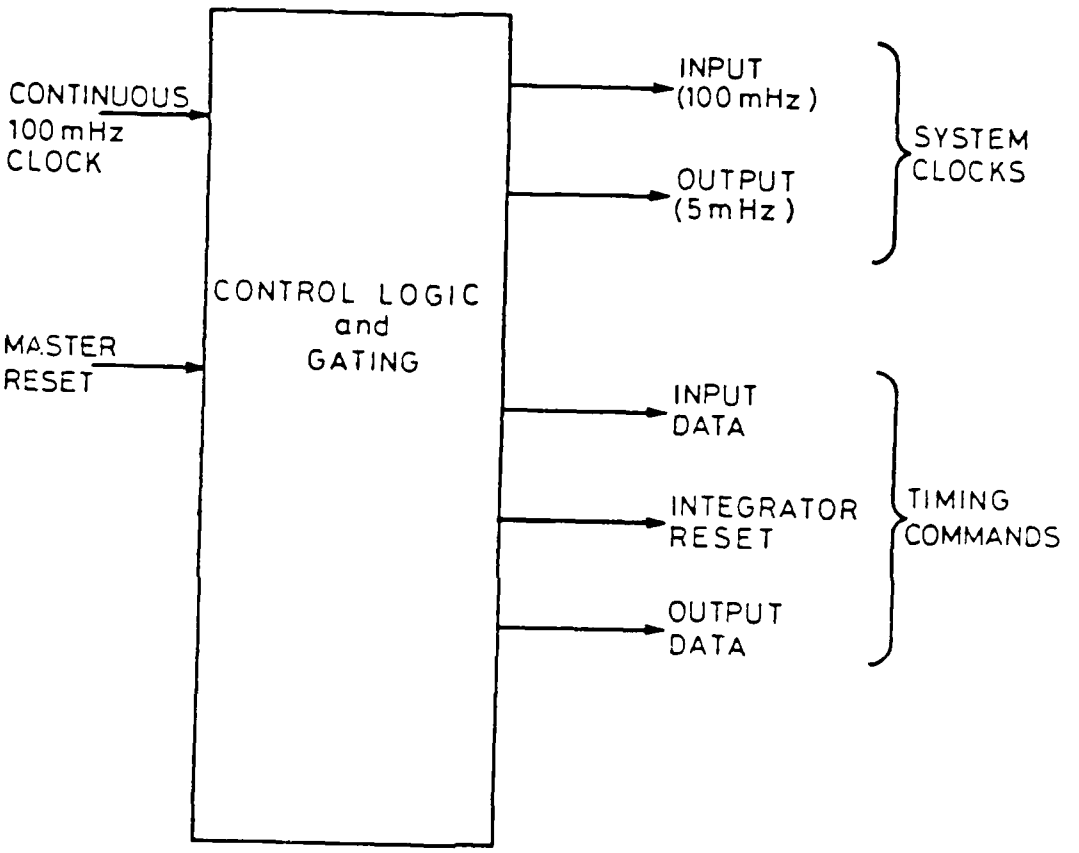


FIG.11 SYSTEM CONTROL MODULE

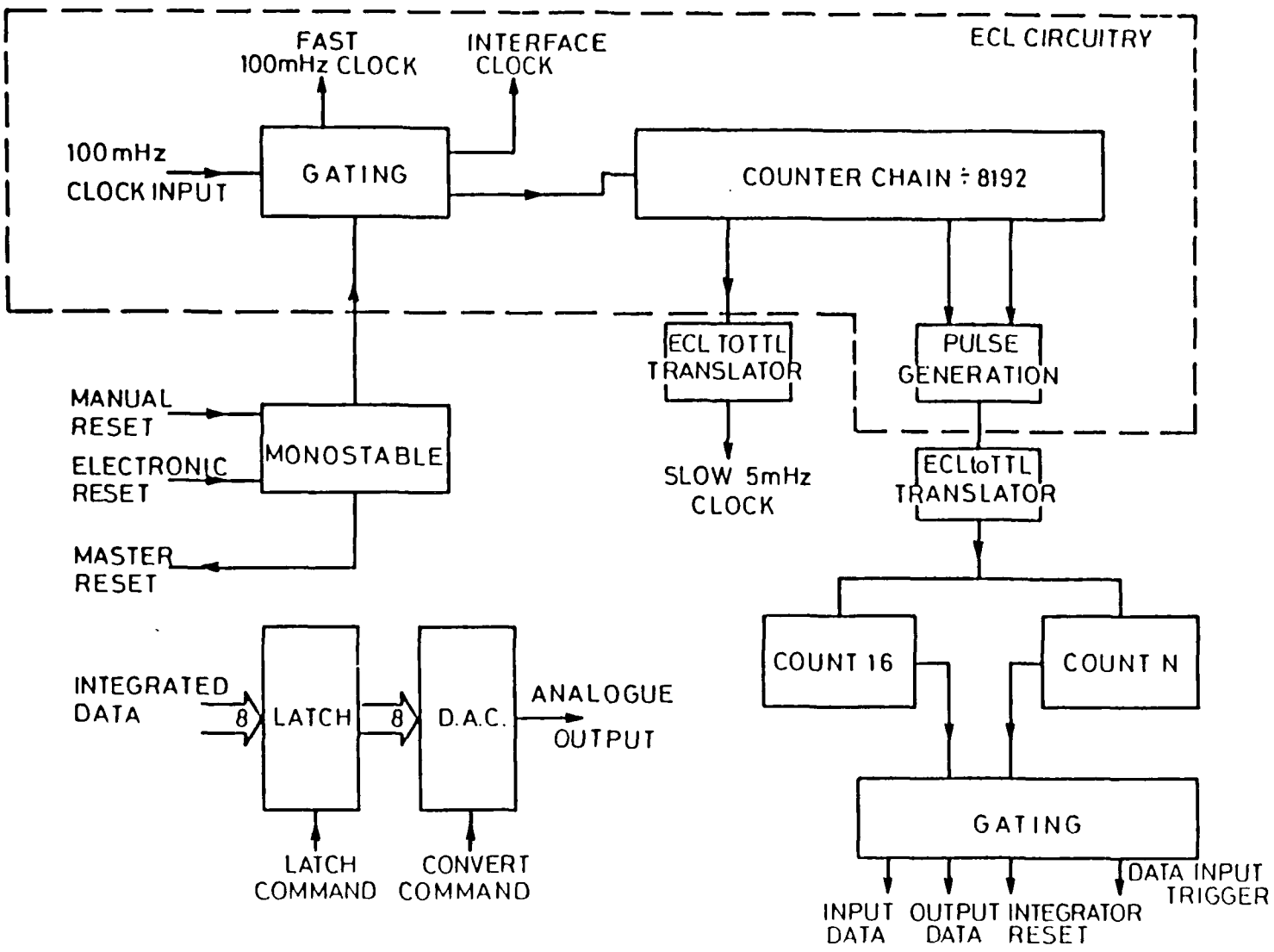


FIG.12 SYSTEM CONTROL MODULE

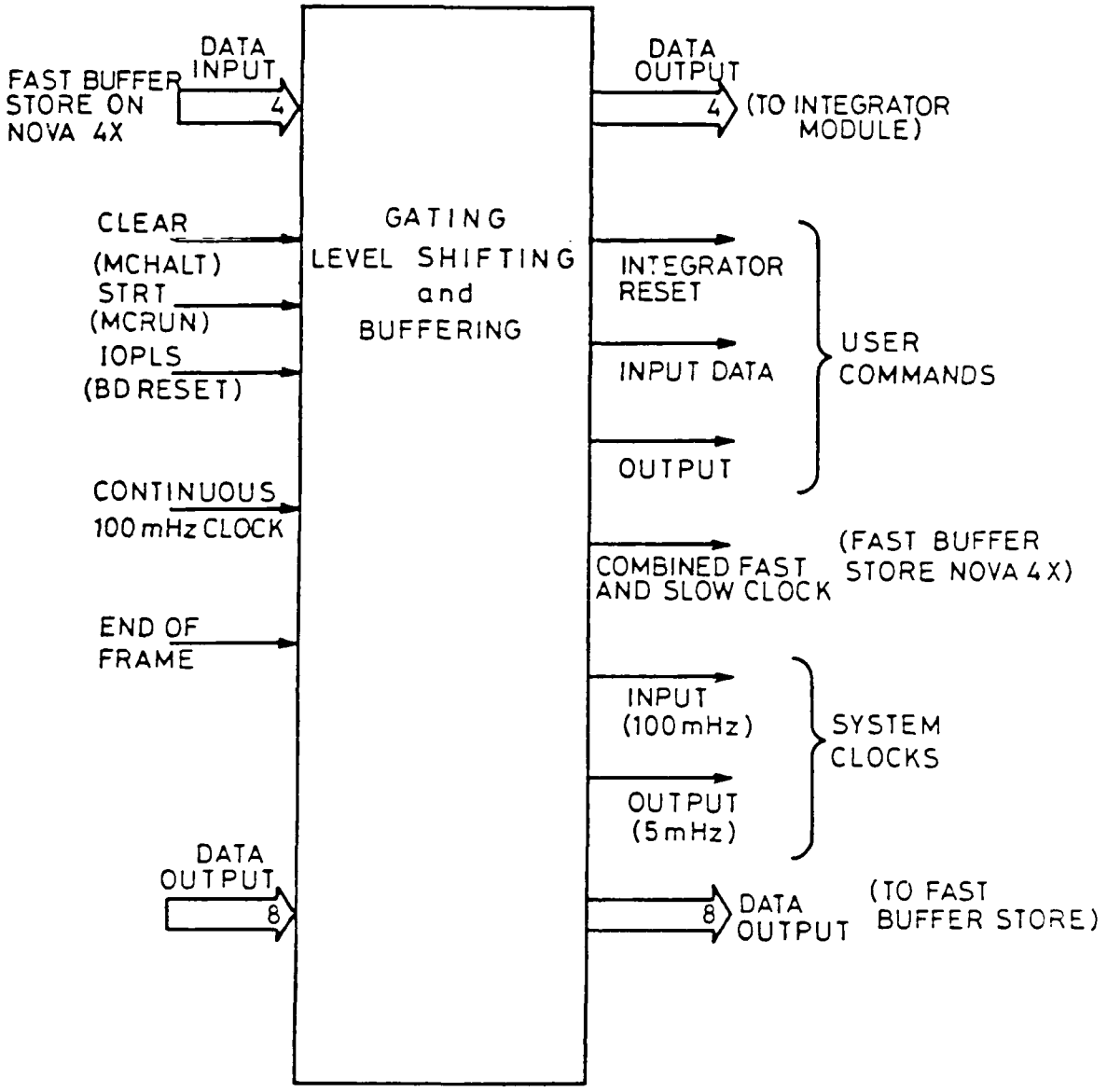


FIG. 13 INTERFACE MODULE

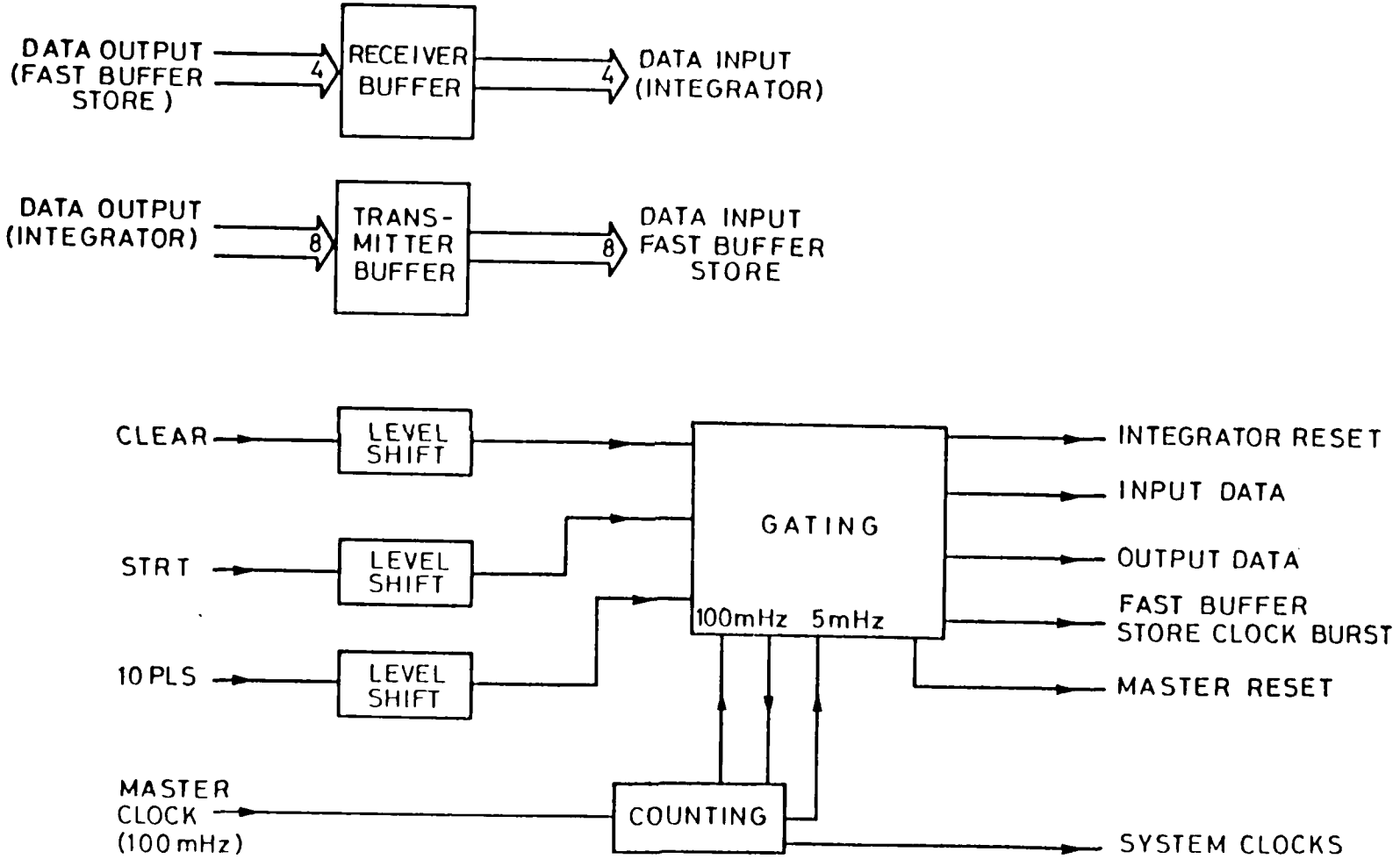


FIG.14 INTERFACE MODULE

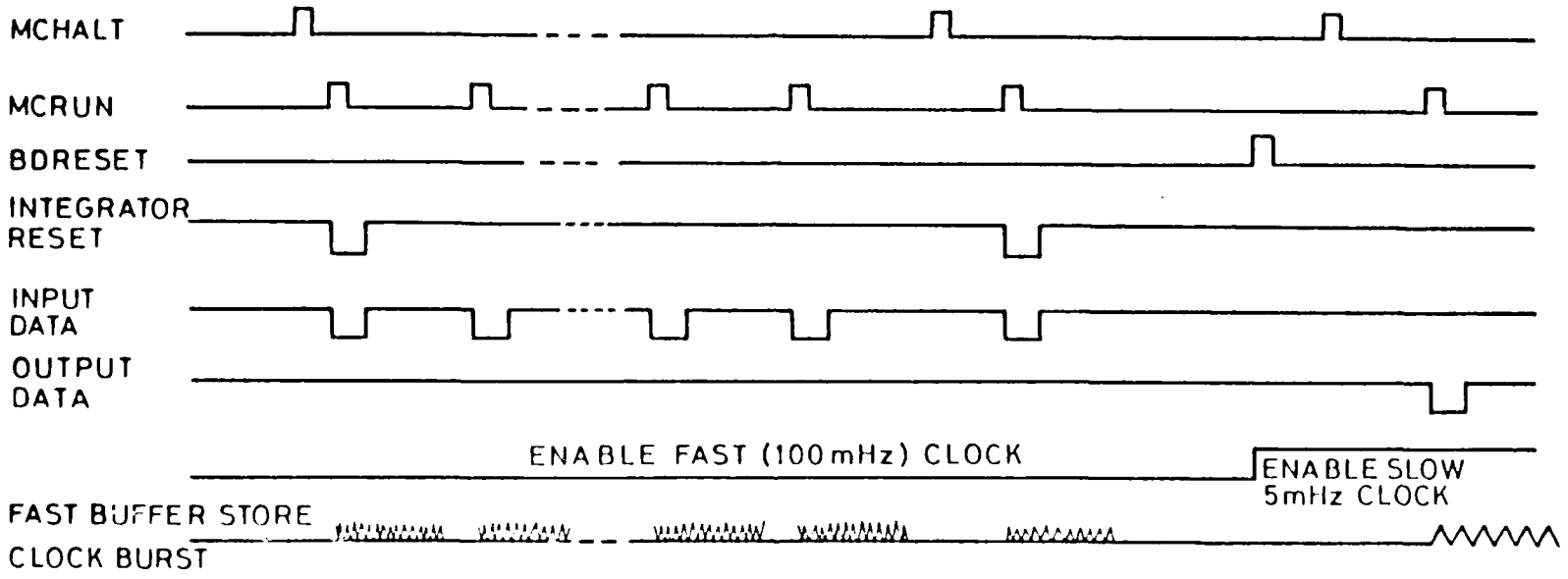


FIG 15 RELATIONSHIPS FOR USER COMMANDS AND CONTROLS

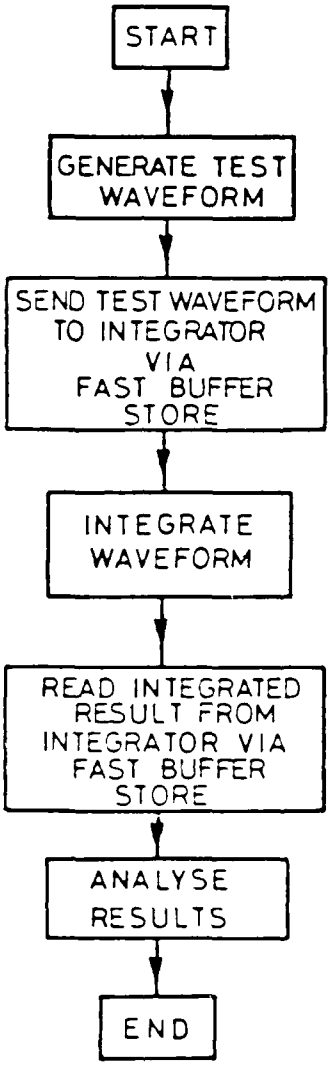


FIG 16 SIMPLIFIED TEST PROGRAM FLOW CHART

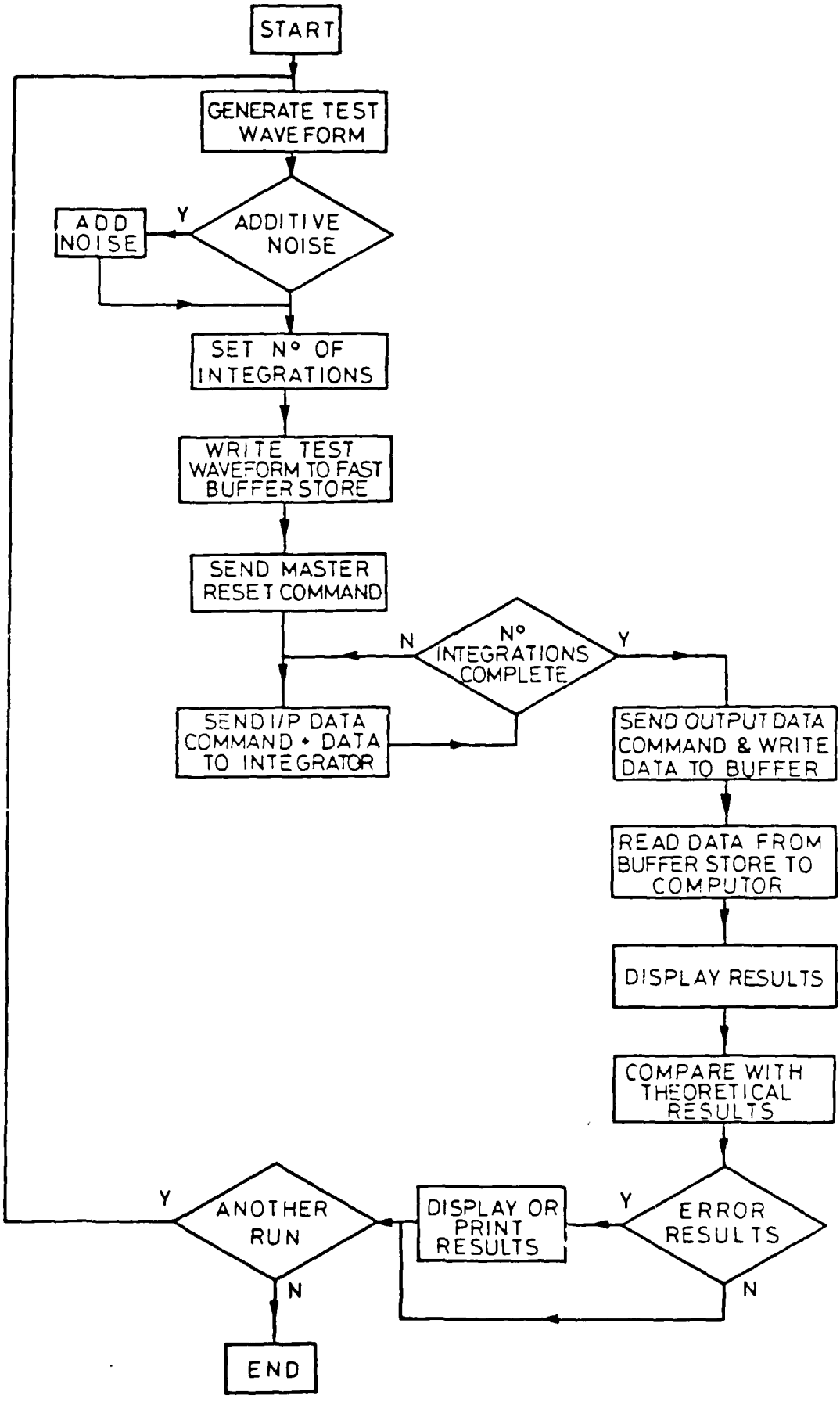


FIG 17 FINAL TEST PROGRAM FLOW CHART

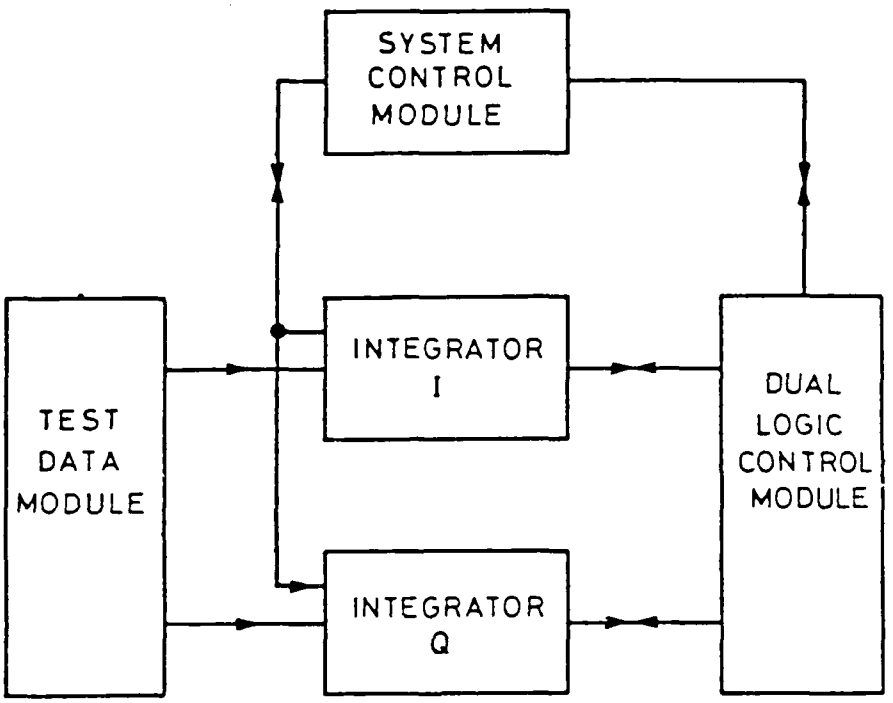


FIG.18 DUAL INTEGRATOR SYSTEM

DOCUMENT CONTROL SHEET

Overall security classification of sheet ..UNCLASSIFIED..... ....

(As far as possible this sheet should contain only unclassified information. If it is necessary to enter classified information, the box concerned must be marked to indicate the classification eg (R) (C) or (S))

1. DRIC Reference (if known)	2. Originator's Reference Memorandum 3672	3. Agency Reference	4. Report Security Classification Unclassified
5. Originator's Code (if known)	6. Originator (Corporate Author) Name and Location Royal Signals and Radar Establishment		
5a. Sponsoring Agency's Code (if known)	6a. Sponsoring Agency (Contract Authority) Name and Location		

7. Title

THE DESIGN, IMPLEMENTATION AND EVALUATION OF A FAST 100 MHz INTEGRATOR SYSTEM

7a. Title in Foreign Language (in the case of translations)

7b. Presented at (for conference papers) Title, place and date of conference

8. Author 1 Surname, initials	9(a) Author 2	9(b) Authors 3,4...	10. Date	pp. ref.
Edwards R D				

11. Contract Number	12. Period	13. Project	14. Other Reference

15. Distribution statement

Descriptors (or keywords)

continue on separate piece of paper

Abstract

A miniature unfocussed synthetic aperture radar has been designed at RSRE. The radar parameters required a video integrator with a high data rate capability. Plessey Research (Caswell) Ltd were engaged to design and develop a 100 MHz shift register based video integrator module. At RSRE a real time test and evaluation system has been developed in conjunction with a minicomputer. A special purpose high speed computer compatible buffer store was developed by Cambridge Consultants Ltd. At RSRE a design incorporating two integrators to provide phase and quadrature processing has been developed. Details of the systems operational concepts, performance and test results are discussed.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58