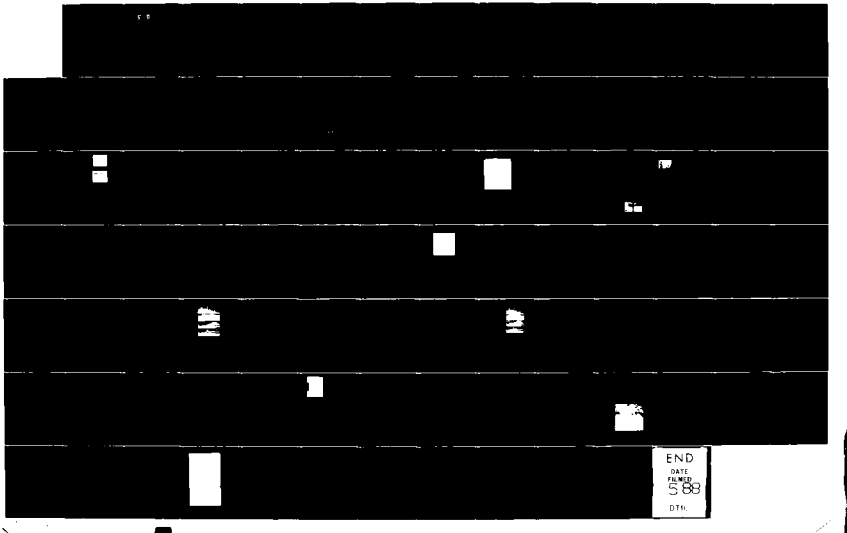
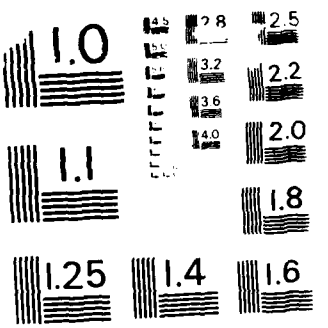
AD-A190 913 LIMITED REACTION PROCESSING FOR SEMICONDUCTOR DEVICE FABRICATION(U) STANFORD UNIV CA STANFORD ELECTRONICS LABS J F GIBBONS DEC 87 ARO-23222.17-EL-A 1/1

UNCLASSIFIED DAAG29-85-K-0237 F/G 9/1 NL





UNCLASSIFIED MASTER COPY - FOR REPRODUCTION PURPOSES (2)

AD-A190 913 REPORT DOCUMENTATION PAGE

Unclassified 2a. SECURITY CLASSIFICATION AUTHORITY	1b. RESTRICTIVE MARKINGS
2b. DECLASSIFICATION / DOWNGRADING SCHEDULE	3. DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S) ARO 23222.17-EL-A
6a. NAME OF PERFORMING ORGANIZATION Stanford University 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION U. S. Army Research Office
6c. ADDRESS (City, State, and ZIP Code) Stanford Electronics Labs. Dept. of Electrical Engineering Stanford California 94305	7b. ADDRESS (City, State, and ZIP Code) P. O. Box 12211 Research Triangle Park, NC 27709-2211
8a. NAME OF FUNDING / SPONSORING ORGANIZATION U. S. Army Research Office 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER DAAG29-85-K-0237
8c. ADDRESS (City, State, and ZIP Code) P. O. Box 12211 Research Triangle Park, NC 27709-2211	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification)
Limited Reaction Processing for Semiconductor Device Fabrication

12. PERSONAL AUTHOR(S)
James F. Gibbons

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Final	FROM 9/30/85 TO 11/30/87	December 1987	87

16. SUPPLEMENTARY NOTATION
The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Rapid Thermal Processing Semiconductor Devices, Semiconductors, Insulators Limited Reaction Processing, Chemical Vapor Deposition,

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Work performed at Stanford under this contract has shown that a new class of semiconductor processing equipment is feasible. We have designed and fabricated test equipment which uses a combination of Rapid Thermal and Chemical Vapor Deposition (CVD) technologies to achieve epitaxial growth and deposition of semiconductors and insulators. The trend towards single-wafer processing makes Limited Reaction Processing (LRP) particularly relevant to state of the art device fabrication research.

20. DISTRIBUTION / AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION	
☐ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS	Unclassified	
22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE (Include Area Code)	22c. OFFICE SYMBOL

DD FORM 1473, 84 MAR 83 APR edition may be used until exhausted. All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE
UNCLASSIFIED

ARO 23222.17-EL-A

SOLID STATE ELECTRONICS LABORATORY

STANFORD ELECTRONICS LABORATORIES
DEPARTMENT OF ELECTRICAL ENGINEERING
STANFORD UNIVERSITY · STANFORD, CA 94305

LIMITED REACTION PROCESSING FOR SEMICONDUCTOR DEVICE FABRICATION

FINAL REPORT

James F. Gibbons
Principal Investigator

December 1987

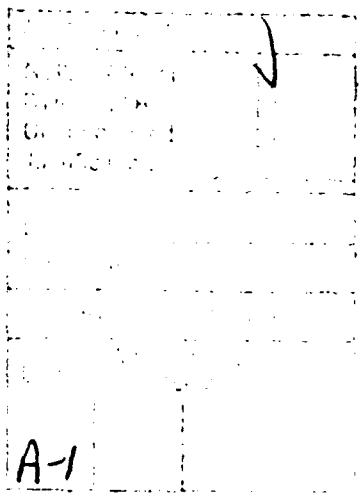
U.S. Army Research Office
Proposal Number 23222-EL-A
Contract DAAG29-85-K-0237
Sept. 30, 1985 – Nov. 30, 1987

LIMITED REACTION PROCESSING FOR SEMICONDUCTOR DEVICE FABRICATION

FINAL REPORT

J.F. Gibbons
Principal Investigator

December 1987



U.S. Army Research Office
Proposal Number 23222-EL-A
Contract DAAG29-85-K-0237
Sept. 30, 1985 Nov. 30, 1987

Stanford University
Stanford, California 94305

FOREWORD

This document is the final report for U.S. Army Research Office contract number DAAG29-85-K-0237, which corresponds to the proposal entitled **Limited Reaction Processing for Semiconductor Device Fabrication**. Limited Reaction Processing (LRP) is a new technique which has been investigated under this contract. LRP uses radiant energy to precisely control thermally driven surface reactions for the growth and deposition of semiconductor layers. This technique grew out of the closely related field of Rapid Thermal Processing (RTP) which is used for short time, high temperature annealing of semiconductor wafers. The goals of the research performed under this contract have been to:

1. determine the feasibility of the LRP
2. identify problems with the technique and explore solutions if necessary
3. demonstrate device applications of RTP and LRP

The emphasis of the research has been on characterizing the semiconductor material grown by LRP using a combination of physical techniques and test devices. Ultimately, these layers will be used to create new and useful device structures. We have demonstrated that LRP is capable of producing silicon-based epitaxial layers with excellent material and electrical properties. Several different minority and majority carrier devices have been fabricated using LRP and *in-situ* processing. The application of LRP to compound semiconductor growth (e.g. GaAs, AlGaAs, and InGaAs) has demonstrated the capability to produce interfaces with abruptness comparable to that obtained by Molecular Beam Epitaxy.

This report constitutes a brief summary of research performed under the above contract. It begins in Part 1 with a complete list of publications associated with this research. A short synopsis of 16 publications which describe our findings is followed by Part 3, which contains reprints of these publications. The final section (Part 4) contains a list of participating scientific personnel.

CONTENTS

Part 1

List of Publications

The following is a list of 16 publications which are summarized in Part 2 of this report. Reprints of these articles appear in Part 3 in the following order:

1. J.F. Gibbons, C.M. Gronet, and K.E. Williams, "Limited reaction processing: Silicon epitaxy", *Appl. Phys. Lett.* **47**, 1 Oct. 1985, pp. 721-723.

2. C.M. Gronet, J.C. Sturm, K.E. Williams, J.F. Gibbons, and S.D. Wilson, "Thin, highly-doped layers of epitaxial silicon deposited by limited reaction processing", *Appl. Phys. Lett.* **48**, 14 April 1986, pp. 1012-1014.

3. J.C. Sturm, C.M. Gronet, and J.F. Gibbons, "Limited reaction processing: *In-situ* metal-oxide-semiconductor (MOS) capacitors", *IEEE Elec. Dev. Lett.* **EDL-7**, May 1986, pp. 282-283.

4. J.C. Sturm, C.M. Gronet, and J.F. Gibbons, "Minority carrier properties of thin epitaxial silicon films fabricated by limited reaction processing", *J. Appl. Phys.* **59**, 15 June 1986, pp. 4180-4182.

5. J.C. Sturm, C.M. Gronet, and J.F. Gibbons, "*In-situ* epitaxial silicon-oxide-doped polysilicon structures for MOS field-effect transistors", *IEEE Elec. Dev. Lett.* **EDL-7**, Oct. 1986, pp. 577-579.

6. C.M. Gronet, C.A. King, and J.F. Gibbons, "Growth of GeSi/Si strained-layer superlattices using limited reaction processing", *Mat. Res. Soc. Symp. Proc. Vol.* **71**, (Materials Research Society, Pittsburg, 1986), pp. 107-112.

7. C.M. Gronet, C.A. King, W. Opyd, J.F. Gibbons, S.D. Wilson, and R. Hull, "Growth of GeSi/Si strained-layer superlattices using limited reaction processing", *J. Appl. Phys.* **61**, 15 March 1987, pp. 2407-2409.

8. J.E. Turner, J. Amano, C.M. Gronet, and J.F. Gibbons, "Secondary ion mass spectrometry of hyper-abrupt dopant transitions fabricated by limited reaction processing", *Appl. Phys. Lett.* **50**, 1 June 1987, pp. 1601-1603.

9. C.A. King, C.M. Gronet, and J.F. Gibbons, "Electrical characterization of *in-situ* epitaxially grown Si p-n junctions fabricated using limited reaction processing", submitted to *IEEE Elec. Dev. Lett.*, Jan., 1988.

10. M.D. Giles, J.L. Hoyt, and J.F. Gibbons, "The depth resolution of dynamic SIMS: Experiments and calculations", *Mat. Res. Soc. Symp. Proc. Vol.* **69**, (Materials Research Society, Pittsburg, 1986), pp. 323-328.

11. J.L. Hoyt, E.F. Crabbé, J.F. Gibbons, and R.F.W. Pease, "Epitaxial alignment of arsenic implanted polysilicon emitters", *Mat. Res. Soc. Symp. Proc. Vol.* **92**, (Materials Research Society, Pittsburg, 1987), pp. 47-52.

12. E. Crabbé, J.L. Hoyt, M.M. Moslehi, R.F.W. Pease, and J.F. Gibbons, "Novel emitter contacts for VLSI bipolar transistors", in *Technical Digest: 1987 International Symposium on VLSI Technology, Systems and Applications*, Taipei, Taiwan, May 13-15, 1987.

13. S. Reynolds, D.W. Vook, and J.F. Gibbons, "Limited reaction processing: Growth of III-V epitaxial layers by rapid thermal metalogranic chemical vapor deposition", *Appl. Phys. Lett.* **49**, 22 Dec. 1986, pp. 1720-1722.

14. D.W. Vook, S. Reynolds, and J.F. Gibbons,"Growth of GaAs by metalorganic chemical vapor deposition using thermally decomposed trimethylarsenic", *Appl. Phys. Lett.* **50**, 11 May 1987, pp. 1386-1387.

15. S. Reynolds, D.W. Vook, and J.F. Gibbons,"Limited reaction processing: Growth of III-V epitaxial layers by rapid thermal metalorganic chemical vapor deposition", *Mat. Res. Soc. Symp. Proc. Vol.* **92**, (Materials Research Society, Pittsburg, 1987), pp. 305-310.

16. J.F. Gibbons, S. Reynolds, C. Gronet, D. Vook, C. King, W. Opyd, S. Wilson, C. Nauka, G. Reid, and R. Hull, "Limited reaction processing: Silicon and III-V Materials", *Mat. Res. Soc. Symp. Proc. Vol.* **92**, (Materials Research Society, Pittsburg, 1987), pp. 281-294.

The following are publications *not* included in Part 3 of this report. They are included here in order to complete the list of publications:

17. C.M. Gronet, J.C. Sturm, K.E. Williams, and J.F. Gibbons, "Limited Reaction Processing of Silicon: Oxidation and Epitaxy", in *Mat. Res. Soc. Symp. Proc. Vol.* **52**, (Materials Research Society, Pittsburg, 1986), pp. 305-310.

18. J.F. Gibbons, C.M. Gronet, J.C. Sturm, C. King, K. Williams, S. Wilson, S. Reynolds, D. Vook, M. Scott, R.Hull, C. Nauka, J. Turner, S.

Laderman, and G. Reid,"Limited Reaction Processing", invited paper in *Mat. Res. Soc. Symp. Proc. Vol.* **74**, (Materials Research Society, Pittsburg, 1987), pp. 629-639.

19. J.L. Hoyt, E. Crabbé, J.F. Gibbons, and R.F.W. Pease, "Epitaxial alignment of arsenic implanted polycrystalline silicon films on ⟨100⟩ silicon obtained by rapid thermal annealing", *Appl. Phys. Lett* **50**, 23 March 1987, pp. 751-753.

20. J.L. Hoyt, E.F. Crabbé, R.F.W. Pease, and J.F. Gibbons "Characterization of arsenic implanted epitaxially aligned polysilicon-on-silicon films", *Mat. Res. Soc. Symp. Proc. Vol.* **106**, (Materials Research Society, Pittsburg, 1988). *in press.*

21. E.F. Crabbé, J.L. Hoyt, R.F.W. Pease, and J.F. Gibbons "Electrical characterization of polysilicon-to-silicon interfaces", *Mat. Res. Soc. Symp. Proc. Vol.* **106**, (Materials Research Society, Pittsburg, 1988). *in press.*

22. J.L. Hoyt, E.F. Crabbé, R.F.W. Pease, and J.F. Gibbons, "Etching technique for characterization of epitaxial alginment of arsenic implanted polycrystalline silicon films on ⟨100⟩ silicon." *J. Electrochem. Soc.*, in press.

23. J.L. Hoyt, E.F. Crabbé, R.F.W. Pease, and J.F. Gibbons, "Lateral uniformity of n^+/p junctions formed by arsenic diffusion from epitaixally aligned polycrystalline silicon on silicon." *J. Electrochem. Soc.*, in press.

Part 2

Summary of the Research

Work performed at Stanford under this contract has shown that a new class of semiconductor processing equipment is feasible. We have designed and fabricated test equipment which uses a combination of Rapid Thermal and Chemical Vapor Deposition (CVD) technologies to achieve epitaxial growth and deposition of semiconductors and insulators. The trend towards single-wafer processing makes Limited Reaction Processing (LRP) particularly relevant to state of the art device fabrication research. A single LRP cycle generally has the following format:

1. While the wafer is cool, a desired reactive gas flow is established over the substrate.

2. Using a high-intensity radiant source, the substrate is rapidly heated and a chemical reaction between the substrate surface and reactive gas is induced.

3. The reaction is allowed to proceed at temperature for the desired time.

4. The reaction is stopped by turning off the lamps and rapidly cooling the substrate.

In this process, the substrate temperature, rather than the flux of reactive gas, is used as a "switch" to turn on and off the CVD reaction. This thermal switching technique has three significant advantages:

- Abrupt composition profiles: since the substrate is hot only during layer growth, LRP inherently minimizes the thermal exposure of a substrate, similar to RTP. This allows the growth of layers at fairly high temperatures while maintaining abrupt composition profiles.

- Growth of ultra-thin layers: the accuracy and reproducibility of the substrate temperature versus time profile afforded by lamp heating produces controlled growth of thin layers of semiconductors and insulators.

- *In-situ* multilayer processing: by changing the ambient gas between high temperature cycles, multiple layers of different composition can be grown sequentially without removing the substrate from the processing chamber. This feature is important for minimizing chemical and particulate contamination.

2.1 Silicon-based research

The following sections summarize our research findings for silicon-based materials as described in Papers 1 through 10 of Part 3 (see also Paper # 16 for an overall LRP summary).

2.1.1 Column IV epitaxy

The first two papers in Part 3 of this report describe the initial implementation of rapid thermal switching applied to silicon epitaxy. A rudimentary LRP reactor was constructed by combining a home-built Rapid Thermal Processor with a gas delivery and exhaust system which includes gases such as SiH_4, SiH_2Cl_2, H_2, O_2, HCl, and Ar. This system uses two banks of tungsten filament lamps and a microprocessor control system to rapidly heat 2 inch silicon wafers. Second and third generation systems were later constructed for 3 inch and 4 inch wafer processing, as indicated below. The earliest results, described in Paper # 1, revealed that LRP produced abrupt transitions in doping concentration at the epitaxial layer/substrate interface for undoped films on heavily doped (n^+ and p^+) substrates. In Paper # 2, the technique is extended to multilayer structures consisting of alternating undoped and heavily boron-doped regions (i.e. $i/p^+/i/p^+$ structures). Van der Pauw measurements indicate that the hole mobilities of the p^+ epitaxial films are comparable to bulk material. In addition, LRP produces a wider dynamic range in *p*-type doping than can be obtained by MBE.

Papers 3-5 describe more detailed electrical characterization of LRP grown layers. Metal-oxide-semiconductor (MOS) capacitors fabricated by growing a thin gate oxide followed by polysilicon gate deposition *in-situ* are discussed in Paper # 3. These capacitors exhibit excellent characteristics, with interfacial fixed charge and mobile ion contaminations of less than 10^{10} cm^{-2}. More stringent tests of the epitaxial layer quality are described in Paper # 4. Generation lifetimes from 1 to 100 μsec were measured, and planar diodes (ion implanted) fabricated in

both n- and p-type epitaxial films show excellent behavior. In Paper # 5, we demonstrate the formation of *in-situ* MOSFET structures, using selective epitaxial growth combined with oxidation and polysilicon gate deposition.

Papers 6 and 7 describe the growth of GeSi/Si strained-layer superlattices. Layers as thin as 150 Å were reproducibly achieved, establishing for the first time the use of a CVD technique to fabricate abrupt GeSi/Si-based heterostructures. In Paper # 8, high resolution Secondary Ion Mass Spectrometry (SIMS) analysis of LRP layers performed in collaboration with HP laboratories is described. Using a special technique, boron doping transition widths as abrupt as 50 Å/decade were measured.

Paper # 9 contains the most recent results on electrical characterization of *in-situ*, epitaxially grown p-n junctions fabricated using the third generation LRP system. These experiments provide the most stringent tests of material quality to date, since the "interrupted growth" interface is contained *within* the diode space charge region. Forward current ideality factors of 1.01 ± 0.3 % were obtained over at least 7 orders of magnitude, extending down to 1 pA. Very low reverse current densities (3.5 nA- cm^{-2} at -5 V) were observed. The results described in this paper indicate that LRP material is suitable for high performance minority carrier devices.

In Paper # 10, we describe the application of LRP to studies of the depth resolution of SIMS. Analysis of LRP-grown layers places some of the most stringent requirements on the SIMS technique, because it demands *both* depth resolution and dynamic range. Experimental results on atomically abrupt impurity profiles in Si are explained by a theoretical model. The Boltzmann Transport Equation method for calculating recoil effects during ion implantation was modified to treat the SIMS problem, and good agreement with experimental observations was obtained.

2.1.2 Rapid thermal processing

Papers 11 and 12 describe a combination of LRP and Rapid Thermal Annealing applied to polysilicon emitter contacts for VLSI bipolar transistor fabrication. Paper 11 discusses research on epitaxial regrowth of polysilicon films. This work utilizes a standard LPCVD polysilicon reactor for the material deposition and RTA to provide the desired materials quality, creating a bridge between currently existing silicon process technology and LRP. Bipolar transistors with 0.5 μm-thick

emitter contacts and polysilicon dopings of 5 and 10×10^{20} cm^{-3} show less process sensitivity when subject to RTA ($T \geq 1100$ °C) compared to devices annealed in a furnace in the 900 to 1000 °C range, while retaining advantages over metal contacts.

In Paper # 12, we describe how RTA and LRP are used to taylor the structure of the polysilicon-to-silicon interface to the device application of interest. For high speed devices where emitter resistance is the primary concern, RTA is used to break-up the polysilicon/silicon interfacial oxide and enhance dopant activation in the polysilicon. On the other hand, when minority carrier transport through the interface must be minimized, LRP in an ammonia ambient can be used to grow a thin (15 Å), thermally stable silicon nitride interfacial layer which results in extremely low base currents.

2.2 Epitaxy of compound semiconductors

Paper # 13 describes the application of Limited Reaction Processing to the epitaxial growth of GaAs. A separate LRP system was designed and fabricated for this purpose. The technique produces layers with specular, defect-free surfaces and good electrical characteristics. Growth of related compounds such as AlGaAs and InGaAs is also reported. Extremely abrupt transitions between adjacent epitaxial layers are observed, comparable to MBE grown material.

Paper # 14 describes a new precracking method for reducing the background doping and increasing the electron mobility of epitaxial GaAs layers. This method has resulted in the highest purity GaAs ever grown using a trimethylarsenic source in a CVD reactor. Paper #15 discusses more detailed materials studies performed on LRP-grown GaAs, specifically the quality and abruptness of the hetero-interfaces.

An overall summary of some of the most recent silicon and III-V results on LRP epitaxial layers is contained in the final paper, # 16. Special attention is given to the characterization of the interrupted growth interfaces.

Part 3

Reprints of Publications

This sections contains reprints of the articles listed in Part 1 and described in Part 2.

Paper # 1

Limited reaction processing: Silicon epitaxy

J. F. Gibbons, C. M. Gronet, and K. E. Williams
Stanford Electronics Laboratories, Stanford, California 94305

(Received 17 May 1985; accepted for publication 11 July 1985)

We introduce a new technique, limited reaction processing, in which radiant heating is used to provide rapid, precise changes in the temperature of a substrate to control surface reactions. This process was used to fabricate thin layers of high quality epitaxial silicon. Abrupt transitions in doping concentration at the epitaxial layer/substrate interface were achieved for undoped films deposited on heavily doped substrates.

The fabrication of thin, high quality layers of semiconductor and insulator films is critical to the future of semiconductor processing. It is also of potentially great importance to fabricate several films sequentially without removing the substrate from the processing chamber. This letter describes a technique for achieving these objectives and reports the application of the method for the formation of thin epitaxial layers of silicon with abrupt transitions in doping concentration.

The reaction chamber used for the process is shown schematically in Fig. 1. Gas flow rates in the reaction chamber were controlled by flow meters, and the pressure was measured by a capacitance manometer at the chamber exit. The pressure gauge was used in a closed loop system with an automatic throttle valve upstream of the pump to ensure constant pressure.

The substrate was rapidly heated by two banks of six air-cooled 1.2-kW tungsten lamps backed by water-cooled reflectors. These lamps irradiate both sides of a 2-in.-diam silicon substrate mounted on three quartz pins. For temperature calibration, a W/26% Re vs W/5% Re thermocouple was welded to the edge of a wafer. In addition, melting point standards were used (Omegalaq). Calibrations were performed periodically and were very reproducible (run to run variation < 20 °C). Temperature uniformity was established by growing a thin thermal oxide (10–60 nm) and measuring thickness uniformity using spatial ellipsometry. The variation in oxide thickness over a 2.5×2.5 cm square centered on the 2-in. wafer was less than 3%.

To operate what we refer to as a limited reaction processing (LRP) cycle, the reactant gases are permitted to flow

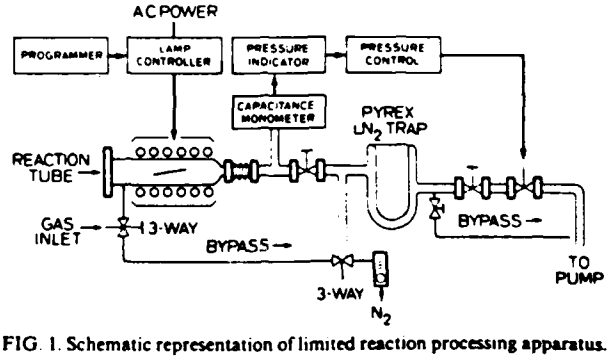


FIG. 1. Schematic representation of limited reaction processing apparatus.

 0003-6951/85/190721-03$01.00

TABLE I. Epitaxial deposition parameters for limited reaction processing samples.

Sample	Temperature (°C)	Pressure (Torr)	Mole % SiH_2Cl_2	Diluent flow (LPM)	Deposition time (s)	Thickness (μm)
LRP 59	980	1.0	11.5	0.5(H_2)	60	0.36
LRP 61	920	19.5	0.77	3.0(H_2) 10.9(He)	15	0.15
LRP 62	980	1.0	21.4	0.5(H_2)	180	2.1
LRP 64	940	5.0	3.9	3.0(H_2)	70	1.0

through the deposition chamber to establish equilibrium flow patterns and rates. The lamps are then activated by a microprocessor to heat the substrate to produce a desired temperature versus time profile. Typical heat up and cool down rates are 1–5 ms/°C, similar to rapid thermal annealing.[1] These rates are sensitive to the thickness of the wafer and the optical coupling between the radiant source and the substrate.[2] However, with proper design, precise, reproducible control of the substrate temperature can be obtained, even for cycles as short as a few seconds. During a LRP cycle, such tight temperature control translates to precise control over a thermally driven surface reaction, such as chemical vapor deposition. Moreover, by changing the gas flows between high-temperature cycles, multiple layers of different compositions can be grown without removing the sample from the deposition chamber. We have applied this technique to the *in situ* growth of multiple layers of SiO_2 and polysilicon, and are currently investigating other multilayer structures which we will report at a later date. Results on the growth of single layers of thin dielectric films using rapid thermal processing have been reported, e.g., nitrides[3] and oxides.[4]

As device geometries shrink, many integrated circuit technologies will require very thin (0.2–1.5 μm) lightly doped silicon layers on top of heavily doped substrates. Thus, we attempted to grow undoped layers of epitaxial silicon on heavily doped (100) and (111) silicon wafers (less than 0.02 Ω cm). All substrates were given an RCA clean, and in some cases 100 nm of thermal oxide was grown and patterned to cap the back and edges of the wafer to minimize autodoping from these surfaces.[5] Prior to deposition *in situ* rapid thermal precleaning was performed. The wafers were heated in H_2 to 1120 °C for 10–30 s and then etched in 1% HCl in H_2 for 10–30 s. The effectiveness of shorter cleaning steps is being investigated to reduce both dopant evaporation from the substrate and dopant redistribution in the substrate or underlying layers. However, preliminary results indicate that an HCl etch of at least 20 s is required to remove carbon and oxygen from the substrate surface.

The epitaxial deposition parameters are summarized for four typical wafers in Table I. Undoped silicon was deposited using a SiH_2Cl_2 source.[6] The reaction chamber was purged with several pump-down/backfill cycles, and then gas flows were allowed to stabilize for a few minutes prior to temperature cycling. Pressures were minimized to reduce vertical autodoping,[7] improve thickness uniformity, and allow single crystal deposition at lower substrate temperatures.[8,9] Compared to standard epitaxial processing, deposition times can be extremely short using LRP. Thus, out-diffusion from the substrate can be minimized, allowing an abrupt transition in the doping concentration at the epitaxial layer/substrate interface. Typical secondary ion mass spectroscopy (SIMS, Charles Evans and Associates) profiles for samples LRP 59 and LRP 64 are shown in Fig. 2. As shown in Table II for LRP 59, the Sb concentration changes two orders of magnitude (10^{16}–10^{18} cm^{-3}) over a distance of less than 30 nm. For comparison, a boron-doped silicon epitaxial layer deposited by molecular beam epitaxy (MBE) at room temperature was analyzed directly after LRP 59 using identical SIMS conditions. This procedure allowed us to compare the SIMS data for LRP 59 with the SIMS data produced by a sample with a doping profile which is presumably a step function. The MBE sample exhibited a change in boron concentration from 5×10^{17} to 5×10^{19} cm^{-3} over a distance of less than 20 nm. This indicates that there may be some very small Sb out-diffusion, or possibly that the SIMS depth resolution is better for B than for Sb. To resolve this we are currently performing SIMS analysis of undoped MBE silicon deposited on heavily doped Sb substrates.

Table II lists details of the transition regions for other

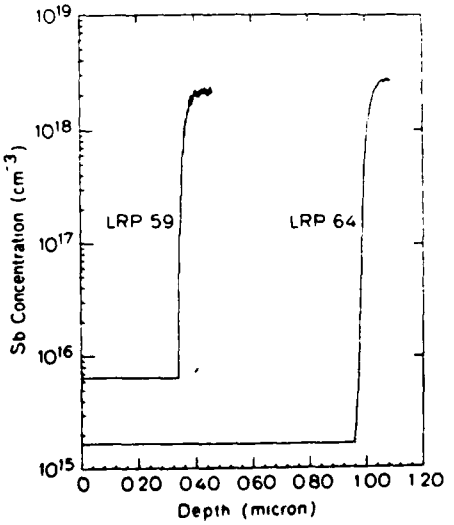


FIG. 2. SIMS profiles for samples LRP 59 and LRP 64 (undoped silicon epitaxial films grown on n^+ Sb-doped substrates). The horizontal lines at the bottom of each profile indicate sensitivity limits. The sputtering rate was decreased for LRP 59 in order to obtain more data points in the transition region. (SIMS was performed by Charles Evans and Associates.)

TABLE II. Secondary ion mass spectroscopy of the dopant transition region and substrate parameters for LRP undoped silicon epitaxial films grown on heavily doped *n*-type substrates.

Sample	Substrate Orientation	Dopant	Transition region Dopant range (cm^{-3})	Transition region Thickness (nm) (SIMS)
LRP 59	(111)	Sb	10^{16}–10^{18}	28
LRP 61	(100)	As	10^{17}–10^{19}	44
LRP 62	(100)	As	10^{17}–10^{19}	63
LRP 64	(100)	Sb	10^{15}–10^{17}	29
			10^{15}–10^{18}	58

samples. The transition region for the SIMS profiles for the As sample is not as steep as the Sb samples because As has a greater tendency for autodoping. However, the As substrates are doped to a concentration ten times higher than the Sb substrates, so some concentration-enhanced diffusion may have occurred. Even sharper transition regions could be obtained with shorter deposition times, but a lower limit is set by a consideration of the growth rate and the desired film thickness. In summary, these results indicate that LRP can produce ultrathin silicon epitaxial films with abrupt changes in doping concentration.

The LRP epitaxial films were specular and indistinguishable from polished substrates when viewed under a Nomarski contrast microscope. Films were deposited between 0.1 and 3.0 μm thick. The crystalline quality was studied using Rutherford backscattering channeling spectra (Fig. 3).

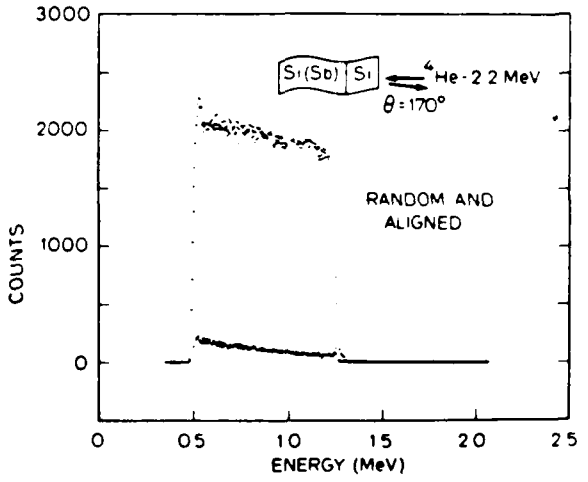


FIG. 3. Rutherford backscattering random and channeling spectra for sample LRP 59. The minimum yield is 2.7%.

The minimum yields for all samples were between 2.7% and 3.0%, indicating excellent crystalline quality.[10] Further investigations using cross-section transmission electron microscopy are in progress.

In conclusion, the deposition of thin silicon epitaxial films with abrupt transitions in doping concentration has been demonstrated using limited reaction processing. We are now investigating the use of this technique for depositing multiple layers of a number of doped and undoped semiconductors and insulators with sharp transition regions. In addition, limited reaction processing can be used to explore the initial growth regimes of almost any chemical vapor deposition process.

The authors wish to thank J. Hoyt, J. Strum, W. Opyd, M. Gutierrez, and Lockheed Corporation for their contributions to this work. C. Gronet acknowledges the support of an Office of Naval Research Fellowship.

[1] D. J. Lischner and G. K. Celler, in *Laser and Electron Beam Interactions With Solids*, edited by B. R. Appleton and G. K. Celler, Materials Research Society Symposium Proceedings, Boston, Nov. 1981 (Elsevier Science, North Holland, New York, 1982), pp. 759–764.
[2] T. E. Seidel, D. J. Lischner, C. S. Pai, and S. S. Lau, in *VLSI Science and Technology/1984*, edited by K. E. Bean and G. A. Rozgonyi (Electrochemical Society, Pennington, NJ, 1984), Vol. 84-7, p. 184.
[3] M. M. Moslehi, K. C. Saraswat, and S. Shatas, IEEE Trans. Electron Devices (to be published).
[4] J. Nulman, J. P. Krusius, and A. Gat, IEEE Electron Device Lett. **EDL-6**, 205 (1985).
[5] D. C. Gupta and R. Yee, J. Electrochem. Soc. **116**, 1561 (1969).
[6] A. Lekholm, J. Electrochem. Soc. **119**, 1122 (1972).
[7] M. Ogirima, H. Saida, M. Suzuki, and M. Maki, J. Electrochem. Soc. **124**, 903 (1977).
[8] M. Duchemin, M. Bonnet, and M. Koelsch, J. Electrochem. Soc. **125**, 637 (1978).
[9] T. J. Donahue and R. Reif, J. Appl. Phys. **57**, 2757 (1985).
[10] L. Feldman, J. Mayer, and S. Picraux, *Materials Analysis by Ion Channeling* (Academic, New York, 1982).

Paper # 2

Thin, highly doped layers of epitaxial silicon deposited by limited reaction processing

C. M. Gronet, J. C. Sturm, K. E. Williams, and J. F. Gibbons
Stanford University Electronics Laboratories, Stanford, California 94305

S. D. Wilson
Charles Evans and Associates, San Mateo, California 94402

(Received 2 December 1985; accepted for publication 14 February 1986)

Limited reaction processing was used to deposit ultrathin, highly doped layers of epitaxial silicon. Multilayer structures consisting of alternating undoped and heavily boron-doped regions were fabricated *in situ*. The interlayer doping profiles of these structures, as determined by secondary ion mass spectroscopy, are abrupt. Van der Pauw measurements indicate that the electrical characteristics of the p^+ epitaxial films are comparable to bulk material.

The control of doping levels and depth profiles in semiconductors is critical for device fabrication. Currently, diffusion and ion implantation are two commonly used methods for introducing dopants into semiconductors. Very large scale integration (VLSI) devices, however, will require abrupt doping transitions and ultrathin, highly doped layers which may be beyond the capabilities of these techniques. Ultimately, a technology with the interface control of molecular beam epitaxy (MBE) and the doping range of chemical vapor deposition (CVD) will be needed.

In an earlier letter,[1] we introduced a technique called limited reaction processing (LRP) which has potential for both of these capabilities. LRP can be used to fabricate thin layers of semiconductors and insulators by precise control of thermally driven surface reactions. Radiant heat is used to produce large, yet rapid changes in the temperature of a semiconductor substrate. The substrate temperature, rather than the flux of a reactive gas, is used as a "switch" to turn a CVD reaction on and off. The substrate is hot only while a deposition or surface reaction is occurring, not during purging, gas flow stabilization, and other process modes. Thus, inherently, the thermal exposure of the substrate is minimized, reducing the broadening of interfaces by diffusion and intermixing. The advantages of a high-temperature process, such as good material quality and high dopant activation, can be realized while maintaining interface control. Moreover, by changing the ambient gases between high-temperature cycles, multiple thin layers of different composition can be grown sequentially without removing the substrate from the processing chamber. The LRP system and its application to the deposition of single layers of undoped epitaxial silicon have been described previously.[1] In this letter we demonstrate the ability of LRP to fabricate single crystal silicon structures consisting of ultrathin, highly doped regions with precise thickness control and abrupt doping profiles.

Heavily doped (100) and (111) 2-in.-diam silicon wafers were used as substrates for multilayer structures. For electrical characterization, p^+ layers were deposited on n-type (100) wafers with a resistivity of 3–10 Ω cm.

To calibrate the wafer temperature for a given lamp power versus time program and sample ambient, a W/26% Re vs W/5% Re thermocouple was electron beam welded to the center of a test wafer. Epitaxial depositions were then carried out on wafers without thermocouples. The radiant source consists of two banks of six tungsten lamps which are controlled by a microprocessor. These lamps can heat a wafer from 25 to 1200 °C in less than 3 s.

Multilayer structures consisting of alternating undoped and p^+ regions were fabricated to study layer thickness control and the abruptness of doping profiles. Samples were chemically cleaned and loaded into the LRP chamber. Multiple layers were then deposited sequentially *in situ* by changing the gas composition between high-temperature cycles. A typical processing procedure is shown below. *Note that the temperature transients for heating and cooling the wafer are on the order of three seconds, and that the wafer is cooled after*

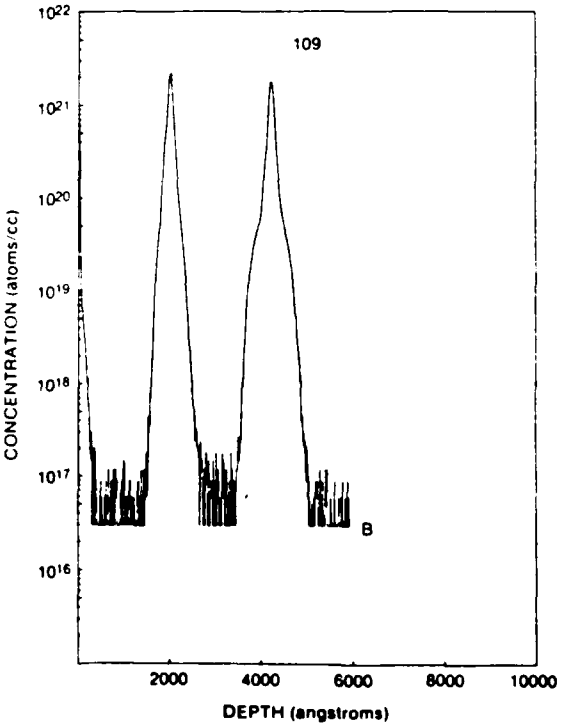


FIG. 1. SIMS profile of multilayer sample LRP 109. The incident beam was oxygen at 10 kV with a substrate bias of − 5 kV (Charles Evans and Associates). The first p^+ pulse deposited shows a slight amount of diffusion caused by the thermal cycles of subsequent layers.

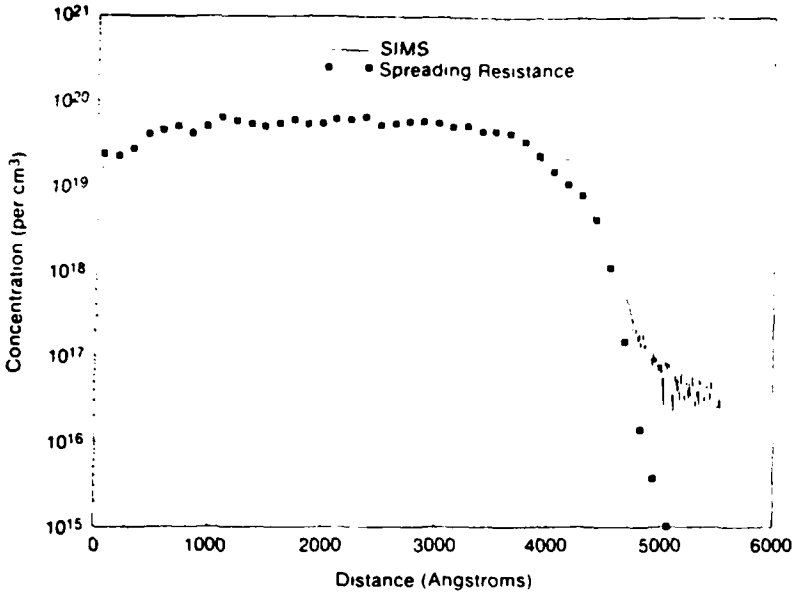


FIG 2 Comparison of the SIMS (Charles Evans and Associates) and spreading resistance (Solecon Labs) profiles for sample LRP 82. The SIMS data are accurate only to about a factor of 2, so the level of boron activation depicted here is approximate.

each temperature cycle so that it is hot only for the time specified for each processing step.

(1) H_2 purge.

(2) H_2 bake at 1150 °C for 60 s at 500 Torr, 3 lpm.

(3) Cool, decrease pressure to 4.2 Torr, introduce SiH_4, let gas flow stabilize.

(4) Epitaxial deposition of undoped silicon in the range of 850–950 °C for 60 s.

(5) Cool, change H_2 to 5.2 ppm B_2H_6 in H_2, let gas flow stabilize.

(6) Epitaxial deposition of p^+ silicon in the range of 850–950 °C for 5–10 s.

(7) Repeat steps (3)–(7) for multiple p^+ "pulse" regions. Dichlorosilane was also used as a silicon source gas with similar results.

A typical secondary ion mass spectroscopy (SIMS) profile of a sample with two p^+ regions is shown in Fig. 1. p^+ pulses with a full width at half-maximum value of 10 nm can be reproducibly deposited. The boron concentration for sample LRP 109 changes four orders of magnitude, from 10^{17} to 10^{21} atoms/cm^3, over a distance of less than 40 nm (10 nm/decade). For comparison, undoped/p^+/undoped multilayer structures deposited by MBE exhibit boron doping transitions of about 10 nm/decade.[2] These transition values are limited by the depth resolution of SIMS. Clearly, however, the p^+ multipulse sample shown in Fig. 1 demonstrates that LRP can produce ultrathin, highly doped films of epitaxial silicon with excellent control of layer thicknesses and doping profiles.

For electrical measurements, p^+ layers (0.1–0.6 μm) were deposited on n-type substrates. Figure 2 shows SIMS and spreading resistance data for sample LRP 82. The spreading resistance curve was scaled by matching its integrated carrier concentration to the value determined by Van der Pauw measurements. The Van der Pauw technique was also used to measure a sheet resistivity of 58 Ω/□ and a hole mobility of 42 cm^2/V s for sample LRP 82. This value of mobility is comparable to that of bulk material with the same hole concentration.[3]

By comparing the chemical concentration of dopant determined by SIMS with the hole concentration determined by spreading resistance, the degree of boron activation can be estimated. However, since the SIMS data are accurate only to about a factor of 2, the level of activation is difficult to determine. The highest hole concentrations measured by spreading resistance and Van der Pauw were in the range of 2×10^{20} cm^{-3}. For some samples, SIMS indicated significantly higher boron concentrations. Thus, inactive boron is probably present, the nature of which is currently being investigated. Previous transmission electron microscopy studies have shown boride particles in heavily doped p^+ bulk material.[4] Annealing experiments are being conducted to learn more about LRP boron incorporation and activation.

A dilute Schimmel etch[5] was used to characterize defect levels. Few defects ($< 10/cm^2$) were found for low-doped epitaxial layers deposited on p^+ substrates, while higher levels (about 3000/cm^2) were found for epitaxial layers deposited on n-type substrates. We are investigating this substrate dependence which may be caused by an internal gettering mechanism. In addition, some of the more heavily doped p^+ layers exhibited a very fine matte or slightly rough surface after defect etching which may be an indication of boride precipitates. It should be noted that these results were obtained without a clean room.

In summary, the fabrication of ultrathin regions of single crystal silicon with high doping densities and excellent electrical properties has been demonstrated using LRP. The ability to produce multilayer structures with sharp interface transitions suggests applications as diverse as those ascribed to MBE. We are currently exploring the use of LRP to fabricate devices based on multiple layers of semiconductors and insulators.

The authors appreciate the support of D. A. Reynolds and DARPA (contract no. DAAG29-85-K-0237), as well as the contributions of J. Hoyt, K. Lee of Bell Labs, C. Evans of Evans and Associates, the staff of the Stanford I. C. Lab, and Lockheed Corporation. C. Gronet acknowledges the support of an Office of Naval Research Fellowship.

[1] J. F. Gibbons, C. M. Gronet, and K. E. Williams, Appl. Phys. Lett. **47**, 721 (1985).
[2] R. A. Kubiak, W. Y. Leong, and E. H. Parker, in *Silicon Molecular Beam Epitaxy*, edited by J. C. Bean (Electrochemical Society, Pennington, NJ, 1985), Vol. 85-7, p. 169.
[3] G. Masetti, M Severi, and S. Solmi, IEEE Trans. Electron Devices ED-30, 764 (1983).
[4] A. Armigliato, D. Nobili, P. Ottoja, M. Servidori, and S. Solmi, in *Semiconductor Silicon 1977*, edited by H. Huff and E. Sirtl (Electrochemical Society, Princeton, NJ, 1977), Vol 77-2, p. 637.
[5] V. D. Archer, J. Electrochem. Soc. **129**, 2074 (1982).

282 IEEE ELECTRON DEVICE LETTERS, VOL. EDL-7, NO. 5, MAY 1986

Limited Reaction Processing: *In-Situ* Metal–Oxide–Semiconductor Capacitors

J. C. STURM, MEMBER, IEEE, C. M. GRONET, AND J. F. GIBBONS, FELLOW, IEEE

Abstract—**Limited reaction processing (LRP) has been used to fabricate *in-situ* silicon–silicon dioxide–polycrystalline silicon layers for metal–oxide–semiconductor (MOS) capacitors. The process consists of multiple *in-situ* rapid thermal processing steps to grow or deposit different layers. Capacitors have been fabricated from these layers and analyzed by capacitance–voltage measurements for interfacial fixed charge and interface state density. The capacitors exhibit excellent characteristics.**

I. Introduction

THE metal–oxide–silicon (MOS) capacitor structure forms a crucial element in modern integrated circuit technology. The capacitor typically consists of an insulating layer (silicon dioxide) grown thermally on a polished silicon wafer. A conducting layer (originally metal but now usually heavily doped polycrystalline silicon) is then deposited on the insulator to form the "gate" electrode. Conventionally, the oxide is grown in one reactor and the wafer is physically transported to a second reactor for the polycrystalline silicon (polysilicon) deposition.

We report here the *in-situ* fabrication of the multilayer MOS structure using multiple rapid thermal processing steps. *In-situ* multilayer fabrication might avoid the inevitable chemical and particulate contamination that occurs when wafers are carried from the oxidation furnace to the polysilicon reactor. Such contamination could diffuse through the oxide during later high-temperature steps to the substrate-oxide interface where it would affect the performance of MOSFET's, etc.

II. Fabrication

Various individual rapid thermal processing steps such as silicon epitaxy [1] and thermal oxidation [2]–[4] have already been demonstrated in separate reactors. However, by changing the ambient gases between high-temperature cycles (from oxygen to silane, e.g.), multiple thin layers of different composition (oxides, polysilicon, etc.) can be grown in a single reactor without removing the sample from the processing chamber. In our experiments, the "limited reacton processing" (LRP) system described in [1] was used for the multiple-level *in-situ* growth. Because the system is essentially a cold wall reactor without a susceptor, only the wafer gets heated during a deposition or growth cycle. Thus "history" effects from one cycle to the next from wall and susceptor deposition should be negligible.

To fabricate the capacitor structure, the two steps of rapid gate oxidation and polysilicon deposition were sequentially performed in the LRP chamber without disturbing the wafer between the steps. The wafers used for the experiments were 2-in diameter phosporus-doped (100) silicon wafers with a resistivity of $\sim 3\ \Omega\cdot$cm. After a chemical cleaning, the wafers were loaded into the LRP chamber. The gate oxidation was performed in an oxygen ambient with 4-percent HCl at a temperature of 1150°C and a pressure of 500 torr. A typical oxidation time of 2 min yielded an oxide thickness of from 290 to 310 Å. Because of the reduced pressure and relatively short time at high temperature, a direct comparison of the oxide thickness to that expected with conventional equipment is not possible. After the high-temperature step, the process gases were changed, and a layer of heavily boron-doped polysilicon was deposited using a combination of silane, diborane, and hydrogen as the source gases. It should be noted that the source gas flow was stabilized before the heating lamps were turned on, so that the wafer temperature and not the gas flows determined the start and stop of the deposition reaction. The polysilicon layers were deposited at 580°C at a pressure of 1.5 torr. The layer thickness was about 0.4 μm, and the sheet resistivity of the layers ranged from 50 to 100 Ω. Conventional deposition of "polysilicon" below 600°C usually results in amorphous rather than polycrystalline material [5]. However, defect etching indicated that our deposited polysilicon layers were indeed polycrystalline. We have not pursued the cause of this result.

To provide a comparison with conventional processing, a control wafer was processed exactly as above, except that it was removed from the LRP chamber after the oxidation and given a chemical cleaning to simulate conventional handling. It was then reloaded into the LRP chamber for the polysilicon gate deposition.

After the polysilicon deposition, conventional processing and photolithography were performed on all samples to change the uniform layers (Fig. 1(a)) into the final capacitor structure shown in Fig. 1(b). The final processing step was a 375°C forming gas anneal (90-percent N_2, 10-percent H_2).

III. Results

Conventional high- and low-frequency capacitance–voltage (CV) measurements were performed to measure the quality of the substrate silicon–silicon dioxide interface (see [6] for a

Manuscript received January 9, 1986; revised February 25, 1986. C. M. Gronet was supported by an ONR Fellowship. This work was supported by DARPA under Contract DAAG29-85-K-0237.

The authors are with Stanford Electronics Laboratories, Stanford University, Stanford, CA 94305.

IEEE Log Number 8608606.

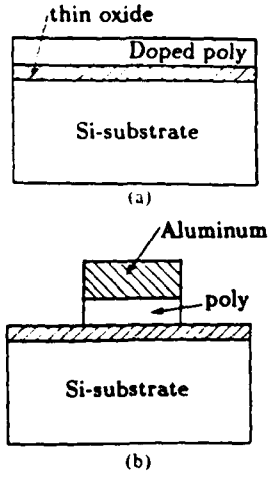


Fig. 1. (a) The structure created *in situ* by LRP and (b) the finished capacitor structure.

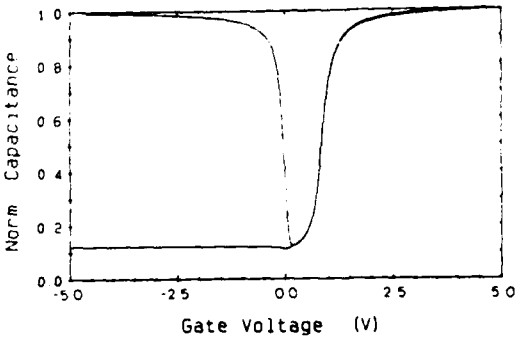


Fig. 2. Typical *CV* curves for an *in-situ* MOS capacitor (1150°C 15-s anneal) with an area of 4.5×10^{-3} cm^2. The capacitance values have been normalized to the maximum capacitance of 504 pF.

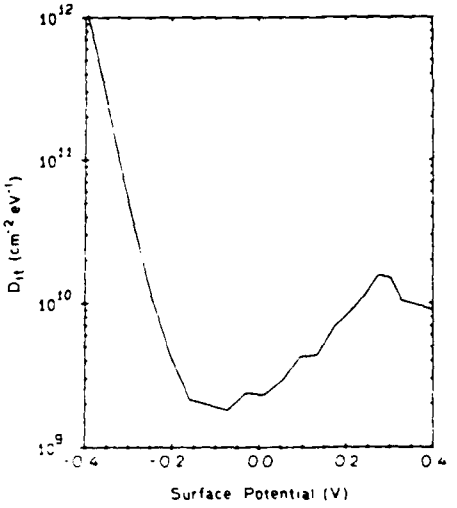


Fig. 3. Interface state density as a function of position in the bandgap for the capacitor of Fig. 2.

good review of *CV* techniques). From the high-frequency curve, the oxide thickness, substrate doping, and the interfacial fixed charge N_f can be extracted. From a combination of the two curves, the interface state density D_{it} can be calculated [6], [7]. The capacitor area was 4.5×10^{-3} cm^2. Several capacitors were measured on each sample for statistical significance. The effect of mobile ions on N_f, as revealed by bias-temperature stress measurements, was less than 1×10^{10} cm^{-2}.

The measured high- and low-frequency *CV* curves exhibited the classical shape [6], and the extracted interface state density of all samples yielded the conventional *U*-shaped curve with a minimum near midgap. The extracted substrate dopings were consistent with the resistivities of the starting wafers. Both the *in-situ* sample (LRP 91) and the sample that received an external chemical cleaning between the oxidation and the polysilicon deposition (LRP 90) showed midgap interface state densities of $2\text{–}3 \times 10^{10}$ cm^{-2}·eV^{-1}. Sample LRP 91 had an interfacial fixed charge of $2.5 \pm 0.1 \times 10^{11}$ cm^{-2}, compared to a fixed charge of $2.1 \pm 0.1 \times 10^{11}$ cm^{-2} for sample LRP 90.(A difference in work functions between the gate and an intrinsic substrate Φ_{ms} of 0.54 eV was assumed [8].) Fixed charges and interface state densities in these ranges are typical for conventional thermal oxides grown at 1150°C and not annealed at high temperature in an inert ambient [9]. It is not known if the difference in fixed charge between the two samples is significant or represents a normal run-to-run variation. It is possible that removing LRP 90 from the chamber and subjecting it to a chemical cleaning would lead to a different Φ_{ms} than for the sample processed *in situ* because of an interfacial dipole layer [8].

After the polysilicon deposition, one of the samples processed *in situ* received a further 1150°C 15-s anneal in an argon ambient. It is well known that such anneals improve interface quality [4], [9], [10]. The high- and low-frequency *CV* curves for this sample are shown in Fig. 2, and the interface state density is shown in Fig. 3. With the anneal, the midgap interface state density decreased to $\sim 5 \times 10^9$ cm^{-2} eV^{-1}, indicative of an excellent interface. The fixed charge measured $0 \pm 1 \times 10^{10}$ cm^{-2}. Although such a interface charge is unusual, an error in the assumed Φ_{ms} of only 0.03 eV would change the calculated N_f by 2×10^{10} cm^{-2}.

To further probe the oxide quality, tunneling current measurements were performed. Fig. 4 shows the tunneling current in an annealed, *in-situ* polysilicon capacitor of area 4.5×10^{-3} cm^2. The gate was biased positive to inject electrons from the substrate into the oxide. (Because of a larger barrier height [11], hole tunneling from the gate into the oxide can be ignored.) The voltage was scanned five times, but the first four times the scan was stopped 4 V before destructive breakdown. The fact that the curves fall on top of one another indicates good oxide stability. On the fifth scan, the voltage was increased until breakdown. The breakdown field of 10 MV/cm is that expected for high-quality SiO_2 films.

IV. Summary

In summary, the use of limited reaction processing to fabricate *in-situ* multiple layers for MOS capacitors has been demonstrated. The fabricated capacitors exhibit excellent characteristics. The ability to deposit gate electrode layers *in*

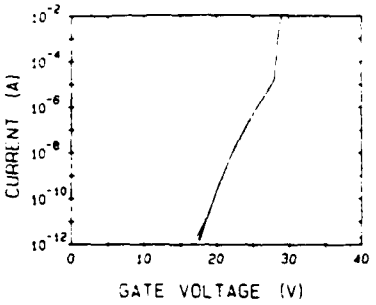


Fig. 4. Tunneling current for a capacitor annealed at high temperature.

situ should provide a useful tool for studying gate electrode-semiconductor work function differences. Larger scale experiments are still needed, however, to evaluate the process yield and uniformity implications of *in-situ* multiple layers.

Acknowledgment

The authors appreciate the continued interest of Dr. R. A. Reynolds. The authors thank K. Williams for his assistance with the LRP apparatus and also thank M. Prisbe and the rest of the staff of the Stanford I.C. Lab.

References

[1] J. F. Gibbons, C. M. Gronet, and K. E. Williams, "Limited reaction processing: Silicon epitaxy," *Appl. Phys. Lett.*, vol. 47, pp. 721-723, 1985.

[2] J. Nulman, J. P. Krusius, and A. Gat, "Rapid thermal processing of thin gate dielectrics—Oxidation of silicon," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 205-207, 1985.

[3] J. Nulman, J. Scarpulla, T. Mele, and J. P. Krusius, "Electrical characteristics of thin gate implanted MOS channels grown by rapid thermal processing," in *IEDM Tech. Dig.*, 1985, pp. 376-379.

[4] A. Gat, "Rapid thermal processing of gate dielectrics," *Semiconductor Int.*, vol. 8, pp. 120-124, May 1985.

[5] T. I. Kamins, M. M. Mandurah, and K. C. Saraswat, "Structure and stability of low pressure chemically vapor-deposited silicon films," *J. Electrochem. Soc.*, vol. 125, pp. 927-932, 1978.

[6] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982.

[7] M. Kuhn, "A quasi-static technique for MOS C-V and surface state measurement," *Solid State Electron.*, vol. 13, pp. 873-885, 1970.

[8] T. W. Hickmott and R. D. Isaac, "Barrier heights at the polycrystalline silicon-SiO_2 interface," *J. Appl. Phys.*, vol. 52, pp. 3464-3475, 1981.

[9] B. E. Deal, "The current understanding of charges in the thermally oxidized silicon structure," *J. Electrochem. Soc.*, vol. 121, pp. 198C-205C, 1981.

[10] A. I. Akinwande, C. P. Ho, and J. D. Plummer, "Experimental determination of the temperature dependence of argon annealed fixed oxide charge at the Si/SiO_2 interface," *Appl. Phys. Lett.*, vol. 45, pp. 263-265, 1984.

[11] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim tunneling into thermally grown SiO_2," *J. App. Phys.*, vol. 40, pp. 278-283, 1969.

Minority-carrier properties of thin epitaxial silicon films fabricated by limited reaction processing

Paper # 4

J. C. Sturm, C. M. Gronet, and J. F. Gibbons
Stanford Electronics Labs, Stanford University, Stanford, California 94305

(Received 2 December 1985; accepted for publication 28 February 1986)

Generation lifetimes and diode properties have been measured in epitaxial silicon films grown by limited reaction processing. Generation lifetimes from 1.4 to 94 μs were measured by observing the recovery of MOS capacitors from deep depletion. Planar diodes fabricated in both *n*- and *p*-type epitaxial films show excellent behavior in both forward and reverse bias. *p*-*n* junctions formed by growing *p*-type epitaxial silicon directly on an *n*-type substrate show no evidence of excessive interface defects or traps.

Limited reaction processing (LRP) is a new technique for fabricating thin semiconductor and insulator layers by controlled high-temperature surface reactions.[1] In an earlier letter, the growth of thin epitaxial silicon layers with extremely abrupt doping profiles was described. The film quality was evaluated in our laboratory by both Rutherford backscattering (RBS)[1] and by majority-carrier mobility measurements. These measurements both showed the material to be indistinguishable from single-crystal silicon substrates. However, these techniques do not provide very exacting tests of crystal quality. Minority-carrier properties and devices provide a much more stringent and ultimately more practical test of the quality of semiconductor layers. In this communication we report the results of generation lifetime measurements and *p*-*n* junction formation in LRP epitaxial silicon films.

The LRP technique uses the sample temperature to control the start and stop of surface reactions (such as epitaxial growth or oxidation), rather than using the gas flows as is conventionally done. The wafer temperature can be rapidly and reproducibly controlled using radiant heating from lamp banks controlled by microprocessors. (Others have used radiant lamp heating to control the wafer temperature for epitaxial growth, but they have used the gas flows, as opposed to the sample temperature as done here, to control the start and stop of the growth process.[2]) Because the LRP technique minimizes the time a wafer is exposed to high temperature, it has the ability to grow ultrathin epitaxial layers with the detectable transition thickness approaching those of molecular beam epitaxy (MBE).[1,3]

The epitaxial films grown by LRP studied here were typically 2–3 μm thick and had carrier concentrations on the order of 5×10^{16} cm^{-3}. *n*-type films were grown on Sb-doped *n*-type (100) 2-in. silicon substrates with a resistivity of $\sim$0.02 Ω cm, and *p*-type films were grown on boron-doped *p*-type (111) substrates with a resistivity of $\sim$0.05 Ω cm. The source gases for the growth were silane and diborane in a hydrogen carrier for the *p*-type samples, and dichlorosilane for the *n*-type samples. The deposition temperature was in the range of 850–950 °C, the growth pressure was 4.2 Torr, and the growth rate varied from 0.5 to 1.0 μm/min.

The minority-carrier generation lifetimes were measured in the epitaxial films by the technique of deep depletion recovery of MOS capacitors described in principle by Zerbst.[4] The capacitors were formed by oxidizing the epitaxial layers in a steam ambient at 1000 °C to give an oxide thickness of about 650 Å. A high-temperature anneal, metal evaporation, lithography, and patterning, and a 450 °C forming gas anneal completed the fabrication of the test structure. For control purposes, test capacitors were also fabricated directly in both *n*- and *p*-type (100) Czochralski single-crystal substrates, with doping levels comparable or lower than those in the epitaxial films. During the measurements, a computerized feedback system was used to adjust the gate voltage to hold the depletion width (and, hence, the generation volume) constant.[5,6] Guard rings were used to minimize lateral effects. This is especially important for lightly doped layers. Five to ten capacitors were measured on each sample.

The results of the generation lifetime measurements are shown in Table I. In all cases there was some random variation in the measured lifetimes, but the generation lifetimes in the LRP samples were consistently in the range of microseconds for *n*-type epitaxial films and tens of microseconds for *p*-type epitaxial films. Why the *p*-type sample yielded longer lifetimes than the *n*-type sample is not known. While the lifetimes for the LRP films were roughly an order of magnitude lower than those found in the virgin Czochralski wafers, they nevertheless represent excellent material. Generation lifetimes in the 10 μs range are common for epitaxial silicon films used for very large scale integration (VLSI) processing.[7]

The simplest minority-carrier device is a *p*-*n* junction diode. Planar diodes were fabricated in the LRP epitaxial layers described earlier by ion implantation and annealing. The implants were masked by deposited oxide which was lithographically patterned. A dose of 1×10^{15} cm^{-2} of 50-keV BF_2^+ ions was implanted into an *n*-type epitaxial layer and annealed at 1000 °C for 3 min to create p^+-*n* diodes. As^+ ions (100 keV, 2×10^{15} cm^{-2}) were implanted in a *p*-type epitaxial layer and annealed for 20 s at 1000 °C to create n^+-*p* diodes. The depth of the annealed junctions was on the order of 0.2 μm in both cases, much less than the 2–3 μm thickness of the epitaxial layers. Because the implanted layers were heavily doped, the junction depletion regions were primarily in the lightly doped unimplanted epitaxial material under the heavily doped surface layers. Since the performance of *p*-*n* junctions is strongly dependent on the material

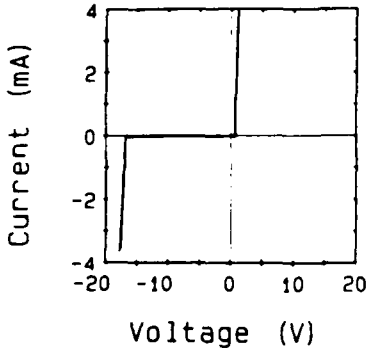


FIG. 1. Typical curve-tracer characteristics for an n^+-p diode.

quality in the depletion region, these diodes should be a good probe of the "as-grown" epitaxial material. Metal contact formation and a forming gas anneal completed the diode fabrication.

Both the n^+-p and p^+-n diodes had well-behaved curve-tracer characteristics (Fig. 1) and had breakdown voltages consistent with the doping of the epitaxial films (24 V for the p^+-n diodes, 16 V for the n^+-p diodes). More interesting is the low current behavior of the diodes in forward bias. A commonly used measure of semiconductor junction quality is the diode quality factor commonly referred to as "n." The quality factor describes how fast the diode current increases in forward bias compared to the ideal maximum slope (59 mV/decade of current at room temperature, $n = 1.00$). In diodes in material with very low lifetimes, the forward current will be dominated by recombination at defects in the depletion region, leading to a slope of 2×59 or 118 mV/decade ($n = 2.00$).[8]

Figure 2 shows the current-voltage relationship of a typical p^+-n diode in forward bias. From the linear portion of the curve on this semilogarithmic plot, a diode quality factor of 1.05 is found. The diode quality factor for the n^+-p diodes was 1.10. Control diodes in Czochralski substrates had a quality factor of 1.00–1.03. The reverse-bias leakage current was measured on p^+-n diodes in the LRP films with an area of 3.4×10^{-4} cm^2. A typical leakage current at a reverse bias of 5 V was 7 pA. Using a simple one-dimensional

TABLE I. Generation lifetimes for LRP epitaxial layers and control Czochralski (CZ) wafers.

Sample	Doping type and orientation	Doping level (cm^{-3})	Generation lifetime (μs)
CZ	n-(100)	2×10^{15}	49–87
LRP	n-(100)	2.5×10^{15}	1.4–4.3
CZ	p-(100)	7×10^{15}	144–203
LRP	p-(100)	7×10^{15}	14–94

approximation for the depletion region width, a generation lifetime in the epitaxial film of 4 μs can be calculated to be consistent with the observed currents. This lifetime is within the range of those measured by the deep depletion recovery method (Table I).

Because defects and generation-recombination centers can lower lifetimes by many orders of magnitude, the relatively good lifetimes and diode performance indicate that the LRP epitaxial layers are of rather high quality. Good films suggest accurate alignment of the first epitaxial layers nucleated during the temperature ramp-up in the LRP deposition cycle. This is fortunate because these layers serve as templates for subsequent growth, and a few poor initial layers would likely result in a low-quality film. (Low-temperature deposition for long times results in poor epitaxial alignment or even polycrystalline growth.) Apparently, the rate of increase of the sample temperature (room temperature to ~ 900 °C in ~ 3 s) is fast enough to avoid such problems.

To further examine the epitaxial layer–substrate interface, p-n junctions were formed by growing p-type epitaxial silicon films (thickness ~ 2 μm, doping $\sim 5 \times 10^{17}$ cm^{-3}) directly on the n-type silicon substrates described earlier. The depletion regions associated with the junctions should then include the substrate interface. Individual p-n diodes were formed by aluminum deposition and patterning followed by silicon mesa etching. Note that no ion implantation or high-temperature annealing was required to create the diodes. The forward-bias characteristics of three diodes of different area is shown in Fig. 3. Note that the current scales as the area of the diodes. The diodes exhibit an ideality factor of 1.05, indicating a minimum of defects in the depletion

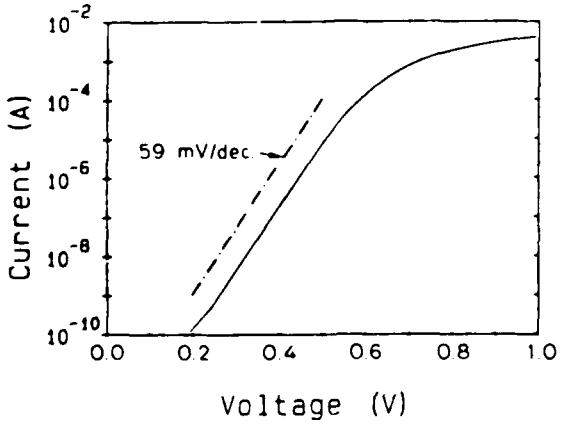


FIG. 2. Typical current-voltage relationship for a p^+-n diode in forward bias. The diode area was 3.4×10^{-4} cm^2.

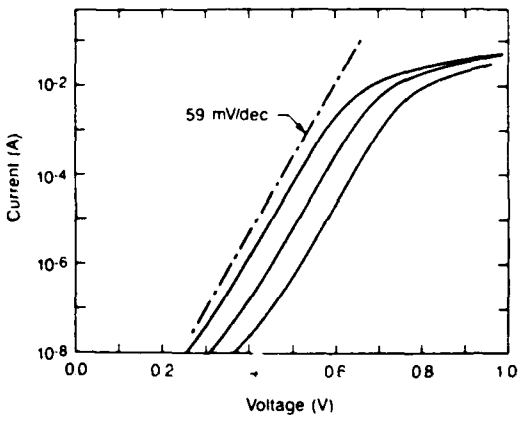


FIG. 3. Forward bias characteristics of substrate–epitaxial layer n-p diodes. The diode areas are 4.9×10^{-3}, 5.1×10^{-4}, and 4.8×10^{-4} cm^2.

region and, hence, negligible defects at the substrate interface. Thus, the temperature transient during the beginning of the LRP growth cycle appears to have had no adverse affects on the electrical properties of the substrate-epitaxial layer interface. The actual atomic quality of the epitaxial layer-substrate interface is currently under further investigation.

In summary, the minority-carrier properties of silicon epitaxial films grown by limited reaction processing have been investigated. The films exhibit relatively high lifetimes (1–100 μs) and good diode characteristics. Furthermore, the substrate–epitaxial layer interface shows no evidence of excessive traps or recombination centers. High-quality films and interfaces combined with the ability to grow 10-nm layers[3] should make LRP a useful tool for the fabrication of high-performance electronic devices.

The authors appreciate the support of Dr. R.A. Reynolds and the Defense Advanced Research Projects Agency (contract no. DAAG29-85-K-0237). One of the authors (C.M. Gronet) is supported by a fellowship from the Office of Naval Research. The authors also thank K.E. Williams for the construction of the LRP apparatus and thank S. Bernard and the rest of the staff of the Stanford Integrated Circuit Lab.

[1]J. F. Gibbons, C. M. Gronet, and K. E. Williams, Appl. Phys. Lett. **47**, 721 (1985).
[2]V. J. Silvestri and G. R. Srinivasan, J. Electrochem. Soc. **131**, 877 (1984).
[3]C. M. Gronet, J. C. Sturm, K. E. Williams, and J. F. Gibbons, Appl. Phys. Lett. **48**, 1012 (1986).
[4]M. Zerbst, Z. Angew. Phys. **22**, 30 (1966).
[5]R. F. Pierret and D. W. Small, IEEE Trans. Electron Devices **ED-22**, 1051 (1975).
[6]W. D. Eades, J. D. Shott, and R. M. Swanson, IEEE Trans. Electron Devices **ED-30**, 1274 (1983).
[7]J. O. Borland, C. I. Drowley, Solid State Technol. **28**, 141 (Aug., 1985).
[8]A. S. Grove, *Physics and Technology of Semiconductor Devices* (Wiley, New York, 1967), pp. 186–191.

Paper # 5

In-Situ Epitaxial Silicon–Oxide-Doped Polysilicon Structures for MOS Field-Effect Transistors

J. C. STURM, MEMBER, IEEE, C. M. GRONET, C. A. KING, STUDENT MEMBER, IEEE, S. D. WILSON, AND J. F. GIBBONS, FELLOW, IEEE

Abstract—**Limited reaction processing (LRP) has been used to achieve the *in-situ* growth of epitaxial silicon–oxide-doped polysilicon layers. The *in-situ* growth of these multiple layers was combined with the selective epitaxial growth technique to create structures for MOSFET fabrication. The results of n- and p-channel transistor fabrication utilizing these structures are presented.**

I. Introduction

THE silicon substrate–oxide-doped polysilicon structure forms the heart of the modern MOSFET. For some CMOS isolation techniques, a silicon epitaxial layer is added to create a substrate–epi–oxide–polysilicon sandwich [1]–[4]. Conventionally, these layers are each fabricated in a separate step in a separate reactor, and the wafers must be physically transported from one reactor to another. In this letter we report the *in-situ* fabrication of epi–oxide–polysilicon structures and present the performance of n- and p-channel MOSFET's fabricated using these structures.

The multiple-layer structures were fabricated using the limited reaction processing (LRP) technique [5]. This method uses rapid changes in sample temperature to control the growth or deposition of thin high-quality semiconductor or insulator layers. The LRP system has been described previously [5]. It consists of a quartz reaction tube surrounded by microprocessor-controlled tungsten lamps. One end of the reaction tube is connected to a gas control system which can supply several conventional processing gases such as Ar, O_2, SiH_4, etc. The other end is connected to a low-pressure pumping apparatus. Silicon samples in the reaction tube can be brought to typical processing temperatures (e.g., 1000°C from room temperature) in a matter of seconds. By changing the process gases in the reaction tube between high-temperature cycles, multiple semiconductor and insulator layers may be sequentially grown or deposited *in situ*, i.e., without removing the wafer from the reaction chamber.

We have previously used this technique for the sequential *in-situ* growth of a thin oxide and then the deposition of doped polysilicon for the fabrication of MOS capacitors [6]. However, that work did not include an epitaxial silicon layer and was not extended to a fabrication process for MOSFET's.

Manuscript received April 28, 1986; revised August 13, 1986. This work was supported by DARPA under ARO Contract DAAG29-85-K-0237. C. M. Gronet was supported by an ONR fellowship.

J. C. Sturm was with Stanford Electronics Laboratories, Stanford University, Stanford, CA 94305. He is now with the Department of Electrical Engineering, Princeton University, Princeton, NJ 08544.

C. M. Gronet, C. A. King, and J. F. Gibbons are with Stanford Electronics Laboratories, Stanford University, Stanford, CA 94305.

S. D. Wilson is with Charles Evans and Associates, San Mateo, CA 94402.

IEEE Log Number 8610840.

II. Fabrication

The starting materials for the experiments were (100) Sb-doped n-type silicon wafers for p-channel FET's and (100) B-doped p-type wafers for n-channel devices. Both types of substrates had a resistivity of ~0.01 Ω·cm. Two-inch squares were cut from larger wafers to fit into the limited reaction processing tube. Initially, a uniform field oxide of thickness 6000 Å was grown by wet oxidation at 1100°C in a conventional furnace. Holes in the field oxide for subsequent selective epitaxial growth were then opened using a conventional "diffusion" mask and wet chemical etching. After a chemical cleaning, the wafers were loaded into the LRP chamber and baked in H_2 for 30 s at 1150°C and 1.0 torr. Three successive high-temperature steps were then carried out to create the structure in Fig. 1(a). These steps were: 1) selective epitaxial silicon growth; 2) gate oxidation; and 3) doped polysilicon deposition. The process gases were changed and purge cycles were performed between the high-temperature steps, but the vacuum seal to the chamber was not broken.

The primary source gases used for the epitaxial growth were 7-percent SiH_2Cl_2 and 2-percent HCl in an H_2 carrier. The HCl flow was chosen to achieve selective growth, i.e., to grow epi in the oxide holes but to avoid polysilicon deposition on top of the field oxide. For n-channel MOSFET's, 1.8 μm of p-type epi was grown on a p^+ substrate (sample LRP 169), and 1.8 μm of n-epi was grown on an n^+ substrate for p-channel devices (sample LRP 171). The pressure during the epitaxial growth was 4.2 torr, the wafer temperature was 925°C, and the growth rate was ~ 1 μm/min. The epitaxial layer doping in both cases was 5×10^{16} cm^{-3}. Note that the epitaxial layer was some three times thicker than the field oxide. The detailed nature of the faceting that occurs at the edge of the epitaxial silicon surface [7] was not investigated.

The gate oxidation was performed at 1150°C in an oxygen ambient at a pressure of 500 torr for a period of 60 s. The gate oxide thickness was 140 Å. After the oxidation, heavily doped p-type polysilicon was deposited using silane and diborane at 580°C and 1.5 torr. The polysilicon layer thickness was 0.3 μm.

After the LRP steps, conventional processing (beginning with gate lithography and etching) was carried out to create the MOSFET structures shown schematically in Fig. 1(b). Rapid thermal annealing of the source–drain implants was performed to minimize outdiffusion from the heavily doped substrate.

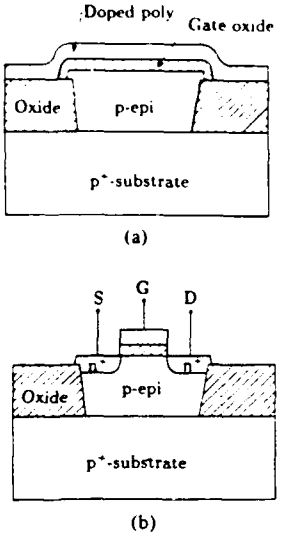


Fig. 1. (a) Multiple-level epi-oxide-poly structure grown *in-situ* by LRP, and (b) the schematic cross section of MOSFET's made from this structure. Note that the actual epitaxial layer in our experiments was three times thicker than the field oxide.

During the back-end processing, the wafers were subjected to a total of 15 min at 900°C. A titanium-aluminum metallization and a 400°C forming gas anneal completed the processing.

III. Results

On-chip capacitor test structures confirmed the gate oxide thickness of 140 Å and showed an epitaxial layer doping of 4–5 × 10^{16} cm^{-3} for both the p and n epitaxial layers. Both the n- and p-channel MOSFET's exhibited qualitatively well-behaved characteristics. A curve-tracer photograph of a typical short-channel n-MOS device is shown in Fig. 2. (The effective channel length of 0.8 μm was determined by measuring the transistor conductance for many different gate lengths at several different gate biases.) The typical performance of a p-channel device (with L_{eff} = 1.0 μm) is shown in Fig. 3.

Threshold voltages and channel mobilities were extracted from long-channel (50-μm) devices in the triode regime. The n-channel transistors had a threshold voltage of 1.25 ± 0.05 V and an electron surface mobility of 490 ± 10-percent $cm^2/V \cdot s$. Given the epi doping concentration of 5 × 10^{16} cm^{-3}, a surface mobility of 600 $cm^2/V \cdot s$ might have been expected [8]. However, the *CV* measurements indicated a surprisingly high fixed charge at the epi Si-SiO_2 interface (N_f ~ 5 × 10^{11} cm^{-2}). Excess scattering caused by these charge centers can reduce surface mobilities [8]. The reason for this large interface charge is not known. The p-channel devices had a threshold voltage of −0.80 ± 0.05 V and a hole mobility of 120 $cm^2/V \cdot s$. The subthreshold behavior of the devices was also well behaved. Both the n- and p-channel devices showed subthreshold slopes of approximately 90 mV/decade. The source (drain)-to-substrate breakdown voltages for both types of devices ranged from 12 to 20 V. Such breakdown voltages are consistent with the measured epitaxial layer doping.

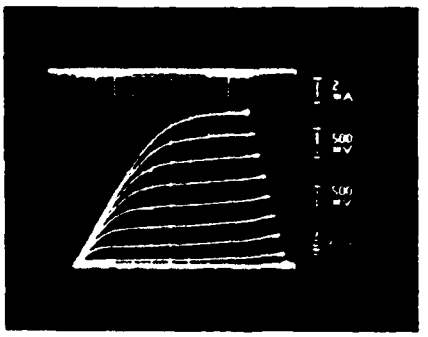


Fig. 2. Curve-tracer characteristics of a typical n-channel device with L_{eff} = 0.8 μm and W = 50 μm.

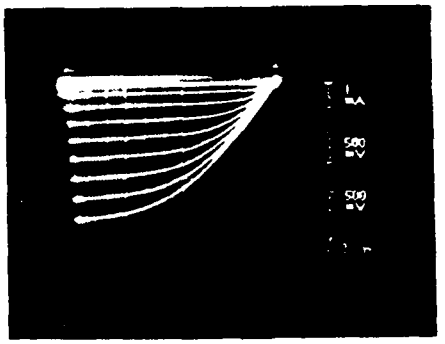


Fig. 3. Curve-tracer characteristics of a typical p-channel device with L_{eff} = 1.0 μm and W = 50 μm.

The low carrier mobilities and the high interfacial charge indicate some material problems at the epitaxial layer-thin oxide interface. Although it is conceivable that the high fixed charge is related to the *in-situ* processing, it is more likely that the selective epitaxial growth step was not properly optimized. Uniform nonselective epitaxial silicon layers grown by LRP have been shown to exhibit excellent material and electrical properties [5], [9]. These include minority-carrier lifetimes in the range of tens of microseconds and electron and hole surface mobilities (for conventionally processed FET's) of 830 and 200 $cm^2/V \cdot s$, respectively. It should be noted that two-step *in-situ* processing (oxidation plus polysilicon deposition) has been found to yield excellent interface quality [6].

IV. Discussion

Multiple-level *in-situ* processing could reduce the inevitable contamination (particulate and chemical) that occurs when wafers are transported from one reactor to another. Cleaner interfaces between layers could lead to greater process uniformity and higher yields. Such considerations could be important for ULSI. However, the scale of the processing in these experiments (2-in wafers and discrete devices) was not sufficient to allow realistic testing of parameters such as threshold uniformity and yield.

Because limited reaction processing minimizes the high-temperature exposure of the wafer, the substrate-epitaxial layer interface remained sharp. A SIMS profile of the B

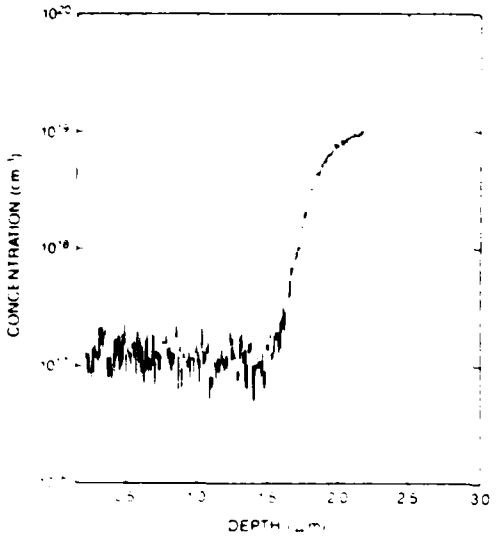


Fig. 4. SIMS profile of the boron doping in the epitaxial layer after the completion of MOSFET processing (sample LRP 169).

doping profile in sample LRP 169 after the completion of the processing shows the B concentration at the interface changes by nearly two orders of magnitude in only 0.3 μm (Fig. 4). Hence the epitaxial layer thickness could have been much thinner than the ~2 μm used in these experiments without adversely affecting the transistors. Note that depositing the polysilicon *in-situ* implies that any implants for threshold shifting would have to be done through the gate polysilicon. As an alternative to such implants, the tight control of dopant profiles offered by LRP may make it possible to tailor the doping of the epitaxial layer during the layer growth. Such a technique would depend on very precise control of the dopant level in the epitaxial material, however.

In this work, n- and p-channel devices were fabricated on separate substrates. Further work is underway to combine both types of transistors onto a common substrate for complementary structures. Such a process will probably require two separate selective epitaxial steps. Because of the oxide isolation and the heavily doped substrates, the complementary structure should be rather immune to latch-up.

V. Summary

The use of limited reaction processing to fabricate multiple-layer semiconductor and insulator structures has been demonstrated. These layers have been used to fabricate both n- and p-channel MOSFET's. Further experiments are necessary to evaluate the yield and process uniformity implications of multiple layer *in-situ* growth. Construction of a large-scale reactor for this purpose is in progress. Combining limited reaction processing with *in-situ* patterning (such as laser beam assisted deposition [10]) may make it possible to someday build a complete circuit without removing the wafer from the processing chamber!

Acknowledgment

The authors thank Dr. R. A. Reynolds of DARPA for his continued interest. The authors also appreciate the assistance of K. E. Williams and thank the staff of the Stanford I.C. Lab.

References

[1] D. B. Estreich, A. Ochoa, Jr., and R. W. Dutton, "An analysis of latch-up in CMOS IC's using an epitaxial-buried layer process," in *IEDM Tech. Dig.*, 1978, pp. 230-234.

[2] J. Manoliu, F. H. Tseng, B. J. Woo, and T. J. Meier, "High-density and reduced latchup susceptibility CMOS technology for VLSI," *IEEE Electron Device Lett.*, vol. EDL-4, pp. 233-235, 1983.

[3] N. Endo, K. Tanno, A. Ishitani, Y. Kurogi, and H. Tsuya, "Novel device isolation technology with selective epitaxial growth," in *IEDM Tech. Dig.*, 1982, pp. 241-244.

[4] S. Nagao, K. Higashitani, Y. Akasaka, and H. Nakata, "Application of selective silicon epitaxial growth for CMOS technology," in *IEDM Tech. Dig.*, 1984, pp. 593-596.

[5] J. F. Gibbons, C. M. Gronet, and K. E. Williams, "Limited reaction processing: Silicon epitaxy," *Appl. Phys. Lett.*, vol. 47, pp. 721-723, 1985.

[6] J. C. Sturm, C. M. Gronet, and J. F. Gibbons, "Limited reaction processing: *In-situ* metal-oxide-semiconductor capacitors," *IEEE Electron Device Lett.*, vol. EDL-7, pp. 282-284, 1986.

[7] D. R. Bradbury, T. I. Kamins, and C.-W. Tsao, "Control of lateral epitaxial chemical vapor deposition of silicon over insulators," *J. Appl. Phys.*, vol. 55, pp. 519-523, 1984.

[8] S. C. Sun and J. D. Plummer, "Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1497-1508, 1980.

[9] J. C. Sturm, C. M. Gronet, and J. F. Gibbons, "Minority carrier properties of thin epitaxial silicon films fabricated by limited reaction processing," *J. Appl. Phys.*, vol. 59, pp. 4180–4182, 1986.

[10] D. J. Ehrlich, R. M. Osgood, Jr., and T. F. Deutsch, "Laser microreaction for deposition of doped silicon films," *Appl. Phys. Lett.*, vol. 39, pp. 957-959, 1981.

Paper # 6

Growth of GeSi/Si Strained-layer Superlattices Using Limited Reaction Processing

C. M. Gronet, C. A. King, and J. F. Gibbons
Stanford Electronics Labs, McCullough 226, Stanford, CA 94305

ABSTRACT

SiGe/Si superlattices were grown using limited reaction processing in a chamber which allows both W-halogen and Hg arc wafer illumination. Each multilayer structure was fabricated *in-situ* by changing the gas composition between high temperature cycles. Commensurate SiGe alloy layers as thin as 15 nm were reproducibly deposited and were examined using transmission electron microscopy, sputtering Auger electron spectroscopy, and Rutherford backscattering. Preliminary results are presented on UV/ozone cleaning of LRP substrates to remove residual carbon contamination *in-situ* prior to film deposition.

INTRODUCTION

In previous papers [1-4], we introduced limited reaction processing (LRP) as a new technique for the *in-situ* fabrication of multiple thin layers of semiconductors and insulators. The key to LRP is precise control of thermally driven surface reactions. By using radiant energy, large changes in the temperature of a semiconductor substrate can be induced very quickly yet controllably. As shown in Figure 1, such rapid temperature changes are used in an LRP cycle as a "switch" to turn a thermally driven surface reaction on and off.

The LRP technique has three significant capabilities or advantages. First, since the substrate is hot only during layer growth, LRP inherently minimizes the thermal exposure of a substrate, reducing the broadening of interfaces by diffusion and intermixing. Second, LRP allows the controlled growth of very thin layers. The accuracy and reproducibility of substrate temperature vs time profiles afforded by lamp heating allows excellent control of the extent of surface reactions. Third, LRP facilitates *in-situ* processing. By changing the ambient gases between high temperature cycles, multiple thin layers of different composition can be grown sequentially without removing the substrate from the processing chamber. Such *in-situ* processing is important for minimizing chemical and particulate contamination which inevitably occurs during wafer handling between conventional layer growth steps.

This paper describes the application of LRP to the deposition of commensurate SiGe/Si superlattices with ultrathin SiGe alloy layers. SiGe alloy layers are attractive because they have a bandgap which can be tailored by changing the Ge composition [5], can be grown epitaxially on silicon [6-8], and are potentially compatible with current silicon processing technology. Molecular beam epitaxy has been used to fabricate SiGe/Si modulation-doped field-effect transistors [9,10] and infrared detectors [11]. Atmospheric pressure chemical vapor deposition (CVD) has been used to deposit SiGe/Si superlattices [8], but alloy layers thinner than 30 nm could not be grown. LRP superlattices exhibit superior layer thickness control, even for layers as thin as 15 nm.

EXPERIMENTAL

One of the LRP systems used to grow SiGe superlattices has been described

previously [1]. A new chamber, shown in Figure 2, was constructed with W-halogen lamps for wafer heating and a low pressure Hg arc grid lamp for *in-situ* UV light processing. The wafer is supported on three quartz pins in a chamber contructed by sealing a water-cooled stainless steel ring between two quartz plates. Temperature calibration is performed using a W/26% Re vs W/5% Re thermocouple which is electron beam welded to the center of a test wafer. Epitaxial films are deposited on wafers without thermocouples by using a power vs time program for a desired temperature vs time cycle.

The substrates used were 2, 3, or 4 inch diameter (100) silicon wafers. Typically the wafers are given a wet chemical clean prior to insertion into the LRP chamber. Next, in some cases, the Si wafer is given an *in-situ* ozone clean using a combination of oxygen and UV light [12-14]. An example of the effectiveness of UV/ozone cleaning for removing residual carbon contamination is shown in Figure 3 [15]. We are currently investigating the effect of UV/ozone cleaning on the material and electrical properties of epitaxial layers. In all cases, immediately before deposition, the wafers were baked in H_2 for 30 - 120 seconds at 1150 - 1200 ^oC. The temperature necessary for this hydrogen bake step may be reduced by prior UV/ozone cleaning since the formation of SiC could be prevented. Oxide alone can be removed at 1000 ^oC or less [16,17]. Lower pre-bake temperatures result in less thermally induced defects (e.g., slip), less thermal exposure of the substrate or underlying structures, and less autodoping. After the H_2 bake step, the wafer is allowed to cool, the desired reactant gases are introduced, and then the film deposition thermal cycle is initiated typically within 60 seconds of the H_2 cleaning step. Si and SiGe films were deposited at 900 ^oC using SiH_4 and GeH_4 diluted in H_2. Typical deposition pressures were 2 - 4 Torr using total flow rates from 1 - 3 lpm.

RESULTS

First single layers of SiGe alloys were grown for material characterization and growth calibration. For example, a film grown for 60 seconds at 900 ^oC and a pressure of 4.2 Torr using 27 ccm SiH_4, 0.7 ccm GeH_4, and 3 lpm H_2 was analyzed using Rutherford backscattering (RBS) and sputtering Auger electron spectroscopy (AES). The film thickness and Ge fraction were 0.37 u and 9%, respectively. The minimum yield, calculated by dividing the total Ge peak channeling yield by the total random yield, was 5.5%, indicating good crystal quality [18]. RBS analysis of a number of samples was used to correlate the sputtering AES yield with Ge mole fraction in the thin SiGe alloy layers.

Commensurate SiGe strained-layer superlattices were grown *in-situ* using multiple LRP cycles. The reactive gas composition was changed while the wafer was cool, in between high temperature cycles. Growth interruption was typically less than 60 seconds. Figure 4 shows AES and cross-section transmission electron microscopy (TEM) data for a typical superlattice [19]. The bright field TEM photograph distinguishes the SiGe and Si layers as dark and light, respectively, and indicate that the growth is commensurate. Plan view images show that the dislocation density is less than 10^6 cm^{-2}.

CONCLUSION

In summary, we demonstrate that LRP can produce ultrathin, high quality Si and SiGe epitaxial layers with thickness and composition control comparable to molecular beam epitaxy. An LRP reactor was constructed with the capability for *in-situ* UV/ozone processing to improve surface cleanliness. Removal of residual

surface contamination is especially critical for heteroepitaxial deposition. Currently, we are investigating SiGe/Si modulation doped structures where LRP offers a key advantage: the ability to easily achieve high active dopant concentrations in very confined regions [3]. Such high doping levels should allow high conductance in SiGe/Si MODFET structures. In addition, we are also investigating the use of SiGe alloys layers deposited *in-situ* prior to silicon epitaxial layers to create a gettering mechanism [20] and improve Si growth conditions [21].

The authors appreciate the contributions of Dr. J. Bravman of the Stanford University Materials Science Department, R. Hull of Hewlett-Packard Labs, Wally Opyd, Shaun Wilson of Charles Evans and Associates, Dr. Jim Sturm, Lockheed Corporation, John Abelson, R. Mercer, R. Helms, and D. A. Reynolds at DARPA (contract DAAG29-85-K-0237). C. Gronet acknowledges the support of an Office of Naval Research Fellowship.

REFERENCES

1. J. F. Gibbons, C. M. Gronet, and K. E. Williams, Appl. Phys. Lett. **47**, 721 (1985).

2. C. M. Gronet, J. C. Sturm, K. E. Williams, and J. F. Gibbons, *MRS Symposium on Rapid Thermal Processing*, Boston, MA, Dec. 1985 (Materials Research Society, Pittsburgh, PA 1986), Vol. 52, p. 305.

3. C. M. Gronet, J. C. Sturm, K. E. Williams, J. F. Gibbons, and S. D. Wilson, Appl. Phys. Lett. **48**, 1012 (1986).

4. J. C. Sturm, C. M. Gronet, and J. F. Gibbons, IEEE Electron Device Lett., **EDL-7**, 282 (1986).

5. J. C. Bean in *Silicon Molecular Beam Epitaxy*, edited by J. C. Bean (The Electrochem. Soc., Pennington, NJ, 1985) Vol. **85-7**, p. 337.

6. J. C. Bean, T. T. Sheng, L. C. Feldman, A. T. Fiory, and R. T. Lynch, Appl. Phys. Lett **44**, 102 (1984).

7. H. Jorke and H.-J. Herzog in *Silicon Molecular Beam Epitaxy*, edited by J. C. Bean (The Electrochem. Soc., Pennington, NJ, 1985) Vol. **85-7**, p. 352.

8. H. M. Manasevit, I. S. Gergis, and A. B. Jones, Appl. Phys. Lett. **41**, 464 (1982).

9. T. P. Pearsall and John C. Bean, IEEE Electron Device Lett., **EDL-7**, 308 (1986).

10. H. Daembkes, H.-J. Herzog, H. Jorke, H. Kibbel, and E. Kaspar, IEEE Trans. on Electron Dev., **Ed-33**, 633 (1986).

11. T. P. Pearsall, H. Temkin, J. C. Bean, and S. Luryi, IEEE Electron Device Lett., **EDL-7**, 330 (1986).

12. M. Tabe, Appl. Phys. Lett., **45**, 1073 (1984).

13. J. R. Vig and J. W. Le Bus, IEEE Trans. on Parts, Hybrids, and Packaging, **PHP-12**, 365 (1976)

14. N. Norstrom, M. Ostling, R. Buchta, and C. S. Petersson, J. Electronchem. Soc., **132**, 2287 (1985).

15. J. R. Abelson, D. Mercer, and C. R. Helms, Stanford University (to be published).

16. A. Ishitani and S. Itoh, *MRS Symposium on Beam-Induced Chemical Processes*, Boston, MA, Dec. 1985 (Materials Research Society, Pittsburgh, PA 1986), extended abstracts, p. 51.

17. T. Tatsumi, N. Aizaki, and H. Tsuya, Jap. J. Appl. Phys., **24**, L227 (1985).

18. J. C. Bean, L. C. Feldman, A. T. Fiory, S. Nakahara, and I. K. Robinson,

J. Vac. Sci. Tech. A, **2**, 436 (1984).
19. R. Hull, J. M. Gibson, and J. C. Bean, Appl. Phys. Lett., **46**, 179 (1985).
20. A. S. M. Salih, J. S. Ryu, G. A. Rozgonyi, and K. E. Bean, J. Electrochem. Soc., **133** 475 (1986).
21. S. Suzuki and T. Itoh, J. Appl. Phys., **54** 1466 (1983).

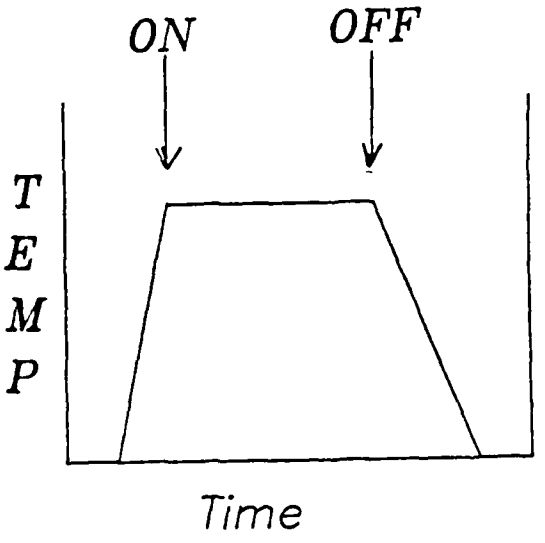


Figure 1 Schematic substrate temperature vs time profile during a typical LRP cycle. Reactive gases are introduced while the wafer is cool, and then the temperature of the substrate is used as a switch to start and stop a thermally driven surface reaction.

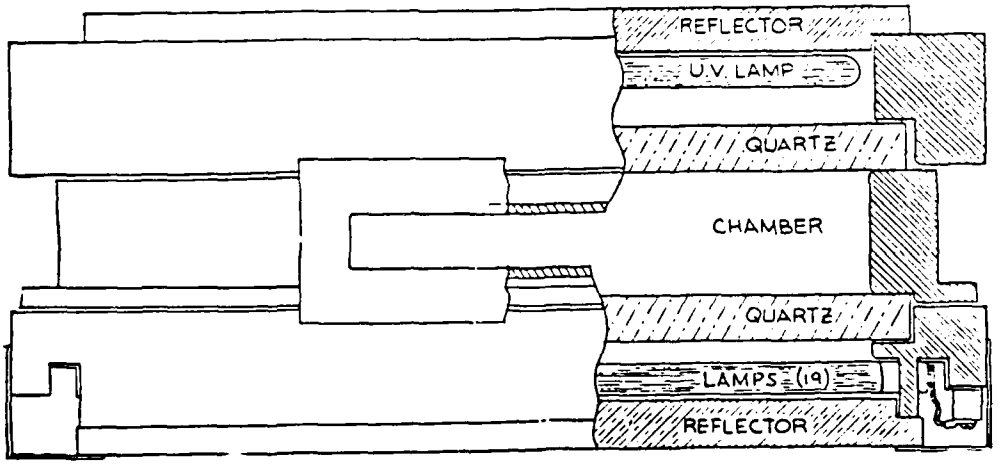


Figure 2 Scale sideview of LRP chamber showing cutaway. The quartz windows are 0.66 inches thick and 11 inches in diameter. The top plate is synthetic quartz for UV transmission. Samples may be loaded through the rectangular port in the side or by opening the top in a clam-shell fashion. 19 - 6 kW W-halogen lamps, 0.5 inches apart, are used for the bottom lamp array. The UV source is an 11 x 11 inch low pressure Hg grid lamp.

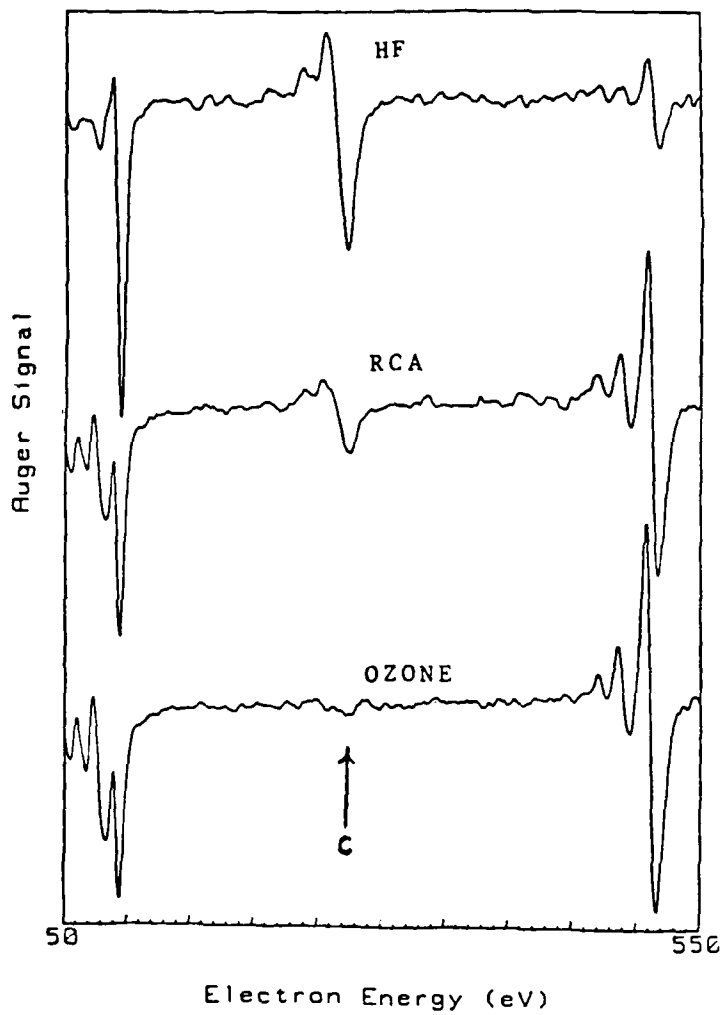


Figure 3 Typical Auger spectra for silicon wafers cleaned using an HF dip, RCA wet chemical clean, and an HF dip followed by an ozone clean. Only the ozone clean is capable of removing all detectable carbon from the silicon surface. Ozone cleaning was performed by placing the wafer in pure oxygen within 2 mm of a low pressure Hg grid lamp for 60 seconds. All samples were inserted into the Auger chamber within 15 minutes of the cleaning procedure.

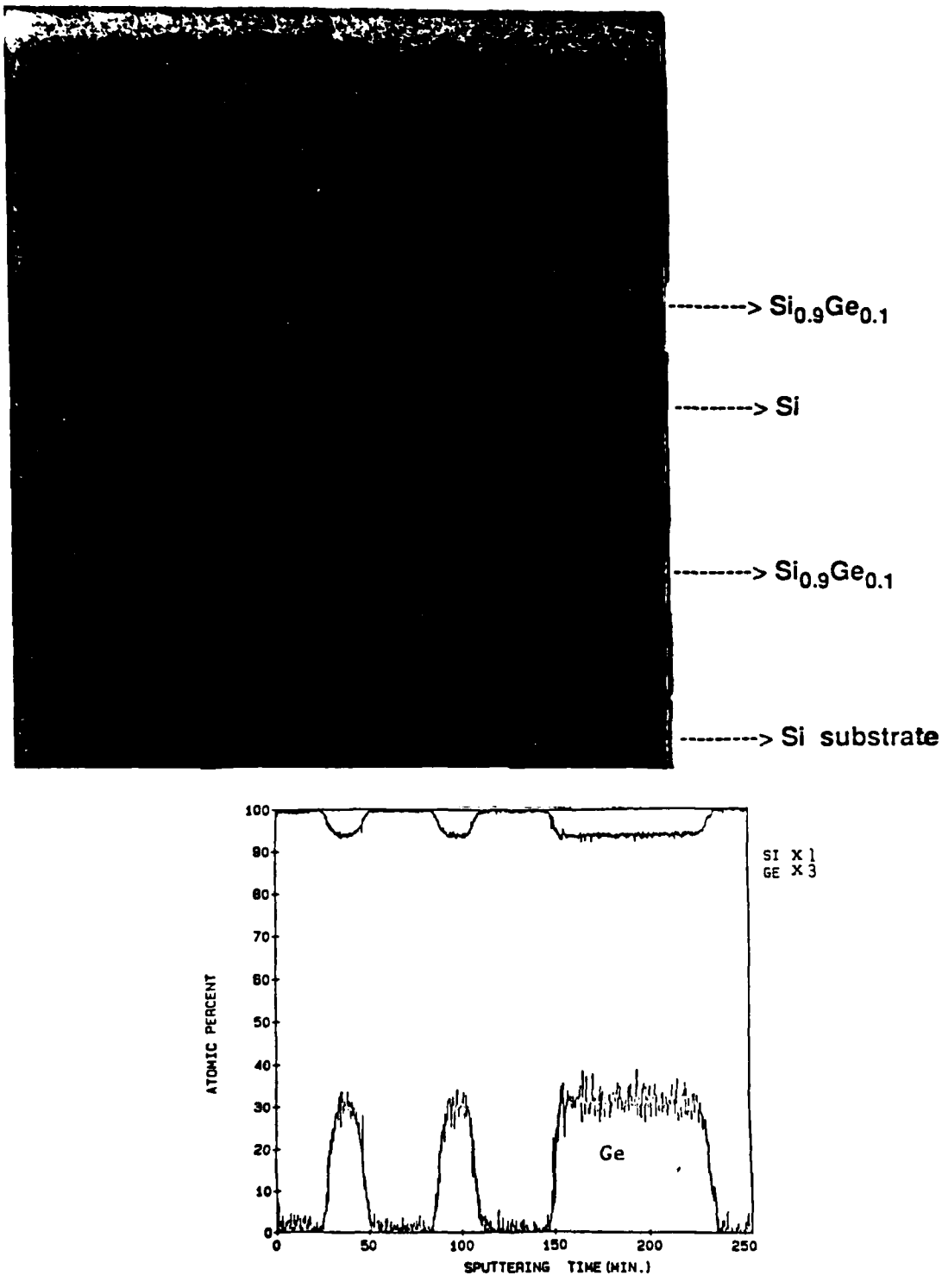


Figure 4 Sputtering Auger spectrum and cross-section TEM for a typical $Si_{0.9}Ge_{0.1}$/Si superlattice structure. The Auger yield was calibrated using RBS data from a number of single alloy layers deposited on silicon. The TEM shows that the growth is commensurate. The thinner alloy layers are 15 nm thick and appear darker in the micrograph.

Paper # 7

Growth of GeSi/Si strained-layer superlattices using limited reaction processing

C. M. Gronet, C. A. King, W. Opyd, and J. F. Gibbons
Stanford University Electronics Laboratories, McCullough 226, Stanford, California 94305

S. D. Wilson
Charles Evans and Associates, San Mateo, California 94402

R. Hull
Hewlett-Packard Laboratories, 3500 Deer Creek Road, Palo Alto, California 94304

(Received 24 June 1986; accepted for publication 7 December 1986)

SiGe/Si superlattices were grown using limited reaction processing. Each multilayer structure was fabricated *in situ* by changing the gas composition between high-temperature cycles. Commensurate SiGe alloy layers as thin as 15 nm were reproducibly deposited and were examined using transmission electron microscopy, sputtering Auger electron spectroscopy, and Rutherford backscattering. Si/SiGe interfaces are abrupt to within a few monolayers, establishing for the first time the use of a chemical vapor deposition technique to fabricate abrupt GeSi/Si-based heterostructures.

In previous letters,[1-4] we introduced limited reaction processing (LRP) as a new technique for the *in-situ* fabrication of multiple thin layers of semiconductors and insulators. The key to LRP is precise control of thermally driven surface reactions. By using radiant energy, large changes in the temperature of a semiconductor substrate can be induced very quickly, yet controllably. Such rapid temperature changes are used in an LRP cycle as a "switch" to turn a thermally driven surface reaction on and off.

The LRP technique has three significant capabilities or advantages. First, since the substrate is hot only during layer growth, LRP inherently minimizes the thermal exposure of a substrate, reducing the broadening of interfaces by diffusion and intermixing. Second, LRP allows the controlled growth of very thin layers. The accuracy and reproducibility of substrate temperature versus time profiles afforded by lamp heating allows excellent control of the extent of surface reactions. Third, LRP facilitates *in-situ* processing. By changing the ambient gases between high-temperature cycles, multiple thin layers of different composition can be grown sequentially without removing the substrate from the processing chamber. Such *in-situ* processing is important for minimizing the chemical and particulate contamination which inevitably occurs during wafer handling between con-

 0021-8979/87/062407-03$02.40

ventional layer growth steps.

This communication describes the application of LRP to the deposition of commensurate SiGe/Si superlattices with ultathin SiGe alloy layers. SiGe alloy layers are attractive because they have a band gap which can be tailored by changing the Ge composition,[5] can be grown epitaxially on silicon,[6–8] and are fairly compatible with current silicon processing technology. Molecular-beam epitaxy has been used to fabricate SiGe/Si modulation-doped field-effect transistors[9,10] and infrared detectors.[11] Atmospheric pressure chemical vapor deposition (CVD) has been used to deposit SiGe/Si superlattices,[8] but alloy layers abrupt to better than 15 nm could not be grown because of smearing or mixing at interfaces. LRP superlattices exhibit superior layer thickness control with interfaces sharp to within a few monolayers.

The LRP systems used to grow the SiGe superlattices have been described previously.[1,12] The wafer is supported on three quartz pins in a chamber contructed from quartz and stainless steel. The radiant source is a bank of 6-kW tungsten-halogen lamps. Temperature calibration is performed using a W/26% Re vs W/5% Re thermocouple which is electron beam welded to the center of a test wafer. Epitaxial films are deposited on wafers without thermocouples by using a power versus time program to produce a desired temperature versus time cycle.

The substrates used were 2-, 3-, or 4-in.-diam (100) silicon wafers. Typically the wafers were given a wet chemical clean prior to insertion into the LRP chamber. Immediately before deposition, the wafers were baked in H_2 for 30–120 s at 1150–1200 °C to create a clean surface. The wafer was cooled, the desired reactant gases were introduced, and then the film deposition thermal cycle was initiated typically within 60 s of the H_2 cleaning step. Si and SiGe films were deposited at 900 °C using SiH_4 and GeH_4 diluted in H_2. Typical deposition pressures were 2–4 Torr using total flow rates from 1–3 lpm.

First, single layers of SiGe alloys were grown for material characterization and growth calibration. For example, a film grown for 60 s at 900 °C and a pressure of 4.2 Torr using 27 sccm SiH_4, 0.7 sccm GeH_4, and 3 lpm H_2 was analyzed using Rutherford backscattering (RBS) and sputtering Auger electron spectroscopy (AES). The film thickness and Ge fraction were 0.37 μm and 9%, respectively. The minimum yield, calculated by dividing the total Ge peak channeling yield by the total random yield, was 5.5%, indicating relatively good crystal quality.[13] RBS analysis of a number of samples was used to correlate the sputtering AES yield with Ge mole fraction in the thin SiGe alloy layers.

Commensurate SiGe strained-layer superlattices were grown *in situ* using multiple LRP cycles. The reactive gas composition was changed while the wafer was cool, in between high-temperature cycles. Growth interruption was typically less than 60 s. Figures 1 and 2 show AES and cross-section transmission electron microscopy (TEM) data for typical superlattices.[14] The alloy layers in sample 284 [Fig. 1(a) and 2(a)] contain 10% Ge, while the alloy layers in sample 334 [Fig. 1(b) and 2(b)] contain 17% Ge. Layers with higher Ge content are produced by simply increasing

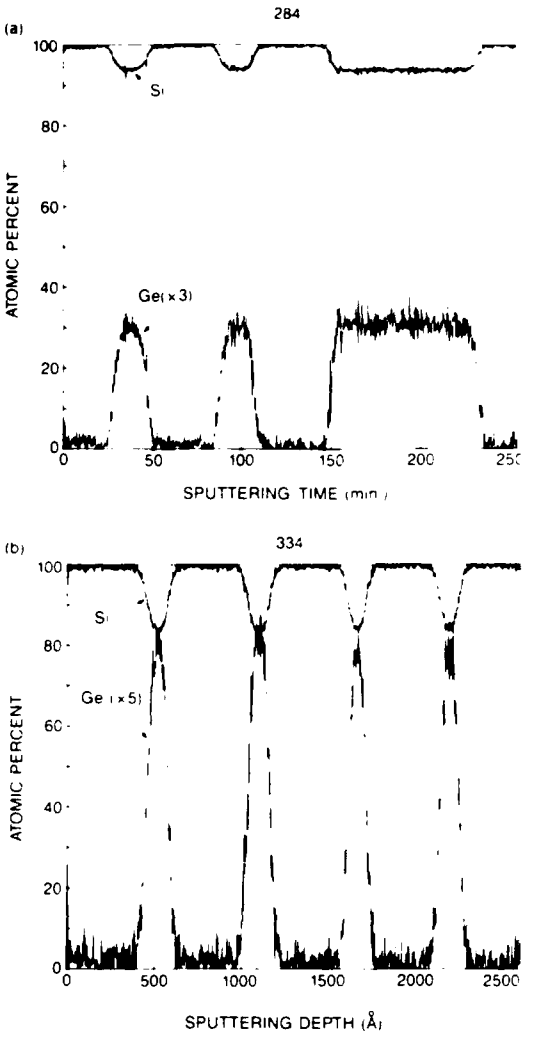


FIG 1. Sputtering Auger spectra for samples 284 and 334 showing nominal alloy layer Ge contents of 10% and 17%, respectively. Note that the Ge data were increased by a factor of 3 for sample 284 (a) and a factor of 5 for sample 334 (b). The sputtering rate was reduced to achieve a depth resolution of approximately 6 nm. The Auger yield was calibrated using RBS data from a number of thick, single alloy layers deposited on silicon (Charles Evans and Associates).

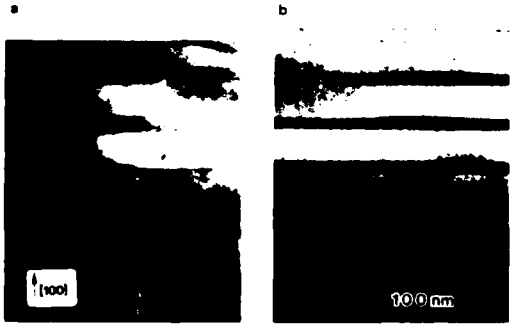


FIG 2. Cross-section TEM's of samples 284 (a) and 334 (b) showing commensurate growth. The SiGe layers appear darker in these micrographs. Plan view images show that the dislocation density is less than 10^6 cm^{-2} (Hewlett-Packard Labs).

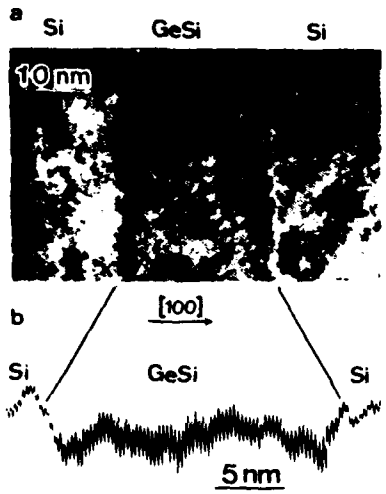


FIG. 3. (a) High-resolution transmission electron micrograph lattice image of part of a SiGe/Si multilayer structure, (011) projection. (b) Microddensitometer trace across the GeSi layer indicating that the SiGe/Si interfaces are abrupt to within approximately 20 Å.

the GeH_4/SiH_4 flow ratio during growth. The bright field TEM photographs distinguish the SiGe and Si layers as dark and light, respectively, and indicate that the growth is commensurate. Plan view images show that the dislocation density is less than 10^6 cm^{-2}. We are currently investigating the SiGe alloy layer thickness nonuniformity apparent in sample 334. Such nonuniformity appears to be indicative of island growth which becomes more favorable as the Ge mole fraction and the deposition temperature are increased.[14]

Figure 3 shows a highly magnified view of one of the $Si_{0.9}Ge_{0.1}$ layers in sample 284. Also shown is a densitometer trace which provides a quantification of the SiGe/Si interface abruptness. Although the interface resolution is limited by Fresnel diffraction effects, the transition width appears to be about five monolayers.

In summary, we demonstrate for the first time that LRP, a CVD-related technique, can produce ultrathin, high quality Si and SiGe epitaxial layers with abrupt interfaces. Compared to molecular-beam epitaxy, the higher growth temperatures used in LRP encourage three-dimensional growth for high Ge compositions, but we have demonstrated abrupt two-dimensional growth for dilute Ge compositions in the regime used for modulation-doped field effect transistors.

The authors appreciate the contributions of Dr. J. Brayman of the Stanford University Materials Science Department, Dr. Jim Sturm, Lockheed Corporation, the Hewlett-Packard Materials Characterization Labs, and D. A. Reynolds at Defense Advance Research Projects Agency (contract DAAG29-85-K-0237). C. Gronet acknowledges the support of an Office of Naval Research Fellowship.

[1] J. F. Gibbons, C. M. Gronet, and K. E. Williams, Appl. Phys. Lett. **47**, 721 (1985).
[2] C. M. Gronet, J. C. Sturm, K. E. Williams, and J. F. Gibbons, *MRS Symposium on Rapid Thermal Processing, Boston, MA, Dec. 1985* (Materials Research Society, Pittsburgh, PA, 1986), Vol. 52, p. 305.
[3] C. M. Gronet, J. C. Sturm, K. E. Williams, J. F. Gibbons, and S. D. Wilson, Appl. Phys. Lett. **48**, 1012 (1986).
[4] J. C. Sturm, C. M. Gronet, and J. F. Gibbons, IEEE Electron Device Lett. **EDL-7**, 282 (1986).
[5] J. C. Bean, in *Silicon Molecular Beam Epitaxy*, edited by J. C. Bean (The Electrochemical Society, Pennington, NJ, 1985), Vol. 85-7, p. 337.
[6] J. C. Bean, T. T. Sheng, L. C. Feldman, A. T. Fiory, and R. T. Lynch, Appl. Phys. Lett. **44**, 102 (1984).
[7] H. Jorke and H.-J. Herzog, in *Silicon Molecular Beam Epitaxy*, edited by J. C. Bean (The Electrochemical Society, Pennington, NJ, 1985), Vol. 85-7, p. 352.
[8] H. M. Manasevit, I. S. Gergis, and A. B. Jones, Appl. Phys. Lett. **41**, 464 (1982).
[9] T. P. Pearsall and John C. Bean, IEEE Electron Device Lett. **EDL-7**, 308 (1986).
[10] H. Daembkes, H.-J. Herzog, H. Jorke, H. Kibbel, and E. Kaspar, IEEE Trans. Electron Devices **ED-33**, 633 (1986).
[11] T. P. Pearsall, H. Temkin, J. C. Bean, and S. Luryi, IEEE Electron Device Lett. **EDL-7**, 330 (1986).
[12] C. M. Gronet, C. A. King, and J. F. Gibbons, *MRS Symposium on Materials Issues in Integrated Circuit Processing, Palo Alto, CA, April 1986* (Materials Research Society, Pittsburgh, PA), Vol. 71, p. 107.
[13] J. C. Bean, L. C. Feldman, A. T. Fiory, S. Nakahara, and I. K. Robinson, J. Vac. Sci. Technol. A **2**, 436 (1984).
[14] R. Hull, J. M. Gibson, and J. C. Bean, Appl. Phys. Lett. **46**, 179 (1985).

Paper #

Secondary ion mass spectrometry of hyper-abrupt doping transitions fabricated by limited reaction processing

J. E. Turner and Jun Amano
Hewlett Packard, 3500 Deer Creek Road, Palo Alto, California 94304

C. M. Gronet and J. F. Gibbons
Stanford University, Stanford, California 94305

(Received 9 February 1987; accepted for publication 6 April 1987)

Secondary ion mass spectrometry (SIMS) is used to quantify the abruptness of hyper-abrupt B-doping profiles in epitaxial silicon grown by limited reaction processing (LRP). By measuring the abruptness of dopant profiles as a function of SIMS primary beam energy and extrapolating to zero energy, doping roll-off decay lengths less than 20 Å are found for both the trailing and leading edges of LRP structures fabricated at 900 °C. Doping abruptness is limited by diffusional broadening during subsequent epitaxial growth. An asymmetry in leading and trailing edges of doping profiles is shown to be a SIMS sputter artifact, and the ratio of extracted decay lengths at these interfaces is predicted from elementary recoil events. A proportionality is found between sputter broadening of the doping profile and Monte Carlo calculations of dopant recoil depth.

Recently, advanced epitaxial silicon processes such as limited reaction processing[1-3] and molecular beam epitaxy[4,5] have shown a potential capability to grow semiconductor structures with unprecedented control of doping profiles. Next generation integrated circuits, including high-speed bipolar and submicron complementary metal-oxide semiconductor (CMOS), will require such control to grow doped structures with hyper-abrupt profiles.

While advanced epitaxy shows potential for the fabrication of very abrupt doping profiles, techniques for the characterization of these profiles are lacking. Spreading resistance is limited by the physical extent of the depletion layer, and is useful only in the measurement of decay lengths greater than about 100 Å. Similarly, techniques such as secondary ion mass spectrometry (SIMS) which rely upon sputtering by high-energy ions suffer a loss of interfacial information due to sample intermixing. The recoil processes induced by these primary ions also limit depth resolution to $\lambda = 100$ Å or more.

A number of researchers[6-14] have investigated the limits of SIMS depth resolution both experimentally and theoretically. Most of these focused on depth profiling of shallow implantation profiles, and perturbation of projected range and range straggling due to sputter recoil phenomena. In particular, Schulz *et al.*[12] showed that beam-induced broadening can be reduced by performing SIMS measurements at low energies, and that an extrapolation of range parameters to zero beam energy gives a good approximation to expected values. In these studies, however, it is very difficult to separate sputter-induced broadening from intrinsic range straggling of the shallow implants under study. For a better understanding of fundamental limitations of sputter techniques, more abrupt doping profiles are desirable.

This letter presents a SIMS study of transition widths on silicon epitaxial structures with extremely sharp doping profiles. By performing depth profiles at various energies, the sputter-induced artifacts of the SIMS measurement can be accounted for, and a true measure of interface width obtained.

Limited reaction processing uses radiant heating to provide rapid, precise changes in the temperature of the substrate to control surface reactions and epitaxial growth. Using this technique with a B_2H_6 source gas, square boron-doping profiles with nominal doping concentrations between 10^{15} and 10^{19} cm^{-3} were obtained at growth temperatures of 900 and 1000 °C in epitaxial silicon grown on Si(100) substrates. SIMS depth profiles were obtained on a custom-built quadrupole UHV instrument, using an Atomika duoplasmotron oxygen (O_2^+) ion source at a sputter angle 20° from the normal. To eliminate instrumental broadening due to effects other than recoil intermixing, secondary ions were collected only from the central portion of the sputter crater. In addition, the crater bottom topography was measured after SIMS profiling with a Dektak profilometer, and was found to be flat within the resolution of the instrument (20 Å).

Figure 1 shows representative B depth profiles obtained at various primary beam energies for the limited reaction processing (LRP) doping profile fabricated at 900 °C. The intended structure was a symmetrical p^+-doping pulse of 500 Å thickness at a doping level of 5×10^{18} cm^{-3}, with the leading interface located approximately 500 Å beneath the surface. Similar profiles were obtained for the doped LRP structure grown at 1000 °C. Doping decay lengths extracted from leading and trailing edges of the 900 and 1000 °C structures are plotted as a function of primary beam energy in Figs. 2(a) and 2(b), respectively, demonstrating that recoil intermixing decreases with decreasing energy for both interfaces.

The linearity of the doping decay length versus primary beam energy suggests that recoil intermixing effects might be eliminated by an extrapolation to zero energy. With this extrapolation, the leading and trailing interfaces of the LRP doping pulse grown at 900 °C as shown in Fig. 2(a), show an

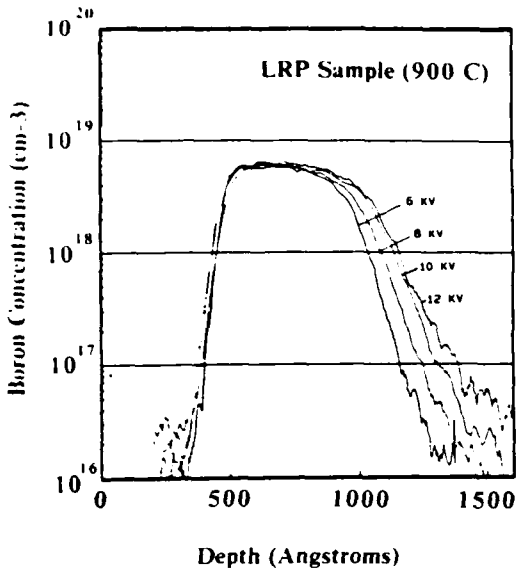


FIG 1. SIMS depth profiles of boron doping pulse in LRP structure, performed at various primary beam energies. LRP growth temperature 900 °C.

actual doping decay length on the order of $\lambda = 20$ Å, indicating an almost atomic abruptness. Doping decay lengths for the structure grown at 1000 °C, shown in Fig. 2(b), extrapolate to much broader sample interfaces of $\lambda = 69$ and 94 A for leading and trailing edges, respectively. It is significant that the trailing edge, exposed to the elevated temperatures for a longer period, has a less abrupt doping interface.

Assuming a random walk diffusion of B in Si during LRP growth, given the diffusion coefficient for B in Si[15] at 900 °C ($D = 2\times10^{-15}$ cm^2/s) and 1000 °C ($D = 2\times10^{-14}$ cm^2/s), and the length of time these interfaces are exposed to epitaxial growth temperatures (30 and 60 s, respectively), one can calculate an expected diffusion length for leading and trailing interfaces. Table I shows a comparison of calculated diffusion lengths with measured interface decay

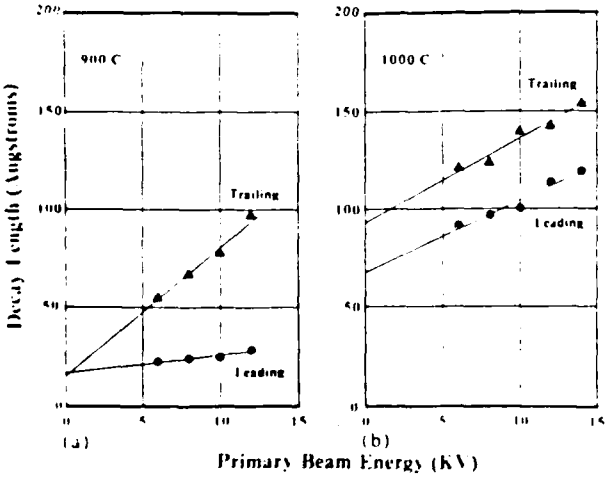


FIG 2. Doping decay lengths for leading and trailing edges extracted from SIMS depth profiles as a function of O$_2^+$ primary beam energy for LRP structures grown at (a) 900 °C and (b) 1000 °C.

TABLE I. LRP doping interface abruptness

	900 °C		1000 °C	
	Leading edge	Trailing edge	Leading edge	Trailing edge
Measured decay length (λ)	20 A	20 A	69 A	94 A
Calculated diffusion length $(Dt)^{1/2}$	25 A	35 A	80 A	110 A

lengths as determined by the energy-dependent SIMS measurements described above. The close correspondence strongly suggests that the doping abruptness of these structures is limited by diffusional broadening during subsequent epitaxial growth.

Now let us discuss the simple linear extrapolation of the decay length versus primary beam energy. The sputter energy dependence of interfacial mixing is known to be a function of the energy range under study, the sputtering and recoil atoms, and other factors.[7,8] In the most elementary model considering only primary recoil events, the energy of the recoil atoms will be proportional to the primary beam energy. Primary collisions between oxygen atoms and dopant atoms will transfer the greatest amount of energy. These high-energy recoil atoms will be implanted furthest beyond the interface and thus should define the extent of sputter broadening of the interface. Calculations based on the Boltzmann transport equation[16] suggest that recoil decay lengths should be proportional to recoil energy. The linear dependence of interface width on primary beam energy observed experimentally in this and other systems[12-14] may thus be justified. A linear extrapolation of decay length for the data shown in Fig. 2 to zero energy will then yield the true sample interface width with an absence of sputter-induced artifacts.

The sputter-induced asymmetry in the SIMS profiles of Fig. 1 can be understood in terms of the elementary recoil sputter processes at each interface. Broadening occurs at the trailing interface via a primary sputter event in which an incident oxygen specie impacts a single boron dopant atom. The efficient energy transfer in such a collision results in a relatively high projected range for the boron atom. In contrast, broadening of the leading edge will occur primarily by the two-atom recoil process in which an incident oxygen ion sputters a silicon atom which in turn causes recoil of a boron atom. The lower energy transfer gives a shallower projected range and a sharper leading interface. This is qualitatively observed in the SIMS profiles of Fig. 1, and would also be expected as a general result in depth profiling of hyperabrupt interfaces.

In fact, one can obtain a quantitative estimate of the relative broadening of front and back interfaces from these elementary sputter events by comparing the average energy imparted to boron atoms in the recoil events at each interface. Using a simple hard-sphere model, a 10-kV oxygen primary beam will impart an average energy of 0.95 kV to a boron recoil atom in the two atom sputter process at the

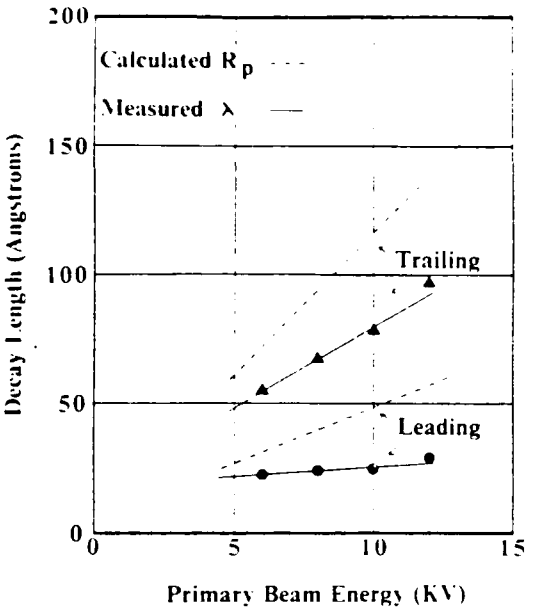


FIG. 3. Monte Carlo calculations of projected range for recoil implantation of boron atoms from hard-sphere collisions with O_2^+ sputtering species at various energies. A linear relationship is found between these implantation depths and experimentally determined decay lengths from SIMS depth profiles on LRP structure fabricated at 900 °C

leading interface. At the trailing interface, boron recoil atoms in the primary sputter event receive an average energy of 2.4 kV. Since a linear relationship has been predicted between recoil energy and decay length,[16] we expect a decay length ratio of 2.4/0.95 = 2.53. Experimentally, the actual decay length ratio at back and front interfaces for the more abrupt 900 °C growth structure at 10 kV was 3.19.

We also note an empirical correspondence between the measured recoil decay length (λ) and the projected range (R_p) for boron atoms with energies given by the hard-sphere calculations above. For each incident primary beam energy, the average energy for boron recoil species was determined at both the front and back interfaces. Monte Carlo TRIM simulations of the implantation process were then performed to calculate R_p for recoil boron atoms in each case. Figure 3 shows the correspondence between calculated R_p and decay lengths (λ) measured for the 900 °C LRP structure. For both leading and trailing edges it appears that there is a linear relationship between implantation depth and decay length approximated by $\lambda \simeq 0.70\, R_p(E_{rec})$, where E_{rec} represents the average energy imparted to the boron recoil atom.

The interface mixing model presented here is tremendously simplified, and does not consider cascade mixing, which is believed to be the dominant recoil process in this energy range.[11] However, the prediction of qualitative features of interface broadening in this context shows that some insight into the limits of SIMS depth resolution can be found by considering only elementary sputter events.

In summary, we have shown that advanced epitaxial techniques such as limited reaction processing (LRP) are capable of extremely abrupt doping profiles. Broader interfaces were obtained at higher growth temperatures, and quantitative agreement between extracted decay lengths and calculated diffusion lengths indicates that interface abruptness is limited by dopant diffusion during subsequent epitaxial growth. Primary features of interface broadening during SIMS depth profiling can be understood by considering the energy transfer to dopant atoms at abrupt interfaces in elementary recoil events. The limitations imposed on the measurement of very abrupt interfaces by recoil intermixing due to the SIMS sputter process can be greatly reduced by energy-dependent measurements.

[1] J. F. Gibbons, C. M. Gronet, and K. E. Williams, Appl. Phys. Lett. **47**, 721 (1985).
[2] J. C. Sturm, C. M. Gronet, and J. F. Gibbons, J. Appl. Phys. **59**, 4180 (1986).
[3] C. M. Gronet, J. C. Sturm, K. E. Williams, and J. F. Gibbons, Appl. Phys. Lett. **48**, 1012 (1986).
[4] *Proceedings of the First International Symposium on Silicon Molecular Beam Epitaxy*, edited by J. C. Bean (Electrochemical Society, Pennington, NJ, 1985).
[5] F. G. Allen, Thin Solid Films **123**, 237 (1985).
[6] K. Wittmaack, Vacuum **34**, 119 (1984).
[7] P. Williams, Appl. Phys. Lett. **36**, 758 (1980).
[8] P. Sigmund, Phys. Rev. **184**, 383 (1969).
[9] M. D. Giles, J. L. Hoyt, and J. F. Gibbons, Mater. Res. Soc. Symp. Proc. **69**, 323 (1986).
[10] J. Remmerie and H. E. Maes, Spectrochim. Acta Part B **40**, 787 (1985).
[11] H. H. Andersen, Appl. Phys. **18**, 131 (1979).
[12] F. Schulz, K. Wittmaack, and J. Maul, Radiat. Eff. **18**, 211 (1973).
[13] W. Vandervorst, H. E. Maes, and R. F. De Keersmaecker, J. Appl. Phys. **56**, 1425 (1984).
[14] F. R. Shepherd, W. H. Robinson, J. D. Brown, and B. F. Phillips, J. Vac. Sci. Technol. A **1**, 991 (1983).
[15] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981), p. 68.
[16] L. A. Christel, J. F. Gibbons, and S. Mylroie, Nucl. Instrum. Methods **182**, 187 (1981).

Paper # 9

Electrical Characterization of *In-situ* Epitaxially Grown Si p-n Junctions Fabricated using Limited Reaction Processing

C. A. King, Student Member, IEEE, C. M. Gronet, Student Member, IEEE, and
J. F. Gibbons, Fellow, IEEE
Stanford Electronics Laboratories, Stanford, CA 94305

S. D. Wilson
Charles Evans & Associates, Redwood City, CA 94063

Abstract

Electrical properties of *in-situ* grown p-n junctions formed by Limited Reaction Processing are investigated. Forward current ideality factors of $1.01 \pm 0.3\%$ were obtained over a large current range extending down to 1 pA. Reverse current densities measured 3.5 ± 1.2 nA/cm^2 at a reverse bias of -5 volts. Breakdown occurred at the expected value of -22 V and displayed a very sharp current rise of 30 decades/volt. Extremely uniform light emission from the junction was observed under a microscope at breakdown: this phenomenon is a visual indication that the material is of high quality and suitable for high performance minority carrrier devices.

Introduction

The growth of thin semiconductor layers with rapidly varying material composition and doping concentration has recently been the basis for many technological developments [1-4]. The ability to produce abrupt changes in the doping profile has several advantages. First, it allows device design to incorporate fine structure with thin doped layers. Such layers are vital for certain device applications such as modulation doped structures and bipolar junction transistors. A second advantage of abrupt junctions is the absence of compensation which degrades drift mobility and thus increases bulk resistance. This resistance may be especially important, for example, in the thin base of a bipolar transistor. Finally, it is desirable to have

an extremely abrupt emitter-base junction. It improves the injection efficiency since minority carrier charge storage in the emitter is suppressed.

In the past Limited Reaction Processing (LRP) has been used to demonstrate the growth of thin, abrupt layers [3.4.3.5], and p-n junction diodes formed by implantation have been studied [3.6]. In this paper, the properties of *in-situ* grown p-n junctions are to be examined and compared with implanted devices.

LRP was used to grow epitaxial silicon p-n junctions. They were grown without removing the wafer from the growth chamber. These junctions were formed by growing two consecutive layers on an n+ substrate, the first layer being doped n-type and the second layer p-type. The ability to carry out this procedure *in-situ* ensures clean interfaces since they are never exposed during subsequent processing. The risk of contaminating sensitive junctions is thereby reduced. This reduced risk will increase reproducibility and reliability as well as performance. *In-situ* grown interfaces will improve such characteristics as reverse leakage current and reverse breakdown.

Grown junction devices displayed excellent forward bias characteristics with ideality factors of $1.01 \pm 0.3\%$ over seven decades of current. Reverse leakage current densities measured 3.5 ± 1.2 nA/cm^2 at a reverse bias of 5 volts implying that the material is of high quality. Extremely abrupt reverse breakdowns were seen at the voltage expected for a step junction with the measured impurity density in the lightly doped side. Uniform light emission across the junction was also observed at breakdown which visually indicates that the density of electrically active defects and metallic impurities is very small.

Fabrication

Layer growth of the devices discussed in this paper was carried out in a reaction chamber which provides radiant heat to a single wafer and uses wafer temperature, not process gas flow, as a switch to initiate and terminate epitaxial growth. The apparatus has been described elsewhere [3.1]. The p-n junctions fabricated in this experiment were isolated using a mesa structure, but three different methods of forming the junctions were utilized. The first method, type A, is a grown junction where both n and p type layers were grown epitaxially *in-situ* on an n+ substrate. Type B junctions were formed by growing a lightly doped n layer on an n+ substrate, but implanting with boron and BF_2 to form the top p layer.

Table 1
Summary of device structures used in this investigation.

Sample Type	n layer	p layer
A	2μm LRP epi 4×10^{16} cm^{-3} Arsenic	0.5μm LRP epi 7×10^{17} cm^{-3} Boron
B	2μm LRP epi 3×10^{16} cm^{-3} Arsenic	Boron and BF_2 Implant
C	5-8 Ω· cm (100) CZ wafer	Boron and BF_2 Implant

Type C diodes were made by directly implanting boron and BF_2 into a 5-8 Ω· cm (100) n-type wafer. Three successive implants, 5×10^{12} cm^{-2} at 45 KeV with BF_2, 8×10^{12} cm^{-2} at 45 KeV with boron, and 1×10^{13} cm^{-2} at 100 KeV with boron were used to achieve a relatively flat profile of the same doping density as the grown junction devices. Table 1 summarizes the structure of the three types of devices. Doping densities and layer thicknesses were measured using spreading resistance profiling (SRP) and secondary ion mass spectroscopy (SIMS).

The substrates used for the type A and type B devices were (100) oriented and doped with Sb to a level 2×10^{18} cm^{-3}. These wafers were given an RCA clean and HF dip immediately prior to loading into the growth chamber. After a 30 second H_2 pre-clean at 1200°C and 250 torr , a 2 μm n-type layer doped to a level of 4×10^{16} cm^{-3} was grown using $SiCl_2H_2$ as the Si source and AsH_3 as the dopant source. Total chamber growth pressure was 6 torr with 0.8% $SiCl_2H_2$ in H_2 present. The n-type layer was grown thick enough to guarantee that the depletion region at breakdown would be fully contained within the epitaxial layer. The growth rate of this layer was 0.25 μm/minute at a growth temperature of about 1000°C. For type A devices, a second layer growth was executed. Upon completion of growth of the first layer, the AsH_3 was switched off and a flow of B_2H_6 sufficient to obtain a p-type doping density of approximately 7×10^{17} cm^{-3} was established. Three minutes after termination of the n-type layer epitaxy, a 0.5 μm p-type layer growth commenced at 900°C and 1000°C using the same conditions as stated above. The

doping densities of these layers are suitable for the base-collector junction of a bipolar transistor.

Once the epitaxial growth was complete, the wafers were given an RCA clean and loaded into a standard LPCVD furnace for deposition of 900 Å of Si_3N_4 at 780°C. Since the mask contained a variety of rectangular patterns, the wafers were patterned such that the mesa sidewalls of all the devices would be oriented in a [100]-type direction so as to minimize the effects of the perimeter leakage on device characteristics [3.7]. The nitride was patterned using an SF_6 and CF_3Br plasma. The nitride layer then served as a mask for the mesa etching of the underlying epi layers. A 4M solution of KOH at 60°C was used to etch the silicon. The wafers were cleaned once again and thermally oxidized at 900°C for 25 minutes and annealed in argon for 15 minutes at 900°C to passivate the mesa sidewalls and activate the implanted dopant in the control wafers. The nitride was then stripped and 2000 Å of Ti and 1 μm of Al-1% Si was sputtered to form an ohmic contact to the p layer. After patterning the metal, the samples were annealed at 400°C for 10 minutes in forming gas.

Results

The forward characteristics of three type A grown junction devices with different areas are shown in Figure 1. An HP-4145 Semiconductor Parameter Analyzer was used for all DC measurements. The slopes of the forward curves have ideality factors of $1.01 \pm 0.3\%$ and the saturation current of each device varies precisely with area. This dependence on area suggests that the sidewalls play an insignificant role in device operation. The forward current characteristic remains ideal from very low currents to levels where bulk and contact resistances dominate. This range of ideal behavior spans nearly eight orders of magnitude, and is an indication that space charge recombination currents are negligible. On the other hand, ideality factors for type B devices were $1.02 \pm 0.4\%$ and type C diodes exhibited factors of $1.05 \pm 1.3\%$. These higher ideality factors are probably a product of the annealing process used here. The temperature and time of the anneal was chosen in order to minimize interdiffusion in the grown junction and yet still passivate the sidewalls. For the thermal cycling given here, these results suggest that the clean interface provided by the grown junction is superior to that obtained by implantation.

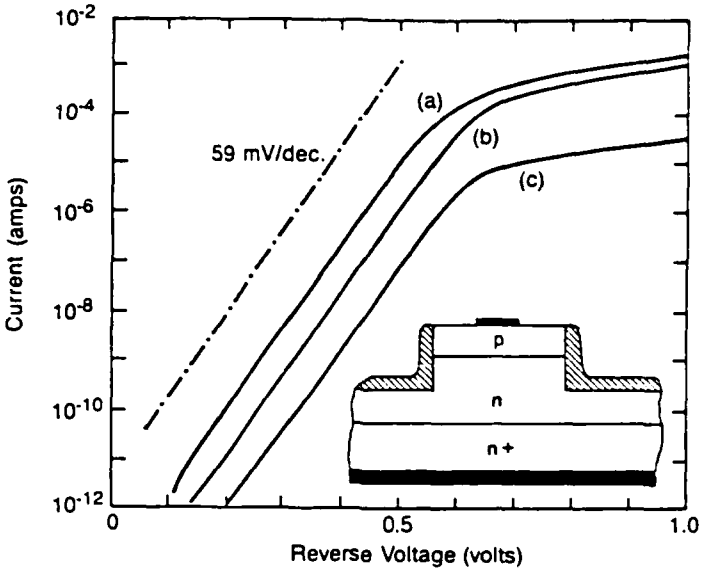


Figure 1. Forward characteristics of three grown junction diodes. Diode areas are (a) 4.0×10^{-3} cm^2 (b) 4.0×10^{-4} cm^2, and (c) 2.5×10^{-5} cm^2. The device structure is shown in the inset.

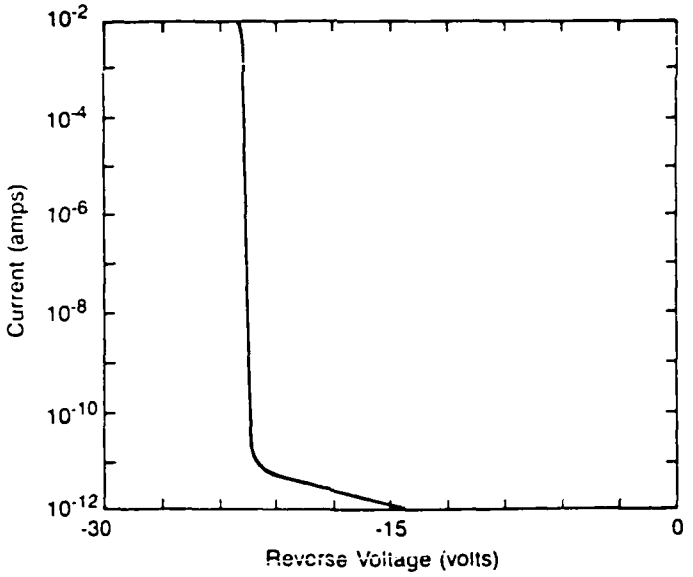


Figure 2. Reverse characteristic of a square diode with current plotted on a log scale. The area of the diode is 1.0×10^{-4} cm^2, and the breakdown voltage is the expected -22.3 volts.

The reverse current characteristic of a grown junction device is illustrated in Figure 2. Small leakage currents below the sensitivity of the HP-4145 exist at low

reverse bias, and at breakdown the device achieves a sharp transition to avalanche mode operation. Reverse current densities of 3.5 ± 1.2 nA/cm^2 were obtained at a reverse bias of -5 V for these devices after measuring several diodes of different area on the same die. Device area varied from 1.6×10^{-5} cm^2 to 4×10^{-3} cm^2. These current densities compare favorably with other recent data presented for diffused diodes [3.8,3.9]. In the same manner, reverse current densities for type B devices measured 4.4 ± 0.1 nA/cm^2 while those of type C diodes were 5.2 ± 0.7 nA/cm^2 at -5 V reverse bias. Type A devices with a p layer grown at 900°C were identical to those grown at 1000°C.

Breakdown in type A devices occurred at the expected value of approximately -22 V for a doping density of 4×10^{16} cm^{-3} in the n-type side [3.7]. The sharpness of the current rise at breakdown, like the ideality factor in the forward bias region, is an indication of junction quality. In the breakdown region, the type A grown junction devices exhibit current rises of 26 to 30 decades/volt before series resistance effects become important. This value agrees well with silicon devices in the literature which showed excellent breakdown characteristics [3.10,3.11]. Type B devices, however, displayed current rises of 11 to 15 decades/volt. Visual evidence of exceptional breakdown behavior in the type A grown junctions was observed through a microscope by biasing a device at a current density on the order of 10 A/cm^2. This bias is sufficient to cause the silicon to heat up and glow in regions where breakdown is occurring. Extremely uniform light generation across the device was noted as can be seen in the photograph of Figure 3. Defects or metallic impurities within the epitaxial layer will produce relatively sparsely distributed 'hot spots' around the junction. These 'hot spots' are definitely not evident in the photograph of Figure 3. Since the light intensity emerging from the device is so weak, a very long exposure time of 8 hours was required for the photograph, and the true nature of the light uniformity is not captured. Even so, a uniform density of breakdown regions is clearly apparent and indicative of a high quality junction.

Conclusion

Mesa p-n junction diodes grown *in-situ* using Limited Reaction Processing were fabricated and examined. Ideality factors of $1.01 \pm 0.3\%$ were obtained for the grown junction devices while control devices utilizing a boron implant to form the junction had inferior factors of $1.02 \pm 0.4\%$ and $1.05 \pm 1.3\%$. Similarly, reverse

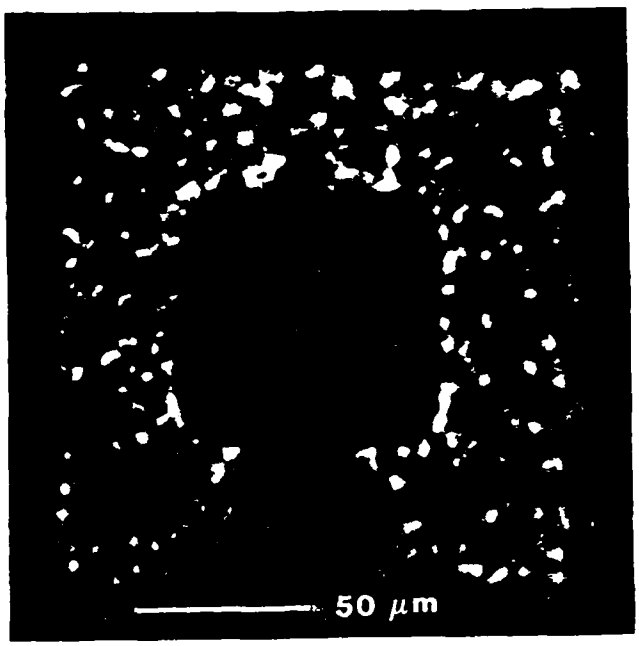


Figure 3. Photograph of a reverse bias diode with area 2.25×10^{-4} cm^2. The dark area in the center is the metal contact.

leakage currents for grown junction diodes at -5 V bias were 3.5 ± 1.2 nA/cm^2 while the controls showed current densities of 4.4 ± 0.1 nA/cm^2 and 5.2 ± 0.7 nA/cm^2. Breakdowns were sharp for the grown junction at the expected reverse voltage of -22 V. Grown junction devices exibited a 30 decade/volt current swing once breakdown occurred. Uniform light emission from the devices provided visual confirmation of the excellent breakdown performance. From these experiments, it is apparent that excellent minority carrier devices can be fabricated from grown junctions formed by LRP.

Acknowledgement

The authors wish to thank D. A. Reynolds of DARPA for his continued interest and support. The authors are also grateful for the assistance of J. L. Hoyt and the staff of the Center for Integrated Systems, especially S. Taylor and R. King.

References

[1] J. F. Gibbons, C. M. Gronet, and K. E. Williams, *Appl. Phys. Lett.*, vol. 47, p. 721, 1985.

[2] J. C. Bean and E. A. Sadowski, *J. Vac. Sci. Technol.*, vol. 20, p. 137, 1982.

[3] B. S. Myerson, *Appl. Phys. Lett.*, vol. 48, no. 12, p. 797, 1986.

[4] C. M. Gronet, J. C. Sturm, K. E. Williams, and J. F. Gibbons, *Appl. Phys. Lett.*, vol. 48, no. 15, p. 1012, 1986.

[5] C. M. Gronet, C. A. King, W. Opyd, J. F. Gibbons, S. D. Wilson, and R. Hull, *J. Appl. Phys.*, vol. 61, no. 6, p. 2407, 1987.

[6] J. C. Sturm, C. M. Gronet, and J. F. Gibbons, *J. Appl. Phys.*, vol. 59, no. 12, p. 4180, 1986.

[7] S. M. Sze, *Physics of Semiconductor Devices*, John Wiley and Sons, New York, 1981.

[8] T. N. Nguyen, D. L. Harame, J. M. C. Stork, F. K. LeGoues, and B. S. Myerson, *Technical Digest*, 1986 IEEE IEDM, p. 305.

[9] Kyeong-Tae Kim and Choong-Ki Kim, *Elec. Dev. Lett.*, vol. EDL-8, no. 12, p. 569, 1987.

[10] William Shockley, *Solid State Electronics*, vol. 2, no. 1, p. 35, 1961.

[11] B. Senitzy and J. L. Moll, *Phys. Rev.*, vol. 110, no. 3, p. 612, 1958.

Paper # 10

THE DEPTH RESOLUTION OF DYNAMIC SIMS: EXPERIMENTS AND CALCULATIONS

M.D. Giles*, J.L. Hoyt, and J.F. Gibbons
Stanford Electronics Laboratories, Stanford, CA 94305
* AT & T Bell Laboratories, Murray Hill, NJ 07974

ABSTRACT

This study is concerned with the fundamental limitations imposed by cascade mixing and recoil implantation on the depth resolution of secondary ion mass spectrometry (SIMS), and the effects of these limitations on the determination of impurity profiles in semiconductors.

We present experimental results of measurements on atomically, or near atomically abrupt impurity profiles in Si using magnetic sector (Cameca) and quadrupole (Atomica) SIMS machines. The analysis conditions and samples have been chosen to minimize instrument (crater wall resputtering) and surface (equilibration time) effects. Under such conditions the leading edge of an abrupt signal is smeared to a complimentary error function, while the trailing edge exhibits an exponential decay reminiscent of recoil implantation profiles.

Modifications of the Boltzmann Transport Equation (BTE) approach to ion implantation in multilayer targets will be shown to provide a first principles calculation of such SIMS knock-on phenomena, which is in good agreement with the empirical results.

INTRODUCTION

Modern semiconductor device process monitoring places high demands on materials characterization techniques in terms of both depth resolution and dynamic range. Because of its high sensitivity, secondary ion mass spectrometry (SIMS) is often the technique of choice for chemical depth profiling of dopants in semiconductors. Trends in device processing require the analysis of shallower, more abrupt impurity profiles, which have already exceeded the depth resolution of conventional SIMS. Hence, it is of interest to better understand and characterize the depth resolution, in order to minimize the undesirable effects, with the eventual hope of deconvolving the system resolution from SIMS data.

Like all techniques which employ sputtering, SIMS analysis is subject to ion beam mixing effects. An excellent review of beam-induced broadening effects in sputter depth profiling is given by Wittmack in [1], who notes that 'dilute systems' (i.e. impurities in semiconductors) are desirable for studying atomic mixing processes as they avoid the complications associated with large composition changes at interfaces. Schulz et al. [2], and Shepherd and co-workers[3] have studied the shape of low energy B and As implants in Si as obtained by SIMS with Ar^+ and O_2^+ bombardment. For Ar^+ primary ions, an explicit exponential tail is evident on B profiles, with a decay length λ_B proportional to the Ar^+ energy.

Vandervorst, et al. [4] have made detailed studies on very low energy As implants into pre-amorphized Si and SiO_2 using Ar^+ and O_2^+ ions. For O_2^+ bombardment, these authors find a linear dependence of λ_{As} on E_0 for $E_0 \leq 2$ KeV per atom. Above this energy, they find $\lambda_{As} \approx E_0^{.32}$. Under Ar^+ bombardment, it appears that $\lambda_{As} \approx E_0^{.53}$, which they note is close to the square root energy dependence predicted by calculations of collisional mixing [5].

The theory of sputtering has been treated by Sigmund [6], and collisional mixing is described by Sigmund and Gras-Marti [7,8]. Simple cascade mixing calculations of Anderson [5] predict a symmetrical smearing out of sputter profiles, characterized by a standard deviation σ which depends upon the primary ion energy, mass, and the substrate mass. Monte Carlo calculations [9], and full-blown transport theoretical treatments [10,11] predict assymetrical distortion of sputter profiles, and exponential tails.

This work is not concerned with instrument or special sample effects. We present experimental examples of beam mixing effects on impurity profiles of As, B, and Sb in Si under 'typical' SIMS profiling conditions. The original motivation for this work was to investigate the effects of limitations in SIMS depth resolution on the measured shape of doping profiles produced by high concentration As^+ implantation into Si, followed

by rapid thermal annealing (RTA). During the short time, high temperature annealing cycle, the concentration dependence of the As diffusivity produces a box-shaped depth profile with an abrupt junction. The SIMS profiles of these RTA samples are compared to those of samples prepared by molecular beam deposition (MBD), which is known to produce impurity transition regions on a monolayer scale.

In addition, the Boltzmann transport equation calculations [12] used for ion implantation simulation have been enhanced to model recoil implantation effects for the SIMS case, and results of these calculations will be described.

EXPERIMENTS

Several types of samples were used in this study. Boron doped, 5 to 10 $\Omega-cm$,⟨100⟩ Si wafers were implanted at room temperature with 80 KeV As^+ to a dose of $8 \times 10^{15}\ cm^{-2}$. Samples were then rapid thermal annealed for 10 to 15 seconds at temperatures ranging from 1050 to 1200 °C to regrow the amorphous layer and diffuse the As. For the reference samples, the molecular beam deposition of doped and undoped Si was performed at room temperature, resulting in an amorphous layer. Some of the samples were then annealed at 700 °C for 30 minutes, producing polycrystalline Si. SIMS analysis showed no difference between the depth profiles of as-deposited and annealed MBD layers. A third set of samples was produced by limited reaction processing (LRP), a chemical vapor technique which uses tungsten lamps for rapid substrate heating [13], thereby minimizing dopant diffusion. Epitaxial Si layers with a constant B concentration were grown on lightly-doped p-type substrates. Thin, alternating layers of p^+ and undoped layers were also grown by this technique. These samples provide a good test of SIMS depth resolution and dynamic range, as B can be incorporated into the Si at concentrations much higher than obtained in MBE (up to $1 \times 10^{21}\ cm^{-3}$).

All of the samples in this study were analyzed on a Cameca IMS-3f using 15 KeV Cs^+ primary ions, and negative secondaries. Typical primary beam currents were in the range of .8 to 6 μA rastered over a $500 \times 500\ \mu m^2$ area, resulting in sputtering rates of 5 to 30 Å/second. Standard techniques (e.g. a field aperture for crater edge rejection) are used to minimize instrumental effects on the depth resolution without undue sacrifice in sensitivity and dynamic range. On this machine, the angle of the primary column with respect to the sample normal is nominally 35°, but for Cs^+ bombardment with negative secondary ions, the secondary extraction optics bend the primary beam as it approaches the sample, so that in practice the beam angle is closer to normal incidence.

The B doped samples were also profiled with a 5 KeV O_2^+ beam on the Cameca ion microscope using positive secondary ions. In this case, the primary beam bends away from the sample normal, resulting in an incidence angle of about 45°. Typical sputtering rates were 5 to 10 Å/second.

A quadrupole mass analyzing machine (Atomica) was used to profile the As samples at a lower energy, employing 6 KeV O_2^+, at a current of .1 μA scanned over a $400 \times 400\ \mu m^2$ area. The resulting sputter rate was .5 Å/second. The beam strikes the sample at two degrees from the normal. The molecular interference signal due to $^{29}Si^{30}Si^{16}O$ limits the ultimate SIMS sensitivity in the case of ^{75}As in both the Cameca and Atomica machines, and is suppressed by offsetting the sample voltage during As anaysis.

In all cases, sputtering rates were determined from crater depths measured on a Dektak stylus meter. To reduce uncertainties associated with SIMS quantitation errors, we have normalized all the As SIMS data to the dóse as measured by Rutherford backscattering (RBS), which should be accurate to within 15 %.

Figure 1 depicts the SIMS response to the leading edge of an atomically abrupt doping transition for 15 KeV Cs^+ bombardment. The sample in figure 1(A) is a 3300 Å molecular beam deposited Si layer. During the deposition of the first 2300 Å , the B shutter was open, resulting in a layer with $\approx 7 \times 10^{19}\ cm^{-3}$ doping concentration. The B shutter was closed for the last 1000 Å of deposition, producing an abrupt transition at a depth of 1000 Å. Figure 1(B) shows a SIMS profile for an undoped, 5200 Å MBE layer on an Sb-doped Si substrate.

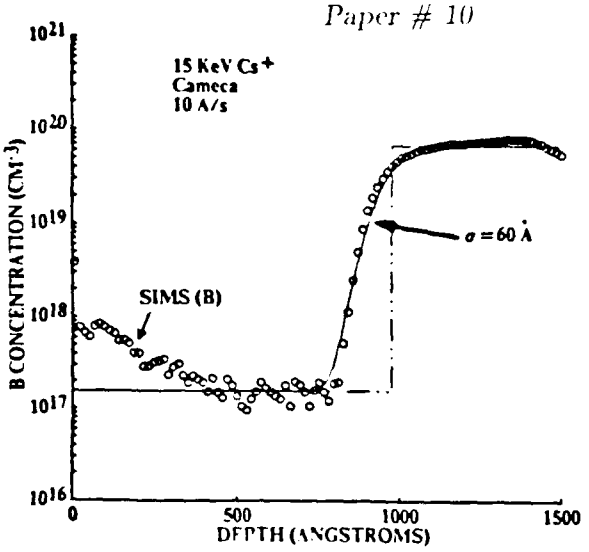


Figure 1A: SIMS response to the leading edge of an abrupt B doping transition. The solid line is the convolution of a step function with a gaussian with half width equal to 60 angstroms.

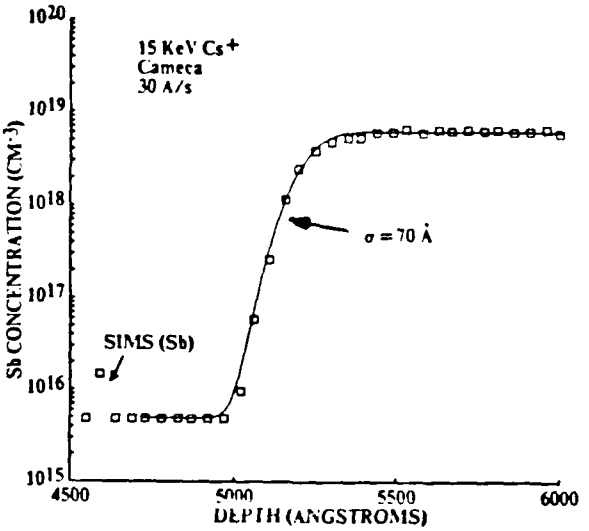


Figure 1B: SIMS profile of the interface between an undoped MBE layer and an Sb-doped Si substrate.

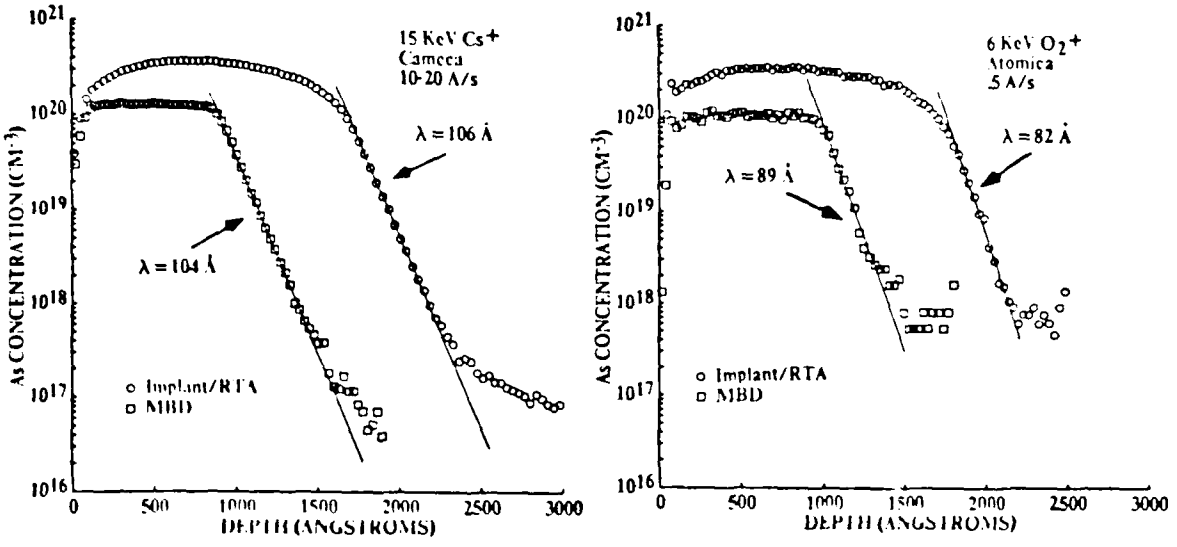
Both profiles can be fit to error funcions (shown by the solid lines) with convolving gaussians of standard deviation $\sigma \approx 60$ Å, corresponding to the symmetrical (e.g. cascade mixing) component of the sputtering distortion. For these SIMS conditions, the depth resolution measured on a leading edge is roughly the same for B and Sb in Si, and is independent of the sputtered depth, in the range of 1000 to 6000 Å.

Figure 2 compares As depth profiles of a molecular beam deposited As doped layer with an ion implanted and rapid thermally annealed sample. The data in figure 2(A) was obtained with 15 KeV Cs^+ bombardment. Both profiles exhibit exponential tails over 2.5 to 3 decades, with decay lengths λ_A, of 105 Å. Clearly, the shape of the RTA As profile beyond 1700 Å is obscured by the beam-induced distortion during the SIMS analysis. For comparison, figure 2(B) shows SIMS profiles of the same samples obtained with 6 KeV O_2^+ primary ions on the Atomica machine. Although the background is higher by almost an order of magnitude in this case, the exponential tails fall off slightly faster, with decay lengths of 89 and 82 Å. This is consistent with the fact that the calculated range [14] of 3 KeV O^+ is 90 Å, while that of 15 KeV Cs^+ is 158 Å. It is also consistent with Vandervorst's [4] value of $\approx$ 105 Å for λ_A, in SiO_2 under 6 KeV O_2^+ bombardment, since he observed that the decay lengths in oxide were slightly higher than those in Si.

The gain in depth resolution obtained for B in Si on the Cameca machine as a result of switching from 15 KeV Cs^+ to 5 KeV O_2^+ primary ions is evident from figure 3. This sample was grown by LRP. Although the Cs^+ SIMS profile has slightly better dynamic range, the shape of the B pulses is almost completely obscured by the beam mixing effects. The trailing exponential decay lenghs on the pulse centered at a depth of 2000 Å are 134 and 65 Å under Cs^+ and O_2^+ bombardment respectively. Note that for Cs^+ bombardment, the broadening is much more assymetrical than for the case of O_2^+ primaries.

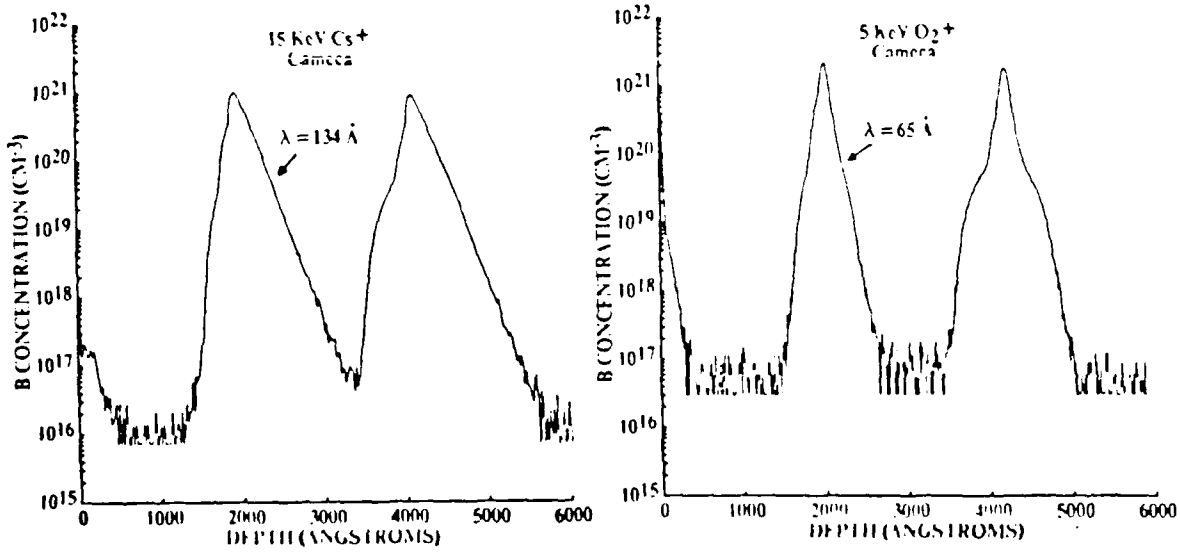
BOLTZMANN TRANSPORT CALCULATIONS

The BTE method has been successfully applied to the calculation of primary ion and recoil range distributions in a variety of ion implantation problems [12,15]. A pertinant example is the calculation of the profile and yield for oxygen atoms recoil implanted into



A: Cesium sputtering (Cameca). B: Oxygen sputtering (Atomica).

Figure 2: SIMS profiles for an atomically abrupt junction produced by molecular beam deposition, and an As implanted/RTA sample.



A: Cesium sputtering. B: Oxygen sputtering.

Figure 3: Comparison of boron profiles in Si grown by LRP, obtained in the Cameca machine with two different primary beams. The superior depth resolution obtained with O primaries reveals some outdiffusion in the deeper peak during the growth of the overlying layers.

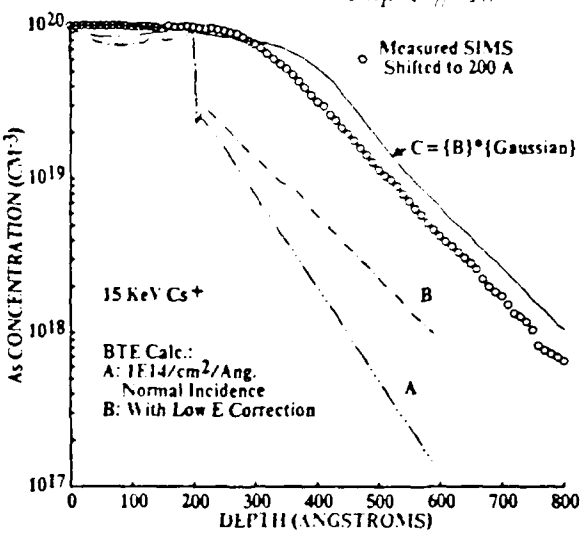


Figure 4: Comparison of calculated profiles with measured SIMS data for sputtering through a 200 Å MBE layer doped with As to $1 \times 10^{20}\ cm^{-3}$. The actual layer thickness is 1000 Å, but the data is shown shifted to 200 Å for comparison to the calculated profile. The solid line (C) is the result of convolving the BTE calculated recoil profile (B) with a mixing gaussian of half width equal to 60 Å.

the underlying substrate during an implant (of As, for instance) into a thin layer of SiO_2 on Si [16]. Since the details of such calculations have been described elsewhere, only a brief description is given here.

In this method, the evolution of the ion momentum distribution $F(E, \theta, z)$ is given by the Boltzmann transport equation in terms of the differential scattering cross sections. In practice, a computer program keeps track of how the distribution changes for each ion type (primary and recoils) as a function of depth, given the initial condition in which all the primary ions are at the surface, moving with the energy E_0.

The calculations may be extended to the sputtering case by explicitly including the sputtering process as follows. Suppose that a total dose ϕ of primary ions is required to sputter a sample to a depth t. Conceptually, this situation may be considered as a series of n low energy implants, each of dose $\frac{\phi}{n}$ into a fresh surface of a sample whose composition has already been altered by the previous implant. In practice, the entire calculation is not repeated n times, but the 'fresh surface' is simulated by keeping the beam energy fixed during the sputtering process, and adding new primary ions to the appropriate momentum distribution according to the dose rate per angstrom sputtered (measured empirically).

In a standard BTE implant calculation the target may consist of a series of layers of fixed, uniform composition. For the SIMS case, we are interested in recoils from a dopant profile contained in a background material. As the calculation proceeds, dopant atoms left behind are considered sputtered and collected by the SIMS system. Other dopant atoms will be recoiled further into the target. The code was modified to include the recoiled dopant ions into the target description so that they may become candidates for recoil again as the sputtering beam moves by. Stopped atoms from the primary beam are also treated as part of the target to model the changes in composition resulting from the large sputtering doses. Care must be taken in updating the target composition since time has already been integrated out in this formulation of the transport equation. For the SIMS calculations however, the target is continually being depleted of dopant atoms and accumulating primary ions. Predictions of the number of displaced atoms based upon a static target will overestimate the number of recoils. An algorithm based upon a statistical argument is used to limit the number of recoils generated in a given layer to $((x) * (max))/(x + max)$ for x attempts to displace atoms from 'max' sites.

Figure 4 compares the calculated and measured SIMS profiles for 15 KeV Cs^+ sputtering through the As MBE layer shown in figure 2(A). A problem in dealing with the recoil ion distributions arises because of the energy resolution of the energy-angle matrix, since a recoil generated with energy less than the energy resolution can not be followed. In recoil calculations during an ion implant through a surface layer, a correction to account for these cascade recoils is applied near the interface. This is not satisfactory for sputtering calculations because it does not allow for multiple recoils of these low energy ions. For a 15 KeV primary beam, the energy resolution is 1 KeV, so that many low energy recoils will be neglected, resulting in a shorter As profile decay length (curve A). This situation is corrected for in the algorithm which limits recoil generation described

above by removing recoils moving at large angles with respect to the beam direction in preference to low angle recoils. The result is the curve labeled B. Finally, the BTE calculated profile (B) is convolved with the mixing gaussian with σ = 60 Å. The result, indicated as curve C in the figure, shows very good agreement with the measured decay length of λ_{A_s} = 105 Å.

Calculations have also been performed for Cs^+ on B in Si. Using the same calculation parameters as for the As case, the predicted decay length of the simulated SIMS profile is close to the measured value of λ_B = 130 Å. BTE calculations for 6 KeV O_2^+ sputtering do not have the energy resolution problems found in the 15 KeV Cs^+ case, so that no corrections need to be made in the handling of high angle recoil generation. Reasonable agreement is again obtained.

CONCLUSIONS

For a Cameca IMS-3f with 15 KeV Cs^+, the leading edges of B and Sb abrupt doping transitions in Si may be fit to profiles which are the convolution of a step function and a gaussian with standard deviation $\sigma \approx 65$ Å. Trailing edges exhibit explicit exponential tails. This work, and that of others suggests that the characteristic decay length, λ depends upon the projected range of the primary ion in Si (a function of M_0,E_0, and θ_{tilt}). In addition, it is species dependent, e.g. $\lambda_{A_s} \approx 105$ Å and $\lambda_B \approx 135$ Å under 15 KeV Cs^+ bombardment. This may be understood in the recoil framework in terms of the range of the recoiled dopant atoms in Si. The Boltzmann Transport Equation method for calculating recoil effects during ion implantation has been modified to treat the SIMS problem. The calculations predict recoil profiles which are in good agreement with the measured results.

ACKNOWLEDGEMENTS

We would like to thank Kwing Lee of AT & T Bell Laboratories for providing the MBE samples used in this study. Also, Chris Gronet generously offered LRP samples and SIMS profiles. SIMS analysis was performed by C. Evans and Associates, and Northern Analytical Laboratories.

REFERENCES

1. K. Wittmaack, Vacuum **34**,119 (1984).
2. F. Schulz, K. Wittmaack, J. Maul, Rad. Effects, **18**, 211 (1973).
3. F.R. Shepherd, W.H. Robinson, J.D. Brown, and B.F. Phillips, J. Vac. Sci. Technol. A **1**,991 (1983).
4. W. Vandervorst, H.E. Maes, R.F. DeKeersmaecker, J. Appl. Phys. **56**,1425 (1984).
5. H.H. Anderson, Appl. Phys. **18**,131 (1979).
6. P. Sigmund, Phys. Rev. **184**,383 (1969).
7. P. Sigmund and A. Gras-Marti, Nucl. Instr. Meth. **168**, 389 (1980).
8. P. Sigmund and A. Gras-Marti, Nucl. Instr. Meth. **182/183**, 25 (1981).
9. T. Ishitani and R. Shimizu, Appl. Phys **6**,241 (1975).
10. U. Littmark and W.O. Hofer, Nucl. Instr. Meth. **168**, 329 (1980).
11. J. Remmerie and H.E. Maes, Spectrochimica Acta **40B**, 787 (1985).
12. L.A. Christel, J.F. Gibbons, and S. Mylroie, J. Appl. Phys. **51**,6176 (1980).
13. J.F. Gibbons, C.M. Gronet, and K.E. Williams, Appl. Phys. Lett. **47**,721 (1985).
14. J.F Gibbons, W.S. Johnson, and S.W. Mylroie, *Projected Range Statistics: Semiconductors and Related Materials, Second Edition*, (Halsted Press, New York, 1975).
15. M.D. Giles and J.F. Gibbons, Nucl. Instr. Meth. **209/210**, 33 (1983).
16. L.A. Christel, J.F. Gibbons, and S. Mylroie, Nucl. Instr. Meth. **182/183**,187 (1981).

Paper # 11

EPITAXIAL ALIGNMENT OF As IMPLANTED POLYSILICON EMITTERS

J.L. Hoyt,E.F. Crabbé,J.F. Gibbons, and R.F.W. Pease,
Stanford Electronics Laboratories, Stanford, CA 94305

ABSTRACT

We demonstrate a clear advantage for high-temperature, short time annealing to induce intentional, complete epitaxial alignment of arsenic implanted, 0.5 μm-thick polysilicon films on ⟨100⟩ silicon, while minimizing arsenic outdiffusion into the substrate. Using MeV ion channeling and cross-sectional electron microscopy, epitaxial alignment was studied in the 1050-1150 °C temperature range, for arsenic doping concentrations between 1 and 10×10^{20} cm^{-3}. The alignment efficiency increases dramatically with chemical arsenic concentration in this range. An arsenic concentration of 10^{20} cm^{-3} yields alignment behavior which proceeds from the polysilicon/single-crystal interface. Between 1 and 5×10^{20} cm^{-3}, the random grain growth can exceed the rate of alignment, and large grain, highly oriented polycrystalline films can result from the RTA. For 0.5 μm-thick polysilicon films with an average doping of 10^{21} cm^{-3}, the rate of achievement of a high degree of epitaxial alignment exceeds the rate of arsenic penetration into the substrate at temperatures $\geq$ 1150 °C.

Bipolar transistors with 0.5 μm-thick emitter contacts and polysilicon dopings of 5 and 10×10^{20} cm^{-3} show less variation in base current when subjected to RTA (T $\geq$ 1100 °C) compared to devices annealed in a furnace in the 900 to 1000 °C range, while retaining the advantage over metal contacts.

INTRODUCTION

Polycrystalline silicon (polysilicon) films formed by low pressure chemical vapor deposition (LPCVD) are widely used in advanced bipolar integrated circuit technology. When deposited directly on the single crystal silicon, polysilicon serves as a diffusion source and a self-aligned contact to the extrinsic base and emitter regions. The LPCVD process results in a thin interfacial layer between the poly- and single-crystal silicon [1,2]. Subsequent furnace annealing in a standard high-speed bipolar transistor process produces partial breakup of this layer, allowing an uncontrolled amount of epitaxial regrowth of the polysilicon to take place. The transistor base current and emitter resistance are strongly dependent on the morphology of this interfacial layer [3,4]. A short, high-temperature emitter drive-in which intentionally induces complete epitaxial alignment of the polysilicon with the substrate should alleviate this process sensitivity. An added benefit of the high temperature RTA is reduced base and emitter resistance [5].

Epitaxial alignment of undoped polysilicon deposited on ⟨100⟩ silicon has been studied previously by furnace [6], and rapid thermal annealing [7] (RTA). Alignment is observed to proceed from the polysilicon/single crystal interface, where epitaxial columns form and grow towards the surface at a rate of 20-200 Å/min. in the 1000 to 1100 °C temperature range. Alignment of arsenic implanted emitters has been realized in high-frequency devices using fast furnace annealing at 1150 °C [8,9]. These authors report that high arsenic doping enhances the alignment. However, it is clear that a more thorough understanding of the epitaxial alignment process in heavily doped films is required in order to design a successful RTA process for polysilicon emitter annealing. In this work, the effect of arsenic concentration on the nature of the epitaxial regrowth is elucidated, and the kinetics and temperature dependence of alignment quantified. Bipolar transistors were also fabricated by this process, and the device results are briefly summarized in the final section.

EXPERIMENTS

Starting substrates were boron doped, 11-15 Ω – cm (100) silicon. Undoped polysilicon films of thickness 0.5 micron were deposited in a conventional LPCVD reactor at 620°C. Prior to loading, wafers were given a standard RCA clean followed by an etch in 50:1 HF with no subsequent rinse. As^+ was implanted at low beam current densities into some wafers at 150 KeV to a dose of 5×10^{15} cm^{-2}, and others at 60 KeV to doses of 2.5 and 5×10^{16} cm^{-2}. Because arsenic diffuses so rapidly in polysilicon, uniform doping

throughout the layer as measured by RBS depth profiling is obtained during the alignment anneal for the temperatures investigated in this study. The above implant schedule results in constant arsenic concentrations of 1, 5, and 10×10^{20} cm^{-3} in the polysilicon. Wafers were capped with LPCVD oxide deposited at 450 °C to prevent arsenic loss, and then cleaved into small squares. For a given anneal condition, samples from all three wafers were subjected to RTA in a tungsten-halogen lamp system simultaneously. Samples were placed on a silicon wafer with a thermocouple embedded in its center, and the annealer was operated in closed-loop mode. Temperatures ranged from 1050 to 1150°C for times of 10 to 1000 seconds. After the RTA, arsenic diffusion profiles were obtained by Rutherford backscattering (RBS). Structural changes in the polysilicon films were studied via 2.2 MeV ^{4}He ion channeling and cross-sectional transmission electron microscopy (XTEM).

A. Arsenic concentration effects and temperature dependence

The strong effects of arsenic concentration and temperature on the morphology of annealed films are illustrated in Fig. 1, which shows XTEM micrographs of samples subject to 10 second anneals. The three samples shown in Fig. 1 (a)-(c) were annealed simultaneously at 1150 °C. At an arsenic concentration of 10^{20} cm^{-3} (a), the polysilicon is partially aligned from the interface towards the surface, leaving an uppermost layer which remains polycrystalline. The extent of alignment is laterally nonuniform. Increasing the doping to 5×10^{20} cm^{-3} results in complete epitaxial regrowth to the sample surface over most of the film, with a defected layer remaining (b). The major residual defects are twins and stacking faults. The same anneal yields complete alignment for a sample doped to 10^{21} cm^{-3} (c). The interfacial layer between the original poly- and single-crystal silicon is still visible, but has broken up into individual oxide inclusions as seen in other XTEM studies of polysilicon alignment [2]. Decreasing the anneal temperature by 50 degrees produces the film morphology illustrated in (d), for an 1100 °C anneal. The high arsenic concentration (10^{21} cm^{-3}) has resulted in enhanced grain growth, so that after only 10 seconds the average grain size in the film has exceeded the layer thickness of 0.48 microns. Selected area diffraction patterns (not shown) indicate that some grains (e.g. region A in the figure) are epitaxially aligned to the substrate, while others are not (region B).

Fig. 2 shows the ⟨100⟩ axial ion channeling spectra for the samples pictured in Fig. 1 (a)-(c) (1150-10 sec. RTA), compared to a spectrum for an unannealed polysilicon film. For an arsenic doping of 10^{20} cm^{-3} (curve (a)), we see that the **average** regrown thickness extends ≈ 2000 Å from the poly/single-crystal interface. The graded low-energy edge of this spectrum results from the nonuniform regrowth seen in the TEM. (Fig. 1(a)). When the arsenic concentration is raised to 5 and 10×10^{20} cm^{-3}, the dramatically enhanced grain growth alters the nature of the resulting channeling spectra (b) and (c), and it is no longer meaningful to speak of an 'alignment rate'. A useful measure of the degree of epitaxial alignment in cases where the average grain size reaches the film thickness is the integrated yield χ_{int}, defined as the integral of the aligned spectrum over the 0.48 micron film thickness, divided by the corresponding integral of the random spectrum. The integrated yields for the spectra in Fig. 2(b) and (c) are 0.10 and 0.065 respectively. For comparison, we find an integrated yield of 0.055 for a virgin silicon sample.

Fig. 3 compares the kinetics of the alignment process at 1100 °C for 10^{20} (a) and 10^{21} cm^{-3} (b) arsenic concentrations in the polysilicon. In the lower arsenic concentration case (a), the 30 and 90 second spectra show that the film aligns from the interface in a manner qualitatively similar to the undoped case [7]. However, the increase in aligned thickness appears to be nonlinear in time. In general, we have measured initial alignment rates which are higher than those extrapolated from our longer time data. In the high concentration case (b), the backscattering yield within the 0.48 μm layer is high for the 10 second RTA, but drops with increasing anneal time, indicating improving epitaxial alignment. For a given anneal time, the yield is constant within this layer, and the shape of the channeling profile is typical of large-grain polycrystalline films, in sharp contrast to the spectra shown in (a).

B. Alignment kinetics versus diffusion

We have studied the temperature dependence of the alignment kinetics in detail for the highest arsenic doping in the polysilicon (10^{21} cm^{-3}), and compared it to the rate of

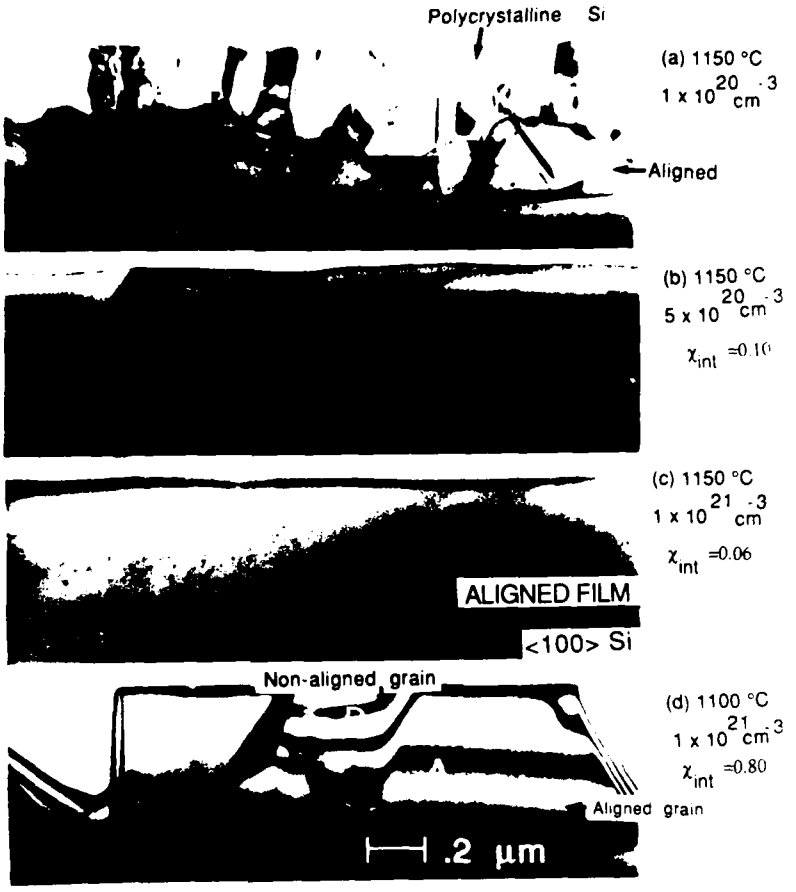


Fig. 1: Cross-sectional transmission electron microscopy observations of 10-sec. anneals illustrating the strong effect of arsenic doping N_{As} on epitaxial alignment. At an arsenic concentration of 10^{20} cm^{-3}, the polysilicon is partially regrown from the interface towards the surface. The epitaxial alignment increases dramatically as N_{As} is increased to 5 (b) and 10×10^{20} cm^{-3} (c). The interfacial layer has broken up into oxide inclusions. Micrograph (d) illustrates the decrease in alignment efficiency for a 10^{21} cm^{-3} sample annealed at 1100 °C, compared to (c) at 1150 °C. The MeV ion channeling integrated yields are also indicated.

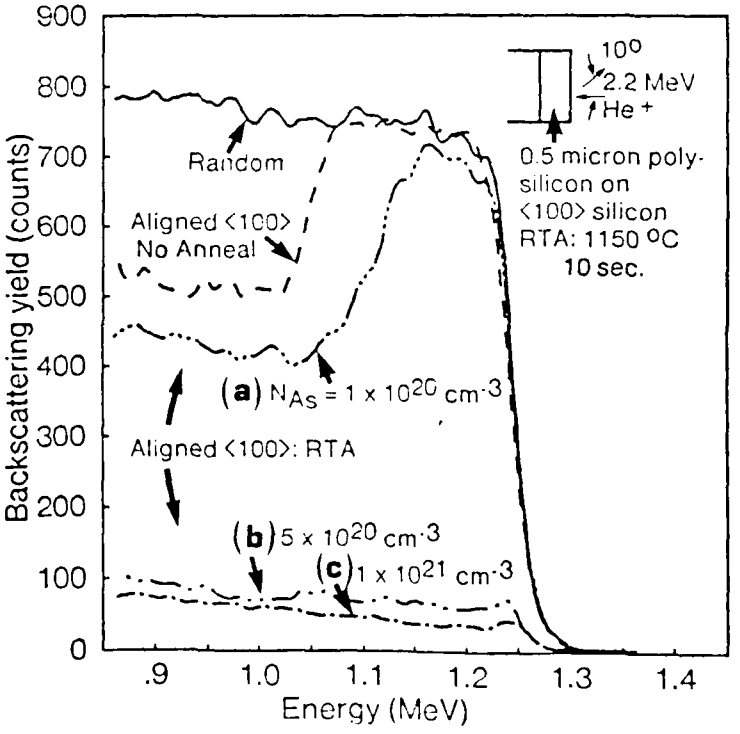
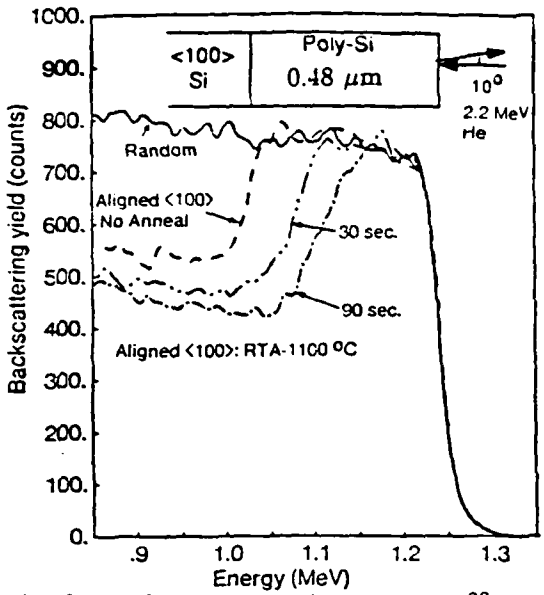
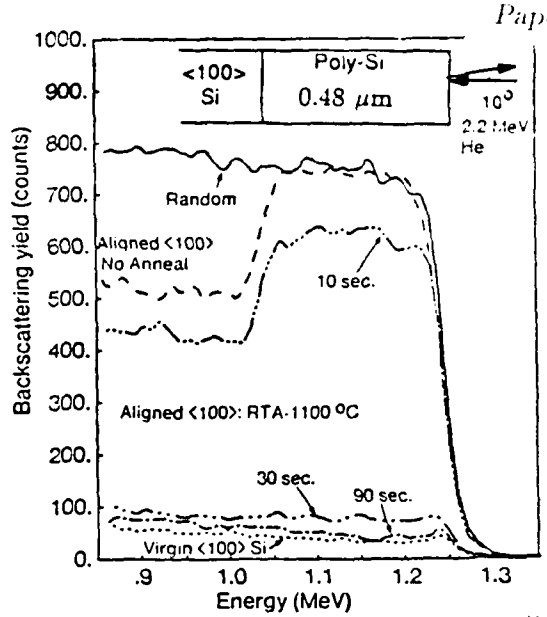


Fig. 2: Backscattering spectra corresponding to the micrographs of Fig. 1 (a)-(c), for an 1150 °C-10 sec. RTA. The graded low-energy edge of spectrum (a) corresponds to the nonuniform regrowth seen in the TEM (Fig. 1(a)). The fact that the aligned yield for this sample does not reach the random value indicates that some fraction of the film has regrown to the surface. The drop in the aligned yields for (b) and (c) illustrates the dramatic improvement in alignment efficiency for $N_{As} \geq 5 \times 10^{20}$ cm^{-3}.



(a) Channeling spectra for $N_{As} = 10^{20}$ cm^{-3}. The polysilicon film aligns from the interface towards the surface. The initial rate of alignment appears higher than that between 30 and 90 sec.



(b) Channeling spectra for $N_{As} = 10^{21}$ cm^{-3}. The higher doping produces large grain polycrystalline silicon and hence the different shape of the profiles compared to (a).

Fig. 3: A comparison of the kinetics of the alignment process at 1100 °C for the lowest (a) and highest (b) arsenic dopings. Channeling spectra were obtained by aligning the analyzing beam to the substrate ⟨100⟩ direction.

arsenic outdiffusion into the substrate, as measured by Rutherford backscattering depth profiling. The shape of the arsenic diffusion profiles is indicative of the degree of epitaxial alignment with the substrate. Fig. 4 illustrates the evolution of the 1100 °C diffusion profiles as the film changes from large grain polycrystalline after 10 seconds, to epitaxial silicon after 90 seconds. The arsenic segregation peak at the original poly/single-crystal interface disappears between 10 and 30 seconds as the integrated yield drops to 0.1, and subsequent diffusion profiles exhibit a shape associated with high concentration arsenic diffusion in single-crystal silicon.

Junction depths measured with respect to the original silicon surface were extracted from the RBS profiles by noting the depth corresponding to an arsenic concentration of 1×10^{19} cm^{-3}(see Fig. 4). Fig. 5 compares junction depths (closed symbols) to integrated yield (open symbols) as a function of anneal time at 1067, 1100, and 1150 °C. Since the XTEM of Fig. 2 (b) shows few residual defects, and corresponds to an integrated yield χ_{int} of 0.065, we have chosen this value as a criterion for reasonable alignment. For a χ_{int} of 0.065, the junction depths are 1500 Å at 1150 °C and 2000 Å at 1100 °C. This clearly illustrates the advantage of higher temperature, shorter time anneals. Since we have made direct comparisons of junction depth and integrated yield on the same samples, this conclusion is **independent** of errors in the determination of the exact temperature versus time profiles.

Fig. 6 is an Arrhenius plot comparing the epitaxial alignment and arsenic outdiffusion processes. The rate of increase in epitaxial quality may be measured by the inverse of the time required to reach an integrated yield of 0.065, $(\tau_{0.065})^{-1}$, which has a very strong temperature dependence. A measure of arsenic diffusion into the substrate may be obtained by the slope of graphs of X_j^2 versus time at a given temperature, which is the dashed line in the figure. We find an activation energy of 4.2 eV for this process, consistent with high concentration arsenic diffusion in silicon[10]. By dividing the diffusivity scale by $(10^{-5}$ cm$)^2$ we can use the left-hand axis to find $(\tau_{0.1\ \mu m})^{-1}$, the inverse of the time required to produce an arsenic penetration of 0.1 μm, and can compare the two processes directly on the same scale. In this case, annealing at temperatures $\geq$ 1150 °C (the intersection of the two curves) is necessary to minimize arsenic outdiffusion while maximizing the alignment process for 0.5 μm-thick films.

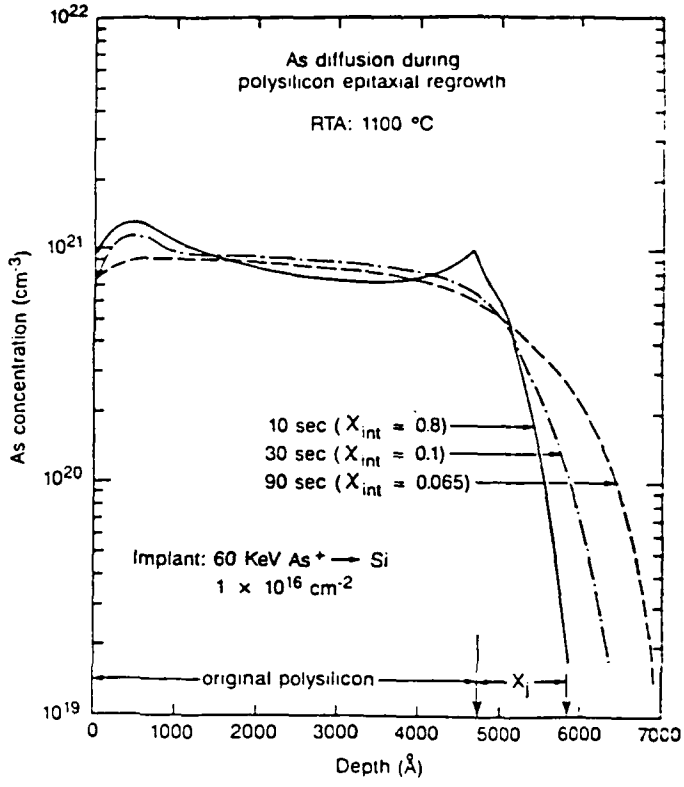


Fig. 4: Arsenic diffusion profiles for samples annealed at 1100 °C for 10, 30 and 90 seconds, obtained by Rutherford backscattering. Also indicated are the measured integrated yields calculated from the channeled spectra of Fig. 3 (b). The segregation at the original polysilicon /single-crystal interface is no longer visible after the 30 sec. anneal.

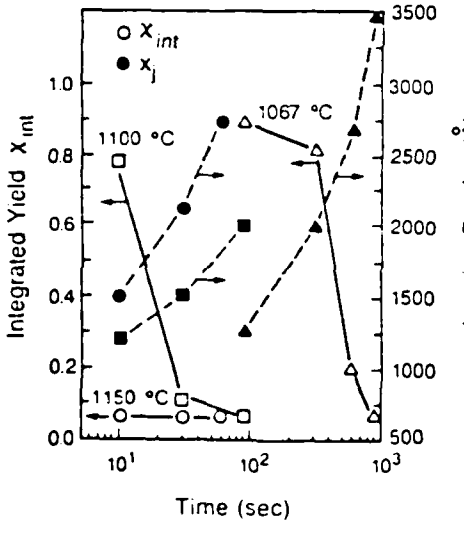


Fig. 5: Integrated yield (open symbols) and arsenic junction penetration (solid symbols) vs. RTA time for three different temperatures. An integrated yield of 0.065 is obtained for anneals of 1150 °C-10 sec. and 1100 °C-90 sec., with corresponding junction depths of 1500 and 2000 Å, demonstrating the advantage of high temperature RTA.

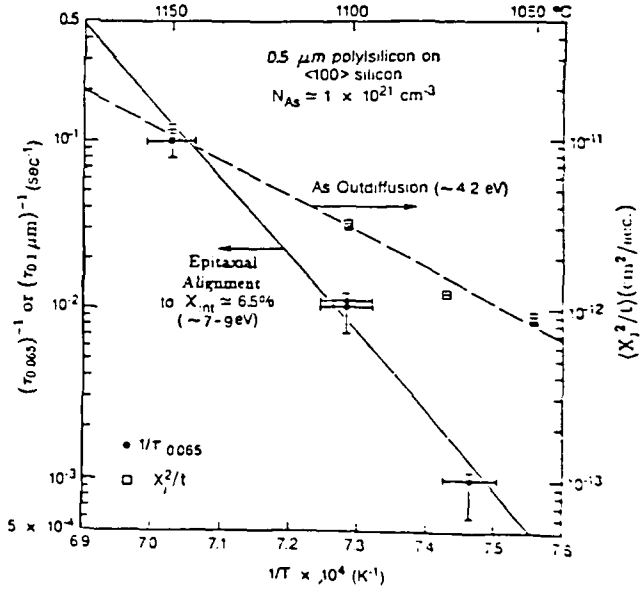


Fig. 6: An Arrhenius plot comparing the outdiffusion (dashed line) and epitaxial alignment (solid line) processes. $\tau_{0.065}$ is the time required to reach an integrated yield of 0.065 from Fig. 5. When referred to the left-hand axis, the dashed line also represents $(\tau_{0.1\,\mu m})^{-1}$, the inverse of the time to produce an arsenic penetration of ≈ 0.1 μm.

C. Device Results

Bipolar transistors were fabricated with 0.5 μm-thick polysilicon contacts to the emitters, and average polysilicon dopings of 5 and 10 $\times 10^{20}$ cm^{-3}. The devices were annealed at temperatures ranging from 1100 to 1180 °C. High polysilicon doping levels are necessary to minimize the storage of minority carriers in the aligned emitters. The devices were characterized by their base current, which is a measure of emitter performance [3]. We found the base current to be quite independent of the measured integrated yields although a wide range of values of χ_{int} was obtained [11]. The higher temperatures have essentially eliminated the major effects of the interfacial layer and also produced enhanced dopant activation in the aligned polysilicon. The insensitivity of the base current to the integrated yield may be explained by the fact that it is dominated by Auger recombination in the emitter, and the Auger lifetime is so low at such high doping levels that the final quality of the regrown material has little effect on the base current. We have found that the advantage of using a polysilicon contact to the emitter remains after the RTA. In addition, the emitter resistance of such devices is expected to be very low, and less process dependent than for furnace annealed devices.

CONCLUSIONS

For LPCVD polysilicon on (100) silicon, a quantitative analysis of epitaxial quality and arsenic diffusion into the underlying substrate shows a clear advantage for high temperature RTA to obtain more complete epitaxial alignment and minimum arsenic outdiffusion. For 0.5 μm-thick polysilicon films with an average doping of 10^{21} cm^{-3}, the rate of achievement of epitaxial alignment to a channeling integrated yield of 0.065 exceeds that of arsenic penetration into the substrate to a depth of roughly 0.1 μm for temperatures $\geq$ 1150 °C. The alignment efficiency increases dramatically with chemical arsenic concentration from 1 to 10 $\times$ 10^{20} cm^{-3}. An arsenic concentration of 10^{20} cm^{-3} yields alignment behavior similar to the undoped case. Between 1 and 5 $\times 10^{20}$ cm^{-3}, the grain growth rate exceeds that of alignment, and large grain, highly oriented polycrystalline films can result from the RTA. Bipolar transistors fabricated with 0.5 μm-thick emitter contacts and polysilicon dopings of 1 and 5 $\times 10^{20}$ cm^{-3} show less variation in base current when subjected to RTA ($T \geq 1100$ °C) compared to devices annealed in a furnace in the 900 to 1000 °C range, while retaining the advantage over metal contacts.

ACKNOWLEDGEMENTS

We wish to thank W. Opyd and Dr. A. Marshall for assistance with the XTEM, and and Dr. J. Crowley of Peak Systems for annealing the device wafers. The support of the Defense Advanced Research Projects Agency, Lawrence Livermore National Laboratory, and Tektronix Inc. is also acknowledged.

REFERENCES

1. C.Y. Wong, A.E. Michel, R.D. Isaac, R.H. Kastl, and S.R. Mader, *J. Appl. Phys.*, **55** (4),1131 (1984).
2. J.C. Bravman, G.L. Patton, and J.D. Plummer, *J. Appl. Phys.*, **57** (8),2779 (1985).
3. G.L. Patton, J.C. Bravman, and J.D. Plummer, *IEEE Trans. Electron Devices*, **ED-33**,1754 (1986).
4. E. Crabbé, S. Swirhun, J. del Alamo, R.F.W. Pease, and R.M. Swanson, 1986 Intl. Elect. Dev. Meeting Tech. Dig. (IEEE,New York,1986),p. 28.
5. H.Takemura, et al., 1986 IEDM Tech. Dig. (IEEE,New York, 1986), p. 424.
6. B.Y. Tsaur and L.S. Hung, *Appl. Phys. Lett.*,**37**, 648 (1980).
7. H.B. Harrison, C. Wong, Y. Komem, and S. Cohen, Mat. Res. Soc. Symp. Proc. Vol 71, (Materials Research Society, Pittsburgh, 1986),p. 455.
8. N. Natsuaki, M. Tamura, T. Miyazki, and Y. Yanagi, Intl. Elect. Dev. Meeting Tech. Dig. (IEEE, New York, 1983),p. 662.
9. M. Tamura, N. Natsuaki, S. Aoki, *Jap. Journal Appl. Phys.*, **24** (2),L151 (1985).
10. J.L. Hoyt and J.F. Gibbons, Mat. Res. Soc. Symp. Proc. Vol. 52, (Materials Research Society, Pittsburh, 1986), p. 15.
11. E. Crabbé, et al., to be published in Tech. Dig. of the 1987 Symp. on VLSI Technology, (Karuizawa, Japan, 1987).

Paper # 12

Novel Emitter Contacts for VLSI Bipolar Transistors

E. Crabbé, J.L. Hoyt, M.M. Moslehi, R.F.W. Pease, and J.F. Gibbons

Stanford Electronics Laboratories, Stanford University

Abstract

Polysilicon emitter contacts are extremely attractive for bipolar transistors, but they suffer from process sensitivity. Two different approaches are proposed to improve the reproducibility. In the first, rapid thermal annealing is used to induce complete epitaxial alignment of the polysilicon to the substrate. The base current of these devices exhibits little dependence on the anneal conditions while retaining the advantage of polysilicon compared to metal contacts. In the second approach, the silicon surface is thermally nitrided prior to polysilicon deposition to form a very thin nitride interface, and the resulting base currents are extremely low.

Introduction

As bipolar transistors are scaled laterally and vertically to increase the speed of operation, the emitter thickness is reduced to 0.1 μm or less and the contact to the emitter dominates the DC characteristics. Polysilicon contacts to the emitter provide substantial improvements compared to conventional metal contacts. The current gain is increased, and it can be traded-off for a decrease in base resistance to improve the switching speed. The morphology of the interfacial layer between the polysilicon and the single-crystal silicon critically affects the base current and the emitter resistance of these devices. For high-speed applications, high polysilicon doping levels and moderate to high anneal temperatures are preferred in order to reduce the emitter resistance by partially breaking up the interfacial oxide [1,2]. The integrity of the interfacial oxide layer is very sensitive to the process, leading to large variations in base current and emitter resistance from run to run. Two approaches to reduce this process sensitivity while maintaining the advantages of the polysilicon contacts are investigated in this paper. The first one consists of rapid thermal annealing (RTA) the polysilicon-contacted devices to eliminate the interfacial layer and induce epitaxial alignment with the substrate. The nature of this recrystallization is discussed in the next section, and the resulting transistor characteristics are described in the following one. The second approach consists of improving the integrity of the interface by growing an extremely thin thermal nitride layer by rapid nitridation. Bipolar transistors with such emitters were fabricated and their characteristics are described.

Characterization of aligned polysilicon

The process dependence of the polysilicon epitaxial alignment to the substrate was investigated first before transistor fabrication. Undoped 0.5 μm-thick polysilicon films were deposited in a conventional LPCVD reactor at 620°C. Prior to loading, the wafers were given a standard RCA clean followed by an etch in 50:1 HF with no subsequent rinse. Arsenic was then implanted to achieve polysilicon average doping concentrations of 1×10^{20}, 5×10^{20} and 1×10^{21} cm^{-3}. After low temperature oxide deposition to form a cap, the wafers were rapid thermal annealed (RTA) in a tungsten-halogen lamp system with temperatures ranging from 1050 to 1150°C and times of 5 to 30 seconds. The regrown films were characterized by MeV ion channeling, Rutherford backscattering (RBS) and cross-sectional transmission electron microscopy (XTEM).

The strong effect of arsenic concentration on the morphology of annealed films is illustrated in Figs. 1 and 2. Fig. 1 shows the ion channeling spectra and the corresponding XTEM micrographs are given in Fig. 2. Both figures are for samples subjected to an 1150 °C anneal for 10 sec. It is clear that both the grain growth and the epitaxial alignment rates increase with arsenic concentration, and that the epitaxial quality is greatly improved for $N_{As} \geq 5\times10^{20}$ cm^{-3}. A good indication of the extent of alignment is the integrated yield χ_{int} defined as the integral of backscattered counts for a (100) aligned spectrum over the 0.5 μm film, divided by the corresponding integral of the random spectrum. Figs. 1 and 2 illustrate the correspondance between the spectrum shape, the quantity χ_{int}, and the film morphology as revealed by XTEM. Figs.

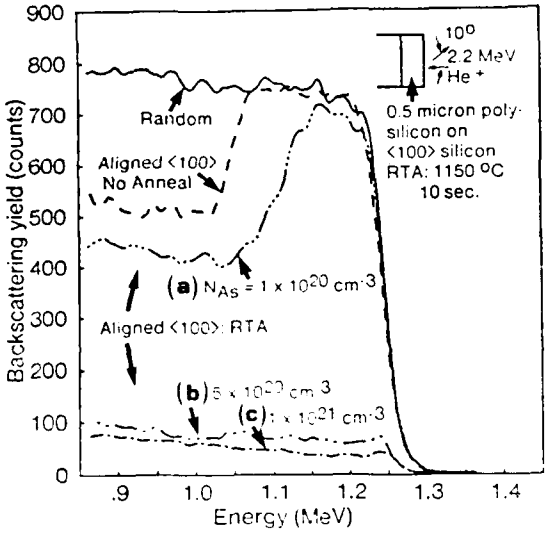


Fig. 1 Backscattering spectra illustrating the strong arsenic concentration dependence of the epitaxial alignment of 0.48 μm-thick LPCVD, arsenic implanted polysilicon films. All three samples were annealed simultaneously at 1150 °C for 10 seconds. Arsenic concentrations throughout the polysilicon are 1, 5, and 10 $\times 10^{20}$ cm^{-3} for samples with ion channeling spectra labeled (a), (b) and (c) respectively. The epitaxial quality of the regrown films is greatly improved for $N_{As} \geq 5 \times 10^{20}$ cm^{-3}.

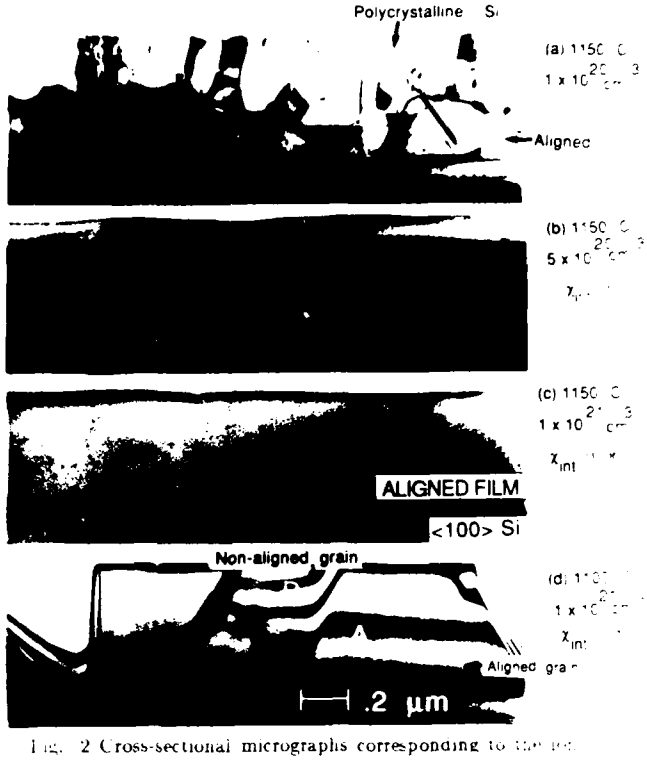


Fig. 2 Cross-sectional micrographs corresponding to the ion channeling spectra for samples (a), (b), and (c) of Fig. 1. At an arsenic concentration of 1 x 10^{20} cm^{-3}, the polysilicon is partially regrown epitaxially from the interface toward the surface. The graded low-energy edge of Fig. 1 (a) corresponds to the nonuniform regrowth seen in the TEM (a). Increasing the doping to 5 x 10^{20} cm^{-3}results in complete regrowth to the sample surface, with a highly defected layer as seen in (b). The corresponding channeling spectra has an integrated yield χ_{min} of 0.10. The same anneal yields complete epitaxial alignment for a sample doped to 1 x 10^{21} cm^{-3}(c). Micrograph (d) illustrates the decrease in alignment efficiency for a 1 x 10^{21} cm^{-3} sample annealed at 1100 °C, compared to (c).

2 (c) and (d) also illustrate the strong temperature dependence of the alignment process. A quantitative study of the trade-off between junction depth measured with respect to the original silicon surface and epitaxial alignment indicates that higher temperatures for very short times are preferable to lower temperatures and longer times. This minimizes arsenic outdiffusion and improves the epitaxial quality [3].

Recrystallized emitters

When the interfacial layer between the polysilicon and the single crystal is eliminated, the hole storage in the emitter is of primary concern. The emitter component τ_e of the delay $\tau = 1/2\pi f_T$ where f_T is the cutoff frequency must be minimized. Since τ_e is directly proportional to the Auger recombination lifetime, the emitter doping level should be as high as possible. An arsenic concentration above 4×10^{20} cm^{-3} will satisfy this requirement and, as discussed previously, will improve the alignment rate. Very high anneal temperatures are also desirable in this context to maximize dopant activation.

RTA offers two advantages for the fabrication of bipolar transistors: it reduces the process sensitivity of the emitters as described below, and it is also responsible for a substantial decrease of the extrinsic base and emitter resistances as a result of the higher dopant activation in the polysilicon (both the polysilicon resistance and the metal-to-polysilicon contact resistance are reduced) [4,5].

Bipolar transistors with 0.5 μm-thick polysilicon contacts to the emitters were fabricated. Wafers received an HF dip etch immediately before the LPCVD polysilicon deposition, and hence only a native oxide is present at the interface. The wafers were then implanted with doses of 2.5 and 5×10^{16} cm^{-2} and then capped with LPCVD oxide to prevent arsenic outdiffusion. The devices were then annealed by RTA at temperatures of 1100 to 1150 °C and times varying between 1 and 30 sec. A Peak Systems ALP-6000 was employed to take advantage of its extremely fast temperature rise and fall times.

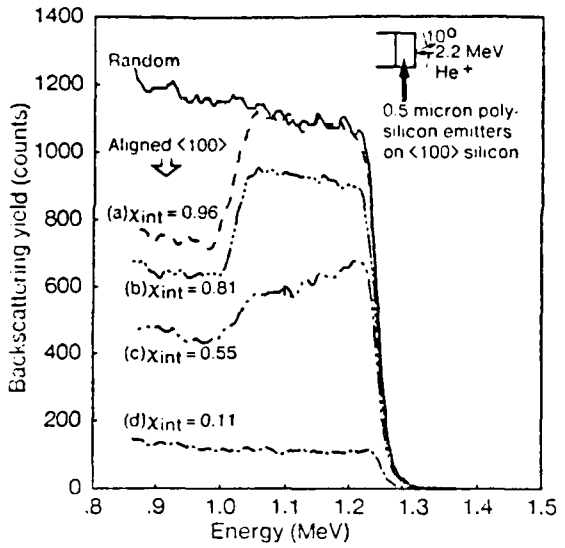


Fig. 3 Representative backscattering spectra obtained for polysilicon emitters subjected to RTA. The anneal conditions were chosen to yield a wide range in the extent of epitaxial alignment as measured by ion channeling. Spectra (a) and (b) are for samples doped to 1×10^{21} cm^{-3} with RTA conditions of 1100 °C for 10 and 30 seconds respectively, and (c) and (d) for 5×10^{20} cm^{-3} with RTA conditions of 1150 °C for 5 and 30 sec. respectively. *The improvement in epitaxial quality* with time at a fixed temperature is illustrated by the drop in the yield for (c) as compared to (d).

Sample	N_{A_0} (cm^{-3})	RTA (°C - sec.)	χ_{int}	X_j (μm)	Φ_{Hall} (cm^{-2})
b1	1×10^{21}	1100-10	0.96	0.085	1.63×10^{16}
b2	1×10^{21}	1100-30	0.81	0.16	1.95×10^{16}
n13	1×10^{21}	1150-5	≤ 0.55	0.11	-
n14	1×10^{21}	1150-30	≤ 0.106	0.25	-
b3	1×10^{21}	1180-1	0.75	0.090	1.87×10^{16}
b6	5×10^{20}	1100-10	≥ 0.96	0.08	1.39×10^{16}
b7	5×10^{20}	1100-30	≥ 0.81	0.14	1.50×10^{16}
b4	5×10^{20}	1150-5	0.55	0.08	1.46×10^{16}
b5	5×10^{20}	1150-30	0.106	0.21	2.14×10^{16}

Table 1 Integrated yield χ_{int}, junction depth measured with respect to the original polysilicon/single crystal silicon interface X_j, and the total emitter charge Φ_{Hall} as measured by sheet Hall effect for device wafers subject to RTA after the emitter implant.

The quality of the recrystallized emitter contacts was analyzed by ion channeling and characterized by the integrated yield χ_{int} (see Table 1). The values obtained for χ_{int} in the device run at a given temperature differ slightly from those described in the previous section; the discrepancy is attributable to small differences in the temperature calibration of the two RTA systems. The ion channeling spectra of Fig. 3 indicate that the various RTA conditions produced a wide range of epitaxial alignment quality among the device wafers: χ_{int} varies between 0.11 and 0.96 (Table 1). The emitter profiles were obtained by SIMS, RBS and spreading resistance. The junction depths with respect to the original interface are given in Table 1 and vary between 0.09 and 0.25 μm. The integrated charges in the emitters are also given in Table 1 and were obtained by Hall effect measurements.

The emitters are characterized by their saturation current densities J_{oe} rather than the current gain of the transistors to eliminate the base dependence. As base recombination is negligible in these devices, J_{oe} can be extracted from the ideal component of the base current as illustrated in Fig. 4. The values of J_{oe} are reported for a temperature of 300 K, as a decrease in temperature of only 6°C leads to a reduction of J_{oe} by a factor of roughly 2.7. All measurements were performed on devices with large area-to-perimeter ratios to neglect the perimeter component of the base current.

The experimental values for J_{oe} are given in Fig. 5 as a function of the anneal conditions and for the two polysilicon doping levels. Although a wide range of epitaxial alignment is obtained, J_{oe} is quite independent of χ_{int} and is rather high compared to optimized polysilicon emitter contacts ($\sim 1.5 \times 10^{-12}$ vs. $\sim 5 \times 10^{-13}$ A/cm^2). This is not surprising considering the high anneal temperatures and the high emitter doping levels. The anneal temperatures are high enough to eliminate the interfacial oxide layer which blocks hole injection into the polysilicon. J_{oe} is dominated by Auger recombination, and the Auger lifetime is so low at such high doping levels that the final quality of the recrystallized material is a secondary consideration as far as J_{oe} is concerned. Lower doping levels may induce a reduction of J_{oe}, but the increased hole storage in the emitter would dramatically degrade the frequency performance (τ_e would be the dominant component in the equation for f_T).

The experimental J_{oe} values are compared to those obtained by simulation for devices contacted by metal and with identical profiles in the single-crystal part of the emitter under the original interface. The modeling procedure is the one described in [6] and consists of solving the minority-carrier transport equations using the single-crystal emitter profile. The parameters from [7] are used for the heavy-doping effects. The modeling was checked by computing J_{oe} for a transistor with a metal contact and comparing it to the experimental value: the two are within 10% of each other, and no fitting parameter is used in the model. For

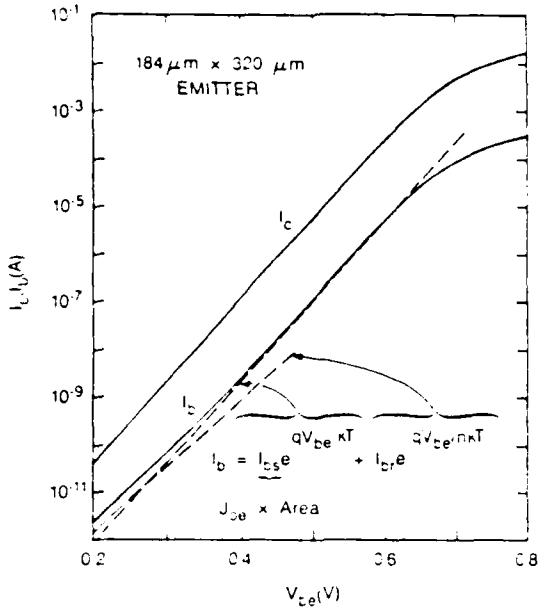


Fig. 4 Transistor collector and base characteristics illustrating the extraction of the emitter saturation current density J_{oe} from the ideal component of the base current.

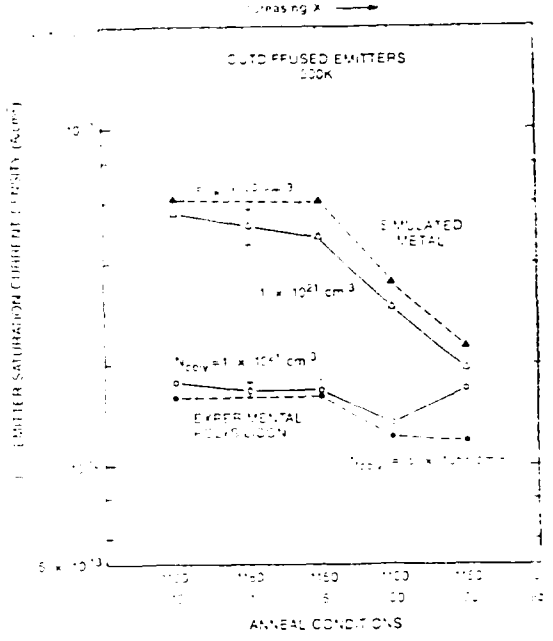


Fig. 5 Emitter saturation current density J_{oe} for various anneal conditions and two polysilicon concentrations. J_{oe} is fairly insensitive to the process variations. For comparison, we show simulated J_{oe} values for devices with identical outdiffused emitter profiles but contacted by metal. The advantage over metal contacts clearly remains after epitaxial alignment by RTA.

long anneals such as 1150°C for 30 sec., the single-crystal part of the emitter becomes almost opaque and the contact plays a small role. The advantage of the polysilicon contacts over metal contacts clearly remains after epitaxial alignment by RTA.

Nitrided interfaces

In standard polysilicon emitter contacts, the break-up of the native oxide at the interface is responsible for the high process sensitivity of these devices. The integrity of this interface can be improved by thermally nitriding the emitter surface prior to polysilicon deposition. Films 15 to 20 Å-thick were obtained by rapid thermal nitridation (RTN) in an AET ADDAX R1000 Rapid Thermal Processor. After a standard RCA clean, the wafers received an HF dip etch just prior to the nitridation. The thermal nitridations were performed in an ammonia ambient for 30 seconds at either 750 or 900°C. The wafers were then immediately loaded in an LPCVD reactor for undoped polysilicon deposition. Several implant and anneal conditions followed. The resulting J_{oe} are shown in Fig. 6. All the devices have pre-implanted emitters (arsenic implants of 5×10^{14} cm^{-2} annealed for 1 hour at 1000°C before polysilicon deposition). For comparison, the J_{oe} for polysilicon emitter contacts with native oxide interfaces are also presented.

The interfaces of the devices with polysilicon arsenic concentrations of 2×10^{20} cm^{-3}annealed at 1000°C for 1/4 hr. were examined by high resolution transmission electron microscopy (HREM). The thicknesses of the nitride interfaces are 17 Å and 21Å ± 2Å for the 750 and 900°C nitridations respectively. In both cases, no break-up of the interface is observed, and no alignment of the polysilicon has taken place although the anneal temperature is high.

The emitter saturation current densities of the nitride interfaces are substantially lower than those of native oxide interfaces (Fig. 6). These extremely small values for J_{oe} indicate that little recombination occurs at the thermally nitrided interfaces. In contrast to oxide interfaces [6], thicker nitride layers do not improve J_{oe}, and J_{oe} is fairly independent of the polysilicon doping level. Contrary to native oxide interfaces, a high anneal temperature reduces J_{oe}. Low emitter resistances should be obtainable by decreasing the nitride thickness. This can be achieved by performing RTN and polysilicon deposition in-situ, immediately after an in-situ substrate plasma clean.

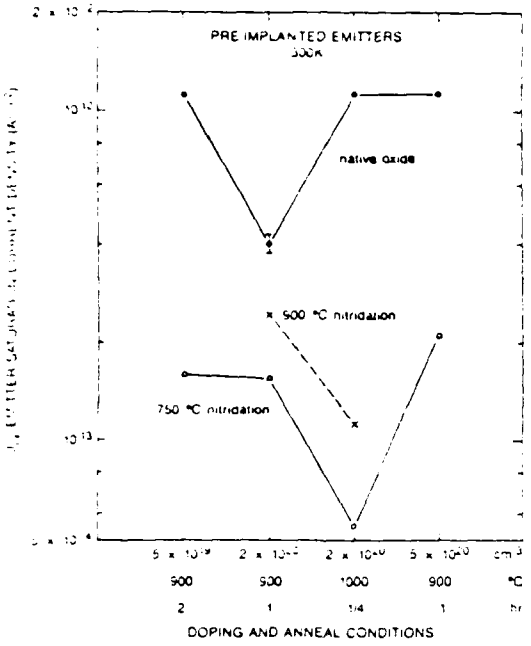


Fig. 6 J_{oe} versus process conditions for devices with different interface treatments. The upper curves are for native oxide interfaces obtained by performing an HF dip just prior to loading wafers into the LPCVD reactor. The lower curves are for devices with nitrided interfaces (by rapid thermal nitridation). The nitrided emitters have J_{oe}'s substantially lower than the native oxide emitters.

Conclusion

Two approaches to reduce the process dependence of polysilicon emitter contacts while maintaining their advantages have been explored. In the first one, rapid thermal annealing eliminates the interfacial layer at the polysilicon-silicon interface and promotes complete epitaxial alignment of the polysilicon. The base current exhibits little dependence on process conditions and the emitter resistance should be very low. The second approach consists of improving the integrity of the interfacial layer by growing an extremely thin thermal nitride layer. This film is not degraded by anneal temperatures as high as 1000°C, and the emitter saturation current densities are as low as 6×10^{-14} A/cm^2, almost an order of magnitude lower than for native oxide interfaces.

Acknowledgements

We would like to thank John Crowley of Peak Systems, Wally Opyd for help with TEM sample preparation, Dr. Ann Marshall for the timely TEM analysis and the staff of the Integrated Circuits Laboratory. The support of Lawrence Livermore National Laboratories under contract 8916605, Tektronix Inc. and DARPA under contract DAAG29-85-K-0054 is greatly appreciated.

References

1. J.M.C. Stork and J.D. Cressler, "The impact of non-ohmic polysilicon resistance on bipolar transistor performance," *1986 Symp. on VLSI Technol. Dig. Tech. Papers*, p.47.

2. E. Crabbé, S. Swirhun, J. del Alamo, R.F.W. Pease and R.M. Swanson, "Majority and minority carrier transport in polysilicon emitter contacts," *1986 IEDM Tech. Dig.*, p.28.

3. J.L. Hoyt, E. Crabbe, J.F. Gibbons and R.F.W. Pease, "Epitaxial alignment of arsenic implanted polycrystalline silicon films on (100) silicon obtained by rapid thermal annealing," *Appl. Phys. Lett.*, in press, March 1987.

4. N. Natsuaki, M. Tamura, T. Miyazaki and Y. Yanagi, "Rapid-thermal annealing of a polysilicon-stacked emitter structure," *1985 IEDM Tech. Dig.*, p.602.

5. H. Takemura, T. Kamiya, S. Ohi, M. Sugiyama, T. Tashiro and M. Nakamae, "Submicron epitaxial layer and RTA technology for extremely high speed bipolar transistors," *1986 IEDM Tech. Dig.*, p.424.

6. G.L. Patton, J.C. Bravman and J.D. Plummer, "Physics, technology, and modeling of polysilicon emitter contacts for VLSI bipolar transistors," *IEEE Trans. Electron Devices*, vol. ED-33, p.1754 (1986).

7. J. del Alamo, S. Swirhun and R.M. Swanson, "Simultaneous measurements of hole lifetime, hole mobility, and bandgap narrowing in heavily doped n-type silicon," *1985 IEDM Tech. Dig.*, p.290.

Limited reaction processing: Growth of III-V epitaxial layers by rapid thermal metalorganic chemical vapor deposition

S. Reynolds, D. W. Vook, and J. F. Gibbons
Stanford University Electronics Laboratories, McCullough 226, Stanford, California 94305

(Received 6 October 1986; accepted for publication 28 October 1986)

We have demonstrated a new technique for III-V epitaxial layer growth combining rapid thermal processing and metalorganic chemical vapor deposition. This technique yields enhanced layer thickness control and abrupt interfaces while maintaining a high growth rate (>10 Å/s). Multilayer structures have been grown with smooth, featureless surfaces and good electrical quality ($N_d = 2\times10^{16}$ cm^{-3}, $\mu_n = 3000$ cm^2/V s) using trimethylarsenic and trimethylgallium.

The recent interest in GaAs and related III-V materials has been stimulated by the development of epitaxial growth techniques which yield materials of both good crystal and electrical quality along with tight control over layer thickness and interface abruptness. One of these techniques, metalorganic chemical vapor deposition (MOCVD), produces abrupt interfaces using elaborate and costly gas switching systems along with reduced reactor pressure. Recently, a new method of layer control has been demonstrated by Gibbons *et al.* for high quality thin layer growth of silicon layers with abrupt interfaces.[1,2] This method, limited reaction processing (LRP), uses rapid precise changes in the substrate temperature to switch layer growth on and off rather than relying on gas phase switching.

We report rapid thermal switched growth of GaAs epitaxial layers. We have extended this technique with equal success to $Al_xGa_{1-x}As$ ($0<x<0.25$) and $In_yGa_{1-y}As$ ($0<y<0.03$), all on GaAs substrates. Good electrical characteristics and surface morphology, featureless to within the resolution of our Nomarski microscope (1100 ×), have been consistently obtained. In contrast to standard MOCVD, this technique maintains a high growth rate (10 Å/s) at atmospheric pressure while producing abrupt interfaces.

Layers were grown using trimethylarsenic, trimethylgallium, trimethylaluminum, and triethylindium, all purchased from Alfa Products (Danvers, MA). Substrates, undoped and Si doped (100) Czochralski, were degreased and given a 5:1:1 H_2SO_4:H_2O_2:H_2O etch prior to loading. Optimum layers were grown at 670–720 °C with 3.5 l/min of total H_2 flow and a trimethylarsenic partial pressure of about 0.5 Torr. GaAs layers have *n*-type background doping (2×10^{16} cm$^{-3}\leq N_d\leq 1\times10^{17}$ cm^{-3}) and mobilities of 2500–3000 cm^2/V s at room temperature. We believe the high backgrounds are due to impurity incorporation from the trimethylarsenic, as has been reported by others.[3] Trimethylarsenic was selected on the basis of safety; it is known that arsine produces much higher purity films.

Our reactor design is shown in Fig. 1. Since layer switching is now done thermally, it is possible to use a simplified gas control system. The wafer sits on a thin (20 mil) graphite susceptor heated from the underside by a bank of high power tungsten halogen lamps, as in a rapid thermal annealer. Temperature is measured with a thermocouple inserted down a 2-mm-o.d. sealed quartz tube in contact with the susceptor. For initial calibration an additional thermocouple is welded to the sample[4] and the relationship between the wafer temperature and the inserted thermocouple is established. The graphite susceptor is used for temperature measurement only; we believe that supporting the sample on quartz pins alone and measuring temperature with an optical pyrometer would improve this technique by reducing thermal rise and fall times.

In rapid thermal MOCVD gas flows are initiated and stabilized while the wafer is cool. The growth of epitaxial layers is initiated by pulsing the lamps and bringing the wafer rapidly to growth temperature. At the end of each layer the lamps are shut off, the wafer cools rapidly toward room temperature, and the reaction is halted. The cooling rate is

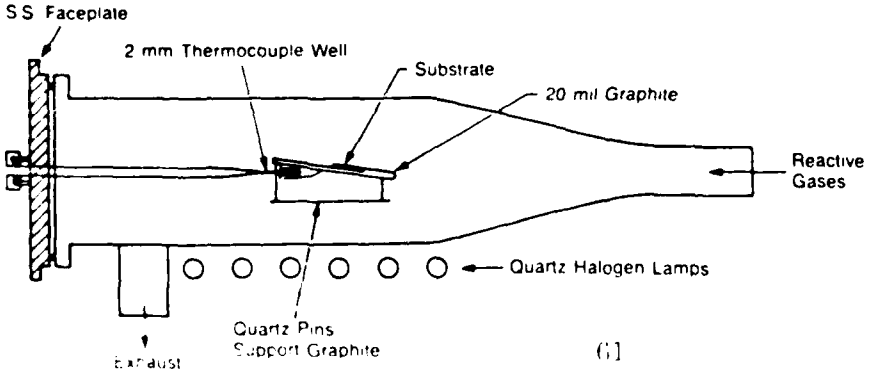


FIG. 1. Schematic drawing of the quartz reaction chamber used in our experiments. The wafer sits on a low thermal mass graphite susceptor and temperature is monitored by a thermocouple sheathed in a 2-mm-o.d. quartz tube.

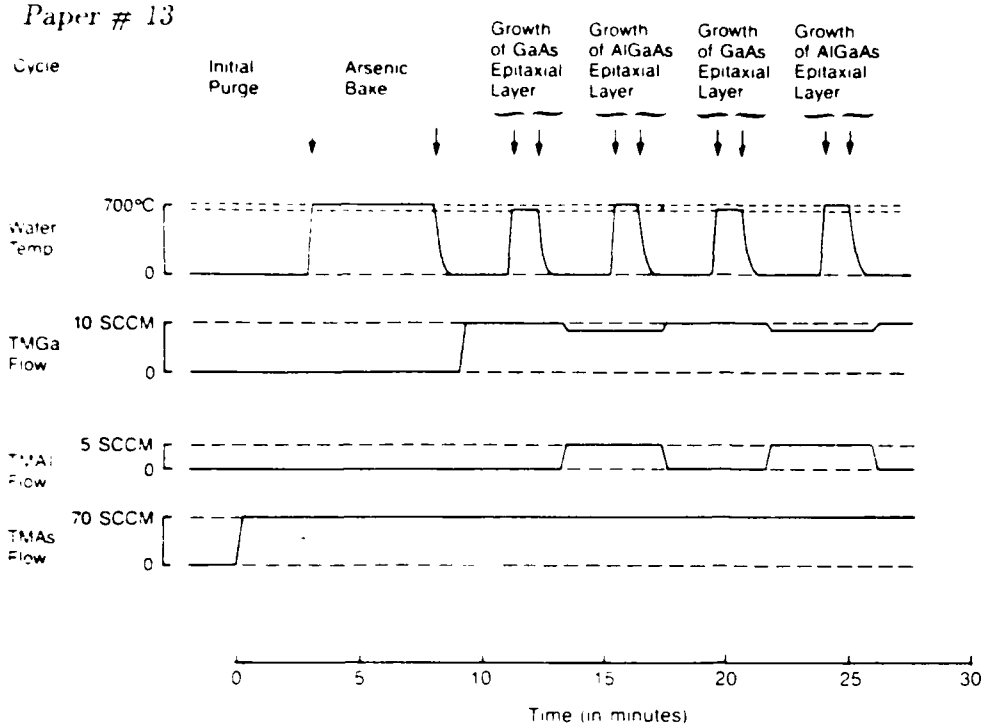


FIG. 2. LRP process timing diagram showing how layers are grown by pulsing the wafer temperature in the presence of the correct reactive gases.

enhanced by cooling the walls of the quartz reaction chamber with a high flow of compressed air, switched on at the termination of layer growth. Heat conducts rapidly away from the wafer through the hydrogen carrier gas. Rise and fall times are on the order of 10 s. Any desired structure may be grown by a sequence of these steps, as shown in Fig. 2 for a GaAs/$Al_xGa_{1-x}As$ multilayer structure. Note that the GaAs is grown at 670 °C and the AlGaAs at 720 °C. We found these temperatures gave the best mobility and surface morphology for single layers of each material.

One of our early concerns was that poor material would be grown during the cool down period, creating defects in the growth of subsequent layers. Test structures consisting of multiple layers of GaAs or alternating layers of GaAs/AlGaAs (3–11 layers, 500–2500 Å layer thickness) have been grown by a sequence of rapid thermal cycles. These structures have excellent surface morphology and electrical characteristics, equivalent to single layers grown by conventional MOCVD in our reactor. Such test structures have been analyzed by Rutherford backscattering and ion channeling, showing no evidence of crystal defects at the interfaces. Minimum yields are about 4.0%, the same as bare GaAs wafers. Rutherford backscattering detects only gross crystal defects; more sensitive tests of interface quality are in progress, including device fabrication and high resolution transmission electron microscopy.

An Auger depth profile of a GaAs/$Al_{0.12}Ga_{0.88}As$ multilayer structure grown by this technique is shown in Fig. 3. Layers are abrupt to within the resolution of Auger (50–60 Å). The total thickness of this structure is about 6000 Å. Because gases are completely purged between layers, we believe this technique is capable of atomically abrupt interfaces.

In conclusion, we have demonstrated rapid thermal MOCVD by growing multiple layers of high quality III-V compound semiconductors. These layers exhibit electrical characteristics and surface morphology equivalent to layers produced by traditional MOCVD in our reactor. The rapid thermal MOCVD technique promises abrupt interfaces and thin layers combined with high growth rates.

We would like to acknowledge the technical assistance of K. E. Williams and helpful discussions with D. Houng of Hewlett-Packard Laboratories, C. P. Kuo of Hewlett-Packard Optoelectronics Division, and H. Beneking of Aachen

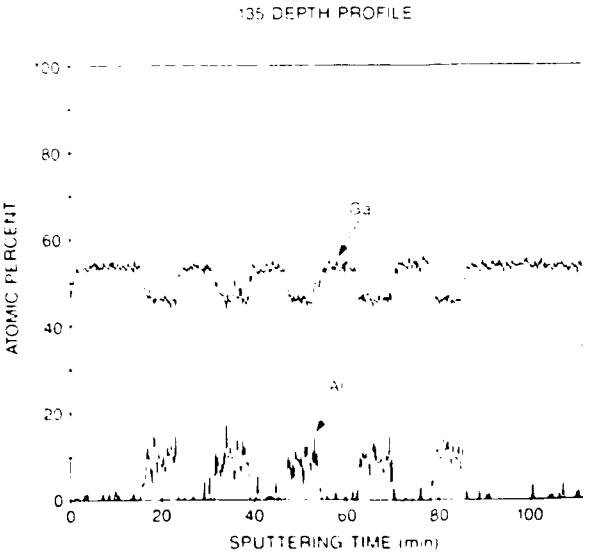


FIG. 3. Sputtering Auger profile for sample 135 showing a structure of alternating GaAs/$Al_{0.3}Ga_{0.7}As$ layers. Total thickness is about 6000 Å. Aluminum scaled by 2. (Charles Evans and Associates, Redwood City, CA.)

Technical Institute, Aachen, West Germany. We also acknowledge the support of J. Zavada and D. A. Reynolds at Defense Advanced Research Projects Agency (contracts DAAG29-85-K-0054 and DAAG29-85-K-0237). S. Reynolds acknowledges the support of an Office of Naval Research fellowship.

J. F. Gibbons, C. M. Gronet, and K. E. Williams, Appl. Phys. Lett. 47, 7. (1985).
C. M. Gronet, J. C. Sturm, K. E. Williams, J. F. Gibbons, and S. D. Wilson, Appl. Phys. Lett. 48, 1012 (1986).
C. A. Tromson, P. Gibart, R. Drunhe, Y. Monteil, J. Bouix, and G. Vi[illegible], Jam. Rev. Phys. Appl. (France) 20, 569 (1985).
J. L. Hoyt and J. F. Gibbons, Mater. Res. Soc. Symp. Proc. 52, 15[illegible]

Growth of GaAs by metalorganic chemical vapor deposition using thermally decomposed trimethylarsenic

D. W. Vook, S. Reynolds, and J. F. Gibbons
Stanford University Electronics Laboratories, McCullough 226, Stanford, California 94305

(Received 12 January 1987; accepted for publication 13 March 1987)

We have developed a novel thermal precracking technique which has improved the electrical quality of GaAs grown using trimethylarsenic, while maintaining excellent surface morphology. Background doping is reduced by a factor of 5, and carbon incorporation is reduced by a factor of 10 or more. This method may prove useful for reducing carbon incorporation from other organometallic arsenic sources as well. Net background doping below 10^{16} cm^{-3} and room-temperature electron mobilities of 4000–4500 cm^2/V s have been obtained. These are the best values reported for GaAs grown using trimethylarsenic.

One of the principal disadvantages of using metalorganic chemical vapor deposition (MOCVD) to deposit GaAs is the need to handle toxic arsine gas. Liquid organometallic sources for arsenic, less toxic than arsine, have been available for several years. Unfortunately, GaAs grown with these sources has had relatively high background doping.[1] We present a method using thermal precracking to improve the electrical quality of GaAs grown with trimethylarsenic (TMAs). We believe this technique will be applicable to other organometallic arsenic sources as well.

This study was undertaken because of our reluctance to use arsine gas in the laboratory. TMAs was selected as a readily available alternative, but we were unable to grow sufficiently pure GaAs for our purposes. Secondary ion mass spectrometry (SIMS) of GaAs grown using TMAs revealed a chemical concentration of carbon exceeding 10^{17} cm^{-3}, with no other *p*-type dopants present (Si and S contents were also high). Presuming that some of the carbon came from methyl groups on the TMAs, we sought to reduce it by precracking the TMAs.

A schematic drawing of our apparatus with the precracking chamber is shown in Fig. 1. The reactor is heated using unfocused tungsten halogen lamps, so that the entire chamber is flooded with intense infrared and visible light. This minimizes condensation of elemental arsenic on the cool quartz walls. TMAs and trimethylgallium (TMGa) are injected into the chamber through separate ports, preventing upstream GaAs deposition. TMAs with hydrogen carrier gas flows in a convoluted path through a set of graphite baffles before mixing with TMGa in a cool section of the reactor. The temperature of the precracking chamber is 800–900 °C. The sample sits on a graphite susceptor and the temperature is controlled within ± 2 °C.

Undoped (100) GaAs wafers were degreased and etched in 5:1:1 H_2SO_4:H_2O_2:H_2O prior to loading. All samples were annealed for 5 min at 700 °C in flowing TMAs immediately prior to growth. Epitaxial layers were grown at atmospheric pressure with 3.5 l/min of total H_2 flow in a 40-mm-diam reaction tube. Temperatures ranged from 600 to 700 °C, with a growth rate of 2.5 μm/h. Layer thicknesses ranged from 0.6 to 3.0 μm.

The samples were smooth, specular, and featureless when viewed under our Nomarski microscope. Layers grown at 600 °C using the thermal precracker showed pyramidal hillocks, with increasing density for higher TMAs flows. There were virtually no visible defects over the temperature range from 625 to 700 °C at V/III ratios of 6 or less. Higher V/III ratios were not tried and would probably not be advantageous because of the increased deposition of arsenic on the reactor walls.

Two different lots of TMAs were used in this study, both purchased from Alfa Products (Danvers, MA). The manufacturer's analysis of lot AP-1 indicated 3 ppm Si, along with S, Se, and Ge present. Lot AP-2 was much cleaner, with impurities below detectability. Layers grown without the precracker using lot AP-1 had *n*-type background doping of 5×10^{17}–2×10^{17} cm^{-3} and mobilities up to 3000 cm^2/V s, as shown in Fig. 2. Lot AP-2 produced layers with *p*-type backgrounds of 3×10^{16}–5×10^{16} cm^{-3}. Using the thermal precracker, optimum layers were grown at lower temperatures with a lower V/III ratio, as shown in Fig. 2. We observed a significant increase in electron mobility and a decrease in background doping. Both lots of TMAs now produced *n*-type material. With an optimum V/III ratio between 1.5 and 3 and a growth temperature of 650 °C, electron mobilities were 4000–4500 cm^2/V s and background doping was about 10^{16} cm^{-3} (using lot AP-2).

Background doping with the thermal precracker was found to be very nearly proportional to the TMAs flow (see Fig. 3). This suggests that the *n*-type background is due to impurities originating in the TMAs source. The background doping had a weak temperature dependence, increasing

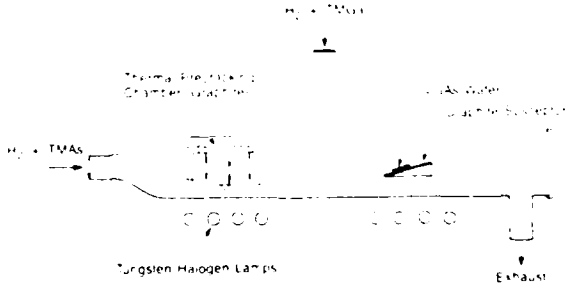


FIG. 1. Schematic drawing of the reactor, including the thermal precracking chamber. TMAs and TMGa, each in H_2 carrier gas, are injected through separate ports and mix in a cool area of the reactor.

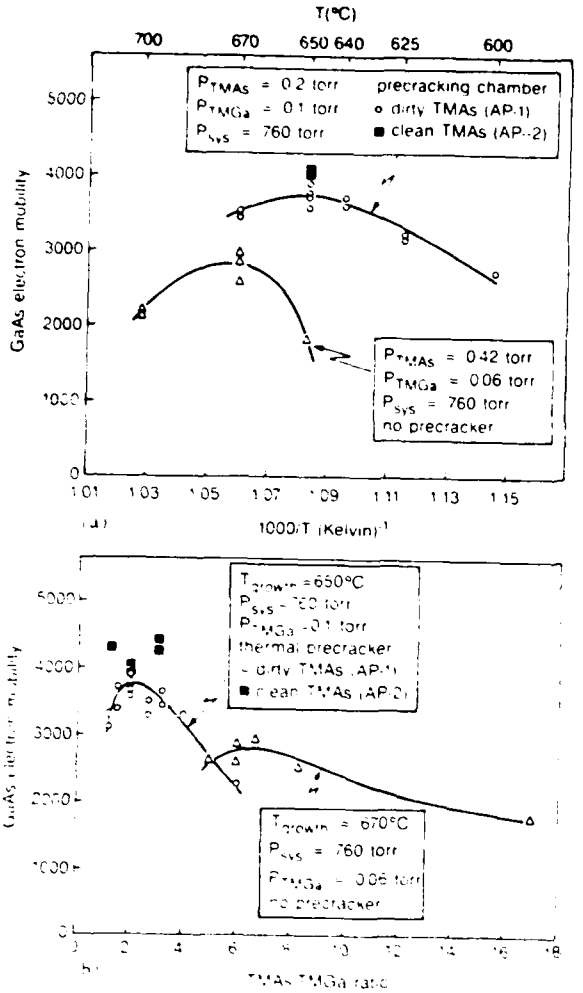


FIG. 2. GaAs electron mobility as a function of (a) growth temperature and (b) TMAs/TMGa ratio. With no precracker, using hot AP-1 (premium) layers were grown at 670 °C with TMAs/TMGa = 0.5. With the precracker, the best layers were grown at 650 °C with TMAs/TMGa between 1.5 and 3. In all cases, the growth rate was 2.5 μm/h.

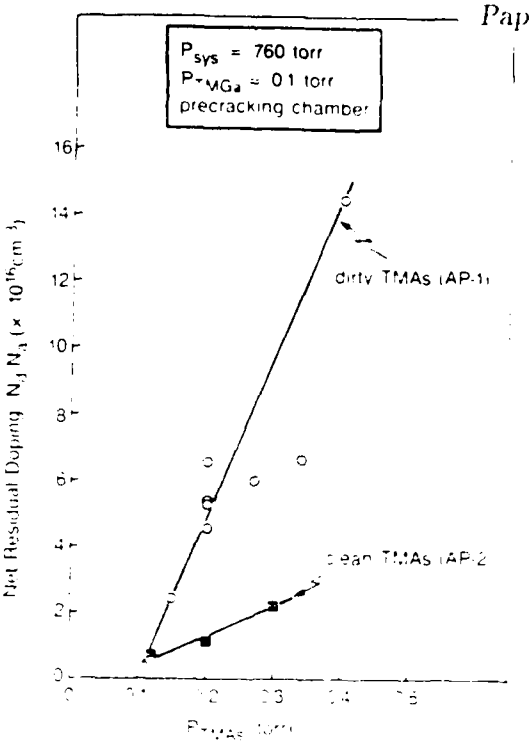


FIG. 3. Net residual doping as a function of TMAs partial pressure for two different lots of TMAs. In both cases, background doping increases linearly with the TMAs flow.

slightly with higher growth temperatures. A drop in the net background doping (from $N_a \simeq 5 \cdot 10^{16}$ cm^{-3} to $N_a \simeq 1 \cdot 10^{16}$ cm^{-3} using AP-2) combined with increased mobility when the thermal precracker is used indicates a reduction in electrically active carbon. Unfortunately, measured 77 K mobilities of about 7000 cm^2/V s show that the material is still compensated.[3]

SIMS results on samples grown with the precracker show carbon incorporation reduced below the SIMS background level ($5 \cdot 10^{16}$ cm^{-3}). Si is present at about 10^{16} cm^{-3} and S at about $5 \cdot 10^{15}$ cm^{-3}.

We suspect that the convoluted design of the precracker and the high temperatures employed fully decompose the TMAs, yielding As_4 at the exit of the precracking chamber. Unlighted areas of the reactor downstream of the precracking chamber receive heavy arsenic deposition. One would then expect our results to be similar to those of Bhat,[4] who used a solid As source to grow GaAs by MOCVD. However, Bhat observed rough surface morphology for all growth conditions, a problem we have not encountered. It appears that the use of As_4 as an active species does not alone contribute to poor surface morphology. In Bhat's reactor it was necessary to heat the upstream walls of the chamber to prevent As_4 condensation. The hot chamber walls may have caused prenucleation of GaAs.

In conclusion, we have used thermal precracking to improve the electrical quality of GaAs grown using TMAs. Because background doping is still proportional to TMAs flow, this background might be improved by further purification of the TMAs, but only to a point. Mobility measurements at 77 K indicate a high degree of compensation, implying that carbon incorporation is still too high. It appears that lack of active H in the As species used for growth increases C incorporation, in agreement with the model of Kuech and Veuhoff.[5] The thermal precracking technique may prove generally useful for other organometallic arsenic sources, such as diethylarsine, if it allowed C chains to be selectively removed from the precursor molecule.

We would like to acknowledge the support of J. Zavada at the Army Research Office and D. A. Reynolds at the Defense Advanced Research Projects Agency (contracts DAAG29-85-K-0054 and DAAG20-85-K-0237). S. Reynolds acknowledges the support of an Office of Naval Research Fellowship.

[1] C. A. Tromson, P. Gibart, R. Druilhe, Y. Monteil, J. Bouix, and B. El Jani, Rev. Phys. Appl. (France) **20**, 569 (1985).
[2] W. T. Dietze, M. J. Ludowise, and C. B. Cooper, Electron. Lett. **17**, 698 (1981).
[3] C. M. Wolfe, G. E. Stillman, and W. T. Lindley, J. Appl. Phys. **41**, 3088 (1970).
[4] R. Bhat, J. Electron. Mater. **14**, 433 (1985).
[5] T. F. Kuech and E. Veuhoff, J. Cryst. Growth **68**, 148 (1984).

Paper # 15

LIMITED REACTION PROCESSING: GROWTH OF III-V EPITAXIAL LAYERS BY RAPID THERMAL METALORGANIC CHEMICAL VAPOR DEPOSITION

S. Reynolds, D.W. Vook, J.F. Gibbons
Stanford University Electronics Laboratories, McCullough 226, Stanford, CA 94305

ABSTRACT

Rapid thermal processing (RTP) has been applied to improve the versatility of metalorganic chemical vapor deposition (MOCVD). We have demonstrated a new pulsed growth method which yields enhanced layer thickness control and abrupt interfaces (2-4 atomic layers) while maintaining a high growth rate (10Å/sec). In this technique, substrate temperature is used as a switch to control the growth of epitaxial layers.

The unfocused tungsten halogen lamps used in RTP have also facilitated a novel thermal precracking technique, producing the best GaAs ever grown using trimethylarsenic (TMAs). Background doping is reduced by a factor of 5, and carbon incorporation is reduced by a factor of 10 or more. Net background doping below $10^{16}cm^{-3}$ and room temperature electron mobilities of 4000 to 4500 $cm^2/V \cdot sec$ have been obtained.

INTRODUCTION

Limited Reaction Processing (LRP), developed by J.F.Gibbons *et. al.* [1-3], uses rapid precise changes in substrate temperature as a switch to control layer growth, rather than utilizing gas phase switching. It was first applied to produce thin abrupt silicon epitaxial layers and has been extended to include Si/SiGe heterostructures. Using this technique we have produced GaAs epitaxial layers with interface abruptness comparable to MBE, and have studied the quality of these thermally interrupted growth interfaces.

During our work on the pulsed growth of GaAs, we discovered RTP technology has two advantages for III-V epitaxy; not only does the fast temperature response give an additional element of control over the process, but the unfocused lamps enable cleaner cold wall operation. These applications are discussed individually in the next two sections.

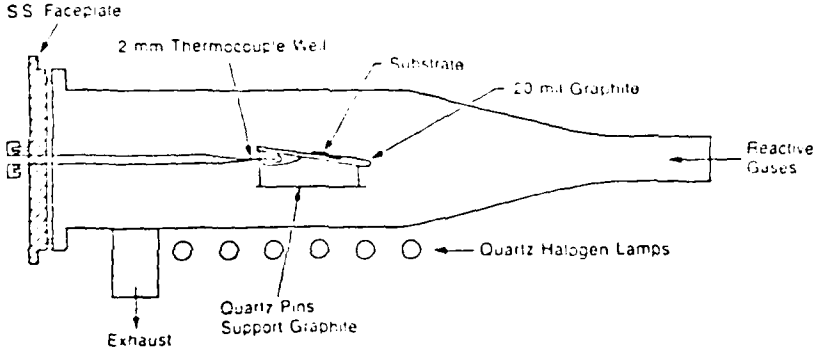


Figure 1: Schematic drawing of the quartz reaction chamber used in our experiments. The wafer sits on a low thermal mass graphite susceptor and temperature is monitored by a thermocouple sheathed in a 2 mm outer diameter quartz tube.

PULSED GROWTH OF GaAs

Our reactor design is shown in figure 1. The wafer sits on a thin (20 mil) graphite susceptor heated from the underside by a bank of high power tungsten halogen lamps, as in a rapid thermal annealer. Temperature is measured with a thermocouple inserted down a 2 mm outer diameter sealed quartz tube in contact with the susceptor. For

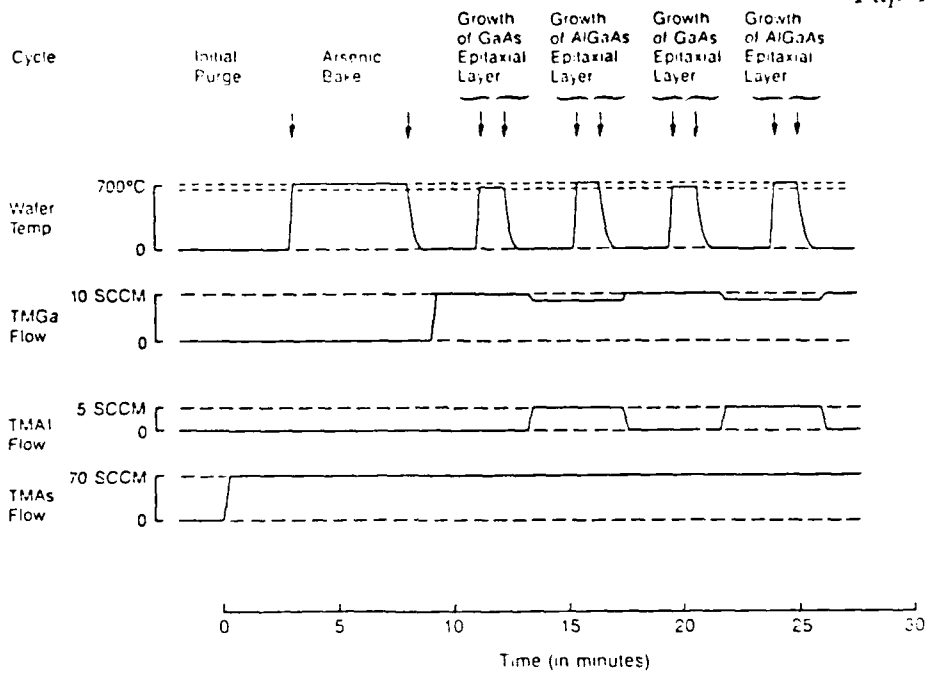


Figure 2: LRP process timing diagram showing how layers are grown by pulsing the wafer temperature in the presence of the correct reactive gases.

initial calibration an additional thermocouple is welded to the sample and the relationship between the wafer temperature and the inserted thermocouple is established. The graphite susceptor is used to measure temperature and to reduce slip.

Layers were grown using trimethylarsenic, trimethylgallium, trimethylaluminum, and trimethylindium, all purchased from Alfa Products (Danvers, Mass.). GaAs substrates, undoped and Si doped (100) Czochralski, were degreased and given a 5:1:1 H_2SO_4 : H_2O_2 : H_2O etch prior to loading. Optimum layers were grown at 670 to 720°C with 3.5 liter/min of total H_2 flow, a trimethylarsenic partial pressure of about 0.5 torr, and a growth rate of $2-3$ μm/hr. $Al_xGa_{1-x}As$ ($0 < x < 1$) layers were smooth and featureless to within the resolution of our Normarski microscope (1100X). $In_yGa_{1-y}As$ ($0 < y < .22$) layers showed a crosshatch pattern characteristic of lattice mismatched epitaxial systems. GaAs layers typically had n-type backround doping of 2×10^{16} cm$^{-3} \leq N_d \leq 1 \times 10^{17}$ cm^{-3} and mobilities of 2500 to 3000 cm^2/V $\cdot$ sec at room temperature, although the background doping varied with TMAs source. We believe the high backrounds are due to impurity incorporation from the trimethylarsenic, as has been reported by others [4,7]. Trimethylarsenic was selected on the basis of safety; arsine is known to produce much higher purity films.

In rapid thermal MOCVD gas flows are initiated and stabilized while the wafer is cool. The growth of epitaxial layers is initiated by pulsing the lamps and bringing the wafer rapidly to growth temperature. At the end of each layer the lamps are shut off, the wafer cools rapidly toward room temperature, and the reaction is halted. The cooling rate is enhanced by cooling the walls of the quartz reaction chamber with a high flow of compressed air, switched on at the termination of layer growth. Heat conducts rapidly away from the wafer through the hydrogen carrier gas. Rise and fall times are on the order of ten seconds. Any desired structure may be grown by a sequence of these steps, as shown in figure 2 for a GaAs/$Al_xGa_{1-x}As$ multilayer structure. Note that the GaAs is grown at 670°C and the AlGaAs at 720°C. We found these temperatures gave the best mobility and surface morphology for single layers of each material.

One of our early concerns was that poor material would be grown during the cool down period, creating defects in the growth of subsequent layers. Test structures consisting of multiple layers of GaAs or alternating layers of GaAs/$Al_xGa_{1-x}As$ (3 to 11 layers, 500 Å to 2500 Å layer thickness) have been grown by a sequence of rapid thermal cycles.

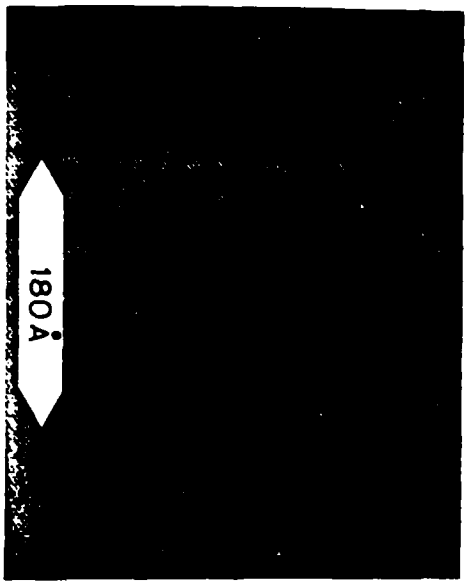


Figure 3: High resolution TEM image of an AlAs-GaAs superlattice. The light layers are AlAs, estimated to be 180Å thick.

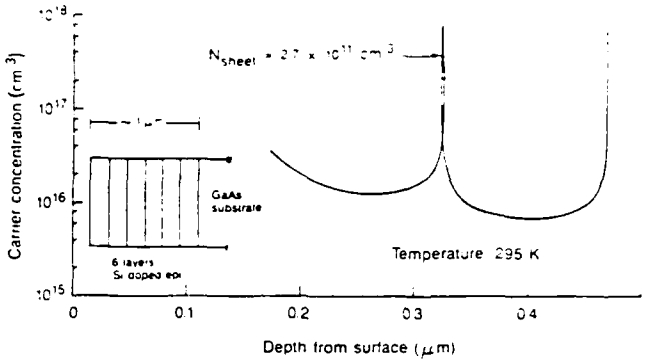


Figure 4: Carrier concentration versus depth for a multiple layer GaAs structure, extracted from C-V measurements. This structure has a total of 6 layers, although only 2 of them appear in this plot.

These structures have excellent surface morphology, and the sheet carrier concentrations and Hall mobilities are equivalent to single layers grown by conventional MOCVD in our reactor. Such test structures have been analyzed by Rutherford backscattering and ion channeling, showing minimum yields of about 4.0%, the same as bare GaAs wafers. Within the resolution of RBS, there are no crystal defects at the interfaces.

Figure 3 shows a lattice image TEM photograph of a GaAs-AlAs superlattice. The transition between the layers occurs within 2 to 4 atomic planes, making the abruptness of this structure equivalent to MBE grown material. Because gases are completely purged between successive layers, we believe that this technique is capable of atomically abrupt interfaces. There are defects present at one interface which we speculate to be oxide inclusions in the AlAs (pure AlAs is very oxygen reactive). The interface at which AlAs is grown on GaAs does not display such defects. These defects are probably not inherent to the pulsed growth process.

We have also made capacitance voltage (C-V) measurements on multiple layer structures of GaAs, by reverse biasing a Schottky diode fabricated on the surface. These layers were grown by flowing TMAs, TMGa, and SiH_4 continuously, but pulsing the lamps through 6 cycles to grow 6 individual layers. Figure 4 is a plot of carrier concentration versus depth extracted from these measurements, revealing large peaks in carrier concentration at regular depths from the surface. The peaks correspond to a sheet carrier density of about $2.7 \times 10^{11}\text{cm}^{-2}$. However, it is not clear whether these peaks are a true profile caused by a sheet of shallow donors (Si pile up at each interface) or a measurement artifact caused by the release of electrons from deep interface states. Similar C-V profiles have been observed for growth interrupted interfaces in MBE [5,6]. We will perform depth profiling by Secondary Ion Mass Spectrometry (SIMS) to see if there are interface impurity peaks corresponding to the C-V peaks. This should distinguish impurity pile up from deep interface states.

These preliminary C-V results indicate that our pulsed growth technique for GaAs generates electrically active interface states or dopant pile up, which may be dependent on the growth conditions. We are planning experiments to explore the effect of thermal ramp times on interface quality. Since other paused growth techniques in MBE and MOCVD have been observed to generate interface states, this may be a general characteristic of the GaAs system.

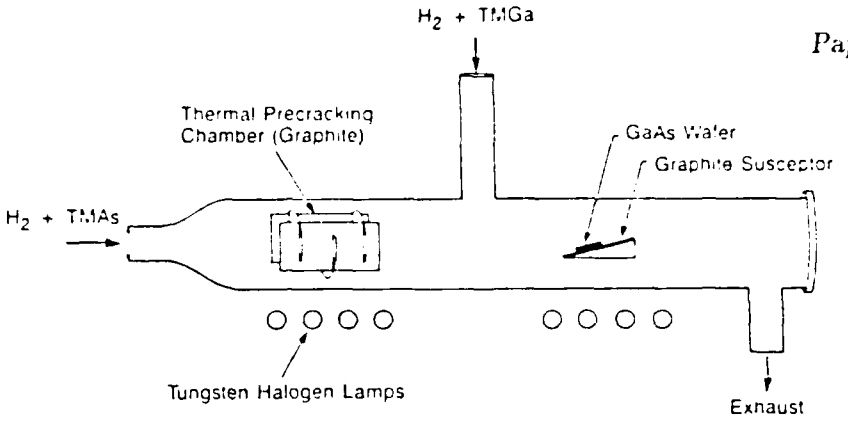


Figure 5: Schematic drawing of the modified reactor, including the thermal precracking chamber. TMAs and TMGa, each in H_2 carrier gas, are injected through separate ports and mix in a cool area of the reactor.

THERMAL DECOMPOSITION OF TRIMETHYLARSENIC

With minor modification to our lamp heated reactor, we have developed a novel thermal precracking technique which has improved the electrical quality of GaAs grown with TMAs. Excellent surface morphology is maintained, while background doping is reduced by a factor of 5, and carbon incorporation is reduced by a factor of 10 or more. Net background doping below $10^{16}cm^{-3}$ and room temperature electron mobilities of 4000 to 4500 $cm^2/v \cdot sec$ have been obtained. These are the best values reported for GaAs using trimethylarsenic.

This study was undertaken because of our reluctance to use arsine gas in the laboratory. TMAs was selected as a readily available alternative, but we were unable to grow sufficiently pure GaAs for our purposes. Other researchers using TMAs have also observed this relatively high background doping [4,7]. Secondary Ion Mass Spectrometry (SIMS) of GaAs grown using TMAs revealed a chemical concentration of carbon exceeding $10^{18}cm^{-3}$, with no other p-type dopants present (Si and S content were also high). Presuming that some of the carbon came from methyl groups on the TMAs, we sought to reduce it by precracking the TMAs.

A schematic drawing of our modified apparatus with the precracking chamber is shown in figure 5. The reactor is heated using unfocused tungsten halogen lamps, so that the entire chamber is flooded with intense infrared and visible light. This minimizes condensation of elemental arsenic on the cool quartz walls. TMAs and trimethylgallium (TMGa) are injected into the chamber through separate ports, preventing upstream GaAs deposition. TMAs with hydrogen carrier gas flows in a convoluted path through a set of graphite baffles before mixing with TMGa in a cool section of the reactor. The temperature of the precracking chamber is 800 to 900°C. The sample sits on a graphite susceptor and the temperature is controlled within ±2°C.

GaAs wafers (100) were cleaned as before, loaded, and then annealed for 5 minutes at 700°C in flowing TMAs immediately prior to growth. In these experiments the growth of epitaxial layers was begun by introducing TMGa flow, as in conventional MOCVD. Growth temperatures ranged from 600 to 700°C. The surfaces were smooth, specular, and generally featureless when viewed under our Normarski microscope. Layers grown at 600°C using the thermal precracker showed pyramidal hillocks, with increasing density for higher TMAs flows. There were virtually no visible defects over the temperature range from 625 to 700°C at V/III ratios of 6 or less. Higher V/III ratios were not tried and would probably not be advantageous because of the increased deposition of arsenic on the reactor walls.

Two different lots of TMAs were used in this study, both purchased from Alfa Products (Danvers, Mass.). The manufacturer's analysis of lot AP-1 indicated 3 ppm Si, along with S, Se, and Ge present. Lot AP-2 was much cleaner, with impurities below detectability. Layers grown without the precracker using lot AP-1 had n-type back-

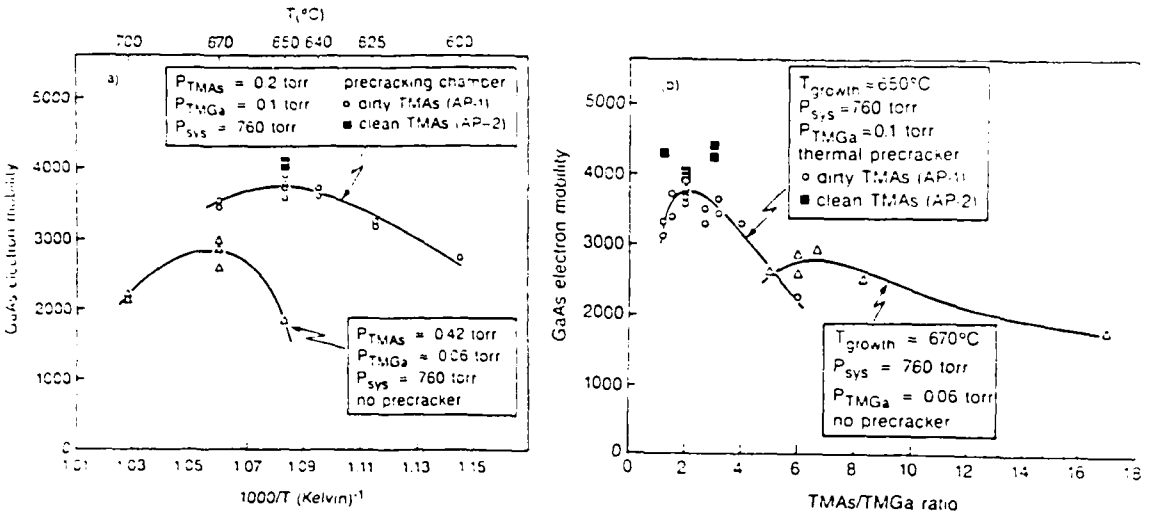


Figure 6: GaAs electron mobility as a function of (a) growth temperature and (b) TMAs/TMGa ratio. With no precracker, using lot AP-1, optimum layers were grown at 670°C with TMAs/TMGa $\approx$ 6.5. With the precracker, the best layers were grown at 650°C with TMAs/TMGa between 1.5 and 3. In all cases, the growth rate was 2.5 μm/hr.

ground doping of 5×10^{16}cm^{-3} to 2×10^{17}cm^{-3} and mobilities up to 3000 cm^2/V $\cdot$ sec, as shown in figure 6. Lot AP-2 produced layers with p-type backgrounds of 3×10^{16}cm^{-3} to 5×10^{16}cm^{-3}. Using the thermal precracker, optimum layers were grown at lower temperatures with a lower V/III ratio, as shown in figure 6. We observed a significant increase in electron mobility and a decrease in background doping. Both lots of TMAs now produced n-type material. With an optimum V/III ratio between 1.5 and 3 and a growth temperature of 650°C, electron mobilities were 4000 to 4500 cm^2/V $\cdot$ sec and background doping was about 10^{16}cm^{-3} (using lot AP-2).

Background doping with the thermal precracker was found to be very nearly proportional to the TMAs flow (see figure 7). This suggests that the n-type background is due to impurities originating in the TMAs source. The background doping had a weak temperature dependence, increasing slightly with higher growth temperatures. A drop in the net background doping (from $N_a \approx 5 \times 10^{16}$cm^{-3} to $N_d \approx 1 \times 10^{16}$cm^{-3} using AP-2) combined with increased mobility when the thermal precracker is used indicates a reduction in electrically active carbon. Unfortunately, measured 77K mobilities of about 7000 cm^2/V $\cdot$ sec (on 3 μm thick layers) suggest that the material is still compensated [8].

SIMS results on samples grown with the precracker show carbon incorporation reduced below the SIMS background level (5×10^{16}cm^{-3}). Si is present at about 10^{16}cm^{-3} and S at about 5×10^{15}cm^{-3}.

We suspect that the convoluted design of the precracker and the high temperatures employed fully decompose the TMAs, yielding As_4 at the exit of the precracking chamber. Unlighted areas of the reactor downstream of the precracking chamber receive heavy arsenic deposition. One would then expect our results to be similar to those of Bhat [9], who used a solid As source to grow GaAs by MOCVD. However, Bhat observed rough surface morphology for all growth conditions, a problem we have not encountered. It appears that the use of As_4 as an active species does not alone contribute to poor surface morphology. In Bhat's reactor it was necessary to heat the upstream walls of the chamber to prevent As_4 condensation. The hot chamber walls may have caused pre-nucleation of GaAs.

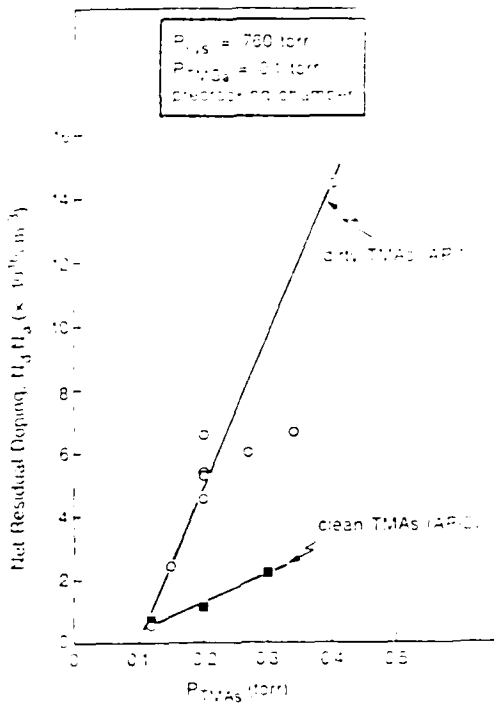


Figure 7: Net residual doping as a function of TMAs partial pressure, for two different lots of TMAs. In both cases, background doping increases linearly with the TMAs flow.

SUMMARY

We have applied rapid thermal processing to improve the versatility of conventional MOCVD. Multiple layers of high quality III-V compound semiconductors have been grown using a thermally pulsed growth technique (LRP). These layers have surface morphology and Hall mobility equivalent to layers produced by conventional MOCVD in our reactor. Abrupt interfaces, with transition widths of 2 to 4 atomic layers, have been obtained at atmospheric pressure using high growth rates (3μm/hr $\approx$ 10Å/sec). There remain potential problems with interface state density which we are investigating.

The unfocused tungsten halogen lamps have also facilitated a novel thermal precracking technique, producing the best GaAs ever grown using trimethylarsenic (TMAs). Background doping and carbon incorporation are substantially reduced, and room temperature electron mobilities up to 4500 $cm^2/V \cdot sec$ are obtained. This material is still not equivalent to that grown using AsH_3, but the technique is promising for use at low pressure or with other organometallic arsenic sources.

We would like to acknowledge the support of J. Zavada at the Army Research Office and D.A. Reynolds at the Defense Advanced Research Projects Agency. S. Reynolds acknowledges the support of an Office of Naval Research Fellowship.

REFERENCES

1. J.F. Gibbons, C.M. Gronet, and K.E. Williams, Appl. Phys. Lett. **47**, 721 (1985).
2. C.M. Gronet, J.C. Sturm, K.E. Williams, J.F. Gibbons, S.D. Wilson, Appl. Phys. Lett. **48**, 1012 (1986).
3. C.M.Gronet *et. al.*, J.Appl. Phys. **61**, (6) 15 March (1987)
4. C.A. Tromson, P. Gibart, R. Druilhe, Y. Monteil, J. Bouix and B. El Jani, Rev. Phys. Appl. (France) **20** no.8 p.569-574 Aug. (1985).
5. Y.Iimura, T.Shiraishi, H.Takasugi, M.Kawabe, J. Appl. Phys. **61**(5), p.2095 (1987)
6. A. Takamori, E. Miyauchi, H. Arimoto, Y. Bawba, T. Monta, H. Hashimoto, Japan J. Appl. Phys. **24**(6), p.1414 (1985)
7. W.T. Dietze, M.J. Ludowise, C.B. Cooper, Electronics Lett. **17**, 698 (1981).
8. C.M. Wolfe, G.E. Stillman, and W.T. Lindley, J. Appl. Phys. **41**, 3088 (1970).
9. R. Bhat, J. Electronic Materials **14**, 433 (1985).

JAMES F. GIBBONS*, S. REYNOLDS*, C. GRONET*, D. VOOK*, C. KING*, W. OPYD*, S. WILSON+, C. NAUKA++, G. REID++, R. HULL++.

*Stanford Electronics Laboratories, Stanford, CA 94305
+Charles Evans & Associates, Redwood City, CA 94063
++Hewlett-Packard Materials Characterization Laboratory, Palo Alto, CA 94304

ABSTRACT

Limited Reaction Processing (LRP) is a new technique which combines Rapid Thermal Processing (RTP) and Chemical Vapor Deposition (CVD). The added temperature control provided in rapid thermal processing enables the use of substrate temperature as a reaction switch. In addition, rapid thermal technology has been shown to provide other advantages for chemical vapor deposition of Si and III-V materials. Results are presented for group IV materials including epitaxial Si, SiGe alloys, SiO_2, and polysilicon. MOSFETs have been demonstrated and sensitive tests of interface quality are presented, paving the way for future bipolar transistor fabrication. III-V materials such as GaAs, AlGaAs, InGaAs have been grown. GaAs electron mobilities are the best reported for material grown using trimethylarsenic. As-ambient rapid thermal anneals of GaAs have also been performed.

INTRODUCTION

For a variety of device applications, it is becoming desirable to grow thinner, more abrupt layers of semiconductors and insulators. Future devices will require cleaner interfaces and fewer particles. We especially want the epitaxial layers to be of good quality, with the highest possible carrier lifetime and mobility. LRP is an improvement over conventional CVD because it provides an additional element of control over the process. Rapid changes in substrate temperature can be made if needed. Temperature is actually used as the reaction switch in all the silicon work and much of the III-V work. Thermal exposure of the substrate can be reduced, and multiple layers of different materials can be grown in the same chamber.

Group IV Materials

Over the past two years, limited reaction processing has been used to grow group IV structures with three primary advantages:

1. minimum thermal exposure of the substrate (abrupt interfaces)
2. ultrathin layer capability (100 Å)
3. in-situ multilayer processing for high purity interfaces

Many test and device structures have been grown which demonstrate these capabilities and verify intralayer and silicon/oxide interface quality [1-10]. Recently we have investigated the structure and purity of semiconductor/semiconductor interfaces. LRP inherently presents two potential problems for the growth of any multilayer structure:

- non-optimum deposition during the thermal transients
- contamination at the interrupted growth interface

For example, during the deposition of an LRP epitaxial Si layer, some amorphous or polycrystalline material may deposit on the substrate during

the initial thermal transient, potentially nucleating defects. Deposition during the cooling transient may disrupt the crystalline template for the growth of a subsequent epitaxial layer. In addition, an inherent part of any LRP multilayer structure is an interrupted growth interface. The wafer is cooled after the first layer growth, gases are purged out of the chamber, and then the gases for the next layer are introduced. During this gas switching stage, the cool, bare silicon surface may getter impurities from the gas stream which could nucleate defects in the next layer. We thus investigated the purity and structure of the interrupted growth interface.

Structure

The structure of LRP semiconductor interfaces can be viewed directly using high magnification cross-section TEM. Si/SiGe superlattices are convenient to analyze because the contrast between the layers provides an interface marker. Figure 1 shows a TEM image of such an interface. The rows of dots show no distortion across the interrupted growth interface, indicating excellent atomic alignment. However, since TEM analyzes a very small portion of the sample, a more sensitive test of interface structure was conducted. Multiple layers of Si epi were grown by simply flowing a mixture of SiH_2Cl_2 in H_2 during five or more LRP

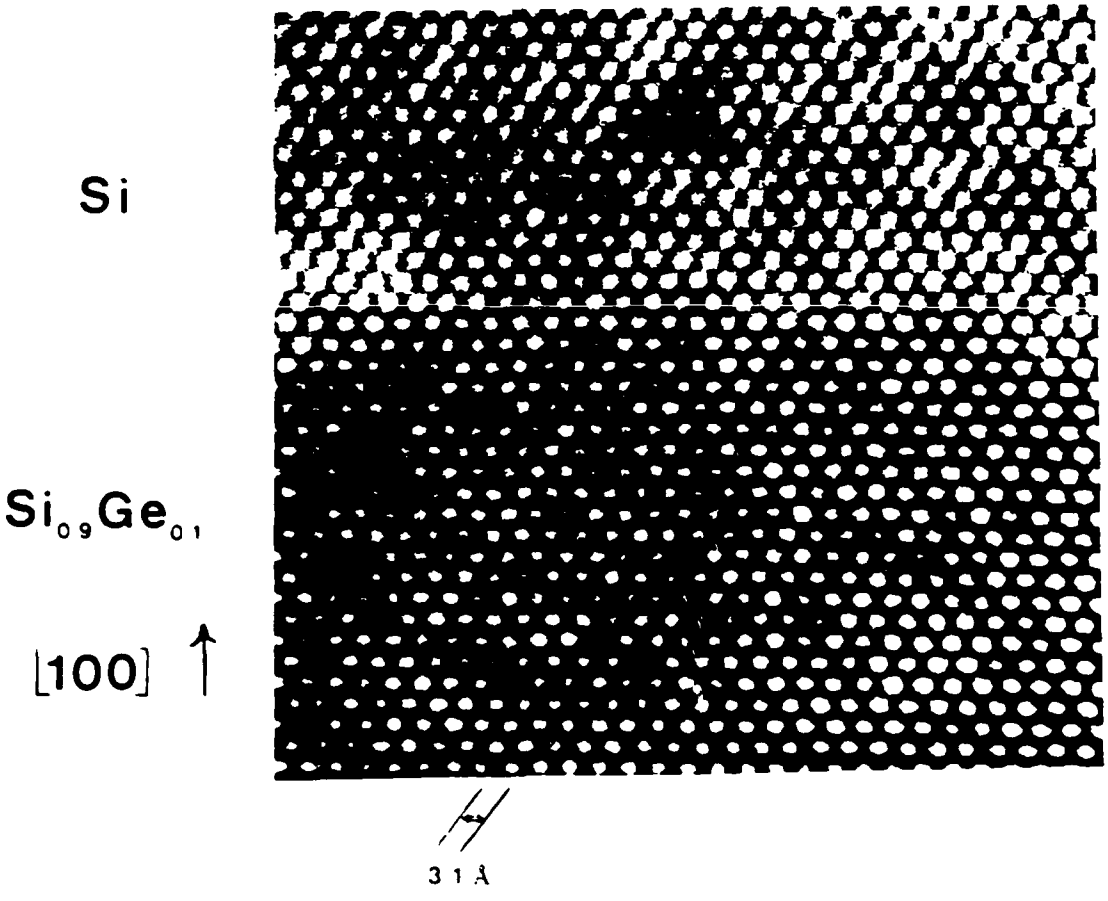


Figure 1. High magnification cross-section TEM of part of an LRP $Si/Si_{0.9}Ge_{0.1}$ superlattice. The alloy layer is commensurate and the alignment of atomic planes across the interrupted growth interface is excellent.

thermal pulses. This "multipulse" test sample was grown to provide a structure with properties dominated by the quality of the interrupted growth interface. Wright etching was performed (45-90 seconds), and the sample was analyzed for etch pits using a Nomarski microscope and an SEM. Early samples typically contained 100-1000 dislocations and hillocks per cm^2, but recently, by optimizing growth conditions and sample handling, we have grown multipulse structures which appear featureless after defect etching. Thus, using our ramp and growth rates (300-400°C/sec, 0.1-02 μm/min, respectively), the two factors which govern the amount of deposition during LRP thermal transients, we have obtained epitaxial, low-defect interrupted growth interfaces.

Purity

The multipulse test samples were also used to probe the purity of LRP interfaces. No evidence of Ca, K, Na, Al, or Cu was found to the sensitivity of SIMS analysis, about 10^{16} atoms/cm^3. Surprisingly, as shown in Figure 2, even for an interrupted growth duration of 5 minutes, SIMS revealed no interfacial carbon or oxygen contamination to a sensitivity of about $1-5x10^{17}$ atoms/cm^3 for oxygen and $5-9x10^{16}$ atoms/cm^3 for carbon. One would expect that residual oxygen and water in the gas (probably around 1 ppm) would oxidize the cool, free silicon surface which exists during the interrupted growth portion of an LRP cycle [11]. We offer three possible explanations for the SIMS data:

1. Oxide contamination exists, but it is below the SIMS detectability limit or less that the oxygen level dissolved in the silicon.
2. The oxide is desorbed during the ramp up transient for the growth of the next layer.
3. The epi gases may provide an in-situ gettering effect to drastically reduce the amount of contaminants near the wafer.

These possible explanations are under further investigation. Very recent results indicate we can obtain Si-Si and Si-SiGe interfaces with undetectable carton and oxygen for growth temperatures as low as 900°C.

DLTS was also used to analyze the multipulse samples for metallic contamination to a more sensitive level. Figure 3 shows essentially featureless DLTS spectra, indicating that less than about 10^{11} metal traps/cm^3 (hole or electron) exist within the bulk or at the interfaces of LRP Si epilayers. These results were corroborated by photocurrent decay measurements which measure the minority carrier recombination lifetime. The multipulse samples shown in Figure 3 exhibited lifetimes in the range of 30-80 μs, compared to Czochralski silicon control substrates which yielded about 10 μs using the same apparatus.

In summary, the structure and purity of LRP Si or SiGe interrupted growth interfaces appear to be excellent. Traditionally, ion implantation and diffusion have been used, in part, to bury sensitive device interfaces in bulk material where good structure and purity is usually assured. The LRP technique offers the possibility of growing multiple device interfaces, thus allowing us to use the excellent layer thickness and doping control of the technique to define device geometry and add new versatility for improving device performance.

LIMITED REACTION PROCESSING FOR III-V MATERIALS

In this section we report on the thermally switched growth of epitaxial GaAs and related compounds. We have used the technique to grow layers of $Al_xGa_{1-x}As$ ($0<x<1$) and $In_yGa_{1-y}As$ ($0<y<.22$) with good electrical characteristics and surface morphology. LRP maintains a

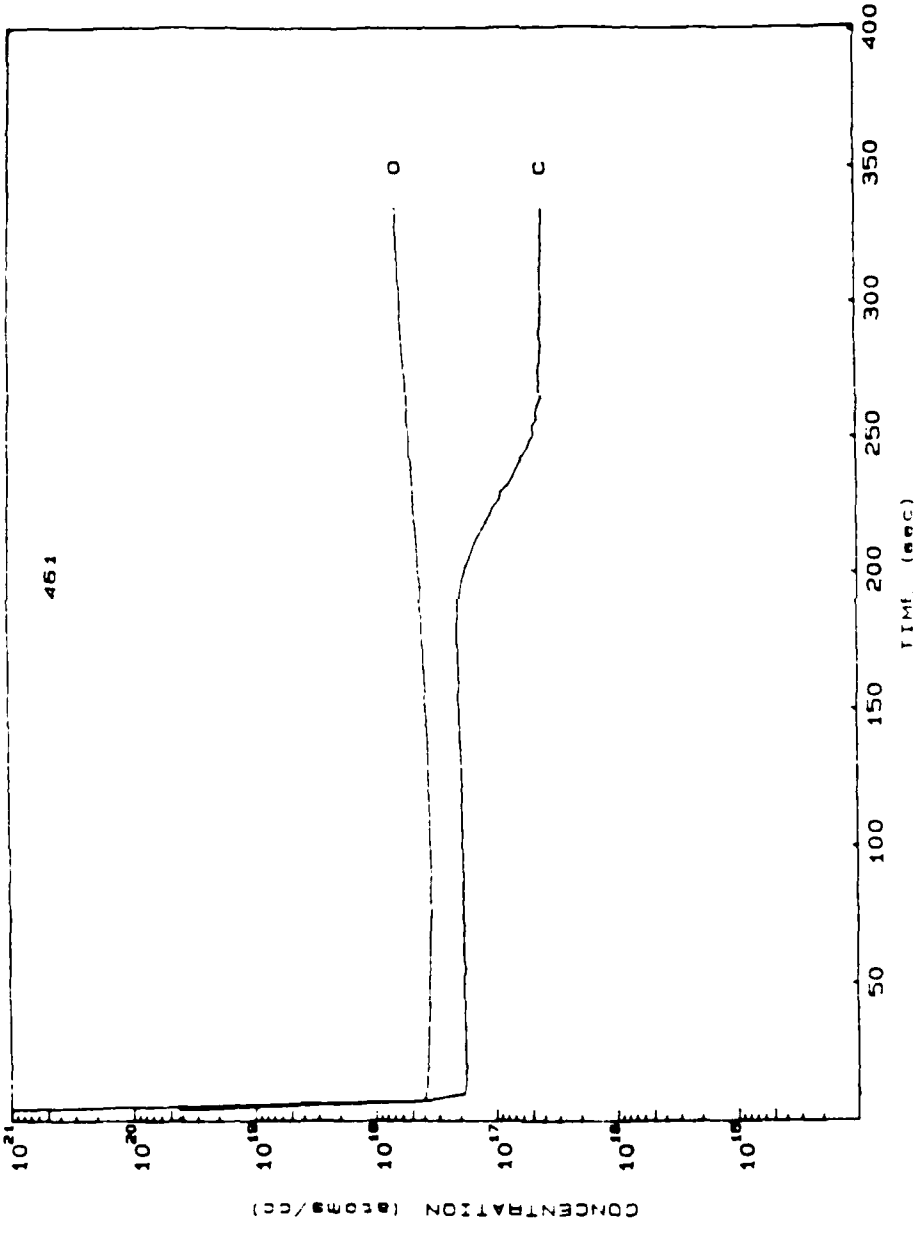
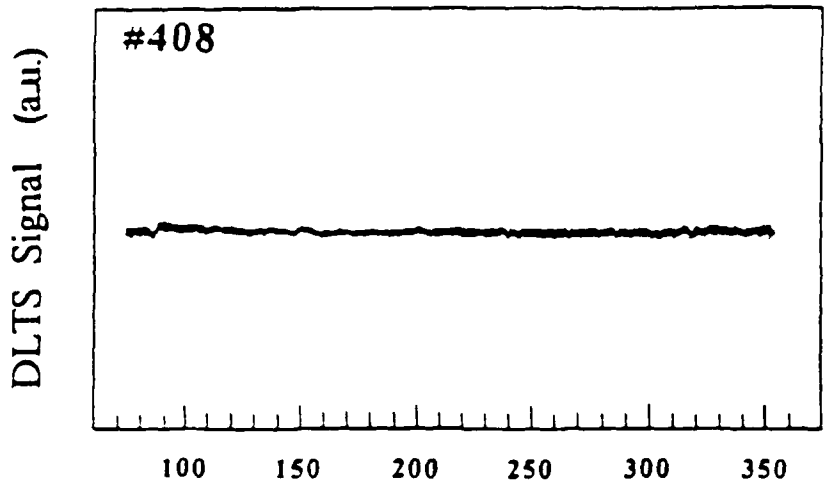


Figure 2. SIMS profile of oxygen and carbon concentration versus depth for an LRP sample containing four interrupted growth interfaces. The interrupted growth time was varied from two to five minutes. Note the absence of any C or O spikes at any of these interfaces. The carbon level in the epilayer is slightly higher than the substrate because of residual contaminants in the source gas and possible backstreaming of pump oil.

DLTS p/p+ substrate



delta DLTS < 1 x 10^{11} at/cm^3

DLTS n/n+ substrate

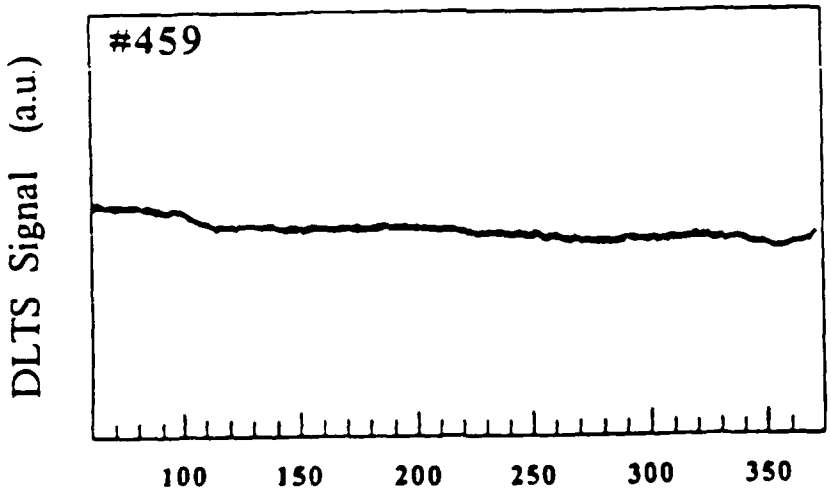


Figure 3. Deep level transient spectra of two LRP multipulse samples. The spectra are essentially featureless, indicating that the level of hole and electron traps is less than $10^{11}/cm^3$.

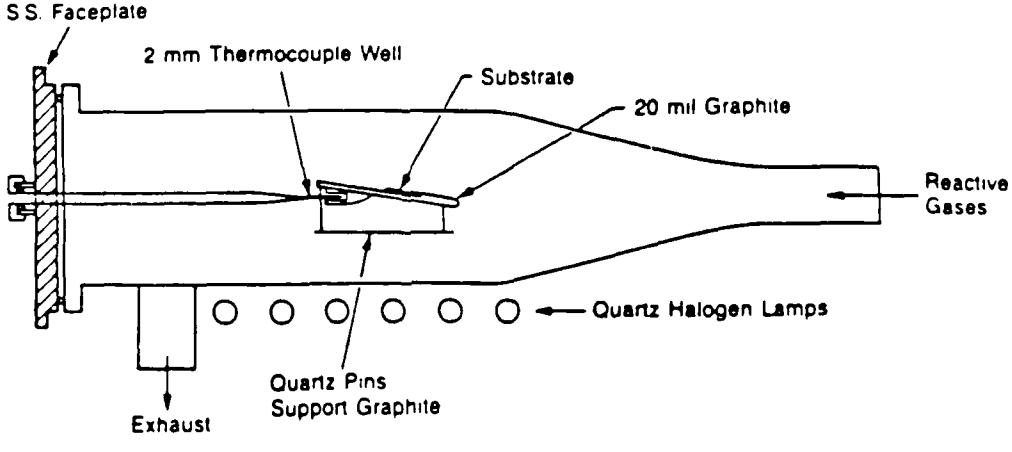
high growth rate (2-3 μm/hour) at atmospheric pressure, while producing abrupt interfaces in multilayer structures. Interface widths of 2-4 atomic layers have been measured using lattice image TEM. We have also used our reactor to perform As-ambient rapid thermal annealing, with encouraging preliminary results.

Considerations in III-V Epitaxy

The growth of GaAs has important practical differences from Si growth--differences which affect the LRP process as well as our reactor design. One difference is the need to provide an As overpressure whenever the wafer temperature is above 450°C, to prevent GaAs surface decomposition. The need for a certain minimum As pressure also sets limits on the total growth pressure. (All the work reported here is atmospheric pressure, although we have grown GaAs as low as 10 Torr.) In addition, GaAs is best grown in the mass transport limited regime, so that uniform laminar flow must be established in the reactor. These pressure and flow constraints argue for a substantially different reactor design than is used for Si work. Our design, shown in Figure 4, is similar to a conventional MOCVD reactor but has much lower thermal mass for the susceptor.

Despite operation in the mass transport regime, temperature control is important for high quality epi. Our studies show that the highest electron mobilities are obtained within a ±15°C temperature window [12]. In addition, dopant incorporation is a strong function of growth temperature. Temperature control is made difficult because As_4 and GaAs deposit on the reactor walls, attenuating or reflecting the lamp power. Closed loop temperature control with a thermocouple in the chamber (but not exposed to reactive gases) is necessary. The use of a thin graphite susceptor gives reasonably fast temperature sensing while minimizing or eliminating slip in the GaAs wafer.

One final consideration is the extreme toxicity of arsine (AsH_3), normally used for GaAs growth. For safety reasons, we are reluctant to use high concentrations of arsine gas in our laboratory. We selected trimethylarsenic (TMAs) as a substitute and are presently investigating other alternatives to arsine. Films grown with TMAs are known to be much less pure than those grown with arsine [13,14]. However, using



Schematic drawing of the quartz reaction chamber used in experiments. The wafer sits on a low thermal mass graphite and temperature is monitored by a thermocouple sheathed in outer diameter quartz tube.

a new precracking technique in our reactor, we have substantially improved the electrical quality of GaAs grown with TMAs [12]. Our electron mobilities with this technique (4000-4500 $cm^2/v.sec$) are the best reported for TMAs. This work is described in a separate paper presented in Symposium B of this conference.

Results III-V Epitaxy

Layers were grown using trimethylarsenic, trimethylgallium, trimethylaluminum, and trimethylindium, all purchased from Alfa Products (Danvers, Ma). GaAs substrates, undoped and Si doped (100) Czochralski, were degreased and given a 5:1:1 $H_2SO_4H_2O_2:H_2O$ etch prior to loading. Optimum layers were grown at 670-720°C with 3.5 l/min of total H_2 flow and a trimethylarsenic partial pressure of about 0.5 Torr. GaAs layers have n-type background doping ($2x10^{16}$ $cm^{-3} \geq N_d \geq 1x10^{17}$ cm^{-3}) and mobilities of 2500-3000 cm^2/V s at room temperature.

As in Si LRP, gas flows are initiated and stabilized while the wafer is cool. The growth of epitaxial layers is initiated by pulsing the lamps and bringing the wafer rapidly to growth temperature. At the end of each layer the lamps are shut off, the wafer cools rapidly toward room temperature, and the reaction is halted. The cooling rate is enhanced by cooling the walls of the quartz reaction chamber with a high flow of compressed air, switched on at the termination of layer growth. Heat conducts rapidly away from the wafer through the hydrogen carrier gas. Rise and fall times are on the order of 10 s. Any desired structure may be grown by a sequence of these steps, as shown in Figure 5 for a GaAs/Al_xGa_{1-x} As multilayer structure. Note that the GaAs is grown at 670°C and the AlGaAs at 720°C. We found these temperatures

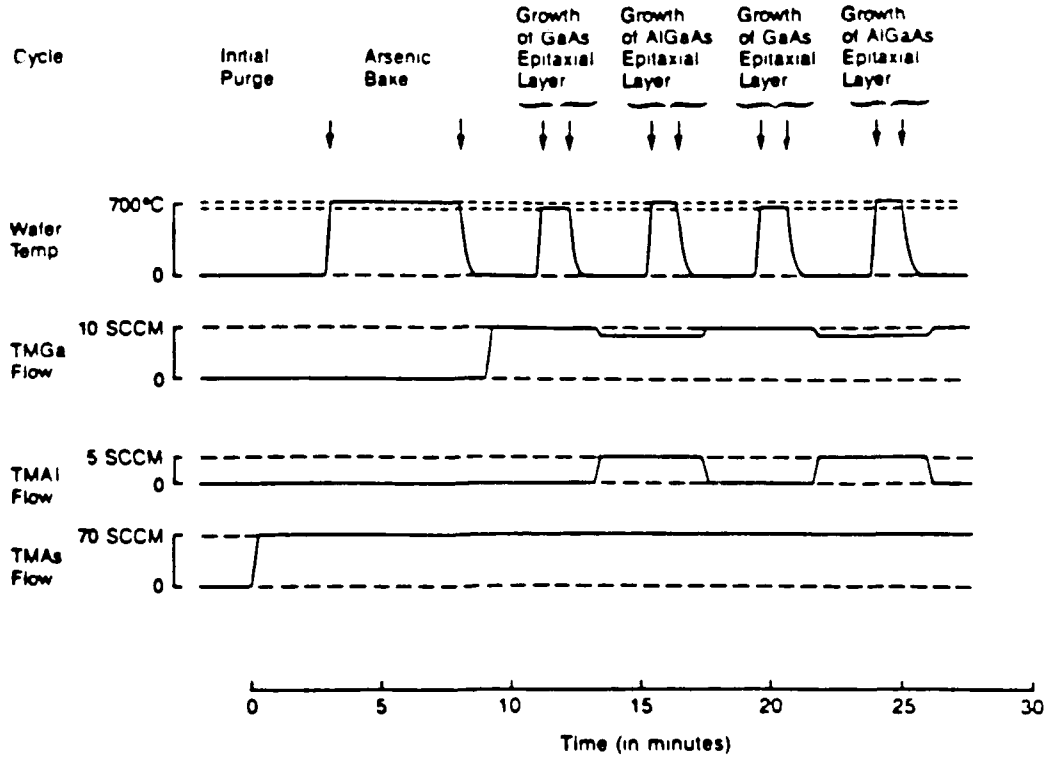


Figure 5. LRP process timing diagram showing how layers are grown by pulsing the wafer temperature in the presence of the correct reactive gases.

gave the best mobility and surface morphology for single layers of each material. An Auger depth profile of a GaAs/$Al_{0.12}Ga_{0.88}As$ multilayer structure grown by this process sequence is shown in Figure 6. Layers are abrupt to within the resolution of Auger (50-60Å). The total thickness of the structure is about 600 Å.

One of our early concerns was that poor material would be grown during the cool down period, creating defects in the growth of subsequent layers. Test structures consisting of multiple layers of GaAs or alternating layers of GaAs/$Al_xGa_{1-x}As$ (3 to 11 layers, 500 Å to 2500 Å layer thickness) have been grown by a sequence of rapid thermal cycles. These structures have excellent surface morphology, and the sheet carrier concentrations and Hall mobilities are equivalent to single layers grown by conventional MOCVD in our reactor. Such test structures have been analyzed by Rutherford backscattering and ion channeling, showing minimum yields of about 4.0%, the same as bare GaAs wafers. Within the resolution of RBS, there are no crystal defects at the interfaces.

Figure 7 shows a lattice image TEM photograph of a GaAs-AlAs superlattice. The transition between the layers occurs within 2 to 4 atomic planes, making the abruptness of this structure equivalent to MBE grown material. Because gases are completely purged between successive layers, we believe that this technique is capable of atomically abrupt interfaces. There are defects present at one interface which we speculate to be oxide inclusions in the AlAs (pure AlAs is very oxygen reactive). The interface at which AlAs is grown on GaAs does not display such defects. These defects are probably not inherent to the pulsed growth process.

We have also made capacitance voltage (C-V) measurements on multiple layer structures of GaAs, by reverse biasing a Schottky diode fabricated on the surface. These layers were grown by flowing TMAs, TMGa, and SiH_4 continuously, but pulsing the lamps through 6 cycles to grow 6 individual layers. Figure 8 is a plot of carrier concentration versus

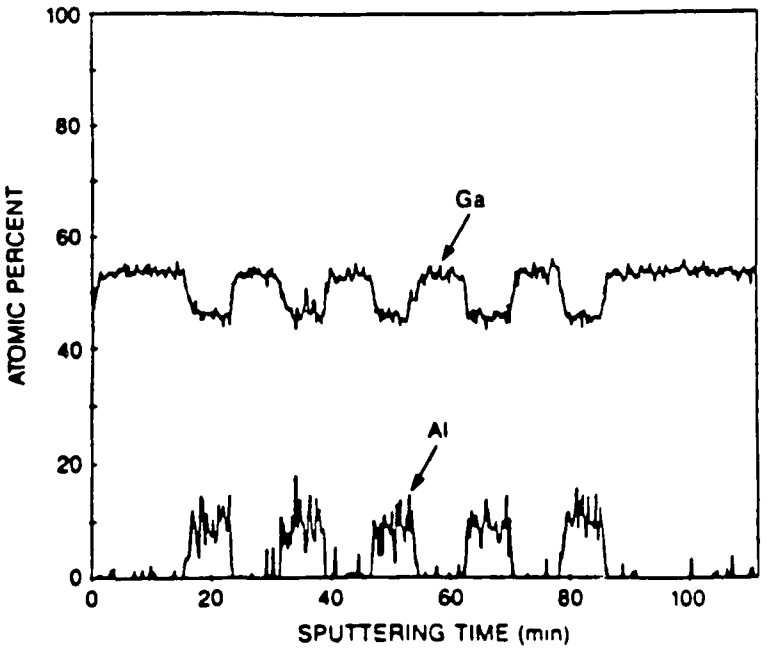


Figure 6. Sputtering Auger profile for sample 135 showing a structure of alternating GaAs/$Al_{.12}Ga_{.88}$ As layers. Total thickness is about 6000 Å. Aluminum scaled by 2 (Chas. Evans & Associates, Redwood City, CA).

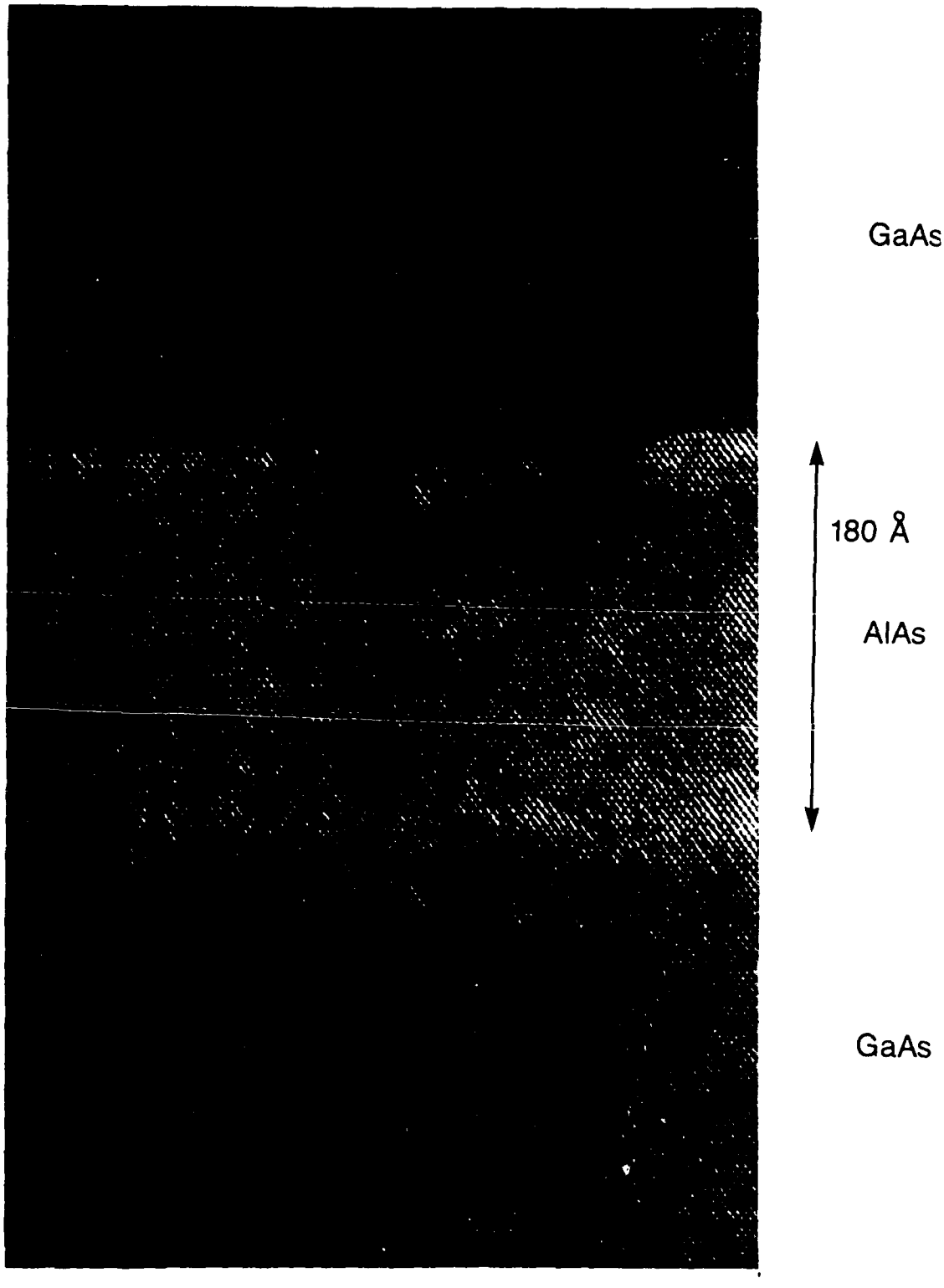


Figure 7. High resolution TEM image of an AlAs-GaAs superlattice. The light layer is AlAs, 180 Å thick.

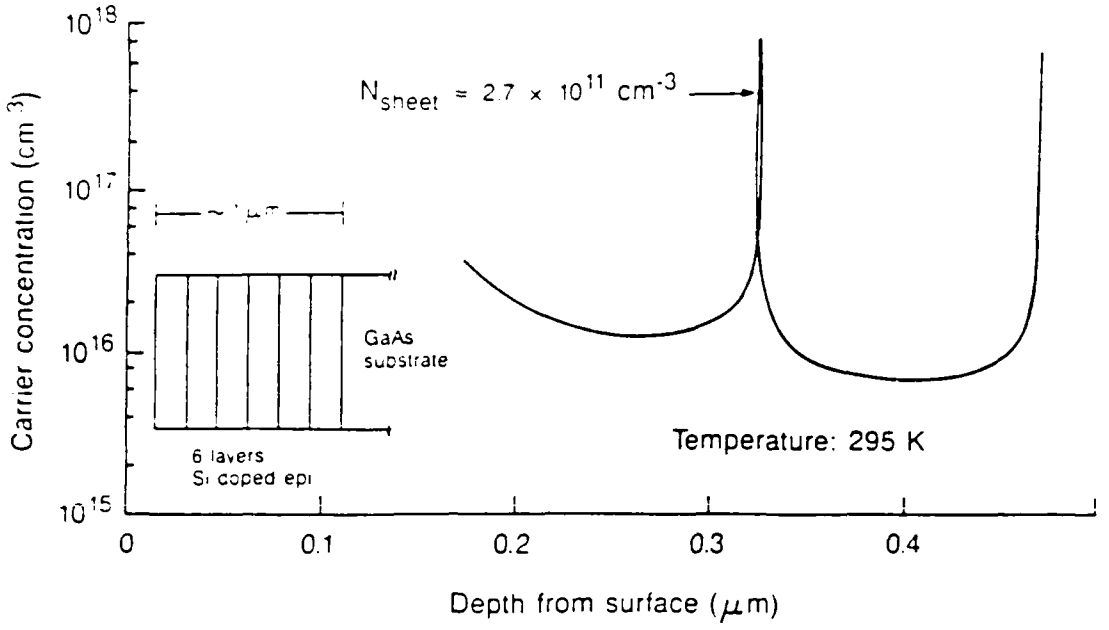


Figure 8. Carrier concentration versus depth for a multiple layer GaAs structure, extracted from C-V measurements. This structure has a total of 6 layers, although only 2 of them appear in this plot.

depth extracted from these measurements, revealing large peaks in carrier concentration at regular depths from the surface. The peaks correspond to a sheet carrier density of about 2.7×10^{11} cm^{-2}. However, it is not clear whether these peaks are a true profile caused by a sheet of shallow donors (Si pile up at each interface) or a measurement artifact caused by the release of electrons from deep interface states. Similar C-V profiles have been observed for growth interrupted interfaces in MBE [15,16]. We will perform depth profile by Secondary Ion Mass Spectrometry (SIMS) to see if there are interface impurity peaks corresponding to the C-V peaks. This should distinguish impurity pile up from deep interface states.

These preliminary C-V results indicate that our pulsed growth technique for GaAs generates electrically active interface states or dopant pile up, which may be dependent on the growth conditions. We are planning experiments to explore the effect of thermal ramp times on interface quality. It may also be possible to reduce these states by means of a different temperature profile. For instance, As condensation on the surface may be occurring when the wafer is cooled rapidly in an As ambient. Cooling to an intermediate temperature or including an anneal step between successive layers may give different results.

Future Work in III-V Epitaxy

The ability to rapidly change substrate temperature could be extremely useful even if not used as an on/off reaction switch. For example, it could allow GaAs and AlGaAs layers to be grown at different optimum temperatures, as in the modified process diagram of Figure 9. In this diagram growth of layers is commenced by introducing reactant

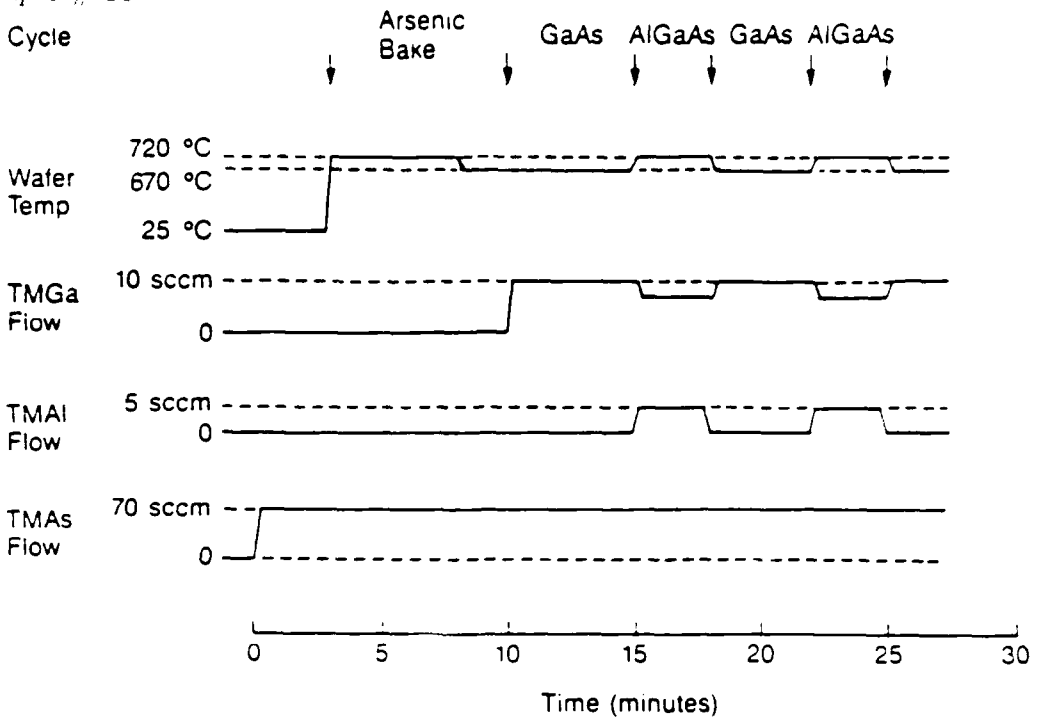


Figure 9. Modified process timing diagram showing how the various layers in a structure could be grown at different optimum temperatures, using rapid lamp heating.

gases, but the wafer temperature can follow the gas composition much more rapidly than in traditional MOCVD. It would be entirely reasonable to raise the wafer temperature for as short as 10 seconds to grow a thin AlGaAs layer, then return it to a lower growth temperature for other layers. Rapid lamp heating is also ideal for GaAs on Si growth, since it would allow short high temperature pre-cleaning of the silicon wafers or in-situ annealing steps to improve the GaAs on Si crystalline quality.

As-ambient RTA

We have some preliminary results for the rapid thermal annealing of Si implanted GaAs in a TMAs overpressure. We have begun a study of arsenic overpressure annealing in a time/temperature regime not accessible with an arsine furnace. We are also making a comparison of proximity capped (2 GaAs wafers face-to-face) versus As-ambient RTA.

Undoped GaAs wafers were implanted with Si at doses of 10^{13} to 10^{15} cm^{-2} and energies of 50-100 keV. Anneals were performed at atmospheric pressure in $\simeq$ 1 ℓ/min of flowing H_2 with 2.0 Torr TMAs. Figures 10 and 11 show the activation efficiency of a 10^{13} cm^{-2}, 50 keV implant for various anneal conditions. As expected, activation efficiency increases with anneal temperature up to about 830°C, above which it increases slowly. At 830°C, a 10 second anneal is just as effective as a longer one.

Rutherford backscattering has been used to study the surface degradation of As-ambient samples compared with proximity capped samples. The As-annealed samples always show lower surface backscattering yields. The higher yields on the proximity capped samples are thought to be

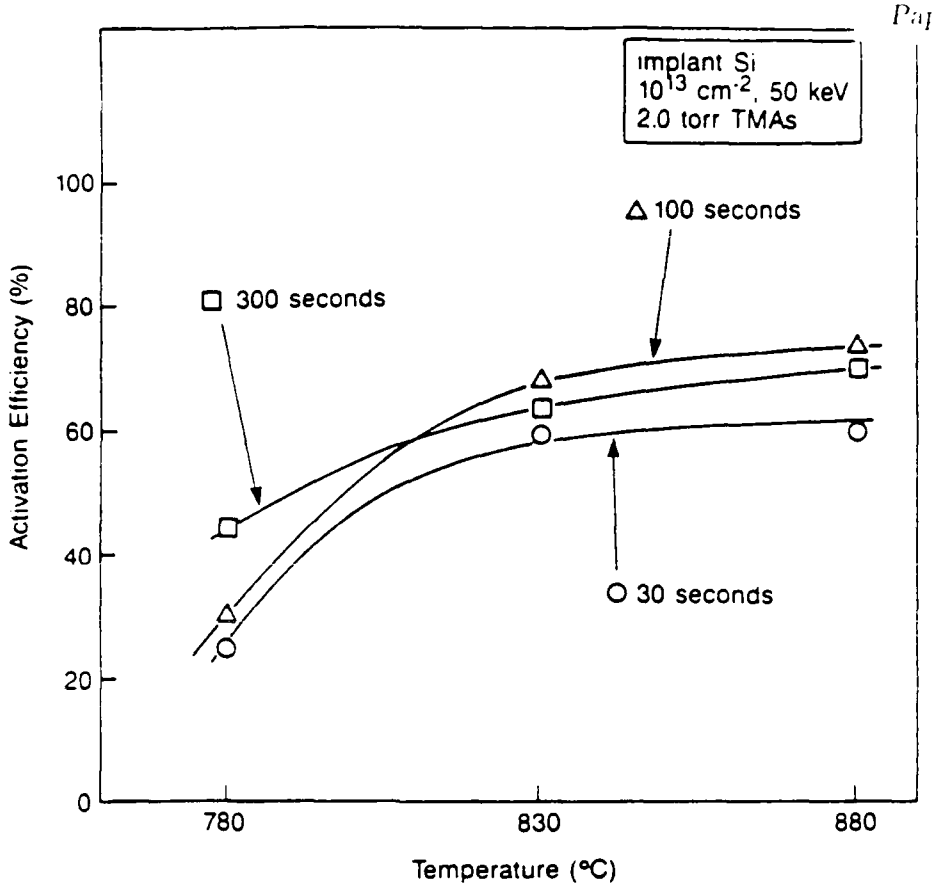


Figure 10. Activation efficiency versus anneal temperature for a TMAs ambient RTA.

caused by preferential arsenic evaporation. This study will be reported in more detail when we have completed it.

SUMMARY

Limited reaction processing (LRP) has been used to grow high quality multiple layer films of Si with clean interfaces. MOSFETs have been fabricated in layers grown by selective silicon epitaxy, with the gate oxide fabricated in the same reaction chamber immediately following epi growth. More demanding bipolar structures are in process. Epitaxial growth of Si_xGe_{1-x} alloys has also been demonstrated. We are continuing studies on this material and hoping to fabricate heterostructure devices.

LRP has also been used to grow multiple layers of GaAs and related III-V compounds. These layers have surface morphology and Hall mobility equivalent to layers produced by conventional MOCVD in our reactor. Abrupt interfaces, with transition widths of 2 to 4 atomic layers, have been obtained at atmospheric pressure using high growth rates (3 μm/hr ≈ 10 Å/sec). There remain potential problems with interface state density which we are investigating.

The unfocused tungsten halogen lamps have also facilitated a novel thermal precracking technique, producing the best GaAs ever grown using trimethylarsenic (TMAs). Background doping and carbon incorporation are substantially reduced, and room temperature electron mobilities up to 4500 cm^2/V.sec are obtained [1]. Finally, we have reported

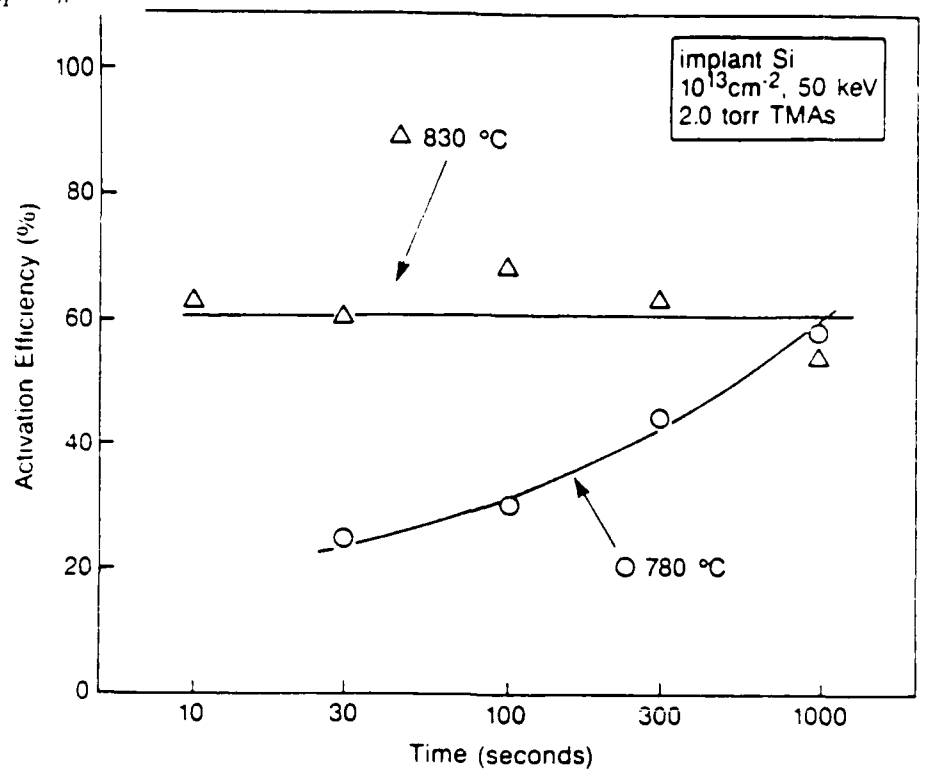


Figure 11. Activation efficiency versus anneal time, same conditions as Figure 7.

preliminary results for arsenic ambient RTA. Initial data indicates significantly reduced surface degradation compared to the proximity capping technique.

ACKNOWLEDGMENTS

We would like to acknowledge the support of J. Zavada and R. A. Reynolds at Defense Advanced Research Projects Agency under contracts DAAG 29-85-K-0054 and DAAG 29-85-K-0237. C. Gronet and S. Reynolds acknowledge support of Office of Naval Research Fellowships.

REFERENCES

[1] J. F. Gibbons, C. M. Gronet and K. E. Williams, Appl. Phys. Lett. **47**, 721 (1985).

[2] C. M. Gronet, J. C. Sturm, K. E. Williams and J. F. Gibbons, MRS Symposium on Rapid Thermal Processing, Boston, MA, Dec. 1985 (Materials Research Society, Pittsburgh, PA 1986), Vol. 52, p. 305.

[3] C. M. Gronet, J. C. Sturm, K. E. Williams, J. F. Gibbons and S. D. Wilson, Appl. Phys. Lett. **48**, 1012 (1986).

[4] J. C. Sturm, C. M. Gronet and J. F. Gibbons, IEEE Electron Device Lett. **EDL-7**, 282 (1986).

[5] S. Turner, C. Gronet and J. Gibbons, Appl. Phys. Lett. to be published.

[6] C. M. Gronet, C. A. King, W. Opyd, J. F. Gibbons, S. D. Wilson and R. Hull, J. Appl. Phys. **61**, 2407 (1987).

[7] J. Sturm, C. Gronet, C. King, S. Wilson and J. Gibbons, IEEE Electron Device Lett. **EDL-7**, 577 (1986).

[8] J. C. Sturm, C. M. Gronet and J. F. Gibbons, J. Appl. Phys. **59**, 4180 (1986).

[9] C. M. Gronet, C. A. King and J. F. Gibbons, MRS Symposium, Palo Alto, CA 1986 (Materials Research Society, Pittsburgh, PA 1986), **71**, 107.

[10] J. F. Gibbons, C. M. Gronet, J. C. Sturm, C. A. King, K. Williams, S. Wilson, S. Reynolds, D. Vook, M. Scott, R. Hull, C. Nauka, J. Turner, S. Laderman and G. Reid, MRS Symposium, Boston, MA, Dec. 1986 (Materials Research Society, Pittsburgh, PA 1987), to be published.

[11] F. W. Smith and G. Ghidini, J. Electrochem. Soc., **129**, 1300 (1982).

[12] D. W. Vook, S. Reynolds and J. F. Gibbons, Appl. Phys. Lett., to be published.

[13] C. A. Tromson, D. Gibart, R. Druilhe, Y. Monteil, J. Bouix and B. El Jani, Rev. Phys. Appl. (France) **20**, 569 (1985).

[14] W. T. Dietze, M. J. Ludowise and C. B. Cooper, Electronics Lett. **17**, 698 (1981).

[15] Y. Iimura, T. Shiraishi, H. Takasugi and M. Kawabe, J. Appl. Phys. **61(5)**, 2095 (1987).

[16] A. Takamori, E. Miyauchi, H. Arimoto, Y. Bawba, T. Monta and H. Hashimoto, Japan J. Appl. Phys. **24(6)**, 1414 (1985).

Part 4

List of Scientific Personnel

1. James F. Gibbons, Principal Investigator
2. James C. Sturm, Research Associate
3. Graduate Students:
   (a) Chris M. Gronet
   (b) Judy L. Hoyt*
   (c) Cliff A. King
   (d) Walter G. Opyd
   (e) Scott K. Reynolds*
   (f) Dietrick W. Vook

* indicates Ph.D. earned while employed on this project


FILMED
58