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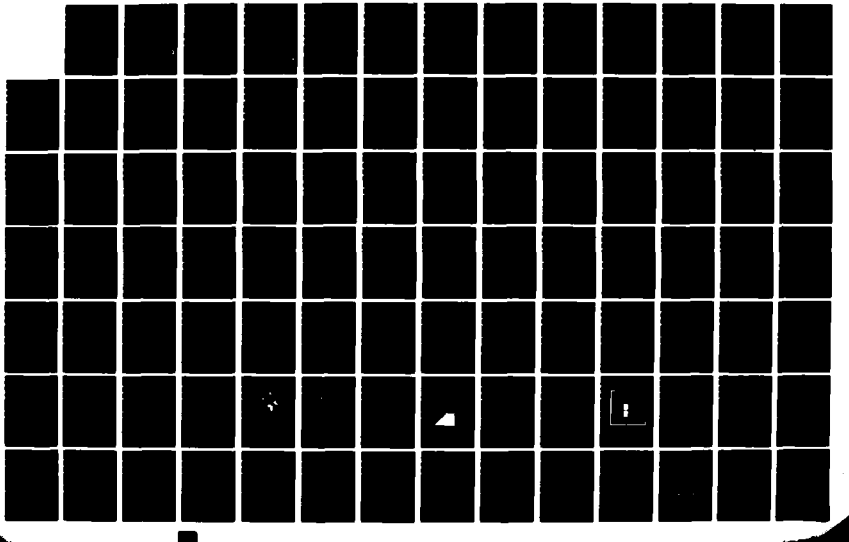

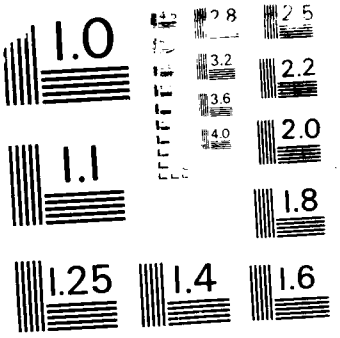

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FABRICATION AND ELECTRICAL CHARACTERIZATION OF MULTILEVEL ALUMINUM INTERCONNECTS USED TO ACHIEVE SILICON-HYBRID WAFER-SCALE INTEGRATION

THESIS

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THESIS

Presented to the Faculty of the School of Engineering

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Air University

In Fulfillment of the

Requirements for the Degree of

Master of Science in Electrical Engineering

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First Lieutenant, USAF

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Preface

The purpose of this research was to develop, fabricate, and electrically characterize a silicon-hybrid wafer-scale integration (WSI) technique. The development of a WSI technique is driven by the high-speed interconnection requirements of the 272-point Prime Factor Algorithm (PFA) processor. However, the technique can be broadly applied to other high-speed systems employing very large-scale integrated circuits (VLSIC).

Circuits on two discrete die were integrated on a single wafer, and the interconnects between the two die were electrically evaluated. Because of problems encountered in the processing environment, a system test of the wafer-scale circuit could not be performed. Instead, a limited test was performed to compare an isolated interconnect with the present hybrid integrated circuit technology. The results show that the interconnect design is very promising. Therefore, research into WSI should be continued along with improvements to the AFIT integrated circuit processing environment.

I am indebted to many people for the successful completion of this thesis. I would like to give special mention to my advisor, Maj Edward S. Kolesar. His advice and encouragement throughout the experimentation and writing of this thesis was always motivational. I also wish to thank Capt Robert W. Mainger for the benefit of his previous experience with this research. In addition, I would like to express my appreciation for the processing assistance given by Mr. Donald Smith at the Cooperative Electronics Materials and Processes Laboratory, and Mr. Stuart Callahan at the Avionics Laboratory. A word of thanks is also owed to Capt David Gallagher whose assistance helped me submit my MOSIS circuit design in record time. Finally, I want to thank my wife Melissa and my daughter

Caroline. Their sacrifice during my studies at AFIT are more than I could ever dream of repaying. Above all, I thank God for giving me this precious opportunity to learn the secrets of His creation.

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Abstract

The purpose of this research was to develop, fabricate, and electrically characterize a wafer-scale process developed for use with the 272-point Prime Factor Algorithm (PFA) processor. This process integrates discrete integrated circuit die in a planarized wafer package. The entire wafer surface was coated with photosensitive polyimide, which was patterned with vias for the interconnect contacts. The two die were electrically interconnected with printed aluminum interconnects using conventional silicon processing equipment.

The original goals of this research included a system test to evaluate the interconnect network. However, difficulties in the processing environment only allowed a single interconnect to be parametrically evaluated up to 10 MHz. The aluminum interconnect was 26 microns wide and 1.2 microns thick. This interconnect exhibited no distinguishable propagation delay and attenuation for a one centimeter path length. In addition, the the level of distortion introduced by the printed interconnect was no greater than the level of distortion introduced by a conventional wire-bonded interconnect. Therefore, the printed wafer-scale interconnect design was shown to be a superior electrical conduit.

The processing environment introduced a number of fractures in the interconnect network. These fractures were isolated at severe topographical steps encountered on the wafer's surface. The severity of these discontinuous steps were attributed to the uneven fill of the

mounting epoxy in the wafer-to-die transition. It was also determined that the spin-on materials used to fabricate the interconnects did not provide adequate planarization and coverage over this transition. Further research is recommended to determine the planarization capability and controllable patternability of the photosensitive polyimide used in this research. In addition, alternate photoresist materials are recommended for application to this future research.

FABRICATION AND ELECTRICAL CHARACTERIZATION

OF

MULTILEVEL ALUMINUM INTERCONNECTS

USED TO ACHIEVE

SILICON-HYBRID WAFER-SCALE INTEGRATION

I. Introduction

Background

Due to the recent influx of numerous approaches for achieving wafer-scale technology, an industry standard definition of wafer-scale integration (WSI) is difficult to identify. In 1983, Douglas Peltzer, Vice President of Technology Operations, Trilogy Systems Corporation, defined WSI as:

> ... the ability to create an integrated circuit that is large enough to cover the entire surface of a silicon wafer -- an area on the order of three inches in diameter (51:43).

At first thought, this capability apparently requires only a simple extension of current technology over a larger area. However, Peltzer warned against this naive approach by enumerating six problems encountered with this higher level of integration: "... wafer yield, heat dissipation, package connections, circuit and system design, CAD [computer-aided design] tools, and testing" (51:43). Since "random point" defects (e.g. crystal dislocations and mask registration errors) increase exponentially with circuit area, the probability of a catastrophic defect occuring will increase, and adversely affect wafer yield. Because WSI increases the density of active devices, heat dissipated by the circuit is

confined to a smaller area, reducing the maximum power allowed for the circuit. Also the increased number of circuit elements introduces the problem of routing power to these densely packed devices, posing additional packaging requirements. Optimizing circuit speed and device parameters becomes more difficult because longer interconnects are required between subsystems. As a result, considering design trade-offs at the transistor level (where as many as 250,000 circuit elements are possible) is hardly a trivial task; therefore, CAD tools specially designed for WSI systems must be employed. The vast number of states for a circuit this extensive is equally as formidable; nevertheless, testing procedures and tools must be designed to meet the challenge. Therefore, a transition from VLSI to WSI must overcome several obstacles (51:43-46).

Until recently, the benefits of WSI seemed hardly worth the problems encountered. In the 1960's Texas Instruments pursued one of the semiconductor industry's first attempts at large-scale integration using a WSI approach; however, it was eventually dropped for the more economical process of individually packaging diced and tested chips (43:32). For almost twenty years, WSI was given little attention until recent advances in device technology made the delays in conventional integrated circuit (IC) interconnects appreciable. By 1983, feature sizes were reduced to below 1.5 microns, and switching speeds were about two nanoseconds. As a result, interconnect delays had become a major contributor to the overall delay in integrated circuit system design (6:88). Since conventional IC packaging can increase the effective area consumed from two to ten times the chip area, interconnect lengths could be reduced by more economical packaging techniques (43:32). Because wafer-scale integration can eliminate individually packaged chips and result in faster systems,

several companies and institutes have embarked on this new wave of technology (42:32).

In 1986, Donald Meyer, a consultant with New Technology Concepts, categorized all WSI techniques into two basic approaches -- "monolithic" or "hybrid" (47:32). Monolithic WSI incorporates redundant copies of each chip directly printed on the substrate to improve wafer yield. The large-scale integration (LSI) practice of dicing and sorting good chips from bad is not performed. Instead, the bad chips are left on the wafer and bypassed by various "discretionary" wiring techniques. Hybrid WSI uses only functional chips diced and sorted from various whole wafers. The acceptable die are mounted on a separate wafer where the interconnects are created (47:32).

The Air Force Institute of Technology (AFIT) is investigating a hybrid wafer-scale technique for its 272-point Prime Factor Algorithm (PFA) processor currently under development. As a multi-chip VLSI system requiring high-speed interchip communications (i.e. a 35 MHz memory cycle), the PFA processor is a suitable candidate for wafer-scale integration. In 1986, a model WSI fabrication process for the PFA effort was proposed by Major Edward S. Kolesar and implemented by Captain Robert W. Mainger. This process includes a technique to anisotropically etch wells into a silicon wafer substrate for retaining discrete ICs (40).

Problem Statement

The purpose of this research is to implement and characterize the electrical performance of the AFIT WSI process. The interconnects and their interface to complementary MOS (CMOS) circuits will be physically and electrically characterized to determine what limits can be expected

for the PFA implementation. The ultimate goal of this thesis project is to assess the feasibility of implementing the 272-point PFA processor using the WSI process developed at AFIT.

Scope

This project continues the thesis effort of Capt Mainger's research toward the goal of identifying an appropriate WSI fabrication procedure to implement the PFA processor (40). Because the thickness of chips vary with each fabrication line, the WSI process must be adapted to provide selective control for etching the cross-sectional area and depth of wells in the silicon wafer substrate. In addition, the process must be expanded to include second-level metallization.

Since inactive die (aluminum lines) were used to develop the initial WSI fabrication process, an appropriate interchip connection technique using active chips (functional circuits) requires further investigation. The electrical performance characteristics of two interconnection methods -- wire bonding and direct aluminum metallization -- will be accomplished, electrically tested, and compared. If either of these techniques prove feasible, the optimum interconnect method will be recommended to integrate the PFA processor on a wafer scale.

Assumptions

Because this research is intimately tied to materials and products furnished by others, several assumptions had to be made before this effort began. Since the Metal-Oxide Semiconductor Implementation Service (MOSIS) was proposed to fabricate the functional die used in this project, the chip thickness was assumed to be at most 200 microns. Because wafer thickness has never been a critical parameter for circuits fabricated by

MOSIS, the PFA system will likely include die of different thicknesses. Further, it is assumed that an appropriate bonding material for the die will be recommended as a result of Capt Mainger's research. In addition, it is assumed that at most two metallization layers will be required to implement the PFA system. Finally, if neither of the proposed interconnect techniques work, the failures will be thoroughly evaluated, and an alternative technique will be recommended to achieve the ultimate goal of this study.

Approach

As an initial thrust, the problem of evaluating the electrical performance characteristics of multilevel aluminum interconnects will be analyzed. Several metallization structures will be fabricated to satisfy certain processing, physical and electrical requirements. These structures will be tested with inactive die before selecting a structure to integrate with functional circuits. Next, a test circuit will be designed using complementary metal-oxide semiconductor (CMOS) technology. Two copies of this test circuit will be mounted on a silicon substrate using the WSI design selected in the earlier tests. In addition, a control sample with wire-bonded interconnects will undergo the same system test performed on the candidate structure. These integration techniques will be electrically characterized and compared to evaluate the merits of the proposed AFIT WSI technique.

Presentation

This report will document this research effort. To establish the foundation of wafer-scale interconnect technology, chapter II reviews the research concerning the fabrication and electrical characterization of

integrated circuit interconnects. Based upon this background, an optimal interconnect design will be proposed. To evaluate the efficacy of this design, an experimental evaluation will be accomplished as outlined in Chapter III. An analysis of the results of these experiments will be documented in chapter IV, and recommendations for further research will be proposed in chapter V.

II. Theoretical Background

Although the approaches to wafer-scale integration published in the literature are numerous, each deal with basically the same set of interconnection problems (42:3128). The success of each approach is determined by how quickly and reliably it can propagate a multitude of signals from circuit to circuit. This chapter surveys the efforts of others who have attempted to obtain this capability. First, various fabrication techniques for wafer-scale interconnections will be reported through a survey of published literature. Next, several electrical phenomena possessing the potential to degrade reliable signal propagation will be reviewed. Finally, a candidate interconnect design will be proposed.

Fabrication Techniques for Multilevel Interconnects

This section concentrates on previous work and studies pertinent to the fabrication of wafer-scale interconnects. Special emphasis will be paid to the materials used to construct planar levels and the methods adopted to insure high yield interconnects. As process development engineers at Gould AMI Semiconductors, Saxena and Pramanik stated:

> ...the addition of extra levels of interconnects ... results in severe topography throughout the die and is caused by the underlying layers containing patterned conductors and dielectrics. Additional topography is due to vias/contacts made in the dielectric layers ... Planarization is desirable in double metal technology for yield improvement but is regarded as essential in triple and 4-level metal technologies and beyond (62:95).

This section looks at the fabrication techniques used to realize reliable planarized layers of metal and dielectric.

Metals. Of the WSI processes surveyed, all used or recommended

aluminum or its alloys for multilevel metal interconnects. This is not surprising since aluminum is extensively utilized in silicon integrated circuit processing (70:372). Honeywell specified AlTiW as an aluminum alloy for interconnects (67:194), while MIT's Lincoln Laboratory used an AlSiCu alloy (55:121). Titanium, tungsten, and copper can be used to enhance the electromigration resistance of aluminum conductors (20:68). In addition, the Honeywell circuits were flip-chip mounted with solder bumps; therefore, a special external contact material (CrCuAu) was required (67:194).

The technique employed for aluminum deposition and patterning was specified in only two cases. R. Wayne Johnson and his Auburn University colleagues used aluminum, "patterned using positive photoresist", for first-level metal. For the second-level die-to-wafer interconnect links, they recommended:

> The surface should be backsputtered to reduce via contact resistance prior to sputter deposition of aluminum. The metallization is patterned using wet chemical etching and no post annealing is used (29:847,8).

Saxena and Pramanik explained the use of this technique to planarize metal:

> The distribution of material sputtered from the target is usually such that perpendicular step walls do not experience adequate coverage. A negative substrate bias can help aleviate this problem by inducing ions from the plasma to bombard the growing film. One of the effects of this bombardment is to resputter material from bottom of the step to the sidewalls of the step and from [the] topmost edge of the step to the bottom. This effect has been used to realize planarized Al films (62:98).

Backsputtering was suggested for thin film aluminum deposition. However, the WSI work at Rensselaer Polytechnic Institute (RPI) used a thick film lift-off procedure (14:54). Lift-off techniques, like RPI's, which use stud vias have acknowledged planarizing effects (62:98).

Dielectric. Apart from obvious electrical insulating capabilities, interconnect dielectrics should possess the following properties: (1) small dielectric constant to reduce signal delays, (2) low pinhole density to prevent shorting between layers, (3) high modulus of elasticity to withstand temperature coefficient of expansion mismatches between materials, (4) low reflow temperature to allow good step coverage without damaging previous layers, (5) good adhesion to maintain monolithic integrity with other processing materials (63:97).

Where mentioned, all WSI approaches surveyed grew a thermal oxide layer on the silicon substrate before forming the first-level metal pattern (29:846;67:194;55:125). Interlevel dielectrics are split between glass (67:194), polyimides (14:55;29:848;55:122), and amorphous silicon (55:125;7:11). A final passivation layer was also suggested, however, a specific material (silicon nitride) is referred to only once (67:194).

Thermal Oxides. The highest quality oxide is a thermally grown silicon dioxide (SiO_2) layer. Although thermally grown SiO_2 layers are appropriate where a silicon surface is available (e.g. unprocessed wafers), once the first metal layer has been formed, an additional SiO_2 layer cannot be thermally grown on the metal surface. Therefore, an alternate oxide deposition method must be adopted to produce the necessary interlevel dielectric. In addition, if the metal is aluminum, the deposition temperature must be significantly below 650°C to keep the metal from melting (70:341,343).

CVD Oxides. Low Pressure Chemical-Vapor-Deposited (LPCVD) oxides can be deposited by reacting silane and oxygen at 450°C. Vias in CVD oxides can be wet-etched with hydrofluoric acid (70:358) or dry-etched with a CHF_3/O_2 plasma (50). However, CVD oxides are highly nonconformal

at the sharp steps formed by the underlying metal pattern. As a consequence, the poor step coverage may allow second- and first-level metal to be shorted. Step coverage can be improved by doping the oxide with phosphorous using a simultaneous reaction of phoshine and oxygen at 450°C. The resultant material, known as phosphosilicate glass (PSG), must be heated to its re-flow temperature (about 1100°C for 20 minutes) before step coverage benefits are realized (70:357,360). At AT&T Bell Laboratories, planar step coverage was obtained at 950°C by doping PSG with boron (37:129). However as pointed out by Saxena in 1984:

> Clearly the thermal flow of dielectric is not feasible for dielectrics deposited over Al lines as processing temperatures must be kept preferably below 450°C (63:97).

As a low temperature alternative compatible with Al lines, planarization can be achieved by etching back excess glass. Studies performed at Northern Telecom Electronics exploited the improved step coverage obtained when thick films are applied. J. S. Mercier, et al, reported:

> Dry etching techniques can be successfully used on overthick [sic] PSG films to reduce the ratio of the PSG film's thickness to underlying step height towards unity, while preserving the superior step coverage profile obtained with the thicker films (46:103).

Another highly practiced etchback technique employs the excellent conformal characteristics of spin-on films. Nitin Parekh and his colleagues at the Xerox Palo Alto Research Center described this procedure:

> "... a low viscosity liquid is spin coated to form a sacrificial semi-planar layer over the insulator which is to be planarized. The resulting semi-planar surface is then etched anisotropically in an etch mixture which etches the sacrificial layer and the insulator at roughly the same rate. The sacrificial layers usually employed are photoresists or polyimides. Problems have been encountered with non-reproducibility of etch rates and excessive contamination of the etcher with polymer. Recently, there has been increased

> interest in the use of so called 'spin-on glasses' (SOG) as sacrificial layers. This may be due in part to the fact that their etch properties are closer to those of CVD oxides" (50).

John K. Chu and his co-workers at Intel Corporation explained why SOG cannot be used as a "stand alone" dielectric:

> The simplest technique with SOG planarization would be using a stand alone SOG film as the intermetal dielectric [IMD]. Since there is no such glass material that can spin on [sic] up to [a] 1 um thick film on metal pattern and still maintain its crack resistance and dielectric characteristics, stand alone SOG as the IMD is clearly not an available choice (11:475).

In fact, even as a planarization coating over CVD oxide, the SOG should be etched away. Parekh, et al detailed the problems encountered when depositing metal on SOG surfaces:

> Photoresist can exhibit poor adhesion to some SOG materials during via photomasking operations. In addition, when aluminum/2% Cu is deposited directly on SOG, problems are experienced during subsequent patterning of the aluminum. Regions of the cured SOG apparently chemically interact with the Al/2% Cu resulting in some regions of metal which have a very high resistance to our plasma aluminum etch. Residue is consequently left behind after etching the second metal resulting in a severe intra-level shorts problem. Finally, the ability of our aluminum plasma etch to stop on SOG was poor, resulting in significant loss of SOG (50).

Because some SOGs use "silicate-like precursors dissolved in organic solvents" (50), a French research group also discovered that there is a "leakage current between two aluminum lines that appears with carbon-rich SOG" (58:491).

To avoid the reliability concerns of interfacing SOG directly to aluminum and losing CVD oxide during etch back, Chu, et al suggested:

> ... a sandwich scheme with SOG etched back and encapsulated between two layers of CVD dielectric films can be employed. Unlike resist planarization, only partial etching of the SOG and the bottom CVD dielectric composite is needed prior to the second CVD dielectric deposition on top. ... Since only a small amount of SOG remains between metal spacings, it is completely protected from subsequent maskings by the CVD films, which are materially far more compatible than SOG (11:475,6).

Nevertheless, this scheme does not reconcile the disadvantages encountered when using SOG. Parekh, et al added:

> The SOG apparently exhibits a tendency to quench the etch rate of of the plasma etch process used for the definition of vias (50).

Polyimides. In 1981, Arthur M. Wilson of Texas Instruments evaluated polyimide as a reliable intermetal dielectric:

> Polyimide films are reliable high temperature planarizing insulators for multilevel interconnection systems, which may be the key to high yielding bipolar and MOS very large-scale integrated circuits (76:145).

John J. H. Reche of Reche Corporation, discussed the comparative advantages of polyimide compared to CVD oxides:

> ... polyimides are generally less costly, easier to use and provide more process flexibility. Common photoresist processing equipment is suitable for polyimides. This provides a significant savings over the capital required for CVD or PVD [physical vapor deposition] processing. ...And the processing of polyimides is done at 300°C to 400°C, which is lower than typical 800°C CVD requirements (57:116).

However, there are disadvantages to using polyimides primarily due to trace water contamination due to incomplete curing or poor dehydration. Mitchell and Goodner of Motorola noted this problem in 1984, but added that it could be easily prevented:

> A major problem with processing polyimide as intermetal dielectric is bubbling of metal that is over polyimide during high temperature processing. ...A dehydration bake of 85°C for four hours is sufficient to prevent metal bubbling in device [sic] which has three layers of polyimide and three layers of metal (24:130,3).

Use of polyimide as a planarizing media are well known. In fact, polyimide has been used as a planarizing sacrificial layer for CVD oxides (58:96). Consequently, the formation of reliable vias through the dielectric is the critical step for insuring functional interconnects. Wet chemically etched vias can be formed in polyimide using negative resist as the mask and hydrazine-hydrate as the etchant. In 1983, Mukai

and his associates at Intel found excellent results with this technique:

> "Layers of 3.5 um thick PIQ [polyimide isoindroquinazoline-dione] are used for the interlevel dielectric and final protection. The second-level aluminum layer is connected to the first layer by means of 20 x 15 um^2 via-holes. ...The yield of a via-hole contact proved to be over 99.9998 percent" (48:465-6).

Several techniques to slope via edges have been employed to improve metal step coverage through vias. Wilson related the results of those using positive resists as the etch mask:

> Partially cured polyamic acid resins are easily etched with dilute bases. Yen took advantage of the fact that positive resists are developed with dilute solutions of strong bases to develop the latent resist image and to etch the via in the polyimide simultaneously in a single process step. The use of a positive resist developer composed of buffered mixtures of tetramethyl-ammonium hydroxide and an organic acid is claimed to provide a favorable slope [angle] of 45^{o}-55^{o} (76:158).

Polyimide can also be dry etched using oxygen reactive ion etching (RIE). In 1984, C. H. Ting and his coworkers at Intel Corporation showed how dry etching can be used to realize sloped vias:

> Sloped sidewall [sic] can also be obtained in PI [polyimide] when an erodible etching mask such as photoresist is used in the RIE process. The erosion rate of the photoresist in the lateral direction will determine the sidewall slope. ...Furthermore, the slope angle obtained with [a] nearly vertical resist pattern [sic] has a strong dependence on the operating pressure during O_2 RIE (71:108).

Intel also successfully created sloped vias using a "non-erodible etch mask" of SOG by etching first with high pressure oxygen followed by a low pressure cycle (71:107-8).

Photo-sensitive polyimides are now commercially available. Reche stated that "the recent introduction of photo-sensitive polyimides has reduced the number of process steps required" (57:117). In fact, photosensitive polyimide precursors cut in half the number of steps required to process standard polyimides with wet etching. Sloped vias

could also be created by using proximity printing to expose the polyimide precursor (18:21).

Amorphous Silicon. Amorphous silicon (a-Si) has been selectively used for fusible links in WSI and "restructurable VLSI" (55:121). In 1987, Mosaic's Albert A. Bogdan related how the "electrically programmable silicon circuit board (SCB)" switches a-Si from an insulator to a conductor:

> "In its normal state, the nominal resistance is approximately 200 Mohms ... When a voltage is applied above a threshold voltage, the resistance switches to a nominal 4 ohms ... The amorphous silicon, upon switching, forms a 1 um filament between the two [metal] layers. ...Tests have shown that once switched, the material does not switch again. It is a permanent connection" (3:12).

In addition, Bogdan cited redundancy as the main advantage WSI accrues from using a dielectric with a fusible link capability:

> "Producing a wafer scale interconnect system on silicon that is defect-free is a difficult task. But with the 'anti-fuses' the interconnect system can withstand defects because the 'antifuses' provide significant redundancy" (3:12).

Essentially, if a defect is found in the link, a new link can be created in its place by reprogramming.

MIT's research into restructurable VLSI also used a-Si as the dielectric. However, in order to prevent the aluminum and silicon from interdiffusing at high processing temperatures, the a-Si is sandwiched between two thin layers of CVD oxide (27:782). Instead of using an electric field to fuse the links, MIT uses an argon laser. Jack Raffel and others at MIT described this technique:

> "The laser pulse incident on top-level metal causes the AlSiCu alloy to melt, and a crater is formed as the metal flows, exposing the amorphous silicon which then melts causing a mixing of melted aluminum and silicon. First-level metal then melts and a conducting path is created between first- and second-level metal, typically on the order of 1 ohm or less" (55:121).

MIT's laser can also cut links to disconnect unused conductors and reduce the line capacitance (55:122).

It should be noted that both Mosaic and MIT used a-Si as the insulator only at points where potential interlevel vias can be made. Although Mosaic did not mention the material used as the interlevel dielectric in the remaining areas, MIT employed a polyimide. In addition, the precise manner in which the a-Si is selectively deposited at via points is not clear from the literature. However, Raffel mentioned that the a-Si can be deposited by "sputtering or plasma-enhanced CVD" (55:122).

Summary. In this section, the materials used in several WSI approaches have been surveyed, and additional studies evaluating alternate techniques to planarize the multilevel structures using these materials have been reported. The planarizing metallization techniques included sputtering and thick-film lift-off, and the methods to planarize dielectrics encompass thermal flow of CVD oxides, spin-on sacrificial layers for CVD oxides, and spin-on polyimides. In addition, methods to fabricate reliable vias between layers have been detailed, including sloped vias in polyimide and programmable vias in amorphous silicon.

Factors Limiting Reliable Signal Propagation

There are several electrical phenomena possessing the potential to degrade the reliable propagation of microwave signals. The ability to predict the behavior of these phenomena will determine how the problems can be controlled and limited. Therefore, the following section will review the physical principles governing three prevalent sources of signal degradation: propagation delay, attenuation, and noise. Based upon these principles, quantitative electrical performance models for each source

will be presented. The associated calculations reveal how material and geometrical parameters impact reliable signal transmission on the interconnect.

Propagation Delays. In the Introduction to this thesis, interconnect delays were cited as the driving requirement for WSI research. Therefore, a wafer-scale design must consider the parameters contributing to signal delay. In this section, the expected signal delay will be derived as a function of electrical and geometrical line parameters. The derivation will begin with the generalized transmission line equation, which will be simplified by limiting assumptions applicable to this thesis. This simplified expression will be solved for the time delay in the line. Next, variations of the time delay expression and techniques for improving unacceptable delays will be presented from the published literature, and examined for applicability to this research. Finally, the mechanisms of signal delay will be applied to pulse distortion caused by dispersion.

Simplified Time-Delay Derivation. Wafer-scale interconnects can be modeled as uniform, lossy transmission lines (25:289). Therefore, they can be characterized by the generalized transmission-line equation (34):

$$\frac{d^2V}{dx^2} = rg\ V + rc\ \frac{dV}{dt} + lg\ \frac{dV}{dt} + lc\ \frac{d^2V}{dt^2} \qquad (1)$$

where

V = signal voltage (volts)
x = distance along the interconnect measured from the source (cm)
r = distributed resistance of the transmission line (ohms/cm)
g = distributed conductance of the transmission line (S/cm)
c = distributed capacitance of the transmission line (F/cm)
l = distributed inductance of the transmission line (H/cm)
t = time (seconds).

Assumptions. The task of deriving a time delay expression from Equation (1) can be simplified by applying several assumptions appropriate to the wafer-scale design envisaged for this project:

(1) The proposed design geometry is depicted in Figure 1, and the line dimensions are specified in Table 1.

(2) Material properties are homogeneous throughout the conductor and dielectric. With this assumption, distributed parameters can be derived from lumped elements by simply dividing by the path length of the interconnect.

(3) For the anticipated operating frequency range (1 kHz to 70 MHz), the lines are "loosely coupled" (i.e. mutual inductance and capacitance are negligible compared to the corresponding distributed parameters of the line) (1:4).

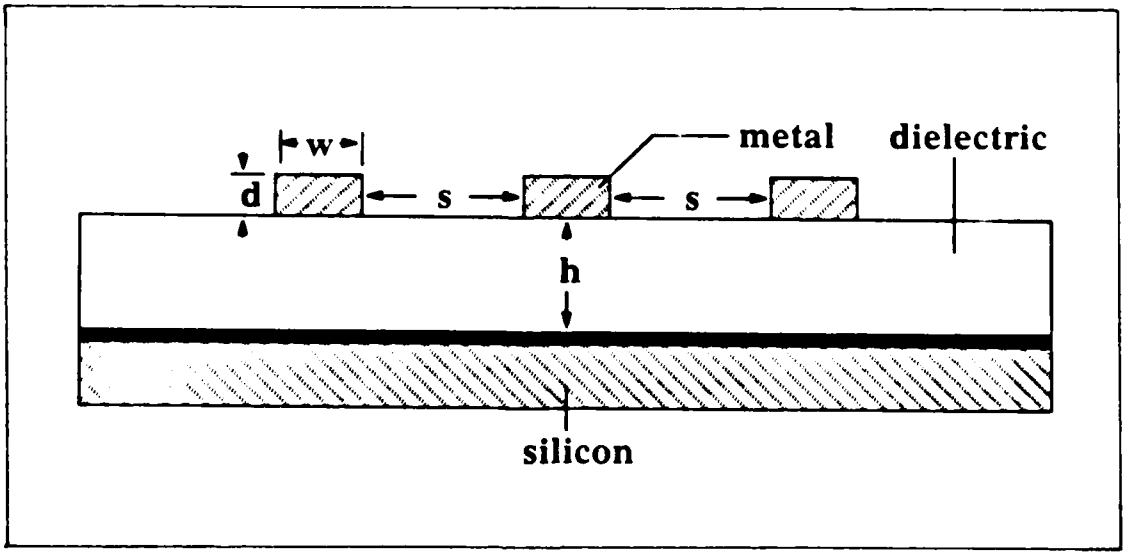

Figure 1. Cross-section of the Proposed Interconnect Structure. Proposed line dimensions for the conductor thickness (d), the conductor width (w), the dielectric thickness between the conductor and the ground plane (silicon) (h), and the conductor separation (s) are given in Table 1.

Table 1. Proposed Line Dimensions

metal thickness, d (um)	metal width, w (um)	conductor-to-ground plane dielectric thickness, h (um)	metal separation, s (um)
1.2	25	20	200

(4) Published experimental measurements for line inductance and capacitance on oxide-passivated silicon substrates are suitable approximations. This seems justified since oxide and polyimide have approximately the same dielectric constant, and most integrated circuit conductors have comparable permeability constants (See Table 3).

(5) The conductor used will be aluminum, and the dielectric will be polyimide (i.e. Selectilux HTR 3-200)

(6) Line conductance will have a negligible effect on the propagation delay. Justification for this assumption will be cited in the following sections.

Estimated Line Parameters. Yuan and his associates at Texas Instruments calculated the line capacitance (Figure 2) and inductance (Figure 3) for a single line on oxide-passivated silicon. By applying Assumptions (1) through (4) and extrapolating the linear characteristic of Figure 2 for a linewidth of 25 microns, the distributed

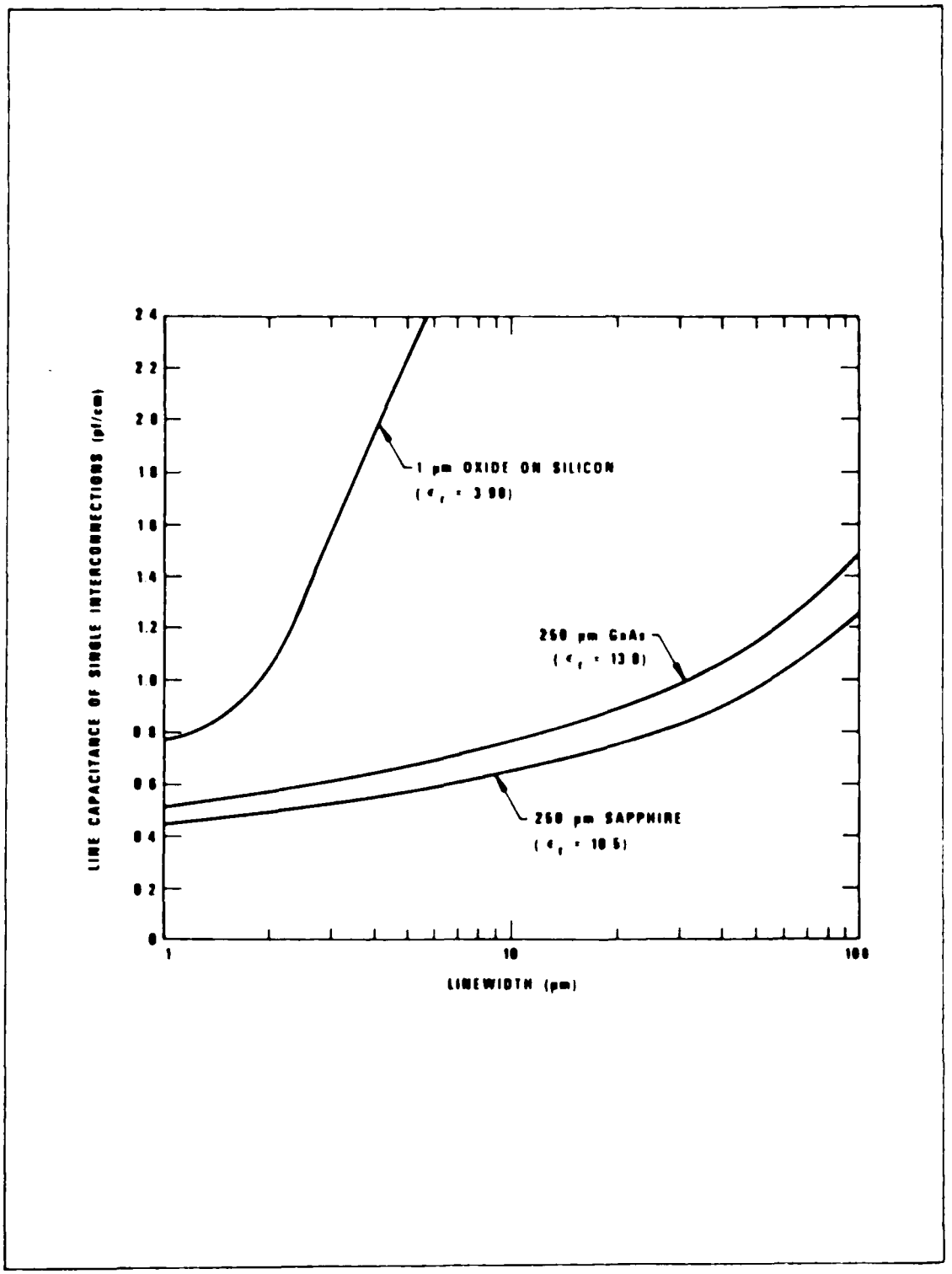

Figure 2. Distributed Capacitance Versus Line Width for a Single Line (77:270)

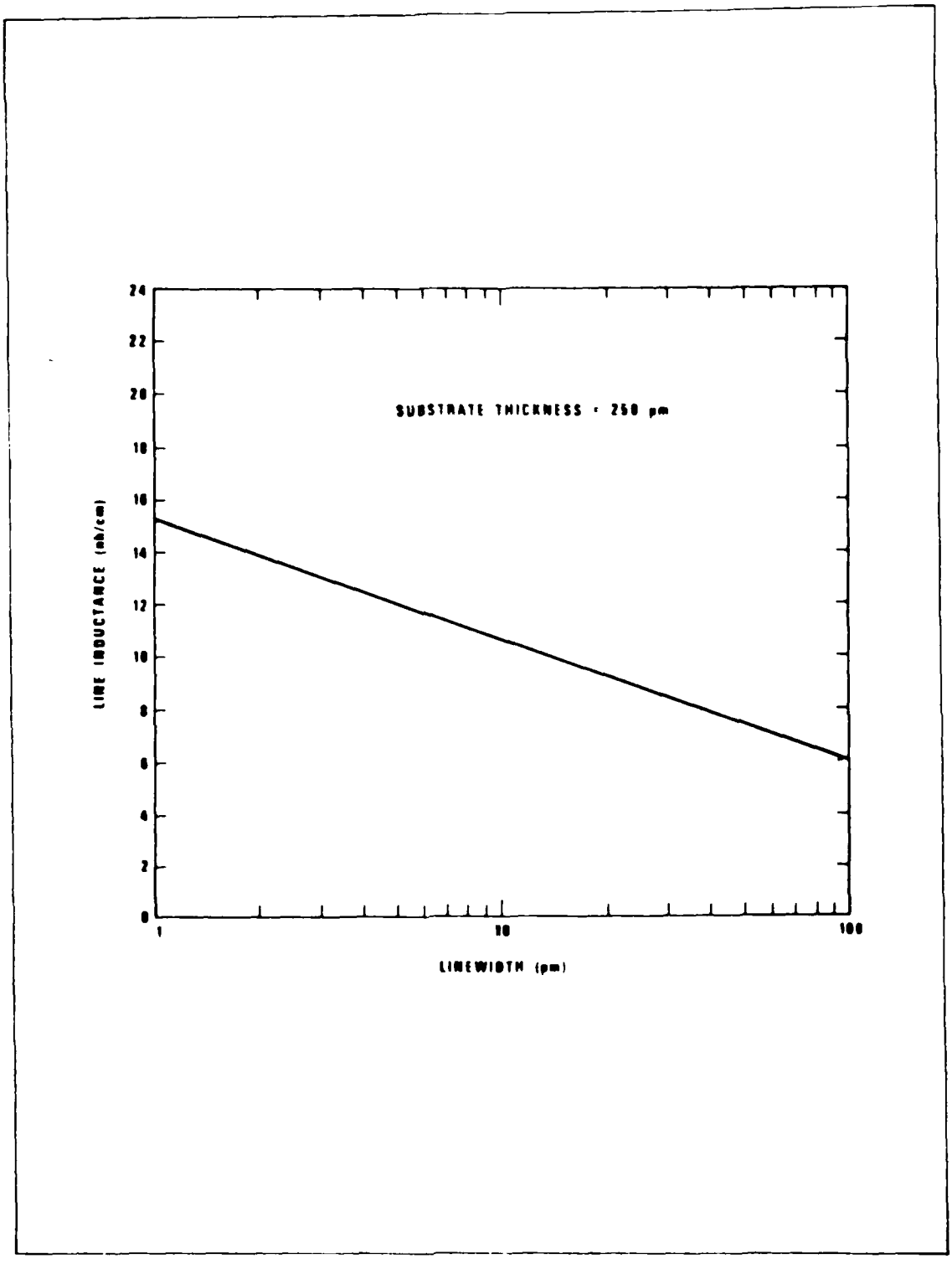

Figure 3. Distributed Inductance Versus Line Width for a Single Line (77:270)

capacitance can be approximated as 50 pF/cm. By direct inspection of Figure 3, the distributed inductance can be estimated as 9 nH/cm for the same linewidth (77:270).

Using Assumption (1), the interconnect resistance (R) is (4:904):

$$R = p \frac{x_o}{A} = p \frac{x_o}{(w)(d)} \quad \text{(ohms)} \tag{2}$$

where

p = resistivity of the interconnect conductor (ohm-cm)
A = cross-sectional area of the interconnect conductor (cm^2)
x_o = length of the interconnect conductor (cm)
w^o = width of the interconnect conductor (cm)
d = thickness of the interconnect conductor (cm).

The electrical resistivity of evaporated thin-film aluminum is 3.0 micro-ohms-cm; therefore, the resistance for a one centimeter long interconnect of aluminum is approximately 4.0 ohms. By invoking Assumption (2), the distributed resistance (r) becomes 4.0 ohms/cm.

The final parameter, conductance (G), is not easily dealt with because of its frequency-dependence (28:88):

$$G = 2\pi f D C \quad \text{(S,siemens)}, \tag{3}$$

where

D = loss tangent of the dielectric
C = capacitance of the line (farads)
f = frequency (1/second).

By applying Assumption (2) once again, the distributed conductance (g) of the line is:

$$g = 2\pi f D c \quad \text{(S/cm)}, \tag{4}$$

where

c = distributed capacitance of the line (F/cm).

Figure 4 shows how the loss tangent for Selectilux HTR 3-200 varies with frequency. However, the PFA processor will operate at 70 MHz.

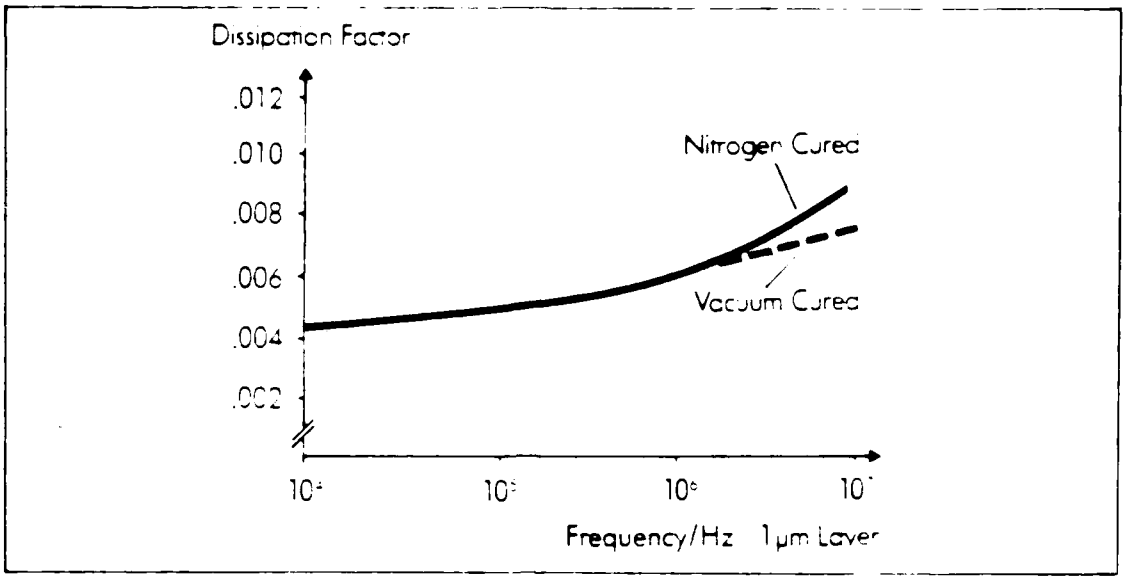

Figure 4. Loss Tangent (Dissipation Factor) Versus Frequency for Selectilux HTR 3-200 (18:27)

Unfortunately, the characteristic does not extend to 70 MHz. However, by extrapolating the curve, an approximate value of 0.014 can be assumed as the maximum loss tangent. This estimate will limit the line conductance to 300 uS/cm at 70 MHz.

Using these approximated parameters, Equation (1) will simplify to an expression retaining only the first two terms on the right-hand side. However, in a survey of many published studies on interconnect propagation delays, all analyses neglected any contribution due to the line conductance (4:904, 17:585, 45:773, 77:269). Only direct current leakage through the dielectric was considered, which is negligable for most practical dielectrics (25:289). However, for this thesis, the validity of this assumption (i.e. Assumption (6)) will have to be verified at frequencies approaching 70 MHz. Nevertheless, to simplify the solution to the differential equation, Assumption (6) will be applied to cancel the

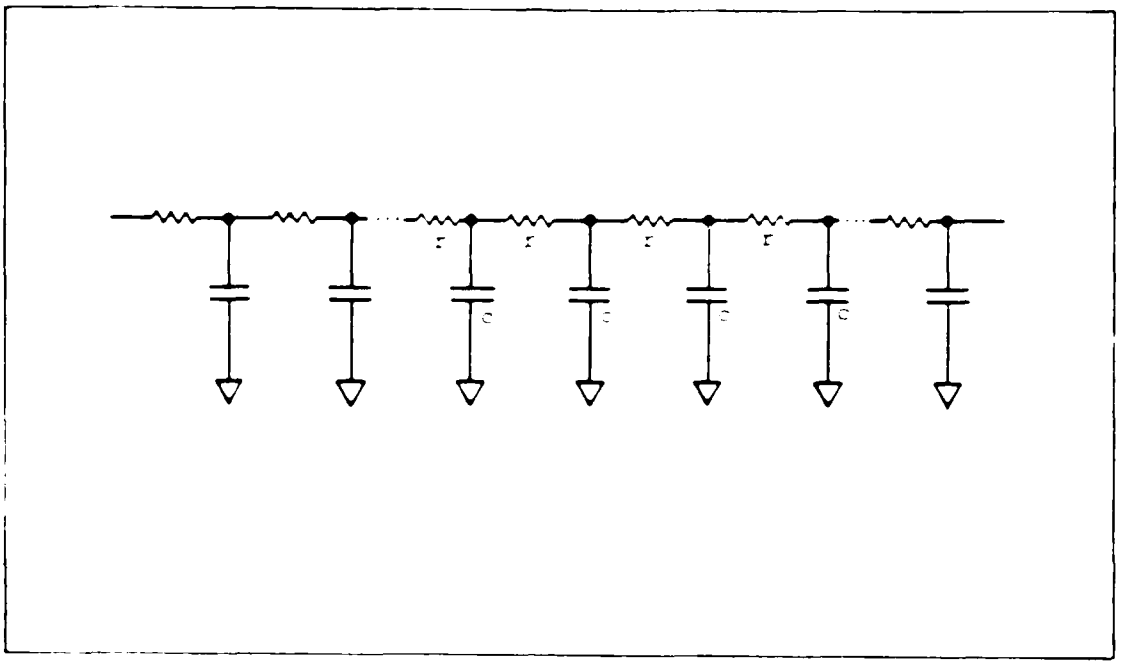

Figure 5. Equivalent Distributed RC Network Model For a Transmission Line (74:132). Shown are the distributed resistance (r), and the distributed capacitance (c).

first term as well. Therefore, the interconnect becomes a distributed RC network (Figure 5), and Equation (1) reduces to:

$$\frac{d^2V}{dx^2} = rc\,\frac{dV}{dt} \tag{5}$$

which is the form of the well-known diffusion equation.

To find the time delay (t_d), Equation (5) can be solved for V using a discrete analysis. Let the following boundary conditions be applied to the interconnect (9:94-101):

(i) At $t < 0$, $V(x) = 0$ for $0 \leq x \leq x_o$,
(ii) At $t = 0$, $V = V_o$ at $x = 0$, and
(iii) At $t = t_d$, $V = 0.63\ V_o$ at $x = x_o$,

where

x_o = the path length of the interconnect (cm).

Applying these boundary conditions to the solution for Equation (5), the time delay can be derived (74:133):

$$t_d = rc \frac{x_o^2}{2}. \tag{6}$$

Weste and Eshraghian based this definition of the time delay on the assumption that "the time taken for a signal to reach 63 percent of its final value approximates the switching point of an inverter" (74:134).

Therefore, the propagation delay can be calculated from just two of the distributed line parameters. Under the conditions of Assumption (2), the distributed resistance can be accurately calculated from Equation (2). Sakurai and Tamaru derived an expression for the capacitance of a line accurate to within 10 percent for $0.3 < w/h < 10$, $0.3 < d/h < 10$, and $0.5 < s/h < 10$ (60:184):

$$\frac{c}{\epsilon_o \epsilon_r} = 1.15\left(\frac{w}{h}\right) + .80\left(\frac{d}{h}\right)^{0.222} + \left[0.06\left(\frac{w}{h}\right) + 1.66\left(\frac{d}{h}\right)^{0.222} - 0.14\left(\frac{d}{h}\right)^{0.222}\right]\left(\frac{s}{h}\right)^{-1.34} \tag{7}$$

where

- h = dielectric thickness between the conductor and the ground plane (silicon) (cm)
- w = line width (cm)
- s = separation between adjacent lines (cm)
- d = conductor thickness (cm)
- ϵ_r = relative permittivity of the oxide material
- ϵ_o = permittivity of free space (F/cm).

The first term of Equation (7) is the capacitance of the upper and lower surfaces of an isolated interconnect (C1), and the second term corresponds to the sidewall contributions of the isolated interconnect (C2). The final term is due to the coupling capacitance with the neighboring lines (C3) (See Figure 6) (4:904;60:184).

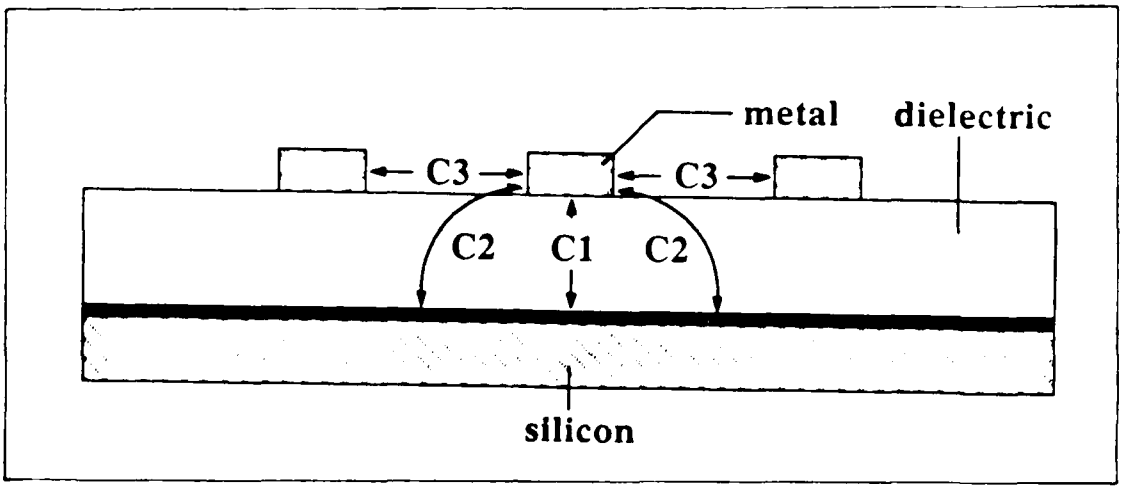

Figure 6. Capacitances of an Interconnect Flanked by Two Parallel Interconnects. Highlighted are the capacitance of the upper and lower surfaces of the isolated interconnect (C1), the sidewall contributions of the isolated interconnect (C2), and the coupling capacitance with the neighboring lines (C3) (60:183).

Variations on the Simplified Delay Expression. Within a circuit, the interconnect delay will be affected by parasitics from the driving transistor at the line input and the load transistor at the line output. These parasitics are the channel resistance (R_{tr}) contributed by the driving transistor, and the gate capacitance contributed by the load transistor (Figure 7). The channel resistance of the driving transistor can be calculated as (4:904):

$$R_{tr} = \frac{L_{tr}/W_{tr}}{u_c \, Cg \, V_{dd}} \tag{8}$$

where

L_{tr} = channel length of the transistor (cm)
W_{tr} = channel width of the transistor (cm)
u_c = mobility of majority charge carrier in the channel ($V\text{-}s/cm^2$)
Cg = gate capacitance due to the oxide (F)
V_{dd} = supply voltage (volts).

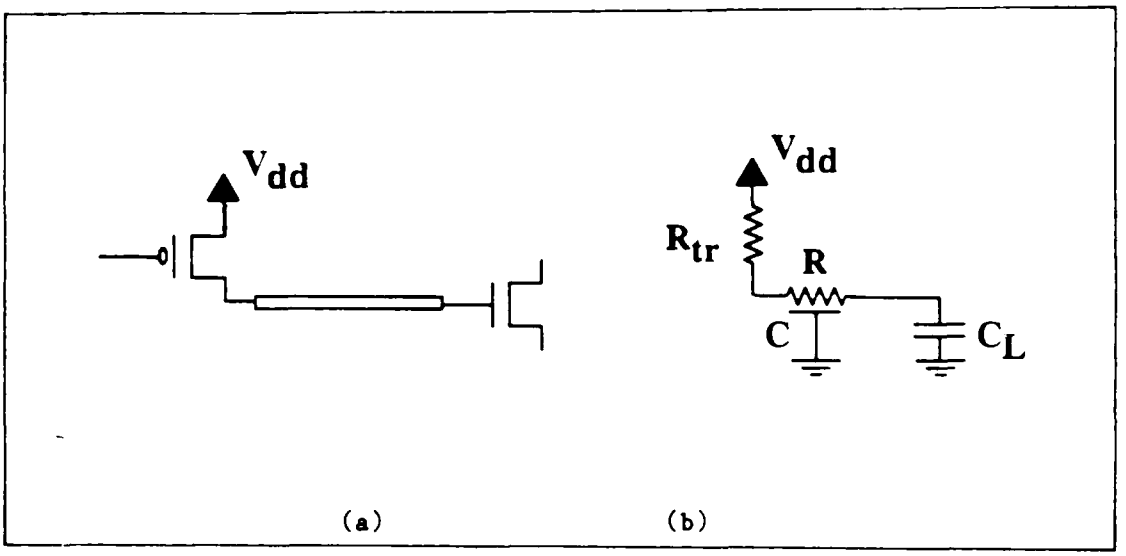

Figure 7. Equivalent Lumped Network with Terminations. (a) Schematic including the driving transistor and the load transistor, (b) Schematic highlighting the channel resistance of the driving transistor (R_{tr}), the gate capacitance of the load transistor (C_{tr}), the lumped resistance of the interconnect (R), the lumped capacitance of the interconnect (C), and the supply voltage of the circuit (V_{dd}) (4:904).

However, Bakoglu and Mendl considered the gate capacitance of the load transistor to be negligible (4:904). Yuan and his associates introduced an additional term to Equation (6) to account for the channel resistance of the driving transistor (77:273):

$$t_d = R_{tr}C + \frac{R\,C}{2} \tag{9}$$

where

R_{tr} = channel resistance of the driving transistor (ohms)
R^{tr} = lumped resistance of the interconnect (ohms)
C = lumped capacitance of the interconnect (farads).

The second term, which is the delay contributed by the line resistance, has been converted to lumped elements by applying Assumption (2). It should also be noted that Equation (9) represents the time delay for a

step response. This is the time required for the amplitude at the end of the line to reach 50 percent of the input step voltage (77:273).

Equation (6) can be used to predict the behavior of an unterminated line, and Equation (9) can be used to predict the circuit performance when a MOS transistor's gate terminates a line. If delays prove to be unacceptable, improvements can be made by using repeaters in the interconnect circuitry (74:133) or exponentially cascaded drivers (40:773).

More complicated propagation delay expressions have been derived at Stanford University by Bakoglu and Meindl, and at the Toshiba Corporation by Sakurai; however, these expressions are for the rise time of the signal response to a unit step function. The rise time was defined as the time required for the signal to rise from 0 to 90 percent of its final value (4:904,51:421). However, this research effort is focused on defining the time required to drive the gate of a CMOS transistor. Since the gate switching threshold is usually designed at approximately 50 percent of the supply voltage (74:54), the time delay expressions (i.e. Equations (6) and (9)) are more appropriate for this thesis. Nevertheless, the rise-time is a major characterization of signal distortion and may be valuable to observe during actual tests. The major sources of distortion are dispersion and attenuation (41:192). Since dispersion involves propagation delay, it will be considered in the following section.

Dispersion. Previous calculations assumed an ideal non-dispersive medium (i.e. the phase velocity is independent of frequency (36:437)); however, a dispersive medium can appreciably distort pulse waveforms. It should be noted that a periodic pulse train is composed of

a continuous frequency spectrum (i.e. a Fourier spectrum) (46:192). Because the dielectric constant of the material proposed by this thesis increases with frequency (Figure 8), each frequency component in the spectrum will be affected by a unique line capacitance (see Equation (7)). Higher frequencies will see a larger dielectric constant, and thus, a higher capacitance. Lower frequencies will experience a smaller dielectric constant, and thus, a lower capacitance (41:193). By Equation (6), this variation in capacitance will produce a longer delay time for the higher frequency components. Consequently, a propagating pulse will be distorted, since the low-frequency components lead the high-frequency components (Figure 9).

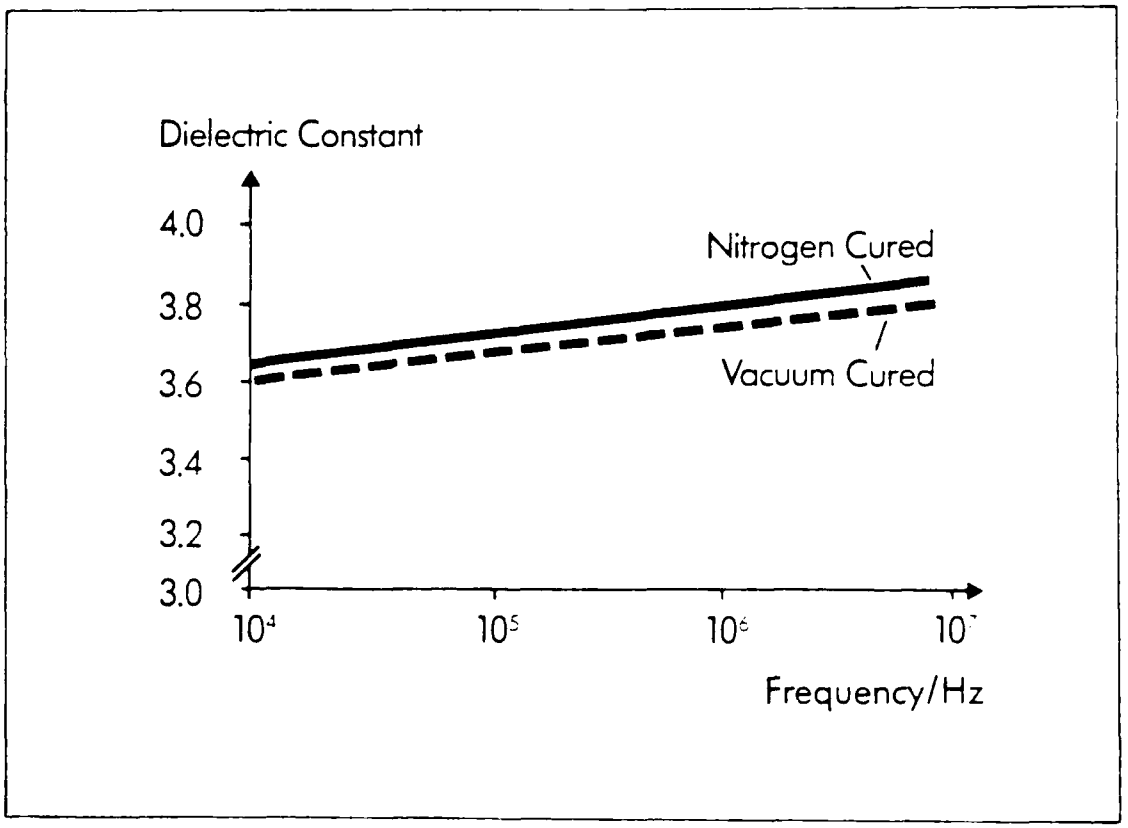

Figure 8. Dielectric Constant vs. Frequency for Selectilux HTR 3-200 (18:27).

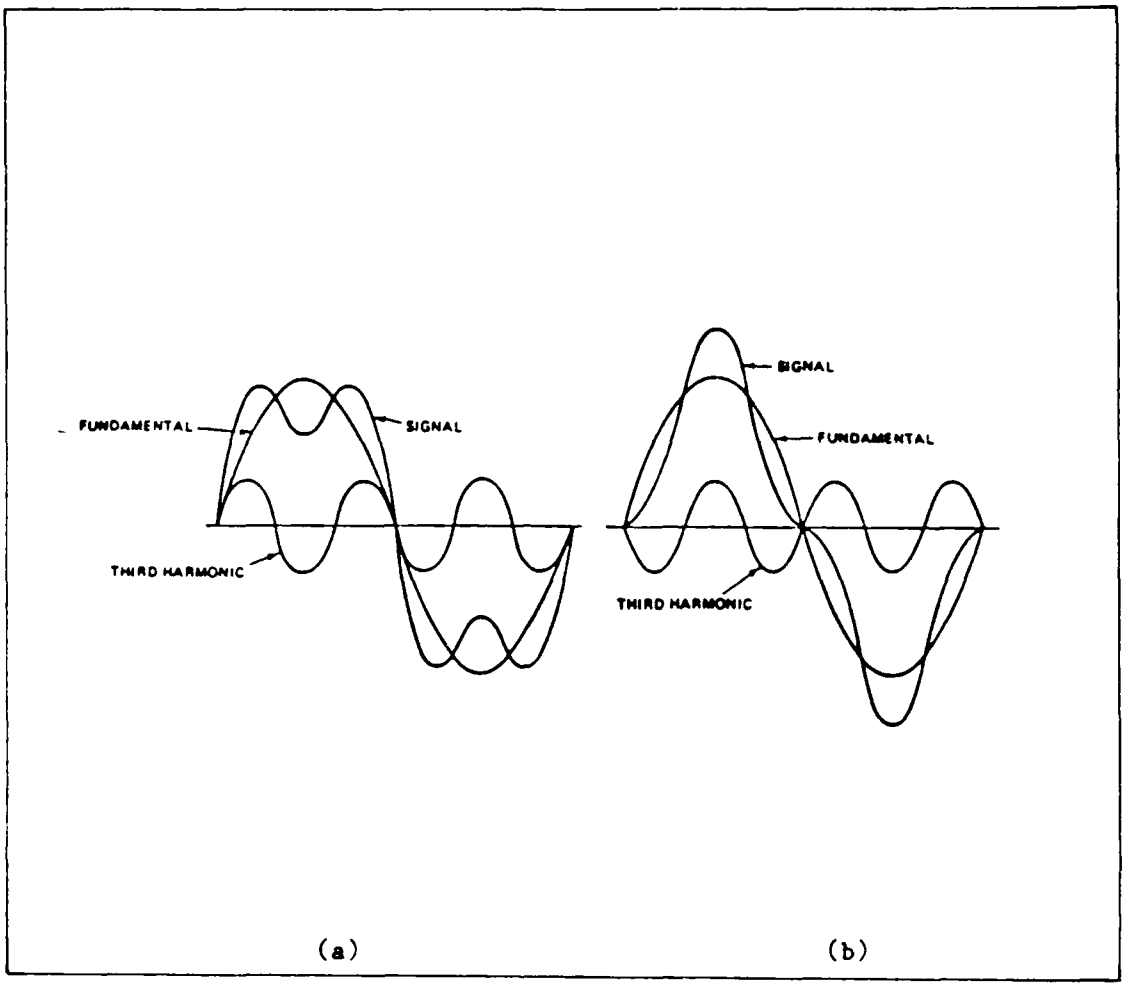

Figure 9. Signal Distortion Due to Dispersion. (a) At t = 0, the fundamental and third harmonic contributing to the pulsed signal, (b) At t > 0, the third harmonic shifted -180° with respect to the fundamental. As a result, this signal is significantly distorted (35).

In this section, the delay and distortion of signals propagating on an interconnect have been examined. In the following section, the second major cause of signal distortion, attenuation, will be presented.

Attenuation. Large levels of attenuation can cause signals to unintentionally cross the switching threshold of the transistor's gate at the interconnect output, severely impairing circuit operation. In order

to determine the influence of attenuation on performance, the loss mechanisms associated with three modes of attenuation will be addressed. First, direct current losses, as predicted by Ohm's Law, will be reviewed. Next, high frequency losses will be modeled by stripline equations. Finally, the high frequency distortion limit associated with the skin effect will be discussed.

Low Frequency Losses. Significantly below microwave frequencies, attenuation is caused by a differential voltage determined by the bulk resistance and the current in the interconnect. This is predicted by the well known equation for Ohm's Law, V=IR. The bulk resistance (R) can be simply evaluated from Equation (2).

High Frequency Losses. However at microwave frequencies, electrostatic and electromagnetic effects prevail, preventing a simple application of Ohm's Law. As previously noted from Equation (4), the line conductance can be appreciable at high frequencies. The conductance represents the current leakage through the dielectric from one conductor to another, which results in losses similar to those resulting from ohmic leakage. Analogously phrased, resistance "represents the imperfection in the conductor", and conductance "represents the imperfection in the dielectric" (30:6). And at high frequencies, both must be considered as contributors to the total line loss (a_T) (3:91):

$$a_T = a_d + a_c \quad (dB/cm) \tag{10}$$

where

a_d = dielectric loss (dB/cm)
a_c = conductor loss (dB/cm).

In 1986, a joint research effort performed by members of Rensselaer Polytechnic Institute (RPI), General Electric (GE) Corporation, and IBM,

used a stripline geometry to analyze high-frequency attenuation in wafer-scale interconnects. They concluded that the following requirement must be met to minimize rise time degradation (42:3129):

$$(d)(b) >> p\,\epsilon_o\sqrt{\epsilon_r}\,x_o\,c_o \qquad (11)$$

where

d = conductor thickness (cm)
h = dielectric thickness (cm)
b = separation between ground planes (cm)
p = resistivity of the metal conductor (ohm-cm)
ϵ_o = permittivity of free space (8.85×10^{-14} F/cm)
ϵ_r = relative permittivity of the dielectric
x_o = path length of the conductor (cm)
c_o = speed of light in free space (3.00×10^{10} cm/s).

Given the stripline geometry depicted in Figure 10, a one-centimeter interconnect path length, and the geometrical parameters proposed in Table 1, Equation (11) would not be satisfied. Therefore, the signal rise-time delay will likely result in significant attenuation. The following sections will examine stripline equations to predict the magnitude of attenuation for the proposed geometrical parameters. This approach is extremely convenient, since well-established equations, for both dielectric and conductor loss, have been formulated and empirically proven for striplines.

Dielectric Loss. As with conductance (see Equation (4)), the dielectric loss is empirically dependent upon the loss tangent of the dielectric material and the frequency of operation (3:91):

$$a_d = \frac{27.3\sqrt{\epsilon_r}\,D}{\lambda_o} = \frac{27.3\sqrt{\epsilon_r}\,f\,D}{c_o} \quad \text{(dB/cm)} \qquad (12)$$

where

ϵ_r = relative permittivity of the dielectric
D = loss tangent of the dielectric
λ_o = wavelength in free space (cm)
f = frequency of operation (Hz)
c_o = speed of light in free space (3.00×10^{10} cm/s).

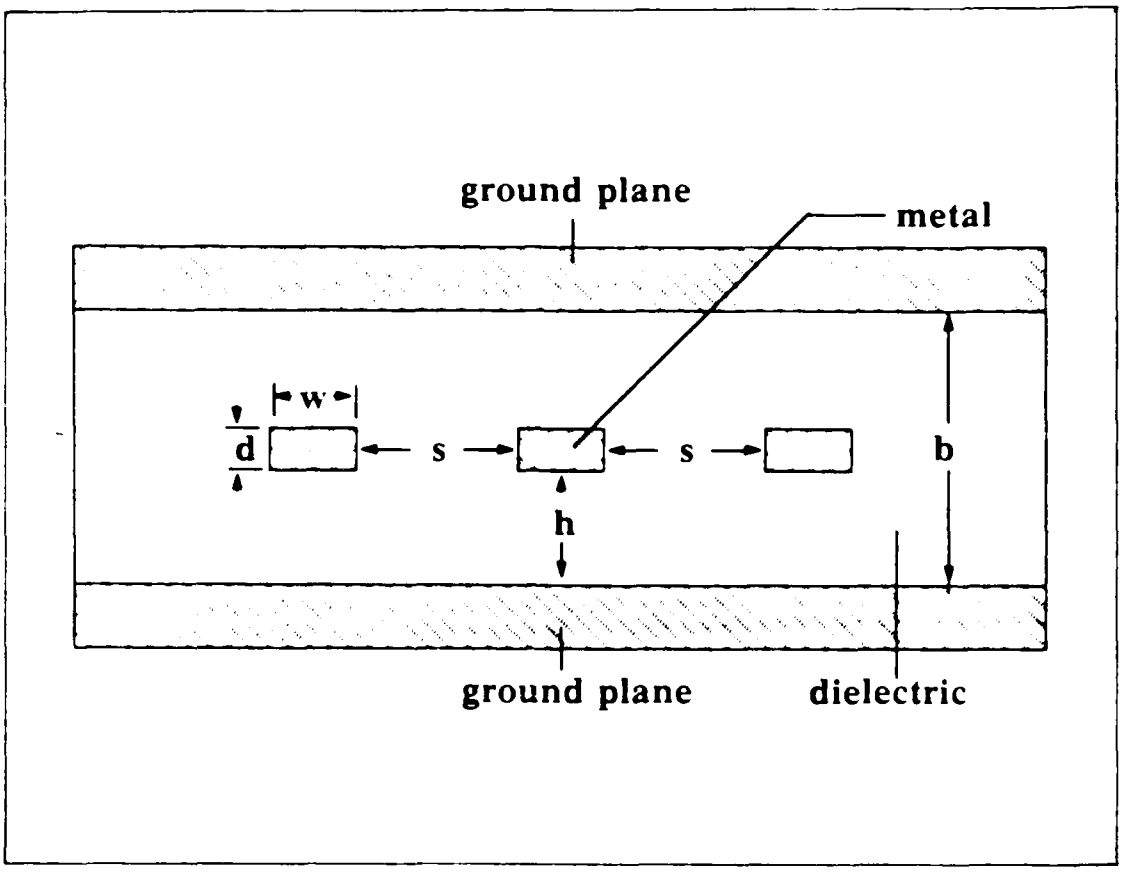

Figure 10. Cross-section of a Stripline Structure. Highlighted are the conductor thickness (d), the conductor width (w), the dielectric thickness between the conductor and the ground plane (h), the ground plane separation (b), and the conductor separation (s).

Conductor Loss. It is obvious, by inference, that conductor loss is dependent upon the properties of the stripline conductor; however, the relationship between conductor loss and the properties of the dielectric may not be as apparent. At high frequencies, conductor loss is influenced by the incremental inductance associated with the magnetic flux passing through the dielectric into the conductor (3:91). Therefore, empirical expressions for conductor loss can be very extensive. For the geometry proposed in Table 1, the expression for the

wide center strip case (i.e. w/b > 0.35 and negligible fringe field interaction is assumed) is most applicable (26:17):

$$\alpha_c = \frac{2.02 \times 10^{-6} \epsilon_r [f(GHz)]^{1/2} Z_o}{b} \left[\frac{1}{1 - d/b} + \frac{2\, w/b}{(1 - d/b)^2} + \left(\frac{1 + d/b}{\pi (1 - d/b)^2} \right) \ln \left(\frac{\frac{1}{1 - d/b} + 1}{\frac{1}{1 - d/b} - 1} \right) \right] \quad (dB/cm) \tag{13}$$

where

b = separation between ground planes (cm)
$f(GHz)$ = frequency (GHz)
d = thickness of the conductor (cm)
w = width of the conductor (cm)
Z_o = characteristic impedance of the line (cm).

The characteristic impedance (Z_o) of the line is empirically defined as (26:35):

$$Z_o = \frac{1}{\sqrt{\epsilon_r}} \frac{94.15}{\frac{w/b}{1 - d/b} + \frac{C'}{0.0885\, \epsilon_r}} \quad (ohms) \tag{14}$$

where

ϵ_r = relative permittivity of the dielectric

and

$$C' = \frac{0.0885\, \epsilon_r}{\pi} \left[\frac{2}{1 - d/b} \ln \left(\frac{1}{1 - d/b} + 1 \right) - \left(\frac{1}{1 - d/b} - 1 \right) \ln \left(\frac{1}{(1 - d/b)^2} - 1 \right) \right] \quad (pF/cm), \tag{15}$$

Knowing when to apply either low or high frequency loss equations requires an understanding of the skin effect. The following section explains the skin effect phenomenon and derives the demarcation frequency at which this effect becomes appreciable.

Skin Effect. Bulk resistance is applicable when the current in the interconnect is uniformly distributed throughout its entire

cross-sectional area. Although this characteristic is generally true for low frequency signals, with increasing frequency, the current becomes more concentrated at the surface of the conductor. Because current is limited to flow through a small area of the conductor's cross-section, the effective resistance of the conductor is increased. This phenomenon, known as the skin effect, can best be understood by modeling the interconnect as a collection of infinitesimally thin parallel strands (Figure 11). By adding a time-varying component to the current signal, each strand will contribute a reactive component to the impedance with respect to the nearest neighbor strands. An additional voltage drop is induced in the strands due to the inductive reactance. However, strands at the outer surface of the interconnect are inductively coupled to fewer

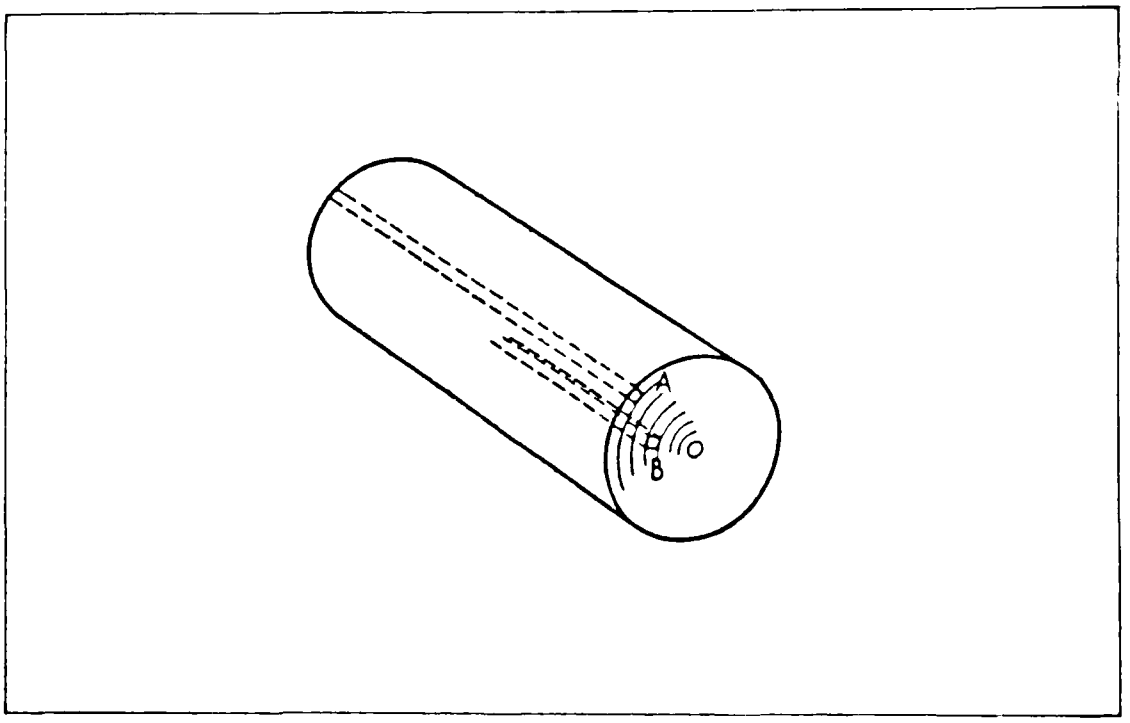

Figure 11. Interconnect Modeled By Infinitesimal Parallel Strands. The strand A is inductively coupled to fewer strands than strand B (60:139)

strands than those in the interior. Therefore, the impedance of the interconnect is smaller at the surface. If the potential across the entire cross-section of the interconnect is the same, then the current in the interconnect must be higher at the surface to compensate for the lower impedance (75:139-140).

A useful parameter to determine the impact of the skin effect is the skin depth (δ) (41:449):

$$\delta = \sqrt{\frac{p}{f \pi u}} \quad \text{(cm)} \tag{16}$$

where

p = the resistivity of the metal conductor (ohm-cm)
f = the frequency of operation (Hz)
u = the permeability of the metal conductor (H/cm).

The surface current density is approximately 2.7 times as great as the current density at a depth inside the surface. The current continues to decrease exponentially deeper into the conductor (75:146).

The "skin-resistance" increases with the square root of frequency. For a given frequency, the series resistance and reactive components introduced by the skin effect will be equal in magnitude (41:194). The resistive component is equal to the direct current resistance of the conductor with a thickness equal to the skin depth. Using Equation (2), the distributed resistance introduced by the skin effect (r_{sk}) is (36:69):

$$r_{sk} = \frac{p}{w \delta} \quad \text{(ohm/cm)} \tag{17}$$

where

w = the width of the conductor (cm).

By substituting Equation (16) into Equation (17), the relationship between skin resistance and frequency becomes:

$$r_{sk} = \frac{1}{w}\sqrt{\pi f p u} \quad \text{(ohm/cm)}. \tag{18}$$

As mentioned earlier, the skin-resistance can be ignored for frequencies below a certain cut-off. Magnusson stated that the line resistance can be approximated by the direct current resistance (Equation (2)) as long as the "skin-effect resistance ratio" is less than unity (39:381). This quantity is simply the ratio of Equation (18) and Equation (2):

$$\frac{r_{sk}}{r} = \sqrt{\frac{\pi f u d^2}{p}} \tag{19}$$

where d = thickness of the conductor (cm).

The point at which the skin-resistance becomes appreciable is known as the "skin-effect-demarcation frequency" (f_{sk}) (39:382). This frequency (f_{sk}) can be found by setting the skin-effect resistance ratio to unity and solving Equation (19) for f:

$$f_{sk} = \sqrt{\frac{p}{\pi u d^2}} \quad \text{(Hz)}. \tag{20}$$

For the aluminum conductor geometry (that is, d = 1.2 um) proposed in Table 1, this cut-off frequency is 4.6 GHz. Frequency components above this frequency will be attenuated more than those below it. Therefore, the higher frequency components producing the sharp edge of a pulse will be attenuated, resulting in a slower rise-time. However, the skin-effect can be ignored if the bandwidth of the pulse signal lies below this demarcation frequency (41:199).

The thickness of the conductor can be reduced to limit the distortion caused by the skin-effect. In fact, the 1986 joint research team from

RPI, GE and IBM suggested that second-level lines should be made thinner to reduce skin-effect distortion. Since second-level lines are usually much shorter than first-metal lines, the increased bulk resistance caused by thinner lines should be negligible (42:3130).

This section has addressed the mechanisms attending attenuation in interconnects. The immediate difficulties caused by attenuation are reduced noise margins.

Noise. Electrical noise is defined as any undesirable signal impeding the reception of desirable information (13:1). If the noise levels are allowed to surpass the input noise margins of the load transistor, erroneous information can pass through an interconnect (74:52). This section examines how levels of critical noise sources can be managed. The noise signals affecting the construction of wafer-scale interconnects are crosstalk, power surges, and signal reflections.

Crosstalk. Crosstalk is noise due to electrostatic and electromagnetic coupling between adjacent interconnects. The strength of this coupling is represented by the parameters of mutual inductance and capacitance. In this section, these parameters will be explained using the fundamental links between field and circuit theory. Next, a method of predicting the strength of this coupling will be presented as a function of the interconnect geometry.

Mutual Inductance and Capacitance. The concept of mutual inductance is derived from a combination of the Biot-Savart Law and Faraday's Law. The Biot-Savart Law establishes that magnetic fields are created by current carrying elements, and the magnitude of this field decreases inversely with the square of the distance from the element (36:152). Therefore, a time-varying current in a neighboring line will

produce a time-varying magnetic field. Faraday's Law links this time varying magnetic field with an induced electromotive force in a neighboring line (36:366,375):

$$V_{ind} = \oint \bar{E} \cdot d\bar{x} = -\int_s u \frac{d\bar{H}}{dt} \cdot d\bar{s} \quad \text{(volts)} \tag{21}$$

where

V_{in} = induced electromotive force across the neighboring line (V)
$\bar{E}$ = electric field induced across dx of the neighboring line (V/cm)
$\bar{H}$ = magnetic field due to the Biot-Savart Law (Wb/cm)
$\bar{x}$ = path of integration along the neighboring line (cm)
u = permeability of the dielectric (H/cm)
$\bar{s}$ = surface bounded by the current-carrying circuit (cm^2)
t = time (seconds).

The mutual inductance (L_{12}) directly relates the time-varying current (I_1) in one line to the induced emf in the neighboring line (V_2) (36:336):

$$V_2 = L_{12} \frac{dI_1}{dt} \quad \text{(volts)}. \tag{22}$$

In a similar manner, the fact that electric fields are produced by voltage gradients (that is, $\bar{E} = -\nabla V$) (36:32) combines with Ampere's Law to create the concept of mutual capacitance (C_{12}).

The noise due to crosstalk is the superposition of these induced voltages and currents upon the signals transmitted on the neighboring line. Because the strength of these voltages and currents differ along the length of the interconnect, distributed parameters must be used to determine their values at any point (x) along the neighboring line (Figure 12). Using the Laplacian notation, Equation (22) and its capacitive analogy become (1:2)

$$\Delta V_2(x) = s\, L_{12}\, I_1(x)\, \Delta x \tag{23a}$$

$$\Delta I_2(x) = s\, C_{12}\, V_1(x)\, \Delta x \tag{23b}$$

where

ΔV ( ) = induced voltage at (volts)

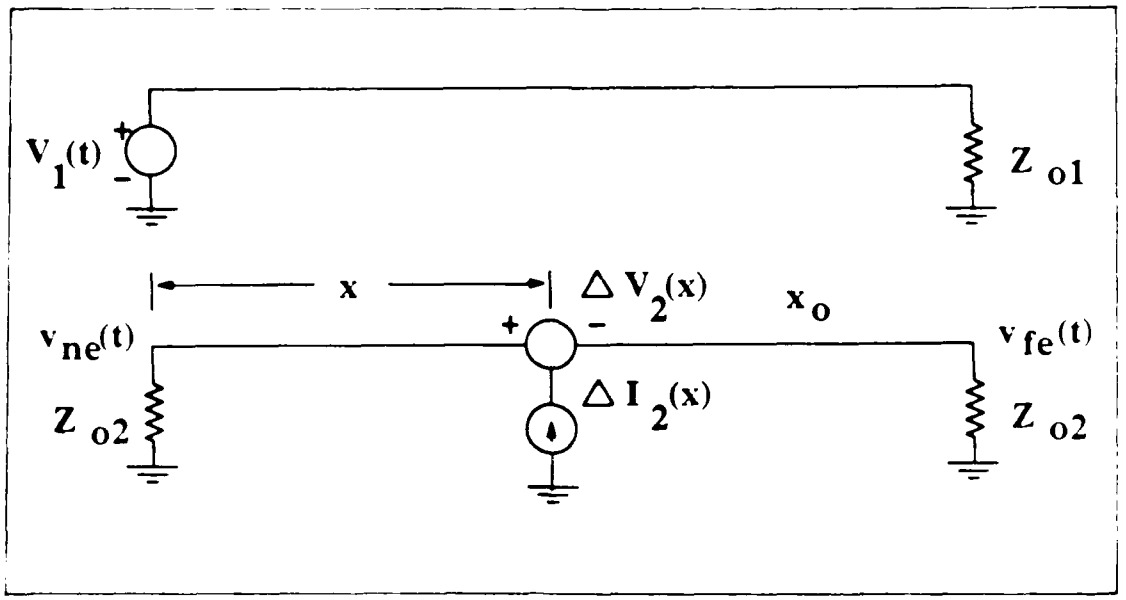

Figure 12. Circuit With Crosstalk. The voltage driven on the active line ($V_1(t)$) induces a voltage ($\Delta V_2(x)$) and current ($\Delta I_2(x)$) inserted on the quiet line at x (i.e. no voltage is driven on the line). Given that the two lines are terminated by their own characteristic impedances (Z_{o1} and Z_{o2}), the near-end noise ($v_{ne}(t)$) can be measured on the quiet line at x = 0, and the far-end noise ($v_{fe}(t)$) can be measured on the quiet line at $x = x_o$ (1:3).

$\Delta I_2(x)$ = induced current at x (amperes)
L_{12} = distributed mutual inductance between the two lines (H/cm)
C_{12} = distributed mutual capacitance between the two lines (F/cm)
$V_1(x)$ = voltage in the active line at point x (volts)
$I_1(x)$ = current in the active line at point x (amperes)
Δx = incremental distance about x along the quiet line (cm)
s = the Laplacian variable (1/seconds).

Coupled Noise Prediction. In practice, the noise measurements of greatest interest are the near-end noise [$v_{ne}(t)$] and the far-end noise [$v_{fe}(t)$] (See Figure 12). Near-end noise, measured at the input of the line (x=0), and far-end noise, taken at the output of the line ($x=x_o$), can be predicted given the assumptions made in the previous sections of this thesis. Specifically, the lines must be loosely coupled (Assumption (2)). This situation seems reasonable since it is desirable

to keep the levels of crosstalk as low as possible (27:481). In addition, both lines must be in an homogeneous medium (Assumption (3)). This assumption simplifies calculations by making the coefficient of capacitive coupling (K_C) equal to the coefficient of inductive coupling (K_L) (1:4). Given these assumptions, the near-end and far-end noise signals can be represented in the Laplace domain by (1:5):

$$V_{ne}(s) = \frac{V_1}{4} K_L (1 + \alpha) [1 - \exp(-2st_d)] \tag{24a}$$

$$V_{fe}(s) = \frac{-V_1}{2} K_L (1 - \alpha) st_d \exp(-st_d) \tag{24b}$$

where

V_1 = Laplace transform of the input signal $[v_1(t)]$ on the adjacent line
K_L = inductive coupling coefficient
α = a constant of proportionality relating K_C to K_L, $\alpha = K_C/K_L$
t_d = delay in the line
s = Laplacian variable.

Equation 24 may be applied by first constructing a piecewise linear approximation of the input signal $[v_1(t)]$. Then the approximation can be used to derive the Laplace transform of $v_1(t)$ $[V_1]$ (Figure 13). The inductive coupling coefficient can be calculated by using the Geometric Mean Distance (GMD) theory (1:5):

$$K_L = \frac{(\ln D_{12},)(\ln D_{12})}{[\ln(D_{11},/D_{11}) \ln(D_{22},/D_{22})]^{1/2}} \tag{25}$$

where D_{11} and D_{22} are the self GMDs of the active and quiet line, respectively,
D_{11}, and D_{22}, are the GMDs of the active and quiet lines with their images, respectively (Figure 14),
D_{12} is the GMD of the quiet and active line, and
D_{12}, is the GMD of the active line and the image of the quiet line.

(The equations for GMD calculations are detailed in Appendix A.) The time

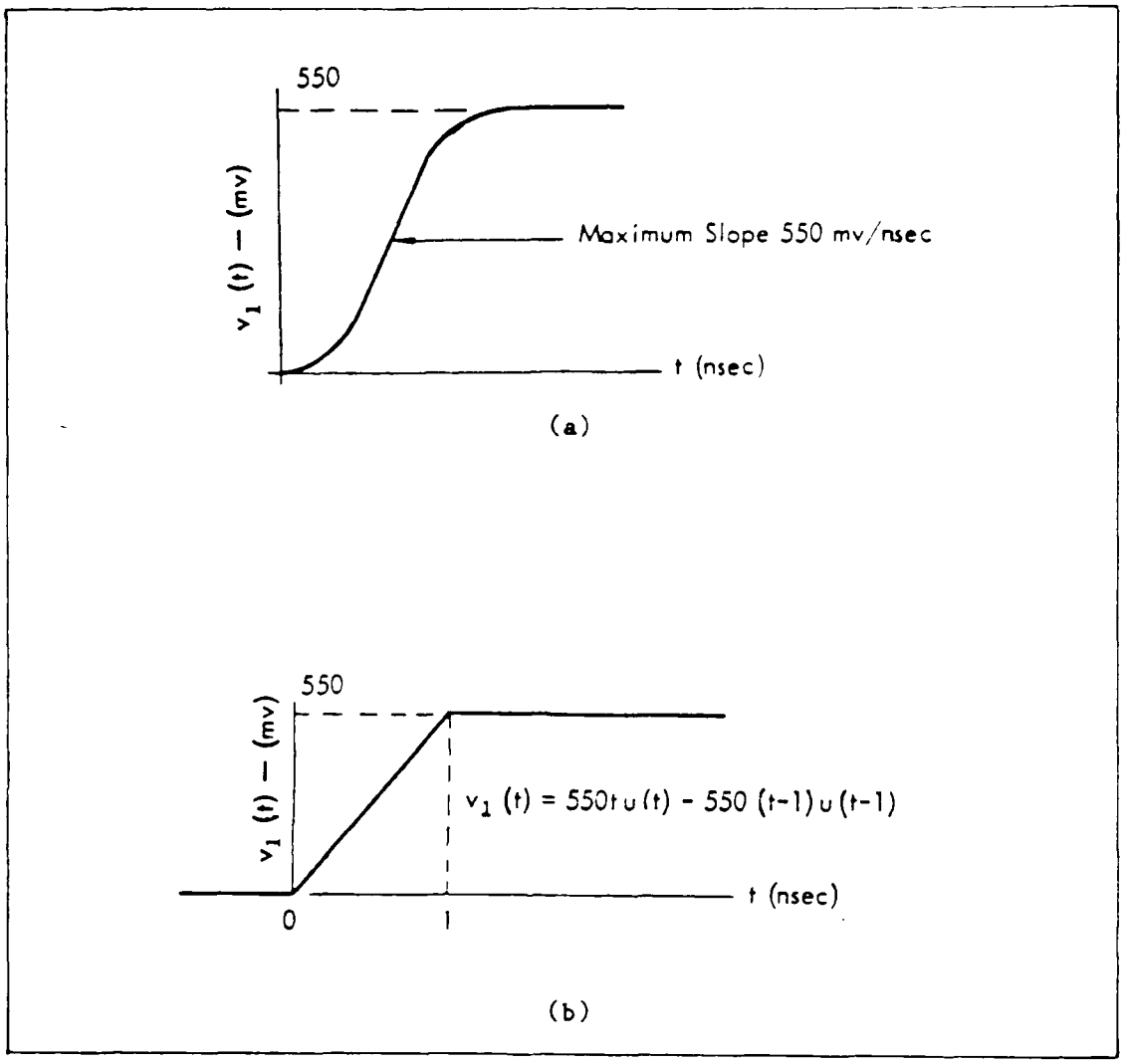

Figure 13. Piecewise Construction Deriving the Laplace Transform. The actual plot (a) of a step voltage input ($v_1(t)$), and the piecewise linear construction (b) of $v_1(t)$ (1:9)

delay of the lines can be calculated using the method described in the previous section. The time domain response of the near-end noise on the quiet line can be found by substituting these calculations into Equation (24) and taking the inverse Laplace transform (1:8-10).

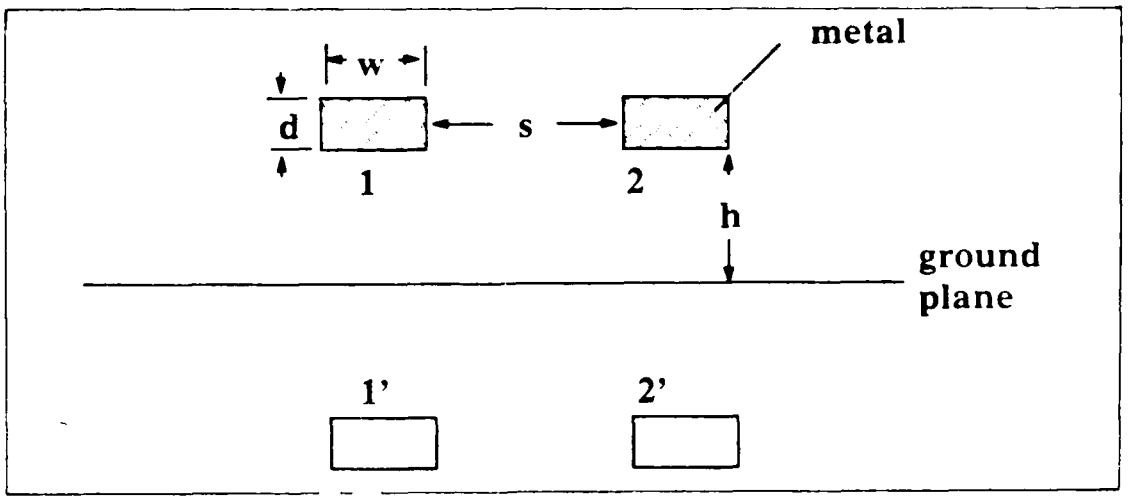

Figure 14. Two Parallel Lines (1 and 2) and Their Images (1' and 2') (1:5).

In addition, it should be noted that coupling between layers of metal can be shielded by fabricating interlayer ground planes (14:58).

Power Surges. Power supply noise is caused by sudden large current surges in the system. Sources of these current surges are precharged circuit blocks (i.e. programmable logic arrays and dynamic random access memory) and I/O switching (e.g. large buffers to drive wafer-scale interconnects) (74:491). The wafer-scale construction can be configured to limit this noise by introducing a large capacitance between power and ground. In 1986, Donlan and others at Rensellaer Polytechnic Institute (RPI) proposed parallel power and ground planes over the entire surface of the wafer. By introducing a thin dielectric material with a large relative permittivity between the two planes, a large bypass capacitance could be created to supress power supply transients (14:55).

Signal Reflections. For an infinite transmission line, two independent solutions can be derived from the general solution of the transmission line equations (Equation 1) (36:383). Both solutions are

travelling waves propagating in opposite directions with the same speed. For a terminated transmission line, the positive travelling wave (V_i) is called the incident wave, and the negative travelling wave (V_o) is called the reflected wave (Figure 15) (23:5).

If the reflected wave amplitute is large, it can significantly degrade the quality of the incident signal. The amplitude of the reflected wave is related to the incident wave amplitude by the reflection coefficient [$\Gamma(x)$] (23:8):

$$\Gamma(x) = \frac{V_i(x)}{V_o(x)}. \tag{26}$$

The output reflection coefficient (Γ_o) is related to the characteristic (Z_o) and load (Z_L) impedances of the line (23:8):

$$\Gamma_o = \frac{Z_L - Z_o}{Z_L + Z_o}. \tag{27}$$

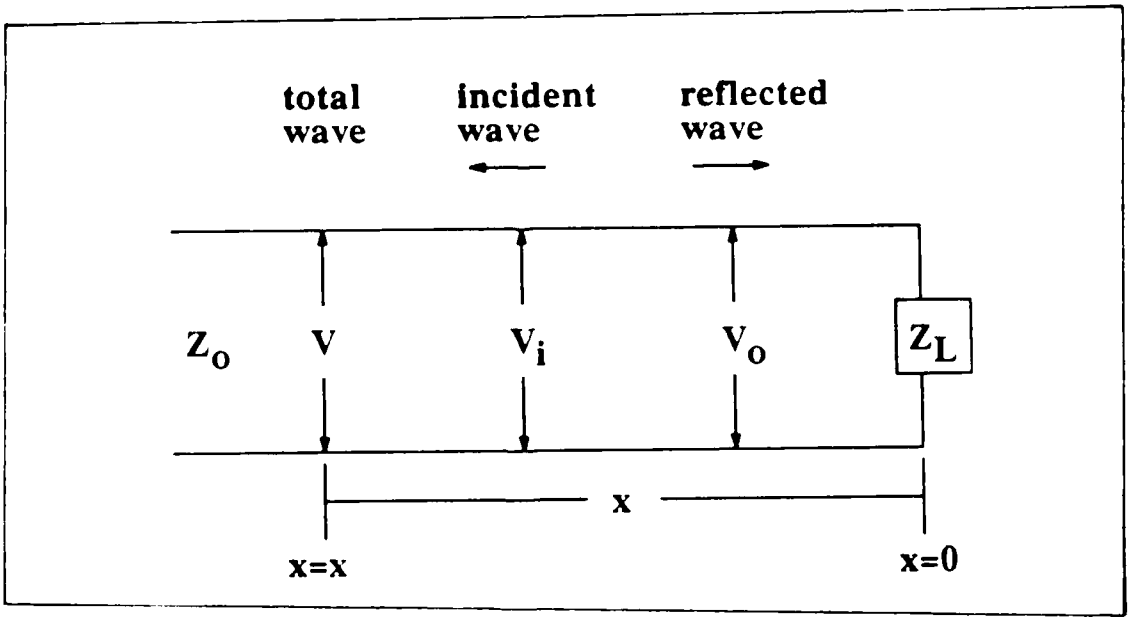

Figure 15. Incident and Reflected Waves on a Transmission Line (36:402)

Due to losses in the line the reflected wave amplitude is greatest at the output of the line. Therefore, the calculation of Equation 27 will determine the worst case reflection. As can be noted from this equation, reflections can be eliminated by terminating the line with a matched impedance (that is, $Z_o = Z_L$).

Summary. Three electrical performance factors have been related to the material and geometrical parameters of an interconnect. Hence, fabrication materials and structural geometries can be recommended to optimize the electrical performance of wafer-scale interconnects. However, there are additional fabrication limitations that will not permit an optimal theoretical approach to be taken. In the following section, these restraints will be highlighted as they influence the situation.

Candidate Structure

The materials chosen for the candidate structure are aluminum for the conductor metal, and polyimide for the intermetal dielectric. The following section seeks to justify this choice of materials, given certain electrical and processing criteria. Next, the line geometry proposed in Table 1 will be supported using electrical performance criteria.

Metal. Several factors must be considered when selecting an appropriate interconnect metal. Gise and Blanchard list several metallization requirements: high electrical conductivity, good adhesion at metal-dielectric and metal-metal interfaces, compatible deposition method with existing structures, uniform step coverage, high electromigration limit, resistance to corrosion, and economical feasibility (22:135).

Along with high conductivity, good adhesion is the most discriminating factor for metal selection. Table 2 lists the four most conductive metals. Although silver, copper, and gold all have lower resistivities, aluminum is the most appropriate material due to its superior adhesion to the proposed polyimide dielectric. Since the activity of a metal depends upon its oxidation potential, high adhesive properties can be attributed to the oxidation potential of a metal (that is, the more negative the potential, the better the metal's adhesion properties) (73:278). Gold and silver have large positive potentials, copper is slightly positive, and aluminum is strongly negative (72:D-151,152). Therefore, gold, silver, and copper should have poor adhesion properties. Indeed, gold (21:450) and copper (73:272) are acknowledged as poorly adhesive metals. Therefore, it seems appropriate to conclude that silver will adhere poorly as well. As predicted, aluminum has excellent adhesion properties (21:446). Since aluminum maintains high conductivity with excellent adhesion to dielectric surfaces, aluminum will be chosen as the metal for this thesis.

Aluminum interconnects can be fabricated to satisfy the remaining criteria as well. Electromigration should not be a concern since the proposed line dimensions are relatively large compared to VLSI structures (See Table 1). Good step coverage may be obtained using the planarization techniques discussed previously, vacuum deposition of aluminum can be performed at temperatures tolerable for polyimide, and fine line photolithography is simply achieved with wet chemical etching. Although the high chemical activity of aluminum does enhance corrosion, the problem can be averted by depositing a passivation layer over the aluminum pattern

Table 2. Electrical Properties of Metals at 20°C (72:F-120)

Material	Resistivity (10^{-6} ohm-cm)	Relative Permeability
Silver	1.586	1.000
Copper	1.678	1.000
Gold	2.240	-----
Aluminum	2.655	1.000

(21:447). Finally, aluminum has an obvious economical advantage compared to silver and gold.

It should be noted that gold interconnects can be fabricated with good adhesion; however, the required process adds significant processing complexity. In 1983, RPI's Sorab Ghandhi stated (21:450):

> ... [Gold] can only be used in a multimetal system, where one or more additional layers are used for adhesion to the insulating layer, as well as the gold. Transition metals such as titanium, chromium, and tantalum have all been used for this purpose.

However, gold and the associated transition metal must be deposited and patterned using separate processing steps, increasing the complexity of the metalization process. Because the circuit die to be integrated in the host silicon wafer will have aluminum pads, the aluminum-gold interface poses additional processing limitations. When heated to about 300°C, gold and aluminum will react to form a number of compounds including a material called the "purple plague". Although this material is conductive, it is often accompanied by a brittle tan colored material that compromises the mechanical contact between gold and aluminum (12:168). Therefore,

aluminum is the preferred conductor material because of its superior performance characteristics and planar IC processing compatibility.

Dielectric. Similar to the choice of metal, the criteria for dielectric selection are varied and complicated. As an intermetal dielectric, the insulator must have excellent electrical properties and physically compatible processing methods. Under thermal cycling, the layer must have mechanical properties that will tolerate stresses in the structure, and the material must conduct heat away from the circuit into the ambient (63:97). To assess materials according to these criteria, Tables 3 and 4 tabulate the critical properties of some popular dielectrics used in integrated circuit fabrication.

Electrically, polyimide and silicon oxide have superior properties. As previously mentioned, an electrically superior dielectric should have a small dielectric constant to reduce signal delays (Equations 6 and 7) and a small loss tangent to lower dielectric losses (Equation 12). Also, for

Table 3. Electrical Properties of Dielectrics

Material	Loss Tangent	Relative Permittivity	Dielectric Breakdown Strength (MV/cm)
Polyimide	0.003-0.007 (b)	3.5 (b)	3 (b)
SiO_2	-----	3.9 (c)	1 - 10 (d)
Silicon	-----	11.9 (a)	0.1 (d)
Si_3N_4	-----	7 - 10 (d)	1 - 10 (d)
Al_2O_3	-----	7 - 9 (d)	0.1 (d)

(a) (63:513) (b) (56:104) (c) (63:195) (d) (75:719)

Table 4. Thermal-Mechanical Properties of Select Materials (75:719)

Material	Coefficient of Thermal Expansion $(1/^{o}C) \times 10^{-6}$	Young's Modulus $(dynes/cm^2) \times 10^{-10}$	Thermal Conductivity $Cal\text{-}s\text{-}^{o}C/cm$
Polyimide	20 - 70	3	4
SiO_2	0.3 - 0.5	74	50
Silicon	2.3	160	720 - 3400
Si_3N_4	2.5 - 3	155	280
Al_2O_3	9	373	780
Al	25	70	5700

VLSI use, the dielectric breakdown field should be in excess of 5 MV/cm (63:97). Based upon the criteria of a small dielectric constant alone, polyimide and silicon oxide are noteworthy (See Table 3). However, polyimide does not have the breakdown field strength required for VLSI use. Nevertheless, for the thick films required for this thesis application, polyimide should be more than satisfactory. Physically, polyimide is simpler to process and more compatible with other silicon processing materials. The dielectric must be fabricated below $450^{o}C$ to avoid damaging underlying aluminum patterns (75:718). As previously cited, polyimide has superior planarization properties at lower reflow temperatures than CVD oxide. Although spin-on glass (SOG) can satisfy these planarization and temperature requirements, it cannot achieve the thickness required for this thesis. Polyimide can be easily deposited by spin-coating, and photosensitive precursors can be patterned in fewer steps than either CVD or spin-on glass.

Mechanically, polyimide should serve adequately as the dielectric material. Wilson stated that the thermally induced stress between materials is directly related to the difference between their thermal coefficient's of expansion (TCE) and the Young's modulus associated with the overcoated material (75:719). Polyimide and aluminum have TCEs with the same order of magnitude; therefore, the thermal stress in the metallization pattern should not be a critical concern. However, the polyimide interface with the thermal oxide is a critical concern. Here the TCEs differ by two orders of magnitude. However, polyimide has the best Young's modulus of the dielectrics listed in Table 4. High stresses that are thermally induced at this interface should be absorbed by the polyimide's elasticity. It should also be noted that cracking in CVD oxide has been observed due to stresses caused by ultrasonic bonding. In contrast, polyimide has been shown to absorb these stresses without cracking (48:465).

Polyimide has some negative thermal qualities. Polyimide does not enhance the circuit's ability to dissipate heat. It can be seen in Table 4 that polyimide is nearly a thermal insulator compared to the silicon substrate. Therefore, any heat dissipated by the circuit must be conducted through the substrate.

Considering the advantages and disadvantages, polyimide will be used as the dielectric material for the prototype structure. Although other dielectric materials are better heat conductors, the electrical and physical advantages of polyimide are preferred considering the objectives of this thesis. However, if the low thermal conductivity or high thermal expansion of polyimide is assessed as a negative performance factor during the tests, alternate materials will be recommended.

Geometries. Based on the electrical criteria presented in this thesis, the optimum geometry will minimize propagation delay, line loss, and signal noise. However, given the materials selected in previous sections and the methods of fabrication available at AFIT, the geometry selection is limited to a certain range of values. Therefore, the criteria can only be applied over a limited range of geometries. The proposed line geometry has been shown previously in Table 1 and will now be justified according to these criteria.

AFIT is equipped with an vaccum thermal evaporation system for depositing thin metal films. The maximum film thickness realized with one cycle of this system is approximately 1.2 microns. Therefore, the conductor runs will be limited to thicknesses below this value. Also, AFIT's photomask production equipment is limited to one mil (approximately 25.4 microns) resolution for non-repeatable patterns. Therefore, line widths and separations will be limited to values greater than or equal to 25 microns. The photosensitive polyimide proposed for this project is recommended by the manufacturer for thick film applications spanning 10 to 160 microns (18:19). Therefore, the dielectric thicknesses will be restricted to span these values.

Figures 16 and 17 plot the line delay for a one centimeter long interconnect versus the dielectric thickness for two metal thicknesses. Although a dielectric thickness greater than 20 microns has very little effect on the delay time, the metal thickness has a very profound effect considering the range of interest. Therefore, the maximum metal thickness available (1.2 microns) and a dielectric thickness greater than 20 microns is proposed to limit the propagation delay. From Figures 18 and 19, it is clear that dielectric thickness has very little effect on line loss above

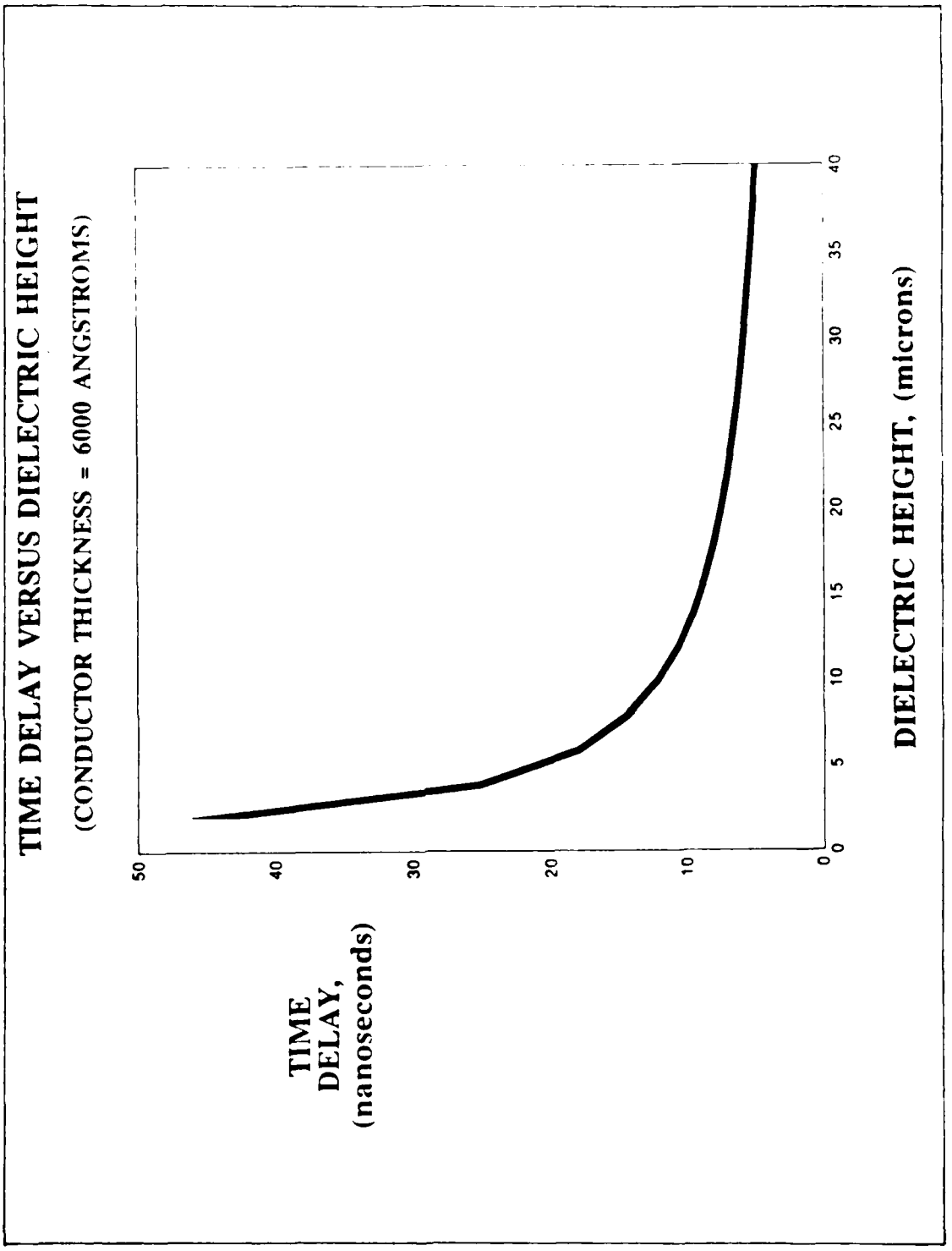

Figure 16. Line Delay Versus Dielectric Thickness for Selectilux HTR 3-200 Polyimide Precursor. Aluminum thickness = 0.6 um. (The spreadsheet calculations can be referenced in Appendix B).

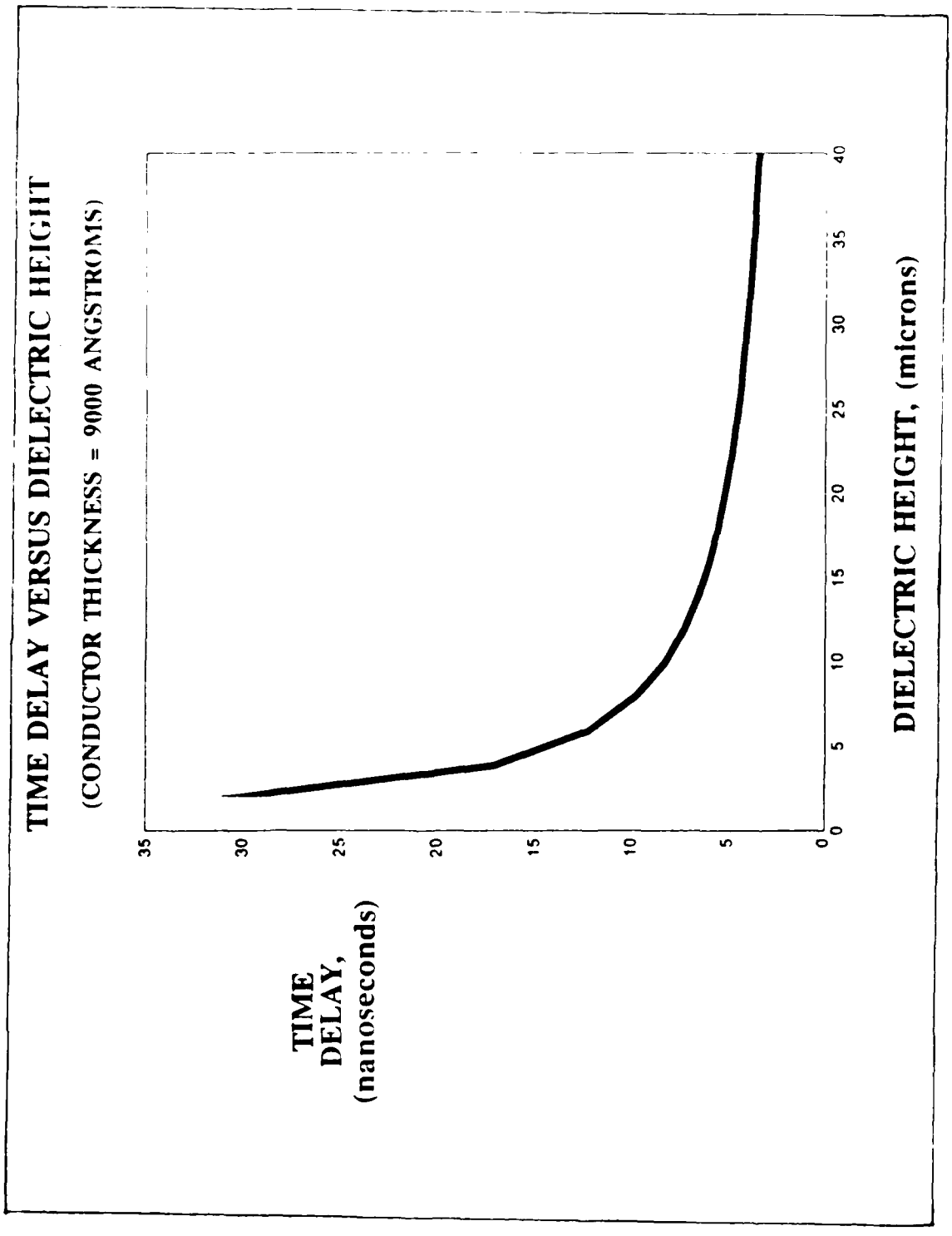

Figure 17. Line Delay Versus Dielectric Thickness for Selectilux HTR 3-200 Polyimide Precursor. Aluminum thickness = 0.9 um. (The spreadsheet calculations can be referenced in Appendix B).

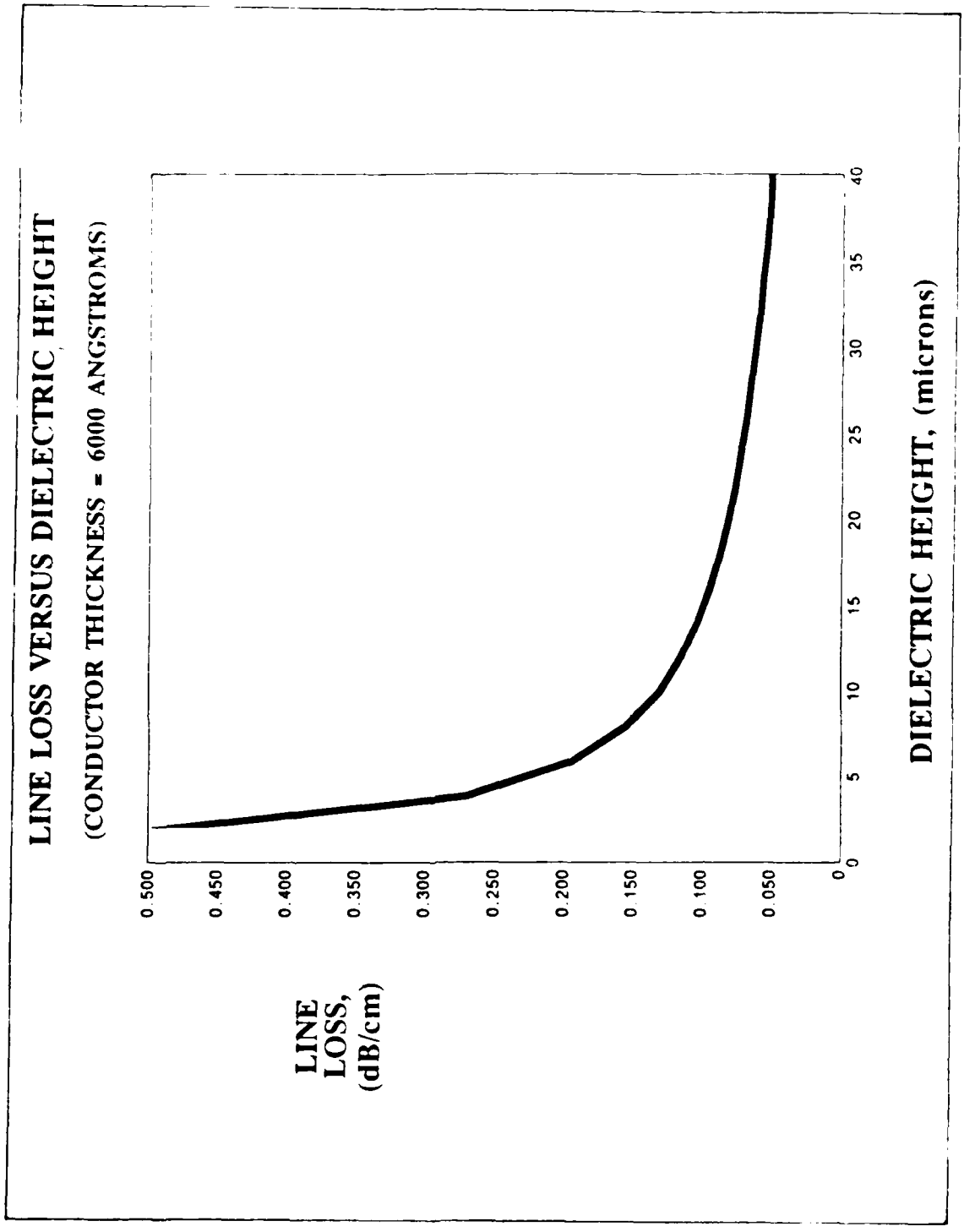

Figure 18. Line Loss Versus Dielectric Thickness for Selectilux HTR 3-200 Polyimide Precursor. Aluminum thickness = 0.6 um. (The spreadsheet calculations can be referenced in Appendix B).

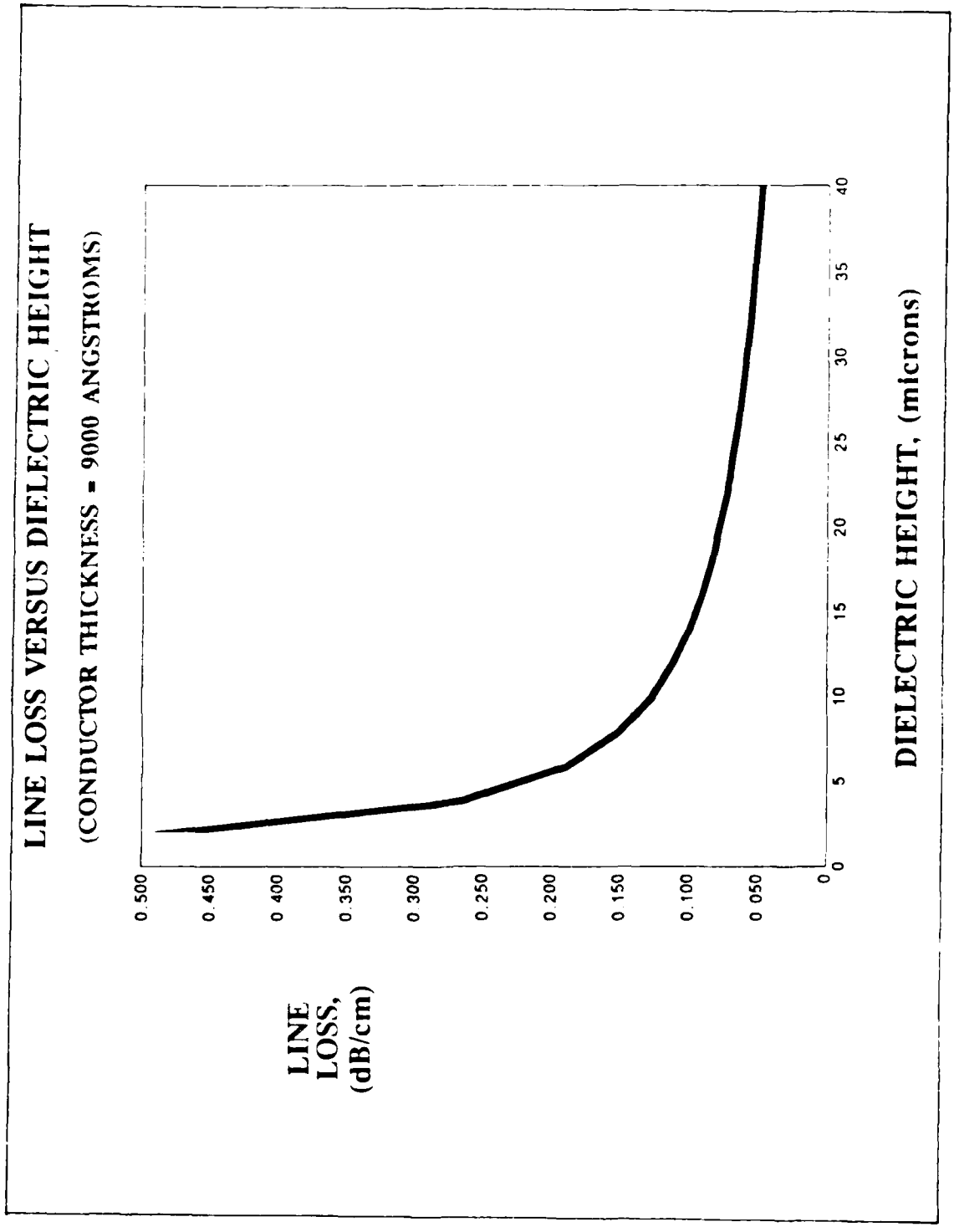

Figure 19. Line Loss Versus the Dielectric Thickness for Selectilux HTR 3-200 Polyimide Precursor. Aluminum thickness = 0.9 um. (The spreadsheet calculations can be referenced in Appendix B).

20 microns, and metal thickness has a similarly negligible effect. The discriminating factor determining the dielectric thickness is a test requirement.

Although many of the tests will be performed with high-impedance probes, if reflections become a source of difficulty, the lines must be terminated with a matched impedance. Considering the range of possible characteristic impedance values (that is, less than 100 ohms) for the proposed conductor width (Table 1), a 50 ohm line is preferred to match the test probe impedance. Figures 20 and 21 show that approximately 20 microns will keep the reflection coefficient near zero. To accommodate wafer-scale integration of VLSI circuits, the narrowest lines possible without a repeatable pattern is proposed. The resolution of the mask fabrication equipment at AFIT is limited to 25 microns without further photoreduction (i.e. step and repeat). In addition, to minimize crosstalk noise, the lines will be separated by 200 microns.

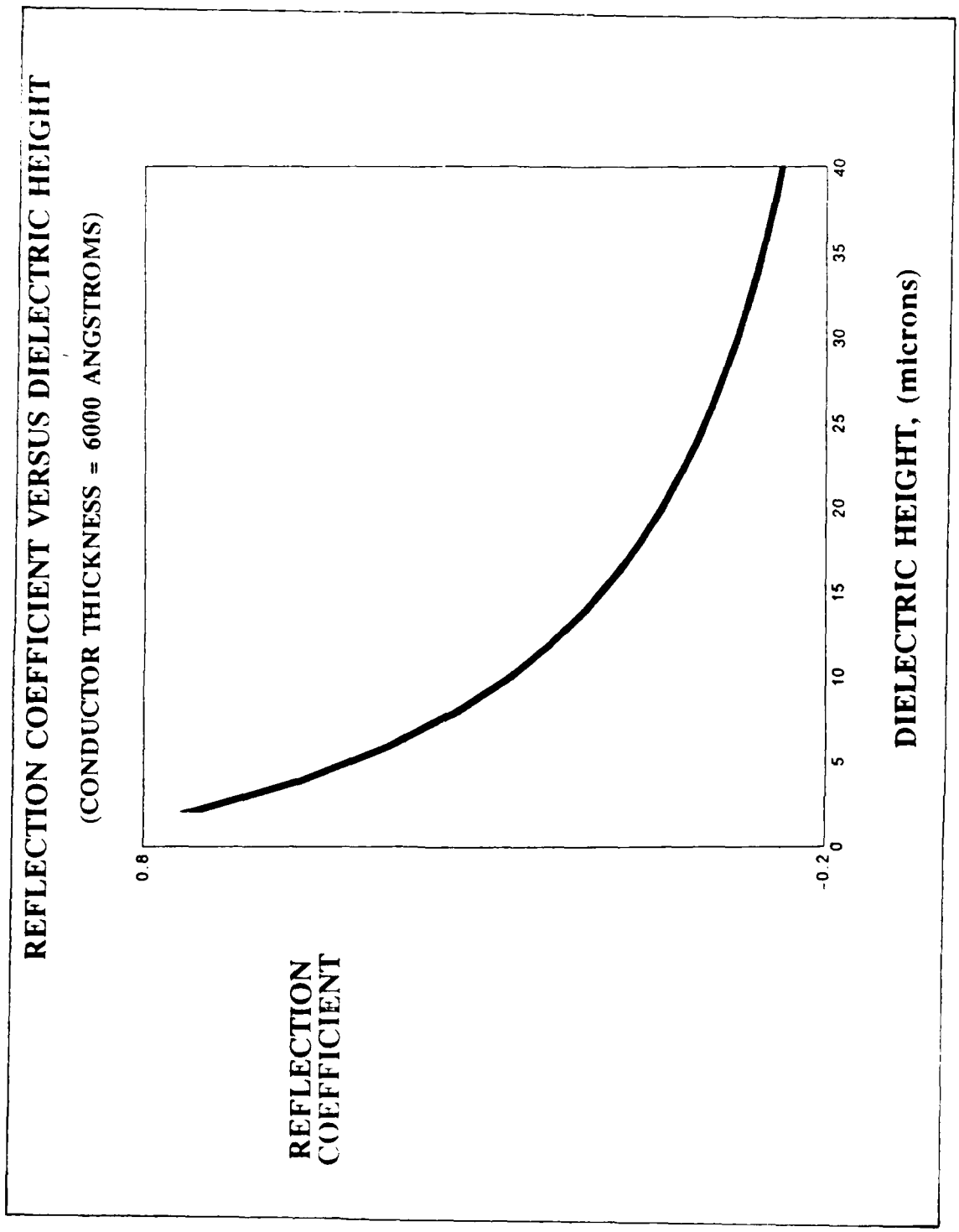

Figure 20. Reflection Coefficient Versus Dielectric Thickness for Selectilux HTR 3-200 Polyimide Precursor. Aluminum thickness = 0.6 um. (The spreadsheet calculations can be referenced in Appendix B).

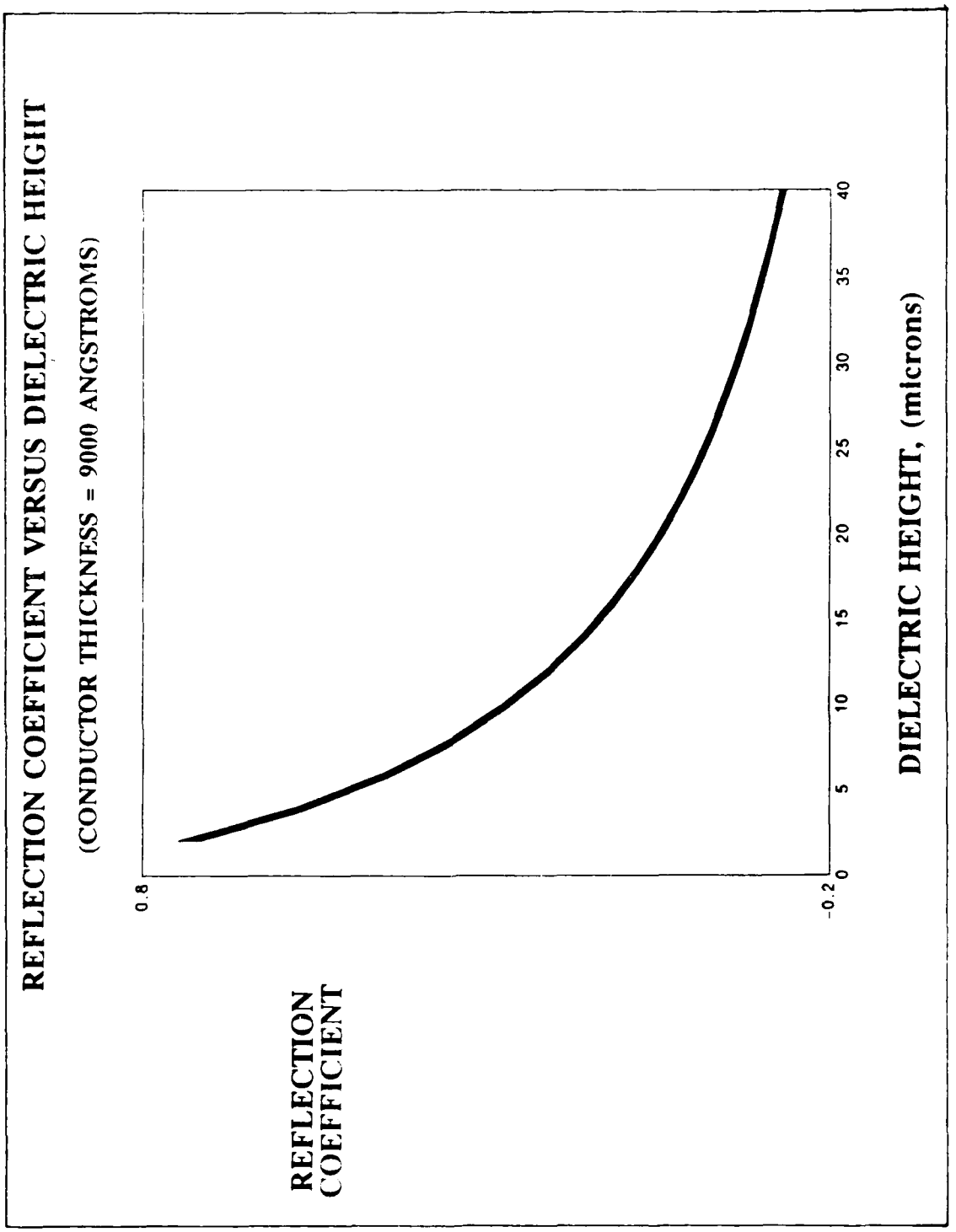

Figure 21. Reflection Coefficient Versus Dielectric Thickness for Selectilux HTR 3-200 Polyimide Precursor. Aluminum thickness = 0.9 um. (The spreadsheet calculations can be referenced in Appendix B).

III. Experimental Procedure

To evaluate the merits of the proposed wafer-scale interconnect structure, a prototype was fabricated and electrically evaluated. This chapter presents the processing schedule required to realize these interconnects, and tne experimental procedure performed to verify its electrical performance.

Development of Processing Schedule

The prototype was fabricated in three basic processing steps. First, the wafer substrate was prepared to receive two integrated circuit die; next, the die were mounted into the wafer substrate; finally, the metallization pattern was deposited with alternate layers of polyimide and aluminum. This section records the design considerations and fabrication procedures utilized.

Substrate Preparation. A wafer substrate was prepared to receive two prefabricated integrated circuits. The substrate design evolved from two requirements: (1) to provide a planar metallization surface after the die are mounted, and (2) to insure structural support against mechanical stresses. These requirements will promote reliable interconnections between the wafer and die circuitries. Two substrate designs, meeting these requirements, were considered. This section documents the decisions made to select a design, and the methods used to create the wafer substrate.

Substrate Design. To meet the requirement for a planar surface, the silicon wafer was anisotropically etched to accomodate the die. Both AFIT and Auburn University researchers have employed variations of this method. AFIT has used this method to etch wells in the wafer (40:1),

while Auburn has used this method to etch holes through the substrate (29:845). The wafer design for this phase of AFIT's research employs Auburn's technique to planarize the wafer surface. However, an additional wafer was added to maintain the structural integrity attained by the AFIT wafer.

Due to limits on the materials and services available, the planarizing substrate design developed at AFIT was unfeasible for this phase of research. As previously mentioned, the integrated circuits were fabricated as part of DARPA's Metal-Oxide Semiconductor Implementation Service (MOSIS) contract (Figure 22). These chips were too thick to apply the substrate design developed at AFIT. AFIT's well-etching design was developed assuming 200 microns was the maximum die thickness. However, the actual circuits fabricated by MOSIS were approximately 375 microns thick. Consistent with the materials previously used at AFIT, a quartered three-inch wafer was utilized as the silicon substrate. Because these substrates were only 500 microns thick, the silicon remaining at the bottom of the well would be inadequate as structural support.

Therefore, to avoid the need for thicker wafers, a dual wafer structure (Figure 23) was utilized. This structure incorporates Auburn's silicon etching and die mounting design for the planarizing substrate (29:845-847). Instead of etching wells, the patterns are completely etched into holes where the die are mounted. This research effort adds an additional supporting substrate to provide structural support.

After this design was chosen, methods for fabricating the substrate were experimentally evaluated.

Substrate Fabrication. The planarizing substrate was prepared by (a) isotropically etching the wafer to a specific thickness, (b)

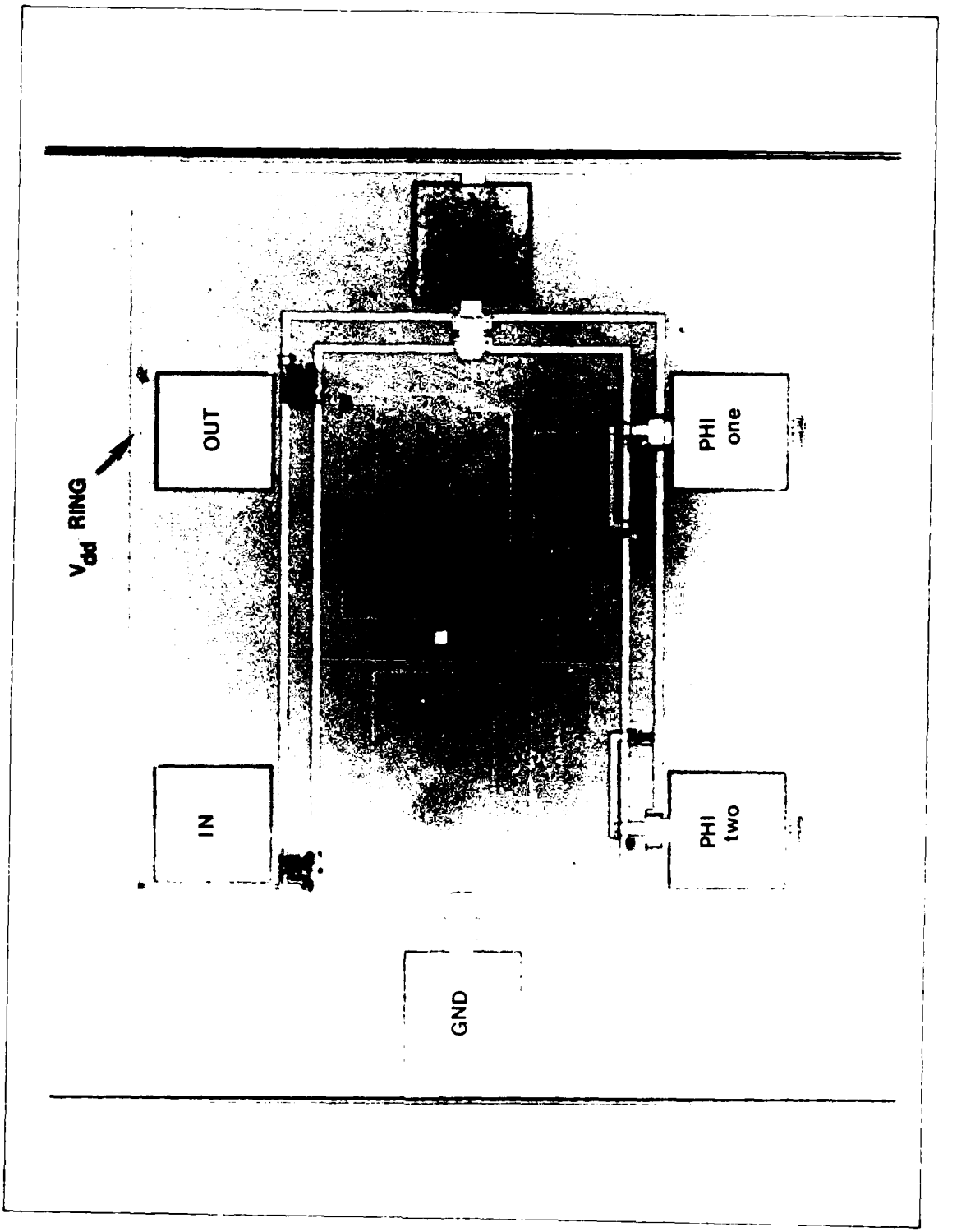

Figure 22. MOSIS Fabricated Integrated Circuit Used For This Research. The circuit design is a simple 2-bit shift register.

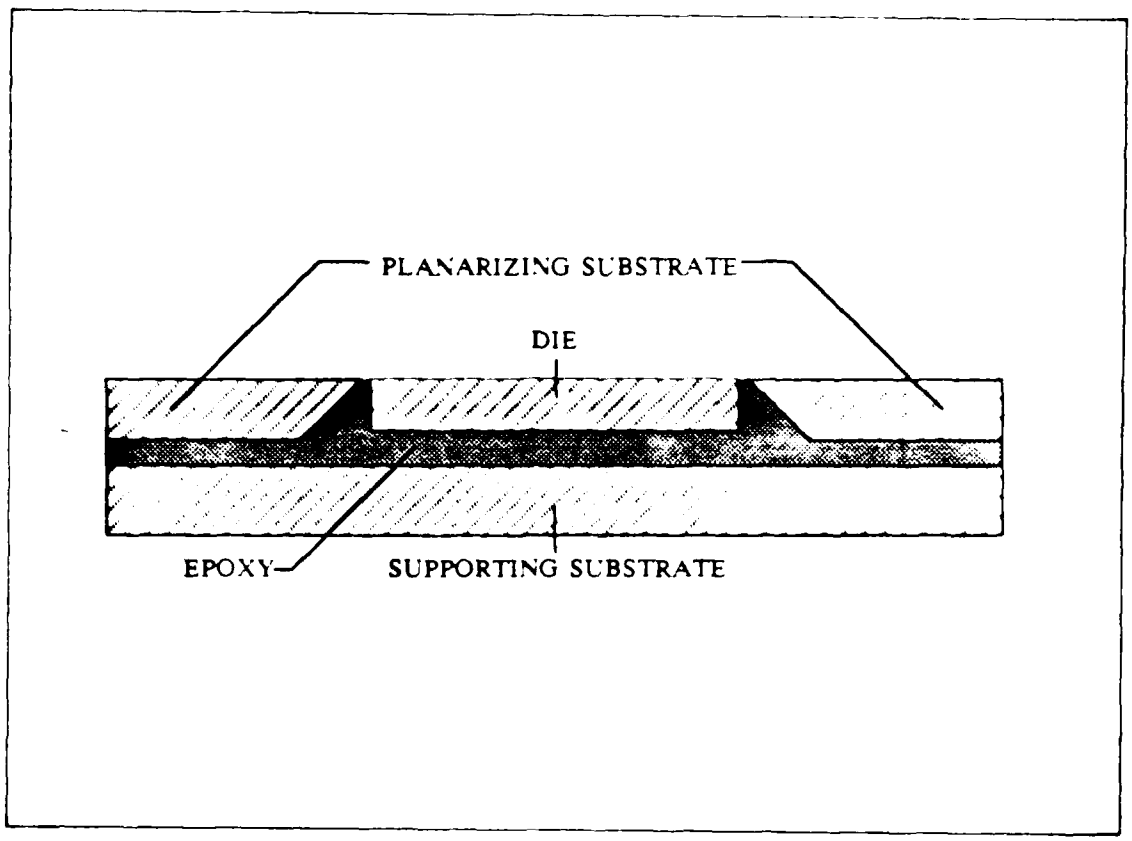

Figure 23. Dual Wafer Structure. The top wafer serves to planarize the circuitry, and the bottom wafer adds mechanical support to the structure.

thermally growing a thick silicon-dioxide mask, (c) photolithographically patterning the oxide mask, (d) anisotropically etching rectangular holes in the wafer, and (e) thermally growing a new silicon-dioxide layer as a dielectric (See Figure 24). The fabrication alternatives and the physical theory for each of these steps are synopsized in the following sections. The procedures for all attempted alternatives are detailed in the Appendices D through H.

Planar Silicon Etch. The wafer substrate had to be etched to a specific thickness to insure consistent hole dimensions. As shown in

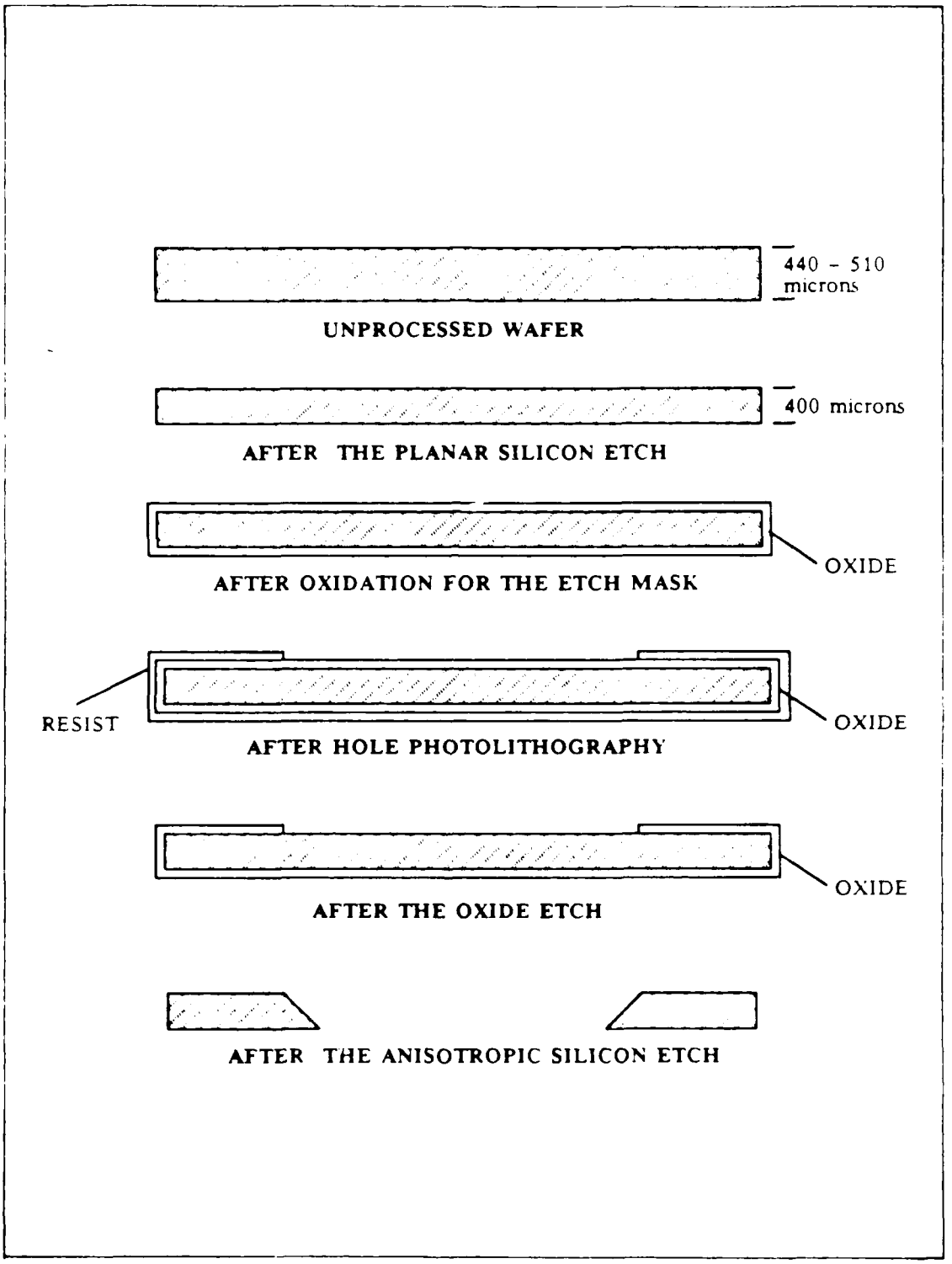

Figure 24. Processing Steps Required to Prepare the Planarizing Substrate.

Figure 25, (100) silicon anisotropically etches at a 54.47° angle with respect to the wafer surface (5:1178). Because the wafers ordered for this project ranged from 440 to 510 microns, the hole dimensions at the wafer surface would have varied by as much as 50 microns. The probability of interconnect fracture was expected to be high at the transition from wafer to chip. By designing the hole pattern to a specified wafer thickness, the distance across this transition can be limited. Therefore, a specific thickness of 400 microns was set to reduce lateral variations across this transition.

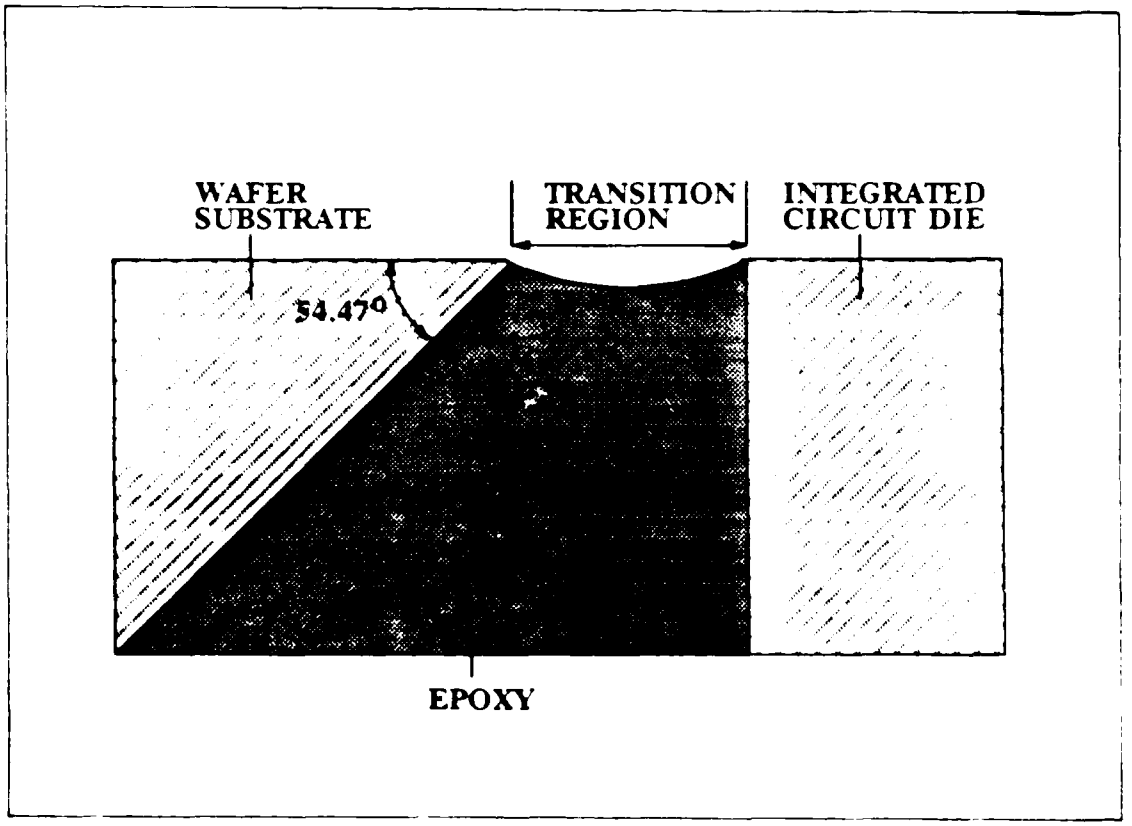

Figure 25. Expanded View of the Planarized Wafer Surface. The topography across the transition between the wafer and die surfaces is extremely rough. To reduce the risk of line breakage, the design goal was to reduce the distance across this region.

An isotropic silicon etching solution was prepared to thin the wafers to 400 microns. The solution was a mixture of 15 parts nitric acid, 5 parts acetic acid, and 2 parts hydrofluoric acid (16:522). This mixture begins the etching process by oxidizing the silicon. The silicon surface is promoted to a higher oxidation state by the liberation of holes produced by an autocatalytic process involving the nitric acid (67:452):

$$HNO_2 + HNO_3 \longrightarrow 2NO^{2-} + 2h^+ + H_2O \quad (28a)$$

$$2NO^{2-} + 2H^+ \longrightarrow 2HNO_2 \quad (28b)$$

$$Si + 2h^+ \longrightarrow Si^{2+}. \quad (28c)$$

Next the silicon is oxidized by hydroxide ions produced by the dissociation of water (67:452):

$$2H_2O \rightleftharpoons 2OH^- + 2H^+ \quad (29a)$$

$$Si^{2+} + 2OH^- \longrightarrow Si(OH)_2 \quad (29b)$$

$$Si(OH)_2 \longrightarrow SiO_2 + H_2. \quad (29c)$$

Finally, the oxide is dissolved by the hydrofluoric acid (70:452):

$$SiO_2 + 6HF \longrightarrow H_2SiF_6 + 2H_2O. \quad (30)$$

The acetic acid serves as a diluent in the system. Preparation and procedures for the planar etch process are detailed in Appendix D.

Oxide Growth for the Etch Mask. Although silicon dioxide etches much slower than crystalline silicon in a potassium hydroxide solution, a very thick oxide layer is required over the entire surface to protect the silicon wafer from the etchant. Mainger reported that a 70°C potassium hydroxide solution etched silicon at 0.87 microns per minute in the <100> direction, and silicon dioxide at 40 angstroms per minute (40:44). Therefore, at least a 1.839 micron oxide layer was required over the entire silicon surface. As a margin of safety, an oxide growth of 2.4 microns was established as a design objective. Steam growth was used to

create this oxide, since thermal oxides grow fastest by wet oxidation (70:343):

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2. \quad (31)$$

A thickness of 2.4 microns can be achieved by wet oxidation after 20 hours at 1050°C (70:350). The oxidation procedures performed in this step are detailed in Appendix E.

Hole Photolithography. Hole photolithography was attempted for both negative and positive photoresists. In addition, two different mask-design methods were investigated. One approach was fully automated, and the other approach was manually assisted. However, the most favorable results were obtained using the manually assisted approach to create a positive photoresist mask.

Two different mask designs were created, one for use with negative photoresist and another for use with positive photoresist. The mask for negative photoresist required only three steps: (1) the initial Rubylith design, (2) the first plate image, and (3) the negative photoresist print. Because these three steps reversed the image twice, the Rubylith pattern was made as a positive image of the negative photoresist mask. However, the mask for the positive photoresist required an additional step. A negative image plate was made from the first plate, resulting in an additional image reversal. Therefore, the initial Rubylith design (Figure 26) was reversed as a negative image of the positive photoresist mask. Because the negative image plate was almost completely black, the mask design included an allignment pattern to outline the edge of the wafer.

Two different methods of Rubylith design were attempted: a fully automated method and a method coupling the automation and manual design methods. The fully automated method was attempted to establish the

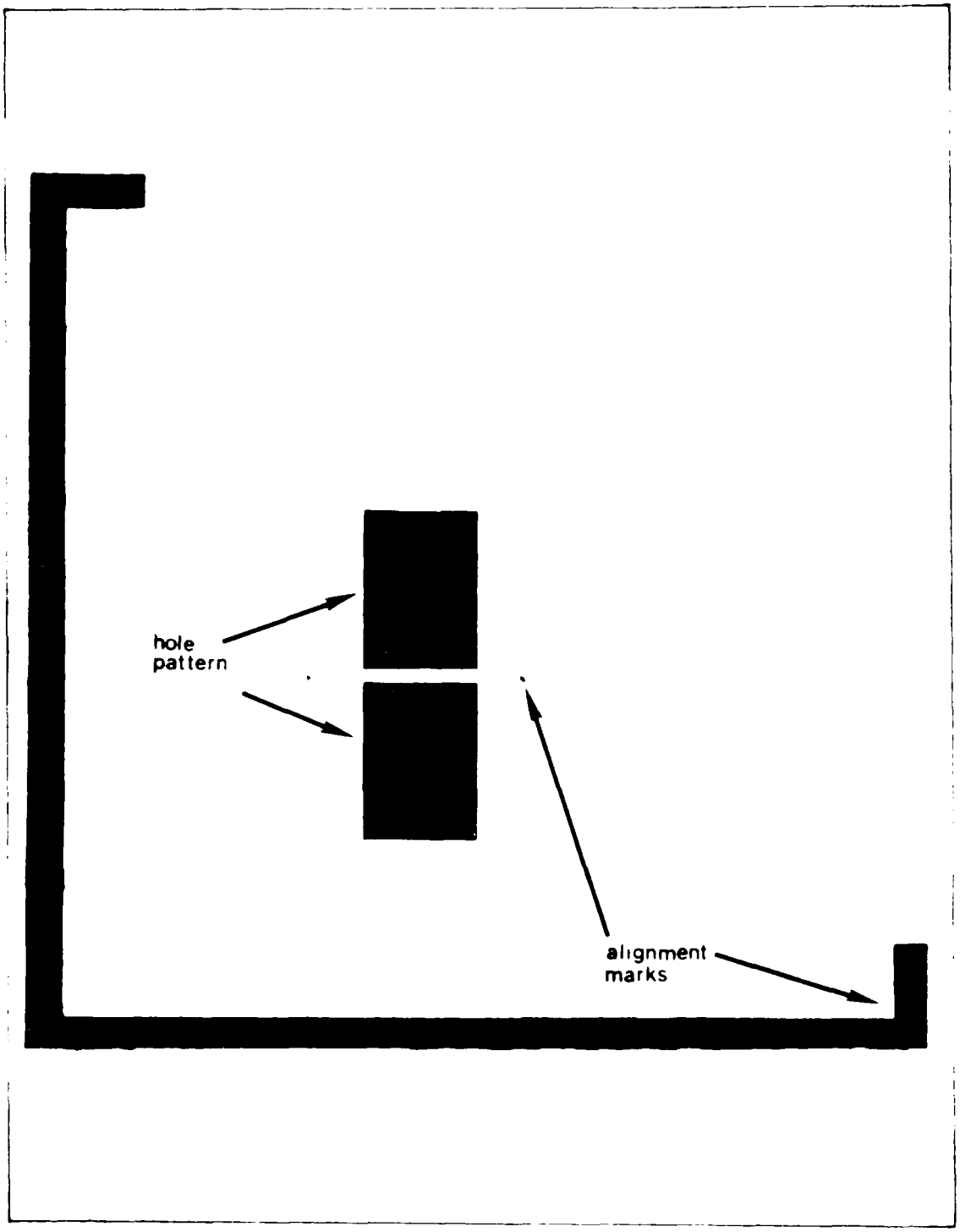

Figure 26. The Mask Design for the Hole Pattern. This mask design was created specifically for use with positive resist. Note the allignment mark outlining the edge of the quartered wafer.

foundation for future research using more complicated wafer-scale designs. The Rubylith designs were created on a Sun workstation using Magic, a computer-aided design (CAD) tool. The mask design was transferred to a magnetic tape medium and ported onto the General Electric CALMA CAD system at the Air Force Wright Aeronautical Laboratory (AFWAL). The CALMA system was used to drive a Xynetics 1100 automated drafting system. The drafting system was reconfigured to cut the Rubylith pattern. However, the translation from the Magic tool to the CALMA system was prone to error; therefore, a manual method of transferring the mask design to Rubylith was employed. Essentially, the Magic file coordinates were converted to mils, and the pattern was manually cut into the Rubylith using the coordinatograph machine in the Cooperative Electronics Materials and Processes Laboratory (CEMPL) at AFIT.

The steps taken to create the photoresist patterns are detailed in the photolithography procedures found in Appendix F. This appendix includes the procedures followed to produce both negative and positive photoresist masks, and the steps taken to use both AFWAL's CALMA system and CEMPL's coordinatograph machine.

Silicon-Dioxide Etch. The pattern developed in the photoresist mask was transferred to the silicon-dioxide mask using buffered hydrofluoric acid. This mixture included six parts ammonium fluoride and one part hydrofluoric acid. It was shown in Equation 28c how hydrofluoric acid dissolves silicon dioxide. In fact, concentrated hydrofluoric acid will etch the oxide uncontrollably and will lift-off the photoresist mask. However, by buffering the acid with ammonium fluoride, the etchant is more controllable and does not attack the photoresist (31). The procedures used to etch the oxide mask are detailed in Appendix G.

Anisotropic Silicon Etch. Anisotropic etching takes advantage of the different etching properties for the three crystallographic orientations in silicon. Generally, the etching rate decreases in the following order: (100), (110), (111). By selecting an etchant that preferentially etches in the <100> direction compared to the <111> direction, etching in the <111> direction can be neglected. In addition, if the mask borders are aligned with the <110> direction, the <110> directed etch will be retarded by the (111) planes. Under these conditions, rectangular patterns can be obtained in (100) oriented silicon wafers. This geometry is required by the rectangular integrated circuit die to be mounted in the wafer. As previously mentioned, the walls of the hole will be sloped at 54.47° with respect to the wafer surface. These sloped walls correspond to the (111) planes. Figure 27 shows how these features combine when the (100) surface is exposed to the etchant (5:1178-1179).

A rectangular hole was anisotropically etched into the silicon with a potassium hydroxide etchant. By weight, the etchant is composed of 25% KOH, 60% deionized water (DIW), and 15% isopropyl alcohol (40:10). There are several theories on how the silicon is actually etched by this solution (32:111, 49:146). However, the reaction proposed by J. B. Price seems to account for the gas product of the reaction in a simple stoichiometric relationship (54:344):

$$Si + H_2O + 2KOH \longrightarrow K_2SiO_3 + 2H_2. \qquad (32)$$

The isopropyl alcohol has a profound effect upon the anisotropy and the etch rate of the mixture. Given a 25 percent by-weight concentration of potassium hydroxide, the etchant will etch preferentially in the <110> direction without isopropyl alcohol. However, when alcohol is added to

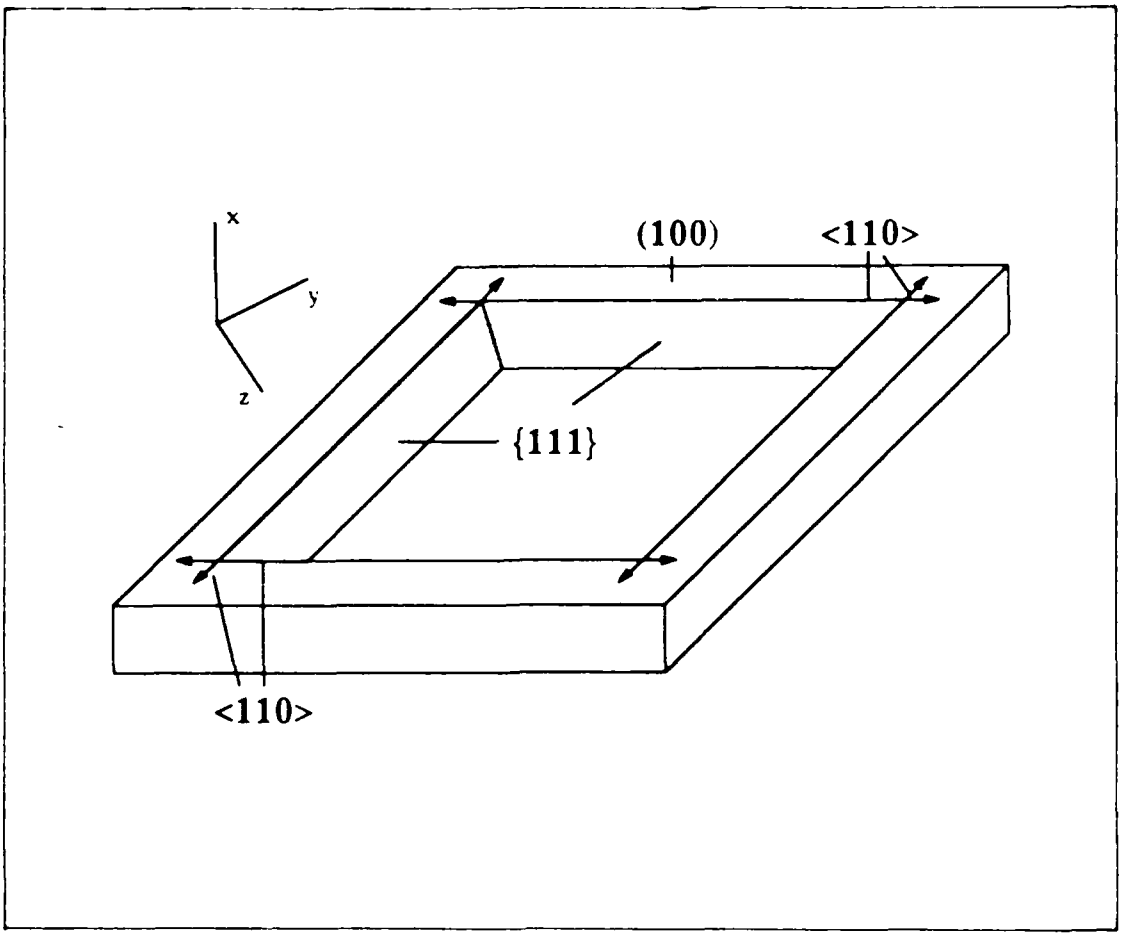

Figure 27. A Rectangular Hole Anisotropically Etched in (100) Silicon.

the mixture, the etch rate is retarded in the <110> direction and enhanced in the <100> direction. The resulting mixture will preferentially etch in the <100> direction with isopropyl alcohol (54:342).

An etchant system employing a water-cooled reflux condenser was established to maintain the composition of the etchant. The solution was heated and maintained at 70°C with a hot plate. At 70°C, the 400 micron thick (100) wafers etched in just under nine hours. The etching procedures are detailed in Appendix H.

Die Mounting. The die were mounted in the etched substrate with an epoxy adhesive. A good adhesive will have a high bond strength to maintain monolithic integrity with the substrate. In addition, the adhesive should be chemically compatible. Finally, the adhesive must have a high temperature resistance to endure high temperature processing steps. Most epoxy adhesives satisfy these requirements (38:200-201).

The adhesive used for the die mounting process is an insulating epoxy produced by Master Bond. Master Bond EP34CA Special is a dielectric-filled epoxy resin system designed to match the TCE of silicon (2.5 x $10^{-6}/^{\circ}C$). This composition facilitates maintaining the bond strength by reducing the thermal stress during its cure. The epoxy's filler, beta eucryptite (a lithium aluminum silicate), has a melting point of $1397^{\circ}C$, and it is essentially chemically inert and compatible for silicon processing. Since cured Master Bond EP34CA is temperature resistant up to $300^{\circ}C$, it is also compatible with the subsequent fabrication steps (8). Therefore, EP34CA was chosen as the adhesive for this project.

The die were mounted into the substrate in three steps. First, the die were bonded into the planarizing substrate. The technique used to achieve this step is similar to the method derived by the Auburn researchers (29:846). The die and the etched silicon substrate were placed face down onto an optical flat, and the adhesive was deposited into the gap between the die and substrate (Figure 28a). The optical flat maintained a planar surface across the wafer while the adhesive cured. Next, the supporting substrate was attached to the bottom of the planarizing substrate. Adhesive was applied over the entire bottom surface of the planarizing substrate, and a clean unprocessed wafer was placed over the adhesive (Figure 28b). A constant force was applied to

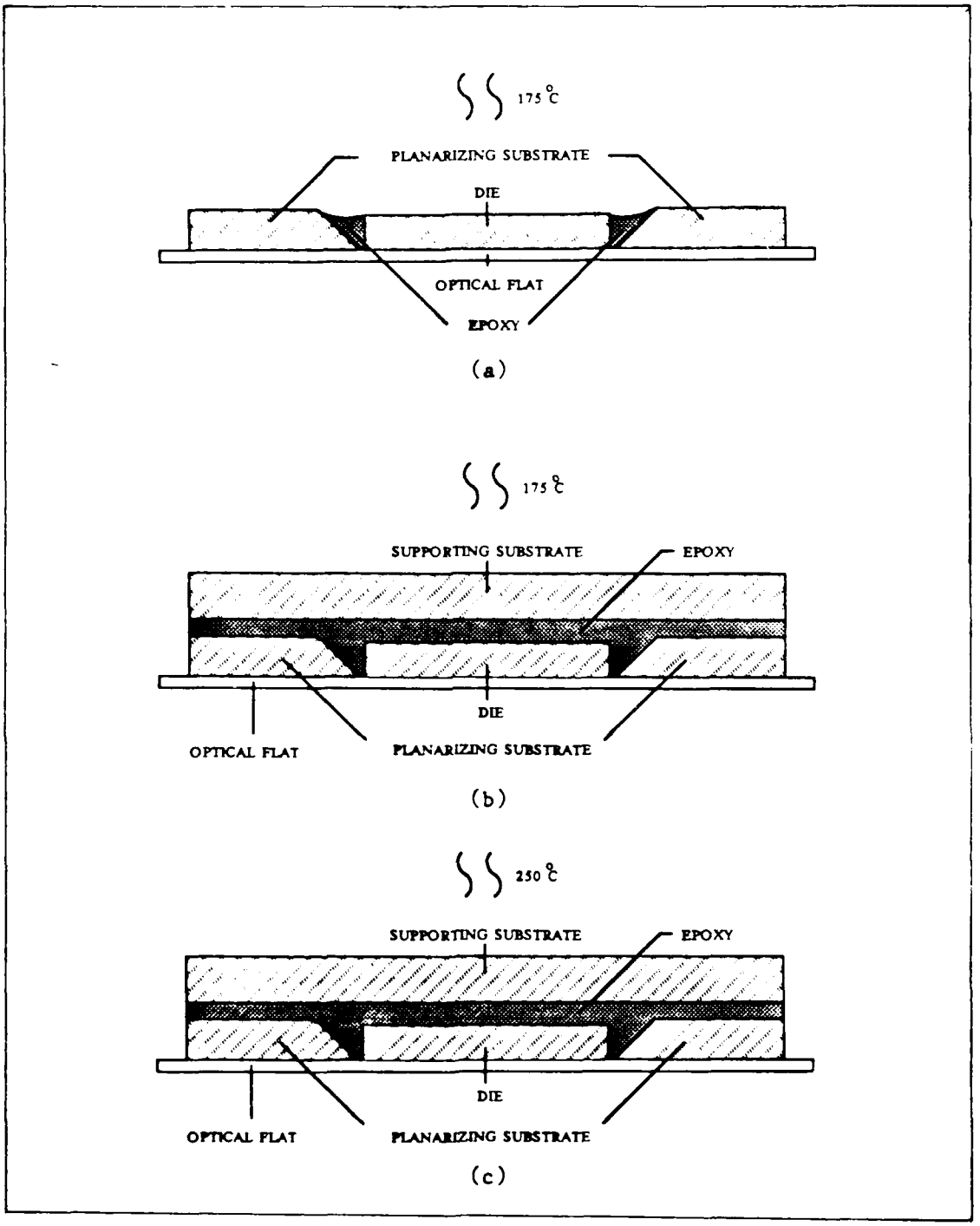

Figure 28. Three Fabrication Steps Resulting in a Dual Wafer Structure. (a) The die were mounted face down into the planarizing substrate, (b) the supporting substrate was attached to the bottom of the planarizing substrate, (c) the entire structure was subjected to a high-temperature curing cycle.

the supporting substrate while the adhesive cured. Finally, the entire wafer was subjected to a high-temperature cure cycle. Because subsequent polyimide applications will require a 250°C cure cycle, the adhesive was subjected to this temperature to ensure its thermal stability (Figure 28c). The procedure for these steps are detailed in Appendix I.

Interconnect Fabrication. After the die were mounted in the wafer, the die were interconnected on the wafer to complete the integration task. The die circuitry were interconnected with continuous printed interconnects on the wafer surface. These interconnects were fabricated with alternate applications of dielectric (i.e. polyimide) and metal (i.e. aluminum) (Figure 29). This section documents the methods employed to achieve these interconnects.

Polyimide Application. A photo-sensitive polyimide precursor developed by EM Industries was used as the dielectric for the interconnects. Selectilux HTR 3-200 is a polyimide precursor suitable for thick-film applications (5 to 80 um after cure) and patternable as a negative acting photoresist (18:4). There has been very little research done to characterize this material as a patternable interconnect dielectric. Therefore, experiments were performed to determine the behavior of sloped vias under controlled conditions. As a result, the optimum dielectric processing conditions were implemented.

Material Characterization. Two studies were performed to determine the effect of proximity printing on via profiles. As previously mentioned, sloped vias are a requirement for reliable contacts when using thin films. Sloped vias are easily obtainable with HTR 3-200 using proximity printing (18:21).

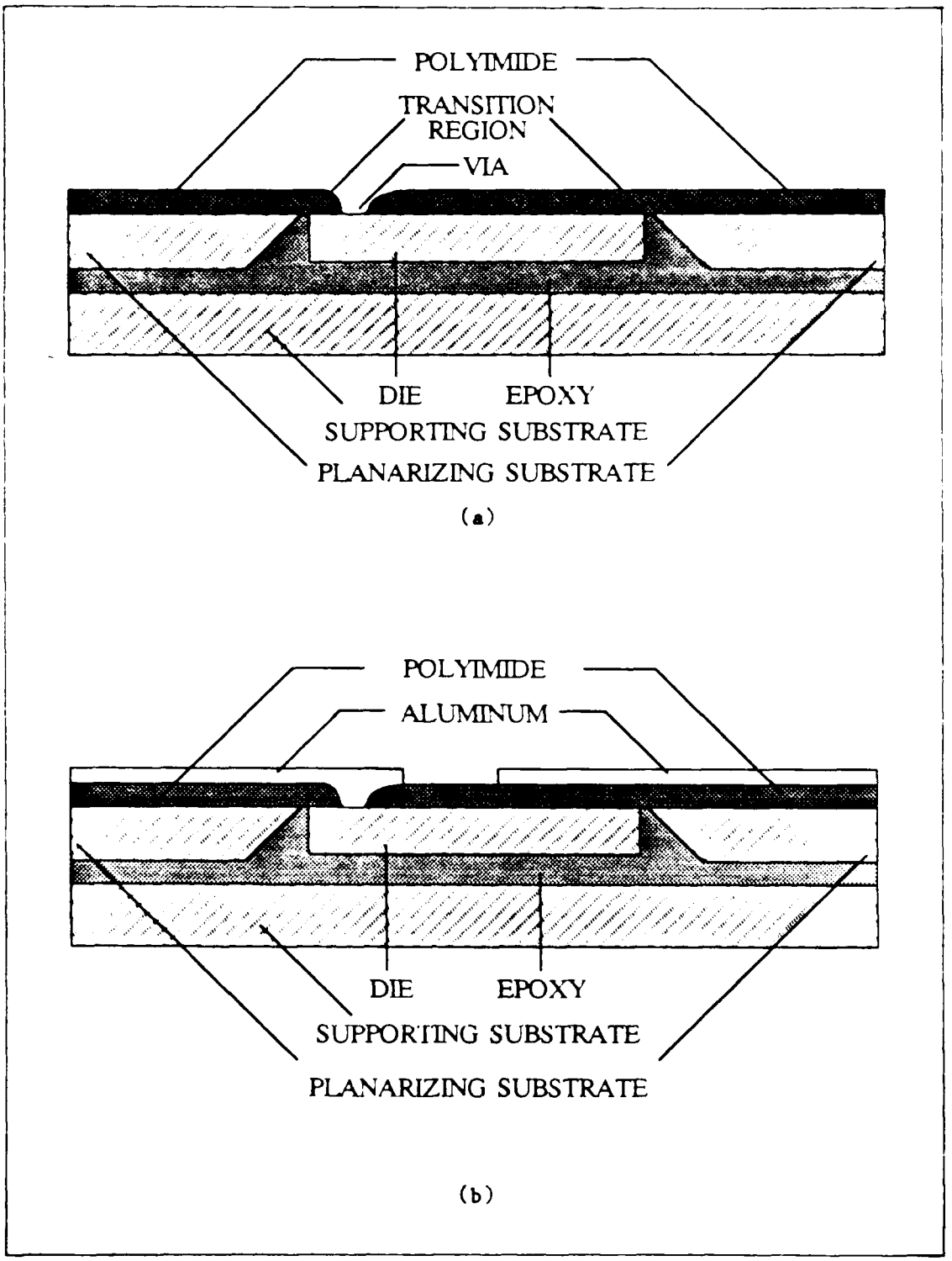

Figure 29. Interconnect Fabrication. The interconnects were fabricated with alternate applications of (a) polyimide and (b) aluminum.

Proximity printing is very similar to contact printing, except that a small gap is maintained between the mask reticle and the wafer surface Proximity printers operate in the Fresnel diffraction range (70:275). Figure 30 shows the relative intensity of a Fresnel diffraction pattern as a function of the distance from the mask edge. The energy incident on the photoresist surface (E_p) at a distance y from the mask edge is (42:472):

$$E_p = k\, E_i\, \exp(-m\, P) \tag{33}$$

where

$$P = y\left(\frac{2}{\lambda z}\right)^{1/2} \tag{34}$$

and

k is the value of E_p/E_i at P = 0,
m is the slope of $\ln(E_p/E_i)$ versus P at the mask edge,
E_i is the energy incident on the mask (mJ/cm^2),
y is the distance measured from the mask edge (cm),
λ is the wavelength of the incident light (cm), and
z is the gap between the mask and the wafer (cm).

For negative resist, the difference between the size of a clear mask feature and the size of the feature on the photoresist is 2y. Equating the energy incident on the photoresist surface (E_p) to the energy threshold (E_T) of the photoresist, and solving Equations (33) and (34) for 2y:

$$2y = N\, z^{1/2}\, [\ln(kE_i) - \ln(E_T)] \tag{35}$$

N = a parameter incorporating m and λ, which are constant for the optics of the printer ($cm^{1/2}$).

Therefore, the size of the photoresist feature can be changed by varying the exposure energy on the mask (E_i), the mask-to-wafer separation (z), or the threshold energy of the photoresist (E_T).

Two experiments were performed to characterize the polyimide. In the first experiment, the wafer-to-mask separation was varied, while the exposure and threshold energies were maintained constant. In the second

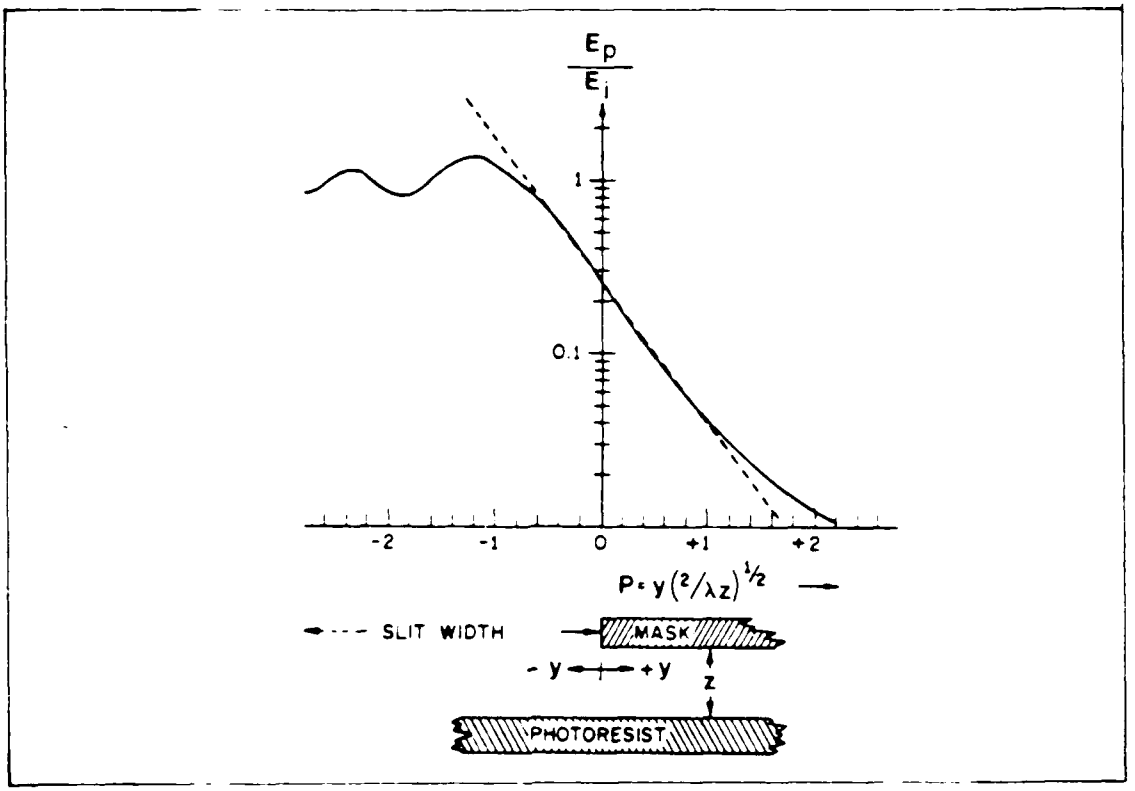

Figure 30. Fresnel Diffraction Pattern at the Mask Edge. E_p is the energy incident on the photoresist surface, E_i is the energy incident on the mask, y is the distance measured from the mask edge, λ is the wavelength of the incident light, and z is the gap between the mask and the wafer (42:472)

experiment, the separation was held constant, while the exposure and threshold energies were varied. The wafer-to-mask gap was varied by using mylar film spacers; the exposure energy was varied by changing the time duration of the exposure; the threshold energy was varied by increasing the thickness of the polyimide layer.

In the first experiment, polyimide was applied on several unprocessed silicon wafers at an approximate thickness of 10 microns. Each wafer was exposed for 80 seconds under a 5 mJ/cm^2 ultraviolet light source.

After the development sequence, the samples were sliced uncured and examined with a scanning electron microscope (SEM). These results are detailed in Chapter IV.

In the second experiment, polyimide was applied on one control wafer. This wafer was completely processed to realize the final sandwich structure described earier. In this experiment, nonfunctional die were epoxied into the etched substrate. The substrate was then coated with varied thicknesses of polyimide, and exposed to ultraviolet light at varying energies. After development, the profile of a selected via was probed with a Sloan Dektak surface profile measuring system. In addition, planarization data was gathered by measuring the profile of an alignment mark on the substrate surface. The results of this experiment are detailed in Chapter IV.

Dielectric Application. Using the substrate preparation and die mounting procedures discussed earlier, ten functional die were mounted in five wafers. A 10 micron thick layer of polyimide was deposited on each of the five wafers. The polyimide was patterned to provide contact vias for the interconnects. The mask design used to create the vias in the polyimide layer is shown in Figure 31. Appendix J documents the procedures employed to apply and pattern the polyimide for the dielectric layer.

The bonding pads on the integrated circuits were larger (i.e. a 562.5 micron square) than normally designed VLSI pads (i.e. a 125 micron square). This enlargement was incorporated to avert unforseen registration errors caused by skewed placement of die during mounting. The mask was designed with marks fashioned to align with the die corners. The contact via mask was manually aligned, and all vias were successfully

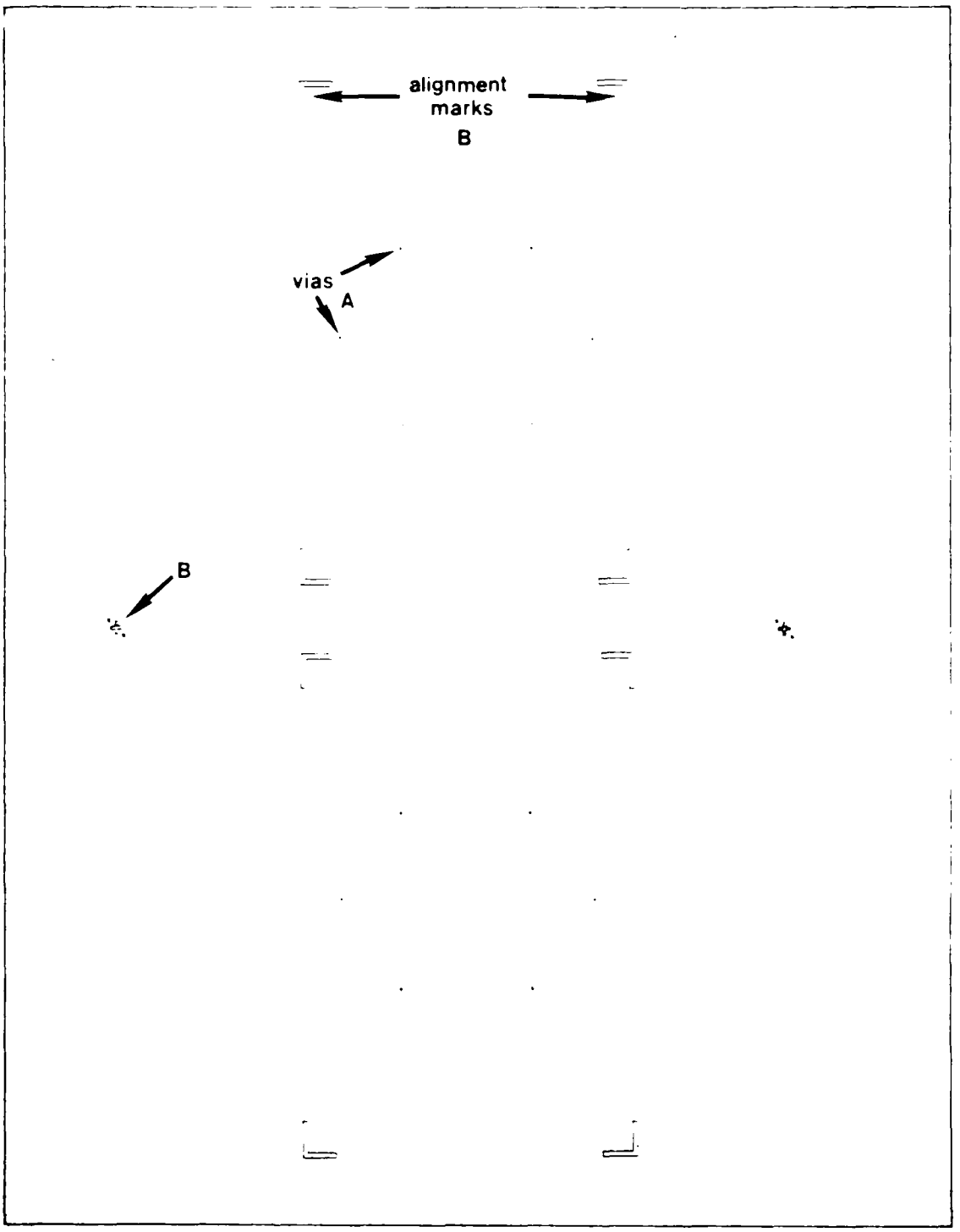

Figure 31. The Mask Design for the Contact Vias Required for the Continuous Printed Interconnects. Highlighted are the contact vias (A) and the alignment marks (B).

aligned with the large pads. In order to assess how much these pads can be scaled down, rotational and lateral misalignment data were collected from these samples.

Aluminum Metallization. A film of aluminum (approximately 1.2 microns thick) was deposited by evaporation over the patterned polyimide dielectric. Several, experiments were performed to evaluate different methods of masking with photoresist. This section documents the purpose and procedures for the experiments, emphasizing the final preparation of metallized samples for subsequent electrical tests.

Metallization Experiments. Five experiments were performed with differently prepared photoresists (Table 5). Each photoresist tested utilized the same mask design for the aluminum pattern (Figure 32). Each photoresist was subsequently evaluated by the following criteria: (1) Fine line resolution, (2) step planarization, (3) compatible stripping methods, and (4) resistance to the etchant. In every case, the unprotected aluminum was etched away in a mixture of 5 parts nitric acid,

Table 5. Photoresist Materials Used for Aluminum Metallization

Photoresist Materials	Spin Application Speed	Cure Time/ Temperature
Shipley M1350J	4000 rpm	30 min / 120°C
Selectilux HTR 3-200	4000 rpm	Uncured
Selectilux HTR 3-200	4000 rpm	60 min / 160°C
Selectilux HTR 3-200	1500 rpm	60 min / 100°C
Shipley M1350J and Selectilux HTR 3-200	4000 rpm 4000 rpm	30 min / 120°C -----

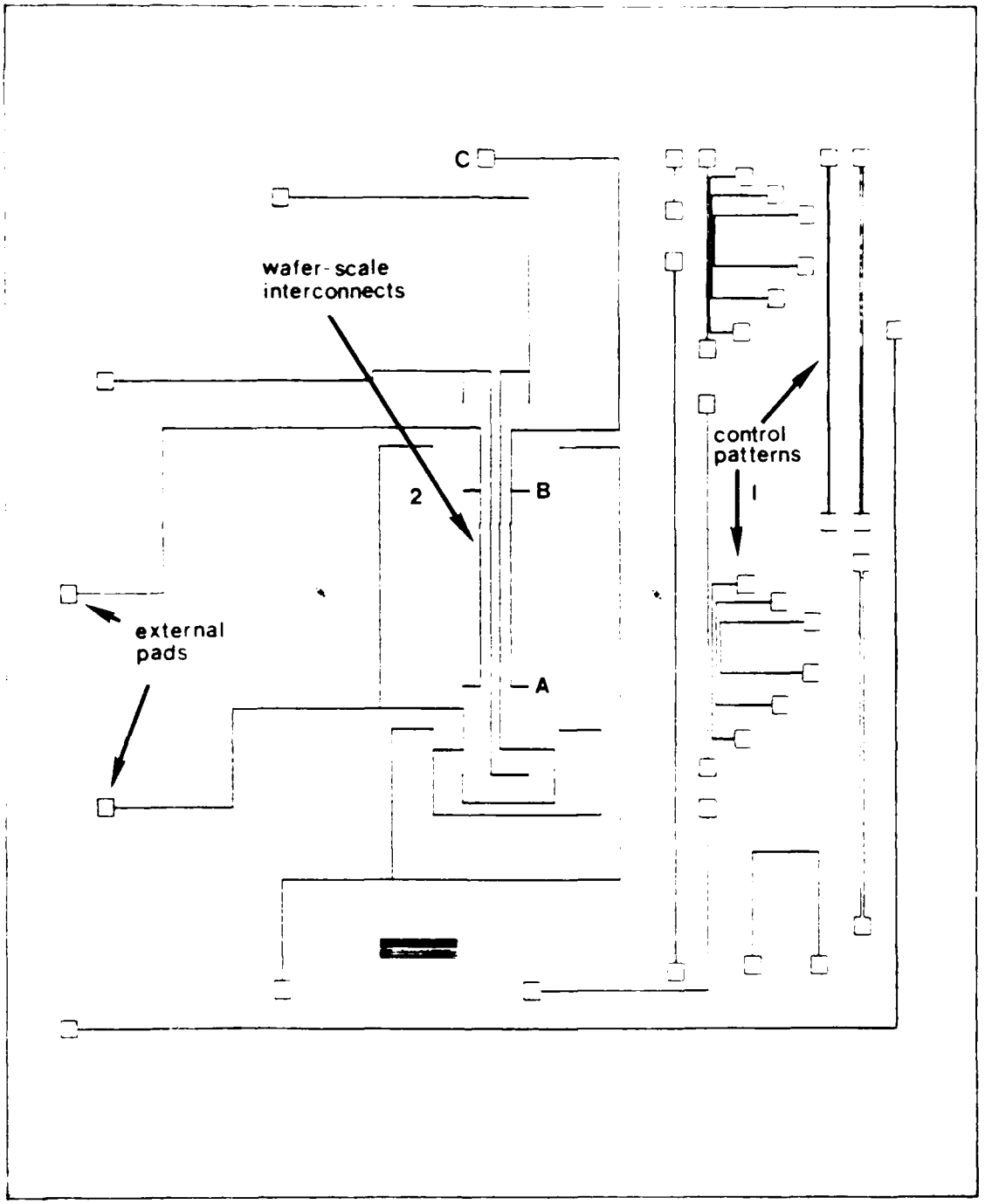

Figure 32. The Mask Design for the Continuous Printed Aluminum Interconnects. Major features include (1) the control patterns and (2) the wafer-scale interconnects. The external pads to the wafer-scale circuit are labeled, and the test points used for the parametric tests are labeled as A, B, and C.

2 parts phosphoric acid, and 5 parts acetic acid. The procedures for aluminum deposition and etching are detailed in Appendix K.

Initially, the Shipley M1350J positive photoresist was evaluated (Figure 33). This selection was preferred because positive photoresist can be easily removed without damaging the aluminum pattern by using acetone. In addition, positive resist layers are thicker than most negative resist layers (that is, at 4000 rpm, the Shipley M1350J photoresist yields a 16000 angstrom thickness (64:3) compared to a 12000 angstrom thickness for Waycoat 43 cps photoresist (53:5)). A thick photoresist layer was required to planarize the die-to-wafer transition.

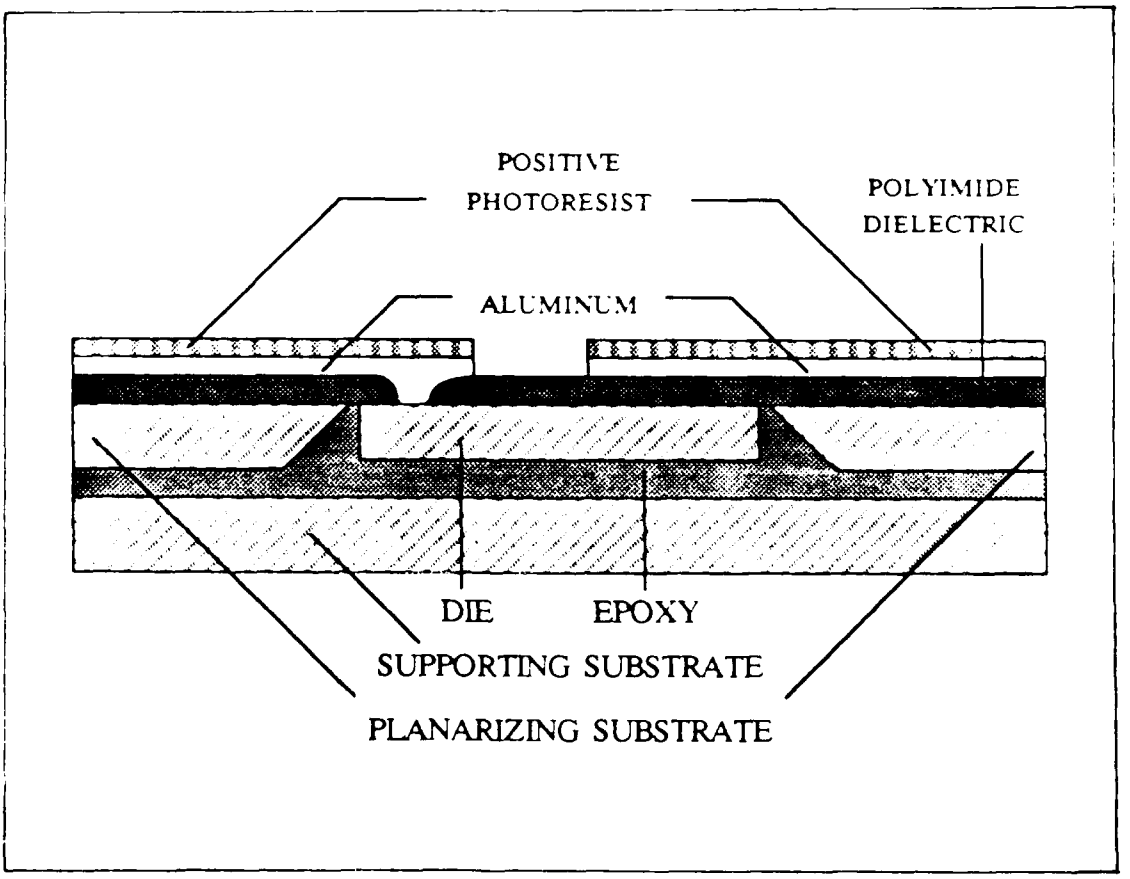

Figure 33. Aluminum Patterned Utilizing a Positive Photoresist Mask.

Fine line resolution can also be obtained with positive photoresist (64:4). The material was applied and patterned in the manner detailed for positive photoresist in the photolithography procedures of Appendix F.

Uncured Selectilux HTR 3-200 polyimide precursor was applied as an alternative photoresist material (Figure 34) as it purports to have greater planarization properties. Uncured, this polyimide was approximately 10 microns thick. When cured, Selectilux polyimide can be removed with Losalin HTR, an ethylene diamine based solvent produced by EM Industries (18:26). However, this technique proved to be incompatible with the polyimide used as the dielectric. It was expected that uncured

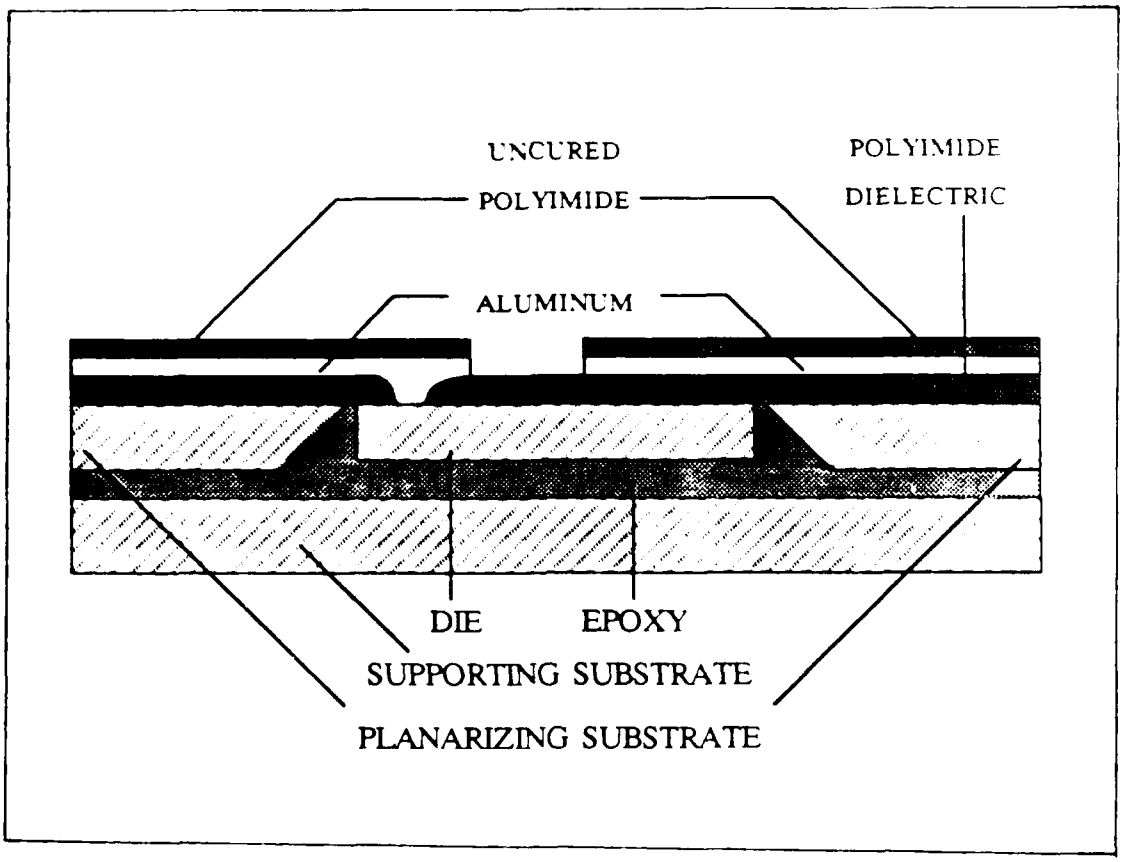

Figure 34. Polyimide Utilized As an Aluminum Etch Mask.

polyimide could be removed with other organic solvents (for example, acetone or trichloroethylene), which would be compatible with the polyimide used as the dielectric. This material was applied in the manner detailed in the polyimide processing procedures detailed in Appendix J.

Selectilux HTR 3-200 polyimide precursor partially cured at 160°C was prepared as an alternative material providing high planarization and high resistance to the aluminum etchant. According to the manufacturer, cure at this temperature will achieve 20 percent imidization (18:25). It was hypothesized that this material would not be removed during etching, and the material could be easily removed with organic solvents. Appendix J details the polyimide processing procedures performed.

Selectilux HTR 3-200 polyimide precursor hardbaked at 100°C was also evaluated as a material possessing the best properties of both the uncured and partially cured polyimide. A 20 micron thick layer of uncured polyimide was applied on the metal surface. The thicker layer was expected to provide greater protection against the etchant than the 10 micron thick layer used previously. According to EM Industries, Selectilux HTR 3-200 will not be imidized at 100°C (18:25). It was believed that the hardbake would drive off the solvents in the polyimide, making it more resistant to the etchant. However, by not imidizing the material, it was hoped that the material could be easily removed by organic solvents. Ammonium hydroxide was used in an attempt to remove the polyimide. As discussed in chapter II, partially cured polyamic acids can be removed with buffered mixtures of tetramethyl ammonium hydroxide and an organic acid. However, Wilson did not mention the manufacturer of this photoresist developer. Therefore, a 7:1 solution of water and ammonium hydroxide was prepared as a stripper.

As the final alternative, a hybrid combination composed of Shipley M1350J positive photoresist and the Selectilux HTR 3-200 was attempted (Figure 35). First, positive resist was applied and patterned using the mask design in Figure 30. An attempt was made to apply and pattern a successive layer of polyimide over the positive resist to cross the die-to-wafer transition only. The portions of the pattern masked only by positive resist would be easily removed with acetone. At the die-to-wafer transition, where planarity was a stringent requirement, removal of the resist would not be necessary.

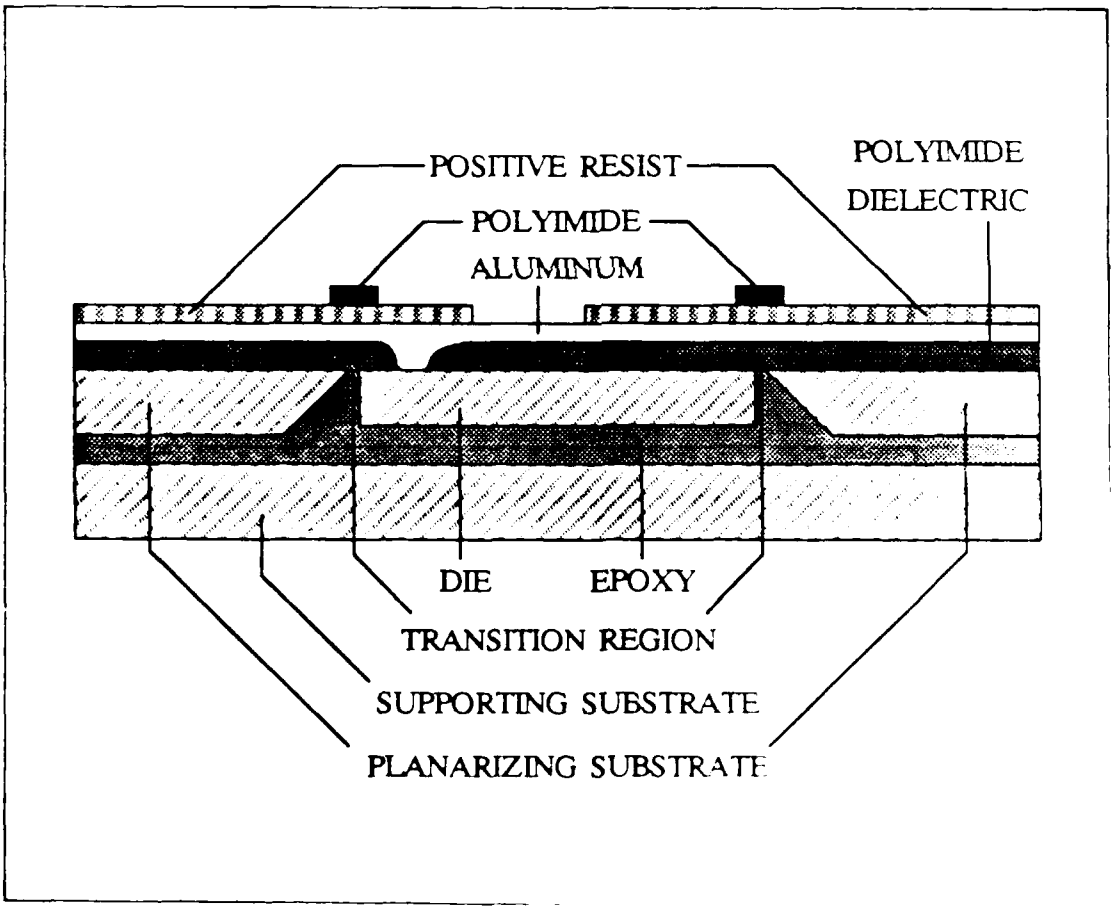

Figure 35. Intended Hybrid Mask - Photoresist and Polyimide

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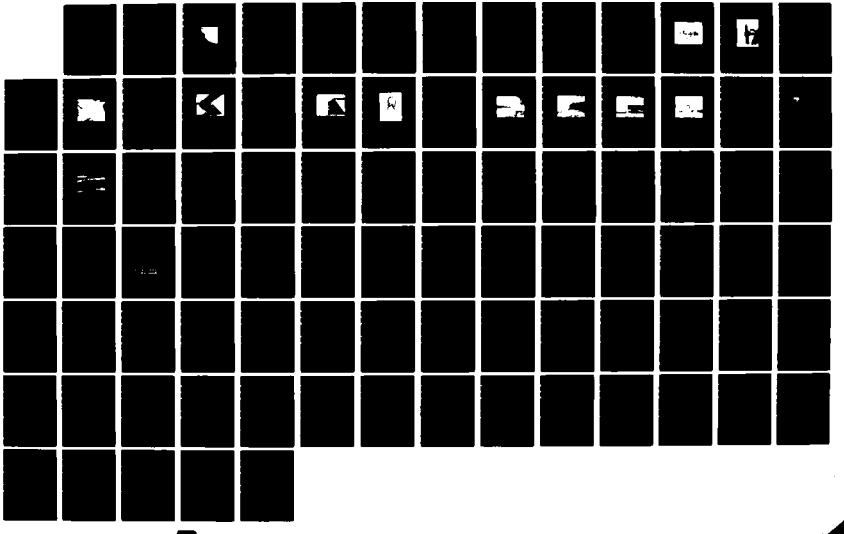

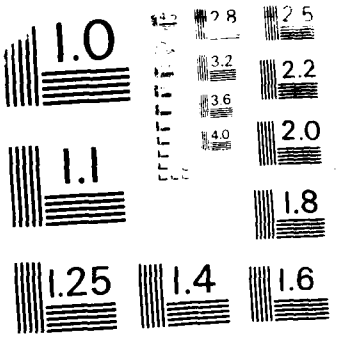

Summary. The wafer-scale circuits were fabricated in three steps: (1) substrate preparation, (2) die mounting, and (3) interconnection fabrication. Two substrate designs were considered before selecting a dual wafer design. Rectangular holes were anisotropically etched into the top wafer. The die were epoxied into the holes to planarize the wafer and die surfaces. An additional wafer was epoxied below the hybrid silicon structure to provide mechanical support. Printed lines were created with alternate layers of photosensitive polyimide and evaporated aluminum. The polyimide was characterized and patterned as the dielectric for the wafer-scale circuit. Then, aluminum was deposited over the dielectric, and several etch masks were evaluated against criteria for reliable interconnects. The final integrated wafer circuit is shown in Figure 36. In order to evaluate the success of the processing schedule, each completed wafer circuit was evaluated with electrical tests.

Test Procedures

Each wafer was functionally evaluated to determine if the interconnect runs and vias were continuous. All wafers with completely successful interconnects would have undergone a system test to determine the parametric behavior of the wafer-scale circuit. However, none of the wafers had a completely successful set of interconnects. Therefore, limited tests were performed on a wafer interconnect driven by the circuitry. This section describes the methods used to functionally evaluate the interconnects, and the procedures followed to evaluate the parametric behavior of a wafer-scale interconnect.

Functional Evaluation. After each wafer-scale circuit was fabricated, the success of the interconnects was confirmed by a continuity

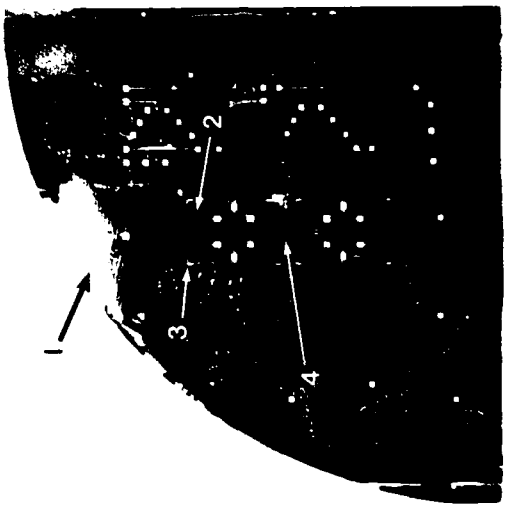

Figure 36. The Two Die Integrated by the Wafer-Scale Interconnects. (1) planarizing substrate, (2) Integrated circuit die, (3) via alignment marks, and (4) aluminum interconnects.

check along the runs and through the vias. Then, a circuit check was performed to insure that the die circuitry had survived the processing schedule.

Continuity Check. Figure 37 shows the common topographical obstacles encountered by the wafer-scale interconnects fabricated for this research. Using microprobes, an ohm-meter was connected across the interconnects from the external pad (point 1) to the via (point 4). If an open circuit was diagnosed on the meter, then the interconnect was inspected under an optical microscope to find the probable sites for open circuits. The wafer-to-die transition region (point 3) and the via step (point 4), were always selected as probable fault sites. However, other possible fractures along the interconnect runs were also found (point 2). Each fault location was isolated by moving the probe from the via (point 4) towards the pad (point 1). For instance, if continuity was established with the probe between points 3 and 4, poor via step coverage would be diagnosed.

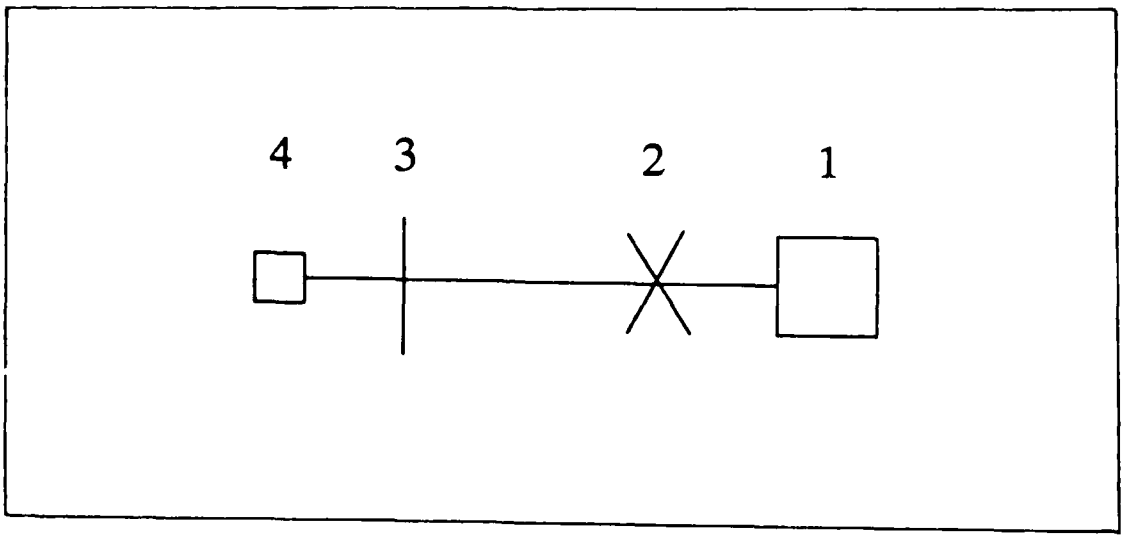

Figure 37. Test Points for the Interconnect Continuity Check

Circuit Check. Even if no faults were found on the wafer during the continuity checks, the wafer-scale circuit would not have functioned if the die circuits had been damaged during processing. Figure 38 illustrates a logic diagram of the die circuitry. The die pads were probed through the polyimide vias, and the circuits were excited with a test pattern.

Parametric Evaluation. As previously mentioned, none of the wafer samples had passed the functional evaluation without a fault. Therefore, one successful printed interconnect was electrically compared with a wire-bonded sample. Because the interconnect had to be excited by a CMOS driver, there were only two possible candidates per wafer for these tests. Therefore, a successful interconnect, terminated by a die circuit output pad, was selected for the tests.

Figure 39 is a schematic of the interconnect test arrangement. The CMOS inverter terminates and drives the interconnect at point A. The

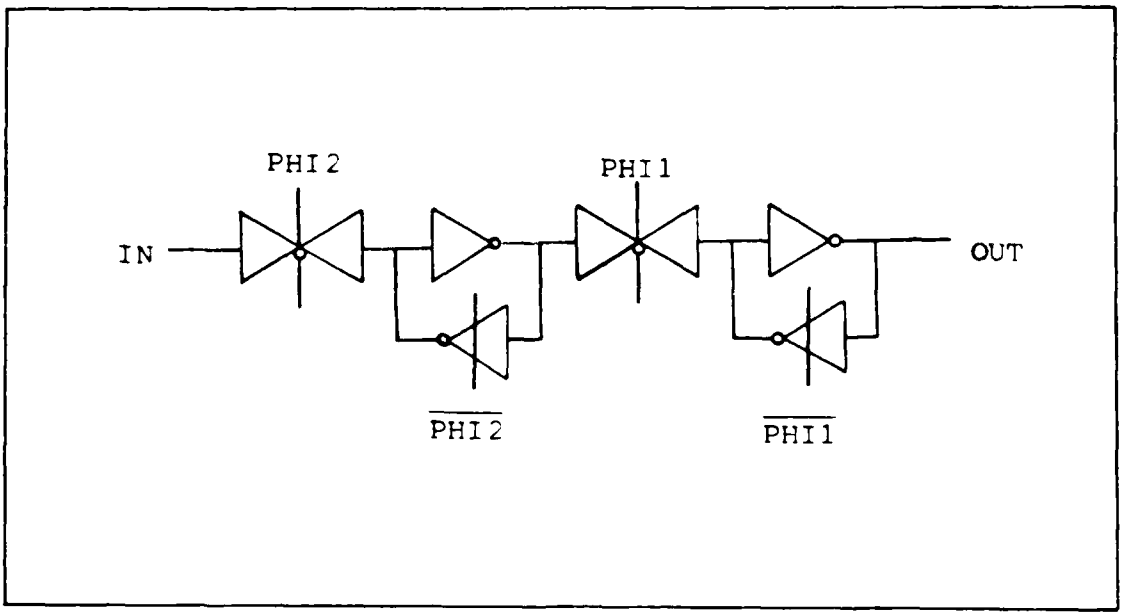

Figure 38. Logic Diagram of the Die Circuitry

signal propagates over the first dice, across the wafer surface, and to the second die. On the second die, the interconnect branches in two directions. One branch is terminated by the input of another inverter at point B. The other branch is left floating at point C. These paths were traversed by a printed interconnect and by a wire-bonded interconnect on separate wafers. Both interconnect samples were subjected to the same performance tests. Essentially, the signal was evaluated and measured for delay, attenuation, noise, and distortion using the Hewlett-Packard 54100A digitizing oscilloscope.

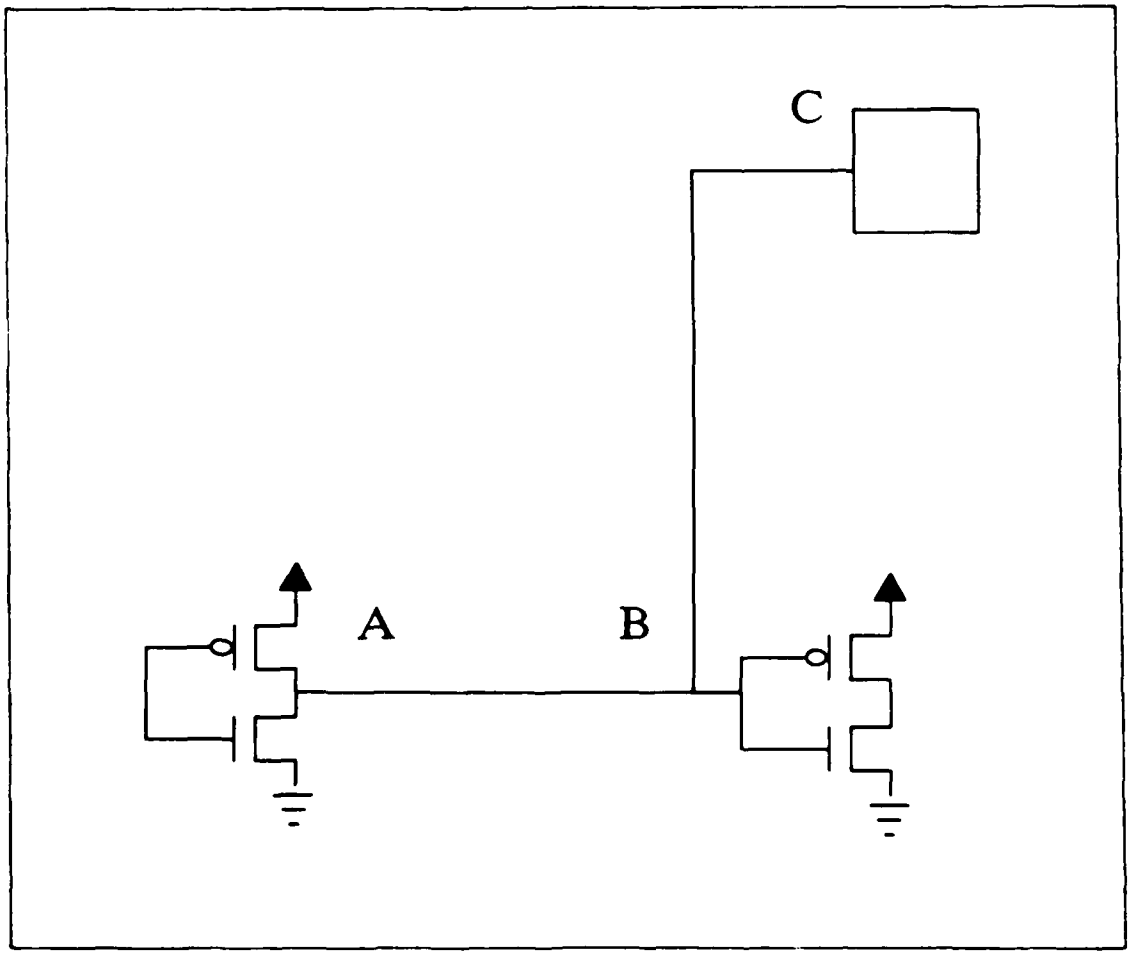

Figure 39. Schematic of the Parametric Test Set-up

The delay measurements will be performed using an arrangement similar to that used by Chang and others (10:8). The signal driven by the CMOS inverter at point A was measured between between points B and C using high-frequency probes. The oscilloscope was configured in the dual channel mode to compare the two signals. First, the signal waveform was recorded at point B, then the probe was moved to point C and the waveform was recorded and compared to the waveform at B. Because each probe varies in capacitance and resistance, only one probe could be used to obtain consistent attenuation measurements. Next the time delay was measured between the 50 percent rise voltages (Figure 40). These tests were

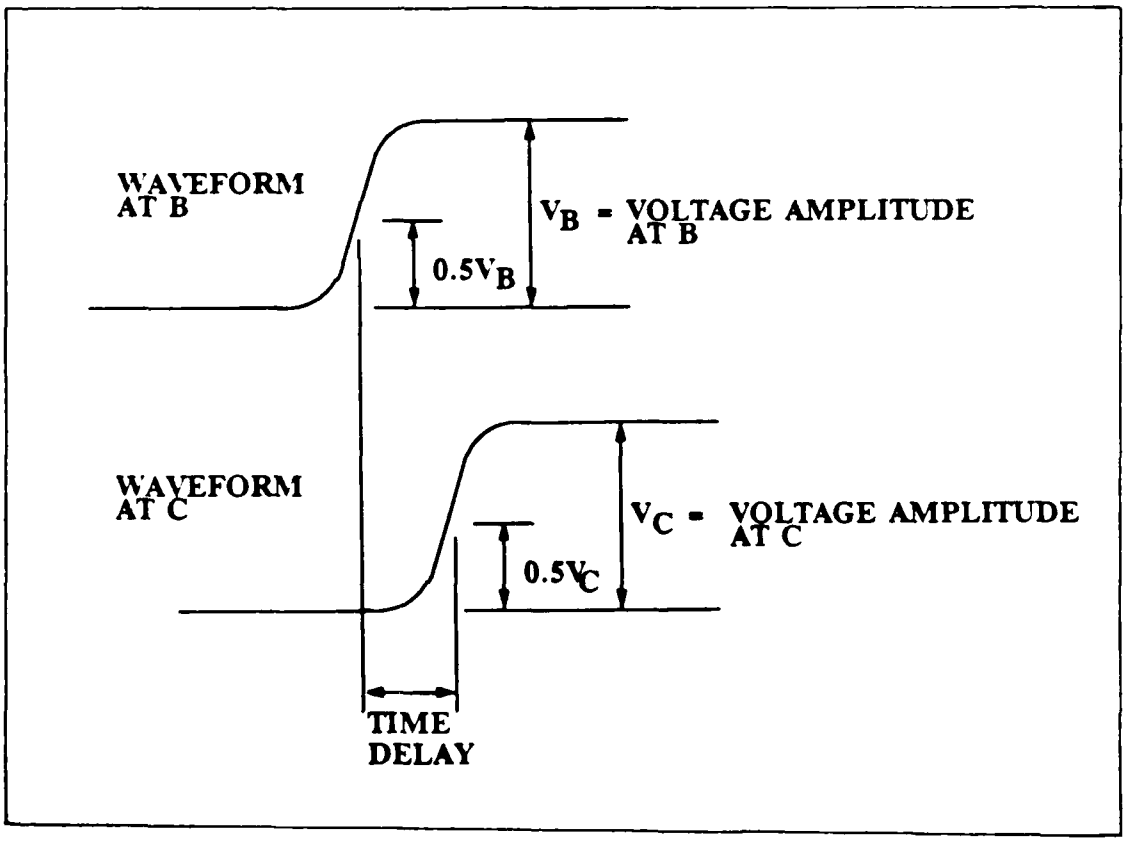

Figure 40. Time Delay Measurement Technique. The time delay is the time difference between the 50 percent rise voltages of the two signals.

performed in decade increments between 1 kHz and 10 MHz, which is the maximum frequency limit for the equipment and circuit used for these tests.

Because the HP 54100A automatically measures risetimes and RMS voltage. The signal was evaluated for distortion during the same tests performed for the delay measurement. The noise levels were also evaluated during these tests.

IV. Results and Discussion

This chapter details the results of the experiments described in Chapter III. First, the effectivity of the wafer-scale interconnects will be evaluated in a discussion of the electrical test results. Then, these test results will be analyzed, and the source of failures or success will be postulated from the intermediate results discovered during processing. First, the continuity test results wil be evaluated. Then, the results of the parametric tests will be evaluated.

Continuity Results

Overall, the fabrication of a hybrid-silicon wafer-scale integrated circuit was not completely successful. The primary failure was open circuits in the interconnect conductors. These faults occurred in the transition region between the wafer and the die, and at the edge of the vias formed in the polyimide. However, many of the processing steps achieved promising results. This section will highlight both the difficulties and the successes encountered throughout each of the three basic processing steps.

Open Circuits in the Wafer-to-Dice Transition Region. The interconnects created with positive resist were tested for electrical continuity. The interconnect network used for this research encounters the wafer-to-die transition region a total of sixteen times per wafer. Twelve of these crossings passed the continuity check, resulting in a 75 percent success rate. After the test, an interconnect successfully traversing this transition was examined with a scanning electron microscope (SEM). For comparison, an unsuccessful crossing was also

inspected. The associated photographs are shown in Figures 41 and 42. Note that the fractured interconnect (Figure 41) was forced to pass over a very large void in the wafer-to-die transition region. This severe step could be the source of the break. If the step was not completely planarized by the polyimide dielectric, the remainder of the step would have to be planarized by the subsequent aluminum deposition and positive resist mask. However, the continuous line (Figure 42) crosses over a virtually fault free transition region with only a minor loss of resolution.

In Figure 41, the line narrows slightly at the edges of the transition region and widens in transition region itself. This phenomenon could be the result of the planarization properties of the photoresist and the diffractive effects of proximity printing. Figure 43 is a cross-sectional diagram depicting the exposure of photoresist on an uneven surface. An uneven surface of this type was created by a dip in the polyimide dielectric surface. This dip could be the result of the incomplete fill of epoxy in the transition region. Due to the smoothness of the wafer and die, flat surfaces are reestablished to the left and right of this valley. The photoresist attempts to planarize these steps by depositing a thicker coating in the valley and a thinner coating at the step edges. From Equation 35, the photoresist features will vary from the mask as determined by the exposure energy (E_i), the gap between the wafer and the mask (z), and the threshold energy of the photoresist (E_T). However, this equation was formulated for negative resist. As a result of proximity printing, the positive photoresist features will increase rather than decrease in size. Assuming that the exposure energy does not vary across the surface of the wafer, only the threshold energy and the wafer-to-mask

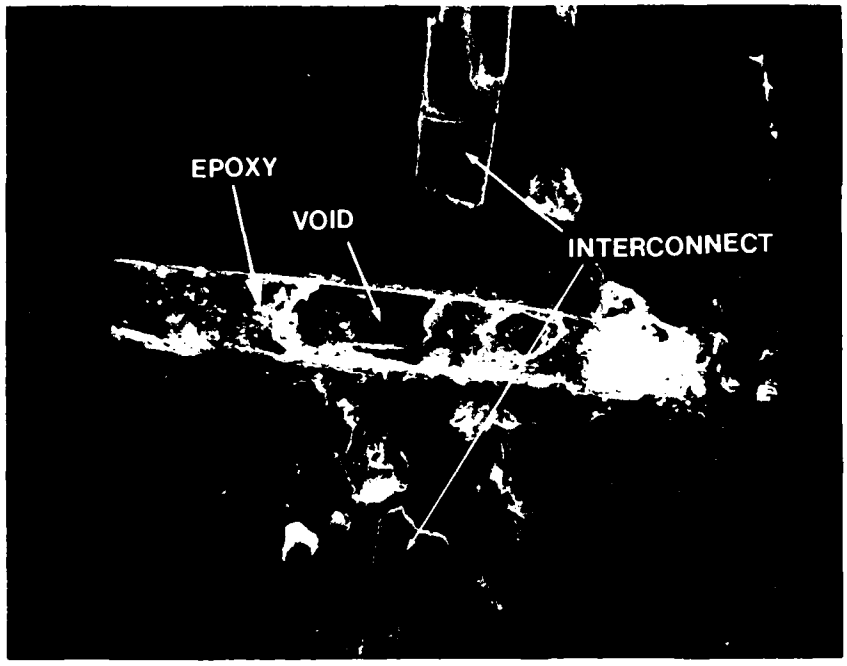

Figure 41. Interconnect Fractured at the Wafer-to-Die Transisition. SEM photograph at 400 X magnification.

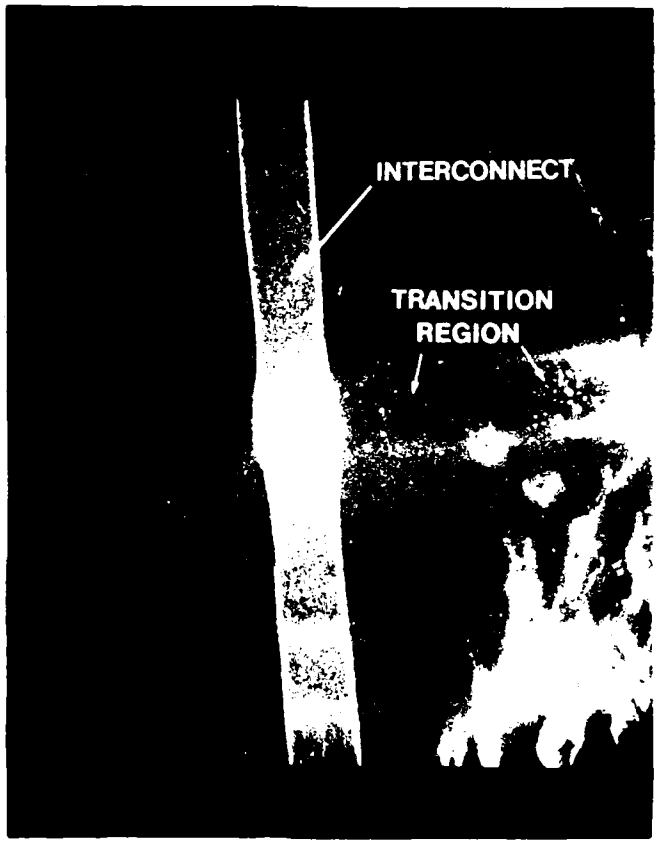

Figure 42. Interconnect Successfully Crossing the Wafer-to-Die Transition Region. SEM photograph at 400 X magnification.

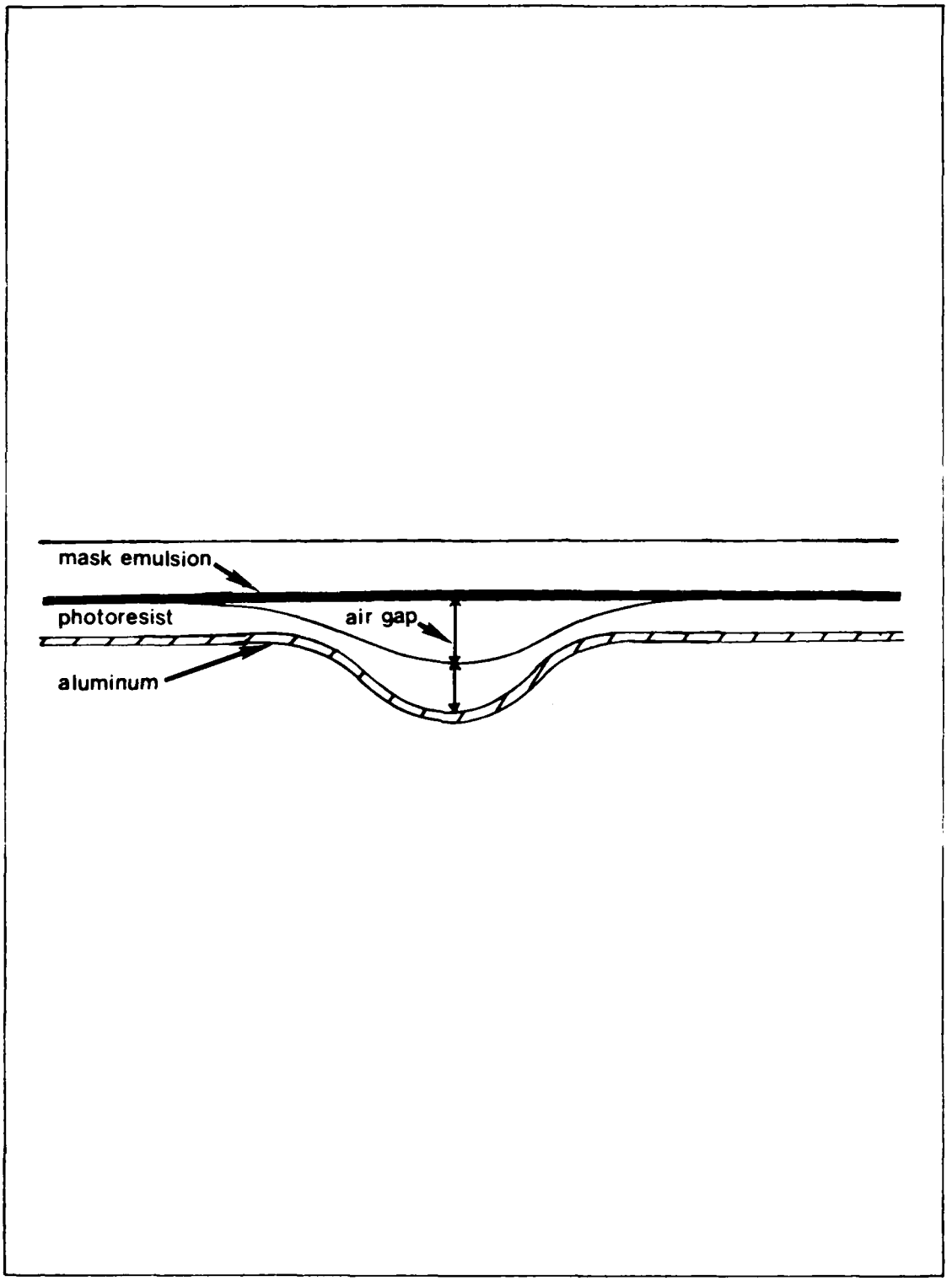

Figure 43. Cross-Sectional Diagram Depicting the Exposure of Photoresist on an Uneven Surface.

separation will change across the transition. Also, the threshold energy is smaller for thinner layers of photoresist. Therefore, at the step edges, where the photoresist layer is thinnest, the threshold energy is lowest. In addition, a separation between the mask and the wafer has been created. These parameter variations combine to increase the difference between the mask and photoresist features (See Equation 35). This difference is observed as a narrower linewidth at the edges of the transition region (Figure 42). In the surface valley, where the photoresist layer is the thickest, the threshold energy is the greatest. If E_T grows larger than kE_i, the difference between the mask and photoresist features will become negative. This difference is noted as the wider linewidth directly over the transition region (Figure 42). In some cases, the linewidth in the transition region expanded so much that a short between two interconnects was barely averted. Figure 44 is a SEM photograph of a transition region after the aluminum was etched. The aluminum covers the entire transition, and the line at the left of the transition is clearly attached to this aluminum.

A large fracture in an interconnect could be the result of inadequate step coverage by the polyimide layer. A void in the wafer-to-die transition region can create two very abrupt steps which the polyimide may have difficulty planarizing. As a result, the subsequently applied photoresist layer would have the same difficulty over the step. As shown in Figure 41, the photoresist might have covered most of the uneven surface. However, as the photoresist nears the step edge, the layer becomes gradually thiner until the resist disappears at the step. When the wafer is immersed in the aluminum etchant, the photoresist pattern will slowly creeped away from the transition region, exposing the bare

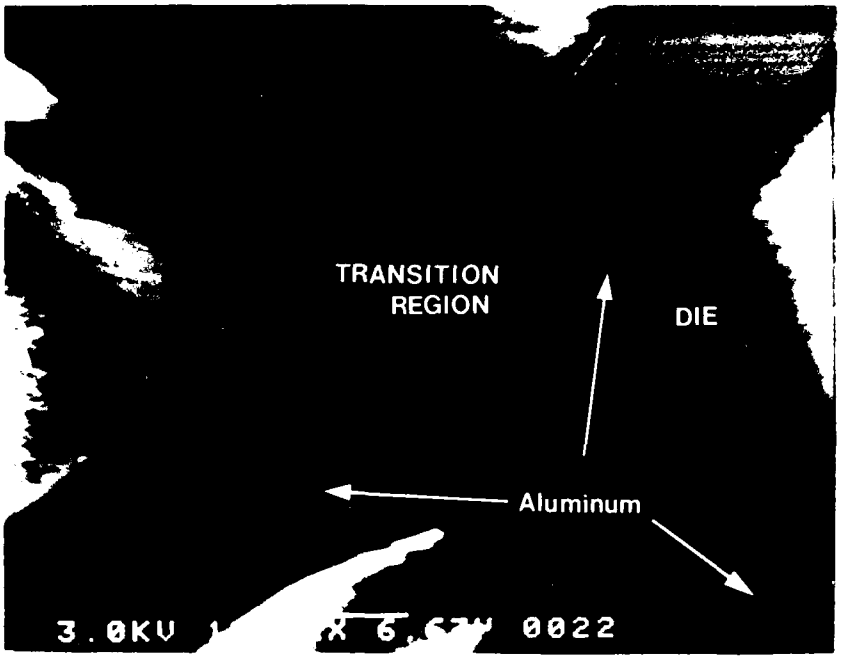

Figure 44. Interconnect Spreading Throughout the Transition Region. SEM photograph at 1500 X magnification.

aluminum to the etchant. At the end of the etching time, a sizable break could be etched into the interconnect.

Therefore, continuous interconnects could be compromised by three inadequacies in the processing schedule: (1) the uneven fill of epoxy in the wafer-to-die transition region, (2) poor step coverage by the polyimide dielectric over the severe transition region topography, and (3) inadequate planarization by and exposure of the photoresist mask.

The Uneven Fill of Epoxy in the Transition Region. The uneven fill of epoxy was very severe in some cases. The die mounting technique was examined for planarity using an optical microscope. Prior to the 250 C epoxy curing cycle, a control wafer was examined at four points along the wafer-to-die transition. Table 6 tabulates the heights of the two steps created at the wafer-to-die transition.

In three of the four measurements recorded in Table 6, the epoxy filled the transition region above the level of the wafer and die surfaces. Figure 45 is a SEM photograph of the wafer-to-die transition

Table 6. Planarization Data For the Wafer-to-Die Transition Region Prior to the 250°C Curing Cycle

Point Measured	Step Distance From the Wafer Surface to the Surface of the Transition Region (microns)	Step Distance From the Surface of the Transition Region to the Die Surface (microns)
1	9.5	- 28.5
2	- 5.0	- 8.0
3	16.5	- 21.0
4	9.5	- 21.5

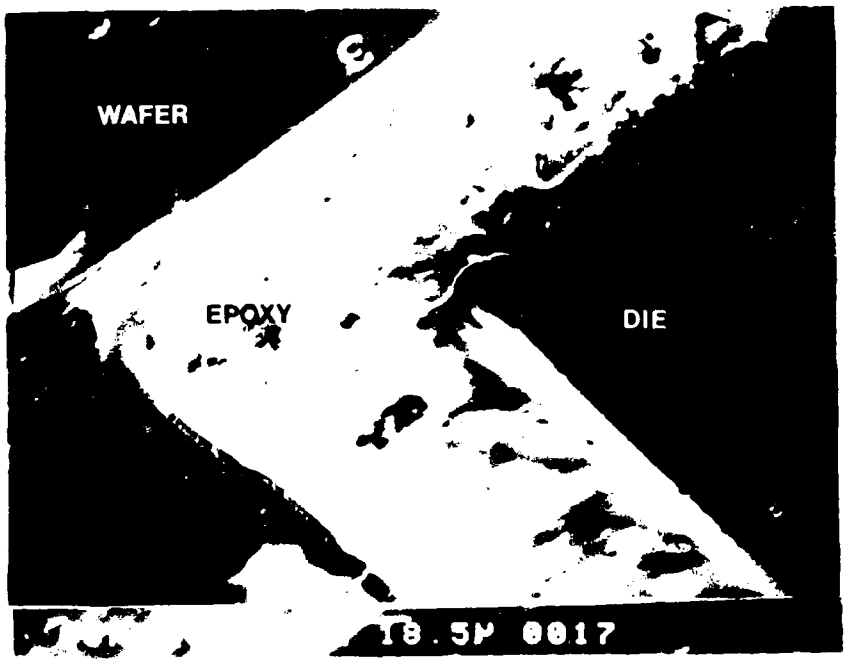

Figure 45. Top View of the Wafer-to-Die Transition Region. The die is to the right and the wafer is to the left of the photograph. Note that the epoxy is above the wafer and die surfaces. SEM photograph at 540 X magnification. Scale: 18.5 um / cm.

prior to the 250°C epoxy curing cycle. Note that the epoxy is indeed above the level of the wafer and die surfaces. During the die mounting processing step, epoxy frequently seeped between the planarizing substrate and the optical flat. This seapage could have caused some of the epoxy to harden above the wafer and die surfaces.

As previously discussed, the incomplete fill of epoxy in the transition region was also observed. Figure 46 is an SEM photograph of the substrate cross-section after the die are bonded. The fill is solid throughout the die-to-wafer transition; however, the epoxy does not reach the level of the wafer and die surfaces. This gap in the epoxy could be caused when the die are bonded into the planarizing substrate. When the epoxy was deposited into the transition region, air could have been trapped against the optical flat. Another hypothesis could attribute these voids to the redistribution of epoxy during the 250°C curing cycle.

Breaks in the Vias. Of the twelve vias developed in the polyimide dielectric layer, only one was unsuccessfully covered by the metallization pattern. Figures 47 and 48 are SEM photographs comparing a successful and an unsuccessful coverage of aluminum into the via. In Figure 47, the metal run clearly reaches the edge of the via; however, in Figure 48, the run stops about 50 microns short of the via. The depth of the vias were measured using an optical microscope. The via depth was calculated as the difference between the focal points of the via bottom and the dielectric surface. The unsuccessful via was 3.0 microns deep. This was the shallowest of the twelve vias. The remaining vias ranged from 7.0 to 12.0 microns in depth.

As previously mentioned, breaks in across the via edge can be averted by sloping the sidewalls using proximity printing. Two brief experiments

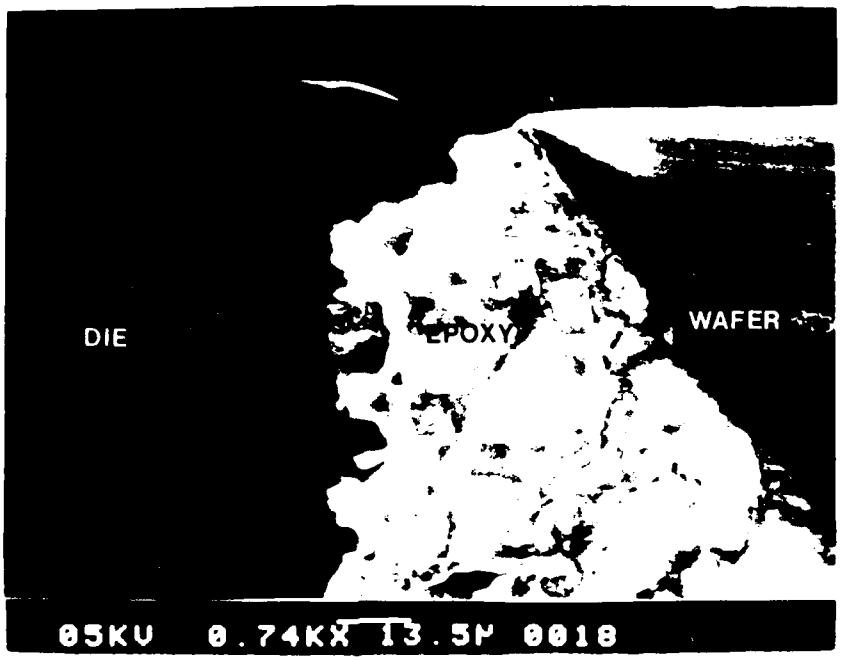

Figure 46. Cross-Section of the Wafer-to-Die Transition. The dice is to the left and the wafer is to the right of the epoxy. The epoxy fill is below the level of the dice surface. SEM photograph at 740 X magnification.

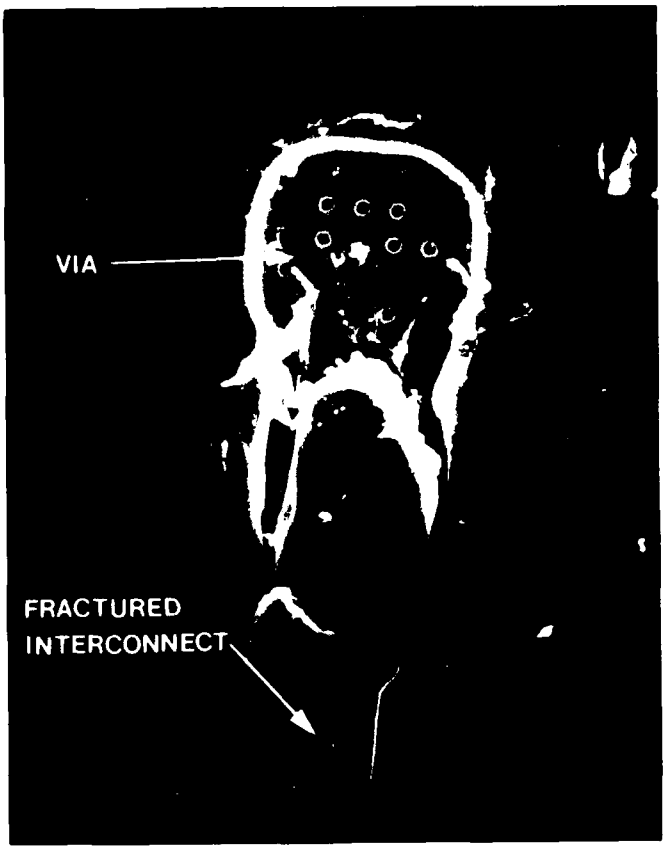

Figure 48. An Unsuccessful Via. Note that the interconnect run (lower portion of photograph) does not meet the via edge. The tears in the polyimide was caused by probing during the continuity tests. SEM photograph at 800 X magnification.

were conducted to gauge the effect of proximity printing on sloped via sidewalls. First, several unprocessed wafers were coated with the same thickness of polyimide precursor (approximately 10 microns prior to cure). Each wafer was exposed to a constant ultraviolet energy source (about a 400 mJ/cm^2 intensity). However, the wafer-to-mask separation was varied for each wafer. Table 7 describes the various wafer-to-mask separations subjected to the test, and a description of the resulting via sidewall profiles.

A second series of tests were performed by varying the exposure energy and the thickness of the polyimide layer. The wafer-to-mask separation was kept constant with a contact exposure for each test. After the polyimide was developed, the vias were measured with the Dektak surface profile measuring system. These measurements are documented in Table 8.

Table 7. Proximity Printing Results with the Wafer-to-Mask Separation Varied.

Separation Method	Wafer-to-Mask Separation (microns)	Results
Contact	-----	Sharp 100° step (Figure 49)
Air Gap	10	Smooth 110° step with slight undercut (Figure 50)
	70	Smooth 110° step with large undercut (Figure 51
	140	Smooth 100° step (Figure 52)

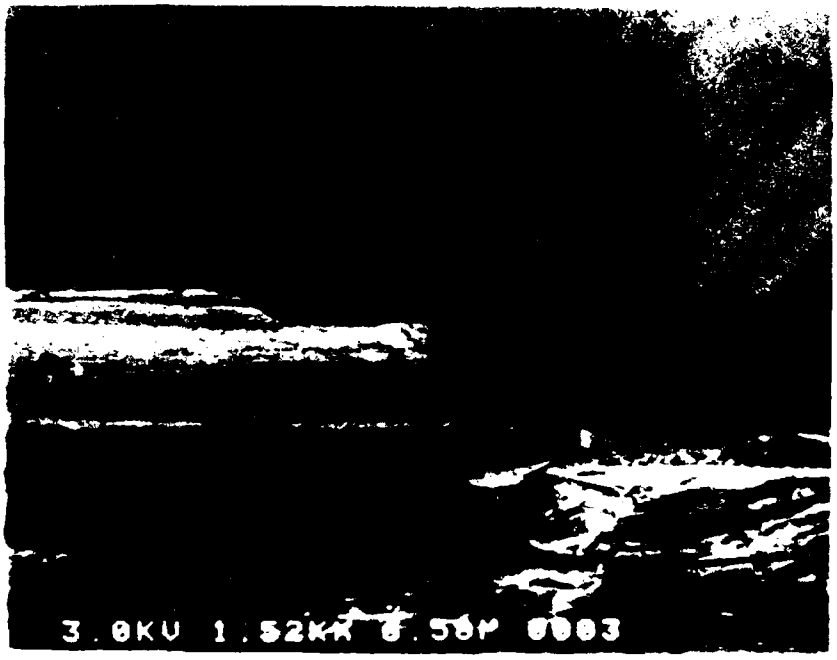

Figure 49. Polyimide Via Step After a 400 mJ/cm^2 Contact Exposure. Note the sharpness of the step. SEM photograph at 1520 X magnification.

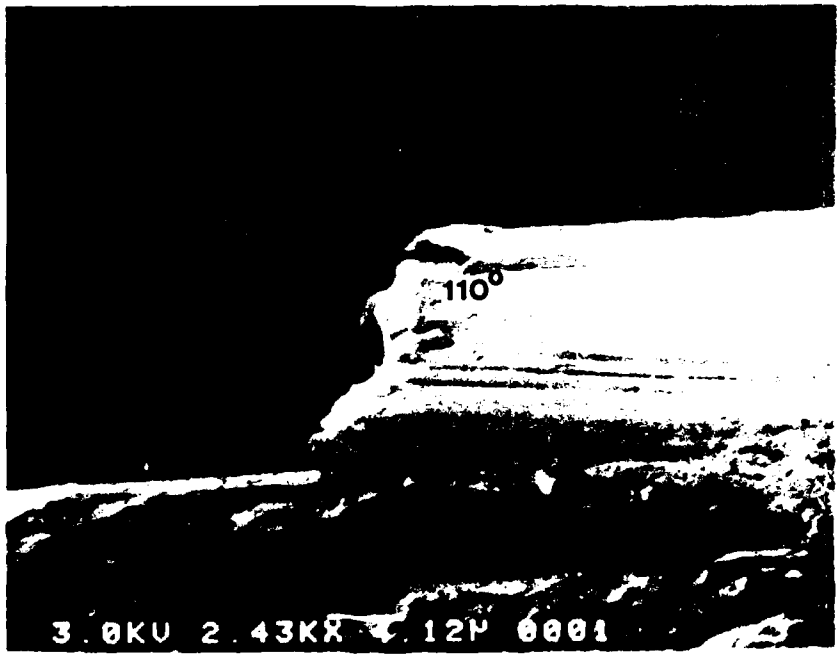

Figure 50. Polyimide Via Step After a 400 mJ/cm^2 Proximity Exposure and a Wafer-to-Mask Separation of 10 Microns. Note the smooth transition at the step. SEM photograph at 2430 X magnification.

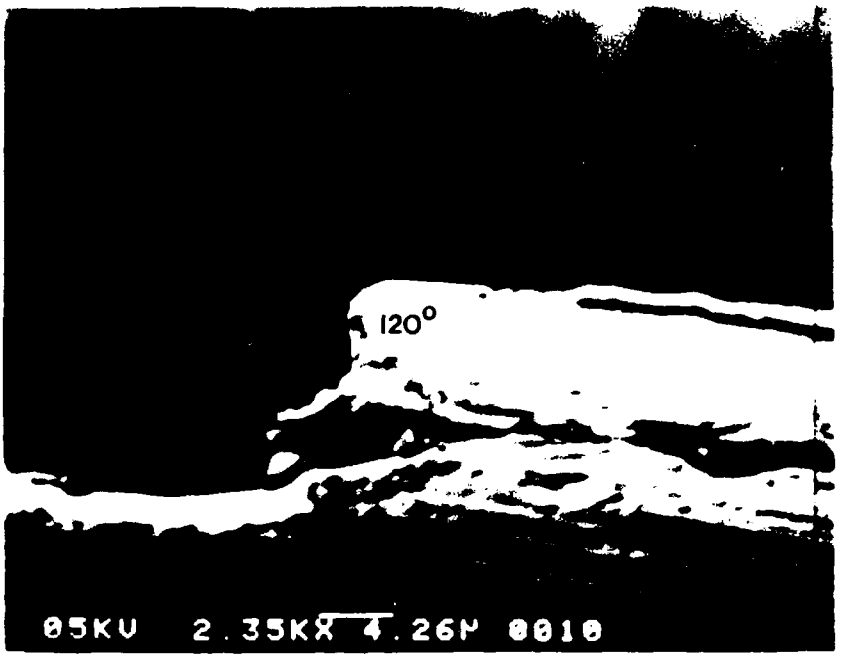

Figure 51. Polyimide Via Step After a 400 mJ/cm^2 Proximity Exposure and a Wafer-to-Mask Separation of 70 Microns. There is a very pronounced under cut below the step. SEM photograph at 2350 X magnification.

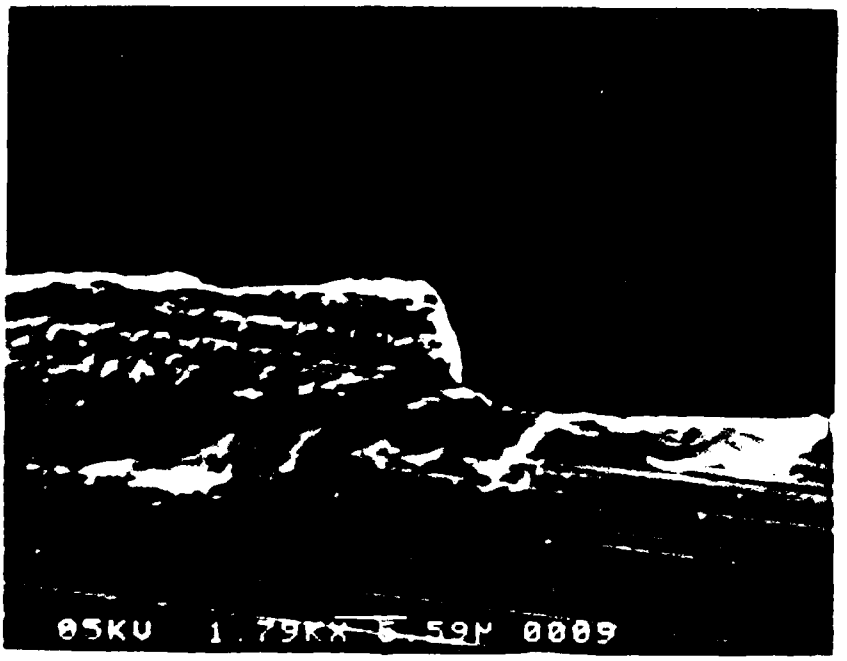

Figure 52. Polyimide Via Step After a 400 mJ/cm^2 Proximity Exposure and a Wafer-to-Mask Separation of 140 Microns. The under cut is gone, and the sidewall slope is degrading. SEM photograph at 1790 X magnification.

Table 8. Proximity Printing Results With the Exposure Energy and the Layer Thickness Varied

Exposure Energy (mJ/cm^2)	Polyimide Thickness (um)	Via Depth (um)	Via Width (um)
240	33	25	110
145	24	22	125
180	27	23	120
250	24	18	50
165	20	19	120
215	20	20	50

Inadequate Planarization of the Photoresist Mask. Of the five etch mask techniques attempted, only the positive resist and the uncured polyimide produced interconnects that could be tested for continuity. The other three methods did not produce interconnect patterns suitable for testing.

The Shipley positive resist exhibited excellent characteristics as an etch mask for the metallization step. For an aluminum thickness of 1.2 microns, the photoresist maintained its masking properties in the aluminum etchant. After the etch was completed, the remaining resist was easily removed by a short soak in acetone. Figure 53 is an SEM photograph of the resulting interconnect. Note that the interconnect line width is consistently 25 microns. However, as noted earlier, the step coverage over the wafer-to-die transition and the via sidewalls was not 100 percent successful (See Figures 41 and 48).

Figure 53. Line Resolution Developed with Shipley M1350J Positive Photoresist as the Mask. SEM photograph at 1900 X magnification.

A 10 micron thick layer of uncured Selectilux HTR 3-200 polyimide was applied as an etch mask for the metallization step. After etching the aluminum, 15 of the 16 transition crossings passed the continuity check, and all the vias sidewalls were covered. However, the polyimide did not survive the etchant. Although most of the polyimide was removed during etching, some of the polyimide still remained along the edges of the line (Figure 54). In addition, the line width produced with a polyimide mask was just over 30 microns (Figure 54).

The planarization capabilities of both the positive resist and the polyimide etch masks were examined after the aluminum etch. Each of the sixteen locations where the interconnect crosses the transition were examined under an optical microscope. The step heights were measured as the difference between the focal points of each surface. From these measurements, the highest step successfully protected from the etchant, and the lowest step unsuccessfully protected from the etchant are tabulated in Table 9. From this Table, the maximum step height coverage obtainable with 10 micron thick uncured polyimide etch mask was nearly

Table 9. Step Height Coverage by Resist Masks Over the Transition Region Steps

	Positive Resist Mask	Uncured Polyimide Mask
Highest Step Covered	13 microns	31 microns
Lowest Step Uncovered	11 microns	32 microns

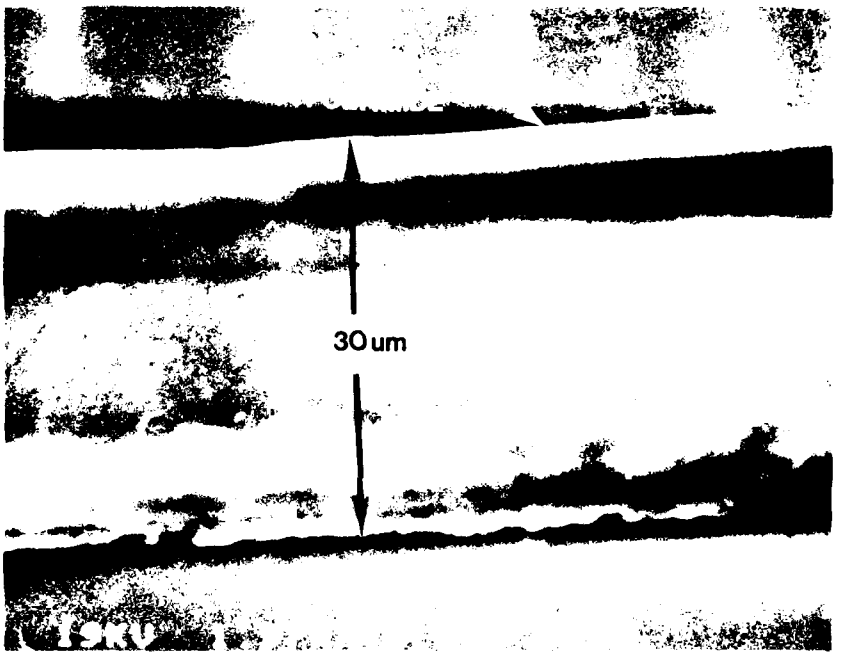

Figure 54. Line Resolution Developed with Uncured Selectilux HTR 3-200 Polyimide as the Mask. Note that the line is wider than the line created with positive resist. Remnants of polyimide are still along the sides of the line. SEM photograph at 1970 X magnification.

three times as high as the maximum step height covered by the 1.6 micron thick positive resist.

Both the partially cured (i.e. 160°C) Selectilux polyimide and the hardbaked polyimide (i.e. 100°C) had all the positive features of the uncured polyimide. In addition, both showed excellent resistance to the etchant. However, in both cases, the resist could not be removed. An attempt to remove the partially cured polyimide with a room temperature soak in Losalin HTR was unsuccessful. After soaking for 10 minutes, the resist had not been removed. But, the aluminum pattern began to separate from the wafer's surface. The hardbaked polyimide was not removed after a one hour soak in acetone and a subsequent 30 minute soak in trichloroethylene. After these two attempts to remove the resist, the wafer was soaked in an ammonium hydroxide solution. After about 15 minutes, the polyimide dielectric layer began to lift away from the wafer; however, the polyimide resist layer remained on the aluminum.

The hybrid mask of Shipley positive resist and Selectilux polyimide was never successfully patterned. Although the positive photoresist was easily patterned, the subsequent application of polyimide immediately dissolved the remaining photoresist. It is suspected that the positive photoresist may have been dissolved by organic solvents in the polyimide precursor.

After the continuity tests, the wafer interconnects etched with the positive resist mask were parametrically tested.

Parametric Results

Prior to the parametric tests, the dimensions of the printed interconnect were measured and recorded in Table 10. The wirebonded

Table 10. Dimensions of the Printed and Wire-Bonded Interconnects

Section	Printed Interconnect	Wire-Bonded Interconnect
metal width (um)	26.0	-----
metal thickness (um)	1.2	-----
dielectric thickness (um)	9.0	-----
wire diameter (um)	-----	25.4
length from A to B (um)	6590.0	3770.0
length from A to C (um)	22578.0	11580.0

interconnect dimensions are also included in Table 10.

Four of the integrated circuit die were tested to confirm that the circuits had not been damaged by the processing schedule. All the circuits passed this functional test, even when the circuit was clocked at 20 MHz. The two-bit shift register drove the output (A) (Figure 39) at 10 MHz. Figure 55 depicts the two waveform plots recorded by the Hewlett-Packard digitizing oscilloscope. The input is latched on the output after two positive transitions of the PHI1 clock (Figure 38).

The circuit output (A) drove the interconnect at 10 MHz, while points B and C were probed to determine the effect of the interconnect run between B and C (Figure 39). The waveforms are compared in Figure 56. There is no discernable signal delay, attenuation, or distortion between the B and C waveforms. The noise can be attributed to switching

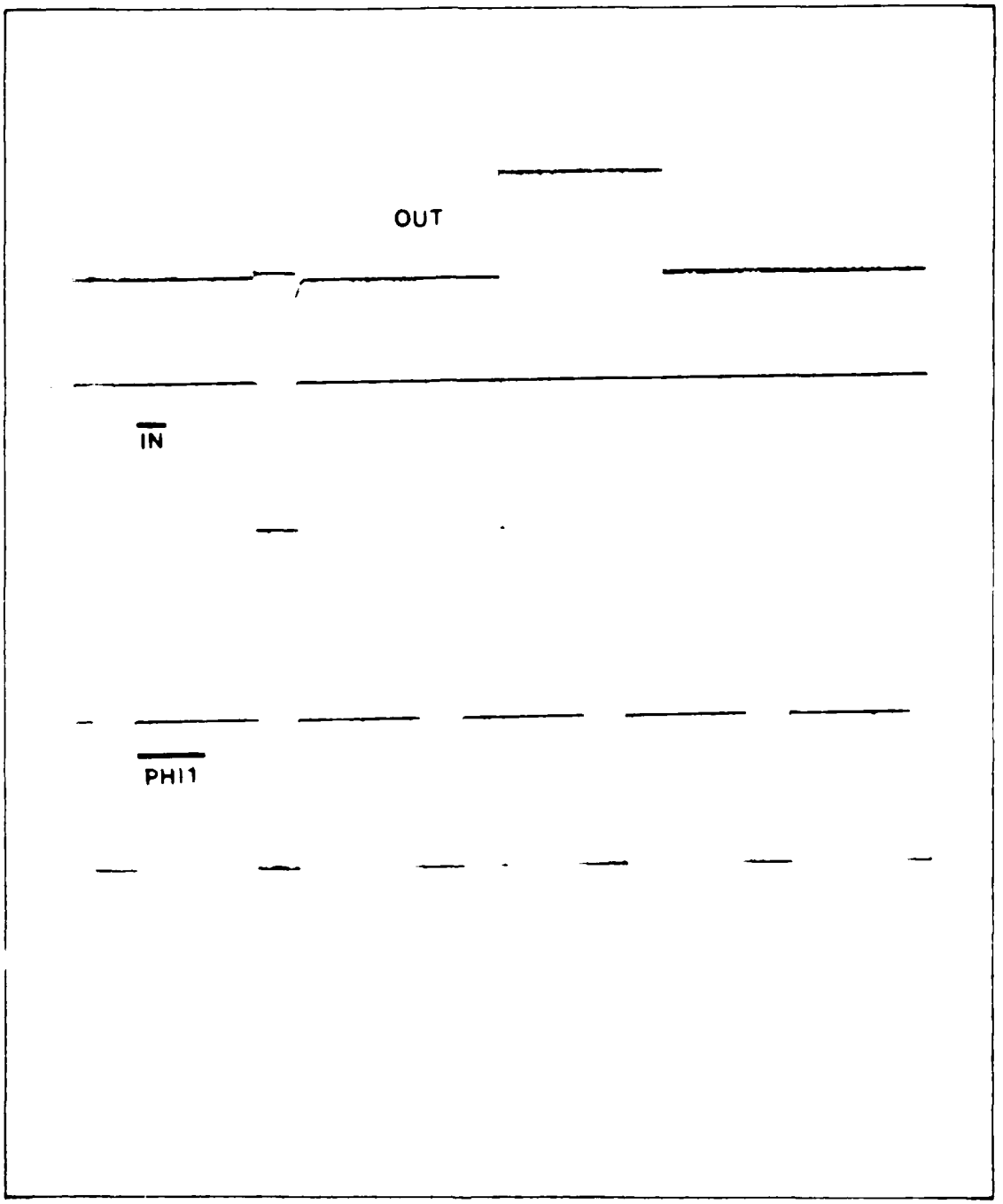

Figure 55. Waveform Traces Confirming the Correct Function of the Die Circuit. The input (IN) is latched at the output (OUT) after two positive transitions of the clock (PHI1). IN and PHI1 were actually the inverse of their displayed waveforms. The die circuit is diagramed in Figure 38. Vertical axis: 2 volts/division. Horizontal axis: 500.0 usec/division.

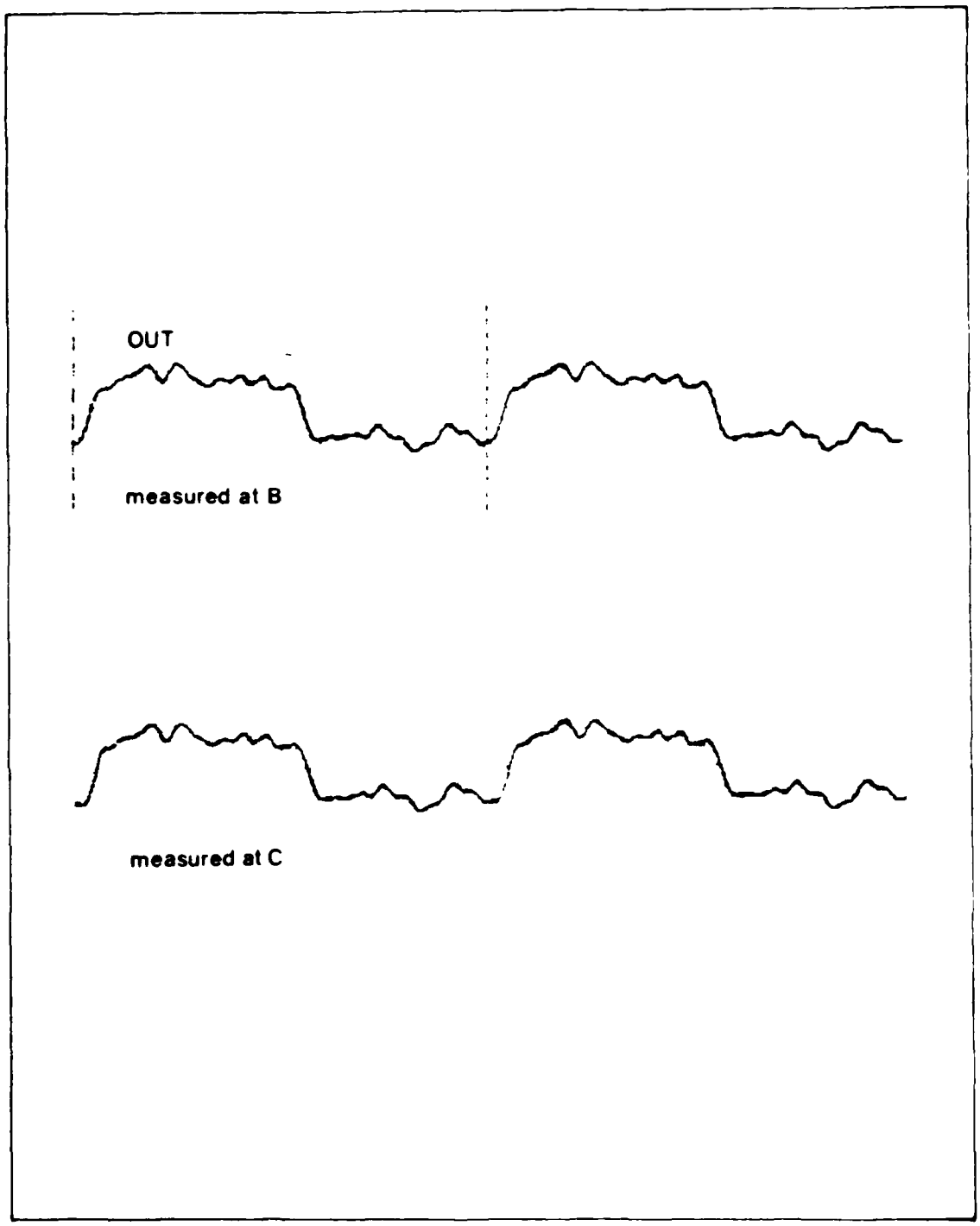

Figure 56. Waveform Traces at Points B and C of the Printed Interconnect at 10 MHz. There is no discernable signal delay, attenuation, or distortion between the two waveforms. These points are highlighted in Figures 32 and 39. Vertical axis: 2 volts/division. Horizontal axis: 20.0 nsec/division.

transients in the circuit. Figure 57 shows that the noise peaks occur onthe rising and falling edge of the clock PHI2.

With the output driven at 1 MHz, the wire bonded interconnect (Figure 58) was compared to the printed interconnect (Figure 59) at points B and C. The printed interconnect displays very little signal distortion along the interconnect. A rise time of 10 ns was measured in both cases. However, the distortion in the wirebonded interconnect is now noticeable between points B and C.

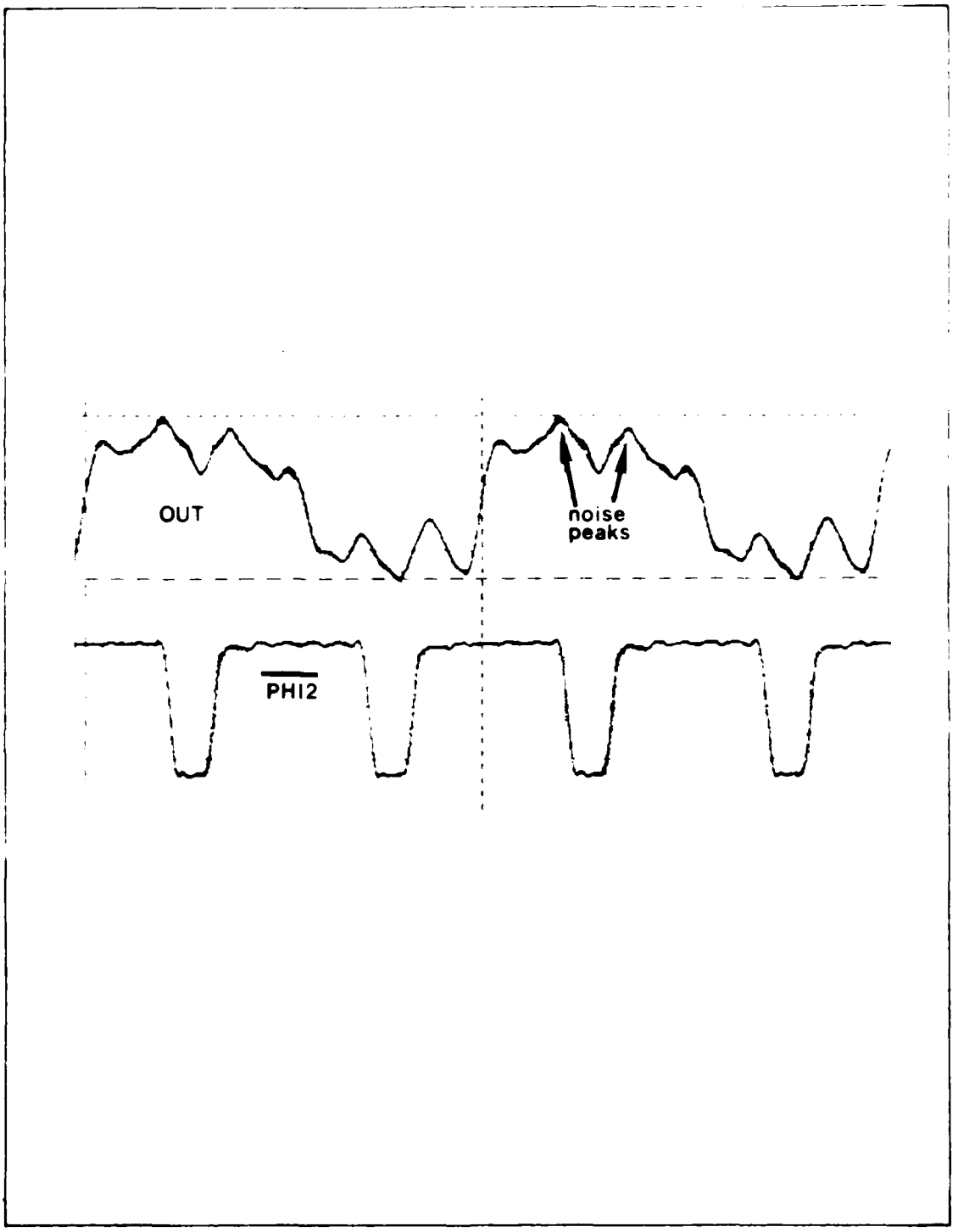

Figure 57. Evidence of Noise Tied to Switching Transients in the Circuit. Note that the noise peaks at OUT correspond to the edge transitions of PHI2. Vertical axis: 2 volts/ division. Horizontal axis: 20.0 nsec/division.

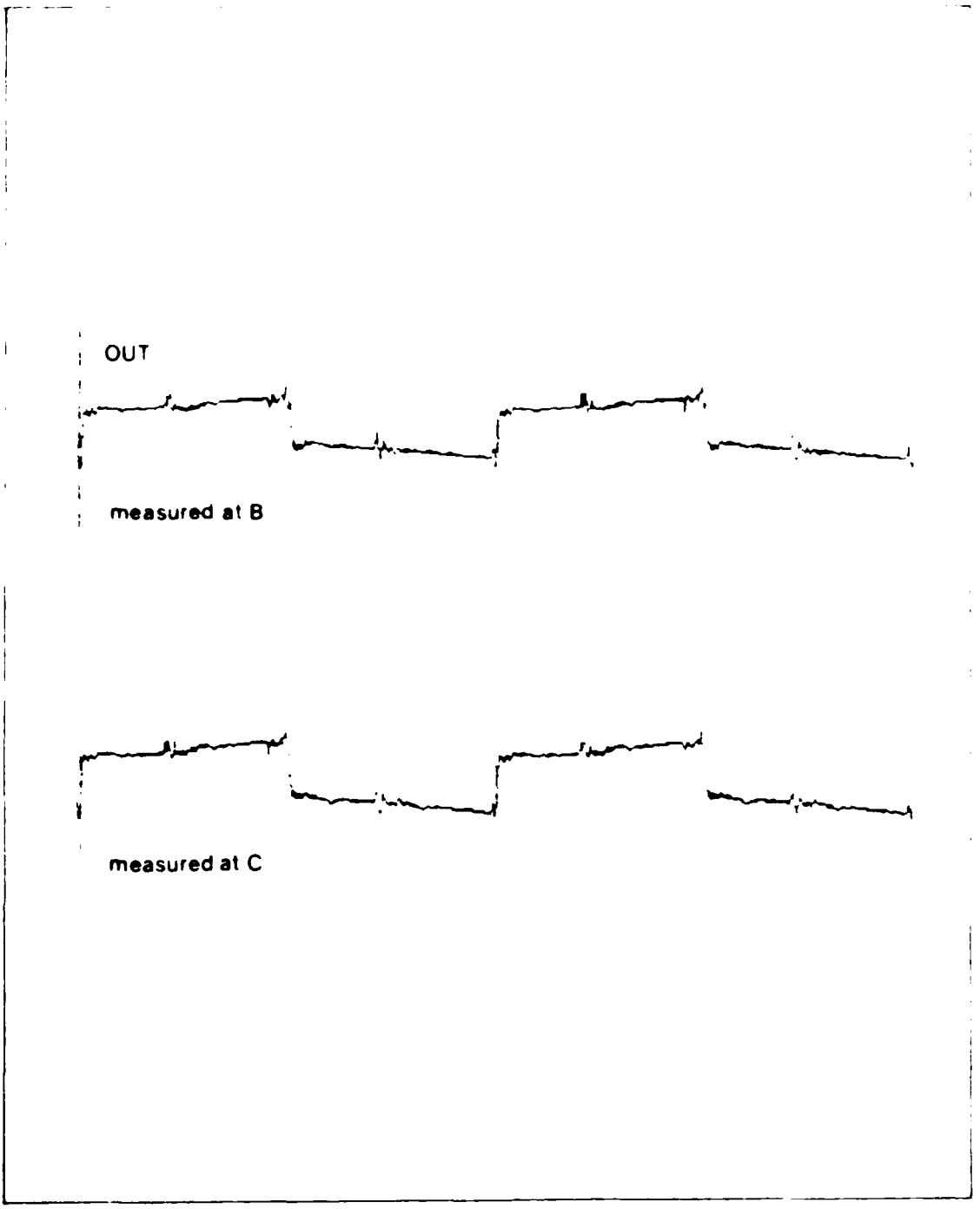

Figure 58. The Output Signal Measured Along the Printed Interconnect at Points B and C at 1 MHz. These points are highlighted in Figures 32 and 39. There is less distortion in the waveform compared to the wire-bonded interconnect (Figure 59). Vertical axis: 2 volts/ division. Horizontal axis: 200.0 nsec/division.

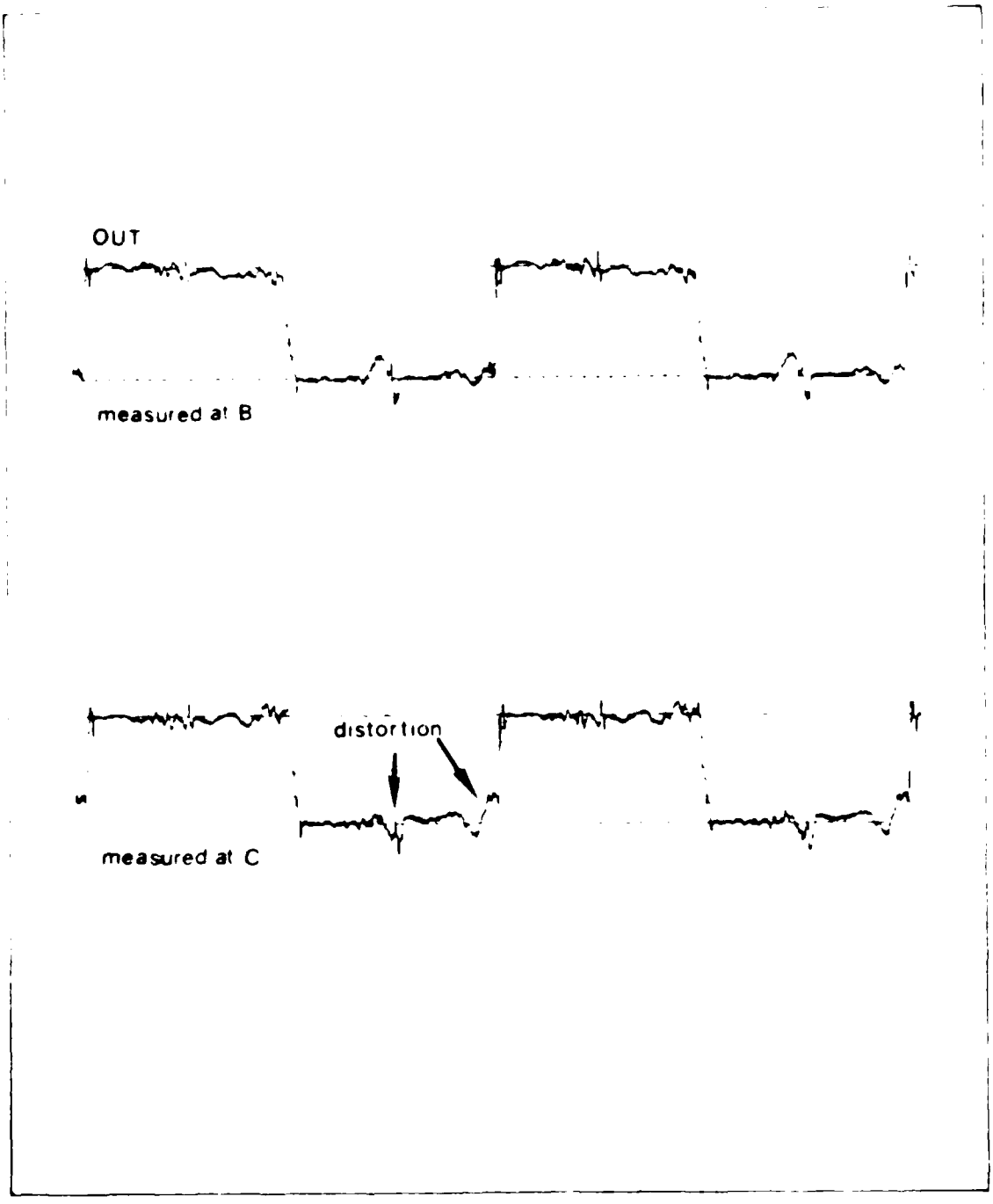

Figure 59. The Output Signal Measured Along the Wire-Bonded Interconnect at Points B and C at 1 MHz. These points are highlighted in Figures 32 and 39. Note the signal degradation evidenced by the rise time of the waveform at C. Vertical axis: 2 volts/division. Horizontal axis: 200.0 nsec/division.

V. Conclusions and Recommendations

A silicon-hybrid wafer-scale integration technique has been developed and tested. Two functional CMOS circuits were epoxied into a dual wafer structure providing planarization and structural support for the wafer-scale interconnects. A photosensitive polyimide precursor, Selectilux HTR 3-200, was used as a dielectric for these interconnects. This thick polyimide precursor was also able to further planarize the wafer surface. In addition, this dielectric allowed the interconnect vias to be directly patterned into the polyimide photosensitively. To interconnect the two die circuitries, aluminum lines were patterned on the polyimide surface using a positive photoresist mask and wet chemical etching.

Electrical tests were performed to evaluate the quality of these interconnects. The parametric tests showed that the signal delay, attenuation, and distortion is indistinguishable for a one centimeter path length of the interconnect. Compared to wire-bonded interconnects, the printed aluminum interconnects produce lower signal distortion.

Conclusions

Several fractures in the interconnects were discovered at the wafer-to-die transition and at the via step edges. Fractures in the transition region can be attributed to either or all of the following factors: (1) the uneven fill of epoxy in the transition region, (2) the inability of the polyimide to sufficiently planarize the transition steps, and (3) the insufficient planarization provided by the photoresist as an aluminum etch mask.

The Uneven Fill of Epoxy in the Transition Region. Very little can be done to prevent the uneven fill of epoxy in the wafer-to-die transition region. The incomplete fill is likely caused by air pockets trapped against the optical flat during the epoxy deposition, or voids created when the solvent evaporates from the epoxy during cure. However, when the epoxy flows between the wafer surface and the flat, the epoxy will fill the region above the wafer and die surfaces. In either case, the transition region will not be planar.

The Inability of the Polyimide to Sufficiently Planarize the Transition Steps. From Figure 41 it is clear that the 9 micron thick polyimide layer (after cure) was not always able to planarize the transition steps. This 9 micron thick layer (before cure) was 20 microns thick before the 250°C after cure. A thicker dielectric layer would enhance the planarization of this region; however, it has been shown that 50 micron square vias are difficult to pattern in thicker polyimide layers (see Table 8).

The Insufficient Planarization Provided by the Photoresist as an Aluminum Etch Mask. For the photoresist masks evaluated in chapter III, it was shown that the Shipley M1350J positive photoresist was the superior masking material for the aluminum metallization processing step (subsection: Development of Processing Schedule, Interconnect Fabrication, Aluminum Metallization). This positive photoresist exhibited excellent properties in three of the four evaluation criteria. However, the results showed that the 10 micron thick uncured polyimide was superior to the 1.6 micron thick positive resist in the remaining criteria: step height coverage (Table 9). However, the arbitrary removal of the polyimide mask during conductor patterning is not desirable.

Recommendations

The Uneven Fill of Epoxy in the Transition Region. To resolve the incomplete fill of epoxy, a low-viscosity gap filler could be utilized to planarize the wafer-to-die transition region (Figure 60). Before depositing epoxy into the gap, a low-viscosity material could be deposited in the gap as a thin layer with a microsyringe. Because this material will interface with the polyimide dielectric, Selectilux HTR 3-200 is recommended as the low-viscosity material. As the polyimide is allowed to cure, air pockets could easily pass through the low-viscosity material. After the polyimide is completely cured to 350°C, the epoxy can be deposited in the gap to bind the die to the planarizing substrate. The supporting substrate can be attached in the manner described in Appendix I.

To insure the epoxy does not flow onto the surface of the wafer, irregularities in both the wafer and die surfaces must be eliminated. It is recommended that 400 micron thick (100) silicon wafers be ordered with both sides polished. This will eliminate any surface irregularities caused by the planar silicon etching process (Appendix D). The uneven topography of the die surface is caused by the various layers of CVD oxide, polysilicon, and aluminum used to fabricate the VLSI circuit. A border can be fabricated around the perimeter of the die to equal the highest point of the die surface. This border will insure that the die will lay flat on the optical flat. A ring of aluminum surrounds most VLSI circuits designed by AFIT (Figure 22). It is recommended that a polysilicon layer be added beneath the metal of this ring. With this simple design change, MOSIS circuits could be fabricated with the necessary border for future WSI research.

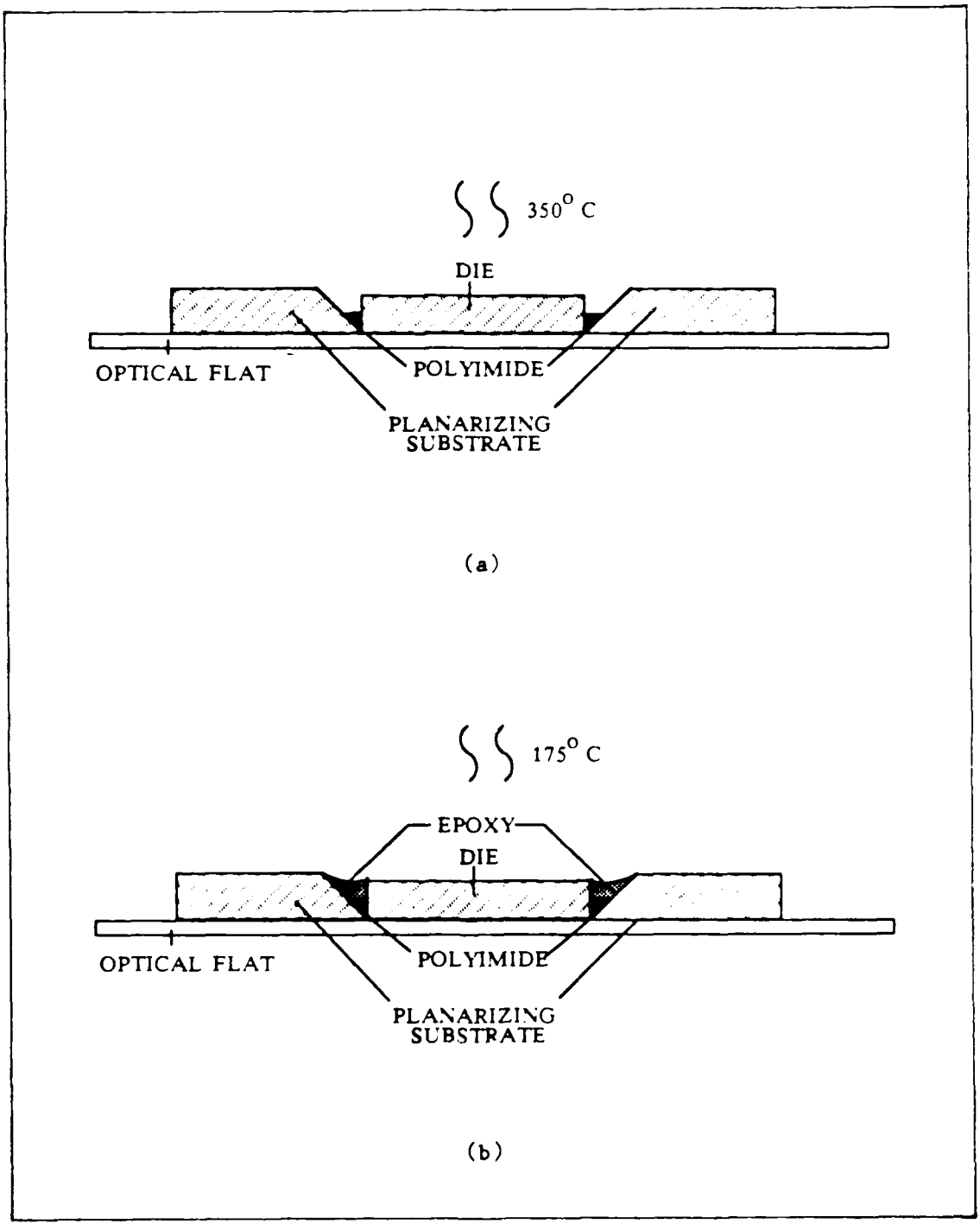

Figure 60. Planarizing the Wafer-to-Die Transition With the Deposition of Polyimide as a Low-Viscosity Gap Filler. (a) polyimide is deposited into the gap and cured at 350°C, (b) epoxy is deposited into the gap and cured at 175°C. The process of attaching the supporting substrate remains the same (Appendix I).

The Inability of the Polyimide to Sufficiently Planarize the Transition Steps. An alternate approach is recommended to planarize the wafer-to-die transition region. The Selectilux HTR 300-2 polyimide precursor displayed excellent planarization capabilities. This material can be applied up to an 80 micron thickness. Because the transition step heights did not normally exceed 30 microns, this polyimide should be more than adequate as a planarizing agent. However, there were other processing limitations that kept the polyimide thickness below 10 microns after cure. Because 25 micron width interconnects were proposed for this research, the vias were only about 50 microns square. Consequently, the dielectric could not be too thick before shadowing and poor step coverage of aluminum would be exhibited in the vias. It is recommend that the vias be expanded to 100 microns square. These dimensions are well within MOS'S design rules for the VLSI bonding pads.

Expanding the vias to 100 microns square will accommodate a 30 to 40 micron thick polyimide layer to be patterned with sloped sidewalls. However, the capability to expose the wafers with very high doses of ultraviolet light will be required. AFIT is currently purchasing a new mask aligner developed by Karl Suss America, Inc. The Suss MJB 3 Mask Aligner, series UV 300, can expose photoresist with 10 mW/cm^2 of light intensity at 310 nm (31:8). However, Selectilux HTR 300-2 is most photosensitive in the 350-450 nm ultraviolet light spectrum (18:18). Because the MJB 3 UV 300 and UV 400 systems both have the same lamphouse, the UV 300 can be converted to the UV 400 with a simple exchange of exposure optics. This can even be achieved without extinguishing the lamp (31:3). In addition, the new UV 300 can perform proximity printing with a gap separation ranging from 0 to 150 microns (31:8).

The unsuccessful via were caused by a shift in the surface of the dice in the hole. The results indicated that the unsuccessful via was the shallowest via on the wafer. This is evidence that the polyimide was thinnest over this region of the wafer. As explained earlier (chapter IV, section: Continuity Results, subsection: Open Circuits in the Wafer-to-Die Transition Region), spin-on materials tend to planarize surfaces by applying thicker layers over lower surfaces and thinner layers over higher surfaces. Therefore, the die was likely tilted up at the site of the unsuccessful via. As the highest level on the chip, this via might have been exposed in contact with the mask. The results indicated that there is a very sharp step for contact printed vias. Repositioning of the dice could be alleviated by curing the epoxy at a higher temperature on the hot plate, before subjecting the wafer to the 250°C curing cycle.

The Insufficient Planarization Provided by the Photoresist as an Aluminum Etch Mask. To resolve the step height coverage problem exhibited by the Shipley M1350J. Because the results indicated that the thicker polyimide was superior to the positive photoresist as a step coverage material, a thicker positive resist is recommended for future research. EM Industries also produces a positive resist that applies in layers up to 3.6 microns (19:2). Selectilux P2100-100 positive resist will likely provide better step coverage compared to the 1.6 micron thick Shipley M1350J. As a positive resist, the material should be easily removed with a simple solvent (for example, acetone).

Summary of Recommendations. It is recommended that this silicon-hybrid wafer-scale integration process be further refined with continued research. The die mounting process should be refined to include the deposition of Selectilux HTR 3-200 as a low-viscosity gap filler. In

addition, a more comprehensive appreciation of the capabilities of the Selectilux HTR 3-200 polyimide precursor is required. It is recommended that the new mask aligner be equipped with supplemental optics for the 350 to 450 nm ultraviolet spectrum. This conversion will allow the equipment to completely characterize the planarization and via slope profiles capable with Selectilux HTR 300-2, and still exploit the performance of the control positive photoresists. Finally, it is recommended that thicker positive photoresists be investigated to improve the step coverage of aluminum for fine linewidths. Essentially, many of the interconnect failures could be avoided with a proper combination of planarizing materials (Figure 61).

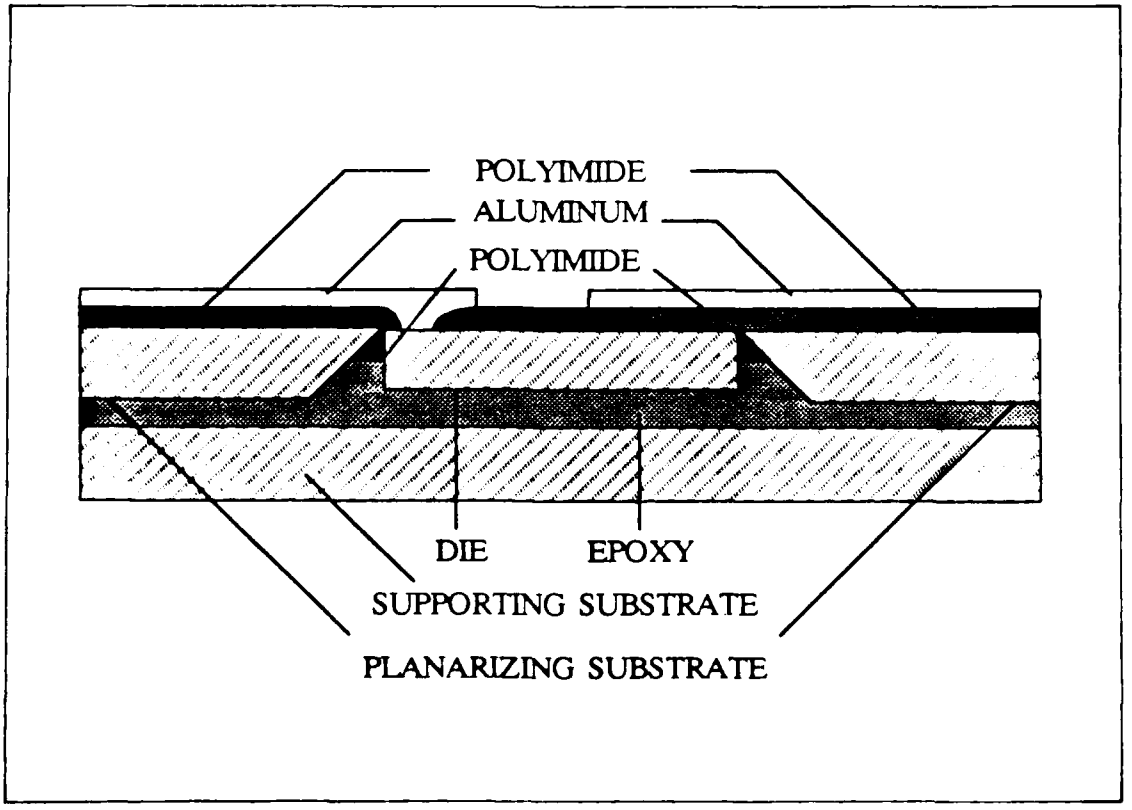

Figure 61. The Wafer Structure With the Recommended Refinements.

Appendix A: Geometric Mean Distance (GMD) Calculations

The GMD theory is a mathematical concept useful for calculating inductance. As defined by Stevenson:

> ... the GMD from one point to a group of points is the geometric mean of the distances from the one point to each of the other points (57:33).

For example, the GMD from one point to four other points (Figure A-1) is (57:33):

$$GMD = \sqrt[4]{D_1 D_2 D_3 D_4}. \qquad (A-1)$$

Self-GMD. To extend the GMD theory to solids, the conductor must be subdivided into several parallel infinitesimally thin strands (see discussion of the skin effect in chapter II). The self-GMD or geometric mean radius (GMR) of a solid conductor is the infinite sum of distances between all pairs of strands (67:106):

$$\log D_{sa} = \frac{1}{w^2 d^2} \int_0^d \int_0^d \int_0^w \int_0^w \log \sqrt{(x-\xi)^2 + (y-\eta)^2}\, dx\, d\xi\, dy\, d\eta \qquad (A-2)$$

where the variables are defined in Figure A-2. Once integrated, the GMD

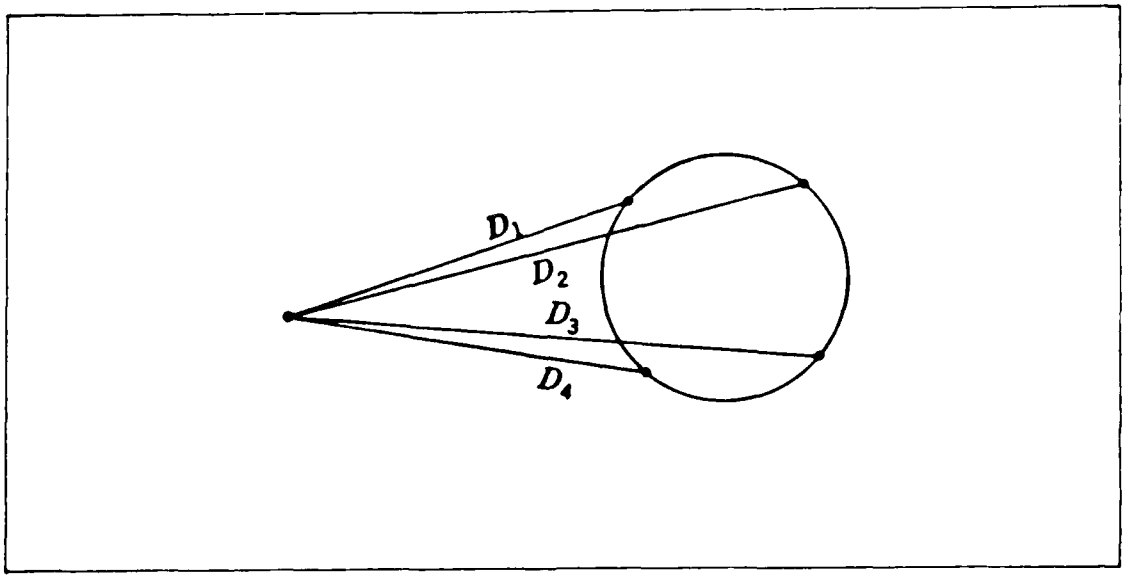

Figure A-1. The GMD of One Point With Respect to Four Other Points (57:33)

can be simply approximated by (57:35;55:1123;67:107):

$$D_{sa} = 0.2235(w + d). \tag{A-3}$$

GMD Between Two Interconnects. Extending this theory to two solid conductors, Equation A-2 becomes (67:107):

$$\log D_{ab} = \frac{1}{w^2 d^2} \int_0^d dY \int_0^d dy \int_0^{s+w} dX \int_0^w \log \sqrt{(X - x)^2 + (Y - y)^2}\, dx \tag{A-4}$$

where the variables are defined in Figure A-2.

The solution to this integral is quite extensive and is not approximated in the literature (13:142):

$$\begin{aligned} D_{ab} = \exp\Bigg[\frac{1}{w^2 d^2}\Bigg[&\frac{1}{4}\left[(s + w)^2\left(d^2 - \frac{(s + w)^2}{6}\right) - \frac{d^4}{6}\right] \ln\left((s + w)^2 + d^2\right) \\ &+ \frac{1}{4}\left[(s - w)^2\left(d^2 - \frac{(s - d)^2}{6}\right) - \frac{d^4}{6}\right] \ln\left((s - w)^2 + d^2\right) \\ &- \frac{1}{2}\left[s^2\left(d - \frac{s^2}{6}\right) - \frac{d^4}{6}\right] \ln(s^2 + d^2) + \frac{1}{12}(s + w)^4 \ln(s + w) \\ &+ \frac{1}{12}(s - w)^4 \ln(s - w) - \frac{1}{6} s^4 \ln(s) \\ &+ \frac{1}{3}\left[w(s + d)^3 - w^3(s + d)\right] \tan^{-1}\left(\frac{w}{s + d}\right) \\ &+ \frac{1}{3}\left[w(s - d)^3 - w^3(s - d)\right] \tan^{-1}\left(\frac{w}{s + d}\right) \\ &- \frac{2}{3}(w s^3 - w^3 s) \tan^{-1}\left(\frac{w}{d}\right) - \frac{25}{12} d^2 w^2\Bigg]\Bigg] \end{aligned} \tag{A-5}$$

where the variables are defined in Figure A-2.

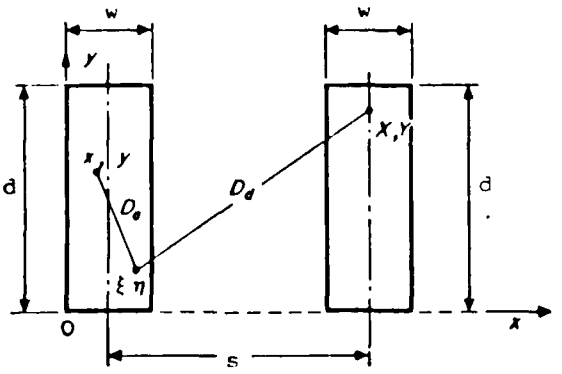

Figure A-2. Cross-Section Through Two Parallel, Rectangular Conductors (57:106)

Appendix B: Calculated Electrical Performance

The following data was compiled using the VIP Professional spreadsheet. Two types of worksheets are included in this appendix: (1) A general electrical performance worksheet, and (2) a detailed calculation of the frequency-dependent losses in the line. These calculations were performed for two conductor thicknesses (i.e. 0.6 and 0.9 microns); therefore, a total of four different worksheets were created. These calculations were intended to show the relationship between geometrical line parameters and the performance of the line. Table B-1 references the equations used to perform these calculations.

Table B-1. Equation References for Worksheets

Parameter	Equations
Delay	(6), (7), (2)
Loss	(10), (11), (12), (13), (14), (15)
Reflection Coefficient	(27), (14), (15)

PREDICTED ELECTRICAL PERFORMANCE (WAFER-SCALE INTERCONNECTS)

conductor:
width= 0.0025 cm
thick= 0.00006 cm
resist'y 0.000002 ohm-cm
length= 1 cm

dielectric:
sep'tion= 0.01 cm loss tan.= 0.002
height= SEE TABLE frequency= 70000000 Hz
rel perm= 3.5
permit.= 3.1E-13 F/cm load= 50 ohms

PLATE SEP. (cm)	0.00046	0.00086	0.00126	0.00166	0.00206	0.00246	0.00286	0.00326	0.00366	0.00406
HEIGHT (c)	0.0002	0.0004	0.0006	0.0008	0.001	0.0012	0.0014	0.0016	0.0018	0.002
DELAY (ps)	46.06565	25.17957	18.06189	14.43264	12.21689	10.71516	9.625599	8.796107	8.141587	7.610623
IMPEDANCE (ohms)	7.292474	13.65161	19.27542	24.29083	28.79421	32.86161	36.55429	39.92232	43.00709	45.84317
COND LOSS (dB/cm)	0.497954	0.270214	0.194307	0.155964	0.132552	0.116588	0.104885	0.095859	0.088632	0.082677
DIEL LOSS (dB/cm)	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238
TOT LOSS (dB/cm)	0.498192	0.270453	0.194546	0.156203	0.132791	0.116826	0.105124	0.096098	0.088871	0.082916
REF. COEF.	0.745429	0.571052	0.443513	0.346061	0.269128	0.206831	0.155344	0.112070	0.075186	0.043371

PREDICTED ELECTRICAL PERFORMANCE (WAFER SCALE INTERCONNECTS)

PLATE SEP. (cm)	0.00446	0.00486	0.00526	0.00566	0.00606	0.00646	0.00686	0.00726	0.00766	0.00806
HEIGHT (c)	0.0022	0.0024	0.0026	0.0028	0.003	0.0032	0.0034	0.0036	0.0038	0.004
DELAY (ps)	7.170279	6.798456	6.479759	6.203126	5.960397	5.745415	5.553447	5.380791	5.224508	5.082235
IMPEDANCE (ohms)	48.45968	50.88132	53.12919	55.22144	57.17378	58.99984	60.71153	62.31933	63.83243	65.25901
COND LOSS (dB/cm)	0.077660	0.073356	0.069609	0.066307	0.063369	0.060730	0.058343	0.056171	0.054182	0.052352
DIEL LOSS (dB/cm)	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238
TOT LOSS (dB/cm)	0.077898	0.073594	0.069847	0.066546	0.063607	0.060968	0.058582	0.056409	0.054420	0.052590
REF. COEF.	0.015644	-0.00873	0.03034	0.04962	0.06692	0.08256	0.09675	-0.10968	-0.12151	-0.13238

PREDICTED ELECTRICAL PERFORMANCE (WAFER-SCALE INTERCONNECT)

FREQUENCY (Hz)	10000	50000	100000	500000	1000000	5000000	10000000	50000000	7000000
PLATE SEP. (cm)	0.00024		IMPEDANCE (ohms) =	7.292474		WIDTH (cm) =			0.0003
HEIGHT (cm)	0.0001		rel. permit.=	3.5		THICKNESS (cm) =			0.00006
						loss tan.=			0.001
COND LOSS (dB/cm)	0.005951	0.013309	0.018820	0.042084	0.059516	0.133083	0.188209	0.420849	0.497954
DIEL LOSS (dB/cm)	0.000000	0.000000	0.000000	0.000001	0.000003	0.000017	0.000024	0.000170	0.000239
TOT LOSS (dB/cm)	0.005951	0.013308	0.018821	0.042086	0.059520	0.133100	0.188234	0.421019	0.498193

FREQUENCY (Hz)	10000	50000	100000	500000	1000000	5000000	10000000	50000000	70000000
PLATE SEP. (cm)	0.00056		IMPEDANCE (ohms) =	13.65161		WIDTH (cm) =			0.0007
HEIGHT (cm)	0.0004		rel. permit.=	3.5		THICKNESS (cm) =			0.00013
						loss tan.=			0.001
COND LOSS (dB/cm)	0.003329	0.007221	0.010213	0.022837	0.032296	0.072217	0.102131	0.228377	0.323214
DIEL LOSS (dB/cm)	0.000000	0.000000	0.000000	0.000001	0.000003	0.000017	0.000024	0.000170	0.000239
TOT LOSS (dB/cm)	0.003329	0.007221	0.010213	0.022838	0.032300	0.072235	0.102155	0.228547	0.323453

FREQUENCY (Hz)	10000	50000	100000	500000	1000000	5000000	10000000	50000000	70000000
PLATE SEP. (cm)	0.00112		IMPEDANCE (ohms) =	19.29542		WIDTH (cm) =			0.0015
HEIGHT (cm)	0.0008		rel. permit.=	3.5		THICKNESS (cm) =			0.0003
						loss tan.=			0.001
COND LOSS (dB/cm)	0.002352	0.005101	0.007214	0.016131	0.022814	0.051003	0.072141	0.161219	0.194217
DIEL LOSS (dB/cm)	0.000000	0.000000	0.000000	0.000001	0.000003	0.000017	0.000024	0.000170	0.000239
TOT LOSS (dB/cm)	0.002352	0.005101	0.007214	0.016133	0.022817	0.051020	0.072165	0.161389	0.194456

FREQUENCY (Hz)	10000	50000	100000	500000	1000000	5000000	10000000	50000000	70000000
PLATE SEP. (cm)	0.00168		IMPEDANCE (ohms) =	24.29081		WIDTH (cm) =			0.0022
HEIGHT (cm)	0.0012		rel. permit.=	3.5		THICKNESS (cm) =			0.0009
						loss tan.=			0.001
COND LOSS (dB/cm)	0.001954	0.004288	0.006094	0.013181	0.018641	0.041693	0.058945	0.131814	0.158954
DIEL LOSS (dB/cm)	0.000000	0.000000	0.000000	0.000001	0.000003	0.000017	0.000024	0.000170	0.000239
TOT LOSS (dB/cm)	0.001954	0.004289	0.006095	0.013183	0.018644	0.041709	0.058969	0.131984	0.159193

FREQUENCY (Hz)	10000	50000	100000	500000	1000000	5000000	10000000	50000000	70000000
PLATE SEP. (cm)	0.00224		IMPEDANCE (ohms) =	28.79421		WIDTH (cm) =			0.0031
HEIGHT (cm)	0.0016		rel. permit.=	3.5		THICKNESS (cm) =			0.0013
						loss tan.=			0.001
COND LOSS (dB/cm)	0.001704	0.003742	0.005318	0.011501	0.015843	0.035428	0.050107	0.112017	0.135154
DIEL LOSS (dB/cm)	0.000000	0.000000	0.000000	0.000001	0.000003	0.000017	0.000024	0.000170	0.000239
TOT LOSS (dB/cm)	0.001704	0.003741	0.005318	0.011504	0.015846	0.035444	0.050131	0.112187	0.135393

PREDICTED ELECTRICAL PERFORMANCE (WAFER SCALE INTERCONNECTS)

conductor:
width: 0.0025 cm
thick: 0.00009 cm
resist'y 0.000002 ohm cm
length: 1 cm

dielectric:
sep'tion 0.01 cm loss tan.: 0.002
height: SEE TABLE frequency: 70000000 Hz
rel perm: 3.5
permit.: 3.1E-13 F/cm load: 50 ohms

PLATE SEP. (cm)	0.00049	0.00089	0.00129	0.00169	0.00209	0.00249	0.00289	0.00329	0.00369	0.00409
HEIGHT (c)	0.0002	0.0004	0.0006	0.0008	0.001	0.0012	0.0014	0.0016	0.0018	0.002
DELAY (ps)	31.08796	17.11093	12.31792	9.901011	8.410688	7.399261	6.664508	6.104479	5.662089	5.302832
IMPEDANCE (ohms)	7.209380	13.44151	19.02850	23.97843	28.42673	32.44808	36.10240	39.43857	42.49697	45.31131
COND LOSS (dB/cm)	0.490790	0.264583	0.189300	0.151361	0.128258	0.112550	0.101067	0.092235	0.085181	0.079382
DIEL LOSS (dB/cm)	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238
TOT LOSS (dB/cm)	0.491028	0.264821	0.189539	0.151600	0.128497	0.112788	0.101305	0.092473	0.085419	0.079621
REF. COEF.	0.747965	0.575261	0.448676	0.351745	0.275075	0.212884	0.161407	0.118085	0.081116	0.049193

PREDICTED ELECTRICAL PERFORMANCE (WAFER-SCALE INTERCONNECTS)

PLATE SEP. (cm)	0.00449	0.00489	0.00529	0.00569	0.00609	0.00649	0.00689	0.00729	0.00769	0.00809
HEIGHT (c)	0.0022	0.0024	0.0026	0.0028	0.003	0.0032	0.0034	0.0036	0.0038	0.004
DELAY (ps)	5.004587	4.752508	4.536245	4.348358	4.183355	4.037091	3.906378	3.788723	3.682143	3.585044
IMPEDANCE (ohms)	47.90997	50.31705	52.55318	54.63606	56.58104	58.40147	60.10902	61.71392	63.22521	64.65090
COND LOSS (dB/cm)	0.074507	0.070333	0.066706	0.063515	0.060679	0.058136	0.055838	0.053748	0.051837	0.050080
DIEL LOSS (dB/cm)	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238	0.000238
TOT LOSS (dB/cm)	0.074745	0.070571	0.066944	0.063753	0.060917	0.058374	0.056076	0.053986	0.052075	0.050318
REF. COEF.	0.021346	-0.00316	-0.02489	-0.04430	-0.06174	-0.07750	-0.09180	-0.10485	-0.11680	-0.12778

PREDICTED ELECTRICAL PERFORMANCE (WAFER-SCALE INTERCONNECT)

FREQUENCY (Hz)	10000	50000	100000	500000	1000000	5000000	10000000	50000000	70000000
PLATE SEP. (cm)	0.00049		IMPEDANCE (ohms)=	7.209391			WIDTH (cm)=		0.0015
HEIGHT (c)	0.0002		rel. permit.=	3.5			THICKNESS (cm.)=		0.00003
							loss tan.=		0.002
COND LOSS (dB/cm)	0.005865	0.013116	0.018550	0.041479	0.058660	0.131169	0.185501	0.414791	0.490791
DIEL LOSS (dB/cm)	0.000001	0.000001	0.000000	0.000001	0.000003	0.000017	0.000034	0.000170	0.000238
TOT LOSS (dB/cm)	0.005866	0.013117	0.018550	0.041481	0.058664	0.131186	0.185535	0.414961	0.491029

FREQUENCY (Hz)	10000	50000	100000	500000	1000000	5000000	10000000	50000000	70000000
PLATE SEP. (cm)	0.00069		IMPEDANCE (ohms)=	13.49151			WIDTH (cm)=		0.0015
HEIGHT (c)	0.0004		rel. permit.=	3.5			THICKNESS (cm.)		0.00003
							loss tan.=		0.002
COND LOSS (dB/cm)	0.003162	0.007071	0.010000	0.022361	0.031627	0.070712	0.100000	0.223612	0.264551
DIEL LOSS (dB/cm)	0.000000	0.000000	0.000000	0.000001	0.000003	0.000017	0.000034	0.000170	0.000238
TOT LOSS (dB/cm)	0.003162	0.007071	0.010000	0.022362	0.031627	0.070729	0.100037	0.223782	0.264789

FREQUENCY (Hz)	10000	50000	100000	500000	1000000	5000000	10000000	50000000	70000000
PLATE SEP. (cm)	0.00129		IMPEDANCE (ohms)=	19.02858			WIDTH (cm)=		0.0015
HEIGHT (c)	0.0006		rel. permit.=	3.5			THICKNESS (cm.)		0.00003
							loss tan.=		0.002
COND LOSS (dB/cm)	0.002261	0.005059	0.007154	0.015998	0.022623	0.050582	0.071548	0.159988	0.189271
DIEL LOSS (dB/cm)	0.000000	0.000001	0.000001	0.000001	0.000003	0.000017	0.000034	0.000170	0.000238
TOT LOSS (dB/cm)	0.002262	0.005059	0.007155	0.016000	0.022626	0.050599	0.071582	0.160158	0.189509

FREQUENCY (Hz)	10000	50000	100000	500000	1000000	5000000	10000000	50000000	70000000
PLATE SEP. (cm)	0.00169		IMPEDANCE (ohms)=	23.97843			WIDTH (cm)=		0.0015
HEIGHT (c)	0.0009		rel. permit.=	3.5			THICKNESS (cm)=		0.00003
							loss tan.=		0.002
COND LOSS (dB/cm)	0.001809	0.004045	0.005720	0.012792	0.018091	0.040453	0.057209	0.127924	0.151361
DIEL LOSS (dB/cm)	0.000000	0.000001	0.000000	0.000001	0.000003	0.000017	0.000034	0.000170	0.000238
TOT LOSS (dB/cm)	0.001809	0.004045	0.005721	0.012794	0.018094	0.040470	0.057243	0.128094	0.151600

FREQUENCY (Hz)	10000	50000	100000	500000	1000000	5000000	10000000	50000000	70000000
PLATE SEP. (cm)	0.00209		IMPEDANCE (ohms)=	28.42673			WIDTH (cm)=		0.0015
HEIGHT (c)	0.001		rel. permit.=	3.5			THICKNESS (cm)=		0.00003
							loss tan.=		0.002
COND LOSS (dB/cm)	0.001532	0.003427	0.004847	0.010839	0.015329	0.034278	0.048477	0.108398	0.128258
DIEL LOSS (dB/cm)	0.000000	0.000000	0.000000	0.000001	0.000003	0.000017	0.000034	0.000170	0.000238
TOT LOSS (dB/cm)	0.001533	0.003428	0.004848	0.010841	0.015333	0.034295	0.048511	0.108568	0.128497

Appendix C: Standard Clean Procedures

EQUIPMENT:

-- Polypropylene wafer holder and beaker (Bldg 125)

-- Glass beaker (Bldg 125)

MATERIALS:

-- Sulfuric acid (H_2SO_4) (Bldg 125)

-- Hydrogen Peroxide (H_2O_2) (Bldg 125)

-- Hydrofluoric Acid (HF) (Bldg 125)

PROCEDURES:

Removing Organics

(1) Particulate matter was removed from the surface of each wafer with nitrogen, and the wafers were placed in a polypropylene holder.

(2) The following solution was mixed in a glass beaker: 300 ml H_2SO_4 and 200 ml H_2O_2.

(3) The wafers were immediately submerged in this solution for 15 minutes.

(4) The wafers were then rinsed in deionized water (DIW) for 5 minutes (or until a 10Mohm standard was attained).

Deglazing

(5) The following solution was mixed in a polypropylene beaker and set aside for 3 hours to stabilize: 500 ml deionized water and 50 ml HF.

(6) The wafers were immersed in the mixture for 30 seconds.

(7) The wafers were immediately rinsed in DIW for 5 minutes.

Appendix D: Planar Silicon Etching Procedures

EQUIPMENT:

-- Polypropylene wafer holder (Bldg 125)

-- Teflon beaker (Bldg 125)

-- Micrometer (Bldg 125)

MATERIALS:

-- Nitric acid (HNO_3) (Bldg 125)

-- Glacial acetic acid (CH_3COOH) (Bldg 125)

-- Hydrofluoric Acid (HF) (Bldg 125)

PROCEDURES:

(1) The following planar etching solution was mixed in a teflon beaker and allowed to stabilize for three hours: 40 ml HF, 300 ml HNO_3, and 100 ml CH_3COOH.

(2) Several quartered silicon wafers of equal thickness ($\pm$ 10 microns) were sorted and arranged in a polypropylene wafer holder.

(3) The wafers were cleaned using the organic cleaning process detailed in Appendix C.

(4) After the organics were removed, and the wafers were thoroughly rinsed in deionized water, the wafers were immediately immersed in the planar etching solution.

(5) After the first five minutes in the etchant, the wafers were removed and rinsed in dionized water for 60 seconds.

(6) One wafer from the batch was selected as a control to monitor the etch rate. This wafer was dried with a nitrogen gas purge, and its thickness was measured using the micrometer.

(7) The control wafer was then positioned in the holder, and the entire batch was immersed in the etchant for another time increment of ten minutes.

(8) Steps (5) through (7) were performed for each ten minute increment until a wafer thickness of 400 microns ($\pm$ 5 microns) was attained.

(9) The wafers were thoroughly rinsed in deionized water for five minutes after the final etch period.

Appendix E: Oxidation Procedures

EQUIPMENT:

-- Thermal Oxidation Furnace with Quartzware (Bldg 125)

MATERIAL:

-- (100) 3-inch, p-doped at 1-3 ohms (quartered at the Avionics Lab)

PROCEDURES:

(1) The wafers were arranged in a quartz boat.

(2) The furnace was stabilized at 1050°C.

(3) Pure oxygen was allowed to flow through the furnace.

(4) The quartz boat was pushed into the furnace one inch/minute for the first twelve inches. The rest of the boat was then pushed the remaining distance to the center of the furnace. The oxygen atmosphere was maintained for 15 minutes.

(5) The steam flow was activated for:

(a) 20 hours (for the oxide mask only). The water bubbler was refilled every 8 to 10 hours.

(b) 3 1/2 hours (for the dielectric layer only).

(6) The steam flow was terminated, and pure oxygen was allowed to flow through the furnace for another 15 minutes. The boat was pulled out to twelve inches from the edge of the furnace. Then the boat was pulled out one inch/minute for the next twelve inches.

(7) The boat was removed from the furnace, the oxygen flow was discontinued, and the wafers were allowed to cool.

Appendix F: Photolithography Procedures

EQUIPMENT:

Rubylith Design:

-- Sun Workstation (Bldg 640)

-- Versatec Plotter (Bldg 640)

For Automated Rubylith Design Only:

-- Magnetic Tape (Bldg 640, Trailer 2A)

-- Magnetic Tape Drive (Bldg 640)

-- General Electric CALMA System (AFWAL/AADR)

-- Xynetics 1100 Automated Drafting System (AFWAL/AADR)

For Manual Rubylith Design Only:

-- Line Printer (Bldg 640)

-- Coordinatograph Machine (Bldg 125)

Plate Processing:

-- Reduction Camera (Bldg 125)

- 3 inch Wray lens
- 20x setting:

Rear Box Position 27.0000

Front Box Position 6.8826

- 4 x 4 inch plate holder

-- Mask Developing System (Bldg 125)

- Stainless steel tanks
- Ultrasonic cooling system
- Polypropylene mask holder

-- Mask Duplicating Camera (Bldg 125)

- 4 x 4 inch plate holders

- Initial Settings:

Plate Separation 2

Vacuum Pumpdown 1.5

N_2 Purge 1

Emulsion Intensity 5

Photoresist Intensity 7

Lamp Servo Normal

Master Hold On

Emulsion On

Manual Exposure Off

Newton Rings Off

Latch Release Off

Master Vacuum On

Main Power On

Photoresist Processing:

-- Convection Ovens (70 to 220 C) (Bldg 125)

-- Cobilt Contact Printer with Mask Alligner (Bldg 125)

-- Optical Microscope (Bldg 125)

For Positive Resist:

-- Photoresist Spinner (Bldg 125)

-- Spray Bottles (Bldg 125)

For Negative Resist:

-- Automatic Spray Development System (Bldg 125)

MATERIALS:

-- Rubylith (40 inch wide roll)

-- Standard Photoplate Developer Chemicals

- Kodak D-8 or high resolution plate (HRP) Developer

- Kodak Stop Bath

- Kodak Fix Bath

-- Methyl Alcohol

-- Photoplates (4 x 4 inch Kodak HRP)

For Positive Resist:

-- Photoresist (PR) adhesion promoter: hexamethyldiasemine (HMDS) (Bldg 125)

-- Positive Resist (Shipley M1350J) (Bldg 125)

-- Resist Developing Chemical

- Shipley Microposit D312:DIW (1:1) (Bldg 125)

For Negative Resist:

-- Negative Resist (Waycoat 28 cps) (Bldg 125)

-- Resist Developing Chemicals

- Xylene (Bldg 125)

- Butyl Acetate (Bldg 125)

PROCEDURE:

Rubylith Design:

(1) The mask was designed on the Sun workstation using the Magic CAD tool.

Automated Rubylith Design Only:

(2) Magic files were converted into Calma stream files using the Magic software package.

(3) The magnetic tape was installed on the tape drive.

(4) The tape drive used was controlled by the Apollo Sun workstation. Therefore, all CALMA stream files were sent to the Apollo Sun workstation, and commands to the drive were made by remotely logging into the Apollo system.

(5) The following command was entered to transfer the stream file from the Apollo system to the tape:

dd if=<filename.strm> conv=ucase of=/dev/rmt0.

(6) The tape was removed from the drive, and hand-carried to AFWAL/AADR.

(7) The tape was loaded into the CALMA system tape drive, and read into the CALMA system.

(8) To use the Xynetics drafting system as a Rubylith cutter, the CALMA file had to be reconfigured.

(9) The reconfigured stream file was loaded onto a tape and transfered to the Xynetics tape drive.

(10) The drafting machine was refitted with cutting blades, and the Rubylith was positioned and secured onto the table.

(11) The coordinates were down-loaded from the tape drive to the drafting machine, and the Rubylith was cut automatically.

(12) The cut Rubylith was carried back to Bldg 125.

Manual Rubylith Design Only:

(13) The coordinates of the Magic file were listed on the lineprinter.

(14) The coordinates (lambda = 1.5 microns) were converted to mils (i.e. 25.4 microns = 1.0 mils) and multiplied by 20.

(15) The Rubylith was secured to the table of the coordinatograph machine.

(16) The origin was selected with respect to the minimum and maximum values of the x and y coordinates.

(17) The Rubylith was cut using the converted coordinates from step (14).

Plate Processing:

(18) Using the mask reduction camera, the rubylith pattern was transfered to a HRP using a 40 second exposure. This exposure time was determined experimentally to provide the best resolution.

(19) Three solutions were prepared in separate tanks: D-8 or HRP developer, stop bath, and a fix solution.

(20) The exposed plate was placed on a polypropylene holder and immersed in the developer. The plate remained immersed under ultrasonic agitation for 3 minutes for the D-8 developer, or 5 minutes for the HRP developer.

(21) The plate was immediately immersed in the stop bath for 30 seconds.

(22) The plate was immediately immersed in the fix solution for 60 seconds.

(23) The plate was immediately rinsed in deionized water for 5 minutes.

(24) The plate was dipped in methyl alcohol, and dried with a nitrogen gas purge.

For Copies Only (Required for Positive Resist Masks):

(25) The mask plate was installed in the duplicating camera with the emulsion side facing out.

(26) Under red light conditions, an unexposed plate was installed in the duplicating camera with the emulsion side facing up.

(27) The exposure was set to 12.0 seconds.

(28) The plates were brought together, and the plates were automatically exposed.

(29) The exposed plate was developed following steps 20 through 24.

Wafer Patterning:

(30) The wafers were dehydrated at 150°C for at least 30 minutes.

For Positive Resist Only:

(31) Particulate matter was flushed from the top surface of the wafer with a nitrogen gas purge.

(32) HMDS was deposited on the wafer's top surface by:

(a) dispensing the material on the surface, and allowing it to flow over the edge of the wafer (allowed 5 seconds),

(b) spinning the wafer at 2000 rpm for 5 seconds (spread cycle),

(c) spinning the wafer at 4000 rpm for 30 seconds (remove the excess).

(33) Positive photoresist was deposited on the wafer's top surface by:

(a) dispensing the material on the wafer and allowing

it to flow over the edges of the wafer (allowed 5 seconds),

(b) spinning the wafer at 4000 rpm for 30 seconds.

(34) The photoresist was softbaked at 95°C for 25 minutes.

(35) The wafer was removed from the oven.

(36) Particulate matter was removed from the wafer's surface and the mask plate surface (nitrogen gas purge).

(37) The wafer was alligned with the mask, and the photoresist was exposed to 160 mJ/cm^2 of ultraviolet energy (e.g. 64 seconds at 2.5 mW/cm^2).

(38) The pattern was developed by:

(a) spinning the wafer at 1000 rpm while spraying the surface with developer for 20 seconds,

(b) spinning the wafer at 1000 rpm while rinsing the surface with dionized water for another 20 seconds,

(c) spinning the wafer at 4000 rpm while drying the surface dry with a nitrogen gas purge for 15 seconds.

(39) The developed photoresist pattern was hardbaked at 120°C for 30 minutes to harden the remaining resist.

For the Hole Pattern Only:

(40) Steps 31-34, and 39 were repeated for the backside of the wafer.

Negative Resist:

(41) Particulate matter was removed from the top surface of the wafer with a nitrogen gas purge.

(42) Negative photoresist was coated on the wafer's top surface side by:

(a) dispensing the material on the wafer's surface and allowing it to flow over the edges of the wafer (allowed 5 seconds),

(b) spinning the wafer at 5000 rpm for 30 seconds.

(43) The photoresist was softbaked at 105°C for 25 minutes.

(44) The wafer was removed from the oven.

(45) Particulate matter was removed from the wafer's surface and the mask plate surface.

(46) The wafer was alligned with the mask, and the photoresist was exposed to 20 mJ/cm^2 of ultraviolet energy (e.g., 5 seconds at 4.0 mW/cm^2).

(47) The pattern was developed in the automatic spray developer as follows:

(a) purge with nitrogen for 20 sec.

(b) spin-spray with Xylene for 30 sec.

(c) spin-rinse with Butyl Acetate for 30 sec.

(d) purge with nitrogen for 40 sec.

(48) The developed photoresist pattern was hardbaked at 175 C for 30 minutes to harden the remaining photoresist.

For the Hole Pattern Only:

(49) Steps 41- 43, and 48 were repeated for the backside of the wafer.

Appendix G: Oxide Etch Procedures

EQUIPMENT:

-- Polypropylene wafer basket and beaker (Bldg 125)

MATERIALS:

-- Ammonium Fluoride (NH_4F) (Bldg 125)

-- Hydrofluoric Acid (HF) (Bldg 125)

PROCEDURE:

(1) A mixture of 600 ml NH_4F and 100 ml HF was prepared in a polypropylene beaker. The solution was allowed to stabilize for at least three hours.

(2) Particulate matter was removed from each wafer with a nitrogen gas purge, and the wafers were arranged in the wafer holder.

(3) The wafers were immersed into the etchant solution for 5 minute increments.

(4) After a 60 second rinse in deionized water, the oxide thickness was estimated by the color chart method.

(5) Steps 3 and 4 were repeated as required until no oxide remained in the hole pattern (i.e. the wafer surface was hydrophobic).

(6) The wafers were rinsed thoroughly in deionized water for 5 minutes.

Appendix H: Silicon Etch Procedures

EQUIPMENT:

-- Quartz etching tank with a reflux condenser lid (Bldg 125)

-- Pyrex thermometer with 1°C graduations ranging from 0 to 110°C (Bldg 125)

-- Polypropylene wafer holder (Bldg 125)

-- Hotplate (Bldg 125)

MATERIALS:

-- Potassium Hydroxide (KOH) (Bldg 125)

-- Isopropyl Alcohol (Bldg 125)

PROCEDURE:

(1) The following chemicals were measured on the scale:

(a) 417 grams of solid KOH,

(b) 250 grams of isopropyl alcohol.

(2) These chemicals and 1000 ml of deionized water were combined in the quartz tank.

(3) The reflux lid was placed over the tank, and cool tap water was trickled through the condenser.

(4) The mixture was heated slowly to 70°C.

(5) The wafers were cleaned and deglazed as specified in Appendix C.

(6) The wafers were immediately immersed in the KOH etching solution.

(7) After 7 hours in the etchant, the wafers were monitored until the holes had etched through the wafer.

(8) The wafers were removed from the etchant and immediately rinsed in deionized water for 5 minutes.

(9) The remaining oxide was removed from the wafer surface using the oxide etching procedures detailed in Appendix F.

Appendix I: Die Attach Procedures

EQUIPMENT:

-- Programmable Convection Oven (Bldg 125)

-- 2 x 2 Inch HRP Plates (Optical Flats) (Bldg 125)

-- Vacuum Pump and Chuck (Bldg 125)

-- Hot Plate (Bldg 125)

-- Petri Dish Lined with Aluminum Foil (Bldg 125)

-- Toothpicks

-- Weight Scale (Bldg 125)

-- Soft Paper Wipes

-- 75 Gram Weights (Bldg 125)

-- Plastic Cup with Stirring Implement (Bldg 125)

MATERIALS:

-- Epoxy adhesive (Masterbond EP34CA, Component A and Component B)

-- Acetone

PROCEDURE:

(1) To strip the emulsion, several discarded HRP plates were cleaned according to the organic clean procedures detailed in Appendix C.

Preparing the Adhesive:

(2) The petri dish was heated to 175^{o}C on the hotplate.

(3) The adhesive was measured using the scale: 3.5 grams of component B and 7.0 grams of component A. The adhesive components were mixed thoroughly in the plastic cup.

(4) The petri dish was removed from the hot plate.

(5) The adhesive was transferred from the plastic cup to the petri dish. The epoxy's viscosity was increased by the heat from the petri dish.

Attaching the Chips to the Planarizing Substrate:

(6) A clean optical flat was place on the hot plate, and an etched wafer (planarizing substrate) was placed, surface down, onto the flat.

(7) Two chips were placed face down into the etched wafer's holes.

(8) The wafer was pressed onto the flat with three weights; one placed on each corner of the wafer. The chip to wafer transition was freely accessible with a toothpick.

(9) One at a time, each chip was pressed down onto the flat with a toothpick. Another toothpick was used to administer a continuous bead of epoxy into the wafer to chip transition.

(10) Careful not to dislodge the chip, the toothpick was slowly lifted from the chip.

(11) After 5 minutes, the weights were removed, the wafer was slided over the plate, and any epoxy on the plate was cleaned with a small acetone-soaked wipe.

(12) Step 10 was performed again after 10 minutes had elapsed.

(13) After 15 minutes had elapsed, the wafer was removed from the plate. The wafer was placed on the vacuum chuck, top-side down. The excess epoxy was scrubbed off with a wipe soaked with acetone.

(14) The wafer was flipped over on the vacuum chuck, and excess epoxy was cleaned off of the top surface with an acetone-soaked wipe.

(15) The optical flat was cleaned with a wipe soaked with acetone.

(16) The wafer was returned to the plate, and the weights were placed back onto the wafer.

(17) Step 10 was performed every 5 minutes until no epoxy was found on the optical flat.

(18) When no epoxy was found on the plate, the wafer was left on the hot plate for 10 minutes before inspection. If the inspection was satisfactory, the period of heating was extended another 5 minutes before inspection (i.e. 15 minutes, then 20 minutes, etc.). The low temperature cure was completed when 65 minutes of heating had elapsed.

Attaching the Supporting Substrate:

(19) The wafer was place on the optical flat once again. Extra epoxy was deposited in the holes to fill the gap above the chips. Small dots of epoxy were applied over the rest of the wafer's surface.

(20) A quartered wafer was placed, shiny side down, onto the epoxy.

(21) A 75 gram weight was placed on the wafer sandwich.

(22) If any epoxy flowed over the edges, the wafer was removed off of the optical flat. The optical flat was cleaned with an acetone-soaked wipe. The edges of the wafer were cleaned as well.

(23) The wafer was placed back onto the optical flat. Two 75 gram weights were placed onto the wafer.

(24) Step 22 was performed again.

(25) The wafer was placed back onto the optical flat. Three 75 gram weights were placed onto the wafer.

(26) Step 22 was performed again.

(27) The wafer was placed back onto the optical flat. The wafer was inspected every 15 minutes to insure that epoxy had not flowed out over the edges.

(28) The low temperature cure was completed when 65 minutes of heating had elapsed.

High Temperature Cure:

(29) The convection oven was programmed as follows:

(a) Hold Temperature: 70°C,

(b) S1 Temperature: 150°C,

S1 Time: 1.5 hours,

(c) S2 Temperature: 200°C,

S2 Time: 1.5 hours,

(d) S3 Temperature: 250°C,

and S3 Time: 4.0 hours.

(29) The wafer was placed top-side down on a clean optical flat.

(30) Three 75 gram weights were placed on top of the wafer.

(31) The wafer was placed in the oven, and the oven cycle was started.

(32) After the cycle was completed, and after the temperature had dropped to the hold temperature, the oven door was opened, and the wafer was removed.

Appendix J: Procedures for Applying Polyimide

EQUIPMENT:

-- Photoresist Spinner (Bldg 125)

-- Convection Oven (Bldg 125)

-- Hot Plate (Bldg 125)

MATERIALS:

-- Selectilux HTR 3-200 photosensitive polyimide precursor (Bldg 125)

-- Selectiplast HTR AP-1 adhesion promoter (Bldg 125)

-- Selectiplast D-2 Developer (Bldg 125)

-- Isopropyl Alcohol (Bldg 125)

-- Mask Alligner (Bldg 125)

PROCEDURE:

Applying the Polyimide on the Wafer

(2) The wafer was baked at 150°C for 30 minutes to dehydrate the surface.

(3) The adhesion promoter was mixed in a graduated cylinder as follows (two-day shelf life):

(a) 1-5 ml HTR AP-1

95 ml isopropyl alcohol

5 ml DIW

The solution was dispensed into an eye dropper.

(4) The wafer was removed from the oven and allowed to cool.

(5) The wafer was placed on the spinner and the wafers were purged with nitrogen to remove particulate matter.

(6) The wafer was flooded with the adhesion promoter for 10-15 seconds. The wafer was immediately spun dry at 4000 rpm for 30 seconds.

(7) The adhesion promoter was allowed to dry for 1 minute on the hot plate at 150°C.

(8) The wafer was placed on the spinner and the wafers were purged with nitrogen to remove particulate matter.

(9) The polyimide precursor was applied on the wafer with an eyedropper to cover approximately one-third of the wafer The polyimide was spread on the wafer using a 20 second, 2000 rpm spin cycle (for 10 micron thick polyimide after cure).

(10) The wafer was softbaked at 65°C for 2 hours.

(12) The wafer was removed from the oven and allowed to cool.

Exposing and Developing the Polyimide

(13) The wafers were purged with nitrogen gas to remove particulate matter.

(14) The exposure level of the mask aligner was set to 400 mJ/cm^2. The mask was manually aligned on the wafer. The wafer was exposed to the ultraviolet light source.

(14) The wafer was placed on the spinner. The wafer was spun at 500 rpm. The wafer was sprayed with the developer for 30 seconds. After 25 seconds of spraying on the developer, isopropyl alcohol was sprayed on the wafer as a rinse. The rinse was maintained for 15 seconds.

Curing the Polyimide

(15) The oven was programmed as follows:

Hold	70°C	
S1	150°C	for 1.5 hours
S2	200°C	for 1.5 hours
S3	250°C	for 4 hours

The wafer was placed in the oven and subjected to the programmed temperature profile. After about 7 hours, the wafer was removed from the oven.

Appendix K: Procedures for Metallization

EQUIPMENT:

-- Aluminum Evaporation Chamber (Bldg 125)

-- Custom wafer holders for quartered 3-inch wafers (Bldg 125)

-- 200 ml glass beaker (Bldg 125)

-- polyethylene wafer holder (Bldg 125)

-- pyrex thermometer (Bldg 125)

-- hot plate (Bldg 125)

MATERIALS:

-- Aluminum Wire (Bldg 125)

-- Source boats (Bldg 125)

-- Glacial Acetic Acid (CH_3COOH) (Bldg 125)

-- Phosphoric Acid (H_3PO_4) (Bldg 125)

-- Nitric Acid (HNO_3) (Bldg 125)

PROCEDURE:

Aluminum Deposition

(1) The wafer was purged with nitrogen gas to remove particulate matter.

(2) The wafers and the aluminum sources were mounted in the chamber, the chamber was evacuated, and aluminum was evaporated onto the polyimide's surface.

(3) The aluminum film thickness was monitored with the DTM meter. When a 12000 angstrom film thickness was deposited, the chamber was vented, and the wafers were removed.

Aluminum Etch

(4) In the glass beaker, 20 ml nitric acid, 80 ml acetic acid, 80 ml phosphoric acid, and 20 ml deionized water were mixed as the etchant.

(5) The etchant solution was heated to 45°- 50°C on a hot plate.

(6) After the wafer was patterned (See Chapter III), the wafer was immersed in the etchant.

(7) The aluminum's etch rate is approximately 2000 angstroms/ minute. Therefore, the wafer was constantly monitored until the aluminum was removed.

(8) The masking material was stripped from the wafer (e.g., acetone was used to remove the positive resist).

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The purpose of this research was to develop, fabricate, and electrically characterize a wafer-scale process developed for use with the 272-point Prime Factor Algorithm (PFA) processor. This process integrates discrete integrated circuit die in a planarized wafer package. The entire wafer surface was coated with photosensitive polyimide, which was patterned with vias for the interconnect contacts. The two die were electrically interconnected with printed aluminum interconnects using conventional silicon processing equipment.

A single interconnect, 26 microns wide and 1.2 microns thick, was parametrically evaluated up to 10 MHz. This interconnect exhibited no distinguishable propagation delay and attenuation for a one centimeter path length. In addition, the level of distortion introduced by the printed interconnect was no greater than the level of distortion introduced by a conventional wire-bonded interconnect.

The processing environment introduced a number of fractures in the interconnect network. These fractures were isolated at severe topographical steps encountered on the wafer's surface. The severity of these discontinuous steps were attributed to the uneven fill of the mounting epoxy in the wafer-to-die transition. It was also determined that the spin-on materials used to fabricate the interconnects did not provide adequate planarization and coverage over this transition. Further research is recommended to characterize the photosensitive polyimide used for this research. In additior alternate photoresist materials are also recommended.

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