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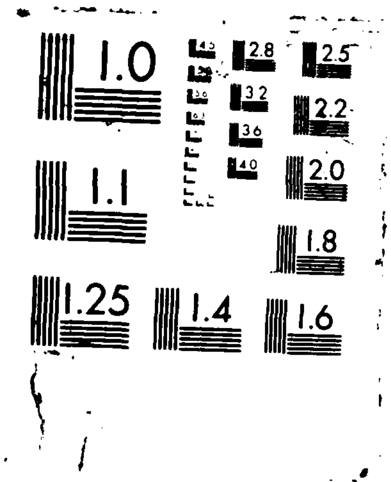
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19. ABSTRACT *(Continue on reverse if necessary and identify by block number)*

A new pruned-trellis search algorithm for high-rate convolutional code is developed. The search time and memory size is significantly reduced from standard search techniques. Some new high-rate systematic optimum convolutional codes of rate up to 7/8 have been found by this new search technique, and with constraint length up to 15.

These newly found high-rate convolutional codes can be efficiently decoded using pruned, error-trellis, syndrome decoding. The real advantage of the pruned error-trellis decoding over the conventional Viterbi decoding algorithm is the reduction of the memory size required. Simulation shows that the error trellis performance of pruned error-trellis decoding suffers only a 0.2 dB loss for some systematic high-rate convolutional codes compared with conventional, full trellis decoding.

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THE ALGEBRAIC STRUCTURE OF CONVOLUTIONAL CODES

AFOSR CONTRACT AFOSR-85-0259

Final Technical Report

July 15, 1985 - July 14, 1987

Irving S. Reed

Final Technical Report

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3. Period Covered: July 15, 1985 - July 14, 1987

4. Report Prepared By: Prof. Irving S. Reed, Principal Investigator

5. Date Prepared: September 25, 1987

6. A One Year Technical Research Summary:

-"Searching High-Rate Systematic Optimum Distance Convolutional Codes."

A new pruned-trellis search algorithm for high-rate convolutional code is developed. The search time and memory size is significantly reduced by this new search technique.

Some high-rate systematic optimum convolutional codes are being searched with rates up to 7/8 and of constraint length up to 15. These codes can be efficiently decoded using pruned error-trellis syndrome decoding.

-"Pruned Error-Trellis Syndrome Decoding for Convolutional Codes."

A new pruned error-trellis syndrome decoding scheme for CCs is developed. It is demonstrated that the real advantage of the pruned error-trellis decoding over both Viterbi and sequential decoding of CCs is the reduction of the number of states and transitions between any two frames.

-"CSI Architecture for Algebraic Syndrome Decoding of Dual-K Convolutional Codes."

An algebraic syndrome decoder is developed to find the best estimated message sequence for dual-K CCs without finding minimum-error paths in an error-trellis diagram. The advantage of this algebraic syndrome decoder over an error-trellis decoder of the dual-K CCs is that the message sequence can be corrected without a necessity for storing a large number of states or paths in a constraint length of the error trellis diagram. Finally, a LSI chip is developed to realize this algorithm.

-"VLSI Design of a Pipeline Algebraic Syndrome Decoder."

A new VLSI architecture is developed for the Algebraic Syndrome decoder. The advantage of this new architecture is that a substantial reduction in the number of transistors is accomplished.

-"Decoder Performance Simulation."

Decoder performance simulation is accomplished both for error-trellis decoding of convolutional codes and for algebraic syndrome decoding of dual-K convolutional codes.

7. Abstracts for Published Papers and Dissertations:

a. Published Papers

-I. S. Reed and T. K. Truong, "Sequential Syndrome Decoding Techniques for Convolutional Codes," submitted to IEE Proceedings, pt. E.

Abstract - This paper reviews previous studies (Refs. 1 and 2) of the algebraic structure of convolutional codes and extends those studies to apply to sequential syndrome decoding. These concepts are then used to realize by example actual sequential decoding, using the stack algorithm.

-J. F. Wang, I. S. Reed, T. K. Truong, J. Sun and J. Y. Lee, "LSI Architecture for Algebraic Syndrome Decoding of Dual-K Convolutional Codes," submitted to IEE Proceedings, pt. E.

Abstract - In this paper, algebraic syndrome decoders are developed which extend the early syndrome decoders of certain convolutional codes such as the Wyner-Ash code. Specifically syndrome decoders are designed to decode both the rate 1/2 and 1/3, dual-k, nonsystematic convolutional codes (CCs). Also the LSI architectures of these decoders are presented. Further, it is demonstrated that such decoders can be realized readily on a single chip with CMOS technology.

The advantage of this algebraic syndrome decoder over error-trellis decoding of dual-k CCs is that the message sequence can be corrected without the necessity for storing a number of states or paths in a constraint length of the error trellis diagram.

-J. M. Jensen and I. S. Reed, "Bounded Distance Coset Decoding of Convolutional Codes," IEE Proceedings, vol. 133, pt. F, no. 5, August 1986.

Abstract - This paper presents a maximum likelihood consistent bounded distance decoding algorithm for convolutional codes. The algorithm correctly decodes all error sequences which fall within the error correcting sphere. A class of codes is defined, in which the decoder exploits the fact that only certain error sequences need to be corrected. For these codes the decoding is based on a reduced encoder state diagram. Thus only a subset of the trellis or tree has to be searched in order to find the error pattern. An exact characterization of the reduced state diagram is given in this paper along with an example.

-H. M. Shao, T. K. Truong, I. S. Hsu, L. J. Deutsch and I. S. Reed, "A Single Chip VLSI Reed-Solomon Decoder," Proc. Int'l. Conf. on Acoustics, Speech and Signal Processing, Tokyo, Japan, April 7-11, 1986.

Abstract - A new VLSI design of a pipeline Reed-Solomon decoder is presented. The transform decoding technique used in a previous design is replaced by a simple time domain algorithm. A new architecture which realizes such algorithm permits efficient pipeline processing with a minimum of circuits. A systolic array is also developed to perform erasure corrections in the new design. A modified form of Euclid's algorithm is developed with a new architecture which maintains a real-time throughput rate with less transistors. Such improvements result in both an enhanced capability and significant reduction in silicon area, thereby making it possible to build a pipeline (255,223) RS decoder on a single VLSI chip.

-J. F. Wang, I. S. Reed, T. K. Truong and J. Sun, "Algebraic Syndrome Decoding of Dual-K Convolutional Codes," to be submitted for publication soon.

Abstract - In this paper, algebraic syndrome decoders are developed which extend the early syndrome decoders of high rate convolutional codes such as the Wyner-Ash code. In this paper, syndrome decoders are designed to decode the rate 1/n dual-k nonsystematic convolutional codes. The advantage of the algebraic syndrome decoders over error-trellis decoding of dual-k

convolutional codes is that the message sequence can be corrected without the necessity of storing a large number of states or paths in a constraint length of the error trellis diagrams.

-I. S. Reed, I. S. Hsu, J. M. Jensen and T. K. Truong, "The VLSI Design of an Error-Trellis Syndrome Decoding for Certain Convolutional Codes," IEEE Trans. on Computers, vol. C-35, no. 9, pp. 781-789, September 1986.

Abstract - A recursive algorithm using the error-trellis decoding technique is developed to decode certain convolutional codes, such as dual-k convolutional code. It is demonstrated that such a decoder can be realized readily on a single chip with NMOS technology.

-J. Sun, I. S. Reed, H. E. Huey and T. K. Truong, "Optimal High Rate Systematic Convolutional Codes for Rates 3/5, 3/4, 4/5, 5/6 and 6/7," to be submitted.

Abstract - A new method to search for high rate convolutional codes is achieved by means of a pruned trellis. This makes possible a reduced search procedure which cannot be done by standard methods. This new search procedure makes use of the expanded column distance sequence of a convolutional code. By the use of the optimum distance profile and a maximization of d_{free}, a number of efficient systematic convolutional codes of rates 3/5, 3/4, 4/5, 5/6 and 6/7 are found and listed in this paper.

-I. S. Hsu, T. K. Truong, I. S. Reed and J. Sun, "A New VLSI Architecture for the Viterbi Decoder of Large Constraint Length Convolutional Codes," IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, Victoria, B.C., Canada, June 4-5, 1987.

Abstract - A new algorithm and its pipeline VLSI architecture is developed for the Viterbi decoder of a convolutional code. This new architecture uses a single sequential processor to compute the path metrics in the trellis diagram. Also the systolic array method is used to store the path information as well as to perform the decoding process. It is expected with current VLSI technology that with this new architecture, a Viterbi decoder for a moderate constraint length can be implemented on a single chip. Furthermore, with this new algorithm and architecture, if the constraint length of

the convolutional code is too large to put the Viterbi decoder on a single chip. It is shown that the decoder can be partitioned naturally with relative ease into several separate chips with this new architecture.

-I. S. Hsu, L. J. Deutsch, T. K. Truong, I. S. Reed and H. C. Shyu, "A VLSI Single Chip (255,223) Reed-Solomon Encoder with Interleaver," IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, Victoria, B.C., Canada, June 4-5, 1987.

Abstract - This paper presents a description of a single chip implementation of a Reed-Solomon encoder with interleaving capability. The code used was devised by the CCSDS (Consulative Committee on Space Data Systems). It is a concatenated code, a convolutional inner code of rate 1/2 and constraint length 7 and an outer code, an RS (255,223) with interleaving code. The architecture, leading to this single VLSI chip design, makes use of a bit-serial finite field multiplication algorithm due to E. R. Berlekamp.

b. Dissertations

-H. E. Huey, "Convolutional Codes Generated by Primitive Polynomials," Ph.D. dissertation, University of Southern California, August 1987.

Abstract - This dissertation studies the properties of rate 1/n convolutional codes that have structural constraints placed on the subgenerators. It is shown that many families of these structure constrained codes have properties which are not conducive to generating a family of codes with good properties. A family of convolutional codes using primitive polynomials is studied which have both large free distance and minimum average weight per branch. A method is given that provides a selection of the subgenerators of a 1/2 rate non-systematic code.

An analysis is presented about the weaknesses of the various structure-constrained codes such as convolutional codes generated by cyclic codes and convolutional codes which have constraints placed on their subgenerator polynomials. The analysis is presented in terms of bounds on free distance and minimum average weight per branch, the generator weight distributions, and catastrophic code generation. A list of properties that tend to lead to the creation of bad families of codes is developed from the study of structure-constrained codes.

Theoretical results are presented that show a relation exists between the two distance measures, free distance and minimum average weight per branch. This relationship is due to the fact that upper bounds can be established for both distance measures which show a dependence on the weight distribution of the subgenerators. The established upper bounds and an analysis of the best free distance codes show that good codes should have a total generator weight near the Heller upper bound and that the subgenerators should have balanced weight. It is also shown that many of the best free distance codes have subgenerator polynomials which are primitive polynomials.

An algorithm is presented that shows how to determine candidate 1/2 rate convolutional codes that should have good distance properties using primitive polynomials as subgenerators. Primitive convolutional codes generated by this algorithm are listed. It is shown that these codes are capable of a better free distance and minimum average weight per branch than the best previously defined structure-constrained codes, the complementary codes.

-J. Sun, "Pruned Trellis for Convolutional Code," Ph.D. dissertation, University of Southern California, October 1987.

Abstract - A pruned trellis can be applied both to the search and error-trellis decoding of high rate convolutional codes. By the use of a pruned coding trellis, an "expanded" column distance function (expanded CDF) is obtained from the search algorithm. This expanded CDF approaches the desired CDF of the code as the pruning weights in a pruned trellis become large. New optimal non-systematic convolutional codes, of rate k/n, are found by this new search algorithm.

If a pruned error-trellis is used to decode a convolutional code, a substantial number of state transitions of the error-trellis can be eliminated. Simulations show that for high-rate non-systematic convolutional codes, this reduction is significant, and that the error probability performance suffers only a small degradation, about 0.2 dB below that of a conventional Viterbi decoding algorithm.

8. List of Profes.ional Personnel Associated with the Research Effort:

-Jaw John Chang received the B.S. degree from National Taiwan University, Taiwan, in 1965, the M.Eng. degree from Asian Institute of Technology, Thailand, in 1970, and the Ph.D. degree from the University of Southern California in 1981.

-Leslie J. Deutsch received the B.S. degree in mathematics from the California Institute of Technology, Pasadena, in 1976, and the M.S. and Ph.D. degrees in theoretical mathematics from the California Institute of Technology in 1979 and 1980, respectively, specializing in harmonic analysis.

-In-Shek Hsu received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan in 1978 and 1980, and the Ph.D. degree in electrical engineering from the University of Southern California, Los Angeles, in 1984.

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-J. M. Jensen received the B.Sc. degree in computer sciences in 1980 and the M.Sc. degree in mathematics in 1983, both from Aalborg University Center, Aalborg, Denmark.

-Irving S. Reed received the B.S. and Ph.D. degrees in mathematics from the California Institute of Technology, Pasadena, in 1944 and 1949, respectively.

-Howard M. Shao received the B.S. degree in communication engineering from National Chiao Tung University, Taiwan, in 1975, and the M.S. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, in 1979 and 1983, respectively.

-Ju Sun received the M.S. degree in electrical engineering from the University of Southern California, Los Angeles, in 1983.

-T. K. Truong received the B.S. degree in electrical engineering from the National Cheng Kung University, Taiwan, China, in 1967, the M.S. Degree in electrical engineering from Washington University, St. Louis, MO, in 1971, and the Ph.D. degree from the University of Southern California, Los Angeles, in 1976.

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