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ARO-20569 8-EL DAAG29-83-K-0125

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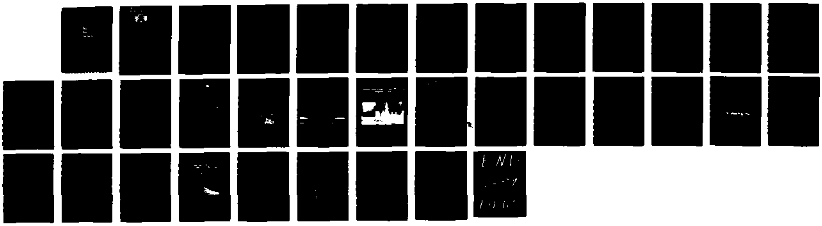

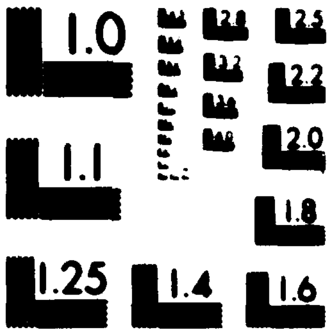

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REPORT DOCUMENTATION PAGE

DTIC ELECTE S D

1a REPORT SECURITY CLASSIFICATION: Unclassified	1b RESTRICTIVE MARKINGS
2a SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION / AVAILABILITY OF REPORT: Approved for public release; distribution unlimited.
2b DECLASSIFICATION / DOWNGRADING SCHEDULE	
4 PERFORMING ORGANIZATION REPORT NUMBER(S)	5 MONITORING ORGANIZATION REPORT NUMBER(S): ARO 20569.8-EL
6a NAME OF PERFORMING ORGANIZATION: Stanford University	6b OFFICE SYMBOL (If applicable)
7a NAME OF MONITORING ORGANIZATION: U. S. Army Research Office	
6c ADDRESS (City, State, and ZIP Code): AEL 201, Stanford, CA 94305	7b ADDRESS (City, State, and ZIP Code): P. O. Box 12211, Research Triangle Park, NC 27709-2211
8a NAME OF FUNDING / SPONSORING ORGANIZATION: U. S. Army Research Office	8b OFFICE SYMBOL (If applicable)
9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER: DAAG29-83-K-0125	
8c ADDRESS (City, State and ZIP Code): P. O. Box 12211, Research Triangle Park, NC 27709-2211	10 SOURCE OF FUNDING NUMBERS: PROGRAM ELEMENT NO / PROJECT NO / TASK NO / WORK UNIT ACCESSION NO

11 TITLE (Include Security Classification): Computer Modeling of Complete IC Fabrication Process

12 PERSONAL AUTHOR(S): Professor Robert W. Dutton

13a TYPE OF REPORT	13b TIME COVERED	14 DATE OF REPORT (Year, Month, Day)	15 PAGE COUNT
Final Report	FROM 10-1-83 TO 2-1-87	May 28, 1987	32

16 SUPPLEMENTARY NOTATION: The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

17 COSATI CODES			18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Process simulation, SUPREM, Device Analysis, SEDAN, PISCES, Hot carriers, parallel processing, Monte Carlo, Transient analysis, SPICE models, Latchup CMOS, BiCMOS, GaAs, HgCdTe, photoconducting switches.

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

The focus of this research effort is the development of fundamental algorithms for process and device modeling as well as novel integration of the tools for advanced IC technology design. The development of the first complete 2D process simulator, SUPREM 4, is reported. The algorithms are discussed as well as application to local oxidation and extrinsic diffusion conditions occur in CMOS and BiCMOS technologies. The evolution of 1D (SEDAN) and 2D (PISCES) device analysis is discussed. The application of SEDAN to a variety of non-silicon technologies (GaAs and HgCdTe) are considered. A new multi-window analysis capability for PISCES which exploits Monte Carlo analysis of hot carriers has been demonstrated and used to characterize a variety of silicon MOSFET and GaAs MESFET effects. A parallel computer implementation of PISCES has been achieved using a Hypercube architecture. The PISCES program has been used for a range of important device studies including: latchup, analog switch analysis, MOSFET capacitance studies and bipolar transient device design for ECL gates. The program is broadly applicable to RAM and BiCMOS technology analysis and design. In the analog switch technology area this research effort has produced a variety of important modeling and technological advances. A novel two-lump representation for both silicon and GaAs FET devices has been developed and confirmed experimentally. Three generations of photo conducting circuit element (PCE) switches have been developed--two in pure silicon technologies and the third using GaAs on Si. The best results show 2.5 ps FWHM pulses for polysilicon.

20 DISTRIBUTION / AVAILABILITY OF ABSTRACT: ☐ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	21 ABSTRACT SECURITY CLASSIFICATION: Unclassified
22a NAME OF RESPONSIBLE INDIVIDUAL	22b TELEPHONE (Include Area Code) / 22c OFFICE SYMBOL

DD FORM 1473, 84 MAR — 83 APR edition may be used until exhausted. All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE: UNCLASSIFIED

ARO 20569.8-EL

COMPUTER MODELING OF COMPLETE

IC FABRICATION PROCESS

Final Report

by

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October 1, 1983--February 1, 1987

Prepared for

U. S. Army Research Office
Research Triangle Park, NC

Contract No. DAAG29-83-K-0125

Approved for public release; distribution unlimited

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COMPUTER MODELING OF COMPLETE IC FABRICATION PROCESS

Abstract

The focus of this research effort is the development of fundamental algorithms for process and device modeling as well as novel integration of the tools for advanced IC technology design. The development of the first complete 2D process simulator, SUPREM 4, is reported. The algorithms are discussed as well as application to local oxidation and extrinsic diffusion conditions occur in CMOS and BiCMOS technologies. The evolution of 1D (SEDAN) and 2D (PISCES) device analysis is discussed. The application of SEDAN to a variety of non-silicon technologies (GaAs and HgCdTe) are considered. A new multi-window analysis capability for PISCES which exploits Monte Carlo analysis of hot carriers has been demonstrated and used to characterize a variety of silicon MOSFET and GaAs MESFET effects. A parallel computer implementation of PISCES has been achieved using a Hypercube architecture. The PISCES program has been used for a range of important device studies including: latchup, analog switch analysis, MOSFET capacitance studies and bipolar transient device design for ECL gates. The program is broadly applicable to RAM and BiCMOS technology analysis and design. In the analog switch technology area this research effort has produced a variety of important modeling and technological advances. A novel two-lump representation for both silicon and GaAs FET devices has been developed and confirmed experimentally. Three generations of photoconducting circuit element (PCE) switches have been developed--two in pure silicon technologies and the third using GaAs on Si. The best results show 2-5 ps FWHM pulses for polysilicon.

Introduction

The area of Technology CAD has evolved rapidly over the last decade. Beginning with the SUPREM program funded in large part Army Research Office grants, three generations of 1D TCAD tools and two generations 2D tools have been developed. During the present grant period the second generation 2D efforts have been aggressively pursued. Over the period of nearly ten years a total of 13 PhD's have been graduated as well as more than a dozen Masters degrees have been awarded with support from this research program. In the following sections the specific accomplishments of this grant period are discussed. Four major areas are considered. The 2D modeling efforts are certainly the most broadly visible and are discussed first. Next the more mature area of 1D TCAD tools are presented. Based on both the 1D and 2D TCAD efforts, a variety of applications have developed and a representative sample of these is given. Finally, the area of analog switch technology is discussed--both as a TCAD application and in terms of its fundamental importance for both analog and digital circuit design.

Two-Dimensional TCAD Tools:

It is useful to begin this discussion by considering state-of-the-art 2D simulators used at the beginning of this grant period. Beginning early in the 1980's, a limited range of 2D TCAD tools emerged. The Stanford tools included: SUPRA (2D process), SOAP (2D oxidation), and GEMINI (2D Poisson). Other codes of this era developed elsewhere include: ICECREAM (2D process) [1], BICEPS (2D process) [2], and MINIMOS (2D device) [3], to mention only a few. Yet all these tools were rather narrow in scope--topographies and technologies were not general. A major goal of this research was directed at overcoming these limitations. Moreover, a set of technologically relevant examples were considered as test vehicles--these will be discussed in a later section.

During the period 1984-1985 the second generation of the PISCES program emerged as Stanford's most robust and versatile 2D device simulation [4] [5]. The program, initially developed as a Poisson and single carrier solver, was generalized to include two carrier analysis for dc, ac, and transient conditions. The topography input capabilities were generalized to handle a wide variety of nonplanar structures. Hence structures including oxidation and even trench isolation could be analyzed. In addition to the broad technology relevance demonstrated with PISCES, the program served as a vehicle for basic investigation of numerical methods. As a result of this work, a comprehensive comparison of iterative techniques including choice of analysis variables was made [6]. More recently, based on consideration of the growing computational bottlenecks involved with TCAD [7], PISCES is now being used as a vehicle for consideration of parallel computation algorithms [8]. The further exploration of parallel algorithms is one of the most exciting areas for follow-on research.

Another aspect of the device analysis programs is the growing importance for hot carrier device physics. The limitations of conventional carrier drift/diffusion analysis are serious, yet simple methods to extend the model accuracy pose both physical and computational difficulties [7]. During the last year of this contract we have demonstrated a novel multi-window version of PISCES where a Monte Carlo analysis is performed within a more extensive drift/diffusion analysis domain [9]. This multi-window version, called PISCES-MC, provides an important tool for better understanding the carrier transport problems in small dimension devices. In the follow-on research program to be partially supported by the Army Research Office, this multi-window technique will be developed and extended further.

The key points to be emphasized concerning 2D device analysis are the following:

1. The development of a robust, technology-oriented device simulator, PISCES 2.
2. A depth of understanding of associated analysis methods and new breakthroughs in terms of parallel processing.
3. Demonstration of a novel multi-window Monte Carlo analysis method (PISCES-MC) with application to a broad range of hot carrier effects.

In parallel with the development of the PISCES 2 device simulator, the development of an integrated 2D process simulator, was initiated. Previous efforts with the SUPRA and SOAP programs had major limitations. In the case of SUPRA, the oxidation kinetic models were totally lacking. For SOAP, the program was a stand-alone oxidation model with no coupling to diffusion. Hence, there was a need for a totally integrated simulator. Progress over this three year contract period has been rapid and productive. A novel time-step approach was first developed to solve the numerically stiff multi-particle diffusion problem [10]. Next, a robust set of gridding techniques were developed to handle the 2D oxide growth and moving interface which affects dopant redistribution [11]. Finally, the coupled dopant diffusion and point-defect kinetic effects have been modeled accurately [12] and applied to specific dopant redistribution problems [13]. Beginning in early 1986 the SUPREM 4 simulator was released. Based on the most recent technical developments and code revisions, the program can handle a majority of intrinsic device and isolation structure process analysis for MOS technologies.

Highlight accomplishments in the area of 2D process simulation include:

1. Advanced gridding techniques and modeling for local oxidation including trench-

etched surfaces.

2. Accurate characterization and modeling of point defect kinetics and coupled dopant diffusion effects.

3. Demonstrated application to CMOS well-diffusion technology.

One-Dimensional TCAD Tools:

The above discussion has highlighted accomplishments in the area of 2D TCAD tools. Commensurate with the need for more powerful 2D tools to magnify and illuminate the detailed technology problems, there is a growing need for more versatile 1D TCAD tools. Specifically, the use of 1D tools is both efficient in looking at the multifaceted problems of technology development and in exploring detailed device physics. During this contract period both of these aspects of 1D TCAD have been developed.

During the first part of this contract period the emphasis in 1D TCAD centered on the development of SEDAN algorithms and models for poly-emitter bipolar devices. The results involved both improved process models in SUPREM [14] and a generalized interface model for SEDAN [15]. The net result was both improved physical models and the ability to link SUPREM 3 with SEDAN 3 to analyze both MOS and bipolar devices. The recent advent of the so-called BiCMOS technology has been an ideal application for this coupled 1D TCAD environment. Indeed, there has already been active industrial use of this tool set to optimize BiCMOS [16].

Beyond the multi-device analysis and optimization applications for 1D TCAD there is a growing set of needs related to analysis of compound materials. The SEDAN environment has been extended and adapted to several classes of compound materials--specifically HgCdTe (HCT) and GaAlAs/GaAs. Although only limited research publications have resulted in these areas to date, the industrial and government interest and use in these areas is tremendous. For example, in the HCT area, companies such as Ford Aerospace (FACC) and Santa Barbara Research (SBRC) are both active and enthusiastic users of SEDAN. In the GaAs and related areas there is encouragement and support from both government (DARPA) and industrial (SRC) agencies to continue the work. There is a range of advanced physical models that have been implemented in SEDAN. For example a tunneling model for HCT and an EL2 trapping model for GaAs are both being tested in SEDAN. Also, the Monte Carlo analysis capability based on SEDAN initial solutions has been used to understand several Schottky contact effects in GaAs and to in turn improve the boundary conditions used in SEDAN. Based on partial DARPA support, a complete 1D TCAD for GaAs based on SUPREM 3.5 and SEDAN 3 is a reasonable goal. However, lack of sufficient funding in the device analysis area is a major limitation.

TCAD Applications

In the initial proposal for this contract period, the coupling of technology, device and even circuit design activities was considered to be an important target. For example, understanding the physical basis for parameters and developing compact engineering representations was desired. Moreover, the extraction of process sensitivities and even application to optimization was suggested as a suitable end goal. In this section a variety of applications are briefly discussed.

During the first half of the contract period, the problems of CMOS latchup and its simulation were pursued. The PISCES program was used extensively to investigate latchup [7] [17] and technology choices to reduce latchup susceptibility [18]. In fact, many of the basic features for PISCES in terms of geometry and general bias conditions for bipolar device effects came out of the needs for latchup simulation. Industrial interest in this application has been very high and there are literally dozens of papers published by other research groups using PISCES as the basic tool for analysis. Included in the latchup analysis work is the development of mixed-mode capabilities for coupled device and small circuit analysis. For example, a variety of circuit-type (resistive and capacitive) boundary conditions are easily implemented with PISCES.

The second half of this contract period has focused the research efforts in the area of process simulation (SUPREM 4). In this area of activities the modeling of process sensitivities has become the major focus. The simulation of n-well choices for a CMOS technology have been one significant application [13]. The problem of lateral dopant diffusion is important for design-rule spacings and in regards to latch-up. The controlling mechanisms related to point defect kinetics are of major concern [12] and on-going experimental efforts are essential to the useful application of SUPREM 4. Further applications related to silicon technology are conceived yet funding limitations preclude aggressive research efforts. Specifically, drain doping profiles (LDD) and isolation structures (LOCOS and trench) can now be modeled and characterized. One technology vehicle of special interest is the BiCMOS process which is becoming the industry standard MOS technology. The demands on all aspects of this technology are severe and future application of process/device simulation tools deserves a more serious research effort.

In addition to the above mentioned major efforts related to TCAD applications and the investigation of process sensitivities, a variety of specific device applications have been demonstrated. The detailed understanding of velocity saturation on short-channel capacitance effects in MOS devices has been achieved [19] and confirmed with novel measurement techniques [20]. The details of analog switch operation in MOS circuits has been experimentally characterized [21] and modeled based on both analytical and PISCES models [22] [23]. Finally, a new methodology for SPICE model development and support has been demonstrated using PISCES as a tool to extract unique electrostatic boundary conditions [24]. In total, these three applications demonstrate both the power and versatility of TCAD-based modeling work. Each effort has facilitated the extraction of detailed model parameters based on physically meaningful process and device information. In the same spirit as mentioned for further SUPREM 4 efforts, BiCMOS will be used as a vehicle in the device modeling area as well. Preliminary results already indicate extremely promising information concerning new ECL circuitry being investigated for BiCMOS application [25]. However, as stated in regard to other applications cited above, the growing deficit of research funding in this area is a critical limitation.

Analog Switch Technology

The above activities have focused primarily on TCAD and its application. During the course of this contract, starting from activities in device characterization, a variety of analog switch technologies have been investigated and modeled. In the previous section the efforts related to silicon "pass transistors" were described. Novel structures were fabricated [21] and extensive modeling was done to characterize fundamental limits [22, 23]. This work has major impact on the ultimate speed/accuracy trade offs in analog digital systems and memory circuits as well. Noise injected by the MOS analog switches is a fundamental limit in scaled circuit technologies. In the following, two other analog switch efforts are now discussed.

From the inception of this research program the need to calibrate TCAD by means of experimental device characterization was recognized. In the area of capacitance modeling discussed in the previous section, new modeling insight as well as characterization methods were developed. For high speed transient device characterization, previous work with s-parameters had yielded very promising results [26]. However, the need for parasitic free time-domain modeling was a major unachieved goal. At the beginning of this contract period we demonstrated our first photo conducting circuit element (PCE) in bulk silicon with sub-50 ps time resolution (full-width-half max) pulses [27]. Over the duration of the contract, two follow-on generations of PCE technology have been developed . First, starting from the bulk silicon PCE technology, and polysilicon implementation was realized with sub-50ps FWHM pulse resolution [28]. Moreover, a new CAD tool was developed to model and characterize the PCE performance. Within the past year, a third generation PCE has been demonstrated using MBE GaAs on silicon technology [29]. This technology shows pulse speeds comparable to our best silicon results and pulse amplitudes as much as an order-of-magnitude larger. From another point of view, the GaAs PCE's have impedances in the range of 100's of ohms compared to 1000's of ohms for the silicon technology. We plan to continue these efforts vigorously although to date we have not found a suitable funding source. The applications we foresee for GaAs PCE technology are centered on optical interconnect and clock distribution systems.

A final topic reported for completeness is the development of a SPICE model for a GaAs HFET [30]. Although the model was developed under industrial (SRC) sponsorship, the implication for analog (i.e. MIMIC) applications is substantial. The basic model is similar to the two-lump MOSFET model discussed above. For both the MOSFET and HFET, the use of two-lumps to represent the channel charge is a key concept. This partitioning allows the consideration of channel transit times and even non-reciprocal effects of gate capacitance, similar to results presented in an earlier contract [31]. The implications are indeed important in understanding the physical effect and also providing an easy-to-implement technique for SPICE modeling. We consider the development of the approach generic to FET structures and a significant conceptual break-through.

Summary and Conclusions

In this report we have outlined broadly the research accomplishments in the area of Technology CAD. Stanford has developed an exceptional TCAD tool set with broad application to not only silicon but also GaAs and HCT technologies. The SUPREM program now has three specific lines of applicability:

1. SUPREM 4 for 2D silicon simulation
2. SUPREM 3 for 1D silicon and multiple cross-section technology optimization
3. SUPREM 3.5 for 1D GaAs simulation

The ongoing development of physical models for these simulators is now supported by SRC (silicon) and DARPA (GaAs). The device simulation area has been driven to support two major activities:

1. SEDAN 3 as a general materials simulator including:
    a. GaAs and HCT
    b. Multi cross-section silicon process optimization
2. PISCES development in the areas of:

3.

a. General geometry simulator of dc, ac, and transient conditions in silicon

b. Hot carrier analysis using a new windowed Monte Carlo analysis

c. Preliminary results in parallel algorithms

Especially in the device analysis area, there is a critical lack of further support for both basic algorithm work and ongoing applications. Appendix 1 summarizes the activities related to SEDAN and PISCES and indicates both future trends and the magnitude of the looming funding crisis in this area.

Turning to Applications of TCAD, the research efforts have provided a variety of demonstrations. The previous sections have considered the following collection of specific applications:

1. CMOS latchup analysis and modeling
2. Capacitance measurement and simulation
3. Analog (Pass Transistor) switch measurement and modeling
4. Methodology based on PISCES and specific model implementations to support SPICE.
5. BiCMOS device technology development and circuit modeling.

Finally in the analog switch technology, the following major accomplishments have been realized:

1. Demonstration of novel PCE structures with the following measured performances:
    a. bulk silicon - 20 psec FWHM pulses
    b. poly silicon - 3 psec FWHM pulses
    c. GaAs on silicon - < 50 psec FWHM pulses
2. Unique two-lump model for mobile channel charge in FETs with demonstrated application to:
    a. Silicon MOSFETs for analog (pass transistor) switches
    b. GaAs HFETs

In addition to the specific thesis research efforts, there has been a concentrated effort to have a dialog with government, universities, and industry. Each year Stanford holds a research review in the TCAD area with broad industrial attendance. Appendix 2 gives sample programs and attendance information. Finally, Professor Dutton is in the final stages of preparing a book for publication on Process and Device CAD. This text is targeted for a broad audience of users of TCAD and is expected to help fill the educational gap in this area. In the area of applications it is anticipated that the next stage will involve a strong development and evolution toward manufacturing science. The need to apply the tools aggressively to the building of real technologies is critical to the long term survival of all high technologies in the United States. As a final point a theme presented throughout the report should be again emphasized. The area of device simulation is critical to advanced technology research and manufacturing science. However, the present situation in federal funding in this area leaves a huge gap between unmet modeling needs and present level of research funding.

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Stanford Research Accomplishments in Device Analysis--- A Short History of SEDAN and PISCES

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Over the period of nearly a decade, the Stanford research group under the direction of Professor Dutton has developed a set of 1D and 2D device modeling tools (SEDAN and PISCES) which provide a unique platform for technology oriented device design. In particular, the SEDAN program provides comprehensive 1D analysis of both dc and transient current flow for silicon, GaAs and HgCdTe (HCT) technologies. The PISCES program solves for dc, transient and ac conditions in nonplanar 2D structures. In the following discussion, each of these two codes and their capabilities are discussed in detail. The emphasis of discussion is focused on capabilities and internal models compared to the numerical aspects of the simulators.

The SEDAN program has evolved from a simple stand-alone 1D solver for Poisson and two carrier continuity equations (version 1) into a technology-oriented tool (version 2). Specifically, the second version was modified to couple with SUPREM, the 1D process modeling program, and provide an integrated process-device analysis environment. However, the physical models were rather basic. In addition to concentration-dependent mobility and lifetime (used in SHR recombination) the effects of Auger recombination and bandgap narrowing were included. With the evolution of SUPREM 3 to include multilayer systems such as polysilicon-silicon, SEDAN was also changed to couple to the technology base. In particular, the modeling of polysilicon emitters was a driving force to expand the physical models. The added multilayer capabilities of SEDAN lead to the generalized materials modeling capabilities to be discussed shortly. The specific concerns related to polysilicon emitter bipolar devices is the interfacial oxide tunneling and grain boundary effects on transport current. The consideration of tunneling effects in fact opened the way for HCT effects to be discussed.

In parallel with the polyemitter developments, SEDAN 3 was generalized to include first GaAs and then HgCdTe material systems. Initially this involved a generalization of the energy band representation and new sets of relationship for mobility, lifetime and recombination--in both cases the composition variations were included as well. Beyond this first step, a variety of more difficult transport problems have unfolded. In the case of HCT, the problem of band-to-band tunneling current is crucial and has been implemented. For GaAs, the trapping of carriers--both the dc and transient effects--is essential and is now included in SEDAN.

The above discussion has briefly outlined the evolution of SEDAN. While the present array of physical models have substantially extended the capabilities, there is a number of further enhancements needed to continue to meet the objectives of technology relevance for generalized semiconductor materials. Most obvious is the need to obtain realistic dopant, defect and stociometry profiles for compound materials. In the case of GaAs, the first generation of SUPREM 3.5 is nearing completion. However, complex effects such as disordering of super lattices, which can dramatically affect transport, are but one example of new models that are needed. Also, the modeling of quantum-well confinement is an important challenge. Similar problems remain to be solved for HCT. Finally, the needs for improvement in the silicon domain are by no means exhausted. Heteroepitaxy in silicon is now every bit as important as for the compound materials. Moreover, the consolidated use for process optimization of several cross-sections--for example in a BiCMOS technology--still provides technical challenges such as new emitter and source/drain materials (i.e. silicides). However, one aspect of SEDAN stands out more than any other. In the context of new models for device analysis, it is an excellent test-bed for both the physics and as a "spring-board" into 2D or even 3D codes. With this background, let us turn specifically to the evolution of PISCES.

The PISCES code (version 1) began as a Poisson and single carrier solver based on a finite element formulation. The initial objective was to explore attractive methods for parallel computation. The evolution of PISCES 2 was driven by a two-fold objective--to model GaAs MESFETs and the latchup problem in CMOS. These divergent needs resulted in a rather general simulator which can handle complex boundary conditions as well as physical models for materials properties. For example, the code treats ohmic, distributed resistive and Schottky boundary conditions as well as dielectric interfaces with surface recombination. The physical models include lifetime, generation and bandgap narrowing expressions very similar to those used in SEDAN. The mobility expressions include doping field effects and the differences due to either silicon or GaAs substrates. Because of the element-oriented method for assembling the data, model changes to account for better physical approximations are easily included. Both Boltzmann and Fermi-Dirac statistics are available.

From a technology perspective, the critical feature of PISCES which separates it from most other 2D simulators is its generality and versatility for analysis of complex geometry structures. For example, Figure 1 shows several geometries and device structures for silicon technologies that have been analyzed with PISCES. Figure 1a shows a twin-tub CMOS process where latch-up properties between the n^+ and p^+ contacts are modeled. Figure 1b shows a different CMOS technology with a trench used to electrically isolate the n^+ and p^+ regions. Finally, Figure 1c shows a dielectrically isolated emitter coupled bipolar pair which is analyzed in a mixed mode (device and circuit analysis) to understand gate transient effects. This range of cross sections shows effects of local oxides, trenches, FET and bipolar devices. Other examples illustrate MESFET, SOI, and a variety of both passive and active distributed device effects. The program accepts 1D process simulation profiles from SUPREM 3 and will soon be extended to interface to SUPREM 4 (2D). Analytic functions can be used independently or in conjunction with SUPREM to generate 2D profiles. Especially the nonplanar analysis aspects of PISCES make it extremely powerful for technology assessment.

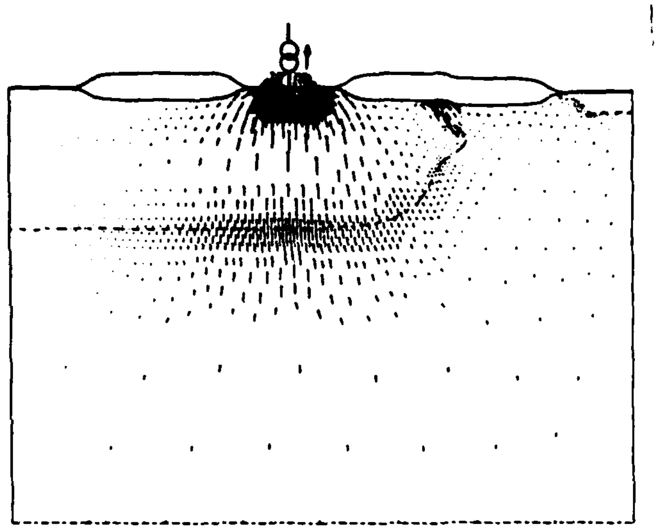
The range of analysis capabilities of PISCES includes dc, transient and ac analysis. The dc solution can include Poisson only, couple one-carrier or full two-carriers and Poisson solutions. A variety of numerical approaches including direct LU factorization or several iterative techniques are also available for the user to select. In some sense the use of the code as a research vehicle for algorithms work has been left in place for the users convenience. To accommodate efficient transient analysis, advanced time step methods have been implemented. Recently, several new algorithms for bias projection have been developed and are expected to be implemented in PISCES as well.

The extension of PISCES in terms of physical models and materials analysis capabilities is the major area of recent research activities. In order to analyze GaAs as well as silicon hot carrier effects, a coupled solution method involving a Monte Carlo (MC) carrier analysis has been developed. Specifically, a MC window is opened within a larger drift-diffusion window. This allows hot carrier transport and even avalanche effects to be simulated. A number of improved materials models have been developed at user sites other than Stanford and are being evaluated for incorporation in a release version. These models include: optical and alpha-trace generation terms and a simple multilayer semiconductor model to approximate planar heterojunction interfaces. A trap model implemented in SEDAN is also planned to be implemented in PISCES. This should be especially important for consideration of effects related to dc backgating and slow-tail transient effects in GaAs MESFETs. This trapping model could also prove useful in analysis of HCT structures.

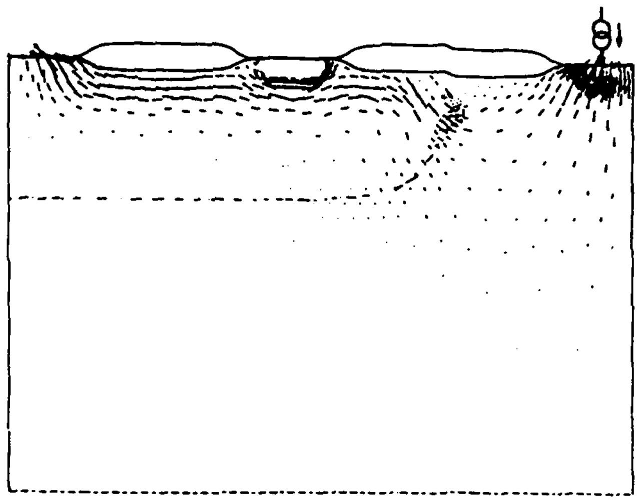
The computation environment suitable for SEDAN and PISCES is diverse and depends on application. SEDAN has been implemented on everything from IBM/AT and Intel Hypercube "personal" computers to MicroVax workstations and Convex C-1 mini-super computers. It uses Fortran 77 and requires only modest (1 Mbytes). Run times for SEDAN are typically of tens-of-seconds per bias point on a workstation. The PISCES program is also written in Fortran 77 and requires somewhat larger amounts of storage (8 Mbytes). The machine environment suitable for PISCES ranges from MicroVAX or SUN workstations up to Convex C-1 mini-super and Cray supercomputers. Several minutes per bias point are typical for PISCES running on workstations. The operating system environment at Stanford is almost exclusively UNIX-based. However, ports of these codes to other system environments are available commercially. Both direct distribution of the Stanford versions and information regarding commercial versions are available through Stanford's Office of Technology Licensing.

Because of growing computational costs of multidimensional device and process analysis, Stanford is now actively investigating multiprocessor implementations of codes such as PISCES and SUPREM. To date the primary research vehicle is the hypercube architecture. Very promising results have been obtained with 16 nodes, achieving as high as 60% utilization, for a nested-dissection LU factorization method. The algorithm research is targeted to be generic and broadly applicable to other parallel architectures. For example, the next generation Cray YMP should be a suitable supercomputer environment and next generations of Convex and Alliant mini-super computers should also be appropriate target machines.

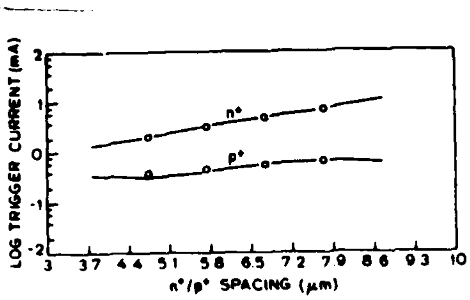
In summary, the Stanford effort's in developing one- and multi-dimension device analysis tools to support a variety of device technology bases--silicon, GaAs and HCT--has been highly successful and productive. Limited funding resources is the major obstacle which now slows progress. The total industrial and government support at this time is less than three full-time equivalent staff members for both the silicon and compound materials efforts. To sustain the past level of productivity the total funding level need to be roughly tripled. It is strongly recommended that interested industrial concerns and major government programs, MMIC, and SEMATECH for example, consider the importance of this research area and specifically the leverage provided by the continued Stanford research efforts.



Current flow prior to triggering for the vertically triggered (n^+) case. Current is primarily electrons flowing in a manner similar to that in an isolated vertical n-p-n transistor.

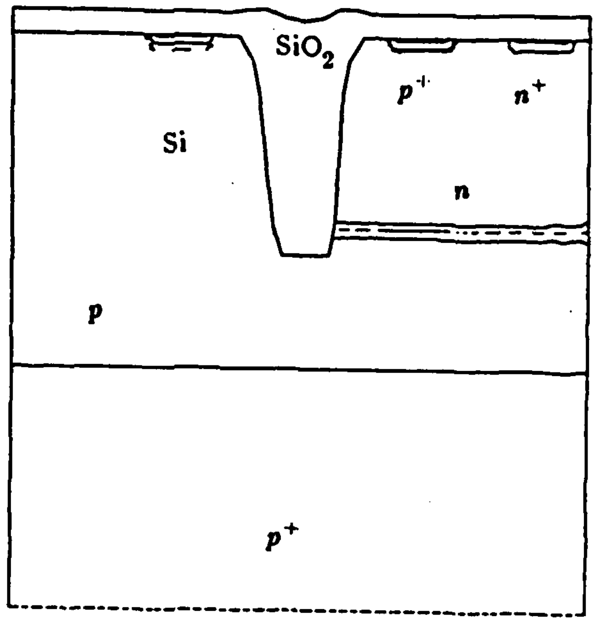


Current flow prior to triggering for the laterally triggered (p^+) case. Note the large majority carrier (hole) current in the p-tub.

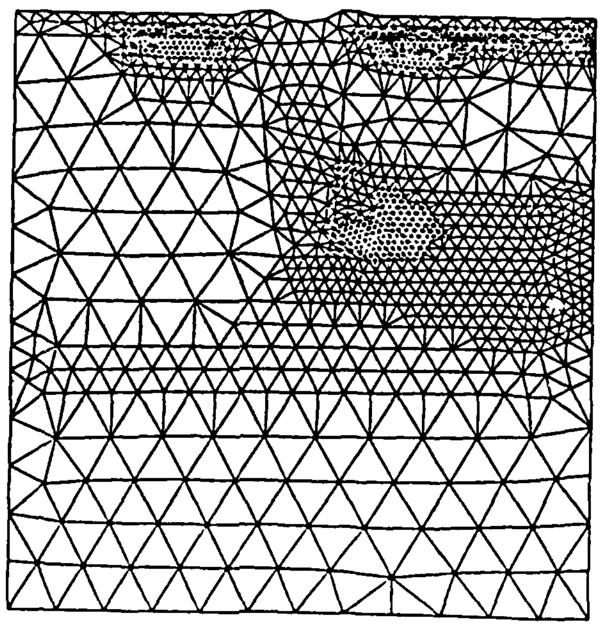


Trigger current (log) plotted as a function of anode-cathode spacing (L) for current injected into the n^+- and p^+-emitters. Solid lines are measured data, and points are simulated.

Figure 1a Twin-Tub CMOS Latch-up Modeling with PISCES,
i) vertical current in n^+
ii) lateral current in p^+
iii) trigger current versus contact spacing

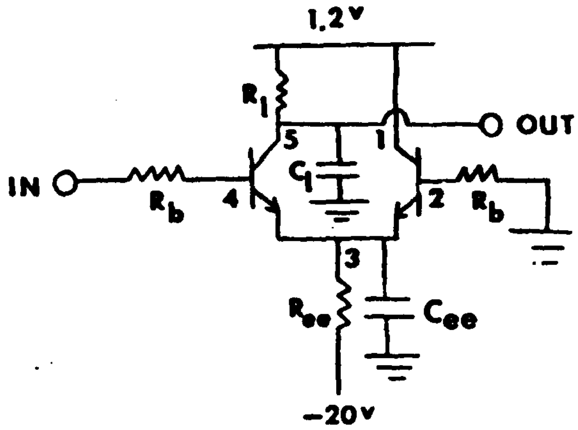


Geometry



Working grid

Figure 1b Trench Isolation Structure
i) physical structure
ii) grid structure used by PISCES



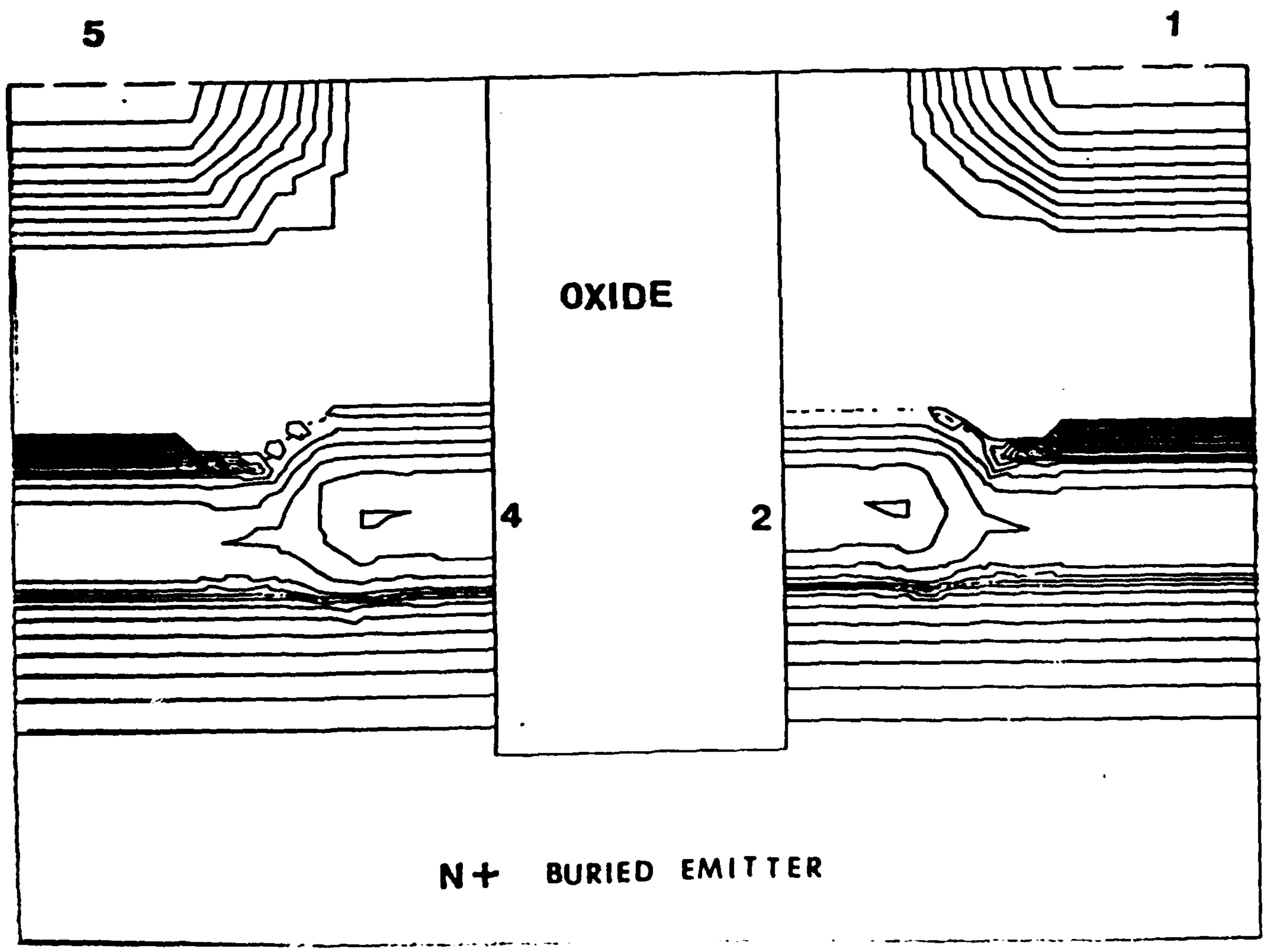
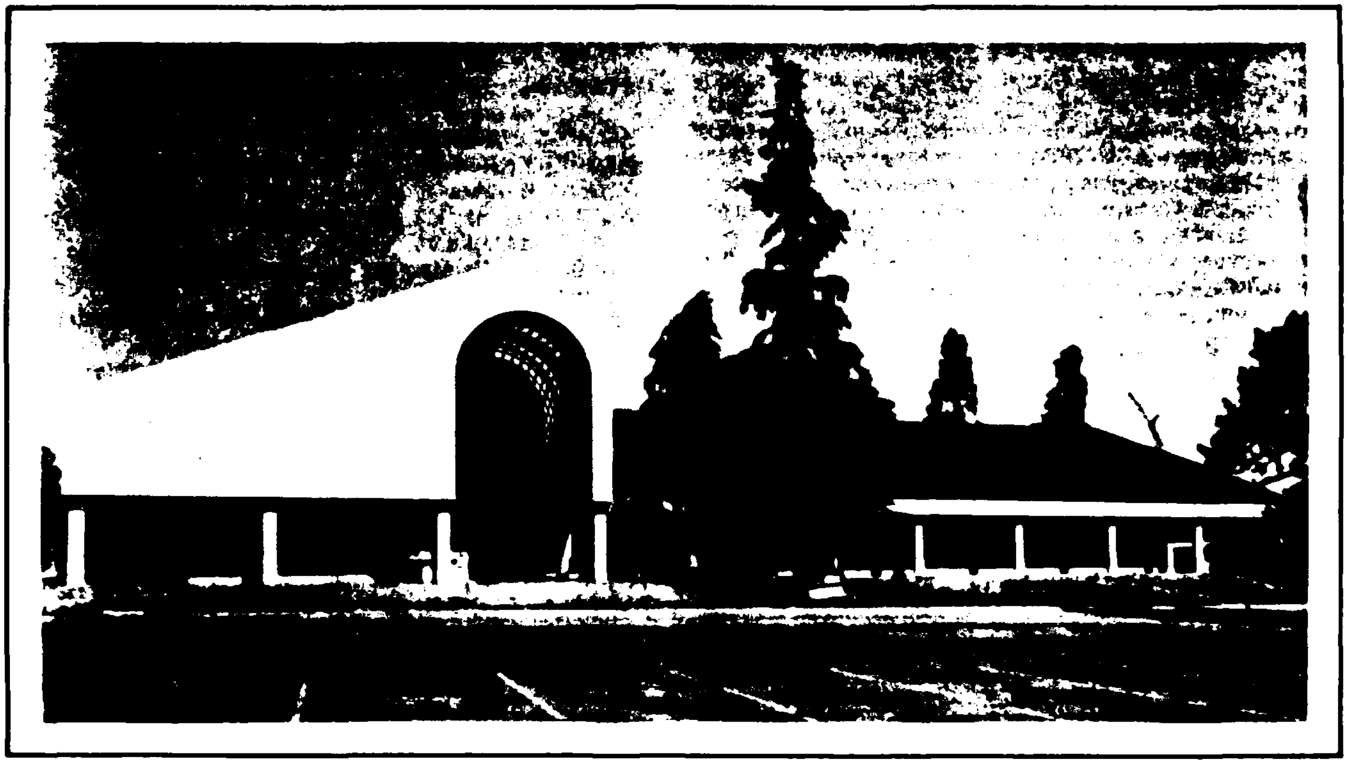


Figure 1C Collector-UP Bipolar ECL Structure
i) circuit schematic
ii) physical cross-section used for PISCES analysis

Stanford University Announces a Three-Day Program

Computer-Aided Design and Manufacturing of Integrated Circuits

August 20-22, 1984



Monday, August 20	Processing Technology
Tuesday, August 21	Simulation and Applications
Wednesday, August 22	Manufacturing Science

Computer-Aided Design and Manufacturing of Integrated Circuits

A three-day program:
August 20-22, 1984, Stanford, California

Over the past decade Stanford University has pioneered a fundamental research effort to understand and model integrated circuit (IC) technology.[1] Once each year the Integrated Circuits Laboratory at Stanford presents a summary of recent findings, in the context of a short-course style discussion. Last year we expanded the program to cover not only modeling and CAD tools but also manufacturing science. This year, topics related specifically to laboratory and equipment automation are discussed. Also, for the first time we will include selected topics on compound semiconductors as well as silicon technology.

The discussion of processing technology at this year's meeting shows both evolutionary and revolutionary changes. Major advances in both analytic tools and models for diffusion kinetics are reported. The introduction of compound semiconductor material topics reflects the growing industrial interest as well as Stanford research effort in the field. Stanford has developed a variety of process and device simulation programs which embody the results of fundamental research efforts and are of substantial value for process development and device design. In the area of process simulation the SUPREM program is widely used for both design and in understanding process sensitivities. Advances in SUPREM models will be discussed. The one-dimensional device simulator SEDAN and the two-dimensional PISCES program have both advanced substantially since last year's meeting. The documentation and release of PISCES are a highlight of this year's meeting.

Stanford has established a manufacturing capability to fabricate IC's for systems design such as the MIPS processor project on a fast-turn-around basis. In this manufacturing spirit we have an ongoing need to develop expertise in IC manufacturing science. We are developing a computer-aided system, FABLE, to assist in line management, documentation, and training for IC manufacturing. A key component of the FABLE system is models for equipment. The emphasis of the third day will be on both the system context and details of equipment automation. This will include consideration of standards to facilitate system integration.

The meeting format will consist of a series of lectures as outlined in the program. Copies of material presented by the speakers are included in the course materials. In addition, there will be a distribution of technical reports which give an extended discussion of background information and details of the experiments, models, and computer programs. The first day will involve primarily lectures and discussions of the materials aspects of technology modeling with substantial emphasis on specific experimental and model results applicable to SUPREM. The second day will focus on more general aspects of process and device simulation as well as Stanford-developed tools. The third day emphasizes automation and equipment models.

A "forum" atmosphere will be encouraged to obtain user feedback. A number of specific applications and results (case studies) will be presented. The registration fee provides for all course materials, as well as lunches and dinner (August 20 and 21, 1984).

Location: Terman Auditorium, Stanford University, Stanford, California

[1] This work has been supported through government as well as industrial funding. The Defense Advanced Projects Research Agency, Army Research Office and Semiconductor Research Corporation are specifically responsible for major sources of research funding.

Fee: The fee for each day is $225 (including lecture notes, luncheon, and dinner (August 20, 21, 1984) or $575 for attending three days. Enrollment is limited, and advance enrollment is required.

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GARY B. BRONNER, Research Assistant, Stanford University
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ZHIPING YU, Research Assistant, Stanford University

PROCESSING TECHNOLOGY

Monday, August 20, 1984

8:00 a.m.	Registration	
8:30	Overview of Silicon Technology	Plummer
9:15	Overview of Compound Semiconductor Technology	Harris
9:50	Break	
10:15	Tools for Process Modeling	Dutton

10:50	Oxidation and Surface Kinetics	Tiller
11:10	Micro Analysis Studies of the Growth of Thin Gate Dielectrics	Han
11:30	Interface Microscopy	Bravman
11:50	Lunch	
1:15 p.m.*	Thermal Nitridation of Silicon and Oxidized Silicon	Moslehi
1:35*	Diffusion Modeling	Fahey
2:05*	Transient Effects in Rapid Thermal Annealing	Reed
2:25*	Gettering Kinetics	Bronner
2:45	Break	
3:10	Implantation Modeling in One and Two Dimensions	Giles
3:35	Interconnections & Contacts	Swirhan
3:55	Phase Changes During Silicide Oxidation and Metal Diffusion in SiO_2	Sigmon
4:15	Applications—Industrial Feedback	
	Compound Materials Session	
1:15 p.m.**	Metal Organic Chemical Vapor Deposition	Burnham
2:00**	Molecular Beam Epitaxy	Miller

Parallel Sessions (*)(**)

SIMULATORS, DEVICES, AND CHARACTERIZATION

Tuesday, August 21, 1984

8:30 a.m.	Implementation and Applications of SUPREM	Hansen
9:00	Diffusion Coefficients in SUPREM	Barbuscia
9:25	SEDAN Models for Polysilicon Emitters	Yu
9:50	Characterization of Polyemitter Devices	Patton
10:15	Break	
10:40	Two-Carrier 2D Device Simulation—PISCES II	Rafferty
11:10	Low Temperature CMOS—Physics and Simulation	Woo
11:35	An Impact Ionization Model for 2D Device Simulation	Chan
12:00	Lunch	
1:15 p.m.	Latchup Modeling and Simulation	Pinto
1:45	Schottky Contact Modeling and Latchup Prevention	Sangiorgi
2:10	Three-Dimensional Device Structures	Sturm
2:35	Break	
3:00	New Compound Semiconductor Devices	Kroemer
3:30	Characterization and Modeling of GaAs/MODFETs	Yeager
3:50	Picosecond Time Domain Device Characterization	Eisenstadt
4:10	On-Chip Capacitance Characterization with Femtofarad Resolution	Oristian
4:30	Parameter Extraction and the Development of SPICE Models	Ward

INTEGRATED CIRCUITS MANUFACTURING SCIENCE

Wednesday, August 22, 1984

8:30 a.m.	A Framework for Equipment Automation	Golovin
9:10	The Users Viewpoint of Computerized IC Fabrication	Christie
9:50	Break	
10:15	The FABLE Language	Reid
11:00	Process Diagnostics and Adaptive Control of IC Fabrication	Strojwas
11:30	Diagnostics an Equipment Control	Murakami
12:00	Lunch	
1:15 p.m.	Equipment Interface Standards	Clare
1:50	Equipment Reliability and Particle Contamination in Manufacturing	Lane
2:20	Break	
2:40	Control of Plasma Etching for VLSI	McVittie
3:10	Process Control of Ion Implantation in Production	Current
3:40	Interfacing and Data Collection for Stepper Lithography	Fu
4:10	Discussion	

General Information

How to enroll: Enrollment is limited and advance enrollment is required. Enrollment may be made by individuals or companies. Deadline for submission of enrollment forms, August 10, 1984.

To enroll: Please complete and return the form provides.

Refunds: If you enroll and then cannot attend, a refund will be granted if requested in writing prior to August 10, 1984.

Housing is available on the Stanford campus in student residences without private baths at reasonable rates. Campus recreational facilities are available for your use. For further information contact the Conference Office at 123 Encina Commons, Stanford, California 94305; telephone (415) 497-3126.

For further information: Write or call Stanford University Integrated Circuits Laboratory, c/o Robert W. Dutton, AEL Bldg., Stanford, California 94305; telephones (415) 497-1349 and 497-4138.

(Enrollment is limited. Advance enrollment is required.)

I enclose a check in the amount of $ ________ to cover ______ enrollment(s) in (check one)

☐ Processing Technology August 20, 1984 ($225)*
☐ Simulation and Applications August 21, 1984 ($225)*
☐ Manufacturing Science August 22, 1984 ($225)*
☐ Entire Program August 20-22, 1984 ($575)*

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Make check payable to Stanford University, and send to Robert W. Dutton, 204 AEL Building, Stanford University, Stanford, CA 94305.

*Preferred-rate registrations for government employees will be accepted based on written sponsor approval. Contact Sven Roosild (Defense Advanced Research Projects Agency) or Bill Sander (U.S. Army Research Office).

CAD and Manufacturing of IC

August 20-22, 1984

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Sheldon Aronowitz	Fairchild
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Nirmal Ratnakumar	Precision Monolithics
Thomas A. Reilly	Lafayette College
James Reynolds	Naval Avionics
Paul Reynolds	Burroughs Corporatio
Llanda Richardson	DEC
Stephen P. Robb	Motorola Semi.
Bernie Rogers	Monolithic Memories
Brian Sadler	Trilogy Systems
Maah Sango	Monolithic Memories
K. G. Schlotzhauer	Bipolar Integ. Tech
Mark Schoenberg	Motorola, Inc.
Steve Schwake	Telmos
Jerold A. Seitchik	Texas Inst.
Nagib Sharif	Synertek
Steven Shatas	AG Associates
Bok Shin	Siemens/Opto
James Shipley	National Semi.
Ritu Shrivastava	Cypress Semi. Corp.
Paramjit Singh	Rockwell Intl.
Barry S. Signoretti	Memorex Corp.
Byron Siu	Intel
Cezary Slaby	Northern Telecom Ele
Peter Smith	Fairchild
R. Kent Smith	AT&T Lab
Skip Smith	National Semi.

Richard Smolen	National Semi.
Ralph J. Sokel	Inmos Corp.
Gianpaolo Spadini	VTI
Edmund J. Sprogis	IBM
Jake Steigerwalt	National Semi.
Dale Sumida	Xerox Corp.
S. C. Sun	Xicor
Jeffrey P. Sung	AMD
Won G. Sunu	Gould Inc.
William A. Surber	Princeton Univ.
Harry E. Talley	Univ. of Kansas
Tankaj Tandon	American Microsystems, Inc.
Sing Pin Tay	Northern Telecom Electronics
David Thornhill	Science Applications
Tim J. Thurgate	TMA
Rebecca Tang	National Semi.
Farid M. Tranjan	Texas Instruments
Huan-chung Tseng	National Semi.
Stanley Tseng	Modern Electrosystems
David Tsuei	Intersil
John R. Tuttle	Unitrode Corp.
Lowrey Tyler	Micron Technology
Vance Tyree	USC Infor.Sciences Inst.
John T. Urbain	Floating Point Systems
Rimantas L. Vaitkus	Motorola
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Ray Vasquez	Motorola
Robert H. Vogel	Lehigh University
George P. Walker	Synertek
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Douglas J. Welter	Motorola Bipolar IC
Moo Y. Wen	IBM
Ralph Whitten	Monolithic Memories
Deborah Witek	Digital Equipment Corp.
Gerald L. Witt	AFOSR
Richard C. Woodbury	Brigham Young Univ.
Richard Woodruff	UTMC
Tze-Kwai Wong	Advanced Micro Devices
E. Gordon Wright	Synertek
In-nan Wu	Fairchild Research Center
Way-Chen Wu	Signetics
Howard Yamamoto	Matsushita Elect. Works
Cheng Yang	Commodore
Jeff T. Yang	Memorex
Abe F. Yee	LSI Logic
Hamza Yilmaz	General Electric Co.
Roger Yin	Siliconix, Inc.
Shinmei Yoshihiko	Matsushita Elect. Works
Raymond Yu	Intel
Sepuan Yu	GE CR&D
Michael Yung	Commodore

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Michael Harrison
Mark Horowitz
Ted Kamins
Jim Kesperis
Paul Losleben
Jim Meindl
Reda Razouk
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Sven Roosild
Bruce Wooley

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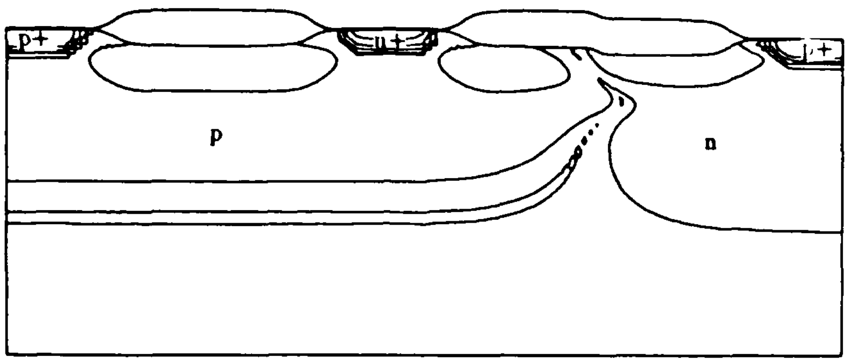
Alex Harwit
Eric Hellman
Stephanie Koch
Les Landsberger
David Liu
Phil Pitner
Ed Wollak
Gideon Yoffe
Kanji Yoh
Ed Young

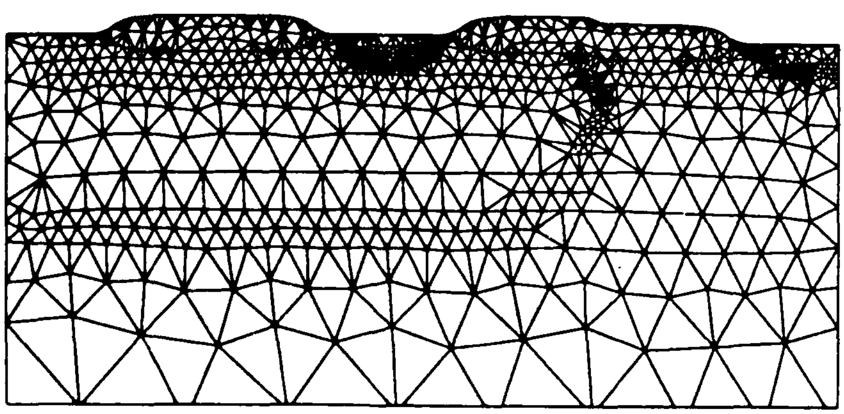
Stanford University Announces a Two-Day Program

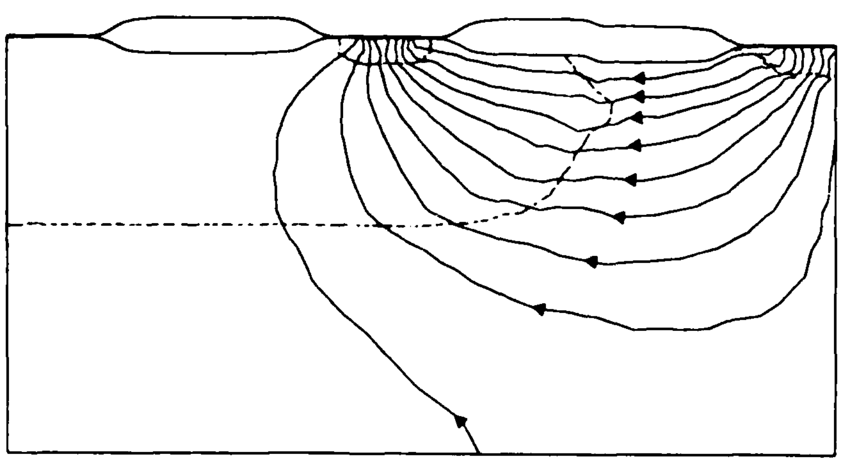
COMPUTER-AIDED DESIGN OF IC FABRICATION PROCESSES

Technology Modeling
Thursday, August 1, 1985

Process and Device Simulation
Friday, August 2, 1985







COMPUTER-AIDED DESIGN OF IC FABRICATION PROCESSES

A two-day program:
August 1-2, 1985 Stanford, California

The evolution of Integrated Circuit technology has resulted in three decades of explosive growth in microelectronics.[1] For two decades Stanford has been a leader in the field of research and teaching of microelectronics. This year marks the tenth anniversary of Stanford's efforts in process modeling. The highlight of this year's program is the discussion of new 2D process kinetic models and the launching of our first fully 2D version of the SUPREM program. In addition to the 2D work in silicon technology, this year marks the formal beginning of our efforts to model compound materials and devices. This two day meeting is intended to provide the participants with in-depth discussions of process and device modeling topics—both for silicon and GaAs technologies. The evolution towards larger wafers for silicon technology has introduced new requirements for process and equipment technologies. In addition to the concerns with two-dimensional implantation, diffusion and oxidation, new efforts in transient processing and plasma etching kinetics are introduced at this meeting. The maturing of the GaAs technology is now reflected in our growing efforts to build quantitative process models for compound materials. In the first day of the conference the emphasis is given to technology, kinetic models and data needed to support the evolution of SUPREM.

The second day of the conference shifts the emphasis to Computer Aided Design (CAD) tools and their applications. As stated earlier, the next generation of process modeling, a full 2D simulator—SUPREM IV—is introduced and discussed. The continued refinement of the 1D tool, version III, is considered. As in the past, we encourage discussion and participation on these topics. The device modeling efforts will reflect three theme areas—MOSFET, Bipolar, and Compound Materials. The PISCES program continues to show stellar performance in a multitude of applications in all three areas. In the discussion of bipolar devices both poly emitter silicon and heterojunction GaAs technologies are considered. The SEDAN III program will be released for the first time with new capabilities to model silicon, III-V and II-VI device structures. Finally, the discussion of MESFET and HFET structures in GaAs will show the state-of-the-art in technology and device modeling.

The meeting format will consist of a series of lectures as outlined in the program. Copies of material presented by the speakers are included in the course materials. In addition, there will be a distribution of technical reports which give an extended discussion of background information and details of the experiments, models, and computer programs. The first day will involve primarily lectures and discussions of the materials aspects of technology modeling with substantial emphasis on specific experimental and model results applicable to SUPREM. The second day will focus on more general aspects of process and device simulation as well as Stanford-developed tools.

A "forum" atmosphere will be encouraged to obtain user feedback. A number of specific applications and results (case studies) will be presented. The registration fee provides for all course materials, as well as lunches and dinner.

Location: Terman Auditorium, Stanford University, Stanford, California.

Fee: The fee for each day is $250 (including lecture notes, luncheon, and dinner (August 1-2, 1985) or $475 for attending both days. Enrollment is limited, and advance enrollment is required.

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[1] This work has been supported through government as well as industrial funding. The Defense Advanced Projects Research Agency, Army Research Office, and Semiconductor Research Corporation are specifically responsible for major sources of research funding.

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ZHIPING YU, Research Assistant, Stanford University

PROCESSING TECHNOLOGY

Thursday, August 1, 1985

8:00 a.m.	Registration	
8:30	Silicon Overview	Plummer
	Silicon Bulk Phenomena	
9:15	2D Diffusion	Griffin
9:45	Gettering Modeling Bronner	
10:10	Rapid Thermal Annealing	Reed
10:35	Break	
10:55	2D Implantation	Giles
11:20	Laser Doping for Shallow Junctions	Carey
	Interfaces and Thin Films	
11:40	TEM Studies of Interfaces	Bravman
12:00	Lunch	
1:15 p.m.	Selective CVD, Contacts and Interconnects	Saraswat
1:40	Silicide/Silicon Structures	Shone
2:00	Plasma Etching	McVittie
2:25	2D Oxidation	Kao
2:50	Break	
	GaAs Process Modeling	
3:10	GaAs Technology, Doping and Diffusion	Sigmon
3:40	GaAs Schottky Diodes and Contacts	Helms
4:05	GaAs MBE	Harris
4:30	Discussion	Plummer/Dutton

PROCESS AND DEVICE SIMULATION

Friday, August 2, 1985
Silicon Process and Device Simulation

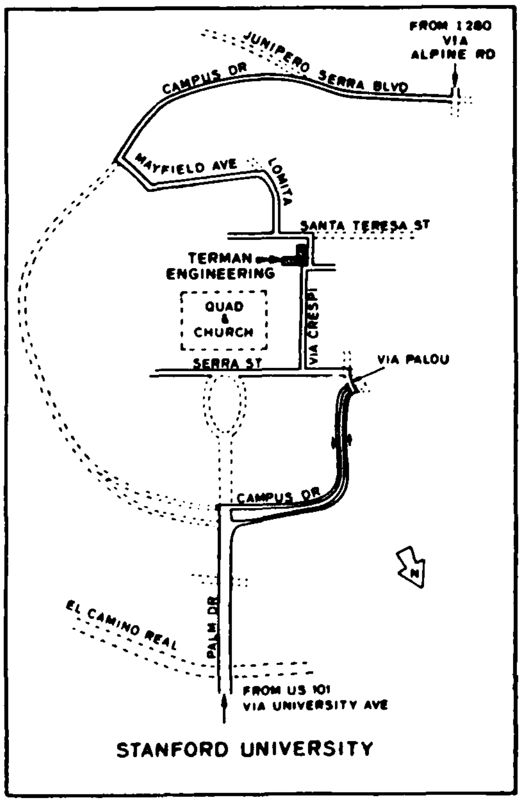
8:00 a.m.	Overview of Process and Device CAD	Dutton
8:40	SUPREM III—Status Report	Hansen
9:10	Simulating Dynamic Process Geometry	Rafferty
9:40	Applications of SUPREM IV for Diffusion	Law
10:10	Break	

MOSFET Technology and Scaling

10:30	PISCES for Transient Device Simulation, Including CMOS Latchup	Pinto
11:20	Capacitance Measurements and Modeling	Oristian
11:40	Hot Carrier Effects—Models and Measurements	Henning
12:00	Lunch	

Technology and Modeling Tools for High Frequencies—
Silicon vs. Compound Materials

1:00 p.m.	GaAs MESFET Charge and Mobility Models	Shenai
1:30	GaAs (heterojunction) HFET—Device and Circuit Models	Yeager
2:05	GaAs (heterojunction) HBJT—Technology and Device Design	Pitner
2:40	Break	
3:00	Technology and Modeling of Polysilicon Emitter Bipolar Devices	Patton
3:30	2D Scaling of Silicon Bipolar Devices	Crabbé
4:00	SEDAN III—A Simulator for Arbitrary Multilayer Bipolar Structures	Yu
4:30	Discussion and Conclusion	



General Information

How to enroll: Enrollment is limited and advance enrollment is required. Enrollment may be made by individuals or companies. Deadline for submission of enrollment forms: July 26, 1985

To enroll: Please complete and return the form provided.

Refunds: If you enroll and then cannot attend, a refund will be granted if requested in writing prior to July 26, 1985

Housing is available on the Stanford campus in student residences without private baths at reasonable rates. Campus recreational facilities are available for your use. For further information contact the Conference Office at 123 Encina Commons, Stanford, California 94305; telephone (415) 497-3126

For further information: Write or call Stanford University Integrated Circuits Laboratory, c/o Robert W. Dutton, AEL Bldg., Stanford, California 94305, telephones (415) 497-1349 and 497-4138.

(Enrollment is limited. Advance enrollment is required.)

I enclose a check in the amount of $ ________ to cover ____ enrollment(s) in (check one)

☐ Processing Technology August 1, 1985 ($250)*
☐ Simulation and Applications August 2, 1985 ($250)*
☐ Both ($475)*

Name ______________________________
last first middle

Employed by ______________________________

Company address ______________________________

____
city state zip

Daytime telephone and extension ______________________________

Make check payable to Stanford University, and send to Robert W. Dutton, 204 AEL Building, Stanford University, Stanford, CA 94305.

*Preferred-rate registrations for government employees will be accepted based on sponsor approval. Contact Robert W. Dutton, Stanford University.

CAD of IC FABRICATION PROCESSES

August 1-2, 1985

Aftab Ahmad	Honeywell, Inc
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D. Dean Casey	GTE Labs
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Jun-Wei Chen	National Semiconductor
Kuang-Yu Chen	Integrated Device Tech
Min-Liang Chen	AT&T Bell Labs
Sung-Ming Chen	Tristar Semiconductor
Micheal Chern	Commodore
Yu-Tai Chia	Sierra Semiconductor
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Roy A. Colclaser	Signetics
Thomas W. Collins	Tandem Computers
John L. D'Arcy	AT&T Bell Labs
Marvin E. Daniel	MCC
Jan L. De Jong	Signetics
Bruce Deal	Fairchild
John A. Detrio	Univ. of Dayton Research Inst
Carl F. Diegert	Sandia
Anant Dixit	Silicon Systems
Dimitri Dokos	Sperry
Ray Donald	Signetics
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Kuni Fukumuro	Xilinx
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Michael C. Garner	Intel
Layne Gehrig	Eaton Corp
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Daniel L. Gerlach	AT&T Bell Labs
Deepak Goel	Ford Microelectronics
Wayne Grabowski	Hughes Aircraft

Jefferey L. Gray	Purdue University
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Rod Harrell	Department of Defense
Kim G. Hellwell	Analog Design Tools
Robert H. Hobbs	United Tech. Res. Center
Richard R. Hoffmeister	NCR Microelectronics
Daniel Hou	Microwave Associates
C. Ming Hsieh	IBM Corp
Daniel Hou	
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Amolak Ramde	Advanced Micro Devices
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Reda Razouk	Fairchild
Llanda Richardson	Digital Equipment Corp
Stephen P Robb	Motorola Inc.
Frederick C Rock	GTE Labs
J G Rollins	Aerospace Corp
Sven Roosild	DARPA
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Robert J Schuelke	GigaBit Logic
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Fred Sexton	Sandia National Lab
Steven Shatas	AG Associates
Alex Shaw	Nikon Precision
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Yoshihiko Shimmei	Matsushita Electric
Yun Sung Shin	Tristar Semiconductor
Howard Shoemaker	TRW, Inc.
Pritpal Singh	Villanova University
Jim Sizemore	Northern Telecom
Cezary Slaby	Northern Telecom
Peter R Smith	Fairchild
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Tom Springett	Intel Corp
Jake Steigerwald	National Semiconductor
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Tim Thurgate	Technology Modeling Associates
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Huan-Chung Tseng	Signetics Corp
Gu-Fung Tsuei	Intersil
Thye-Lai Tung	MIT
Robert M Turfler	Mission Research Corp
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Jan Vanderlinde	Siliconix
Kody Varahramyan	IBM
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Perry Wallia	Honeywell
Ching-Yeu Wei	General Electric
Robert Wixted	MIT Lincoln Labs
Neil Wylie	Fairchild Semicondu
Karl W Wyatt	AT&T Bell Labs
Cary Y Yang	University of Santa C

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Gary Bronner	Stanford University
Paul Carey	Stanford University
Emmanuel F Crabbe	Stanford University
Bob Dutton	Stanford University
Martin Giles	AT&T Bell Labs
Peter Griffin	Stanford University
Stephen Hansen	Stanford University
Jim Harris	Stanford University
Bob Helms	Stanford University
Al Henning	Stanford University
Dah-Bin Kao	Stanford University
Mark Law	Stanford University
Jim McVittie	Stanford University
John Oristian	Stanford University
Gary Patton	Stanford University
Mark Pinto	Stanford University
Phil Pitner	Stanford University
Jim Plummer	Stanford University
Conor Rafferty	Stanford University
Mike Reed	Stanford University
Krishna Saraswat	Stanford University
Krishna Shenai	Stanford University
Fu-chia Shone	Stanford University
Tom Sigmon	Stanford University
Andrzej Strojwas	Carnegie-Mellon Univer
Hal Yeager	Stanford University
Zhiping Yu	Stanford University

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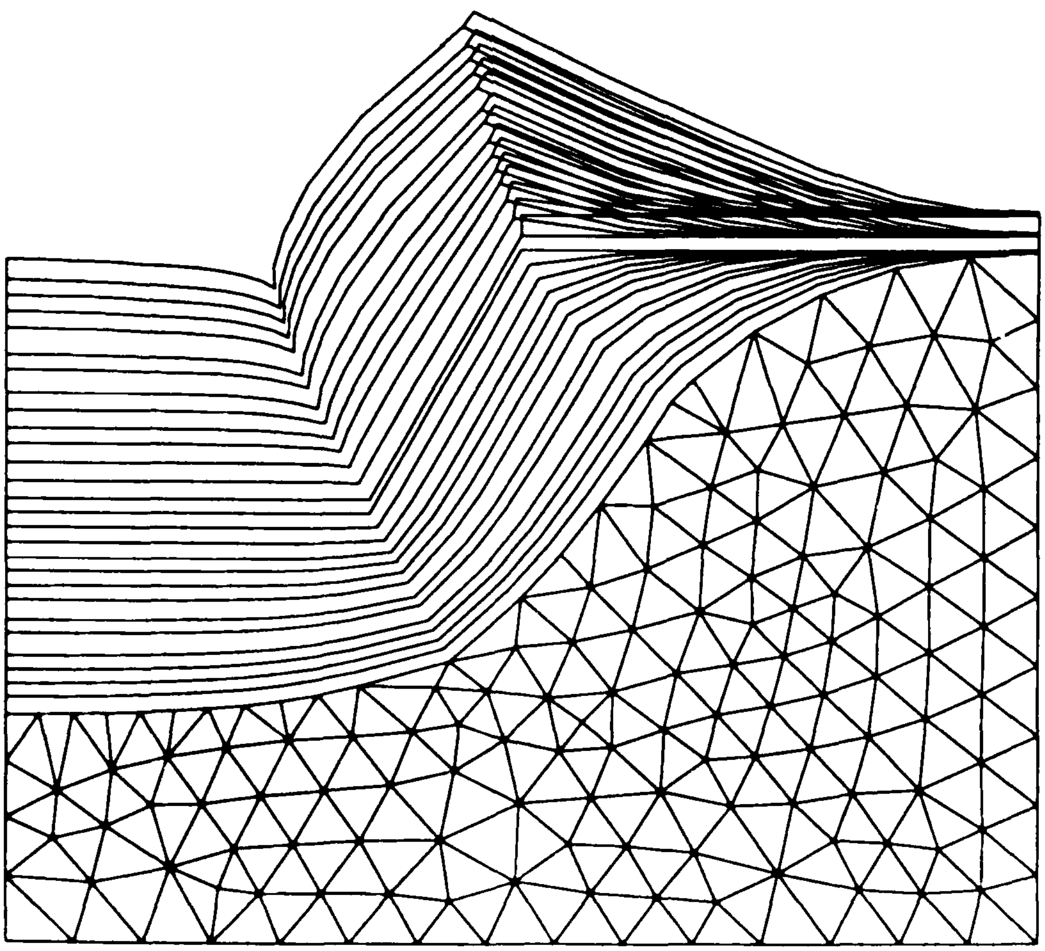
Sung-Tae Ahn	Stanford
Cynthia Bloom	TMA
Bruce Deal	Fairchild
Reda Razouk	Fairchild
Michael Kump	TMA
Les Landsberger	Stanford
Bob Pack	TMA
Reda Razouk	Fairchild
Lester Roberts	Stanford
Andrew Steckl	RPI
Jim Sturm	Stanford
Ed Young	Stanford

Stanford University Announces a Two-Day Program

COMPUTER-AIDED DESIGN OF IC FABRICATION PROCESSES

Technology Modeling
Wednesday, August 27, 1986

Process and Device Simulation
Thursday, August 28, 1986



COMPUTER-AIDED DESIGN OF IC FABRICATION PROCESSES

A two-day program
August 27-28, 1986, Stanford, California

The past several decades have witnessed an explosive growth in microelectronics.[1] During that time, Stanford has contributed broadly to device and process technology—both in silicon and compound materials. During the last decade, Stanford's development of Technology Computer Aids for Design (TCAD) have been of major benefit to the electronics industry. Stanford developed programs such as SUPREM, SEDAN, PISCES, and SUXES have become mainstays of TCAD in universities, government, and industry. This year's program highlights major accomplishments in silicon and GaAs technologies—both in terms of physical processes/understanding and TCAD tools to leverage design applications.

The first day of the conference gives emphasis to technology, kinetic models, and the data needed to support the evolution of SUPREM. A major highlight this year is the release of SUPREM IV for 2D process modeling. During the first day the discussion gives particular attention to 2D kinetic models. The growing importance of GaAs is reflected in several talks on technology and modeling. In particular the roadmap for SUPREM 3.5 will indicate Stanford's long-term goals related to GaAs process modeling.

The second day will shift the emphasis to TCAD tools and their application. Details of the first release version of SUPREM IV will be given. The continuing efforts to upgrade the 1D tools, SUPREM III and SEDAN III, will be discussed. In the area of device modeling the topics CMOS technology and hot carrier effects are emphasized for silicon. In the GaAs area, the extension of both SEDAN and PISCES for non-equilibrium carrier transport are discussed. In addition, the topic of SPICE modeling for GaAs FET devices will be covered.

The meeting will consist of a series of lectures as outlined in the program, and copies of material presented by the speakers are included. In addition, there will be a distribution of technical reports which give an extended discussion of background information and details of the experiments, models, and computer programs. The first day will include lectures and discussions of the materials aspects of technology modeling with substantial emphasis on specific experimental and model results applicable to SUPREM. The second day will focus on more general aspects of process and device simulation as well as Stanford-developed tools.

A "forum" atmosphere will be encouraged to obtain user feedback. A number of specific applications and results (case studies) will be presented. The registration fee provides for all course materials, plus lunches and dinner.

Location: Terman Auditorium, Stanford University, Stanford, California.

Fee: The fee for each day is $275 (including lecture notes, luncheon, and dinner (August 27, 1986) or $500 for attending both days. Enrollment is limited, and advance reservations are required.

---

[1]This work has been supported through government and industrial funding. The Defense Advanced Projects Research Agency, Department of Defense VHSIC Program, Army Research Office, and Semiconductor Research Corporation are specifically responsible for major sources of research funding.

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PROCESSING TECHNOLOGY

Wednesday, August 27, 1986

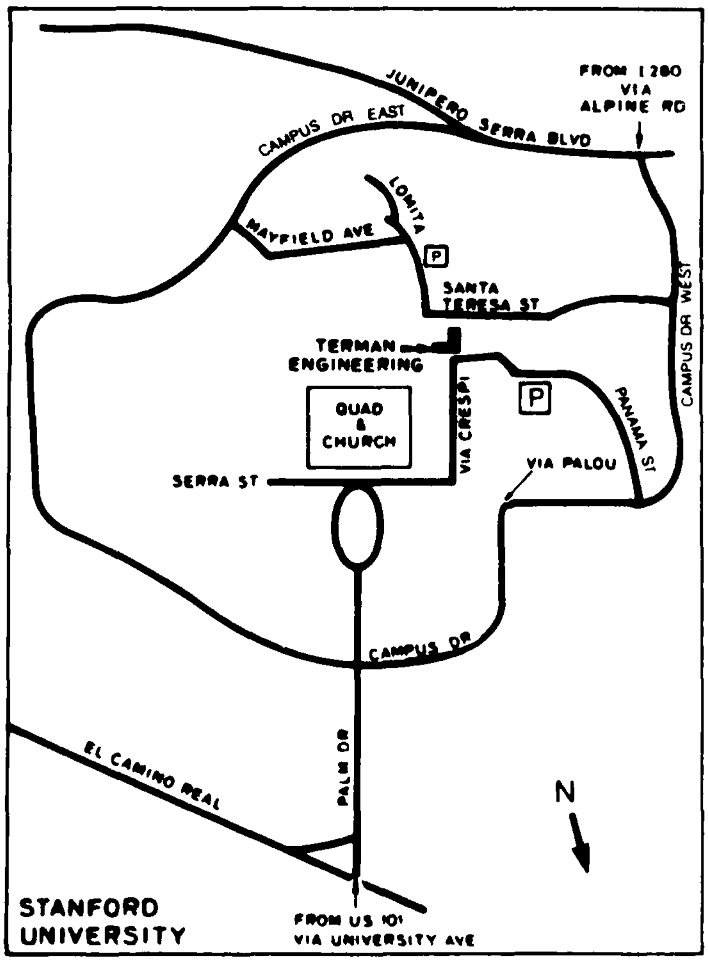
8:00 a.m.	Registration	
	Silicon Technology	
8:30	Silicon Overview	Plummer
9:15	2D Diffusion	Griffin
9:40	Diffusion in SOI Structures	Fahey
10:05	Thin Film Diffusion Studies	Ahn
10:30	Break	
10:50	Diffusion in Insulators	Fishbein
11:15	2D Oxidation	Kao
11:35	Transmission Electron Microscopy	Bravman
12:00	Luncheon	
	Generic (Silicon and GaAs)	
1:15 p.m.	Limited Reaction Processing	Gibbons
1:40	Silicides	Saraswat
2:05	Plasma Etching	McVittie
2:30	Break	
	GaAs Technology	
2:45	SUPREM 3.5 (for GaAs)	Deal
3:15	Ion Implantation/RTA in GaAs	Sigmon
3:40	Contact Technology	Helms
4:05	Molecular Beam Epitaxy	Harris
4:30	Discussion	Plummer/Dutton

PROCESS AND DEVICE SIMULATION

Thursday, August 28, 1986

Silicon Process and Device Simulation

8:30 a.m.	Introduction to CAD Tools	Dutton
9:15	SUPREM III Update	Hansen
9:40	SEDAN III Update	Yu
10:05	RSM Applied to Coupled Process and Device Simulation	Alvarez
10:30	Break	
10:50	SUPREM IV—Program Structure and 2D Diffusion	Law
11:15	SUPREM IV—Grid and 2D Oxidation	Rafferty
11:40	CMOS Latchup	Pinto
12:05	Luncheon	
1:00	Optimized CMOS at LN_2	Watt
1:25	Hot Carriers in Silicon	Henning
1:50	Gate Current in Submicron NMOS	Sangiorgi
2:15	Break	
2:35	Heterojunction GaAs FET Modeling	Yeager
3:00	Monte Carlo Device Analysis	Hwang
3:25	Polysilicon Bipolar Emitters	Patton
3:50	Boron Diffusion in Polysilicon	Ghannam
4:10	Phosphorus Predeposition Model	Shimmel
4:30	Discussion and User Participation	Dutton



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CAD of IC Fabrication Processes

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