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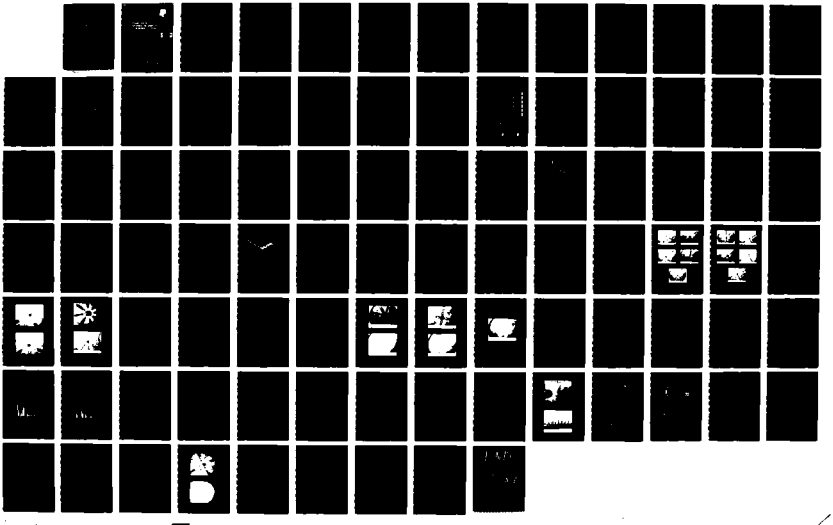

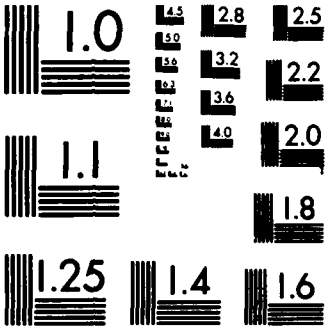

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Final Technical Report
April 1987

EPITAXIAL REACTOR DEVELOPMENT FOR GROWTH OF SILICON-ON-INSULATOR DEVICES

Clemson University

D. J. Dumin

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A hydride vapor phase epitaxy system was designed and constructed for testing boron phosphide as the insulator for a silicon on insulator material study. Layer structures grown were tested for electrical properties and thickness. Silicon deposited on the boron phosphide was of good quality, but not as good as bulk silicon. There was some diffusion of boron and phosphorus into the silicon.

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Table of Contents

Table of Contents Con't

List of Figures

List of Figures Con't

Figure Page

List of Tables

Preface

This final report prepared by Clemson University under Contract No. F19628-85-K-0013 describes research performed in the Department of Electrical and Computer Engineering, Dr. A. Wayne Bennett, Department Head.

The principal investigator was Dr. David J. Dumin, Samuel R. Rhodes, Professor of Electrical Engineering. Mr. Perry J. Robertson was the graduate student working on the project. Parts for the initial epitaxial reactors used in this work were provided by Dr. Marty Peckerar of the Naval Research Labs and Mr. Tom Potts of Eagle-Picher Co. Transistors were fabricated on films of silicon grown on boron phosphide grown on silicon under the supervision of Dr. Gary Carver of the National Bureau of Standards. Measurement of MOS transistor characteristics were performed by Michael Freytag. Facilities for epitaxial reactor were provided by Dr. Cliff Fain and the Ceramic Engineering Department, Clemson University. The assistance provided by these engineers is acknowledged and greatly appreciated.

Abstract

An epitaxial reactor was constructed to investigate novel multilayer silicon-on-insulator structures. Boron phosphide (BP) has been investigated for use as a high resistivity layer on which single crystal silicon may be grown. The characteristics of the BP and silicon layers were found. Changes induced in the BP layer following heating were examined. It was shown that high resistivity ($\approx 10^6$ Ω-cm) BP may be grown on silicon without heat treatments by varying process parameters. MOS devices were manufactured on 1-5 μm n-type silicon layers on BP to electrically characterize the epitaxial silicon layers. Electron channeling patterns indicating high quality crystal growth are presented for both silicon and BP layers. Transistors on silicon layers thinner than 3.0 μm did not operate properly due to high background doping concentrations. The best transistor characteristics were on the 5 μm layers. Results are presented for SOS films grown at high growth rates and high temperatures. Novel Si-BP-SOS films were grown. Results from attempts to grow single crystal silicon dioxide on silicon by the pyrolytic decomposition of silane with water vapor are presented. Silicon substrates were oxidized below 1100°C before single crystal growth could begin. No growth appeared above 1100°C. Techniques for in situ epitaxial film thickness measurement have been discussed.

SECTION I

Introduction

In the past several years the interest in silicon-insulator multilayer structures has been growing. Much of the interest has been concentrated in silicon-on-sapphire (SOS) but other techniques and materials have begun to attract interest. Oxygen implanted buried layers of silicon oxide for SIMOX material looks particularly promising [1]. Recently it has been demonstrated that it is possible to grow boron phosphide (BP) on silicon and silicon on boron phosphide on silicon [2]. This material combination has been used to grow up to five layers of silicon on boron phosphide on silicon substrates and two layers on SOS substrates. PMOS ICs have been fabricated on these multilayers [3]. These ICs had properties similar to those obtained on SOS material.

Since most of the BP work has been done in Japan, it was decided to build an epitaxial reactor at Clemson University and attempt to duplicate the rudimentaries of the work done in Japan on BP. Much of the work done on BP has concentrated on the growth of a high resistivity BP layer. Since boron phosphide is not the ideal material for an SOI application due to the possibility of autodoping of the silicon by either the boron and/or the phosphorus, it was decided to design a reactor that would be capable of growth of other, more benign, insulators, such as silicon carbide, silicon nitride, and silicon dioxide.

An epitaxial reactor was designed and built at Clemson University. This reactor has been used to grow multiple layers of silicon and boron phosphide on silicon and on silicon-on-sapphire.

It has also been used to grow silicon-on-sapphire films and has the capability of growing silicon carbide and silicon nitride. Attempts to grow single crystal silicon oxide by reacting water vapor and silane have been made. Preliminary attempts to grow silicon dioxide have resulted in film growth, however, the film composition is not yet known.

SECTION II

Reactor Design and Construction

The first priority of this project was the design and construction of the epitaxial reactor to be used to grow the films. The reactor consisted of the gas cabinet, reactor chamber, the gas flow system, the temperature monitor system, and the exhaust system. The wafers were heated by reactive coupling of a graphite susceptor to an rf generator operating at 10 kHz. The rf coils were mounted outside of the quartz growth chamber. A gas cabinet was designed and constructed to house all of the reactor plumbing except the exhaust system. The various parts of the epitaxial reactor will be described in detail.

Gas Cabinet

The epitaxial reactor was constructed with the aim of growing various heteroepitaxial insulator/conductor structures. The reactor consisted of a gas cabinet which contained the epitaxial gases (B_2H_6-H_2, SiH_4-H_2, PH_3-H_2, C_2H_6-H_2, HCl, H_2O-H_2), regulators, flow meters, valves and plumbing, water-cooled quartz chamber, rf coil and infrared pyrometer. Purified hydrogen and nitrogen were supplied externally to the gas cabinet. Hydrogen was purified by passing it through a palladium diffusion cell. Nitrogen was passed through a catalytic gas dryer before entering the cabinet.

A diagram of the gas cabinet appears in Figure 1. The gas cabinet was constructed from steel shelving supports six feet long, two feet deep and 5-1/2 feet tall with a plywood top and bottom.

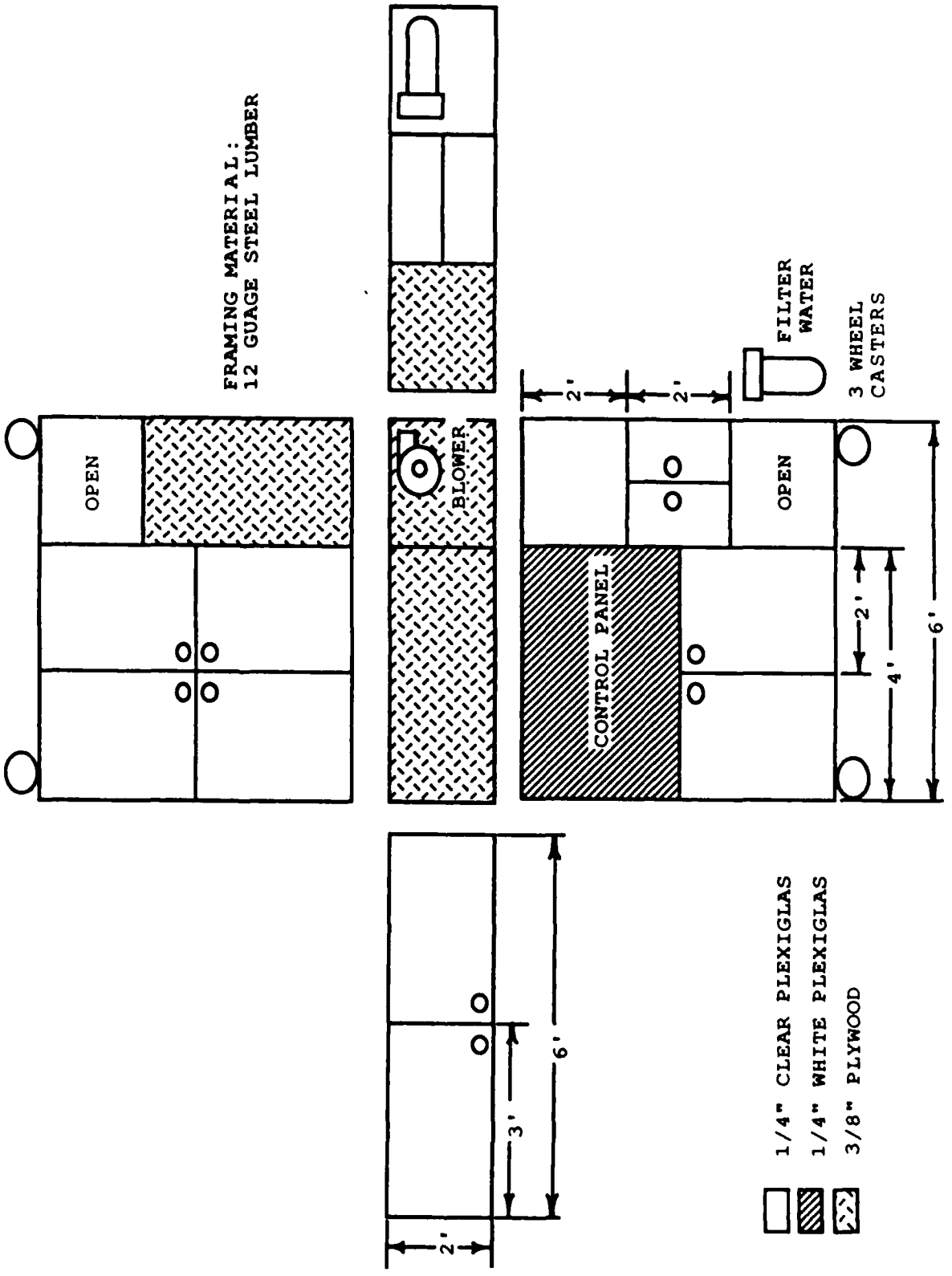


Figure 1. Diagram of the Gas Cabinet. The frame of the cabinet was constructed of steel shelving materials.

The cabinet rested upon four casters. It was completely enclosed by 1/4 inch thick clear plexiglas doors that allowed complete access to the interior of the cabinet. A control panel was mounted on a three by four foot piece of white plexiglas. All valves and flow meters were located on the control panel. These valves and flow meters were mounted in such a way as to provide easy comprehension and control of the flow and mixing of gases entering the quartz chamber.

Reactor Chamber

The interior of the gas cabinet was divided into two sections. The gas bottles were located on the left side of the cabinet behind the control panel. Each gas had a regulator which controlled the delivery pressure to individual flow meters mounted on the panel. Each regulator was equipped with a purge line which allowed for the flushing of each regulator and flow meter with nitrogen following a run.

The water-cooled vertical quartz chamber was mounted in the right side of the gas cabinet. Gas was provided from the mixing chamber through a six inch long, 1/4 inch diameter flexible stainless steel tube at the top of the quartz chamber. Hot exhaust gases were removed from the bottom of the quartz chamber through a 12 inch long, 1/4 inch diameter flexible stainless steel tube. The rf generator coil entered through the back of the cabinet and surrounded the quartz reactor chamber.

A blower was mounted to the roof of the cabinet above the quartz tube to exhaust any gases that might be leaked into the room. Folding clear plexiglas doors provided access to the quartz

tube from the front and right sides of the cabinet.

It was decided to use a vertical chamber with the wafer mounted perpendicular to the flow of the gas. Initially an air cooled single walled reactor was used. However, excessive gas phase decomposition of the reactor gases, contamination of the reactor walls, and the slow cycle time of the air cooled reactor indicated that a double walled, water cooled reactor would be preferable. Early runs of BP were plagued by the leaking of phosphine into the lab from the joint which connects the exhaust line and quartz cap. This problem led to the placement of a plastic shroud over the joint and a blower which would suck the unwanted exhaust out of the lab. It was concluded that the leaking was coming from a bad weld in the 1/2 inch flexible stainless steel tubing used in the exhaust line. A combination of Swagelok and Ultratorr fittings finally provided a leak-tight, quick disconnect joint which allowed for the easy removal of the cap and pedestal from the tube. The final configuration of water cooled quartz reactor with quick disconnect fittings proved to be a good design for all types of epitaxial work. A sketch of the final reactor design is shown in Figure 2.

The vertical water cooled fused quartz chamber had an inside diameter of three inches and is capable of handling up to 2" diameter wafers. The reactor chamber consisted of two parts, the vertical tube and wafer pedestal and cap. The vertical chamber was 20 inches in length with a 12 inch long water jacket. A clear, polished, fused quartz window was installed in the top of the tube to allow direct temperature measurement of the surface of the wafer via an infrared pyrometer. The susceptor and wafer were supported

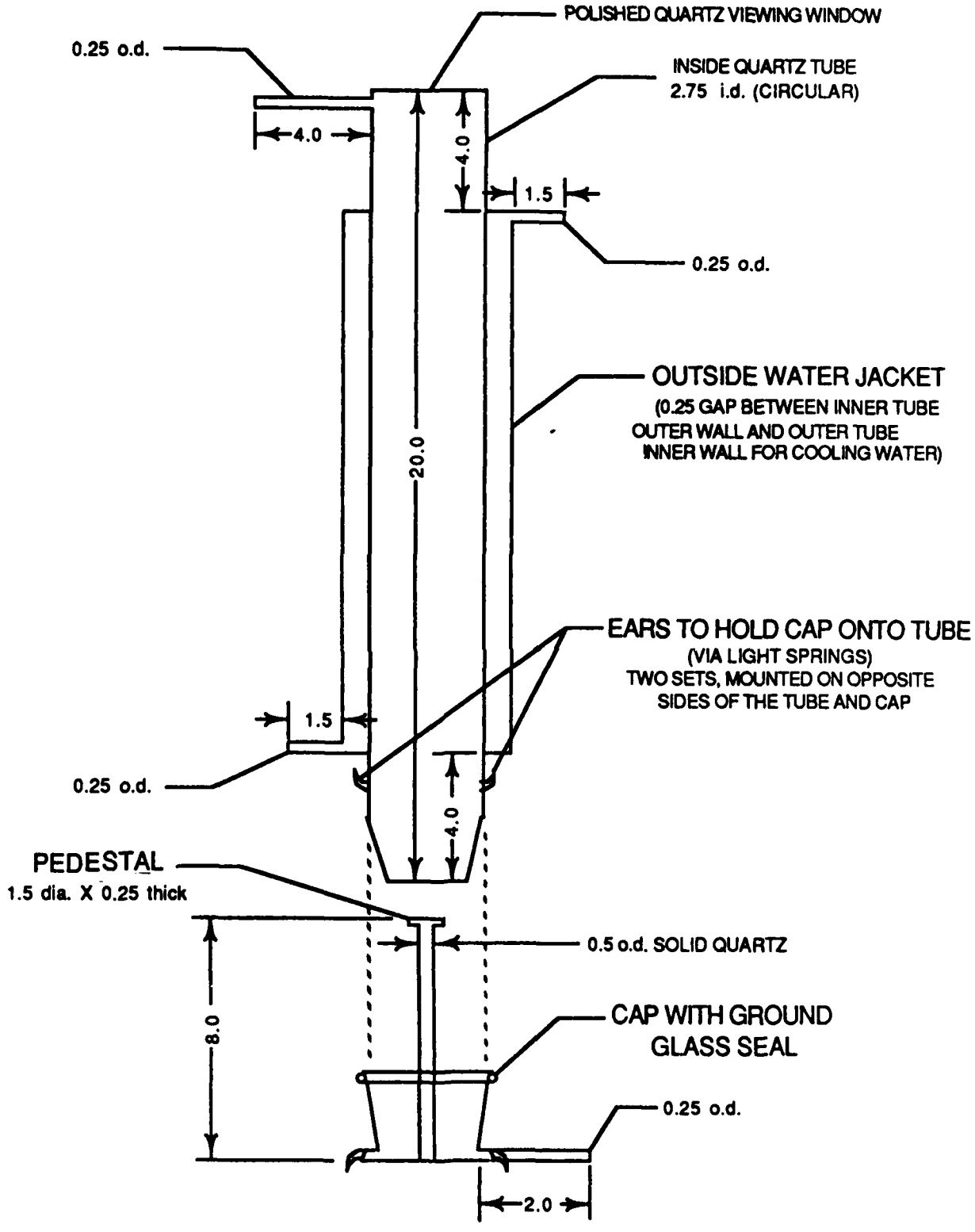


Figure 2. Quartz Epitaxial Reactor Tube. The susceptor is positioned horizontally in the center of the chamber by a fused quartz pedestal.

on a pedestal which was attached to the center of the base of the cap. Gas entered the chamber via a 1/4 inch outside diameter tube at the top edge of the reactor and exited through a 1/4 inch tube mounted in the side of the cap. Quartz hooks were fabricated onto the tube and cap so that the cap may be held onto the tube by two lightweight springs. A ground glass joint was provided to join the cap and tube opening. Silicon vacuum grease was applied to the ground glass joint to eliminate back diffusion of oxygen into the chamber and ease the removal of the cap.

Susceptors

Several different silicon carbide coated graphite susceptors were used in this project. They were all 2-1/4 inches outside diameter with varying thicknesses from 1/4 to 1 inch as shown in Figure 3. Separate susceptors were used for growing BP, SOS, silicon-on-BP, and SiO_2-on-silicon in order to reduce cross-contamination between processes. A shallow depression was machined into the top of the susceptor to keep the wafer from sliding off the susceptor during processing. A slightly deeper and smaller diameter depression was cut into the bottom of the susceptor to center the susceptor on the quartz pedestal. The diameter of this depression is large enough to prevent binding during heating due to differences in coefficients of expansion of graphite and fused quartz and to allow leeway for the centering of the susceptor when

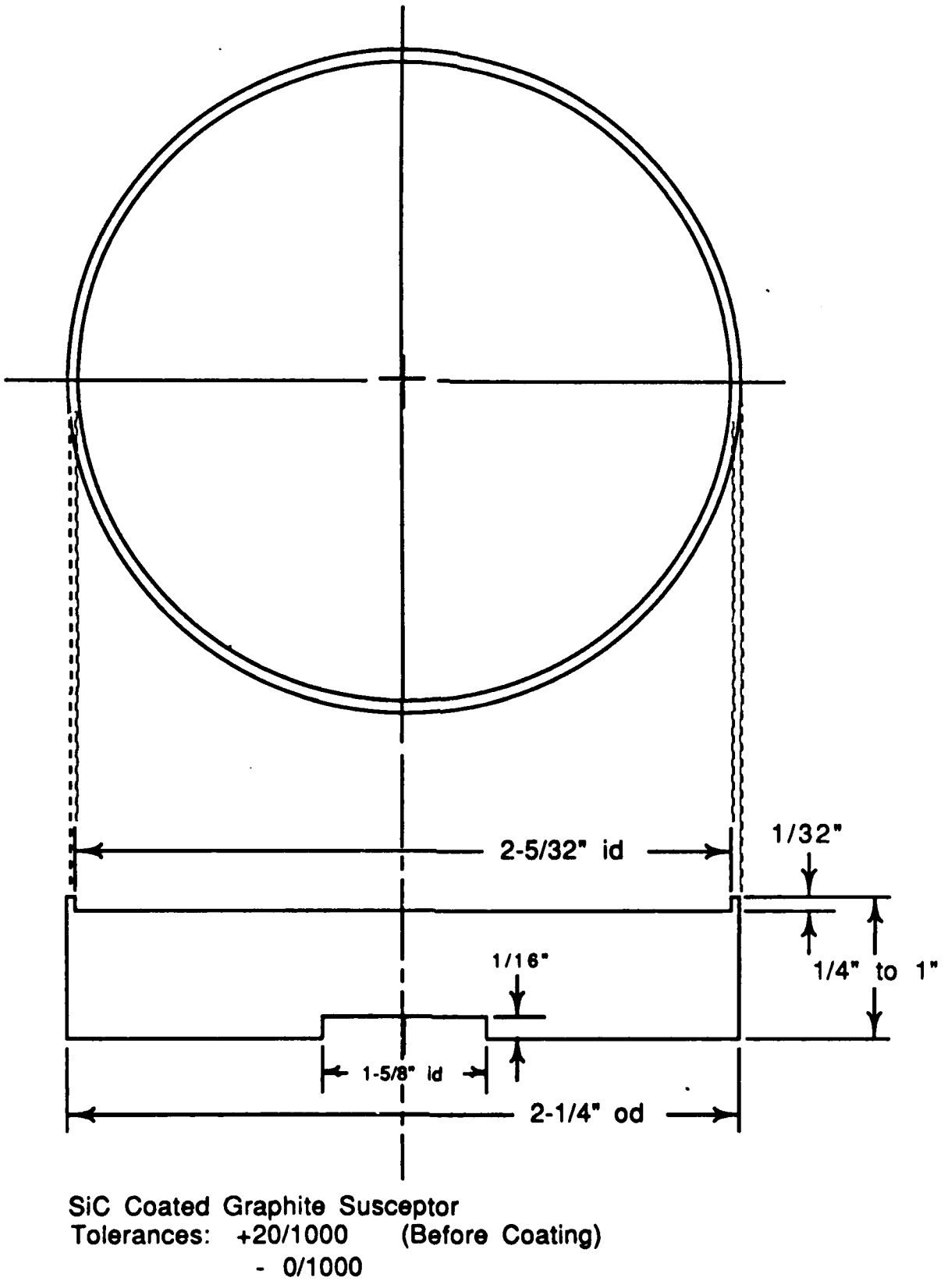


Figure 3. Silicon Carbide Coated Graphite Susceptor Design.

the pedestal was not mounted exactly in the center of the tube. This was important because a susceptor that was placed too close to one side of the reactor would not heat uniformly.

Initially, a poly-silicon wafer holder was set on the SiC susceptor. This combination susceptor had trouble attaining temperatures above 1200°C due to the thermal gradient which existed between the two pieces. The thermal gradient is from 100°C to 200°C depending upon flow rates and power setting of the rf generator. The poly-silicon susceptor did not inductively couple to the coil of the rf generator at the operating frequency of 10 kHz. The poly-silicon was radiatively heated by the graphite susceptor. Attaining temperatures above 1200°C lead to graphite susceptor temperatures approaching 1400°C. At one point, the poly-silicon susceptor began to melt. The use of the poly-silicon susceptor was abandoned after this incident.

Gas Flow System

A schematic sketch of the reactor gas flow system is shown in Figure 4. The hydrogen was purified by passage through a ladium diffusion cell. The nitrogen was purified by passage thr h a catalytic reactor. There were provisions for six reactor gases n the gas cabinet. The flow rates of all gases were measured by rotameters. Filters at appropriate places in the gas lines keep contaminants such as silicon dioxide in the silane from entering the reactor chamber. After construction of the reactor gas system, the system was checked for leaks by pressurizing the system and

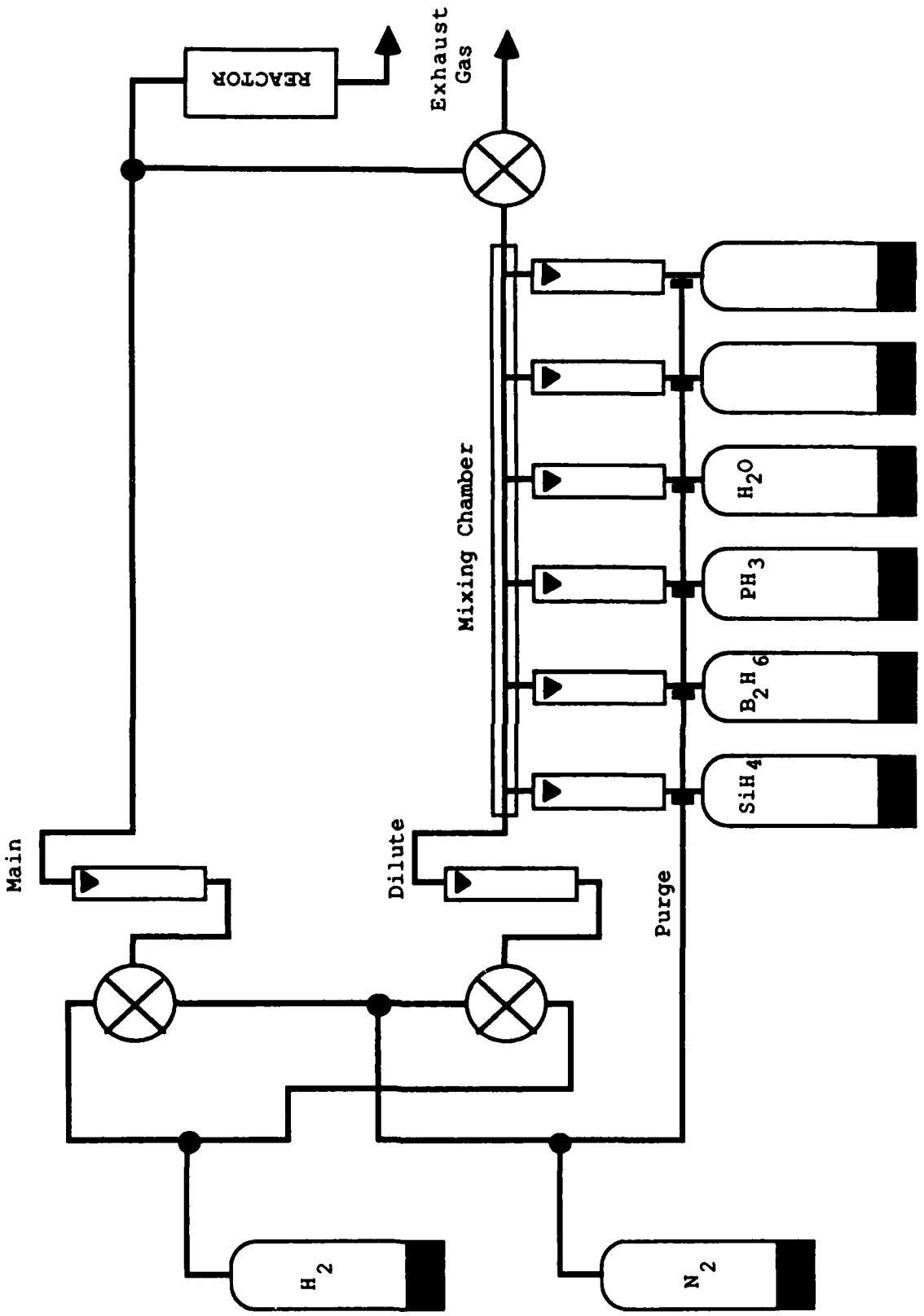


Figure 4. Schematic of Reactor Gas Flow System.

measuring the pressure change over a 24 hour period. The system was considered leak-tight when the pressure dropped less than 5 psi in 24 hours if the initial pressure was 50 psi.

The gas flow through the reactor chamber consisted of two components, the main gas flow and the mixed gas flow. The main gas line was switched, via a three way valve, between the nitrogen and hydrogen supplies. A second valve switched the mixed epitaxial gases to either an exhaust line or into the main gas line where it entered the quartz reactor chamber. Epitaxial gases B_2H_6, SiH_4, PH_3, C_2H_6 and HCl, all diluted with hydrogen were connected to a 1/4 inch stainless steel mixing chamber through separate regulators and flow meters. The needle valves on the flow meters were located on the outlets of the rotameters so that the gas flow rates would remain constant regardless of down stream pressure changes, provided that the inlet pressures remained constant at 15 psig. Also connected to this mixing chamber was a dilute gas line that was switched between the nitrogen and hydrogen supplies. The gas mixture was exhausted to the outside while the flow rates were adjusted to their desired values. The gas mixture was then switched into the main hydrogen gas flow as required.

The reactor used silane-hydrogen mixtures to grow silicon films. Either diborane or phosphine could be added to these mixtures to dope the films p or n-type. The reactor has the capability for mixing dilute silane-ammonia-hydrogen mixtures for experiments aimed at the growth of silicon nitride, silane-propane-hydrogen mixtures for attempts to grow silicon carbide, and silane-water vapor-hydrogen mixtures for the growth of silicon dioxide experiments.

Temperature Monitoring System

The temperature of the wafer was monitored in two ways. An optical pyrometer was used as the primary temperature reference. The pyrometer was sighted between the coils at about a 30 degree angle from the vertical. An optical window was provided in the top of the reactor for an infrared pyrometer to monitor the wafer surface infrared emission. The infrared pyrometer was not calibrated and was used primarily to determine the in situ growth rates [4]. A schematic diagram of the infrared pyrometer is shown in Figure 5.

The film thickness may be measured using the infrared pyrometer technique any time the refractive index of the film is different from that of the substrate material. Film thickness may be measured in situ as oscillation patterns due to constructive and destructive interference of infrared rays emitted from the surface of the substrate and reflected from the film-ambient interface. This process is shown in Figure 6. Constructive interference occurs when the film thickness, $t_c = n\lambda/2\eta$ where λ is the peak wavelength of the detector ($\lambda = 0.9$ μm), η is the index of refraction of the film and n is an integer 0, 1, 2 ···. The thickness per cycle may be calculated from $t_c(n) - t_c(n-1) = \lambda/2\eta$. For silicon this value is 0.12 μm/cycle while for BP this value is 0.17 μm/cycle.

Exhaust System

The reactor gas exhaust system consisted of three parallel lines running outside of the building to a double walled burn chamber. The gas from the reactor was mixed with the internally

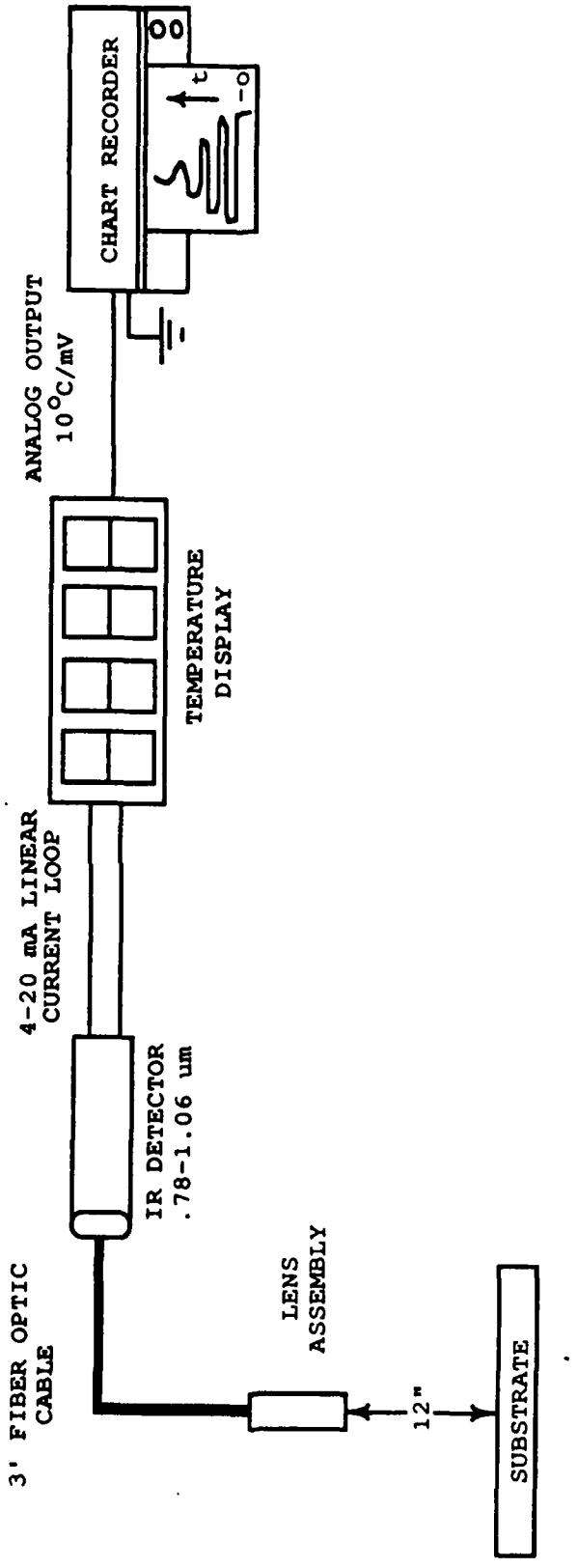
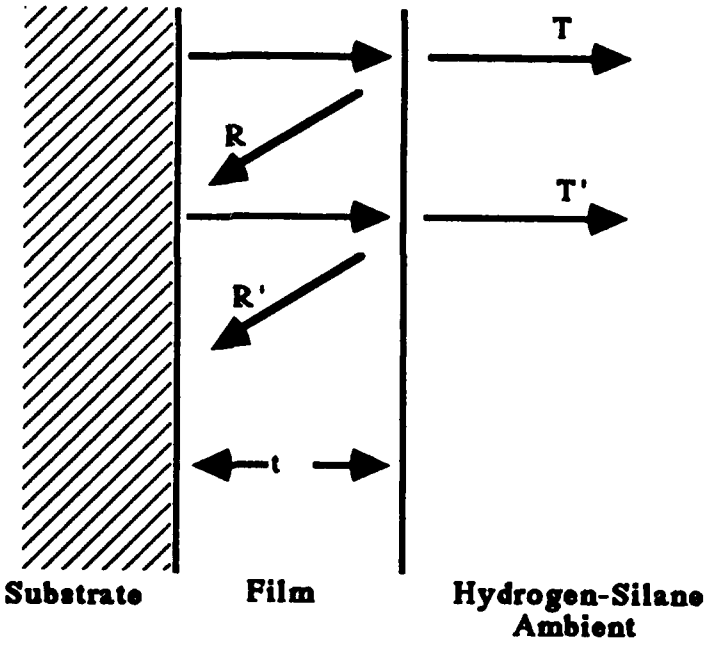


Figure 5. Schematic Diagram of the IR Pyrometer. The peak detectivity of the ir detector was found to be 0.9 μm.



- Infrared emission from substrate reflected from interface
- Constructive interference condition $2t_C = n\lambda / \eta$
- Destructive interference condition $2t_D = (2n+1)\lambda / 2\eta$
- Thickness per cycle $t_C(n) - t_C(n-1) = \lambda / 2\eta$

Figure 6. In Situ Film Growth Measurement Using IR Pyrometer. Constructive and destructive interference patterns are established by reflections of infrared radiation from the film-ambient interface.

bypassed gas and the bleed line from the hydrogen purifier in the burn chamber. The silane used to grow the silicon provided a flame to burn the exhaust gases. A resistive heated wire provided enough ignition to burn the gases when the silane was not present in the exhaust mixture.

Gas mixtures which passed through the reactor chamber were exhausted via a 1/4 inch flexible stainless steel tube into a 1/2 inch copper tube and onto the exhaust burner. The outside fixture was an 18 inch long, 4 inch diameter steel pipe. The pipe was mounted outside a window near the gas cabinet. All exhaust lines terminate at the center of the pipe. A small wire heating coil was mounted at the opening of the exhaust pipes and when attached to a rheostat set to approximately 16% of the line voltage would glow red. The wire temperature was hot enough to ignite the hydrogen. Once ignited, the power was turned off and the constant flow of hydrogen kept the exhaust gases burning.

SECTION III

Growth of the Films

Several types of films grown using this reactor including silicon on silicon or silicon-on-sapphire, boron phosphide on silicon or boron phosphide on sapphire, silicon on boron phosphide, or films obtained from reaction water vapor with silane. The substrates were either (100) silicon or (1-102) sapphire. Regardless of substrate material or epitaxial material(s) the growth sequences were similar.

Silicon wafers were cleaned using a modified RCA etch consisting of:

1. Cotton swab with detergent;
2. Distilled water rinse;
3. Hydrogen peroxide/sulfuric acid, 1:1;
4. Distilled water rinse;
5. Water/hydrofluoric acid, 7:1;
6. Distilled water rinse;
7. Blow dry with nitrogen.

Sapphire wafers were cleaned in a similar manner except steps 5 and 6 were omitted.

The wafers were cleaned immediately prior to their use to minimize contamination and oxide growth on the silicon. No problems with wafer cleaning were observed if care was taken during the cleaning operation.

After the wafers were cleaned they were loaded one at a time into the reactor. Nitrogen was flowing through the reactor and the

mixing chamber during wafer loading. After five minutes of flushing with a high flow of nitrogen, the main line was switched to the hydrogen supply, and after one minute, the rf power was applied to the coil. It usually took about five minutes to bring the wafer up to the desired growth temperature. During the reactor chamber flushing and wafer heating, the mixing chamber was purged with hydrogen and the desired gas flow rates were established. When the wafer had reached growth temperature, the reaction gases were introduced into the growth chamber and the growth was monitored for the desired time. After film growth, the reaction gases were switched back to the exhaust line. The wafers were held at growth temperature for sufficient time to clear the reactor of the reaction gases. The rf power was then removed. When the wafers had reached about 100^{o}C the reactor gas was switched back to nitrogen and the wafer was removed from the reactor when cool. For films in which multiple growths of different materials were required, the same general sequence was followed except for the changing of gases in the mixing chamber between materials.

It was not necessary to determine film thickness after growth since the infrared pyrometer was coupled to a chart recorder and the film thickness was monitored during growth. A typical SOS growth cycle as monitored by the infrared pyrometer is shown in Figure 7. This particular growth was from wafer #340 and was found to have a 0.39 micrometer thick silicon film grown at about 6.0 μm/min. The second pen indicates that the silane was switched into the reactor for only 0.02 minutes or 1.2 seconds. It is also evident that 1.2 seconds elapsed after the silane was switched

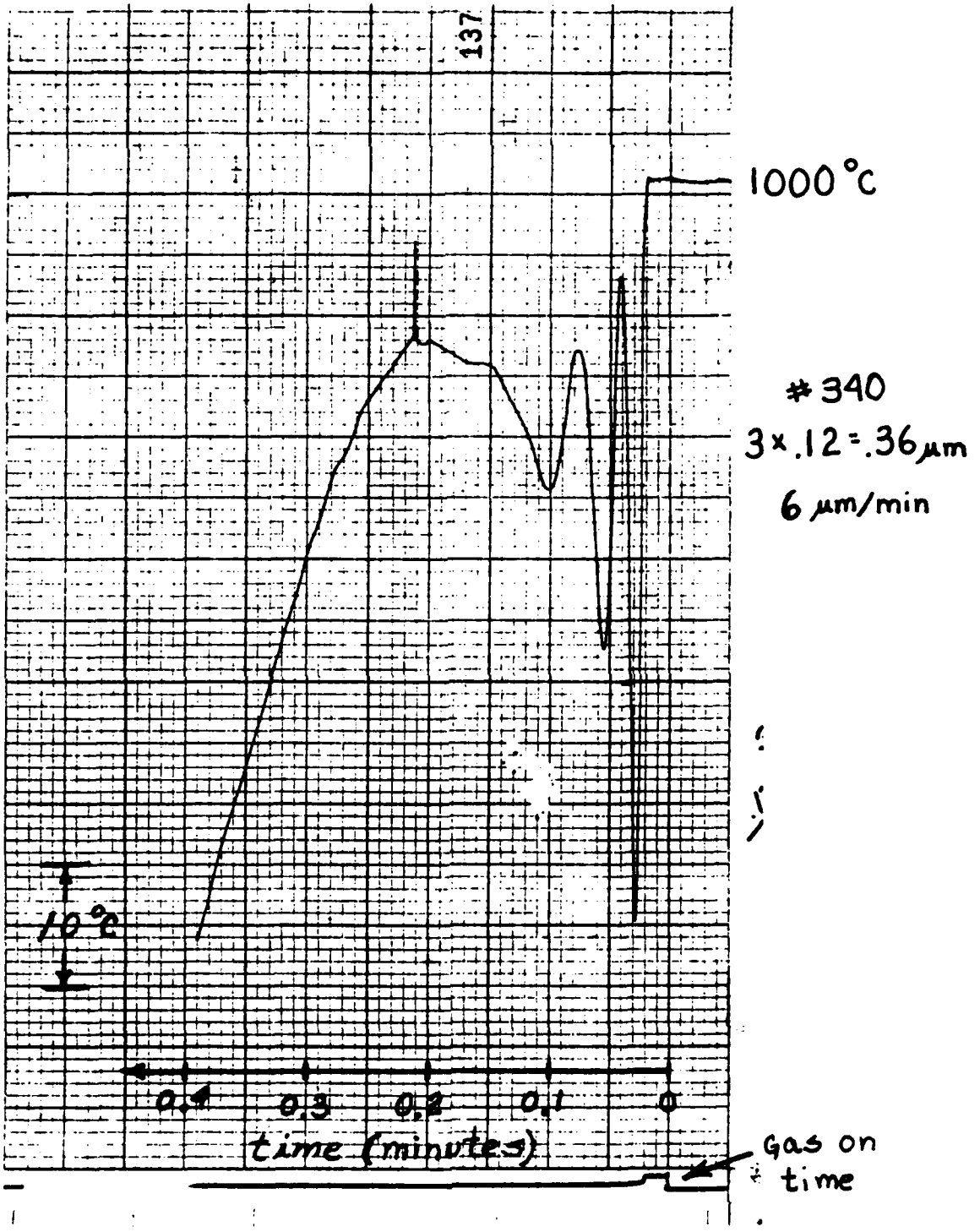


Figure 7. Typical Silicon Growth Cycle. Wafer #340 was a SOS wafer with 0.39 µm of silicon grown at 6.0 µm/min.

into the reactor chamber and before any silicon growth started.

After film growth the general condition of the film was noted. The film resistivity and type was measured and any other desired film properties were measured. Some samples were angle lapped at one degree to verify and correlate film thickness. Some films were taken to the Jeol-848 SEM for electron backscattering measurements to determine crystallinity of the films.

Several of the silicon films grown on both boron phosphide-on-silicon and silicon-on-sapphire were sent to the National Bureau of Standards for fabrication into MOS transistors. These films and the transistor properties will be described below.

SECTION IV

An Examination of Growth and Preparation of Stoichiometric Boron Phosphide

It has been shown that (100) boron phosphide (BP) can be epitaxially grown on a (100) silicon substrate [2] [5-9]. An epitaxial (100) silicon layer can be grown on the BP and used for MOS devices. Both silicon and BP layers have been examined to determine their physical and electrical properties by several authors [10-16]. A general presentation of boron-phosphorus compounds is given by Wasson [17]. The Si-BP-Si structure has been used to develop a double heterojunction which has been examined by Sugiura, Yoshida, Shono, and Dumin [18]. Kim and Shono have shown that BP becomes stoichiometric when heat treated for several hours [19]. In the present paper, results are reported for BP layers of various thicknesses which have been processed in a manner similar to that reported by Nonaka, Kim and Shohno [2]. Variations in the thickness, resistivity and crystal quality of the BP layers following heat treatment is reported for heat treatments at 1000°C and 1050°C. Finally, a comparison was made between BP layers grown at temperatures varying from 950°C to 1075°C.

Initial BP Preparation at 1000°C

Three wafers #252, #263 and #264 were prepared with BP thicknesses of 0.2, 0.5 and 1.0 micrometers respectively on (100), 6-10 Ω-cm, p-type, silicon wafers. The process is described below.

Nitrogen was vented into the reactor chamber at a high flow rate for five minutes to purge any oxygen from the chamber. Hydrogen was switched into the chamber at 9 1/min for one minute. The rf generator was switched on and heat was applied to the wafer. The wafers were heated to 1000°C, a process that usually took from five to ten minutes. Gas flow rates were adjusted while the mixed gases were being vented to the exhaust burner. Epitaxial growths were started by switching the mixed gases into the epitaxial chamber where they mixed with hydrogen carrier gas. A 0.5 micrometer silicon epitaxial layer was grown on the wafer using 5% SiH_4 in H_2 at 1000 cc/min and H_2 dilute at 500 cc/min. Under these conditions, the silicon grew at two micrometers per minute. The SiH_4 flow was switched back to the exhaust line after an appropriate amount of time to stop the silicon growth. The BP was grown at 0.1 micrometer per minute at 1000°C with 1% B_2H_6 in H_2 at 150 cc/min, 5% PH_3 in H_2 at 4200 cc/min and H_2 dilute at 500 cc/min. Immediately following the BP growth, a 5.0 micrometer silicon layer was grown on the top of the BP using the previous silicon flow rates. The top layer was different than the Si_3N_4 layer used to cap the BP by Shono [19]. Because of the large amount of phosphorus deposited on the walls of the quartz tube during the BP growths and autodoping from the BP layer, the silicon layers were found to be n-type with resistivities of 0.0035, 0.0055 and 0.004 Ω-cm for wafers #262, #263 and #264 respectively. These resistivities correspond to impurity concentrations of $2x10^{19}$, $1x10^{19}$ and $1.3x10^{19}$ cm^{-3} respectively [20]. Each wafer was broken into four pieces, each piece being a quarter of the original wafer. Each quarter of each wafer was then heated at 1000°C for 0, 2, 4,

and 6 hours respectively in an attempt to increase the resistivity of the BP layer.

Resistivity Measurements of Initial BP Wafers

Following the heat treatment, silicon was selectively etched from the surface of the BP leaving silicon islands that were used as contact pads for vertical and horizontal measurements of the resistivity of the BP layer. Since the cross sectional area of each vertical measurement was the same, the actual vertical resistance measurement was used as a measure of the vertical resistivity for comparison purposes. The results of the vertical resistance measurements for wafers #262, #263, #264 are shown in Figures 7 and 8. From the data, it can be seen that there was no appreciable change in the resistivity of the BP layer even for heating as long as 6 hours. If there was any trend at all, it was in the tendency of the resistivity of the BP layer to decrease as the time was increased. These results were in contrast with the sharp increase in resistivity reported by Kim and Shono after 100 minutes of heating at 1050^{o}C [19]. Horizontal resistivity measurements of the BP layer were not used for comparison since they were shorted by underlying heavily doped n-type silicon. This underlying n^{+} layer was brought about by diffusion of phosphorus into the silicon substrate during BP growth and subsequent heat treatments.

The samples described above were produced early in the study and measurements made on them were not as uniform as later measurements. Variations in dimensions such as the area of the silicon square used as a contact on the top of the BP layer led to

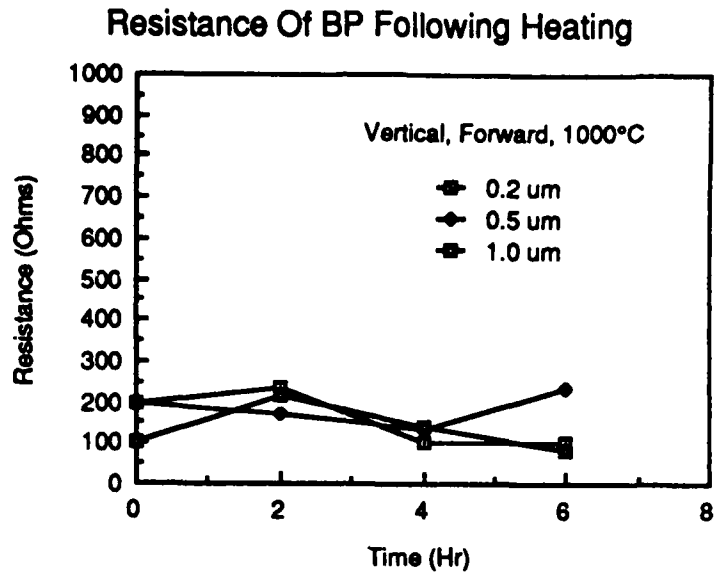


Figure 8. Forward Vertical Resistance Measurement of 0.2, 0.5 and 1.0 μm BP Wafers Heated At 1000°C.

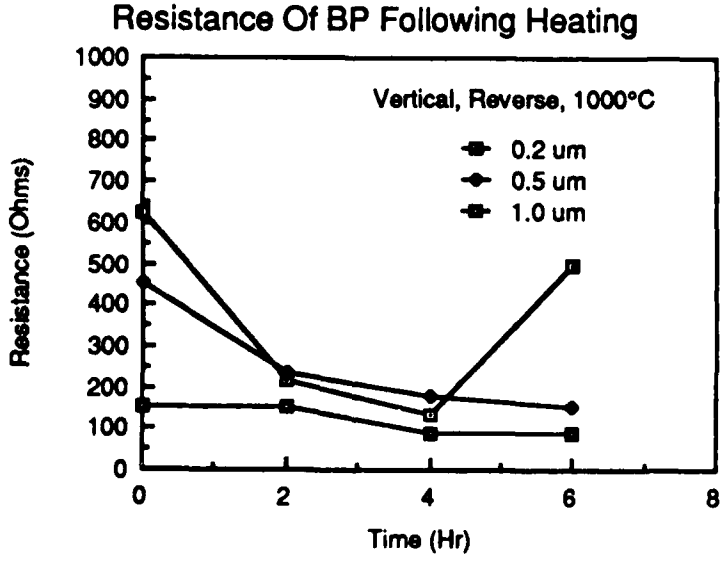


Figure 9. Reverse Vertical Resistance Measurement of 0.2, 0.5 and 1.0 μm BP Wafers Heated At 1000°C.

less than optimal accuracy in the calculation of resistivities. In addition, small angle lappings were not performed on these samples to determine the exact thickness of the BP layers.

Heat Treatment of BP at 1050°C

Since initial tests performed on the BP wafers were inconclusive, it was decided to repeat the experiments with another set of BP wafers. From Shono's results it was assumed that a higher temperature would create a higher resistivity layer in a shorter period of time [19]. Wafers #304, #307, #308, #309 and #310 were prepared under the same growth conditions described above, with 0.05, 0.1, 0.2, 0.5 and 1.0 micrometers of BP respectively on the silicon wafers. This time the reactor tube was cleaned following BP growth to remove the excess phosphorus from the walls so that high resistivity silicon could be grown on the BP layers. It was thought that low doped silicon would aid in diffusion of excess phosphorus from the BP layer into the silicon epitaxial layer during heat treatment. The BP layers were capped with a 1.0 micrometer layer of silicon grown at 2.0 μm/min using 5% SiH_4 in H_2 at 1000 cc/min and H_2 dilute at 500 cc/min. One quarter of each sample was heated at 1050°C for 30, 60, 90, and 120 minutes respectively. Four point probe measurements of the top silicon layer indicated that phosphorus had diffused into the silicon during the heat treatment. The resistivity of the surface silicon is plotted in Figure 10. The data showed that for all but thickest BP sample, the resistivity of the surface silicon fell to approximately 2×10^{-3} Ω-cm after 120 minutes at 1050°C. This

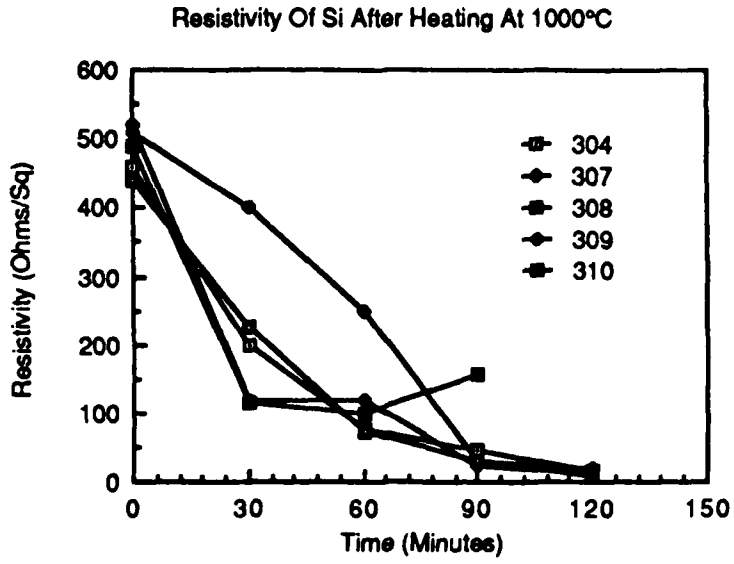


Figure 10. Resistivity of Top Silicon Layer of Si-BP-Si Wafers #304, #307-#310 After Heating At 1050°C. The top silicon layer is auto doped by the underlying BP layer as the sample is heated.

corresponds to an impurity concentration of $3x10^{19}$ cm^{-3} [20, p. 32]. Silicon islands were defined on the top of the BP layers. Measurements were made on each sample of the vertical and horizontal resistance of the BP layer. Problems with etching of silicon islands on the BP made measurement of the cross sectional area impossible. Therefore, the resistivity was calculated from four point probe measurements of the BP surface and thickness measurements of the BP layer. This data is plotted in Figure 11. The measured resistance decreased with increasing duration of the heat treatment due to autodoping of the silicon substrate at the silicon-BP interface. The thickness data has been plotted in Figure 11. It appeared that the thickness of 1.0, 0.5 and 0.1 μm samples of BP had decreased slightly with respect to time.

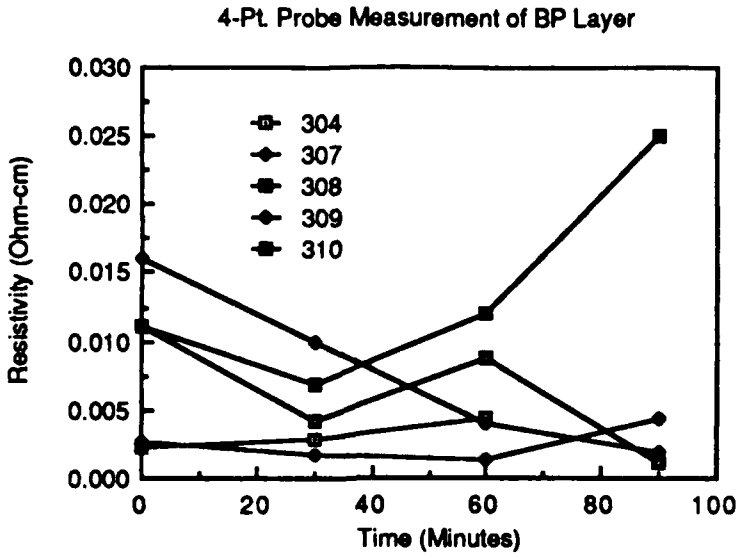


Figure 11. Resistivity of BP Layer of Wafers #304, #307-#310 Measured by Four Point Probe After Heating At 1050°C. The measurement is shorted by n-type silicon at the Si-BP interface.

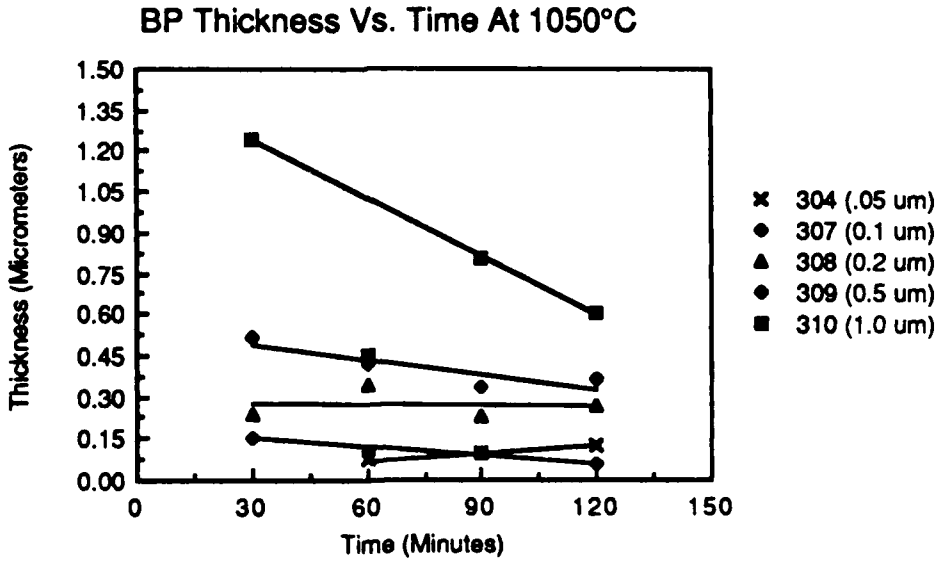


Figure 12. Thickness of BP Layer of Wafers #304, #307-#310 Versus Time At 1050°C. The thickness of the samples appears to be decreasing with respect to time.

Verification of Thickness Changes

Two wafers #353 and #354 were prepared with 0.5 and 0.2 micrometer BP layers respectively on silicon at 1000°C as described earlier. Each wafer was scribed and broken into two pieces. Following cleaning of the phosphorus from the tube, one half of each wafer was coated with one micrometer of silicon. The two halves were then heated simultaneously at 1050°C to create stoichiometric BP [19]. Small chips were scribed and broken from each half wafer sample after 0, 30, 60, 90 and 120 minutes of heating. The area and both forward and reverse vertical resistance of each chip was measured. The chips were then lapped and the thickness of the BP layers were measured.

The forward and reverse vertical resistivities of the BP layers were calculated and are plotted in Figure 13 and Figure 14 respectively. The resistivities were found to be very high ($\cong 10^6$ Ω-cm) even before heat treatment. The BP layers grown at 1000°C had resistivities of approximately the same magnitude as those grown by Shono at 950°C and heated for over 100 minutes at 1050°C [19].

Thickness versus heating time was plotted in Figure 15. It can be seen that the thickness of the BP did not change appreciably after heating at 1050°C for up to 120 minutes. The apparent changes in BP thickness in samples #304, #307-#310 was due to inaccuracies in measurements of the BP thickness. Many of the measurements were performed before equipment was available for more accurate measurements of the lapping angle. A small error in lapping angle would have resulted in large errors in the measurement of the layer thickness [21].

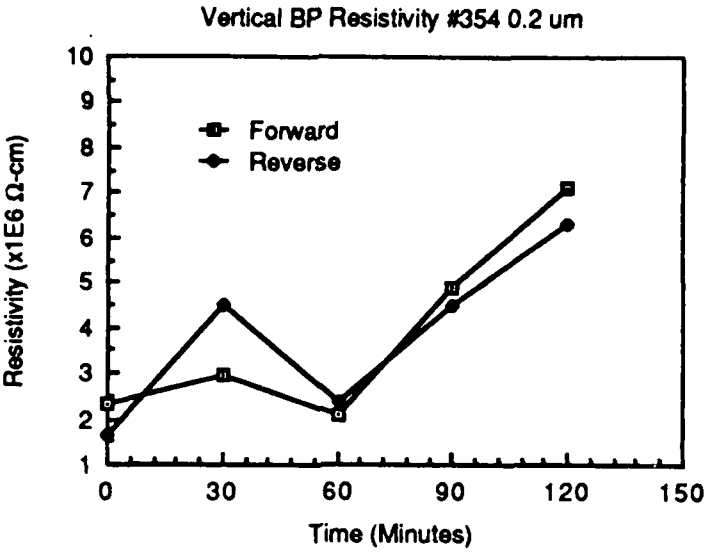


Figure 13. Vertical Resistivity Measurements on 0.2 μm BP Wafer #354. The resistivity of the BP was found to be very high even before heat treatment.

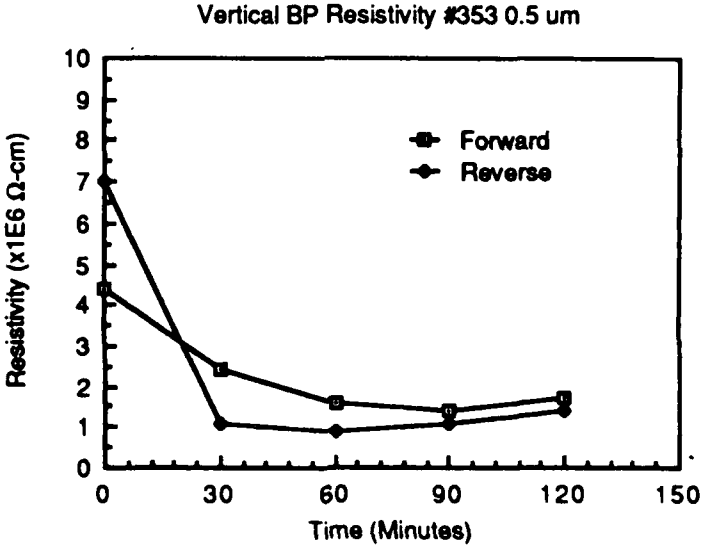


Figure 14. Vertical Resistivity Measurements on 0.5 μm BP Wafer #353. The resistivity has decreased slightly with time.

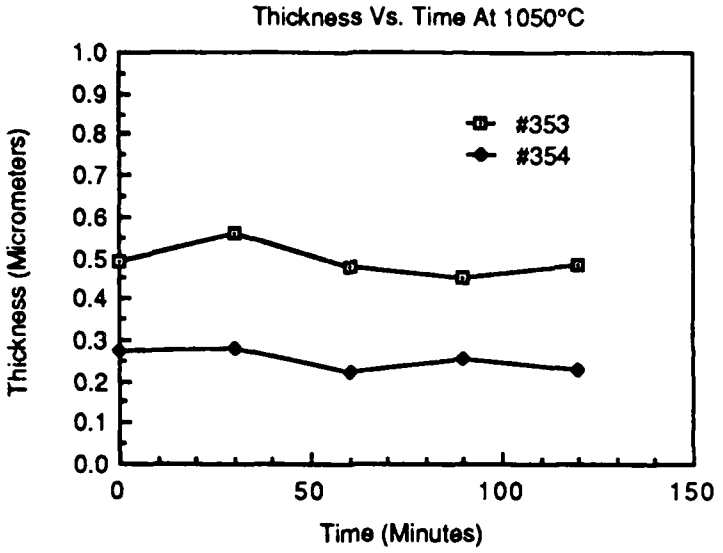


Figure 15. Thickness of BP of Wafers #353 and #354 After Heating At 1050°C. There was no noticeable change in BP thickness even after two hours.

An examination of the resistivity of the BP layer after heating showed that the resistivity of the 0.2 μm BP layer increased by approximately a factor of four to 8×10^6 Ω-cm after 120 minutes. The vertical resistivity of the 0.5 μm BP layer was found to decrease about a factor of four to a final value of 2×10^6 Ω-cm after 120 minutes.

Conclusion

It has been shown that BP may be grown with high resistivity ($\cong 10^6$ Ω-cm) by using appropriate B_2H_6 and PH_3 flowrates at 1000°C. The resistivity of BP as grown appears to be strongly dependent upon growth temperature. In the next section, the variation of BP resistivity is examined as a function of temperature.

SECTION V

Growth of BP Versus Temperature

It was proposed following the previous study that the resistivity and type of the BP layers varied with respect to growth temperature. This characteristic was alluded to by Shono and lead to his variation of the growth process parameters in order to produce both p-type and n-type BP. Shono was then able to convert the BP to a high resistivity BP or to convert n-type BP into p-type BP and vice versa by heating the wafer for a sufficiently long time [19]. In Section IV, it was shown that high resistivity BP could be grown at 1000°C. It was decided to prepare additional wafers to characterize the BP layer with respect to growth temperature.

Experimental Procedure

In order to examine the growth characteristics of BP resistivity versus temperature, 0.2 μm BP layers were grown on (100) silicon wafers #366, #365, #364, #369, #370, #367. The growth temperatures were measured to be 959, 978, 997, 1027, 1055 and 1070°C respectively. BP layers were grown for one oscillation (0.2 μm) using the flowrates in SECTION IV. The results of these runs are compiled in Table 1.

The forward and reverse vertical resistivities are plotted in Figure 16. The resistivity varies from a minimum of 0.6 MΩ-cm at 975°C to over 5.0 MΩ-cm at approximately 1040°C. It is evident from this data that it is possible to grow high resistivity BP layers without subsequent heat treatment of the BP.

Conclusion

It has been shown that BP layers can be grown with resistivities greater than 1.0 MΩ-cm by varying the growth temperature. A maximum resistivity of 5.0 MΩ-cm occurs in BP layers grown at 1040°C. It has been previously reported that n-type BP may be converted to p-type by heating but all layers grown at temperatures up to 1070°C were n-type.

Table 1. Measured Quantities For BP Layers Grown At Temperatures Varying From 950°C - 1075°C.

Wafer Number	Growth Temperature (°C)	BP Thickness (μm)	Silicon Thickness (μm)	Forward Resistivity (MΩ-cm)	Reverse Resistivity (MΩ-cm)
366	959	.26	2.4	.812	.755
365	978	.267	2.4	.581	.581
364	997	.217	3.6	1.711	1.825
369	1027	.223	3.6	3.724	4.612
370	1055	.227	2.77	4.398	2.825
367	1070	.23	2.77	2.883	2.495

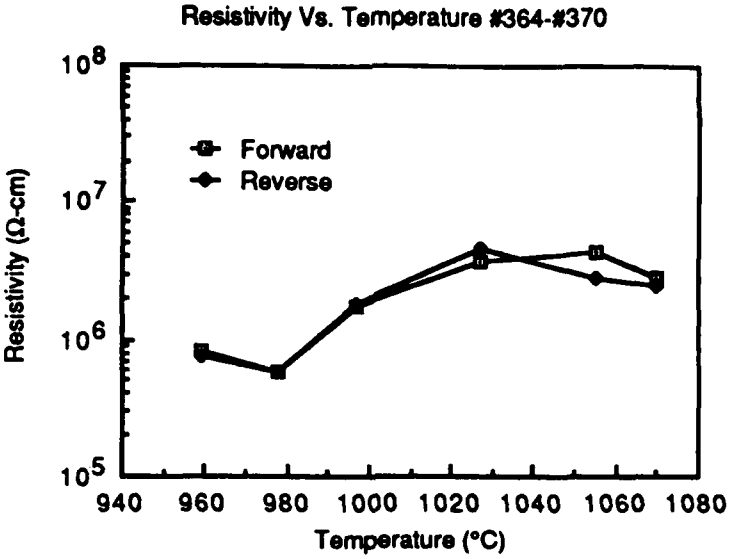


Figure 16. Forward And Reverse Resistivity Measurements of 0.2 μm BP Wafers #364-#370 Grown At Temperatures From 950°C - 1075°C. There is a maximum resistivity of 5×10^6 Ω-cm for films grown at around 1040°C.

SECTION VI

Calculation of the Index of Refraction of BP

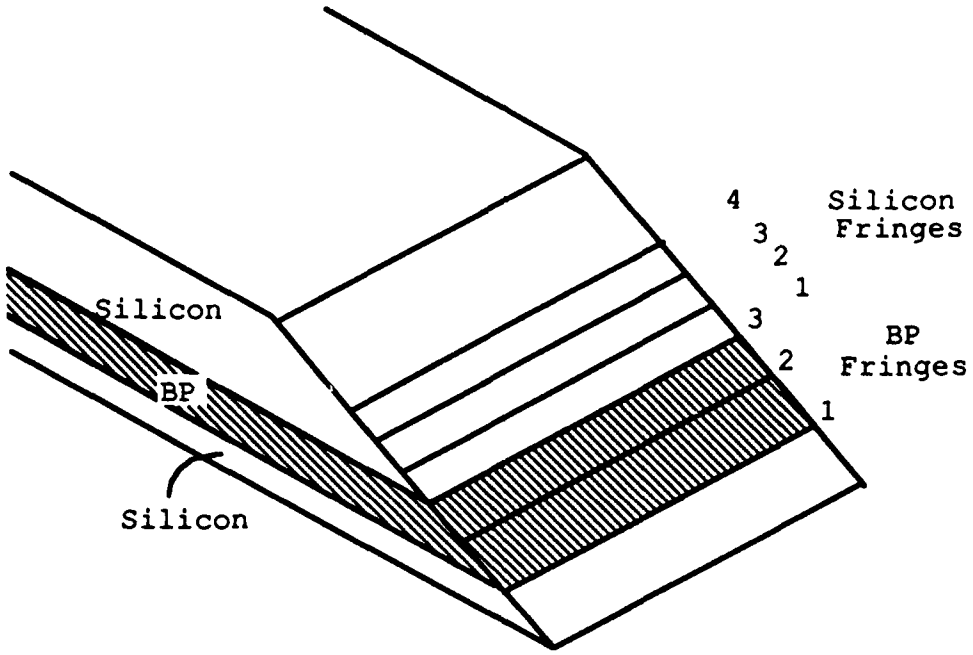
The index of refraction of the BP films grown at Clemson University was found by examining a lapped sample under monochromatic light. Wafers #309 and #310, with 0.5 and 1.0 μm of BP respectively were covered by a layer of silicon and had sufficiently thick BP layers making measurement of the index of refraction of the BP layer possible. The average index of refraction for these BP samples was found to be 2.8.

Experimental Procedure

The index of refraction was found by measuring the distance between dark fringes in a BP layer covered by silicon and comparing the relative distances in the silicon and BP layers. As shown in Figure 17, when lapped at a shallow angle (approximately one degree) and illuminated by monochromatic light (λ = .546 μm) light and dark fringes appear across the lapped portion of the sample due to constructive and destructive interference. Dark fringes occur when

$$D_{Si} = \frac{\lambda\ (n-1)}{2\ \eta}$$

where D_{Si} = thickness perpendicular to the dark fringes, η = refractive index, n = # of fringes (first fringe occurs where the film thickness is zero) and λ = wavelength of illuminating light.



Dark Fringes Occur When:

$$D = \frac{\lambda(n-1)}{2\eta}$$

η = refractive index (3.42 for silicon, 1.45 for oxide)

n = number of fringes (1st fringe occurs where the film thickness is zero)

λ = wavelength of illuminating light in air

Figure 17. Measurement of the Lapping Angle.

The lapping angle, Θ, can then be calculated by

$$\Theta = \sin^{-1}\left(\frac{D_{Si}}{d}\right)$$

where d = distance between the n dark fringes. The magnification, m, of the thickness due to lapping is $M = 1/\sin\Theta$.
Since the index of refraction of silicon is known to be 3.42, the silicon layer on top of the BP was used to find the lapping angle, Θ, and magnification factor, M, for each sample. The distance between fringes in the BP, D_{BP}, is measured and substituted into the equation below to find the index of refraction

$$\eta = \frac{\lambda\ M\ (n-1)}{2\ D_{BP}}$$

where the variables have the same meanings as before.

The above procedure was used to find the index of refraction of eight samples from two wafers #309 and #310 that had been heated at 1050°C for 30, 60, 90 and 120 minutes. All of the refractive index data was in the range 2.5 - 3.1 with the exception of two samples which had questionable measured values of 5.2 and 3.8. No correlation was found between the index of refraction and heat treatment duration. The average index of refraction of the samples (with the exception of the 5.2 and 3.8 cases) was 2.8. This value corresponds closely to previously published values for BP [11].

For our method of in situ film thickness measurement, BP thickness per oscillation, t, was found from the equation

$$t = \frac{\lambda}{2\eta} = \frac{0.9}{2\ (2.8)} = 0.16\ \mu m/oscillation.$$

In the above equation, λ = peak detectivity of our infrared pyrometer and η = index of refraction of BP as found above. Experimental values were found to be 0.2 μm/oscillation which is approximately the calculated value. The index of refraction has been assumed to be independent of temperature for this calculation.

Conclusion

Two wafers with 0.5 and 1.0 μm BP covered by silicon were prepared and pieces of these wafers were heated for 30, 60, 90 and 120 minutes at 1050°C. The index of refraction of the BP layers was found by observing the diffraction pattern on lapped samples under monochromatic light. The lapping angle was found by measuring the distance between dark fringes in the silicon layer. The heating of the wafers was found to have very little effect on the index of refraction of the BP layers which had an average value of 2.8. This value corresponds to previously published data for BP.

SECTION VII

Production of Device Quality Silicon Layers on BP

Two sets of Si-BP-Si wafers were prepared in order to study the quality of the silicon layer grown on the BP. The substrates were (100) p-type 6-10 Ω-cm silicon wafers. BP layers of different thicknesses were grown at 1000°C. Silicon layers of varying thicknesses were grown on the BP to study the effect of thickness on silicon epitaxial quality.

Preparation of 0.2 μm BP

Six wafers were prepared with 0.2 μm of BP grown at 0.1 μm/min. One wafer, #283, had 1.0 μm of silicon grown on it immediately following deposition of the BP layer. This silicon was doped highly n-type with $N_D = 10^{19}$ cm^{-3} as shown in Table 2.

The other five wafers had silicon grown on the BP after cleaning the reactor chamber to remove excess phosphorus from the reactor walls. These wafers, #285-#289, had 1.0-5.0 μm of silicon grown on the BP. All silicon layers were grown at 1000°C using 5% SiH_4 in H_2 at 1000 cc/min. The growth rate of the silicon was 2.0 μm/min. The thicker silicon layers were found to have lower average impurity concentrations as shown in Figure 18. The drop in resistivity is a direct result of decreased autodoping in the silicon further from the BP-silicon interface. The resistivity of the silicon layer was approximately linear over the range from one to five micrometers. The resistivity of the BP layer is shown in Figure 19.

Table 2. Si-BP-Si Wafers Sent To NBS For Processing. Two sets of wafers were prepared with 0.2 and 0.4 μm of BP.

Wafer Number	Thickness Si-BP-Si (μm)	Resistivity (Ω/[])	Resistivity (Ω-cm)	N_D (cm^{-3})
283	.5/.2/1.0	58	.0058	10^{19}
285	.5/.2/1.0	315	.0315	$5x10^{17}$
286	.5/.2/2.0	591	.1182	$7x10^{16}$
287	.5/.2/3.0	1095	.3285	$1.3x10^{16}$
288	.5/.2/4.0	1045	.418	10^{16}
289	.5/.2/5.0	1097	.5485	$9x10^{15}$
298	.5/.4/1.0	500	.05	$2x10^{17}$
299	.5/.4/2.0	1000	.2	$3x10^{16}$
300	.5/.4/3.0	1000	.3	$2x10^{16}$
301	.5/.4/4.0	1200	.48	10^{16}
302	.5/.4/5.0	1600	.8	$6x10^{15}$

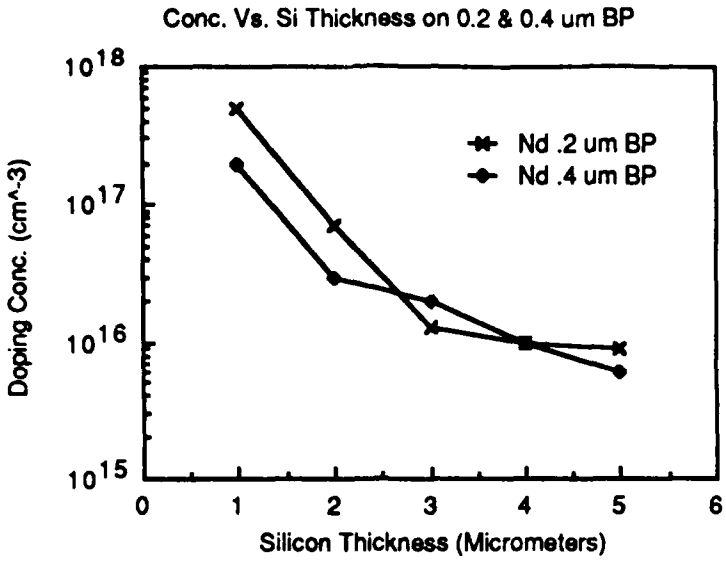


Figure 18. Impurity Concentration of Silicon Layer on 0.2 μm BP Wafers #285-#289 and 0.4 μm BP wafers #298-302.

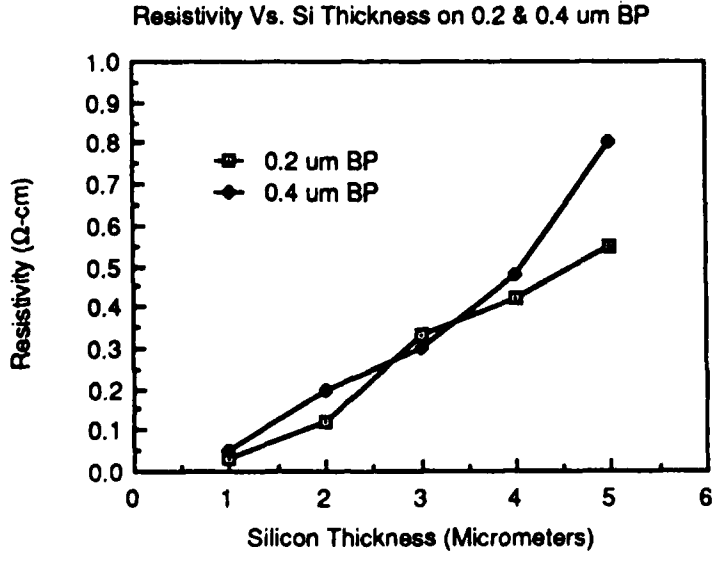


Figure 19. Resistivity of Silicon Layers on 0.2 μm BP Wafers #285-#289 and 0.4 μm BP Wafers #298-#302.

Preparation of 0.4 μm BP

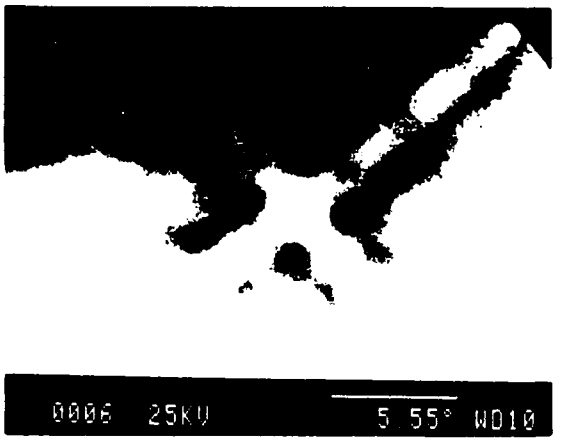
Five wafers were prepared using the same growth conditions as above with 0.4 μm of BP. The reactor tube was cleaned and 1.0-5.0 μm of silicon was grown on the BP layer. These wafers are refered to as #298-#302 respectively. The thicker silicon layers had lower impurity concentrations as shown in Figure 18. The resistivity of the BP layer is shown in Figure 19. The resistivity of the surface of the silicon on the 0.4 μm BP layer rose slightly faster with respect to thickness than the resistivity of the surface of the silicon on the 0.2 μm BP layer. There was essentially no change in the surface resistivity due to variations in the BP thickness implying that autodoping of the silicon is from a constant source of excess phosphorus found at the surface of the BP layer.

The above wafers were sent to the National Bureau of Standards for fabrication of MOS transistors. The transistor properties are described below.

Electron Channeling Patterns

Electron channeling patterns (ECP) were taken of the surface silicon layers using a Jeol-848 scanning electron microscope in backscatter mode. The ECP patterns for the surface silicon layer of the ten Si-BP-Si wafers are shown in Figure 20 and 21. The electron channeling patterns were obtained using an accelerating voltage of 25 KV at a working distance of ten to eleven millimeters.

1



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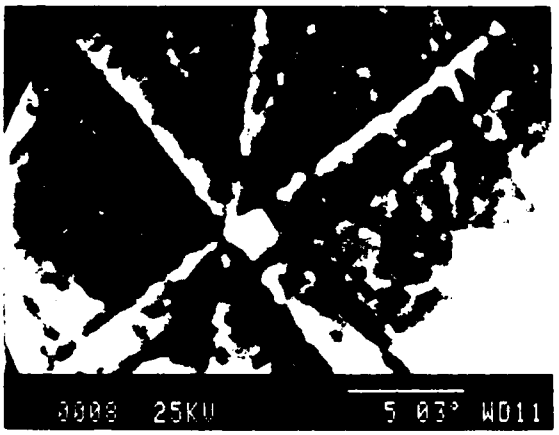

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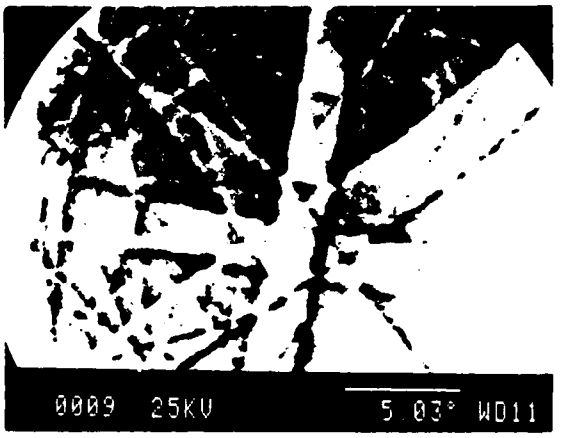

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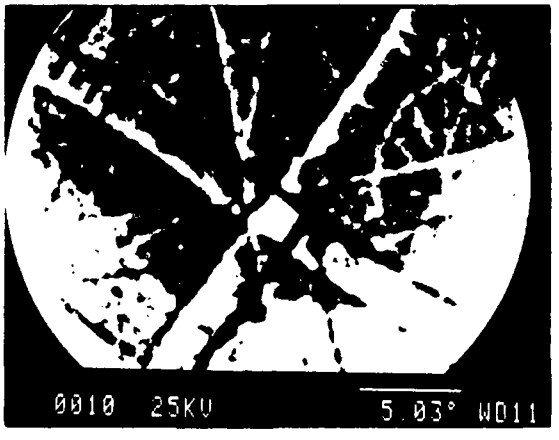

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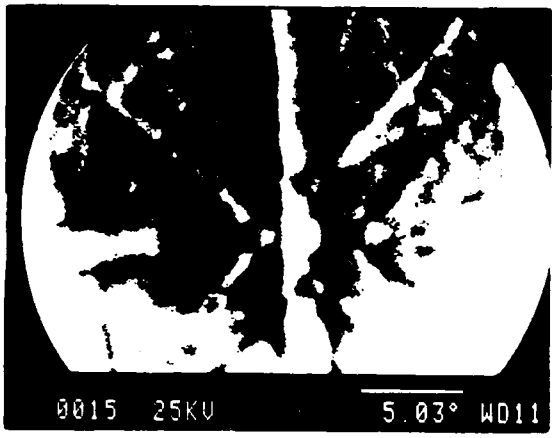
Figure 20. Electron Channeling Patterns of Silicon On BP For Wafers#285-#289. These patterns are for 1, 2, 3, 4, and 5 μm of silicon on 0.2 μm BP.



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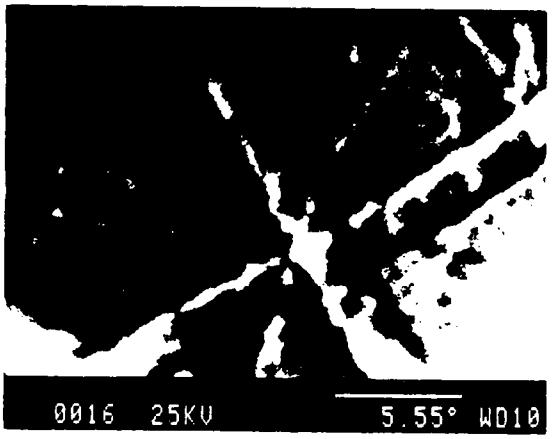

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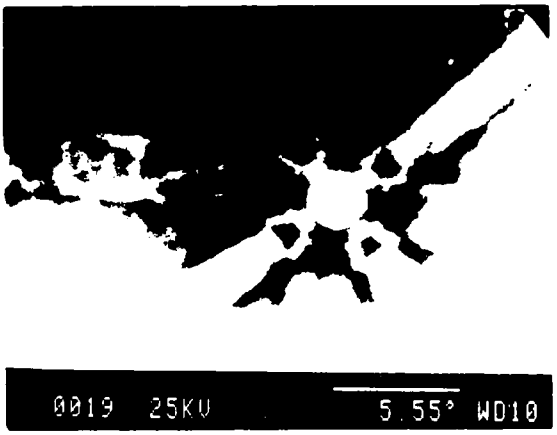

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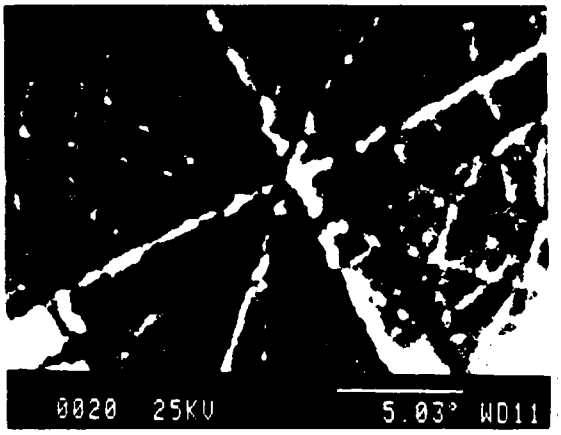

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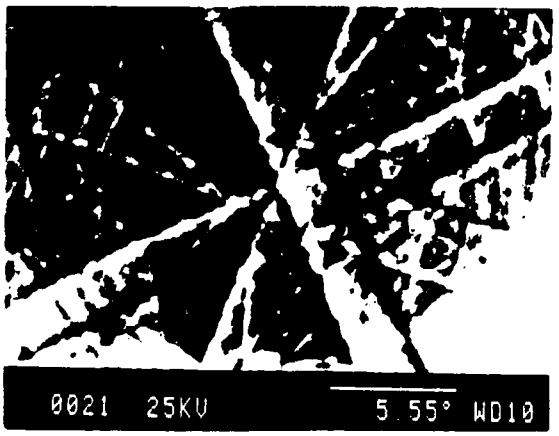

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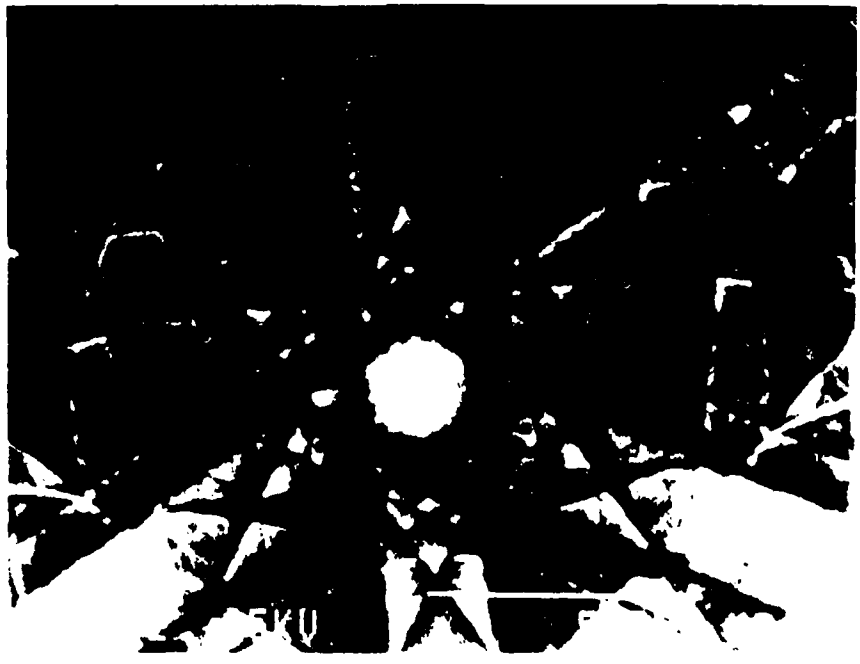
Figure 21. Electron Channeling Patterns of Silicon On BP For Wafers #298-#302. These patterns are for 1, 2, 3, 4, and 5 μm of silicon on 0.4 μm BP.

The general features of the patterns are very similar to the signature patterns from a clean (100) bulk silicon wafer shown in Figure 22. The silicon on BP layers do not show the high degree of crystallinity expected in an heteroepitaxial silicon layer. In general, the silicon layers grown on the 0.4 μm BP layers had slightly sharper ECP patterns than those grown on the 0.2 μm BP layers. Silicon crystalline quality is largely determined by the growth conditions. The apparent lack of long range crystallinity seen in the 2.0/0.2 and 3.0/0.4 ECP photos indicated that these wafers probably had low quality silicon. These wafers also had hazy surface quality which is characteristic of an inferior epitaxial silicon layer.

The electron channeling pattern of the 0.2 μm BP layer is shown in Figure 23. This ECP has a slightly different pattern than the (100) silicon layer. Still present is the strong (100) characteristic of the crystal lattice. Additional reflections in the ECP are due to differences in the size of boron and phosphorus atoms and their relative positions within the crystal lattice.

The electron channeling patterns of the silicon layers on the 0.4 μm BP wafers showed some loss of contrast of the channeling pattern with increased silicon thickness. Wafer #300 had a hazy surface silicon like #286, but #300 had a higher degree of crystallinity. The patterns of wafers #301 and #302 began to exhibit circular patterns characteristic of loss of long range crystallinity across the sample.

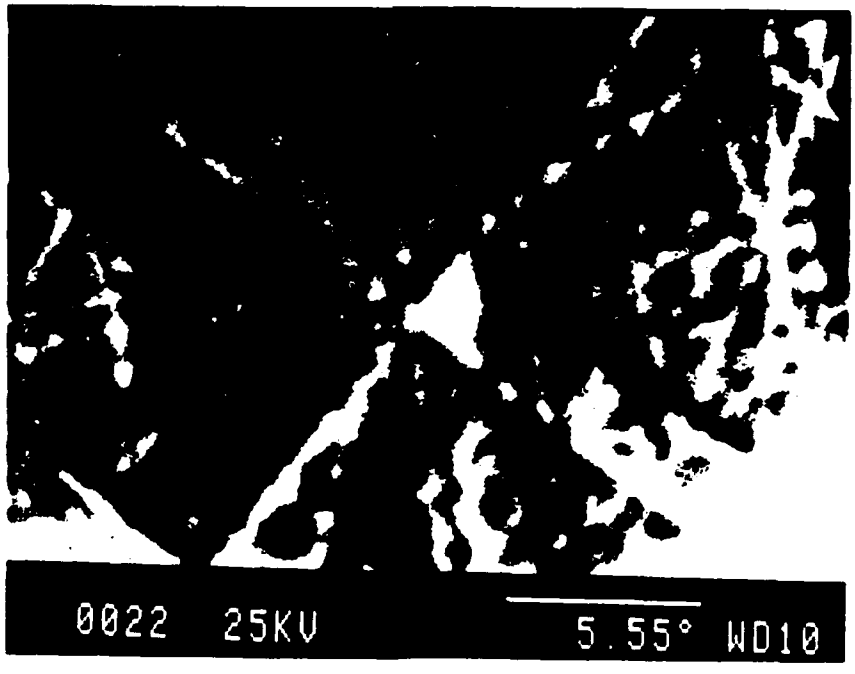
(100)



(111)

Figure 22. Electron Channeling Patterns for (100) and (111) Bulk Silicon Wafers.

(a)



(b)

Figure 23. Electron Channeling Pattern of Uncoated 0.2 μm BP Wafer #293. Picture (a) shows strong (100) pattern. Picture (b) was taken in composition mode to increase image contrast.

MOS Devices

MOS transistors were fabricated on the above wafers. These devices were used to characterize the epitaxial silicon layers. The transistors were metal gate PMOS devices with a gate length of 240 μm and width of 32 μm. The gate oxide was 870 Å thick. The drain and source diffusions were boron implants with $N_A = 10^{20}$ cm^{-3}. Processing was carefully designed to limit thermal excursions thereby minimizing shifts in the doping profile of the top silicon layer during IC processing.

The subthreshold characteristics, drain characteristics, linear and saturation effective surface hole mobilities and threshold voltage of the devices on the Si-BP-Si wafers were measured and compared to bulk silicon values. Transistors manufactured on 1.0 and 2.0 μm silicon layers did not operate properly due to the high background doping concentration. Drain characteristics were ohmic with an average resistance of 165 Ω, 291.3 Ω and 350 Ω for 1.0 and 2.0 μm silicon on BP and 1.0 μm silicon on BP layers respectively. Operating characteristics for transistors on 3-5 μm silicon layers were better as the silicon layers became thicker.

Reverse breakdown voltages were measured and plotted in Figure 24. The corresponding doping densities for one sided abrupt junctions, shown in Figure 25 [20, p. 101], were two to three times higher than measured surface doping concentrations in Figure 18. The reverse breakdown voltage increases linearly with respect to silicon thickness.

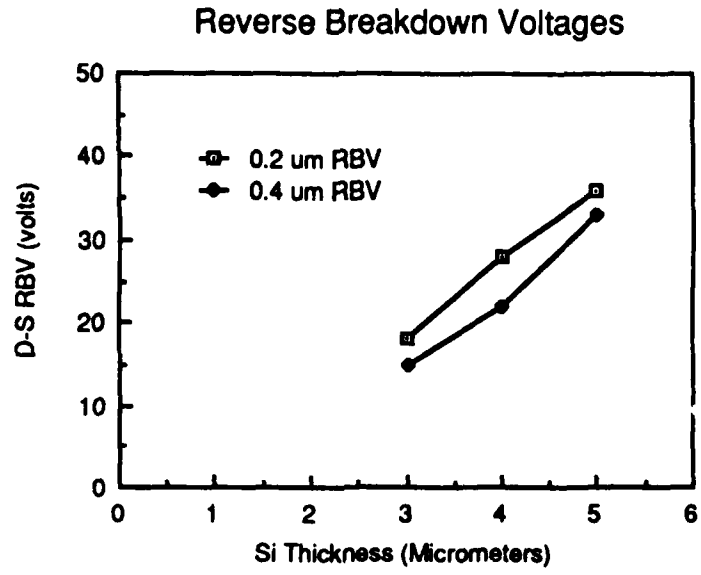


Figure 24. Reverse Breakdown Voltage Versus Silicon Thickness For Silicon on 0.2 and 0.4 μm BP Layers.

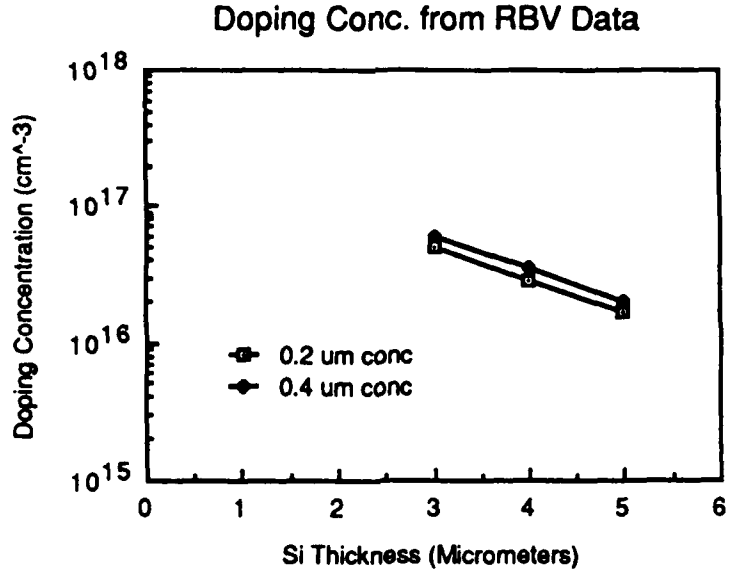


Figure 25. Doping Concentration Versus Silicon Thickness From Reverse Breakdown Voltage Data.

These devices were compared to bulk silicon devices manufactured in the same run which had V_R = 150 volts and corresponding N_A = $5.3x10^{14}$ cm^{-3}.

The average of the effective surface linear hole mobility in working devices was 230 $cm^2/V-s$ while the average saturation hole mobility was 150 $cm^2/V-s$. Mobilities varied little with respect to silicon layer thickness. The mobilities were lower than bulk silicon values due to surface defects but slightly higher than previously published data on a two step silicon layer on BP [16]. Threshold voltages were also the same as previously reported having an average value of -2.6 volts with very little variation from wafer to wafer.

Conclusion

The ECP of the BP layer showed strong (100) orientation. The BP crystal quality was very good. The silicon layers were shown to have (100) orientation with very good crystal quality up to 5 μm thick. The surface doping concentration of the silicon layers decreased with respect to thickness to a value of 10^{16} cm and all layers were n-type. The 1.0 and 2.0 μm silicon layers were doped to $3x10^{17}$ cm^{-3}. Devices manufactured on these layers did not work properly. Devices manufactured on thicker silicon layers worked well having good I-V characteristics. The effective surface linear mobilities on operating devices varied slightly around 230 $cm^2/V-s$ while saturation mobilities were around 150 $cm^2/V-s$. Mobilities were likely limited not by epitaxial silicon crystal quality but by surface defects under the gate oxide.

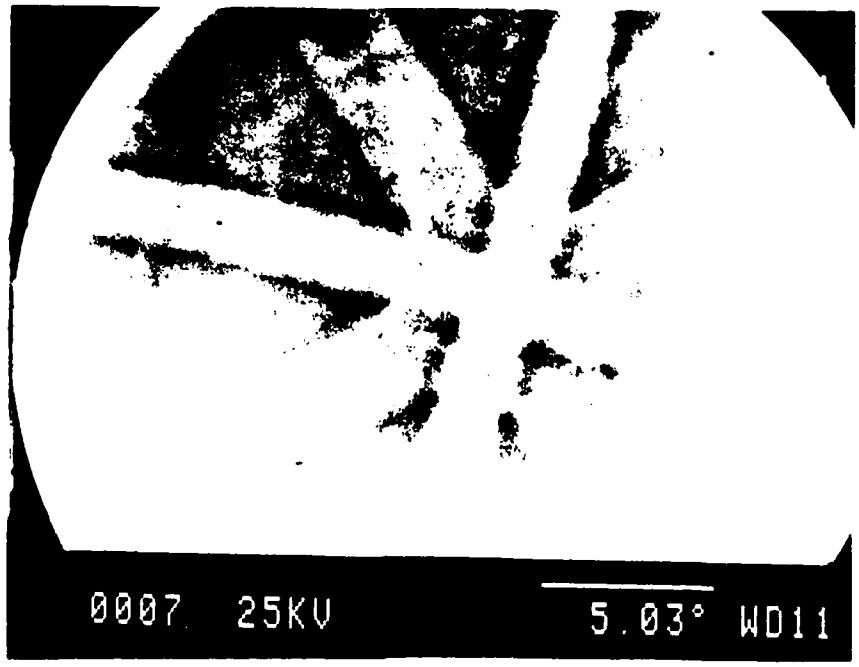
SECTION VIII

Effect of BP Thickness on Epitaxial Silicon Quality

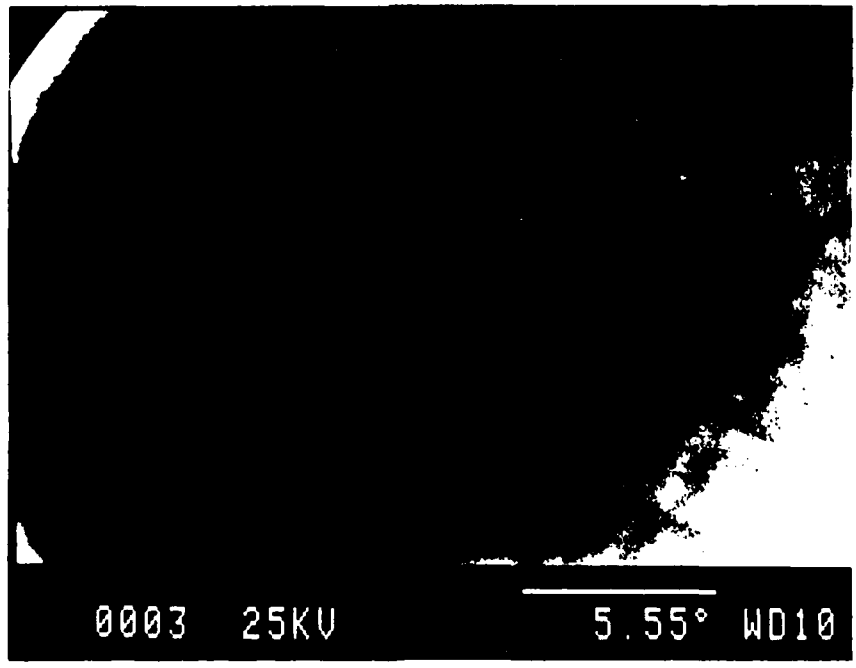
Wafers #304 and #307-310 were prepared with 0.05, 0.1, 0.2, 0.5 and 1.0 μm BP layers covered by 1.0 μm silicon to determine the effect of BP thickness on epitaxial silicon quality. Electron channeling patterns were taken to determine relative crystal quality. The BP and silicon layers were grown at 1000°C using the same flow rates as in SECTION IV.

Electron Channeling Patterns

The electron channeling patterns (ECP) were obtained using a Jeol-848 in backscatter mode with an accelerating voltage of 25 kV at a working distance of 10-11 mm. The ECP photographs of the top silicon layers are shown in Figures 26-28. These photographs indicated that these silicon films were of relatively high crystalline quality and mostly with (100) crystal plane on the surface. These films were not as good as bulk silicon. Wafers #308 and #310 suffered from a lack of contrast characteristic of lesser quality films. It appears that the quality of the silicon film was degraded as the thickness of the BP layer increased. Therefore, crystal quality of the BP layer was degraded for thicker films by a slight amount. This can be contrasted with the situation with SOS films where crystal quality usually improved as film thickness increased [22]. However, it is clear that good quality silicon films may be grown on BP layers as thick as 1.0 micrometer.

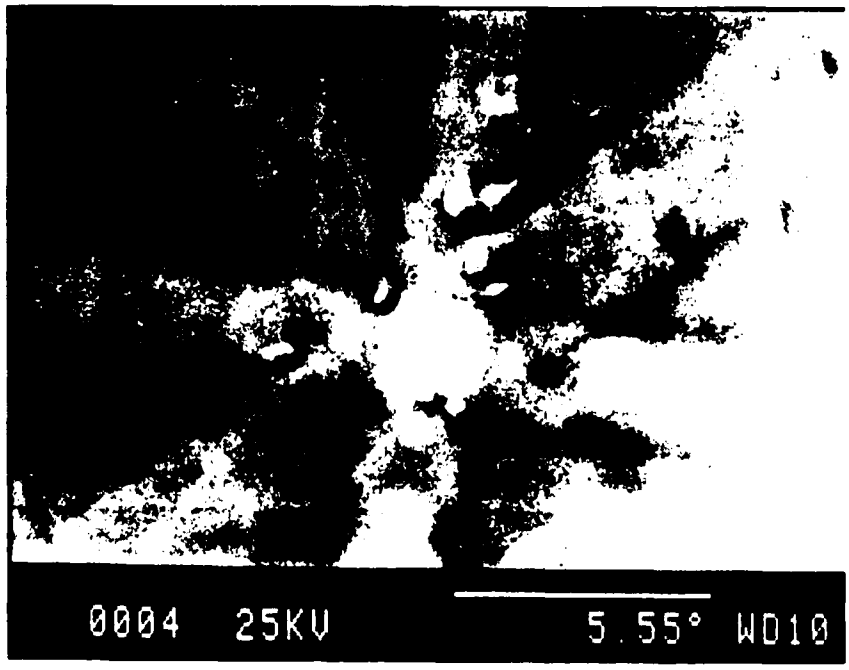


#304

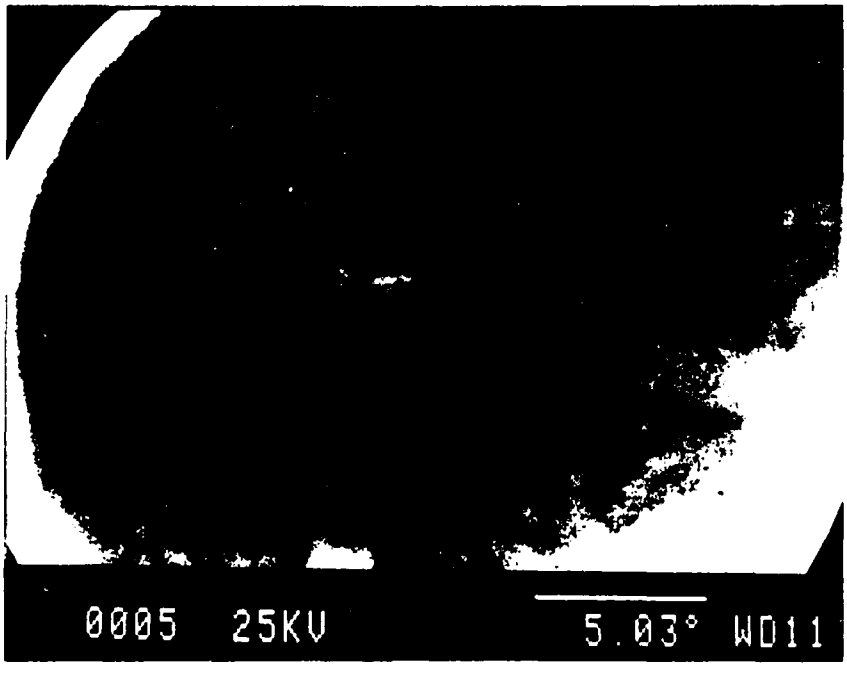


#307

Figure 26. Electron Channeling Patterns of Si-BP-Si Wafers #304 and #307.



#308



#309

Figure 27. Electron Channeling Patterns of Si-BP-Si Wafers #308 and #309.

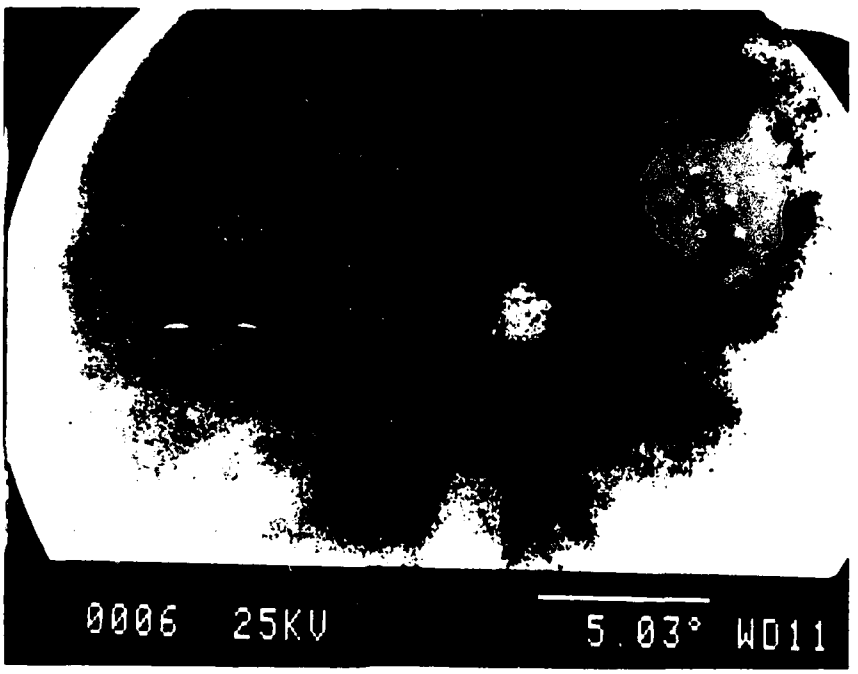


Figure 28. Electron Channeling Patterns of Si-BP-Si wafer #310.

SECTION IX

Depth Profile of a Si-BP-Si Wafer By Spreading Resistance Measurement

Several samples of boron phosphide were prepared for measurement of the depth profile of the Si-BP-Si configuration via spreading resistance measurement. Initially, a 0.5 micrometer silicon epitaxial layer was grown on a (100) p-type 6-10 Ω-cm silicon substrate. A BP layer was grown using the same flowrates as in SECTION IV. Silicon was grown on the BP with 5% SiH_4 in H_2 at 500 cc/min at a growth rate of 1.0 μm/min. All epitaxial layers were grown at 1000°C. Wafers #150-#153 were prepared for this investigation. The measured characteristics for these wafers are tabulated in Table 3.

Table 3. Wafers Prepared For Depth Profile Via Spreading Resistance Measurement.

Wafer Number	Structure	Thickness of Layers Bottom-to-top (μm)	Surface Type	Conductance (Ω/[])
150	Si-BP	.5/.1	P	510
151	Si-BP-Si	.5/.3/.5	P	120
152	Si-BP-Si	.5/.68/.5	P	110
153	Si-BP-Si	.5/.62/.5	P	123

The results of the spreading resistance measurements for wafer #153 are shown in Figure 29 and Figure 30. Figure 29 shows a measurement of the carrier concentration of the sample to a depth of 3.0 μm. The Si-BP-Si layers were clearly evident in the carrier concentration profile. The surface concentration of the n-type silicon layer is about $2x10^{17}$ cm^{-3}. This concentration varies from $4x10^{14}$ to $2x10^{18}$ cm^{-3} through the silicon layer to a depth of approximately 0.4 μm where the BP layer began. The conductivity type in the BP layer remained n-type with a carrier concentration approximately constant at 10^{16} cm^{-3} to a depth of 1.0 μm. The original silicon epitaxial layer was n-type with a carrier concentration of 10^{18} cm^{-3}. All three layers showed the effects of excess phosphorus present in the tube during epitaxial growth. The substrate had a background carrier concentration at a depth of approximately 1.5 μm of 10^{15} cm^{-3}. The corresponding resistivity profile for wafer #153 is shown in Figure 30. The resistivity at the surface of the silicon layer was approximately 0.05 Ω-cm.

These measurements have been used to verify both surface four-point probe measurements and thickness per oscillation measurements for the Si and BP epitaxial layers. Both were found to correlate well to the spreading resistance data.

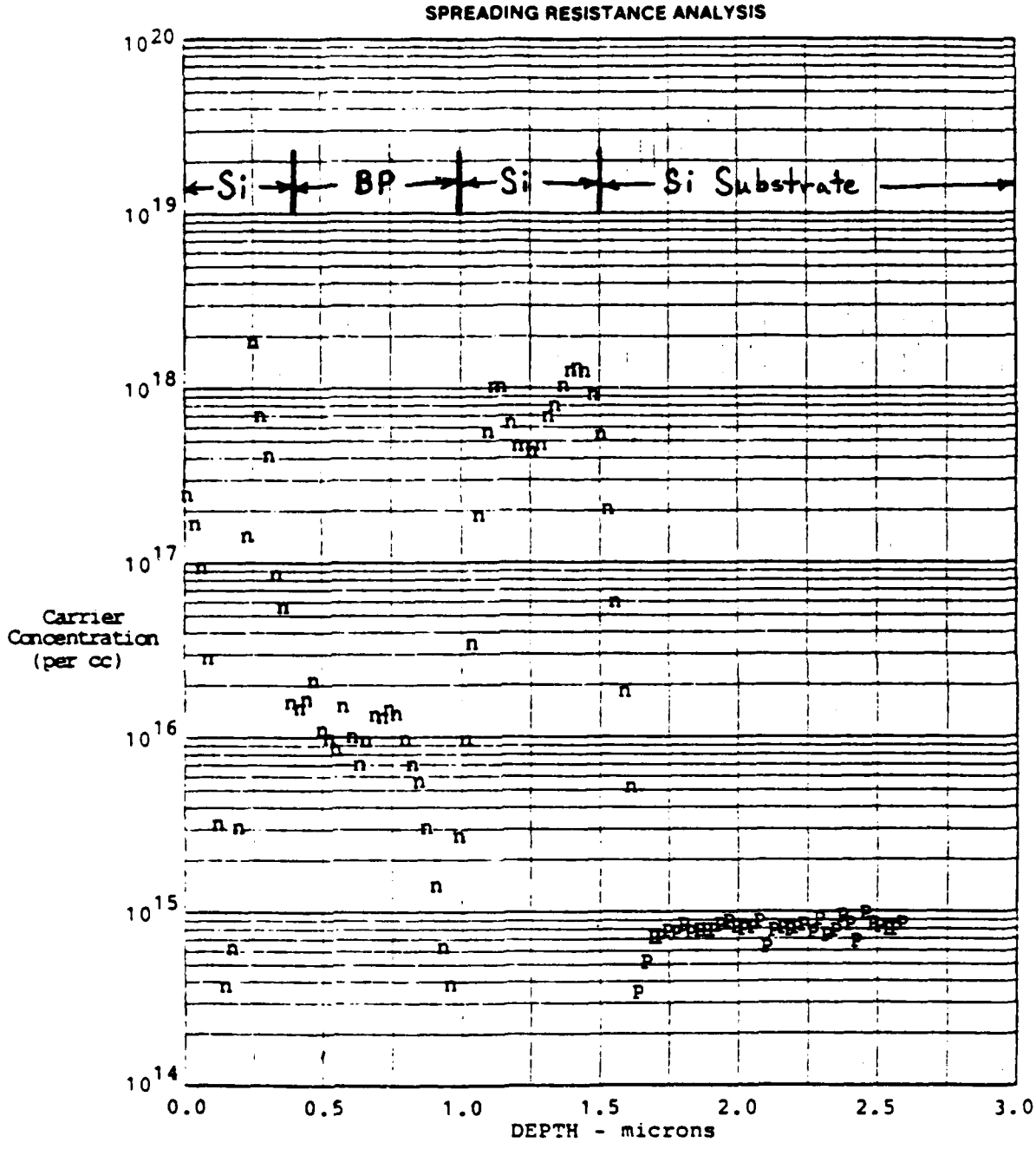
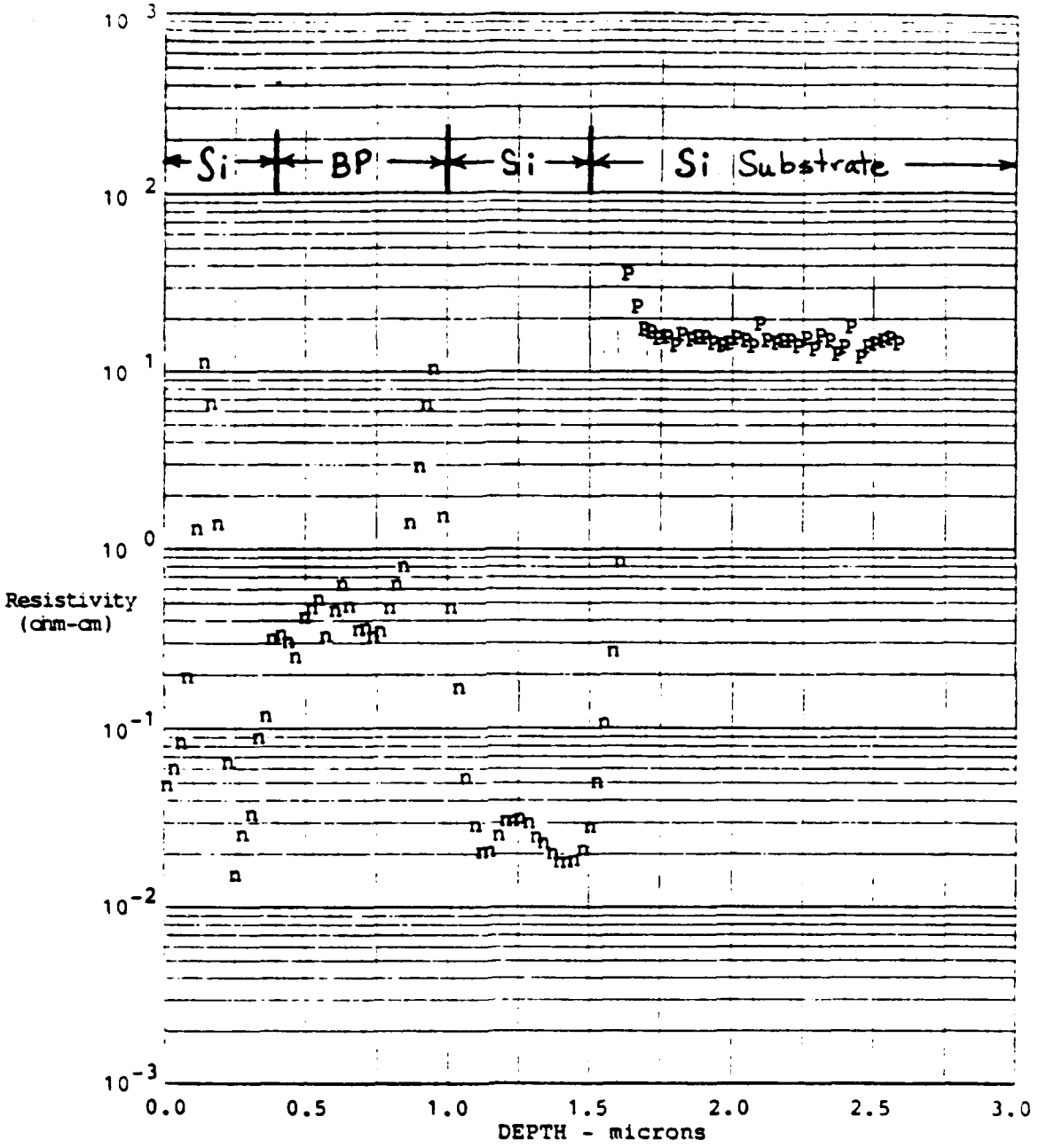


Figure 29. Carrier Concentration Depth Profile For Si-BP-Si Wafer #153.



Date	11/27/85	Probe Load	5g	Orientation	<100>Si
Counter	114300	Bevel Angle	0.0054		
Source	USAFRADC/ESM	Step Increm	5.0um	Sample #	153

Figure 30. Resistivity Depth Profile For Si-BP-Si Wafer #153.

SECTION X

SIMS Analysis of Japanese BP

A sample of BP grown by Professor Shono, Sophia University, Tokyo, Japan, using the same technique used to grow the samples at Clemson University, was subjected to SIMS (Secondary Ion Mass Spectroscopy) analysis. Two spectra were taken, one of the surface of the BP and another of the BP after several hours of ion etching of the surface to remove organic contaminates.

The surface spectrum is shown in Eigure 31. The ion beam was set at 3 kV. Only relative number of counts of each element from the first and second spectrums are shown. On the surface there were indications of hydro-carbon contamination. In addition to the expected boron, phosphorus and silicon peaks (all three were present in large quantity in the epitaxial reactor tube when the BP was grown), there were strong hydrogen, oxygen, carbon, sodium and potassium peaks. An unusual find was the copper peak near 65 AMU. This peak remains relatively constant throughout the sample and is probably due to the copper tubing that was used by Dr. Shono throughout his epitaxial reactor.

Figure 32 shows a spectrum taken after three hours of etching on the surface to expose the underlying BP region. The hydrogen, oxygen and carbon peaks were greatly diminished. There were still strong boron, copper, silicon and phosphorus peaks as expected. The sodium and potassium peaks have remained high probably due to over etching of the surface near the edge of the hole. There was,

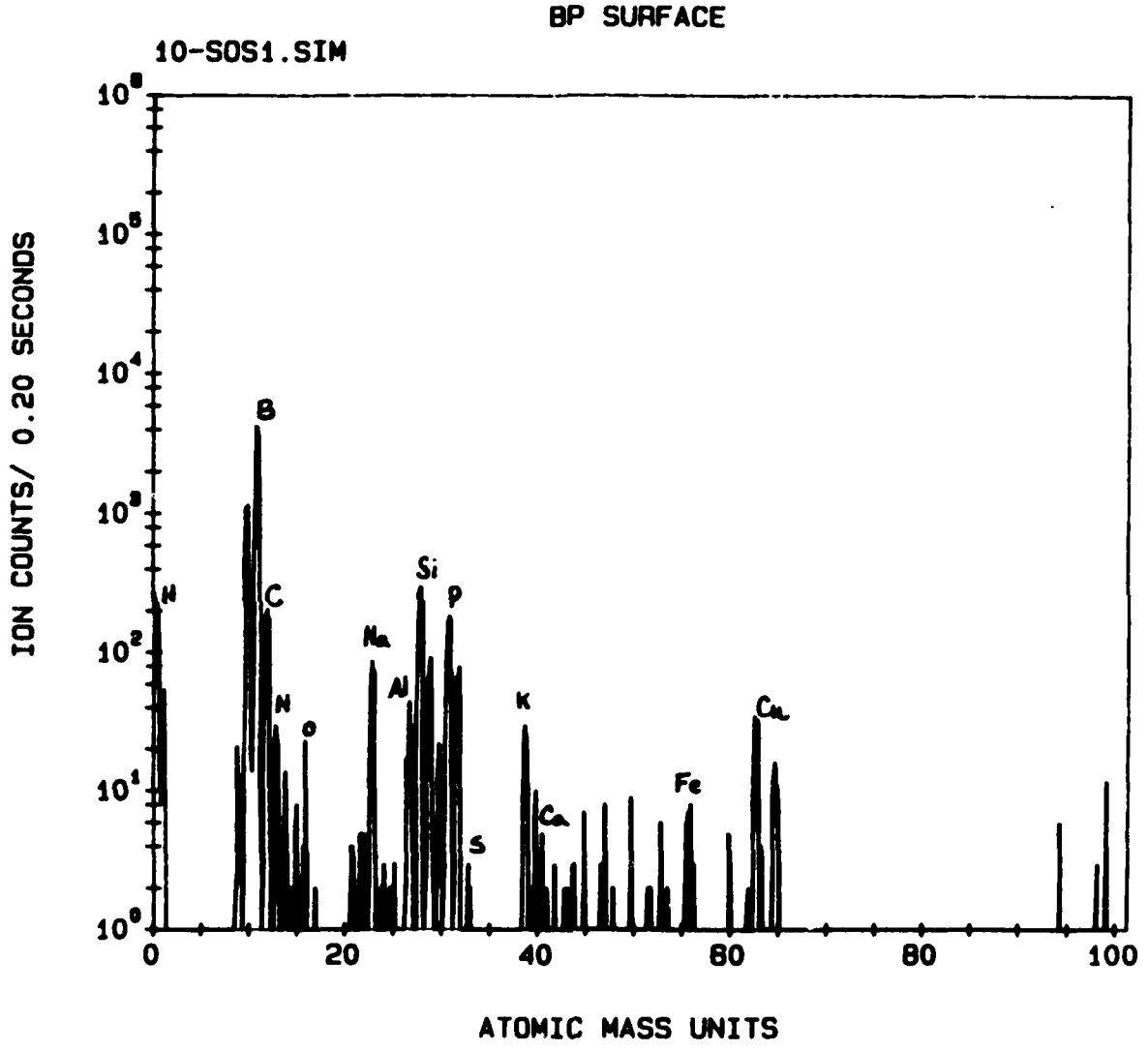


Figure 31. SIMS Surface Spectrum of Japanese BP. Surface contamination is clearly evident by high carbon, hydrogen and oxygen counts.

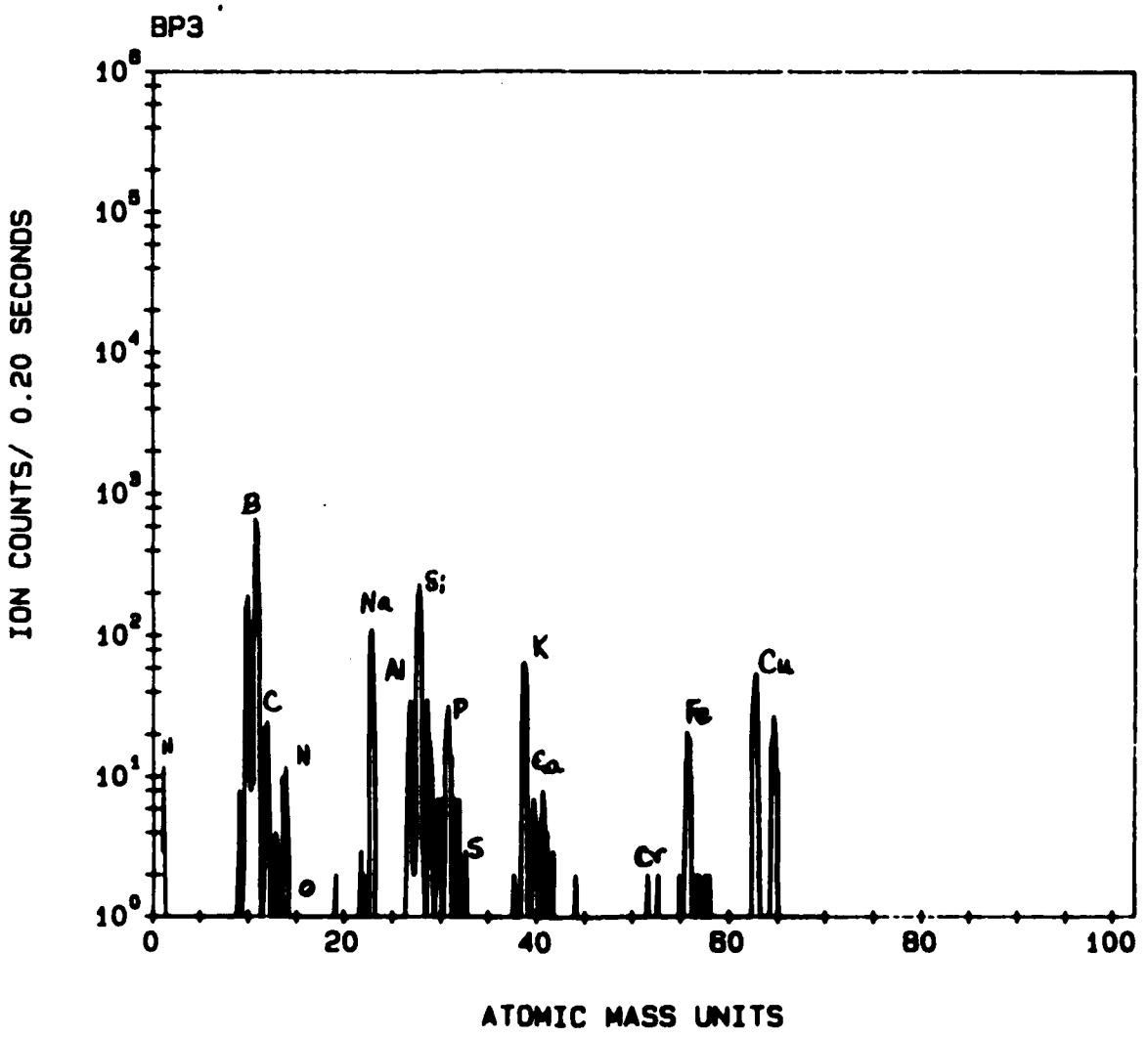


Figure 32. SIMS Spectrum of Japanese BP After Three Hours of Ion Etching. Surface contamination is gone. Large iron and copper counts come from copper tubing used in Dr. Shono's reactor.

however, an unexpected increase in iron concentration within the BP layer. Further SIMS studies of BP layers grown at Clemson University have been delayed while repairs were made to the microscope. Results are not ready as of the date of this report.

SECTION XI

Thin Film SOS Produced at High Growth Rates

SOS Growth at 1000°C

Several SOS wafers were prepared in an attempt to characterize the growth and film quality of very thin silicon films grown on sapphire substrates at growth rates as high as 15 μm/min. These wafers will have MOS transistors fabricated on them in order to fully characterize these films. SOS films were prepared and have been sent to the National Bureau of Standards for processing. The results will be reported when transistors are available for testing.

Silicon-on-sapphire wafers were produced in the same manner as other silicon layers described earlier. Several early attempts were made to grow 0.2 μm SOS at 1000°C with growth rates approaching 32.0 μm/min using 5% SiH_4. The technique used was to set the flow rate of the silane with dilute hydrogen and exhaust the mixture to the outside burner. The silane was then quickly switched in and out of the reactor chamber line. This technique would introduce a slug of silane into the reactor which would pass over the heated sapphire wafer quickly clearing the tube and growing a very thin SOS layer. The maximum concentration of silane achievable with 5% SiH_4 in hydrogen was not high enough to get growth rates much above 10.0 μm/min. It was decided to install 100% SiH_4 on the system in order to grow silicon at even higher growth rates. Using 100% SiH_4, the experiment was repeated making growths at 1000°C with varying flow rates. The time that silane was switched into the growth chamber varied from 30 seconds at very

low growth rates to less than a second at very high growth rates. The results of these experiments are shown in Table 4. The silicon growth rates varied from 0.5 to 24.0 μm/min. Silane flow rates over this range varied from 25 cc/min to over 2500 cc/min. The H_2 main was set at 9 l/min and the H_2 dilute was set at either 500 cc/min or 1000 cc/min. Silicon growth rates were not greatly affected by variations in the main and dilute flow rates.

When the growth rates were high, it became almost impossible to clear the reactor chamber quickly enough to prevent films from growing over 0.2 μm thick. Growths approximately 0.2, 0.5 and 1.0 μm were prepared for most growth rates. Wafer #349 had the highest growth rate of 12.0 μm/min of the wafers with 0.2 μm of silicon.

Table 4. Growth Rate and Film Thickness For SOS Wafers Grown Using 100% SiH_4.

Growth Rate (μm/min)	Silicon Thickness (μm)		
	0.2	0.5	1.0
0.5	#323	#336	----
1.0	#326	#337	----
2.0	#324/#331/#343	#338	----
4.0	#334/#341/#344/#348	#332/#333	----
8.0	----	#340	#339
12.0	#349	#327/#330/#350	----
16.0	----	----	#345
24.0	----	----	#329

SOS Growth at High Temperatures

Silicon-on-sapphire wafers were prepared at temperatures varying from 1000°C - 1150°C using the growth conditions of wafer #349. These growth conditions provided the highest growth rate of any of the 0.2 μm SOS wafers. This growth rate of 12.0 μm/min was grown using 100% SiH_4 at 3000 cc/min. Wafers #374 - #378 were grown under these conditions at 1000, 1050, 1100, 1150 and 1125°C. Above 1000°C, the sapphire substrates were slowly heated to the final growth temperature to prevent breakage. After silicon growth, the temperature was slowly reduced below 1000°C at which time the power was switched off. A summary of the results appears in Table 5.

Table 5. High Growth Rate, High Temperature SOS. Flow rates for these wafers were; SiH_4 at 3000 cc/min, H_2 main at 9 l/min, and H_2 dilute at 1000 cc/min. The growth rates were measured from initial silicon growth.

Wafer Number	Temperature (°C)	Growth Rate (μm/min)	Thickness (μm)
374	1000	16.0	0.4
375	1045	8.0	0.4
376	1097	13.0	>1.0
377	1155	13.0	>1.0*
378	1125	26.0	>1.0*

* indicates polysilicon growth.

Wafers #374 - #376 all had very good, shiny, single crystal silicon epitaxial layers. At growth temperatures above 1000°C, vapor phase decomposition became a problem. By 1100°C, variations in crystal quality were noticeable on the wafer. At this point, it was hard to grow very thin silicon layers.

Wafer #378, grown at 1125°C showed signs of polysilicon growth. Wafer #377, grown at 1155°C was completely covered by poly-silicon. Both of these wafers turned out to have silicon thicker than one micrometer.

It was determined that the best growth temperatures were from 950°C - 1100°C. Above 1100°C, silicon was deposited as poly-silicon over one micrometer thick due to the large amount of vapor phase decomposition present in the reactor chamber above the susceptor. All of the above wafers were sent to the National Bureau of Standards for processing into MOS transistors. The results of the transistor study will be presented when available.

SECTION XII

Attempted Growth of Single Crystal SiO_2-On-Silicon

Process Development

It was proposed that SiO_2 could be grown by the pyrolytic decomposition of silane with water vapor in hydrogen. This would be an epitaxial process, rather than the normal oxidation of silicon by water vapor [23-25], that would allow the growth of single crystal silicon on the oxide. These wafers could serve as a low cost alternative to SOS for SOI applications such as submicrometer CMOS and radiation hardened integrated circuits. An examination of the SiO_2 epitaxial growth process was carried out over the temperature range from 950°C to 1200°C.

Growth Process

A two step process was developed in an attempt to grow single crystal SiO_2. First, a 0.5 μm silicon epitaxial layer was grown on a (100) 6-10 Ω-cm silicon substrate using 5% SiH_4 in H_2. Then a graded buffer layer was grown by increasing the flow rate of 0.1% H_2O in H_2 to a predetermined mixture ratio. This ratio was achieved in 30 seconds. The silane and water vapor mixture was allowed to pass over the heated wafer for four minutes. Both gases were then cut off and the wafer was cooled in hydrogen. The quality of the oxide layer was checked by growing a silicon layer. The flow rate of H_2O was reduced to zero over a period of thirty seconds to grade from SiO_2 to silicon.

Oxide Characteristics

The initial oxide layers were grown with H_2O at 2500 cc/min, SiH_4 at 50 cc/min and H_2 dilute at 5 l/min. The growth temperature was 1000°C. The surface of the oxide covered wafers varied from very shiny dark blue to golden brown, typical of very thin films. Only gray polysilicon could be grown on the oxide layer. The surface was covered with long strands of silicon. Electron channeling patterns of the SiO_2 surface showed no pattern suggesting an amorphous layer.

The hydrogen dilute was reduced to 500 cc/min in an attempt to increase the oxide growth rate. The surface of the wafers were shiny with very dark green color at the edges which became red toward the center of the wafer. Small brown nodules appeared to be evenly distributed across the wafer. These nodules were apparently silicon that had not oxidized with the water vapor. These wafers were examined in the Joel 848 electron microscope. The surface of the oxide is shown in Figure 33. Clearly shown are cracks in the oxide layer formed during deposition which could be the result of strain. The five micrometer silicon layer grown on the oxide with SiH_4 increased to 500 cc/min had thin strands of silicon that rose from the polysilicon surface as shown in Figure 34.

The oscillation patterns for these wafers are shown in Figures 35 and 36 respectively. The growth rate of the oxide layer on wafer #162 was found to be 0.25 oscillations per minute. Both wafers were lapped and the thickness of the oxide layer was found (using the method described earlier) to be 0.31 micrometers indicating a growth rate of $t = 0.31$ μm/osc. The index of refraction, η, of the oxide layer was then found to be

Figure 33. Electron Micrograph of Oxide Surface.

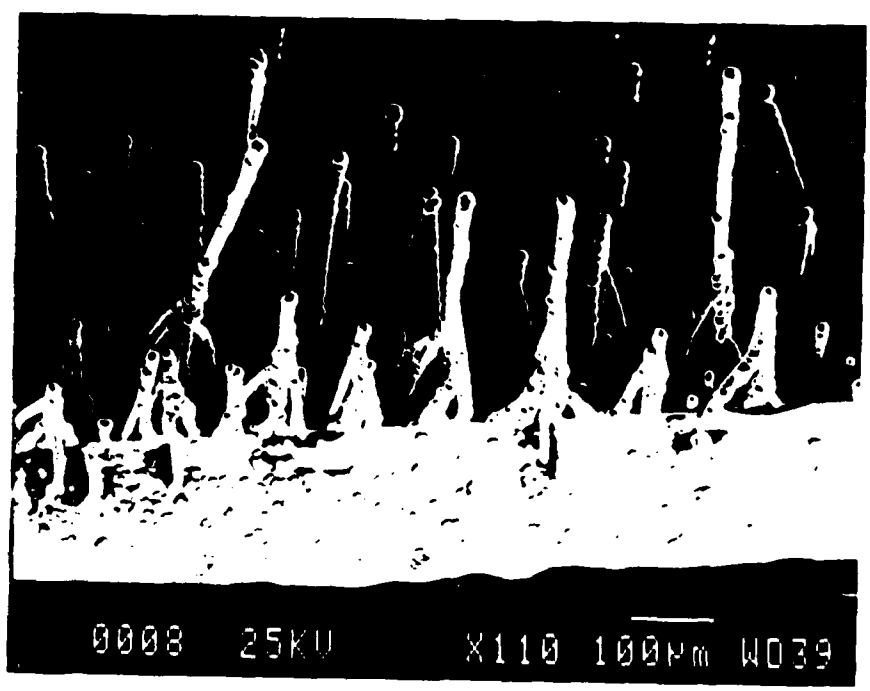


Figure 34. Electron Micrograph of Silicon Surface on Oxide.

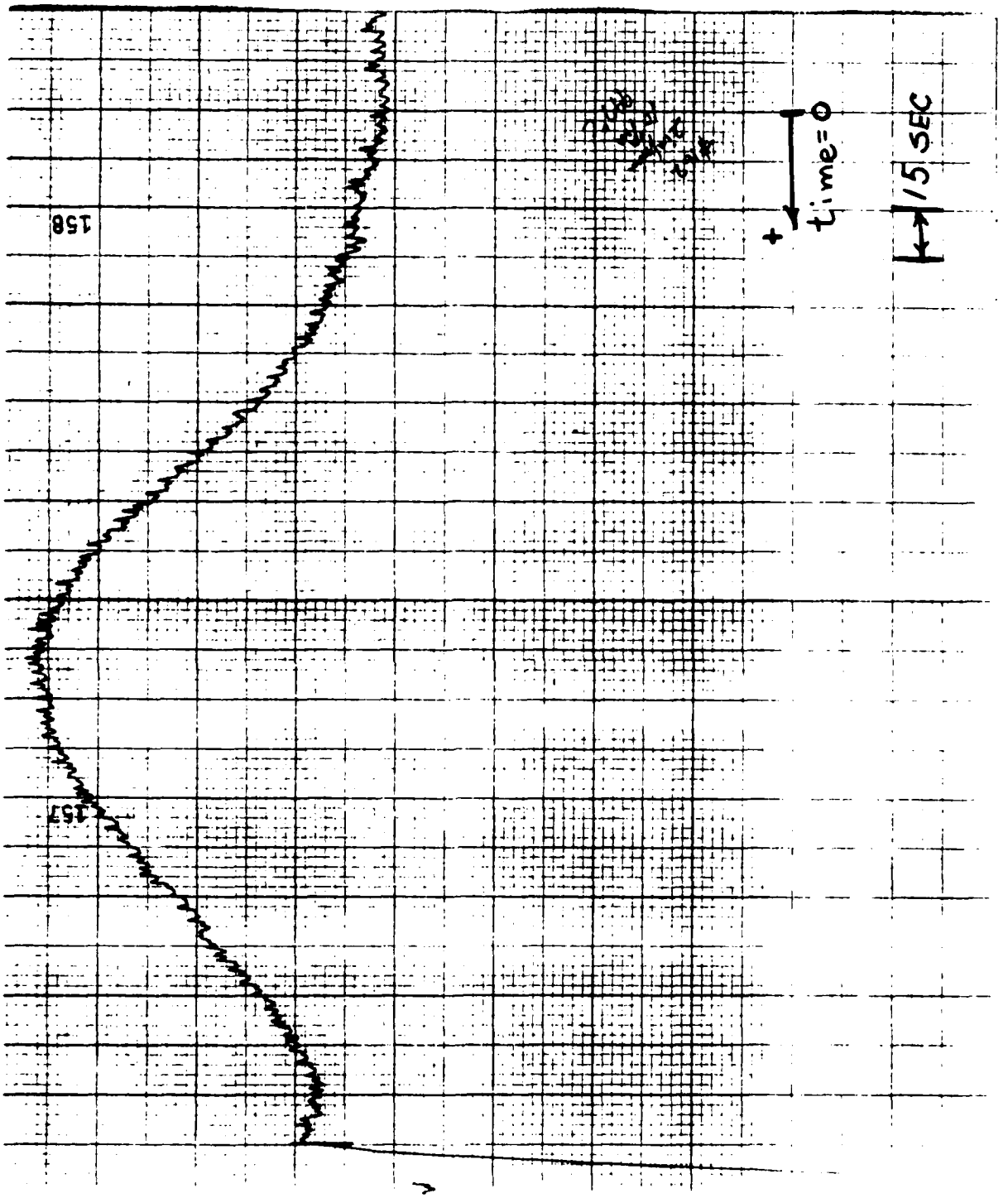


Figure 35. Oscillation Pattern of Oxide on Wafer #162.

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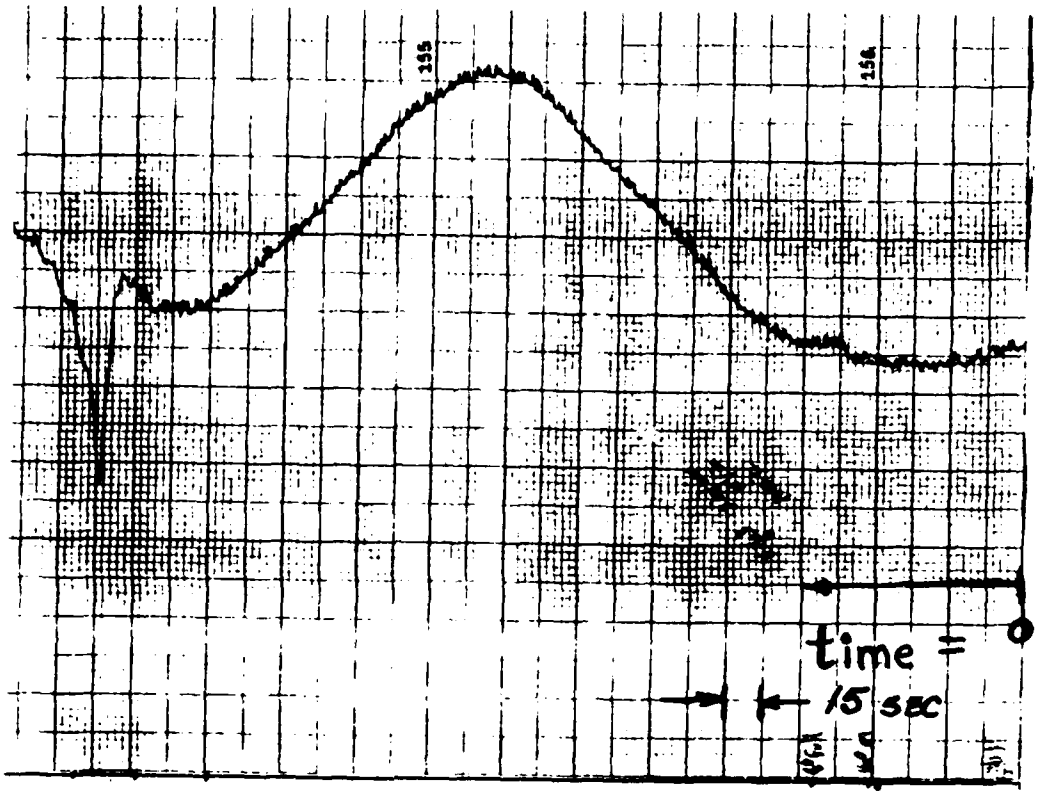

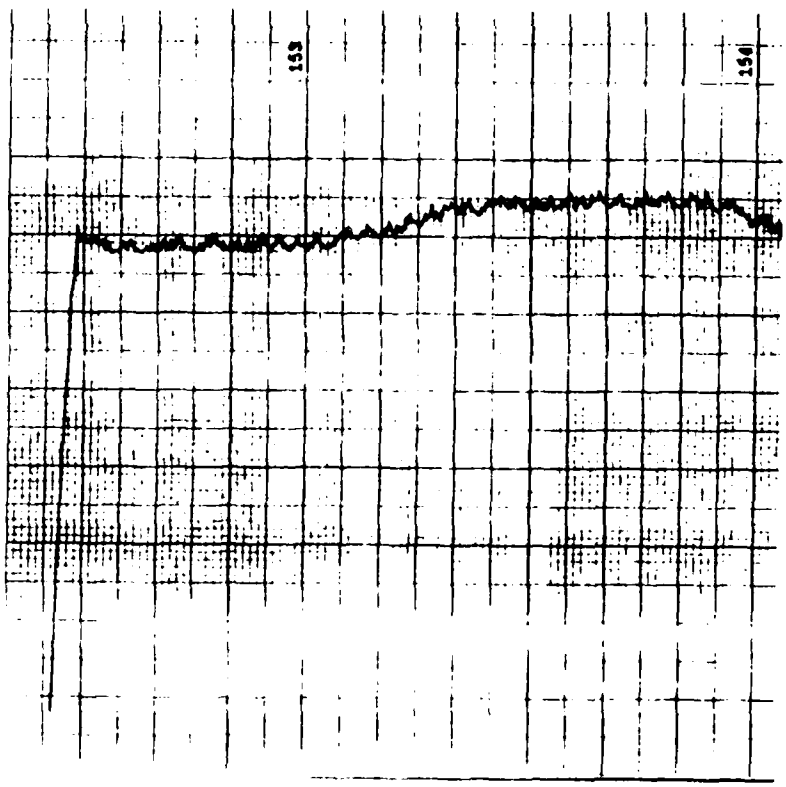

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above

Figure 36. Oscillation Pattern of Silicon on Oxide on Wafer #163.

$$\eta = \frac{\lambda}{2\ t} = \frac{0.9}{2\ (0.31)} = 1.45$$

where λ is the peak wavelength of the infrared detector. This value is the index of refraction of silicon dioxide [26].

Variations in the Initial Growth Parameters

Oxide growths were performed from 950°C to 1150°C while varying the water vapor flow rate from 600 cc/min to 10,000 cc/min in order to examine the effects on crystal quality and growth rate. Silane was kept constant at 50 cc/min and all oxides were grown for four minutes. The results of these experiments have been compiled in Tables 6 - 8.

Several combinations of growth conditions resulted in no oxide growth on the original silicon wafer. Growths occurred for Si:O molecular ratios higher than 1:1 and temperatures below 1100°C. This was expected because silicon oxide is reduced by silicon above 1100°C and thus unstable [27]. The highest growth rates occurred at 1050°C with water vapor at 1250 cc/min and silane at 50 cc/min. These results are shown in Table 6. The molecular ratio was 2:1. These wafers were very shiny with red and green color on the surface due to film thickness variations. As the molecular ratios were increased, the surface layer had an increase in silicon content becoming a dull black deposit. This deposit appeared when the Si:O ratio was greater than 4:1. This same black material was deposited on the silicon carbide susceptor.

Table 7 contains the resistivity in Ω/sq and conductivity type for each combination of flow rate and temperature. The top entry

Table 6. Results of Best Growth Conditions for Oxide. The flow rates of 0.1 % H_2O was 1250 cc/min at 1050°C.

Wafer Number	Silane (cc/min)	layers	Si:O	Surface Desc.	Growth Rate (μm/min)
192	50	$Si-SiO_x$	2:1	red and green	0.16
195	50	$Si-SiO_x-Si$	2:1	dull gray center	0.16
193	100	$Si-SiO_x$	4:1	shiny red and green	0.36
194	200	$Si-SiO_x$	8:1	dull black/yellow	0.78

Table 7. Resistivity and Conductivity Type of Oxide and Silicon on Oxide Surfaces. Top number is an oxide wafer while bottom is oxide covered with silicon. The values in the table are in Ω/sq with 'N' and 'P' corresponding to semiconductor type and an '*' corresponding to intrinsic material. The back of each wafer was doped n-type during processing.

Flow Rate of 0.1% H_2O (cc/min)	Temperature (°C)				
	950	1000	1050	1100	1150
10000		3000/N 16000/*			
5000	330/P 280/*	1800/N 3000/N			
2500	230/* 220/*	242/N 240/*	320/P. 270/P	260/P 12000/N	500/N 4000/N
1250	250/* 150/*	260/N		276/* 259/N	
625		250/N 360/N	250/* 252/*	280/N 1000/N	247/N 350/N

Table 8. Oxide Growth Rate in Micrometers Per Minute. The flow rate of SiH_4 was 50 cc/min. Note 1 refers to wafers which experienced little or no growth as indicated by the oscillation pattern.

Flow Rate of	Temperature (°C)				
0.1% H_2O (cc/min)	950	1000	1050	1100	1150
10000		Note 1			
5000	Note 1	Note 1			
2500	0.04	0.08	0.04	Note 1	Note1
1250	0.06	0.08	0.16	0.12	
625		0.12	0.18	0.16	Note 1

is for a silicon wafer covered with oxide while the bottom entry is for the silicon on oxide layer. Most of the layers were either n-type or intrinsic with resistivities in the 200-400 Ω-cm range. Several were found to have resistivities over 1000 Ω-cm.

Finally, Table 8 contains the growth rate of the oxide layer observed for both sets of wafers. The highest growth rates were found for Si:O ratios above 2:1 at of 1050°C. Above 1100°C, oxide growth was not seen due to reduction of silicon dioxide by silicon [27].

High Gas Flow and Temperature

Four wafers were prepared at 1150°C with higher flow rates in an attempt to get a deposit on the substrate. The film growth process was the same as described earlier. The data for these runs has been compiled in Table 9.

Apparently the only growth that appeared on the surface of the silicon epitaxial layer was a poly-silicon layer that looked brown and hazy. There was no oscillation pattern associated with any of these growths. Rather a totally independent mechanism caused an apparent 15°C rise in temperature. The time that it took for the temperature to rise 15°C was increasingly shorter for higher flow rates. This apparent rise in temperature was due to the roughening of the surface as the poly-silicon was being grown. The surface became more like a black body radiator thus raising the emissivity of the surface of the silicon wafer.

Table 9. Growths of Oxides at 1150°C With High Flow Rates.

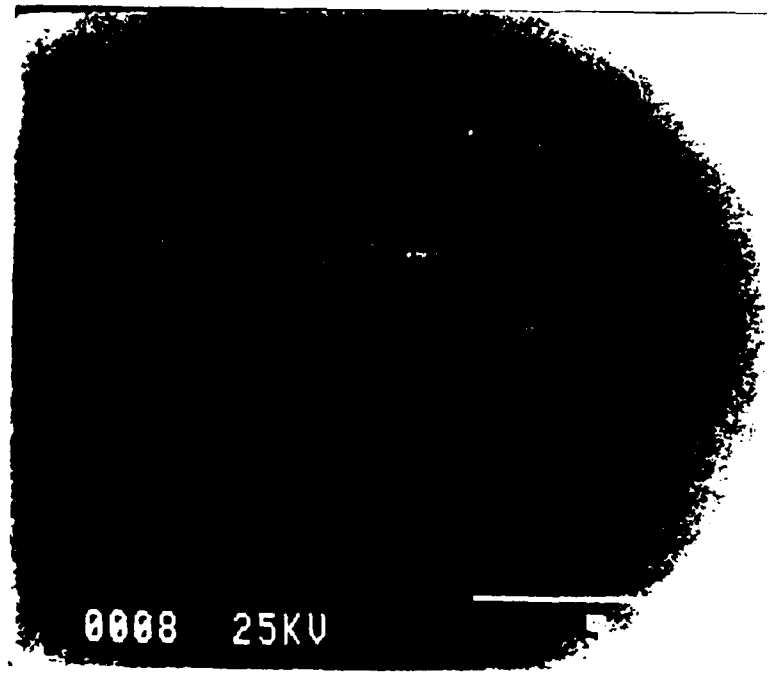
Wafer Number	Flow Rates (cc/min) 5% SiH_4	0.1% H_2O	Surface Desc.	Time for 15°C Temp. Rise (sec)
204	50	600	Shiny, no film	90
205	100	1200	Hazy spot in center	75
206	200	2500	Hazy brown spot	24
207	400	5000	Large brown spot	12

Growth of Oxide on SOS Substrates

The SOS substrate was prepared with one micrometer of silicon grown on one quarter of a sapphire wafer at 1000°C using 5% SiH_4 at 1000 cc/min. The growth rate of silicon was 2.0 μm/min. The SOS was very shiny and brown with an excellent oscillation pattern. Another wafer, #233, was prepared with the same SOS layer as #230 followed by a oxide layer grown with water vapor flow rate increasing to over 10,000 cc/min and silane kept constant at 1000 cc/min. An oscillation pattern appeared during the growth with a period of six seconds. Three and one half oscillations occurred during the 42 seconds of growth. The surface was shiny and black following oxide growth.

Electron channeling patterns were taken of the top layers of #230 and #233 are shown in Figure 37. The SOS showed very good crystal definition. The ECP for #233 was totally devoid of pattern indicating little if any crystal growth.

#230



#233

Figure 37. ECP of SOS Wafer #230 and Oxide on SOS #233.

Conclusion

It appears that our attempts to grow single crystal silicon dioxide epitaxially have resulted only in the oxidation of silicon substrates at temperatures below 1100°C and at a Si:O ratio of 2:1. At ratios above 2:1, a yet unidentified black material is deposited on the substrate. Some of the films grown below 1100°C appear shiny but no evidence has been found for single crystallinity.

References

[1]. P. Chatterjee, "Silicon-on-Insulator: Why, How and When," invited talk at 1986 IEEE Device Research Conference, Amherst, Mass., June, 1986.

[2]. K. Nonaka, C. K. Kim, and K. Shono, J. Crystal Growth, vol. 50, no. 2, pp. 549-551, 1980.

[3]. S. Sugiura, T. Yoshida, Y. Kaneko, K. Shono, D. J. Dumin, IEEE Trans. on Electron Devices, ED-32, 1985, p. 2307.

[4]. D. J. Dumin, Rev. of Sci. Instru., vol. 38, 1967, p. 1107.

[5]. Mituharu Takiqawa, et al, Japn. J. Appl. Phys., vol. 12, no. 10, pp. 1504-1509, 1973.

[6]. Mituharu Takiqawa, et al, Japn. J. Appl. Phys., vol. 13, no. 3, pp. 411-416, 1974.

[7]. Takao Takenaka and Katsufusa Shohno, Japn. J. Appl. Phys., vol. 13, no. 8, pp. 1211-1215, 1974.

[8]. K. Shohno, et al, J. Crystal Growth, vol. 24/25, pp. 193-196, 1974.

[9]. K. Shohno and H. Ohtake, J. Crystal Growth, vol. 45, pp. 187-191, 1978.

[10]. Takao Tanenaka, et al, Japn. J. Appl. Phys., vol. 14, no. 4, pp. 579-580, 1975.

[11]. Takao Takenaka, et al, Jpan. J. Appl. Phys., vol. 15, no. 10, pp. 2021-2022, 1976.

[12]. Y. Hirai and K. Shohno, J. Crystal Growth, vol. 41, pp. 124-132, 1977.

[13]. K. Shono and C. J. Kim, J. Crystal Growth, vol. 56, pp. 511-515, 1982.

[14]. C. C. Wang, et al, RCA Review, pp. 824-825, June, 1964.

[15]. V. Matkovich, Acta Cryst., vol. 14. p. 93, 1961.

[16]. R. J. Archer, et al, Phys. Rev. Lett., vol. 12, no 19, pp. 538-540, May 11, 1964.

[17]. J. R. Wasson, Gmelin Handbuch der Anorganischen Chemie, vol. 19, pp. 93-99, 1975.

[18]. S. Sugiura, T. Yoshida, K. Shono and D. J. Dumin, Appl. Phys. Lett., vol. 44, no. 11, 1 June 1984.

[19]. C. J. Kim and K. Shono, J. Electrochem. Soc.: Solid-State Science and Tech., vol. 131, no. 1, pp. 120-122, 1984.

[20]. Sze, S.M., "Physics of Semiconductor Devices," John Wiley &

Sons, New York, 1981, p. 32.

[21]. Procedure For Angle Lapping With Technology Associates Accessory 1020 & Kit 1015, Technology Associates, Portola, CA.

[22]. M. S. Abrahams and C. J. Buiocchi, Appl. Phys. Lett., vol. 27, p. 325, 1975.

[23]. D. L. Wolters, Inst. Phys. Conf. Ser., no. 50: Chapter 1, pp. 18-27.

[24]. S. M. Sze, "VLSI Technology," McGraw-Hill, New York, 1983, p. 151.

[25]. Roy A. Colclaser, "Microelectronics Processing and Devices Design," John Wiley & Sons, New York, 1980, pp. 84-99.

[26]. S. M. Sze, "Physics of Semiconductor Devices," John Wiley & Sons, New York, 1981, p. 852.

[27]. G. W. Cullen and C. C. Wang, "Heteroepitaxial Semiconductors for Electronic Devices," Spring-Verlag, New York, 1978, p. 33.

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