AD-A184 672 DRAMATICALLY IMPROVED RADIATION HARDNESS FOR CMOS SILICON GATE INTEGRATED (U) MICREL INC SUNNYVALE CA M ALTER 29 JUN 87 N00014-86-C-0436 1/1

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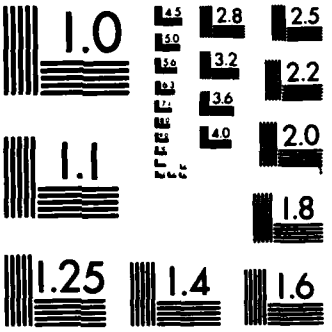

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

INITIAL TECHNICAL ABSTRACT

CONTRACT NUMBER N00014-86-C-0436
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DRAMATICALLY IMPROVED RADIATION HARDNESS FOR CMOS SILICON GATE INTEGRATED CIRCUITS EVEN DOWN TO CRYOGENIC TEMPERATURES

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This program focuses on "Field-Hardness"; specifically, the parasitic N-channel "leakages" which can result on the edge of an N-Channel transistor from source to drain, from drain of one device to the drain of another or from drain (across the CMOS P-Well) to the N-substrate (Vdd). This type of leakage normally causes device failure well before the more "publicized" gate-oxide "problem" cause Vt to drift out of spec. By butting a poly field-plate directly next to the device in the width direction (for example) we dramatically minimize the positive charge which can build up during irradiation since there is a minimal amount of oxide under this field plate; this technique is used to extend previously used concepts of using buried P+ guard-rings and special gate/field overlap layout to improve the Radiation Hardness of Integrated Circuits and has the added bonus of obviously not being sensitive to Carrier Freeze-out phenomena which degrades P+ guard-ring "usefulness" at cryogenic temperatures.

Certainly poly field-plates have been used previously for various shielding and channel-stop applications. We do not believe poly has previously been configured to represent the entire field (non-device) regions as we have done here. We have solved some basic conceptual problems here on how to contact the field plate, how to assure good process yield despite poly "nodules," how to attain good step-coverage at poly-1 edges, and how to design input and output circuits which are <u>still</u> electrostatically discharge protected. The risks with this new technology are minimized due to our comprehensive 6-quadrant test pattern design shown in Diagram 2 which allows the researcher to study numerous layout and device options as well as yield-factors and also by the use of our HCT logic die as a "yield device"; the upside potential is enormous in that we will be proving that we can take a previously non-hardened CMOS Si-gate layout and easily modify it to use this technology thus saving an enormous amount of money and also allowing designs to be quickly "produced."

What is most important for the SDIO program is that this technology is straight-forward; any existing commercial CMOS design can be readily and economically converted to this layout/process concept in a short time. The added "bonus" is the supposition that the cryogenic operation will be enhanced by minimizing sensitivity to carrier freeze-out. We are making good progress and expect masks in early January.

N-CHANNEL "BODY-CONTACT" LAYOUT OPTIONS

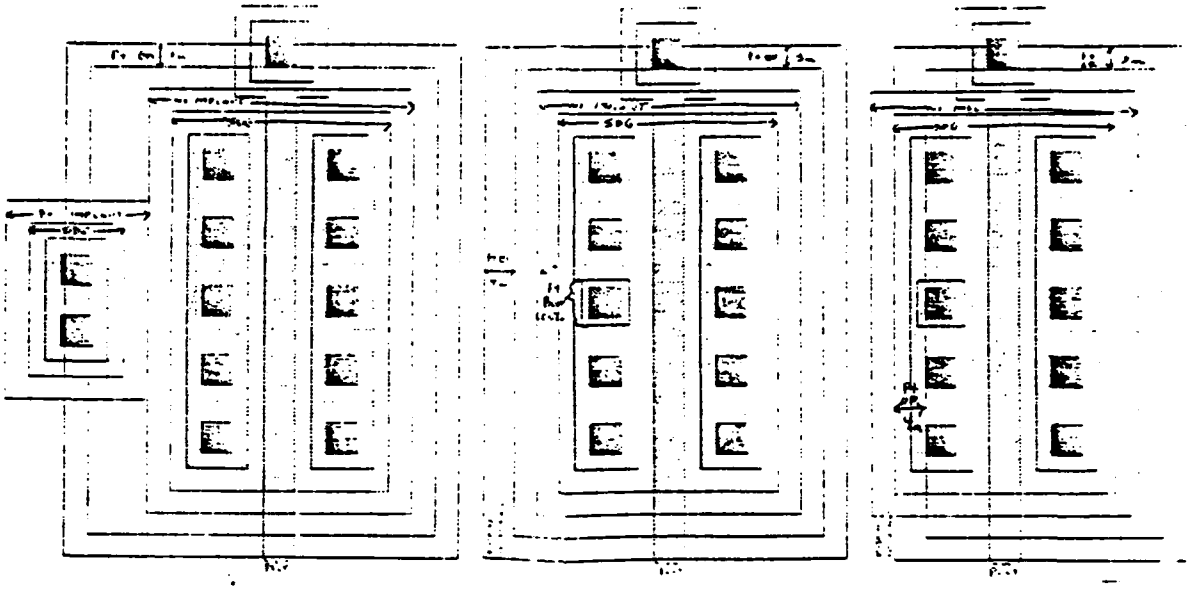

Diagram 1

One of the more subtle but critically important issues concerning layout of N-channel transistors for Radiation-Hard applications is how contact is made to the body (P-well in this case). It has been reported in The Literature that "leakage currents" tend to appear during irradiation; some of these are due to sub-threshold current which can result from a parasitic NPN bipolar transistor which uses the P-well as its "base." It is important to keep the potential as close as possible to "ground" (zero volts) so as to minimize the bipolar base-emitter junction becoming slightly forward biased and it is even more important at cryogenic temperatures when carrier freeze-out occurs. Diagram 1 shows three designs from Quad B of the test pattern which investigates some different body contact options. Most of the HCT design will use a combination of the "left-most" and "center" approaches; the "right" layout is an attempt to merge the guard-ring on the source-side to shrink the design. This "body contact" issue is one of the many aspects of this technology which is being evaluated by this mask set.

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6-QUADRANT TEST PATTERN

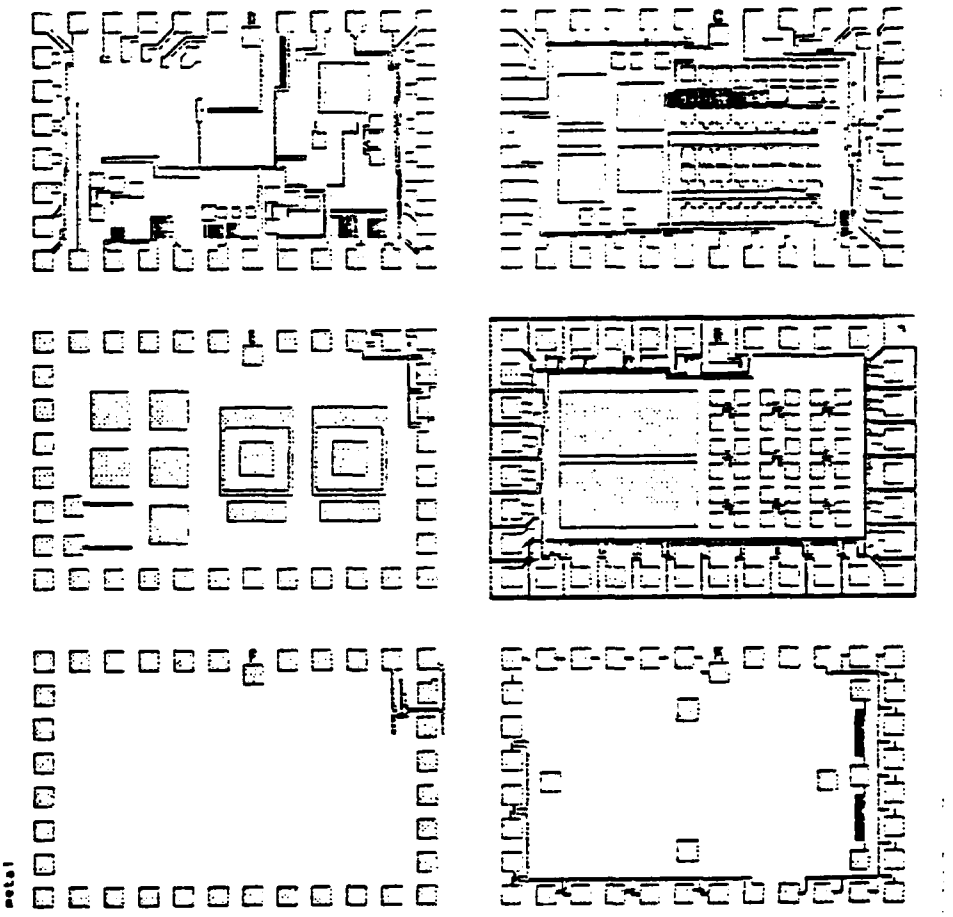

Diagram 2

Two quadrants from the HCT die (C and D) were modified for this technology and added to four others to make the 6 "quad" array shown above (only the metal layer is shown for clarity and quads E and F were not yet complete at the time of this abstract.) What is important to realize is that many aspects of a complicated issue are all being covered by this test pattern. ESD protection options are exhaustively compared on the 36 exterior probe-rings of Quads E and F to assure the products will be able to be reliably tested; in addition, various spacings, parasitic devices, topography issues, tolerances and options are designed in these and other quads. We believe that the thoroughness of this test vehicle will help ensure the success of this program and allow many questions to be answered without additional expense or time delay.

END

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