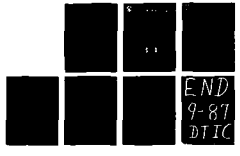
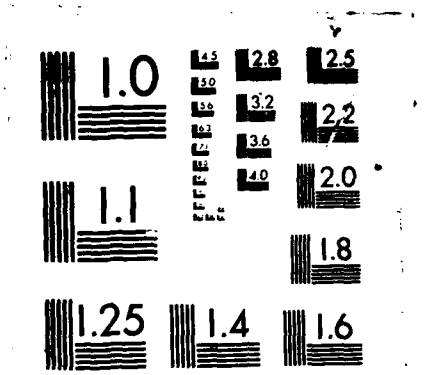
AD-A103 494 RESEARCH AND DEVELOPMENT AT CENTRE SUISSE D'ELECTRONIQUE ET DE MICROELECTRONIQUE(U) OFFICE OF NAVAL RESEARCH LONDON (ENGLAND) J F BLACKBURN 1/1

UNCLASSIFIED 05 AUG 87 ONRL-7-015-R F/G 9/1 NL





ONRL Report 7-015-R

Research and Development at Centre Suisse D'Electronique Et De Microelectronique

Dr. J.F. Blackburn

5 August 1987

Approved for public release; distribution unlimited

U.S. Office of Naval Research, London

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

A183 494

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) 7-015-R	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION US Office of Naval Research Branch Office, London 6b. OFFICE SYMBOL (If applicable) ONRL	7a. NAME OF MONITORING ORGANIZATION
6c. ADDRESS (City, State, and ZIP Code) Box 39 FPO, NY 09510	7b. ADDRESS (City, State, and ZIP Code)
8a. NAME OF FUNDING/SPONSORING ORGANIZATION 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State, and ZIP Code)	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO / WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification)

Research and Development at Centre Suisse D'Electronique Et De Microelectronique

12 PERSONAL AUTHOR(S)
Dr. J.F. Blackburn

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Technical	FROM _____ TO _____	5 August 1987	12

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Microelectronics, Materials, Integrated Circuits, Optoelectronics
09	01		
11	02		

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

The principal current scientific and technical activities at this laboratory in Neuchatel, Switzerland. Those activities are: design of integrated circuits and systems, microelectronics technology, development of custom integrated circuits, optoelectronics and peripheral components, and materials and microelectronics. Having extraordinary versatility, it is one of Europe's important laboratories.

20 DISTRIBUTION/AVAILABILITY OF ABSTRACT ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	21 ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED
22a NAME OF RESPONSIBLE INDIVIDUAL C.J. Fox	22b TELEPHONE (Include Area Code) (44-1) 409-4340 22c OFFICE SYMBOL 310

DD FORM 1473, 84 MAR 83 APR edition may be used until exhausted
All other editions are obsolete

SECURITY CLASSIFICATION OF THIS PAGE
UNCLASSIFIED

CONTENTS

RESEARCH AND DEVELOPMENT AT CENTRE SUISSE D'ELECTRONIQUE ET DE MICROELECTRONIQUE

1 INTRODUCTION

Centre Suisse d'Electronique et de Microélectronique (CSEM) in Neuchatel, Switzerland was created in 1983 through the combining of three laboratories that had been engaged in watch making, chemical sensors, and optoelectronics.

CSEM performs research and development work and small-quantity production of components and systems for industry and government agencies. The staff of 220 includes more than 70 scientists and engineers qualified in microelectronics, optoelectronics, sensors, and micromechanics. It is associated with the Swiss Foundation for Microtechnology Research in Neuchatel.

It is a nonprofit organization, subsidized by the Swiss Government and owned by about 50 shareholding companies, of which 35 percent are watch manufacturers.

The principal scientific and technical activities are:

- Design of integrated circuits and systems
- Microelectronics technology
- Development of custom integrated circuits
- Optoelectronics and peripheral components
- Materials and micromechanics.

2 DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS

Integrated Device Characterization

This activity is responsible for characterizing all devices in an integrated circuit with the accuracy required by circuit designers. P-well resistors have been characterized, including nonlinear effects and their dependence on dimensions and temperature. Other studies on polysilicon diodes and lateral bipolar transistors are underway. As an example, low-frequency noise measurements under a constant current show great improvement when the gate voltage changes from metal-oxide-semiconductor (MOS) to bipolar operation.

Device studies have been done on self-aligned complementary (SAC) MOS including translation of their MOS parameters into a simulation program, and parameter extraction including dimensional and noise effects. Test structures in the first integration include several MOS transistors, vertical and lateral bipolar transistors, Schottky diodes, and resistors.

The characterization of circuits in technology being transferred from CSEM to VLSI Technology Incorporated must be completed, especially for analog applications. Several preliminary measurements of transistors have enabled standardization of the problems. A test structure has been completed to permit a true characterization and to verify the agreement of the parameters after the transfer of the technology.

Some bipolar transistors compatible with CMOS technology have been measured and characterized in several different technologies. Their performance concerning matching and transconductance were compared in bipolar and MOS regimes. Also studied was the influence of geometry on the parameters. The equations of Ebers and Moll were extended to a more complex structure of lateral transistor. The measurements confirmed the model.

Non-Valtile Memories

Electrically erasable and programable read-only memories (EEPROM's) developed at CSEM emphasize compatibility with available CMOS technology and low supply voltage (about 1.5 volts). Small EEPROM blocks are already in use in industrial developments. The physical principle of a memory cell is a floating gate--totally isolated by oxides--and means to change its electrical charge by applying high voltage (about 20 volts) across a localized thin oxide at about 10 nm, thus, inducing a tunneling current.

The aim is an EEPROM building block in a matrix organization. Physical properties of thin oxides, injection phenomena and associated technological processes are being investigated. Several types of two-transistor memory cells have been integrated in a 4-micron technology and tested. Two of them gave good results.

An experimental circuit, including cells, interface circuits, voltage multipliers, several matrix memory blocks, and test structures have been integrated. Some manual exploratory measures, and others controlled by computer, have furnished a large amount of useful information, as well as on fault finding circuits. Functioning of several good matrix memories has been achieved with very weak power (1.3 volts).

Synthesis Program for Analog Circuits

In order to allow system designers to design optimum analog circuits, CSEM has written a synthesis program based on experience and attention to small details. Starting from a well-defined circuit diagram and from process and circuit specifications, the program provides the dimensions of all transistors and other devices, as well as the optimum bias circuits.

Program modules have been written for five different voltage references which take into account process variations and predict typical temperature behavior and worst case behavior. A few seconds of time on a VAX computer are sufficient to design a reference.

A design strategy for optimum quartz oscillators has been developed on the basis of accumulated experience and has been implemented as a new set of modules in the synthesis program.

A test program has been developed for operational and transconductance amplifiers and for voltage references. These programs run on a Hewlett-Packard computer.

It is now possible to design transconductance amplifiers (12 diagrams), operational amplifiers (4 diagrams), low-noise amplifiers using bipolar transistors compatible with CMOS technology (3 diagrams), current references (4 diagrams) and voltage (5 diagrams), quartz oscillators (3 diagrams), and analog/digital converters (2 diagrams).

A subroutine has been developed to advise the user when the program finds no solution and to indicate to him how he can improve the performance of functional blocks. The program for the interactive design of analog circuits can be used in different application domains, using low power at high frequence it determines whether the circuits are valid for the required application.

Analog to Digital Converters

Sigma-delta converters allow high resolution despite poor matching of basic circuit devices such as capacitors and transistors. They consist of a small analog part and a larger digital filter and can easily be implemented in VLSI technology.

The advantages and disadvantages of different sigma-delta A/D convertors have been studied and a strategy for design of first-, second- and third-order converters has been developed. This strategy takes into account the design of the digital decimation filter.

The stabilization of the higher order convertors is achieved by adding zeros to the loop filter. The spectrum of the quantization noise of the third-order converter shows that by doubling the sampling frequency, the signal-to-noise ratio is improved by about 21 decibels.

Digital Signal Processing Integrated Circuits

This project provides methodologies and computer aided design tools for the implementation of digital signal processing algorithms on silicon.

The decompositions of the basic algorithms made in such a way that they result in the most effective VLSI implementations. Studies were first made of basic modules generally used in digital signal processing applications. Special attention was given to very efficient VLSI multipliers, and an exploratory study was made of digital filters. CSEM collaborates with the University of Neuchatel and the Federal Institute of Technology in Lausanne in this project.

Electrical Optimization of Digital Circuits

For high performance in speed and power the behavior of digital circuits must be analyzed at the electrical level.

A large effort has been carried out at CSEM toward electrical optimization of the "microcell" matrix layout approach for designing VLSI circuits. Rules have been developed for placing and for choosing the dimensions of the transistors.

Read only memories (ROM) and random access memories (RAM), used in custom integrated circuit developments, have been optimized for access and write times without any increase in power consumption.

Automatic Layout Generation

A ROM generator has been used by CSEM for many custom integrated circuit developments. It gives freedom in the decoder and the multiplexer organization. This allows the designer to choose the best configuration in order to optimize the chip plan or minimize power consumption. Layout can be generated for the 4-µm process used by CSEM or for the 4-µm and 3-µm self-aligned CMOS process (SACMOS), with which the minimum metal and polysilicon pitch has been obtained for the ROM cell.

CSEM has upgraded the program, called CAMELEON, developed for symbolic editing and compacting. A new internal data-structure using a multidimensional tree has been implemented for providing very fast data search and operations in the plane. A new set of functions allowing geometrical operations has also been implemented, which allows the necessary postprocessing of the geometrical data produced by the compactor. These functions, which are used in other layout generation tools, are available through a library at CSEM.

Some new functions including rotating, mirroring, and copying a group of elements have been introduced. CSEM has done extensive work in documentation and interfacing of all available tools.

Automatic Synthesis of CMOS Integrated Circuits

To improve packing density and speed in VLSI circuits through abutment, a symbolic layout technique called oriented layout and based on the microcell concept is used at CSEM. Appropriate software tools have been improved and a microcell software package is available. It ranges from the topological cell description compiler to the generation of geometrically oriented layouts in different CMOS processes. It is presently applied to the 4-µm CMOS process and the 3-µm SACMOS and it gives, respectively, a metal-oriented layout and a polysilicon-oriented layout.

The microcell software package operates on a VAX/VMS computer. The above layout technique is applied in the design of industrial integrated circuits.

In assembling cells by abutment each cell must be redesigned according to its environment. Algorithms have been developed and tested to automatically generate topological cell descriptions which take account of constraints related to the shape and location of the input and output pins. Experimental programs using backtracking algorithms have been written in Prolog and Pascal languages to search for the best topologies of cells according to the given constraints. This will give a symbolic layout-oriented cell compiler, which can be used as a cell library.

A graphics editor has been developed for the interactive generation of symbolic microcell layouts. The editor has been extended to read a branch description of a cell, construct an initial placement, and allow interactive modification and improvement of that placement while retaining the connectivity. A number of algorithms to tackle combinatorial problems such as initial placement, track assignment, and optimization have been developed and evaluated. These algorithms are being built into the editor.

Testability of CMOS Integrated Digital Circuits

This project is responsible for providing a method for generating test patterns suitable for digital random CMOS logic circuits which have been structurally described.

The test patterns for CMOS circuits are more complex to generate than those for bipolar technologies. The CSEM method

provides test patterns which take into account the given sequential behavior of some typical CMOS defects. The method is suitable for all kinds of random logic circuits without reconvergence paths. CSEM has demonstrated that it is always possible to completely test each random CMOS logic circuit. In order to detect all defaults the static supply current of the circuit should be measured.

Smart Integrated Sensors

CMOS technology can be used to make sensors with negligible or no process variations. CSEM has investigated temperature and optical sensors combined with interface and signal processing circuitry.

One project was the study of a thermometric building block, comprising a temperature sensor, a voltage reference, and an analog/digital converter. Theoretical evaluations have shown that bipolar compatible structures are well suited for the first two functions, and an incremental converter with switched capacitors could be adopted for the third one. Key properties are linearity, reproducibility with a minimum of adjustments, and long-term stability.

Optical sensors have been included in two custom integrated circuits. In both cases sensors, interfaces and other critical analog circuits were studied analytically, simulated, and measured. They performed as expected.

3 MICROELECTRONICS TECHNOLOGY

Processing Technology

The Swiss National Research Program No. 13 is sponsoring at CSEM the development of an advanced 2-µm CMOS technology. The features of this technology are self-aligned source and drain contacts, the formation of silicides for the polysilicon and diffusion intersections, the compatibility with a low doped drain configuration, and the incorporation of electrically erasable and programmable memory cells (EEPROM's). The different features are combined in the CMOS technology. Low power, high density and high speed for digital and analog circuits are the expected results. The feasibility of the concept was established by investigating a number of key elements of the fabrication process and designing a test circuit containing all the new elements of the technology. The mask set, now available, allows characterizing and optimizing all processing steps and establishing the relevant technological parameters.

A crucial feature of the self-aligned contact process of CSEM is the formation of the lateral isolation of the polysilicon gate. They have chosen a low-temperature process, where the lateral sensors are obtained by the conformal deposition of an oxide. The etching of the oxide-covered silicon, the low-temperature oxide deposition, and the anisotropic etching of this oxide are the three critical steps.

Another key element is the EEPROM memory cell, where the isolation of the two polysilicon layers, representing the floating gate and the control electrode, and the characteristics of the thin injection oxide have been studied. The formation of silicides, calling for sputter deposition of a thin titanium layer and a rapid thermal annealing step has also been investigated.

Over the last several years the two-dimensional process simulation program, SESAM (semiconductor simulation program applied to MOS technology), has been developed. It is based on the finite element method and simulates plane and non-plane substrate surfaces. The main steps in integrated circuit fabrication, such as ion implantation, layer depositions, coupled diffusion of one to three impurities, oxidation, and etching processes can be subsequently simulated. The latest version features a simple model for etching and the possibility of choosing one of three options for the simulation of thermal oxidation:

- An analytical model for fast evaluations
- A physical model that involves the diffusion of oxidizing species in the SiO_2 layer and an elastic type of model to determine the shape charge of the layer due to chemical reaction of silicon with the oxidizing species

- The time-dependent shape change of the oxide layer taken from a file containing precalculated oxide growth simulation data.

Another activity at CSEM is the characterization of dedicated dry etching equipment and the process optimization for patterning the Al/Si metallization layer. The process has been introduced in pilot line production.

Integrated Circuit Fabrication

Seven centers of processing competence have been created: deposition of dielectric layers, photolithography, plasma dry etching, metallization, ion implantation, metrology, and computer assisted line management. The latter activity is instrumental in assigning priorities to fabrication runs, tracing lots, and keeping track of in-process measurements and final parameter measurements.

About 3000 wafers, corresponding to more than 50,000 integrated circuits, have been processed. Also, a limited number of process steps has been performed on some 4000 wafers in relation to chemical and physical sensor development and production work and fabrication equipment evaluation. A 4-μm double polysilicon technology has been used predominantly. A significant contribution was made to the development of a two-transistor EEPROM cell, which is relatively insensitive to technology parameter variations.

Quality Control and Failure Analysis

Voltage contrast analysis, in some cases collaborated by infrared microscopy, has been successfully applied to localize areas of malfunction on an integrated circuit chip. Analysis of reliability has led to an improvement in the integrity of the glassivation layer above the aluminum interconnection level.

Stains on the aluminum bonding pads that would affect bond reliability were identified as to origin and chemical composition by Auger electron spectroscopy.

New equipment, recently introduced, allows nondestructive decapsulation of epoxy-packaged integrated circuits. This equipment can be used to selectively remove certain layers on chips. For the French company, Electroniques Serge Dassault, a comparative reliability study was made of 5V/64 kbit EEPROM's from various sources, primarily for operation at high temperatures.

Electron Beam Lithography

An application that is of growing importance is that of masks for integrated optics, usually waveguide structures and associated electrode patterns. Special attention is given to properties such as edge activity, edge continuity, and slope continuity. Neither the writing strategy of pattern generators, nor the standard CAD techniques are really suitable for these requirements. The exposure of beam spots in a fixed raster, and in appropriate digitizing on a high-resolution grid leads to very large data files without improving writing performance. CSEM has developed a special digitizing tool that takes into account the known system limitations and prepares the data in a compact, machine-compatible form. It has proven quite successful and will be incorporated in a complete data processing package.

Diffraction Grid Fabricated for Hipparcos Astronomy Mission

The Hipparcos Astronomy Mission will rely on a telescope launched on a satellite in 1988 by the European Space Agency. The Fourier transform of star images crossing a grid pattern allows accurate star position measurements to be performed--if high-resolution microstructures can be manufactured on an optical lens.

CSEM has generated patterns on nonflat substrates by electron-beam lithography in conjunction with chromium mask-making techniques. The Hipparcos pattern consists of a main grid and several auxiliary patterns, all located on the spherical side (radius 1400 mm) of a quartz block. The main grid consists of 2688 transparent slits, 3.2 μm wide and 22 mm long, with a pitch of 8.2 μm. The auxiliary structures include a number of slits, some of them being inclined

45 degrees with respect to the main grid slits and several markers used as references for optical transmission and alignment. The high performance required for accurate registration and for critical dimension control of the patterns at the 1/10-μm level led to the implementation of a dedicated writing strategy. It was necessary to provide extended compensation for substrate height differences on beam focus and deflection parameters. Also, a special calibration software package for the pattern generator was developed in order to make available a measuring tool with extended submicron capability.

Physical Sensors

An original concept for capacitive silicon sensors is the basis for development in pressure-acceleration-force and magnetic field sensors. The physical quantities to be measured cause the deflection of a movable electrode, which gives rise to a variation of capacity with respect to a fixed counterelectrode.

The capacitance sensor is used in an ultrasensitive accelerometer being developed by CSEM for the European Space Agency (ESA). It consists of a plate, suspended by a pair of torsional bars, and a fixed electrode on each side. Acceleration values as low as 10^{-6} g unit have been measured, demonstrating the suitability for microgravity applications.

A 3-axis accelerometer system, developed for ESA, will be used in a zero-gravity experiment on parabolic airplane flights.

Capacitance pressure sensors allow precise absolute pressure measurements, using an integrated miniaturized reference pressure chamber with volume of the order of 0.02 mm^2. A sealing technique was developed at CSEM allowing residual pressure below 5 millibars to be reached. The dynamic range of the sensors is typically higher than 10^4, resulting in a resolution of 0.1 millibar at 1 bar. Pressure sensors with temperature coefficients below 50 ppm/°C have been built.

A switched capacitor CMOS oscillator chip, developed at the Federal Institute of Technology at Lausanne and fabricated at CSEM, has been successfully tested in a system incorporating a CSEM pressure sensor.

Thin Film Sensor for Heat Flow Measurement

To obtain an inexpensive, flat, heat flow meter, an industrial development was made starting from copper-constantan thermoelectric flow meters developed at Lille University, France, which can be manufactured with printed circuit technology.

The double-sided sensor consists of a Kapton foil with thermoelectric cells connected in series. They are made of two thin layers of copper and constantan, asymetrically structured so that a heat flow perpendicular to the cell will produce a thermal gradient parallel to the x-axis. The cells on one side are arranged top to bottom with respect to the cells on the other side. The sum of these contributions along each constantan ribbon gives rise to a thermoelectric voltage which is proportional to the heat flow perpendicular to the film surface.

Nuclear Radiation Detectors

In the process of examining silicon microstrip detectors for CERN, Geneva, CSEM found a novel analysis method called back-EBIC (electron beam induced current). This method allows sensitive detection, and in some cases three-dimensional localization, of deeply buried recombination centers in silicon.

A new detector structure having the potential for lower radiation damage sensitivity has been developed, and prototypes are being built.

Optical Detectors

The objective of this project is to integrate on the same chip customized photodetectors and arrays with signal processing electronics.

Optimization of the spectral response for a particular wavelength or for a range of wavelengths and the elimination of undesirable interference was achieved by adjusting the oxide layer thickness within the photo-modification

of the basic CMOS technology, leaving the circuit areas unaffected.

4 DEVELOPMENT OF CUSTOM INTEGRATED CIRCUITS

A custom integrated circuit for instrumentation was developed by CSEM for a French company. It consisted of two integrated circuits to be used in a novel, absolute, or incremental optical encoder with programable multiresolution. The circuits contain optical sensors (photodiodes), analog interface electronics, and digital signal processing circuits implemented on the same chip.

Another application, developed with a Swiss company specializing in colorimetry, involves a circuit to measure the color spectrum of any sample between 400 and 700 nm, with a 128-channel resolution and a dynamic range of 80 dB. The chip consists of photo diode sensors and analog and digital circuits.

To develop circuits for watch applications microprocessor architectures of the reduced instruction set computer (RISC) type were used. They minimize power consumption by forcing the processor into a halt mode when it has no specific task to accomplish. Test problems were solved by implementing an additional block onto the circuit, enabling both the complete ROM contents to be read and instructions to be injected to test each of the processor blocks separately. The time required to draw the layout has been drastically reduced by using CAD methods and tools developed at CSEM.

In medical electronics CSEM is implementing for a Swiss customer a system distributed over four chips, of which three are analog and the fourth is digital and contains nonvolatile memories. This system uses low noise and variable gain amplifiers, programable switched-capacitor filters, and compression-expansion circuits comprising translinear loops.

5 OPTOELECTRONICS AND PERIPHERAL COMPONENTS

Referencing of Intensity Modulated Fiber Sensors (IMFS)

Although IMFS can not compete with interferometric fiber sensors in accuracy, dynamic behavior, and resolution, their simplicity makes them suitable for low-requirement sensor applications. A main difficulty is the separation between fiber losses induced by the transducer and losses on the fiber lead, as well as source fluctuations.

To get rid of source fluctuations, an original referencing design has been demonstrated in which the transducer is placed within a fiber cavity made of two semireflecting fiber mirrors. A low-coherence semiconductor source is amplitude-modulated at frequency Ω. The effect of the cavity is to convert the transducer-induced attenuation into a phase change of the frequency component of the signal returning or proceeding to the detector. As opposed to its modulus, the phase of the Ω-component travels unperturbed down the lead and will not be affected by source fluctuations as long as the Ω-component has a time constant lower than that of the fiber cavity.

An experimental demonstration has been performed with a distance or proximity sensor, where the transducing mechanism used is the relative amount of optical power reinjected into the fiber core by the surface of a moving object placed in front of the fiber tip.

Optical Time (Frequency) Domain Reflectometry and Fiber Sensors

Such sensors are widely used in fiber optics for fault location and identification along a fiber. The echo of the input pulse on local and distributed obstacles represents the impulse responses of the fiber. The tool is well adapted to a time-multiplexed interrogation of a number of sensors placed on a single fiber line since it achieves a good cost/performance ratio.

The application of radar techniques in fiber optics has led to increased interest in noncoherent optical time domain reflectometry and fiber sensors. Scanning the AM frequency of the source and measuring the overall echo delivers the fiber transfer function. From it, with the advantages of modulation and detection simplicity for high spatial resolution, fiber line properties and local faults can be localized and identified.

Theoretical and experimental comparisons of the above approaches have been made at CSEM in order to define their domain of use in fiber sensors. Compact, dedicated electronic modules have been fabricated, allowing a rapid assembly of any type of distributed sensor system.

All-Fiber Components

A batch production technique has been developed at CSEM which allows the collective polishing of a number of fibers lying on an anisotropically etched single-crystal silicon wafer. The building block of the family of all fiber components is a "half-coupler," obtained by tangential polishing of the fiber.

A single-mode fiber coupler is obtained by assembling two polished sections. The wavelength dependency of the coupling coefficient offers a way of getting a specific spectral behavior. CSEM has obtained a coupler which can be used as a two-wavelength (de) multiplexer with insertion loss lower than 0.5 dB. A wideband coupler has also been obtained showing a 10 percent variation of the coupling ratio over the full 1.3- to 1.6-μm wavelength range. Multiplexing of a 0.8- and 1.3-μm wavelength in a single-mode fiber coupler has been demonstrated.

Polishing a single-mode fiber close to the core gives access to the modal field, which opens a new domain to fiber sensors using guided wave total reflection spectroscopy. Small optical sensors for biomedical applications can be designed. CSEM has demonstrated a guided wave refractometer which allows nonambiguous measurement of physical quantities affecting the refractive index of a liquid or a plastic surrounding the polished filter section. For example, a temperature measurement yields a 0.1°C accuracy over a 50°C adjustable range with very short response time.

Technologies for Integrated Optics

"Ion exchange in glass," is a technique for optical waveguide fabrication. Single- and multimode waveguides with a wide range of numerical apertures can be obtained, allowing the design and fabrication of a wide variety of passive optical circuits. Silicon technology offers excellent waveguiding dielectric layers useful for optoelectronic integration including optical interconnections on integrated circuit chips. CSEM has concentrated on mask writing, ionic mask deposition, etching, and waveguide characterization.

Optical System for Laser Pattern Generator

CSEM developed a system which simultaneously focuses a red (λ=633 nm) and a blue (λ=442 nm) laser beam on the surface of a preprocessed wafer which consists of integrated circuits with standardized structures. Personalized chips can be manufactured by cutting electrical connections in the top metal layer. This is done by exposing a positive photoresist at the locations of electrical disconnections with the focused blue laser beam. The red laser beam is used for the recognition of the basic structure. Exposure is synchronized from this information. The focus spot size is about 2 μm for the blue laser beam and about 3 μm for the red laser beam.

Holographic Optical Elements for Semiconductor Lasers

Holographic optical elements used with semiconductor laser sources must be fabricated at a wavelength different from the application wavelength, since there are no holographic recording materials available for the infrared range. The aberations due tc the wavelength change between the holographic recording and reconstruction can be eliminated by using aspheric waves for the holographic optical elements formation. Ray-tracing methods were employed at CSEM to evaluate the aberration corrections and the shape of the registration wave fronts. The aspheric waves needed for the holographic optical elements recording at a wavelength (λ) of 488 nm were produced by a computer-generated hologram. Holographic optical elements with no geometric aberrations were obtained at λ=790 nm by the techniques described.

Micropositioning System for Guided Wave Optics

A monolithic 2-axis microtranslator stage was developed at CSEM to meet the exacting alignment specifications required in the field of monomode integrated optics. This unit gives very high resolution, reproducibility, and linearity in the submicron range. Its design relies on a systematic application of purely elastic links for the guidance and the transmission of movements. CSEM also developed electronic units to display, control, and automatically optimize the position coordinated, based on digital and analog circuits.

Quartz Resonator

Industrial prototypes of a miniature quartz resonator at 2.5 MHz, sealed under vacuum in a small, ceramic package have been delivered for evaluation to the Centre National d'Etudes Spatiales (CNES) in Toulouse, France. They are intended for use in distress beacons for maritime, aeronautical, and terrestrial applications where a small volume is essential to limit the power drive of the thermostat, in relation with the satellite-aided search and rescue program.

For this program two problems had to be solved: (1) modification of the typical frequency-temperature characteristics, so as to shift the upper inversion temperature toward 70 to 80°C, a convenient range for thermostatic operation, and (2) precise frequency adjustment, to within ±10 ppm, by means of a laser beam.

Surface Acoustic Wave Resonator

Surface acoustic waves are high-frequency mechanical waves in the frequency range of 0.1 to 2 GHz, which propagate on the highly polished surface of a piezoelectric crystal, usually quartz or lithium niobate.

These devices generally consist of two metallized interdigital transducers defined on the crystal surface by thin-film methods. Each transducer is composed of a network of metal electrodes with alternating polarity. The first transducer converts the electrical input signal into a surface acoustic travelling wave. It is then reconverted into a voltage by a second transducer.

The first surface acoustic wave device made at CSEM was a resonator, as it is more technology dependent than a filter. Using quartz substrates the resonator frequency is nearly 800 MHz, which leads to 1-μm metallization gaps and widths ($\lambda/4$).

The resonator consists of a pair of interdigital transducers flanked by two reflectors which confine the mechanical energy.

Integrated Electrochemical Sensors

For investigation of the fabrication of a fully integrated electrochemical sensor CSEM has developed an Al_2O_3-gate ion-sensitive field effect transistor (ISFET) technology. A process for pH-sensors compatible with on-chip CMOS associated electronics is now available.

Thin-film deposition techniques were developed for the fabrication of a silver/silver chloride (Ag/AgCl) miniaturized reference electrode which can be combined with ISFET structure. A stable electrochemical potential was obtained on an Ag/AgCl planar structure which employs a localized and isolated KCl-saturated hydrogel. A new approach was investigated at CSEM to isolate the reference electrolyte in a cavity made from the silicon bulk and to provide a liquid junction by means of a porous silicon membrane. The response of ISFET's combined with an integrated reference electrode show essentially the same behavior as those with a microscopic reference electrode, such as a standard calomel electrode.

The pH ISFET sensors show a reproducible sensitivity of 54 3-MV/pH. Long-term stability tests show low drift, typically 0.2 MV/hour after several hours in solution. Control electronics has been designed and constructed using a feedback circuit to operate pH-ISFET sensors in a constant current mode.

Miniaturized Oxygen Sensor

Using Ag/AgCl thin-film deposition techniques, a miniaturized "Clark cell" structure was implemented on a silicon substrate using a 0.04 mm^2 cathode and 0.5 mm^2 Ag/AgCl anode.

A poly-HEMA hydrogel layer was deposited to provide a liquid junction between the electrodes, and a silicon-rubber membrane permeable to oxygen was used to cover the structure. The device is potentially a well-controllable oxygen sensor. A sensitivity of about 4.5 nA/torr, calculated from the voltametric experiments and confirmed by chronoamperometry, was demonstrated with good reproducibility and stability within a test period of 2 weeks.

Gas Sensors on Silicon

A Si/SiO_2 substrate for a semiconducting oxide (SnO_2) gas sensor was developed to achieve a device with precisely controlled temperatures and working at the lowest possible power level. Selective etching of silicon was used to remove silicon from beneath chemical-vapor-deposited SiO_2 membranes, which provide good thermal isolation. Thin-film deposition techniques were optimized to produce the resistive heater, the electrical isolation and the sensitive semiconducting film. The structures can withstand repeated thermomechanical stress.

The first series of prototype devices tested for CO gas measurements in air showed various sensitivities dependent on the final treatment of the SnO_2 layer after deposition. The sensitivity and reproducibility of the SnO_2 film is improved by heat treatment in specific gaseous environment. Thermal loss modeling experiments show that the integrated sensor can operate up to 400°C with less than 150-mW heating power.

6 MATERIALS AND MICROMECHANICS

Ultra-Microhardness Tester

The principle of the ultramicrohardness tester under development at CSEM is based on the direct measurement of the indentation depth. This is achieved by capacitive displacement detection and is more precise and reproducible than conventional methods, which include the human factor of evaluation of the indentational diagonal.

The goal is to measure indentation depths of 0.1 μm with extremely light loads. This should allow thin coatings to be characterized, since the higher loads conventionally used interfere with the substrates.

Hard and Tough Coatings With Low Atomic Numbers

The R&D work on this project is directed toward producing coatings and improvements in toughness adhesion and resistance to wear, sputtering, and hot corrosion. The application of such coatings on components inside the TOKAMAD (nuclear fusion) reactor, such as limiters, antennas, and walls requires materials of low atomic number.

To increase the toughness of extremely hard coatings, toughness regulators in the form of a fine dispersion (<1000 Å) or microluminar phases have been incorporated in the matrix material. Work is also underway on coatings consisting of solid solutions of Ti(B,N), Ti(B,C), or Ti(B,C,N).

Chemical Vapor Deposition of SiO_2 and TiO_2

Amorphous, largely stress free, SiO_2 coatings are obtained at temperatures below 800°C by the thermal decomposition of tetraethylorthosilicate (TEOS) in the presence of small amounts of water vapor. Such coatings, between 5 and 8 μm thick, can be used to prevent corrosion by liquid and gaseous products and to protect metallic components in analytical instruments. The critical points in the process are the formation of the intermediate oxide layer and its adherence to the metallic substrate. Work at CSEM has consisted of finding a specific wet or gaseous process for each type of substrate.

Coatings of TiO_2 have potential application in bioengineering and in sensors. TiO_2 deposition is done by thermal decomposition of tetraisopropoxyltitanate (TIPT) at temperatures below 400°C. Substrates including Ti, Al, and Cu and their alloys are of interest at CSEM. Development work has concentrated on eliminating TiO_2 powder formation, on controlling grain size and TiO_2 coating stoichemistry.

Solid Lubricants--Chalcogenides

The coating of molybdenum disulfide (MoS_2) obtained by the PVD process of Microslide (R) developed at CSEM has been successfully tested for the lubrication of space mechanism. However, the performance of MoS_2 lubricating layers is limited due to its poor resistance to humidity; a topic that has been investigated at CSEM.

Complex MoS_2-based coatings have been evaluated including Au, polytetrafluoroethylene, and BN codeposited with MoS_2; Rh, Pd, Ni, and Co have been found to be valuable interlayers. By examining the morphology and the tribological properties of the modified materials, it was found that MoS_2-Au coatings provide higher wear resistance in vacuum and dry air conditions. Systems using a rhodium interlayer and running against monocrystalline ruby, with either MoS_2 PTFE or MoS_2-Au as the lubricating agent, show an important improvement in tribological behavior at high humidity.

The performance of bulk bearings with sputtered MoS_2 lubrication has been studied. TiC-coated balls provide a lifetime increase of a factor of 3 over standard steel balls, when MoS_2 lubrication is present, together with very low torque. Eventual failure of the MoS_2 film maintains the torque within acceptable limits due to the TiC.

Galvanic Deposition of Silicon from Nonaqueous Solutions

The purpose of this project was to achieve galvanic deposition of silicon from nonaqueous solutions, because of its chemical instability in classical electrolytes. Recent effort has been on improving the morphology of the layers and on decreasing the impurity content. Deposits up to 20 cm^2 in size have been obtained. Their quality does not depend on substrates such as Pt, Au, Cu, or Ni--on all of which they adhere well. Adherence on carbon is not yet satisfactory. The films are smooth and without imperfections as observed on a scanning electron microscope, when their thickness is below 0.25 μm. Thicker films show cracks.

A further objective is to obtain crack-free deposits up to 1-μm thick and if obtained to investigate their physical properties and potential cost.

Characterization of Ceramic-Type Thin Coatings

Ceramic-type coatings are used to solve tribological and corrosion problems, especially in hostile environments. The characterization of such coatings is important for establishing relations between the deposition conditions and the mechanical properties of the film.

A study has been made at CSEM of the stresses to chemical vapor deposition (CVD) and physical vapor deposition (PVD) coatings of TiC, TiN, and HfN. This study has shown that:

- A rather low tensile stress is observed in CVD TiC and TiN coatings on cemented carbide
- A medium compressive stress is observed in CVD HfN coatings on cemented carbide
- A medium compressive stress is observed in CVD TiC, TiN, and Ti(C,N) coatings on stainless steel and on high-speed steels
- A high compressive stress is observed in PVD TiN, Ti(C,N), and HfN coatings on stainless and high-speed steel.

Also, the presence of shear stresses and of stress gradients have been detected in the films.

7 CONCLUSIONS

CSEM is a laboratory of extraordinary versatility for its size. Its total staff of 200, of whom about 70 are professional physicists, electrical engineers, and chemists, covers in great depth five major fields: systems and circuits, microelectronics, application-specific integrated circuits, optoelectronics, and materials and micromechanics.

It numbers among its clients some of Europe's most prestigious laboratories and agencies--e.g., CERN, European Space

Agency, Dassault Electronique, and Ecole Nationale Supérieure d'Ingenieurs Electriciens in Grenoble.

Its talented professional staff and effective management mark it as one of Europe's important laboratories.

8 REFERENCE

Rapport Scientifique 1985-1986, (Centre Swisse d'Electronique at de Microtechnique, Maladiere 71, Ch-2007: Neuchatel, Switzerland).

END

9-87

DTIC