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TEMPLATE-SET APPROACH TO DEFECT DETECTION AND
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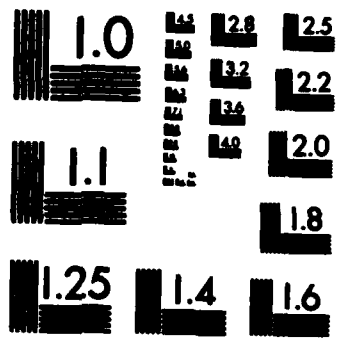
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Template-Set Approach to Defect Detection and Classification for VLSI Patterns

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Automatic inspection of VLSI circuit patterns on photomasks and wafers is increasingly important as the minimum feature size decreases. Real-time inspection at the standard video rate is demanding because the volume of information in VLSI circuits patterns is enormously large. Similar to printed wiring board inspection[1], the goal of VLSI pattern inspection is not only to detect defects, but also to automatically interpret defects for patterning process analysis and control, which is essential to manufacturing automation. However, die-to-die or die-to-database comparison methods employed in most state-of-the-art VLSI pattern inspection systems have only defect detection capability. Simultaneous detection and classification of defects in real time has been challenging because of the complexity of computation required in statistical and syntactic classification methods[2]. We have developed a new approach based on template matching of local binary images with content-addressable memories (CAMs), which can easily be implemented in VLSI circuits because of its modularity and regularity. In a work reported previously[3], this approach was applied primarily to defect detection. Here we focus on its application to defect classification and its system implementation in VLSI circuits.

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While VLSI circuit patterns are complex globally, they are simple and regular locally. As a result, defects can be detected and classified by comparing only the local pattern to properly designed template sets. Each template set represents the local characteristics of a particular category of defects. The size and shape of the window which extracts local patterns from the sensed image must be chosen appropriately so that all possible defect can be completely covered with a manageable number of templates. Don't-care conditions are incorporated in the templates to tolerate an edge roughness of one picture element (pel), which is usually caused by quantization errors. This strategy substantially reduces the number of required templates. Templates are stored in the content-addressable memory for high-speed comparison because the CAM allows comparing a window pattern to all templates in parallel, and the use of maskable CAM cells (Figure 1) further makes don't-care conditions easy to program.

A template consists of two words: a *pattern word* and a *mask word*, each having the same number of bits as the number of pels in the window pattern. If a bit in the mask word is set to one, its position is not included in the comparison during match operation. Thus a match between a window pattern and a template occurs whenever the window pattern and the template pattern word are identical at all bit positions whose corresponding bits in the mask word are not set to one. The window pattern is considered as containing a defect represented by a template set if it matches any template in that set, and acceptable if no match occurs in any template set. Therefore defects can be detected and classified simultaneously by using this technique. Note that no computation is involved besides the comparison of the window pattern to the templates.

The VLSI architecture for this template-set approach has two distinct functional blocks: windowing and matching. The windowing block forms a two-dimensional window pattern from

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delayed serial signals of several horizontal lines of image, and basically consists of a set of shift registers. Its outputs are connected to the bit lines of the CAM array in the matching block. The *match line* for a template is connected, in a wired-AND logic, with all match lines of its maskable CAM cells. Because there is a match line for each template, the *match output* for a template set is the output of an OR operation on all match lines of templates in the set. Figure 2 is the block diagram of an inspection system. Depending on the size of the window, one or more template sets can be integrated in an IC.

Figure 3 shows the simulation result of inspection on a binary SEM image of contact-hole patterns in photoresist. Protrusion, pinspot and pinhole defects, which did not exist in the original image, were added deliberately to facilitate a more comprehensive test. The minimum feature size in this case is 10 pels, and a 7×7 square window was chosen in the simulation, which can detect width and gap errors up to 5 pels in size. Six template sets were employed for protrusion, intrusion, pinhole, pinspot, width error, and gap error, respectively, with a total of 102 templates. As indicated in the figure, all defects in the image have been detected and classified correctly.

This approach is very flexible because each template set can be modified easily with a simple "write" operation. Furthermore, with don't-care conditions, the number of templates in each set is substantially reduced, the false detection problem from acceptable edge roughness is solved and the shape of the window can be programmed. The proposed system can operate in real time at a standard video rate because CAMs capable of 50 ns cycle time can be designed with a 2 μ m double-metal CMOS technology.

Acknowledgment

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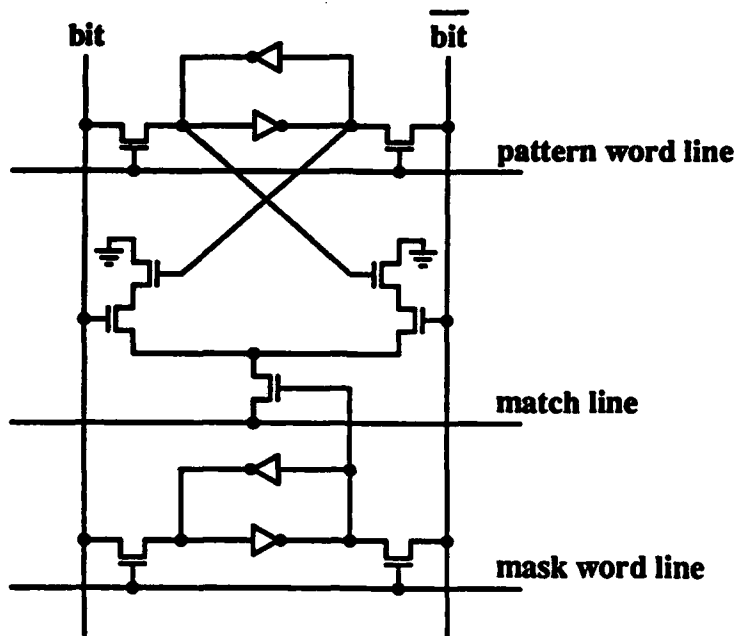


Figure 1. Circuit diagram of a maskable content-addressable memory cell.

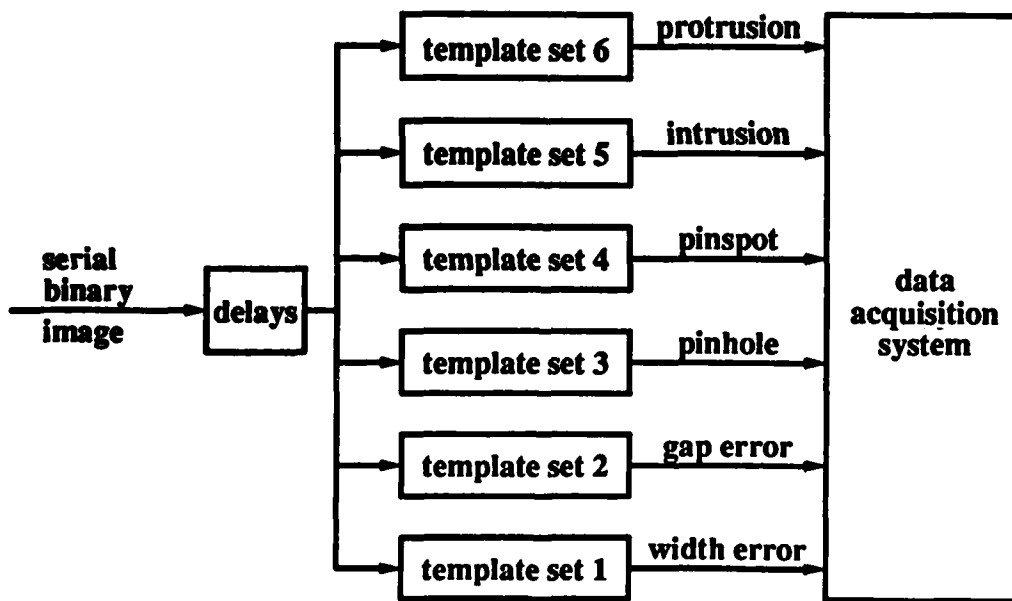


Figure 2. Block diagram of an inspection system. The template set for each type of defect is a separate IC, or several of them could be in the same IC.

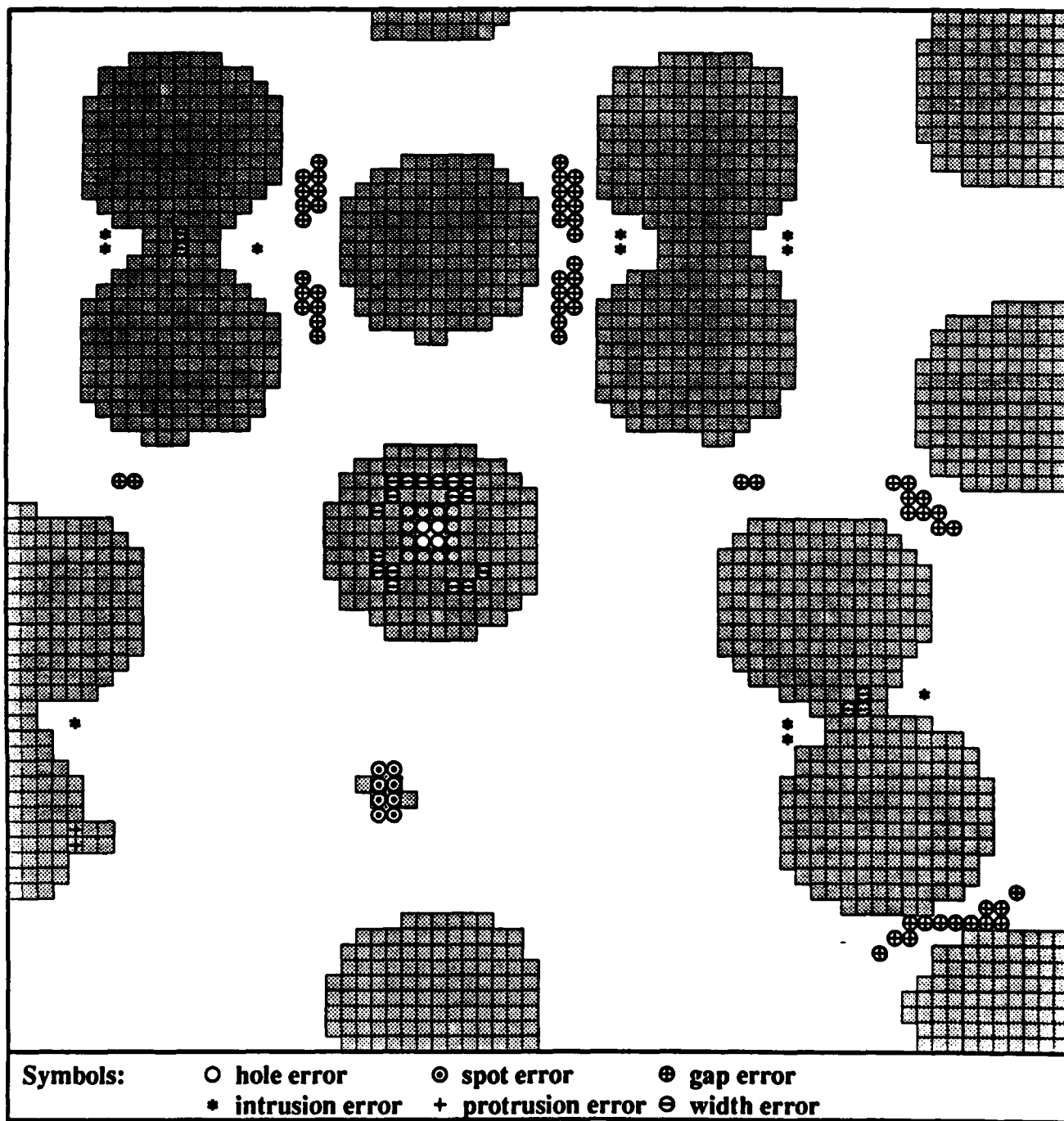


Figure 3. Simulation results from a SEM image of contact-hole patterns in photoresist. In this simulation a 7×7 square window is employed and the minimum feature size is 10 pels. The numbers of templates are 4, 4, 22, 22, 25, and 25 for protrusion, intrusion, gap error, width error, pinhole, and pinspot template sets, respectively. Patterns with an edge roughness of one pel are considered acceptable. Each symbol indicates the center of a window pattern containing errors.

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