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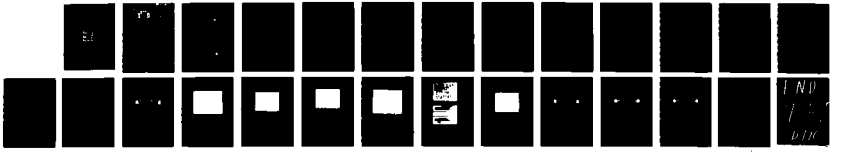

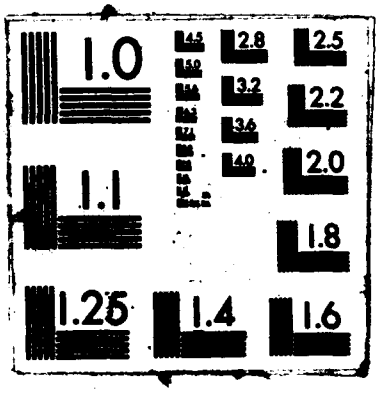
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19. ABSTRACT

The goal of this project is to demonstrate the operation of a new millimeter wave source called a "contiguous domain oscillator". This device uses the transferred electron effect in GaAs to form contiguous charge domains in the channel of a resistive gate MESFET or MODFET. The resulting drain current exhibits microwave oscillations in the range from a few GHz to a few hundred GHz. The oscillation is not based on a transit time effect, and as a result the frequency can be tuned over a broad band during operation by adjusting the gate-to-source voltage.

During the past year we fabricated eight wafers of MESFET-type oscillator devices. Of the six wafers that reached the end of the process, four produced devices which were functional at DC test. The most recent wafer contained thirty six working devices.

We have acquired equipment to conduct microwave measurements up to 90 GHz, which should be satisfactory for initial testing. During the next few months we expect to perform the microwave characterization which will verify the contiguous domain concept.

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Investigation of a New Concept in Semiconductor Microwave Oscillators

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Investigation of a New Concept in Semiconductor Microwave Oscillators

Annual Report

May 31, 1987

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I. Background

The goal of this project is to demonstrate the operation of a new millimeter wave source called a "contiguous domain oscillator". Briefly, the contiguous domain oscillator utilizes the transferred electron effect in GaAs to produce a sequence of contiguous charge domains in the drift channel of an appropriately modified MESFET or MODFET. These charge domains are similar to those which form in a Gunn diode — with one important exception: Since the electrostatic geometry of our device is two dimensional (as compared to the one dimensional electrostatic geometry of the Gunn diode), a contiguous sequence of adjacent domains forms spontaneously in the channel.

The domain formation has been investigated extensively by computer simulation. The domains form and stabilize quickly (within a few picoseconds of the start of the simulation), and the amplitude and spatial period of the domains are uniform along the channel. As electrons enter the channel from the source, they immediately rearrange to form charge domains, so that at any time the channel consists of a contiguous sequence of domains from source to drain. The domains drift along the channel at the steady state drift velocity associated with the applied field, typically around 1.4×10^7 cm/s, and as they enter the drain they create microwave oscillations in the drain current. The oscillation frequency depends only on the drift velocity and the spatial period of the domains in the channel. Frequencies from a few gigahertz to a few hundred gigahertz have been predicted by the simulations.

Two significant advantages of the contiguous domain oscillator should be noted. First, since the field in the channel is established by a resistive gate and not by the drain, the oscillation frequency is not influenced by the response of the load. This makes it possible to deliver microwave power to a resistive load, eliminating the tuned circuit required by all existing microwave diodes. Second, simulations show that the domain spatial period varies inversely with the average electron density in the channel, a quantity which can be controlled by the gate-to-source voltage. As a result of these two factors, it will be possible to adjust the oscillation frequency of the device over a wide range during operation.

The development of the contiguous domain oscillator can be divided into three phases: simulation, fabrication, and characterization. The simulation phase was largely completed before the beginning of Air Force support (although some simulation continues, as will be described presently). The first year of Air Force support was devoted to developing the necessary fabrication expertise to build the devices. Now, at the end of the second year of funded research, we are nearing the end of the fabrication phase and approaching the characterization phase.

During the past year we have built around forty devices which are functional at DC test and which should be capable of working in the microwave environment. In the coming year we will continue fabrication, and we will begin investigating the microwave operation of the oscillators.

II. Device Fabrication

A. Overview

Since most of the research work during the past year has dealt with fabrication issues, it will be helpful first to review the basic fabrication sequence for the device. The cross section of a typical contiguous domain oscillator is shown in Fig. 1. A number of variations on this basic structure are possible, and several of them have already been investigated. The major steps in the fabrication sequence are as follows:

1a.	MBE growth / isolation etch	(option A)
1b.	Channel implantation	(option B)
2.	Source/drain implant	

3. Implant activation
4. Silicon nitride deposition (optional)
5. Nitride etch (optional)
6. Contact deposition
7. Alloy
8. Resistive gate deposition
9. Metal deposition

Each of the above steps presents its own unique problems, and much of the work during the past year has centered on solving these problems and converging on an optimum fabrication sequence. We will summarize the status of each of the steps in the sections which follow.

B. Channel layer formation (step 1)

The n-type channel layer is typically 0.2 μm thick and doped to about $2x10^{17}$ cm^{-3} with Si. This layer may be formed either by MBE growth (option A) or by ion implantation (option B). MBE growth is under good control, and high quality films are routinely obtained. The Perkin Elmer 400 MBE machine is under the supervision of Prof. Mike Melloch.

A disadvantage of MBE growth is that the wafer size is limited to 0.8 in^2, whereas with implantion we can use a full two-inch wafer. Ion implantation is also under good control, but activation of implants has presented some problems, particularly for doses in the low 10^{17} cm^{-3} range (see section II.D. below). Since the depth and concentration of the channel layer is critical to the operation of the device, MBE growth may be the most reliable technique for channel formation at the present time.

C. Source/drain implantation (step 2)

The source and drain regions are implanted with Si^{++} at 175 KeV to a dose of $6x10^{13}$ cm^{-2}, resulting in source/drain regions with a donor density of $2x10^{18}$ cm^{-3} to a depth of about 0.3 μm. After implant activation, the net density of electrically active donors will be around $1x10^{18}$ cm^{-3}.

D. Implant activation (step 3)

Implant activation is by flash annealing in a radiant thermal annealer. The wafers are uncapped and are mounted on a silicon susceptor. The center line of the quartz tube lies at the common focus of four elliptical

reflectors, and each reflector has a 2 kW arc lamp at the other focus. The sample is initially raised to 450 C, then pulsed to the activation temperature (typically 850 C to 950 C) for 5 to 7 seconds. Temperature is monitored and controlled by a thermocouple in contact with the silicon susceptor. Flow gas is nitrogen.

We have calibrated the activation process for three Si implant doses: $3x10^{18}$ cm^{-3}, $6x10^{17}$ cm^{-3}, and $2x10^{17}$ cm^{-3}. For each dose, we have obtained curves of activation percentage and compensation ratio versus anneal temperature. Activation percentage is a weak function of temperature in the range from 1000 C to 900 C, and drops rapidly below 900 C. Activation percentages are around 80% at $2x10^{17}$ cm^{-3}, dropping to around 40% at $3x10^{18}$ cm^{-3}. No surface damage is seen for these short anneal times as long as the temperature is kept below about 1000 C.

We have recently discovered that the region of activation is confined to a narrow strip along the centerline of the anneal chamber. This fact was not noticed in the calibration runs, since the samples were quite small and were more-or-less uniformly activated. However, in the larger samples used in the oscillator fabrication, only a thin strip along the middle of the sample is properly activated. This effect accounts for some of the problems we experienced with ohmic contacts in several of our early wafers. In order to eliminate the problem, we are now performing several flash anneals with the sample progressively moved across the zone of activation.

E. Silicon nitride deposition (step 4)

A silicon nitride film is needed between the gate and drain to improve gate-to-drain breakdown. If a nitride layer were not used, the gate would form a reverse biased Schottky diode to the drain. Since the drain is heavily doped, the planar breakdown voltage of this diode would be about 5 V. Although a 5 V breakdown would be adequate for device operation, field enhancement would be expected along the gate edge, lowering the breakdown voltage to the 1-2 V range.

In order to increase the gate-to-drain breakdown voltage, we initially included silicon nitride under the entire gate region (see Fig. 1). As will be discussed below, this resulted in a breakdown voltage over 18 V, but introduced undesirable hysteresis in the I-V curves due to slow trapping in the nitride. Subsequent wafers have been processed using a mask which

removes the nitride between the gate and channel, leaving a ring of nitride all the way around the gate edge (measured BV around 5 V). We have also completed a wafer without any nitride (measured BV around 2 V).

The silicon nitride is deposited by plasma assisted CVD at a substrate temperature of 225 C. Thickness is around 800 Å.

F. Nitride etch (step 5)

The nitride pattern is etched using 40:1 buffered HF. Some yield problems have occured at this step owing to nonuniformity of the etch, leading to an overetch of some regions of the wafer before other regions have cleared. We are working on this problem.

G. Contact deposition (step 6)

Au-Ge pellets (12% Ge) are evaporated onto a pre-defined photoresist layer. The evaporation is routine, but the photoresist has to be carefully prepared so that liftoff can be achieved after Au-Ge deposition. The resist thickness must be greater than the Au-Ge thickness (typically the resist is around 1 μm and the Au-Ge is less than 0.5 μm), and the resist must be soaked in xylene to harden the upper layer prior to development. This results in an undercut of the pattern in the resist and aids subsequent liftoff of the Au-Ge material. An example of improper procedure is shown in Fig. 2, where a steep wall of Au-Ge remains around the alloy contact region after liftoff. On this wafer (designated "Y2a"), most of the ohmic contacts failed due to lack of metal coverage over this "wall", even though the alloy contacts themselves were good, as verified by probing.

H. Alloy (step 7)

The ohmic contacts are alloyed at 450 C for 2 minutes in nitrogen. This step is routine. Since Ni is not used as a wetting agent, good ohmic contacts give the appearance of having "beaded up" under the microscope. This is normal, and leads to no discernable problems in operation.

I. Resistive gate deposition (step 8)

For the resistive gate, we need a material with a sheet resistance of around 30 KΩ/□ in order to limit power dissipation enough for CW operation. We are presently using evaporated Ni-Cr for the gate material.

At a thickness of around 500 Å, Ni-Cr has a sheet resistivity of only about 300 Ω/□. Thus it will be necessary to operate the completed devices in the pulsed mode with a duty factor less than 1%. The Ni-Cr step does not present any fabrication problems, and liftoff is reliable since the film is so thin.

We have also worked on co-sputtering of SiO and Cr to form a ceramic-metal (CERMET) material. With this material we have achieved a sheet resistance of 265 kΩ/□ at a thickness of 8000 Å and 565 kΩ/□ at a thickness of 3600 Å. The resistance of the CERMET film can be lowered in a controllable fashion by annealing in nitrogen for around an hour at temperatures from 200 C to 400 C.

We still have to work out a patterning procedure for the CERMET material. In particular, in order to use liftoff we need to be sure that the photoresist is not damaged by the plasma in the sputtering system. At the present time, work on CERMET gates is on hold due to lack of personnel.

J. Metal deposition (step 9)

The final step is deposition of aluminum and patterning by liftoff. This step is routine except for the liftoff, which occasionally causes problems. Careful attention must be given to the resist thickness and the length of the xylene soak in order to lift the metal pattern without leaving "stringers" of aluminum.

III. Fabrication Results

A. Introduction

During the past year we have processed a total of eight wafers. Of the six wafers which reached the end of the fabrication sequence, two had no source/drain contacts, but the remaining four produced working devices at DC test. The latest of the four contained a total of thirty six functional devices.

In the following sections, we will summarize the results from each wafer, proceeding in chronological order. An overall summary is provided in Table 1. The designations "B1", "B2", etc. refer to wafers started by Robert Beaty and the designations "Y1", etc. refer to wafers started by Yiwen Yin.

B. Wafer "B1"

The first wafer was completed in June 1986. This wafer had an MBE grown channel layer on a p-type substrate and silicon nitride under the entire gate (see Fig. 1). Four devices were functional at DC test. Two of these devices are shown in Fig. 3. The I-V curves show hysteresis due to the slow trapping in the nitride, but otherwise the characteristics look quite good. Drain breakdown is above 18 V.

An unexpected side effect of the nitride under the gate was the formation of a hole inversion layer at a gate voltage of about -11 V, preventing pinchoff of the n-type channel. As shown in Fig. 3, pinchoff could be achieved by applying 10-15 V of substrate bias (source reverse biased to substrate). As a result of this experience, a new nitride mask was designed limiting the nitride to a narrow ring lying under the perimeter of the resistive gate to prevent edge breakdown.

C. Wafer "B2"

This wafer had an ion implanted channel layer, but was otherwise identical to wafer "B1". This wafer was destroyed when a student knocked it out of a bake oven near the end of the processing sequence.

D. Wafers "Y1" and "B4"

These wafers each consisted of one quarter of a two inch wafer, with the channel formed by ion implantation. "Y1" and "B4" differed in the dose and depth of the channel implant. Both used the modified nitride mask with nitride present only under the edges of the gate. Upon completion, these wafers were unusable due to lack of ohmic contact to the source/drain regions. Although not realized at the time, we now suspect that the failure was due to the localized nature of the implant activation process.

As a result of this failure, we modified the alloy contact mask to create two test devices which can be probed after the alloy step. One device tests the source/drain implant and the other verifies the channel implant. These testers give us early feedback on the implant activation and alloy contact procedures, and allow us to rework the alloy contact step if needed.

E. Wafers "Y2a" and "Y2b"

Wafers "Y2a" and "Y2b" were taken from the same quarter of a two inch wafer, and were separated after implant activation. Consequently, both had the same channel doping and depth. Wafer "Y2b" had already passed the alloy operation (step 7) when we discovered the problem with the localized nature of the implant activation. In an attempt to salvage this wafer, we tried to flash anneal the wafer with Au-Ge present. However, the thermal shock spread Au-Ge over the wafer, and wafer "Y2b" had to be abandoned.

Wafer "Y2a" was returned to the radiant annealer and reactivated in different positions to insure broad coverage. After processing was completed, most of the devices again did not show good source/drain contacts. The problem was traced to improper liftoff of the Au-Ge alloy material, resulting in a "wall" of Au-Ge surrounding each alloy contact, as shown in Fig. 2. The thin aluminum metal was not continuous over this "wall", but direct probing to the alloy contacts revealed many of the devices to be functional. The devices were evidently not fully activated, since they were all enhancement mode, i.e. they required a forward bias on the gate to establish a channel from source to drain. A typical I-V characteristic from wafer "Y2a" is shown in Fig. 4.

F. Wafers "B3a" and "B3b"

These wafers were again taken from the same quarter of a two inch wafer and had identical channel implant doses and depths. Both were activated multiple times. Wafer "B3a" was processed with no silicon nitride anywhere under the gate, and three depletion mode devices were functional at DC test. A typical device is shown in Fig. 5. No hysteresis is present in the I-V characteristics, but the gate-to-drain breakdown voltage is only about 1.4 V. This convinced us that the nitride was indeed necessary, at least under the gate edges.

Wafer "B3b" was completed during the writing of this report, and a total of thirty six devices were functional at DC test. Both the visual appearance and the electrical characteristics are excellent, as shown in Fig. 6. This wafer has a nitride ring under the edges of the gate, and the gate-to-drain breakdown voltage is about 5 V, about as expected given the heavy doping in the drain region. The devices are depletion mode, and the drain current is substantial, indicating good activation of the channel implant. The

hysteresis in the I-V curves was unexpected, since the nitride should be present only around the edges of the gate and not over the active channel — this will be investigated.

G. Work on Interrupted MBE Growth for the MODFET Oscillator

Another structural implementation of the contiguous domain oscillator makes use of a GaAs MODFET (or HEMT, HIGFET, SISFET, etc.) having a resistive gate. Such a device is shown in Fig. 7. In order to construct a viable MODFET oscillator, it will be necessary to arrange for the resistive gate to overlap the ion implanted drain region. One way to achieve this is to interrupt the MBE growth of the heterostructure after growth of the epitaxial buffer layer, passivate the surface in the MBE chamber with a layer of As, AlAs, or InAs, remove the wafer from the MBE machine, perform source/drain lithography and ion implantation, clean the wafer, reintroduce the wafer into the MBE machine, drive off the passivation layer, and grow the AlGaAs barrier layer. This procedure would create isolated source and drain regions under the AlGaAs barrier layer. The resistive gate could then be deposited on top of the AlGaAs barrier, overlapping both the source and drain.

Preliminary work on this interrupted growth technique has been done by Philip Neudeck in collaboration with Prof. Mike Melloch. We have been able to fabricate buried N+ implanted layers under the AlGaAs barrier layer and to make electrical contact to these layers by alloying Au-Ge through the AlGaAs layer. However, to date we have not been succesful in building working MODFET devices with this method. The passivation methods used to date have involved layers of As or AlAs. We would like to try InAs at some time in the future, and will install an indium effusion cell in our MBE machine the next time it needs to be opened.

We are now considering an alternate method for constructing a MODFET oscillator. This new technique will be discussed in Section IV.

IV. Plans for the Coming Year

A. Simulation

In order to improve our understanding of the device operation, especially in the MESFET configuration of Fig. 1, Robert Beaty is working on a full

two dimensional computer simulation of the device. Once thought prohibitively costly in computer time, this type of simulation is now run routinely at Purdue for solar cell modeling using the vector arithmetic of the Cyber 205 supercomputer. Instead of attempting an iterative solution to the two dimensional Poisson equation coupled to the current flow equations, it is now possible to solve this large system of equations by direct matrix inversion on the Cyber. Although most of the experience at Purdue has been with steady-state simulations, we hope to implement a true transient simulation using this approach. A two dimensional simulation is needed for accurate modeling of the MESFET version of the device, where the electron density in the potential well cannot be regarded as an infinitely thin sheet.

As an aside, Prof. Eric Fossum of Columbia University has informed us that he and his students have implemented a one dimensional transient simulation of our device, similar in operation to the program we are running. He also sees oscillations in the electron density, and intends to publish his findings with an appropriate acknowledgement to us.

B. Fabrication

We will be starting new wafers of MESFET oscillator devices in the near future. Some of these wafers will incorporate a new structural design shown in Fig. 8. In this design we use MBE growth to form both the n-type channel layer and an undoped AlAs passivation layer. The source and drain regions are formed by ion implantation after MBE growth, and the gate forms Schottky diodes with the underlying source and drain. (Since the device is depletion mode, the gate is always reverse biased with respect to both the source and the drain.) The AlAs passivation layer should improve the gate-to-drain breakdown voltage by at least a factor of two, owing to the higher bandgap of AlAs. This design will also eliminate silicon nitride and the associated hysteresis, thus simplifying the process and improving yields. It will also improve the control of the channel doping and depth since the channel layer is grown by MBE.

A similar structure can be used to form the MODFET version of the oscillator, as shown in Fig. 9. The AlGaAs barrier layer must be n-doped so that the device will be depletion mode. This allows the gate-to-source voltage to remain negative, keeping the gate-source junction reverse biased. After MBE growth, the processing steps for the MODFET and MESFET oscillators are identical.

We also hope to add to our stockpile by having some devices processed (at no charge) at the ITT Gallium Arsenide Technology Center in Roanoak, VA. We visited ITT in March to discuss our collaboration, and were informed that they plan to process one lot of devices, consisting of six two-inch wafers, beginning in September. They will commense layout work in June, and the completed devices should be in our hands by November. If all goes well, this should supply us with around a thousand testable devices.

C. Characterization

Our most immediate priority is to saw apart wafer "B3b", containing thirty six functional devices, and to mount these devices for microwave testing. The saw apart procedure will be tested first on wafers "Y1" and "B4", since these had no functional devices. We will then use chips from "Y1" and "B4" to help set up the biasing circuitry and to determine the proper duty cycle for the bias pulse to avoid destruction of the resistive gates.

We have taken delivery of a Tektronix 2755 spectrum analyzer capable of detecting signals from 50 kHz to 325 GHz. At this time we have mixers covering the ranges from 26-40 GHz, 40-60 GHz, and 60-90 GHz. (The spectrum analyzer will accept direct input of signals below 21 GHz.) The oscillator chip will be mounted on a shorting plate at the end of a waveguide transition connected to the mixer, as shown in Fig. 10. The transition is needed because the cross section of the mixer waveguide is too small to accomodate our device. Bias will be applied by small wires feeding through holes in the shorting plate, and the microwave output will be coupled to the waveguide by a loop in the bonding wire to the drain. This loop will excite the H field of the TE_{10} mode in the waveguide.

V. Summary

During the past year we have made substantial progress in the fabrication of the oscillator devices. We have processed a total of eight wafers, four of which produced devices which were functional at DC test. The latest wafer, completed only days ago, had a total of thirty six working devices. Our students have gained practical experience with the processing, and we appear to be converging on a workable fabrication procedure. Fabrication will continue on both MESFET- and MODFET-type oscillators to insure an adequate supply of devices for microwave characterization.
We have acquired test equipment capable of measuring device operation over the full frequency range predicted by our simulations, and we will begin microwave testing of our latest devices immediately.

VI. List of Professional Personnel

James A. Cooper, Jr., Professor of Electrical Engineering (Principal Investigator)

Michael R. Melloch, Assistant Professor of Electrical Engineering (Consultant on processing; supervises MBE machine operation)

Robert E. Beaty, Ph.D. Student (Developed most of the fabrication technology, processed wafers "B1", "B2", and initiated the processing on wafers "B3a","B3b", and "B4"; now developing a two dimensional transient computer simulation)

Yiwen Yin, Ph.D. Student (Responsible for processing of MESFET oscillator devices; processed wafers "Y1", "Y2a", and "Y2b", and completed wafers "B4", "B3a", and "B3b".)

Philip G. Neudeck, M.S. Student (Working on interrupted MBE growth for the MODFET oscillator; will soon begin process development for the new depletion mode MODFET oscillator structure)

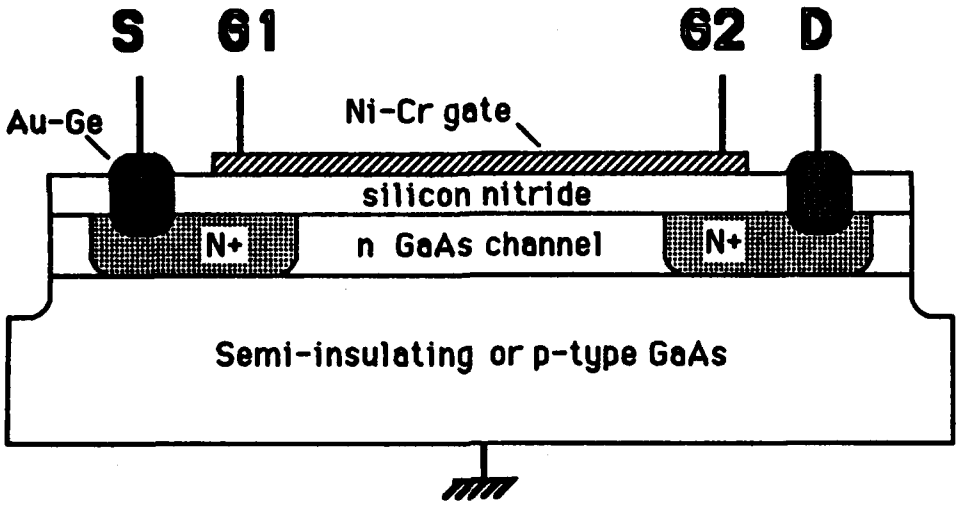

Figure 1. Cross section of a typical buried channel MESFET type contiguous domain oscillator. In this version, the n-channel is grown by MBE and isolated by etching. The silicon nitride under the gate is now usually removed except for a thin ring lying under the periphery of the gate.

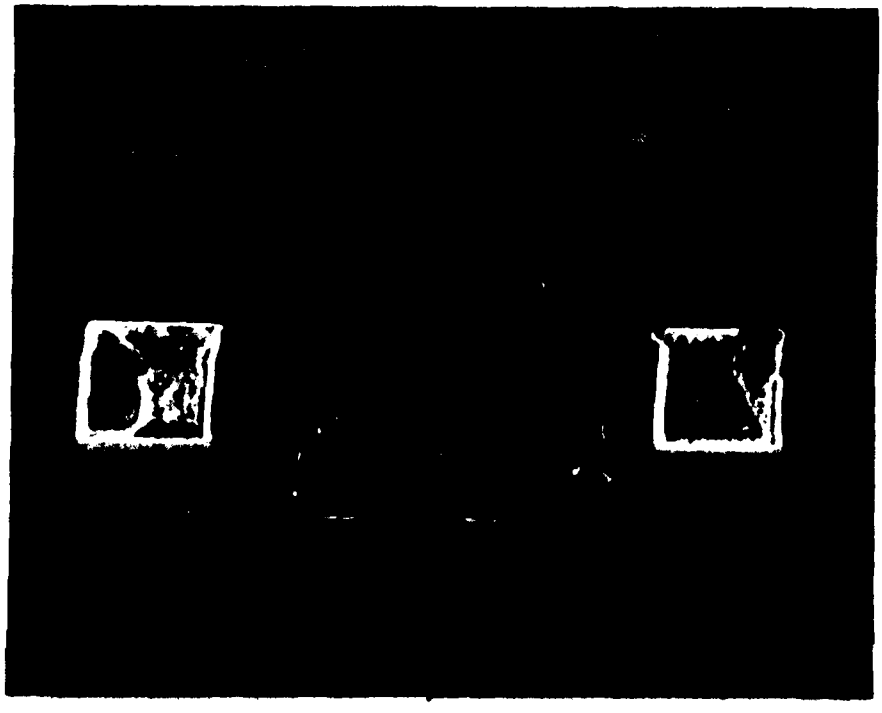

Figure 2. SEM photograph of an oscillator device showing the "wall" of Au-Ge surrounding the alloy contacts. This "wall" was due to improper liftoff, wherein the photoresist was not undercut during development prior to Au-Ge deposition. As a result, some Au-Ge deposited on the tapered side of the photoresist window, resulting in the wall. The metal was not able to cover this step.

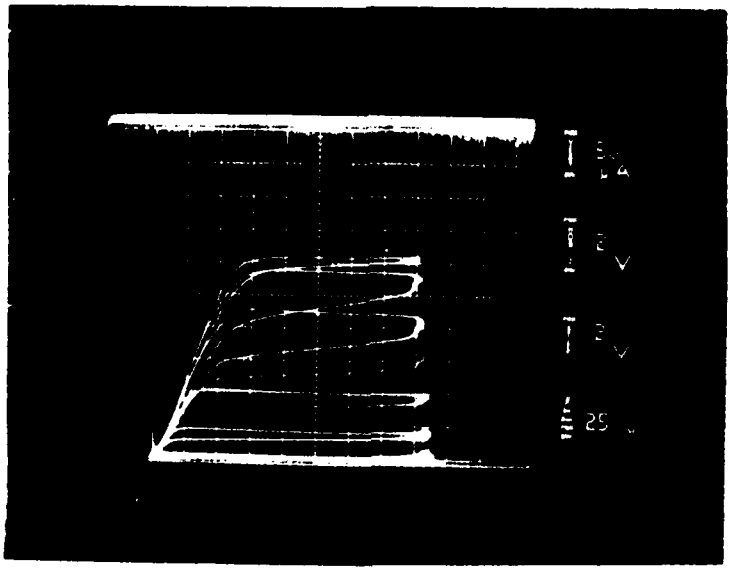

Figure 3. Current-voltage characteristics of a 20 x 50 μm device on wafer "B1". The hysteresis is due to slow trapping in the silicon nitride layer under the gate. The nitride also allows a hole inversion layer to form before the channel can be completely pinched off by the gate, so in this photo the substrate is biased 15 V negative with respect to the source to partially pinch off the channel from the bottom. The top curve is for a gate voltage of zero, and lower curves have gate voltage becoming more negative.

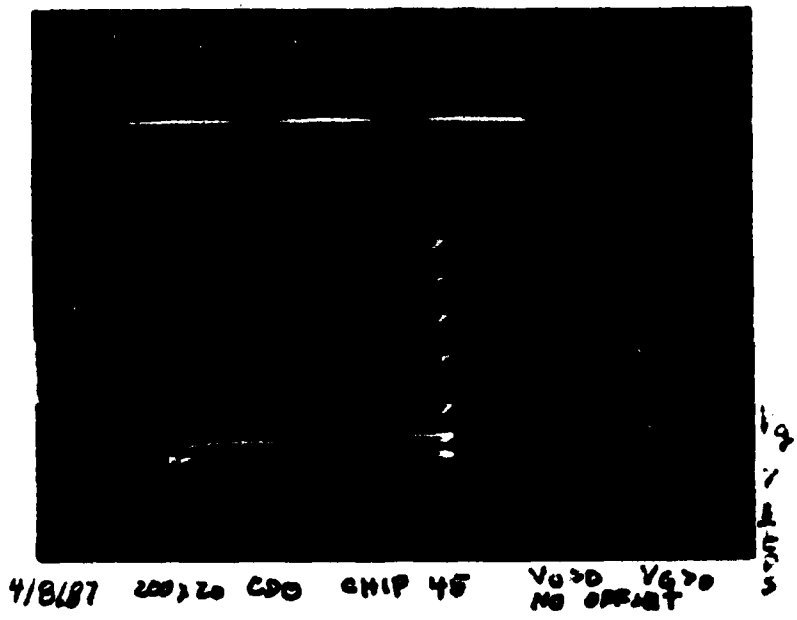

Figure 4. Current-voltage characteristic of a 200 x 20 μm oscillator device from wafer "Y2a". The devices on this wafer were depletion mode, requiring a positive (forward) bias on the gate to establish a channel. The bottom curve is for a gate voltage of zero, and higher curves have gate voltage increasing by 0.5 V/step.

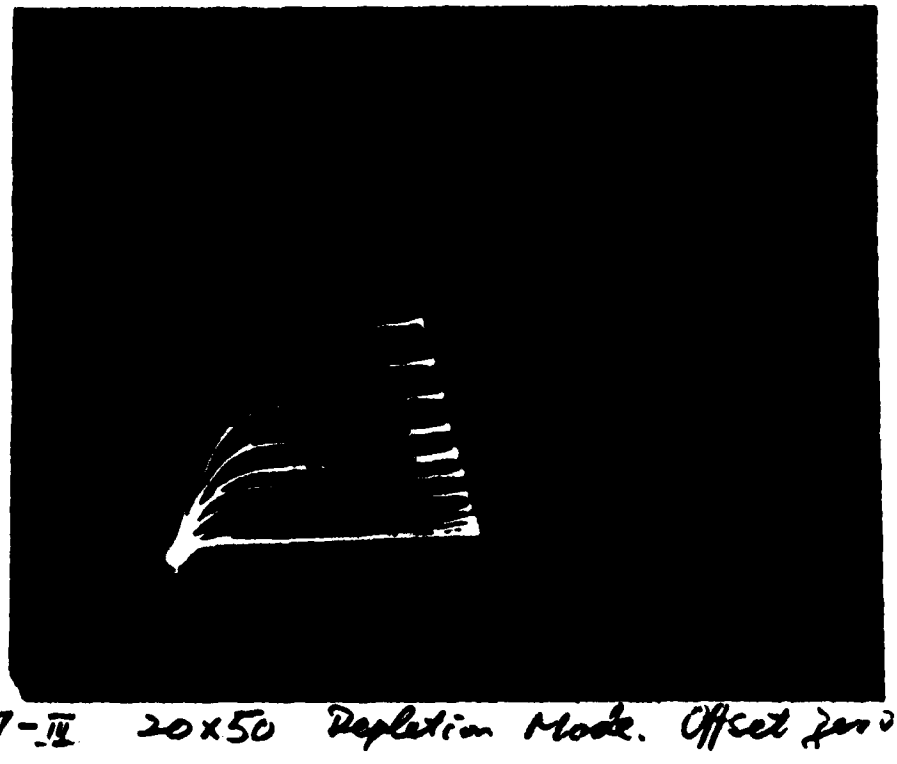

Figure 5. Current-voltage characteristics from a 20 x 50 µm device on wafer "B3a". This wafer had no nitride, as indicated by the absence of hysteresis. The top curve is for zero gate voltage, and gate voltage becomes more negative for the lower curves. The horizontal scale is 0.2 V/div, and gate-to-drain breakdown occurs at about 1.4 V due to the absence of a nitride ring around the edges of the gate.

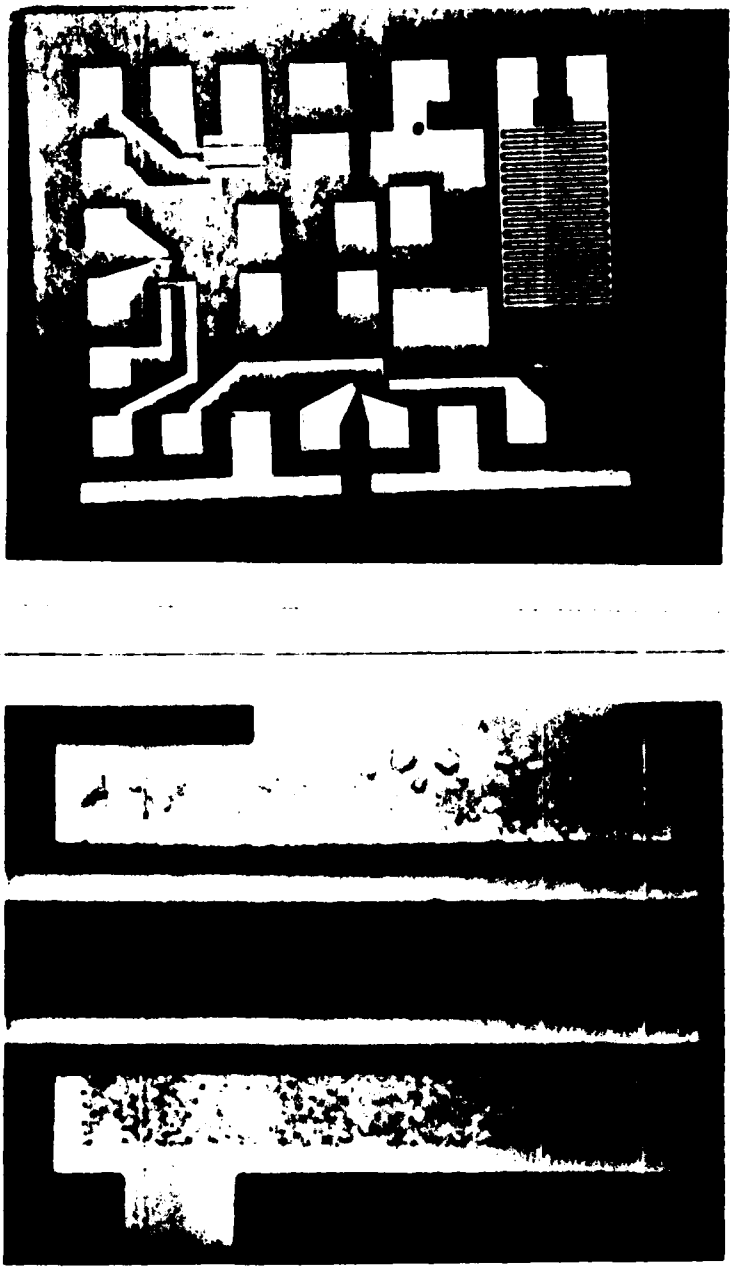

Figure 6a. Microscope photographs of wafer "B3b". The top photograph is an overview of a test chip containing three oscillator devices and several test structures. The bottom photograph shows the 200 x 20 μm oscillator device.

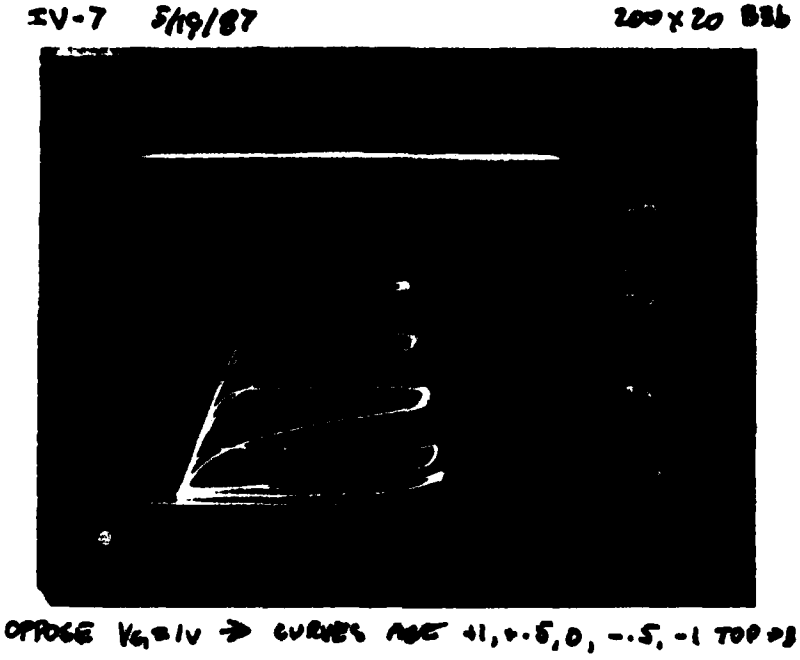

Figure 6b. Current-voltage characteristics of a 200 x 20 µm oscillator device from wafer "B3b". The hysteresis may indicate some residual nitride under the gate. The third curve from the top is for a gate voltage of zero; above the voltage is positive (channel enhanced) and below the voltage is negative (channel depleted). Gate-to-drain breakdown is above 4 V.

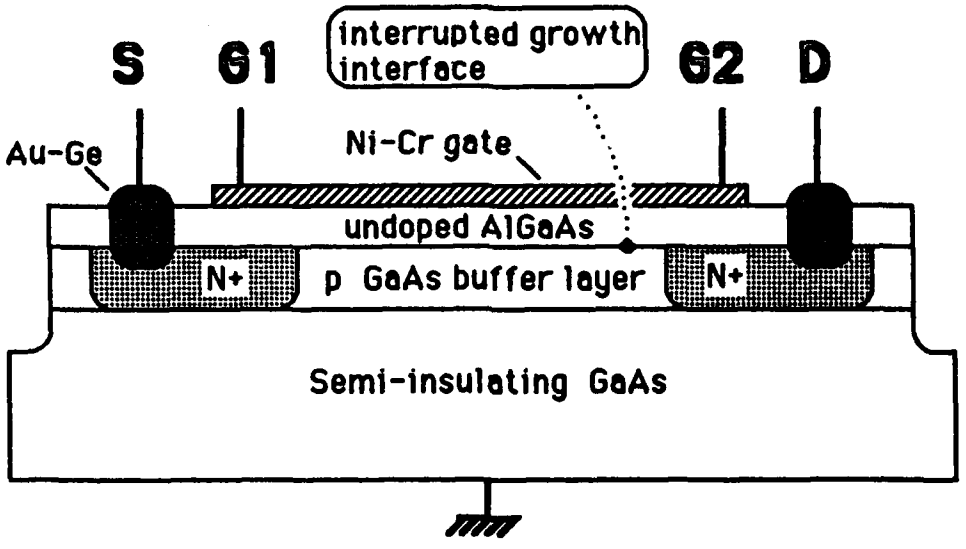

Figure 7. Cross section of a MODFET type contiguous domain oscillator fabricated by interrupted MBE growth. The sample is removed from the MBE after growth of the p-type buffer layer, source/drain implants are performed, and the AlGaAs barrier layer is grown by MBE.

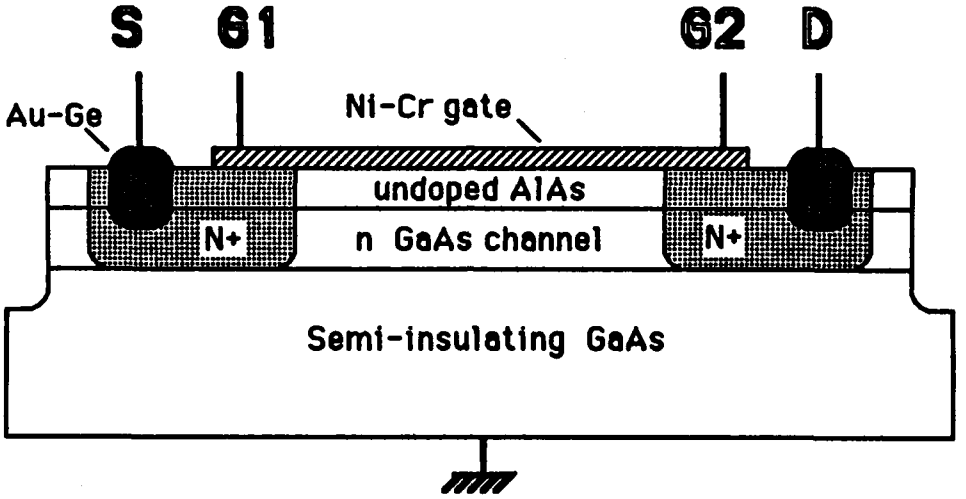

Figure 8. New structural design for the buried channel MESFET type contiguous domain oscillator, utilizing undoped AlAs as a barrier layer in lieu of silicon nitride. The n-type channel layer and AlAs barrier are grown by MBE, and the N+ source/drain implant dopes both the AlAs and GaAs. The gate forms reverse biased Schottky diodes with the source and drain regions.

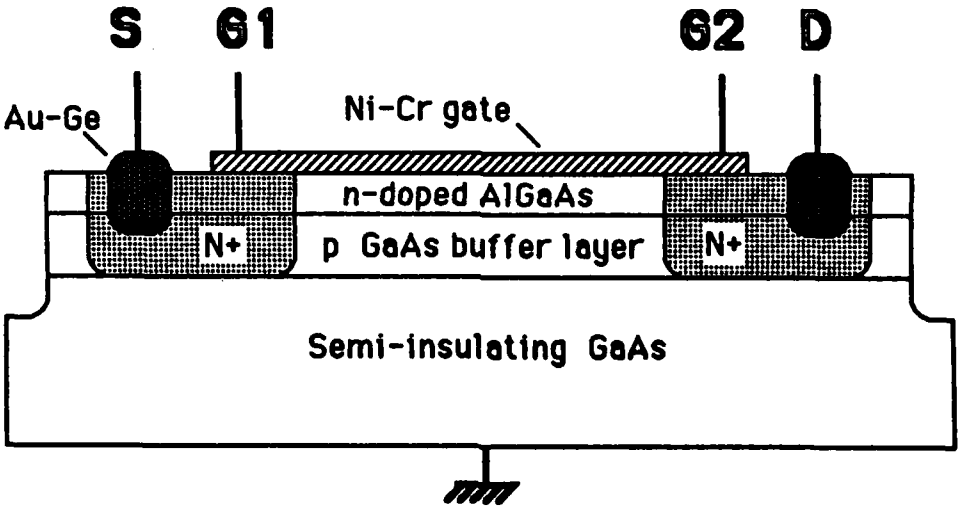

Figure 9. New structural design for the MODFET type contiguous domain oscillator. This structure is identical to the new MESFET structure of Fig. 8 except the n-type GaAs channel of the MESFET is replaced with a p-type GaAs buffer layer and the undoped AlAs is replaced with n-doped AlGaAs. Electron flow is now confined to a thin sheet at the AlGaAs/GaAs interface. No interrupted growth is required in this design.

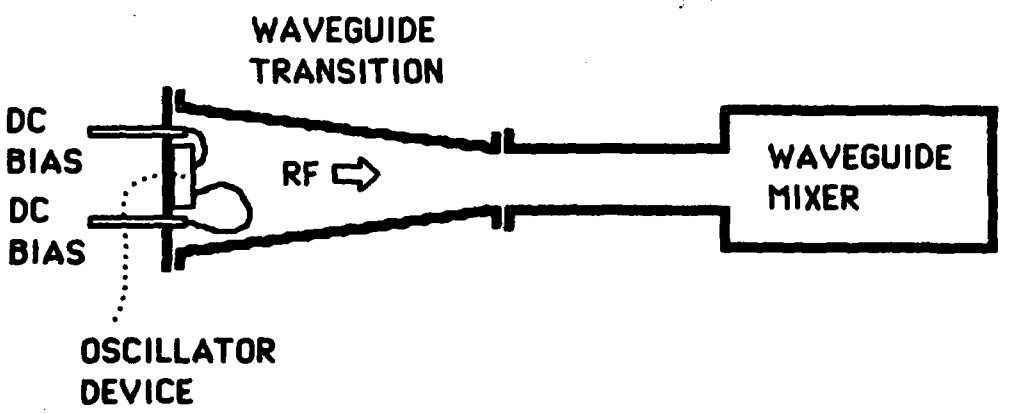

Figure 10. Schematic of microwave test setup. The oscillator device is mounted on a shorting plate at the end of a microwave transition leading to the waveguide mixer. DC bias is provided by feedthroughs in the shorting plate.

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