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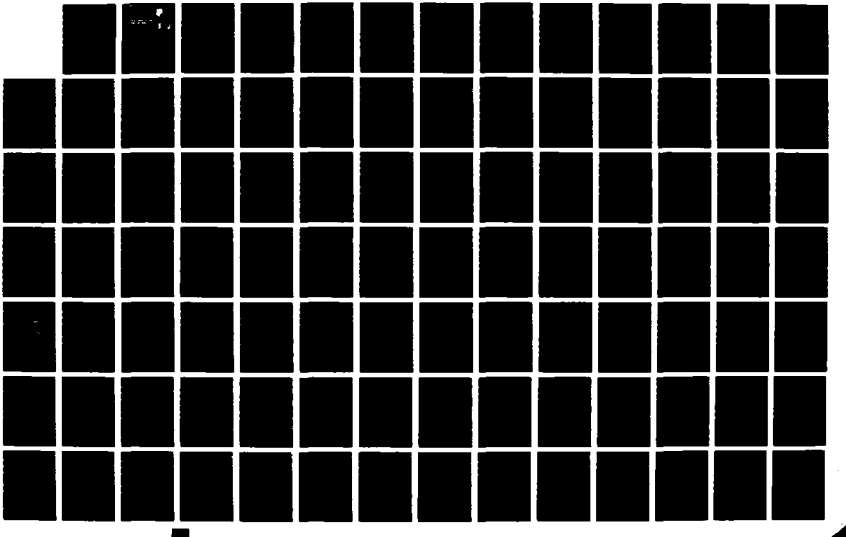

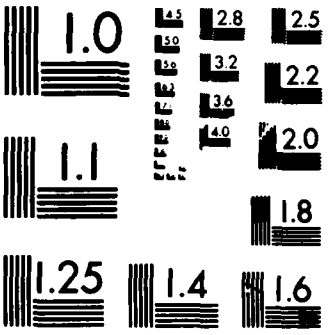

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October 1986

ELECTRICAL CHARACTERIZATION OF VLSI RAMs AND PROMs

GTE Communication Systems Corporation

M. Formoso, D. Giammarrusco, G. Hornbuckle, R. Henrikson and E. Rolley

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Extensive electrical characterizations were performed on 256K bit and 512K bit ultra violet erasable PROMs (UVEPROMs), 64K bit electrically erasable PROMs (EEPROMs), 64K static RAMs (organized as 8Kx8 bits), 256K dynamic RAMs (CMOS) and 32R16 PAL devices available from the merchant semiconductor industry. Based on the data obtained from the devices, parameter limits were established and proposed for the draft MIL-M-38510/XXX specifications. The data, proposed limits and test methodologies and the related discussions are presented.

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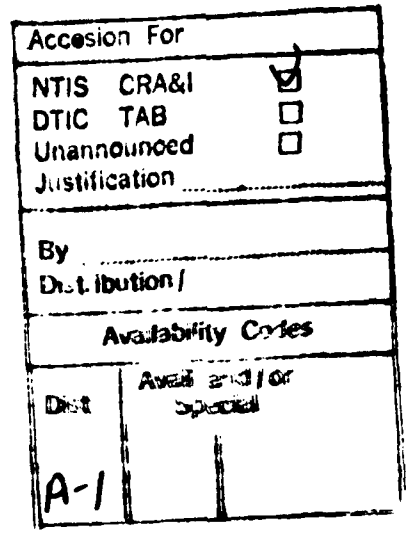

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EVALUATION

The objective of this effort was to evaluate and electrically characterize several commercially available state-of-the-art semiconductor memories, and to make a determination as to their suitability for insertion in military systems. The resulting data was then used to generate draft MIL-M-38510 specifications. The devices selected for this program and their corresponding "slash sheet" numbers are as follows: 256K bit UVEPROM, /224; 512K bit UVEPROM, /270; 64K bit static RAM (CMOS), /292; 64K EEPROM, /228; 256K DRAM (CMOS), /247; and the 32R16 PAL device, no slash sheet number assigned yet. Most testing was accomplished using a Xincom 5588 memory tester; where machine limits were exceeded, bench testing techniques were employed.

This report contains data summaries and discusses the characterization results. In addition, a detailed margin test was developed and verified for the UVEPROM devices. The specifications which resulted from this effort will allow the procurement of reliable military grade components, thereby enhancing the reliability of military systems. Copies of the detail specifications are available from the Defense Electronics Supply Center, Dayton OH.

Charles H Windisch, Jr

CHARLES H. WINDISCH, JR.
Project Engineer

CONTRACTUAL REQUIREMENTS

This report covers the results of the device characterization performed as part of the contract and as established by agreements between GTE Communication Systems Corporation and Rome Air Development Center during meetings following the awarding of the contract. The devices covered under this report include the 256K (32K x 8) UVEPROM, 512K (64K x 8) UVEPROM, 64K (8K x 8) SRAM, 256K x 1 CMOS DRAM, and the 64K (8K x 8) EEPROM. The project was completed under the direction of the Program Manager, Mr. J. E. Meschi and Technical Coordinator, Mr. E. A. Rolley.

Contract Adjustments

The program originally included the characterization of the 32R16 programmable array logic device, but this device was subsequently dropped from the program, due to the lack of sample availability from the vendors, and was replaced with the 512K UVEPROM [1]. Along with the technical data presented for the other devices, a complete report of the activities performed under the contract up to the point of program termination for the programmable array logic device are included for information and completeness.

Report Coverage

The technical report covering each individual device type characterized under this contract is included as a separate part of this overall report and is treated individually with regard to the techniques of testing and the data provided in support of the actual slash sheet produced for that device type. This report is constructed in such manner that each part is complete unto itself and if desired can be removed for individual reference. At the beginning of each part is its own Table of Contents covering only the material in that part. The page numbers of each part begin with the designator for that part which is unique for the device type covered.

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1. Letter from RADC/RBRA C. H. Windisch to RADC/PKRZ Lt. Lynch dated 1 Oct 85.

Summary

In summary the characterization program yielded the preparation of slash sheets for five devices. These included the 256K Ultraviolet Eraseable Programmable Read Only Memory, 512K Ultraviolet Erasable Programmable Read Only Memory, 64K Electrically Erasable Programmable Read Only Memory, 64K Static Random Access Memory, and 256K Dynamic Random Access Memory. The testing of the sample devices provided by the vendors correlated to the values proposed by the vendors. In each case the test results showed that these devices meet or exceed the specified performance reflected in the completed slash sheet specifications which have been provided to RADC.

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256K UVEPROM

LIST OF FIGURES

1. SUMMARY

1.1 OBJECTIVES/RESULTS

The objective of this portion of the contract with Rome Air Development Center was to perform and present the results of a detailed electrical characterization of a 256K (32K X 8) NMOS UVEPROM. In addition, a preliminary MIL-M-38510 slash sheet was developed.

This report documents the results of the electrical characterization on Intel's "MD27256" UVEPROM. Full AC and DC electrical testing was performed over the full military temperature range. A margin test for the floating gate trapped charge on a EPROM cell was developed. This new test has been included in the slash sheet.

In summary, the device performed as expected, per the proposed slash sheet with the exception of propagation delays, which were noticeably shorter.

Details and test data documenting the above findings are presented and summarized in this report and the slash sheet.

2. INTRODUCTION

2.1 OBJECTIVES

The major objective of this effort was to electrically characterize a 256K (32K X 8) UVEPROM and develop a preliminary MIL-M-38510 slash sheet. In general, the effort involved:

- o Memory market survey to determine production status of candidate devices.
- o Selection and procurement of candidate device types for characterization.
- o Development of test procedures compatible with automatic test systems.
- o Determination/verification of limits and test circuits via device characterization.
- o Investigation of margin testing as a viable means of determining the trapped charge on a floating EPROM cell.
- o Development of a preliminary slash sheet based on device analysis and vendor comments.

2.2 BACKGROUND

The original RFP response called for the 128K EPROM device. However, it was decided jointly between RADC and GTE after contract award to pursue the 256K (32K X 8) version since it was announced to be available from Intel earlier than originally expected and the higher complexity part was more desirable to RADC.

3. DESCRIPTION OF DEVICE TYPE

3.1 GENERAL ASPECTS OF 256K EPROMS

The 256K EPROM is a 5 volt only, 262,144-bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM), organized 32K words by 8 bits. The by 8, or bytewide configuration is intended primarily for use with byte oriented microprocessor systems. The two-line (Chip Enable & Output Enable) control and JEDEC-approved, 28-pin package assures easy microprocessor interfacing and minimum design effort when upgrading, adding or choosing between nonvolatile memory alternatives. The 27256's large storage capability of 32K X 8 enables it to function as a high density software carrier.

3.2 ASPECTS OF SPECIFIC DEVICE TYPE

The Intel MD27256 EPROM has several advanced features that allow programming equipment to identify the MD27256 and then rapidly program it using an efficient programming method. The MD27256 is manufactured using HMOS II-E [1] process.

3.3 SYSTEM APPLICATION CONSIDERATIONS

The power switching characteristics of HMOS II-E [1] EPROMs require careful decoupling of the devices. The supply current, ICC, has three segments that are of interest to the system designer: the standby current level, the active current level and the transient current peaks that are produced by the falling and rising edges of Chip Enable. It is recommended that a 0.1uF ceramic capacitor be used on every device between VCC and GND. In addition, a 4.7uF bulk electrolytic capacitor should be used between VCC and GND for every eight devices. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board traces.

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[1] HMOS II-E is a patented process of Intel Corporation

4. DEVELOPMENT OF AUTOMATIC AND BENCH TESTS

4.1 AUTOMATIC TEST EQUIPMENT

The test equipment used to characterize the 256K EPROM is a Fairchild Xincom 5588 Automatic Test System. The system's main processor is a Zilog Z8000 microprocessor. This processor handles all test sequences and test processes. Included in the system is a subsystem which is called the Test Pattern Computer (TPC).

The TPC is a modular subassembly which can be loaded with a microprogram and will output data and address patterns for the main purpose of testing memory devices. All popular industry patterns; e.g., Ping Pong, Checkerboard, March are programmable, plus the capability to microprogram other patterns. Patterns are defined by a set of 48-bit microcoded instructions executed within the TPC at functional rates up to 25MHz (40ns cycle time). Upon command from the main processor the TPC generates the desired pattern and send this pattern to the system for use in the stimulus of input pins and response checking of output pins.

Some additional features of the TPC are:

- o ECL Construction
- o Topological Address Scrambler
- o Address Indexing, Refresh Testing, Butterfly Patterns
- o Truth-Table RAM (Pattern RAM For EPROMS)
- o Algorithmic Pattern Generation
- o Loop Counters
- o Timing Set Selection on the fly

In addition to the TPC other system capabilities include:

- o 14 programmable clock phases
- o 4 programmable power supplies
- o 24 address lines
- o 16 data comparators
- o Parametric Measurement Unit (PMU)
- o Advanced Error Logging System (AELS)
- o IEEE 488 Bus Interface
- o Color Computer Graphics Display
- o Auto Data Logging to Data General Eclipse Host Computer

To interface the device under test (DUT) to the test system, an interface board is used to electrically connect the DUT's pins to the specific test system pin electronic cards. A zero insertion force socket is used to allow for fast removal and insertions of the DUT without causing lead damage.

4.2 BENCH TEST EQUIPMENT

Several instruments were required to perform the Electrostatic Discharge, Capacitance Measurement, and UV Lamp Power Output tests.

The Electrostatic Discharge unit used is a IMCS Corporation, Model number 2400C.

Features include:

- o 0-10,000 Volt Continuously Adjustable
- o 4.5 Digital Display of HV
- o Programmable Pulse Sequence
- o Curve Tracer Output
- o 1-128 pin Configuration
- o Applicable to Mil STD 883 and STD 1686

The Capacitance Analyzer used is a Hewlett Packard, Model number 4192A, probe model number HP-16048C.

Features include:

- o 5 HZ to 13MHZ variable measuring frequency
- o Gain-Phase measurement: amplitude, phase and delay
- o Floating or Grounded devices
- o Frequency accuracy +/- 50ppm

A special measurement was required for the UV erasure and margin tests. A meter that measures the power output of the UV lamp in micro-watts per centimeter squared is required. The meter used is a Spectronics Corp. Model number DS-254E. By knowing the actual power output of a UV lamp, detailed investigations into the actual dose (time X UV output power) required to erase the EPROM array can be determined.

Some features of the UV meter are:

- o 4.5 Digit Digital Display
- o Conversion Rate: 3 reading per second nominal
- o Resolution: One part in 1999
- o Temperature Coefficient: +/- (0.025 of reading + 0.1 digit)/Degree C (0 to 50)
- o Accuracy: +/- 5% with reference to NBS standards

4.3 EPROM PROGRAMMING EQUIPMENT

A Data I/O, model 29A was used to program the test patterns into the EPROM device. The 29A is a microprocessor-based system which is designed around a 6802 microprocessor. The programmer allows the user to create and program unique data patterns. A master device which contains a predetermined pattern can also be copied and programmed. The system has many editing features which enable the user to modify patterns quickly.

A programming pack was required for the 256K EPROM device. This pack is a plug-in module which has the ability to program up to 200 different EPROM and PROM types. This programming pack can be identified as "Uni-Pak," model number 950-0099-10, Software revision V10.

Some features of the system are:

- o 64K X 8 (512K bits) RAM for pattern storage
- o Hexadecimal keyboard with alphanumeric display
- o Automatic check-sum calculation
- o Automatic error routine monitors device integrity
- o 16 switch selectable baud rates for remote terminal and data transfer

5. STATIC CHARACTERISTICS

5.1 OBJECTIVES

During this characterization, several goals were set forth. One of these was to reliably and efficiently characterize the D.C. parameters of the 256K EPROM device. This was accomplished by utilizing Automatic Test Equipment (ATE). This equipment could reliably execute a group of measurements and test conditions with accuracy and repeatability.

5.2 TEST METHODS

The Xincom 5588 memory test system was used to collect data on the D.C. parametric measurements. The tester allowed data to be taken on each device in an accelerated and accurate manner. The sample size for the D.C. measurements was 36 devices. By using a typically larger sample size, we were able to average measurement values to get a basic feel for the "trend" or average values for a specific parameter. The tests performed on the Xincom were: VOH, VOL, IIH, IIL, IOZH, IOZL, ICC and ISB parameter. Test temperatures used were -55^{O}C, +25^{O}C and +125^{O}C. Note that every test was performed at each temperature and worst case voltage.

5.2.1 VOH, VOL TEST

This test is performed to measure the resultant voltage level on the output when driving a load. For this, test currents are forced into the output and the resulting voltage is measured. The forcing current used for the VOH test is -400uA with VCC equaling 4.5V. The current used for the VOL measurement is 2.1mA with VCC equal to 5.5V. Note that VCC is raised to 5.5 volts when measuring the low output voltage level and is reduced to 4.5 volts when measuring the high output level. By margining VCC in this manner, the worst case conditions are tested .

The average values versus temperature are plotted in Figures 1 and 2. Note that in both tests the maximum VOL (max VOL=0.45V) and the minimum VOH (min VOH=2.4V) as specified in the proposed slash sheet were never exceeded.

5.2.2 IIH, IIL TEST

The IIH and IIL tests are done to determine the amount of current drawn when the inputs have a specified voltage applied to them. This test is conducted by driving an input high and low and measuring the resultant current. Test levels for this parameter were Vin=0V (for IIL) and Vin=5.5V (for IIH), where VCC equals 5.5V. The worst case condition for leakage is when Vin equals 5.5 volts.

Leakage measurements were performed at $-55^{o}C$, $+25^{o}C$ and $+125^{o}C$. The specified limits were +/- 10uA. In general, all measurements yielded extremely low currents of 100nA or less. Currents of these magnitudes are typical in LSI devices using NMOS technology.

5.2.3 IOZH, IOZL TEST

This test measures the output leakage current of the device when its outputs are in the high impedance state. The procedure for this test is to set the device's outputs in the high impedance state by applying a logic "1" to either -CE or -OE input pins. Then force a voltage on the output under test and measure the resultant current.

Two forcing voltages are applied. In the IOZH test, 5.5 volts are applied and in the IOZL test, 0 volts are applied. During this test VCC is set to 5.5 volts which is the worst case condition.

As in the IIH and IIL test (section 5.2.2), the specified limits were +/- 10uA. In general, all measurements yielded extremely low currents of 400nA or less over the full temperature range.

5.2.4 ICC, ISB TEST

This test measures the amount of supply current required by the device for two different operating modes. The first mode is device active (ICC). This mode is the typical operating mode when the device is being accessed. The second mode is standby (ISB). During standby the device's maximum active current is reduced by almost 33%.

The device is placed in the standby mode by applying a logic "1" to the -CE input. When in the standby mode, the outputs are in the high impedance state, independent of -OE input.

To perform the active test, all address inputs and control signals (-OE and -CE) are placed at logic "0". The VCC of the device is at maximum (5.5V). The resulting current is then measured and recorded. The Standby test places a logic "1" on the -CE pin and keeps all other inputs low. The resulting current is measured and recorded.

Refer to Figure 3 (Average Supply Current) and Figure 4 (Average Standby Current) for measured values.

In general, -55^{O}C caused worst case supply current for the active state, while +25^{O}C showed an increase in the standby current. The percentage of the change in the standby current was small compared to the overall range. In both cases, the measured values were well within their maximum limits as specified in the proposed slash sheet.

5.3 TEST SUMMARY

During the -55^{O}C testing, a problem occurred with moisture condensing on, in and under the device socket and thermal insulating pad. This moisture caused false leakage measurements. The devices which failed due to this moisture buildup were retested. The false leakage measurements were not considered valid, hence, they were not included in the overall leakage averages.

In general, the measured D.C. parameters were within the maximum and minimum limits set by the proposed slash sheet.

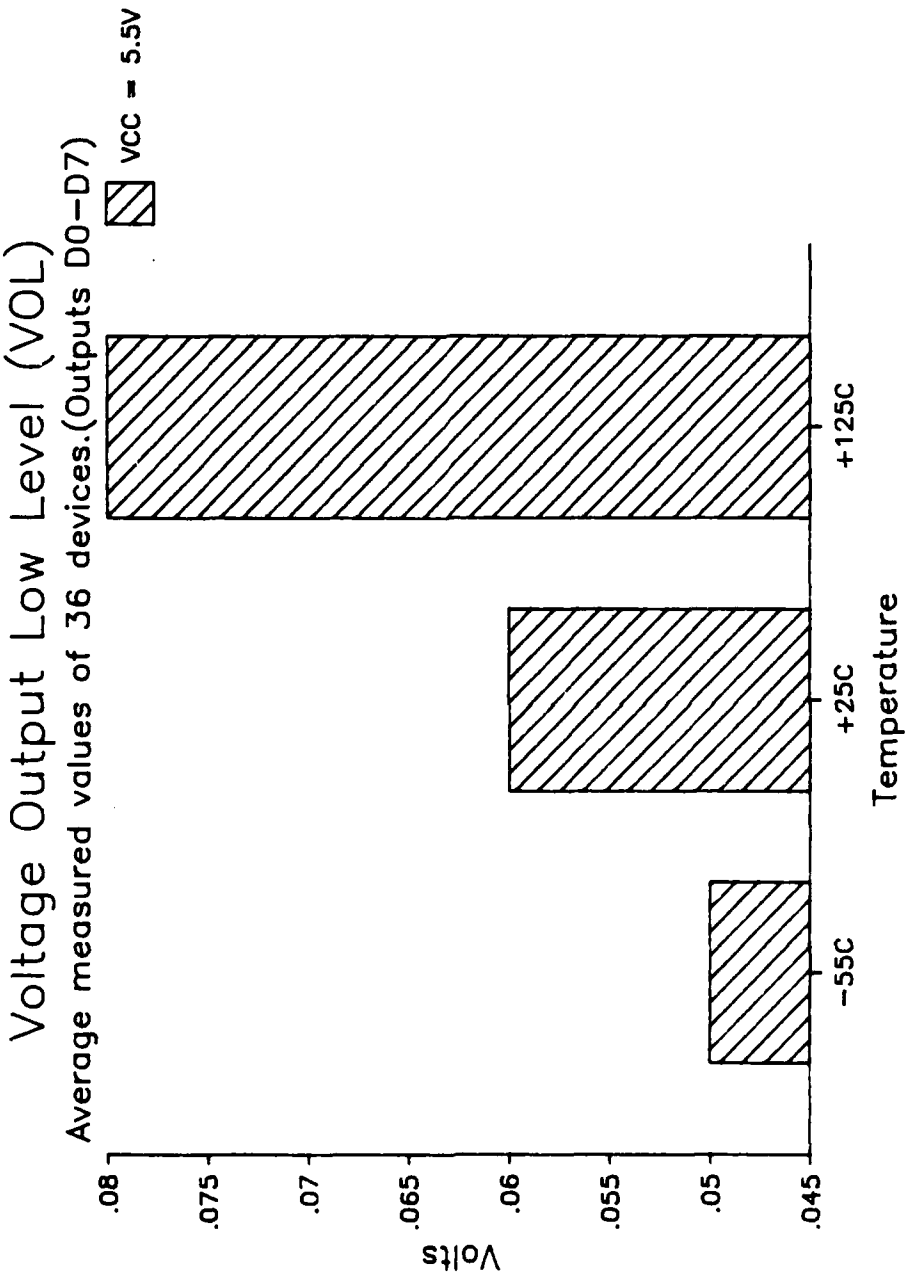

Figure 1: Voltage Output Low Level (VOL)

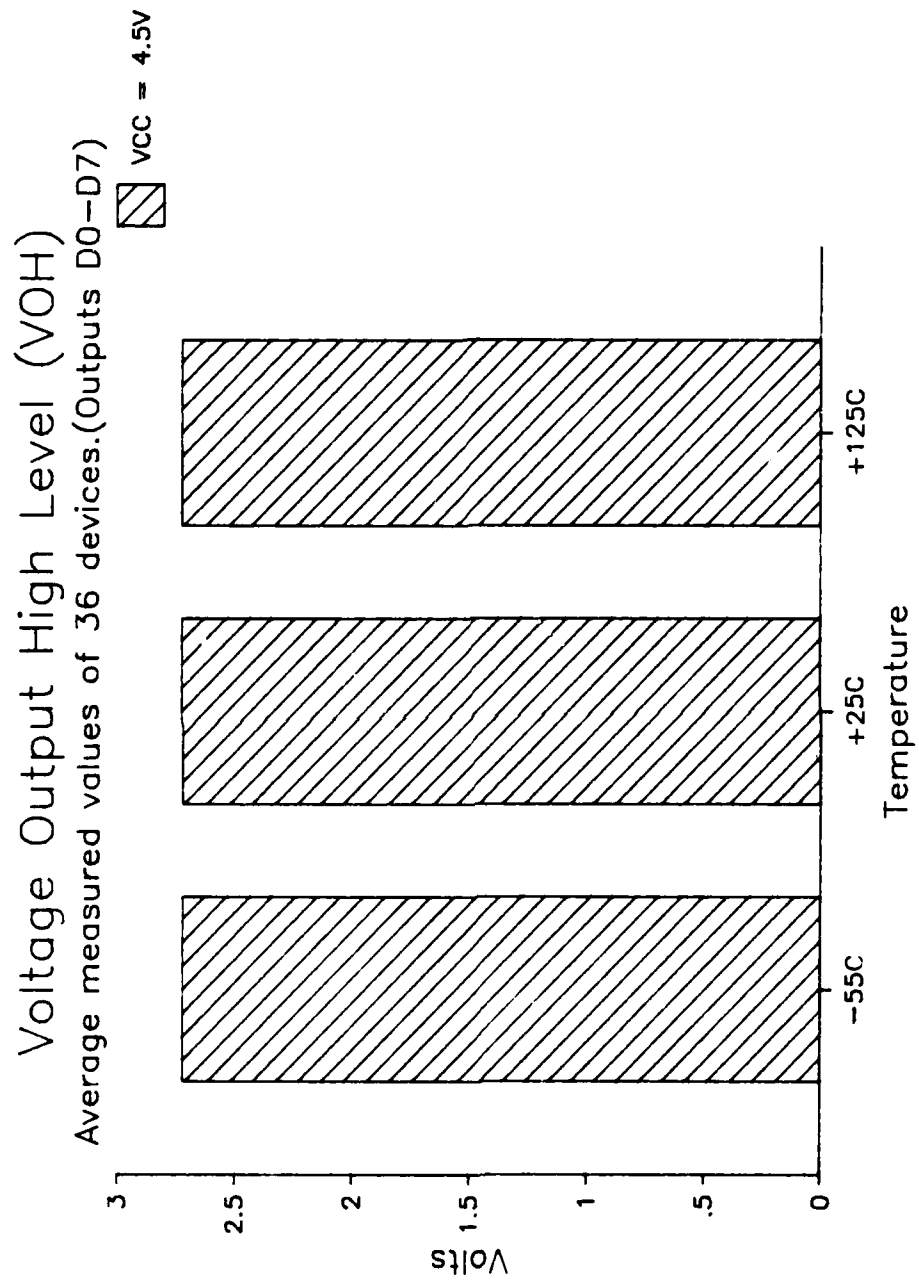

Figure 2: Voltage Output High Level (VOH)

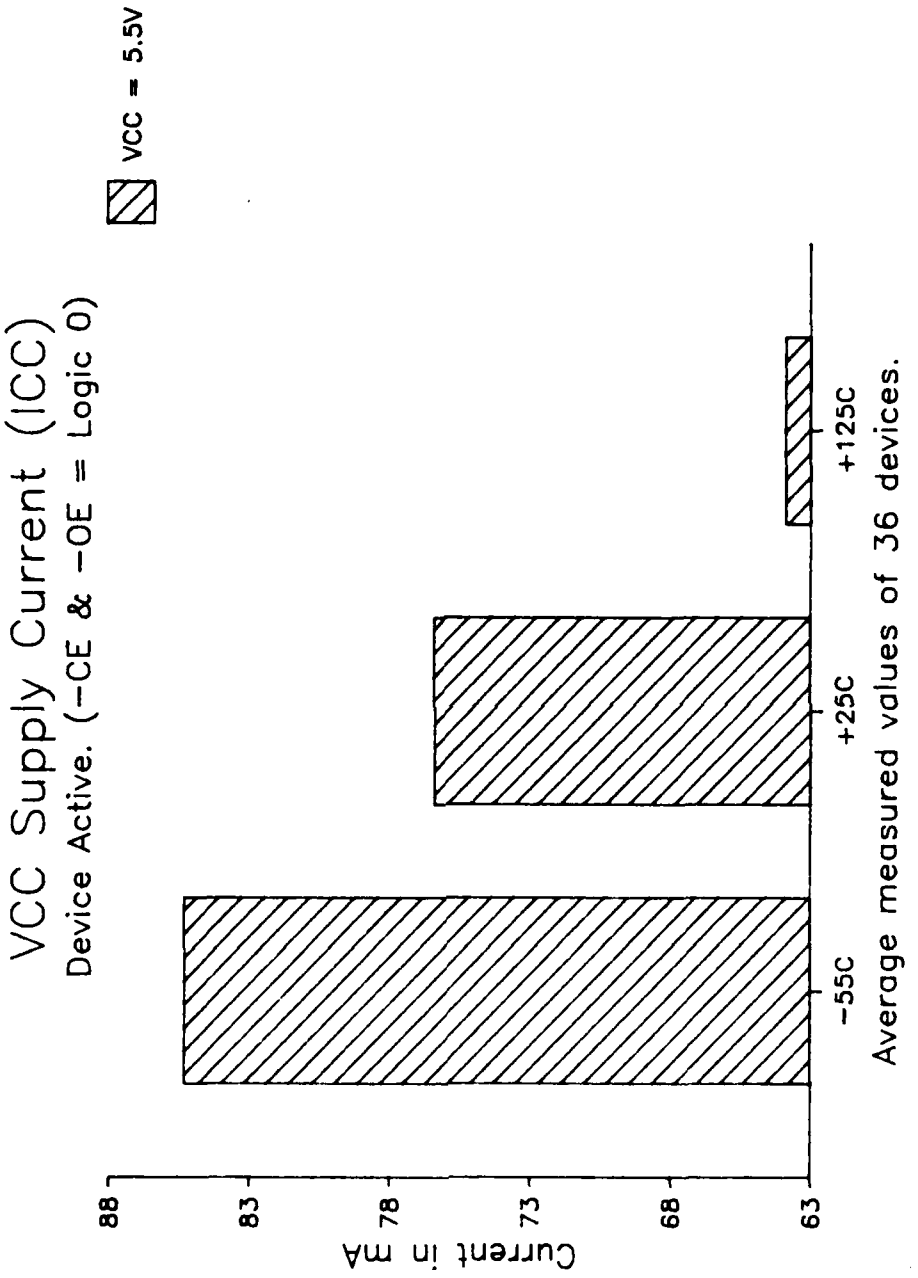

Figure 3: VCC Supply Current (ICC)

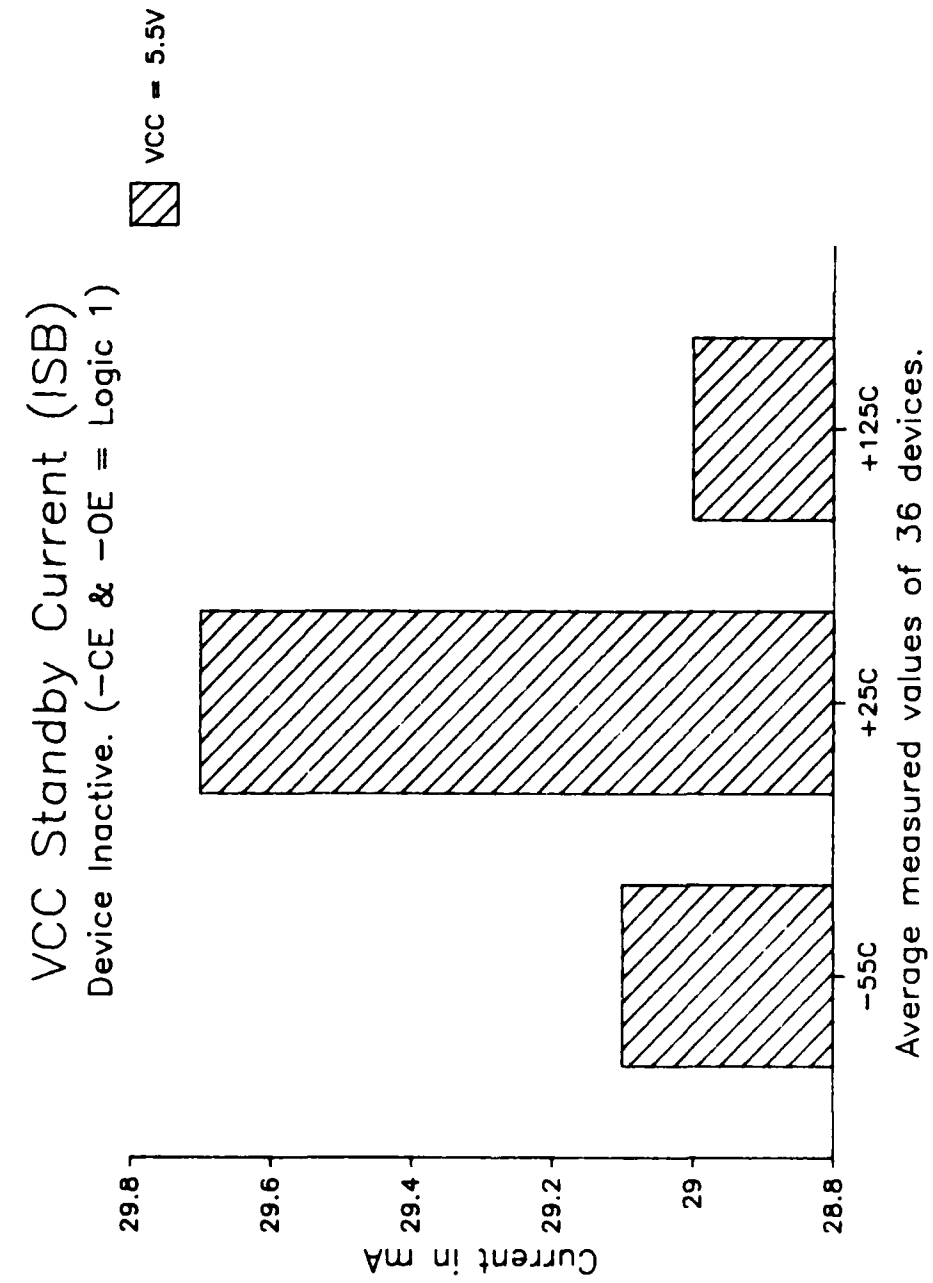

Figure 4: VCC Standby Current (ISB)

6. DEVICE THRESHOLD TESTS

6.1 TEST METHODS

The device threshold test is performed to measure the minimum and maximum margins on the VIL (Voltage Input Low) and VIH (Voltage Input High) levels. These measurements are taken over temperature and min (4.5V) and max (5.5V) VCC levels.

The test consists of programming the device with a pattern and functionally verifying the pattern while varying the input voltage levels. The margin values are measured when the device's outputs no longer match the test pattern.

During this test, the timing parameters are set to a nominal value. Because the timing parameters are set to nominal, the failure can be attributed to the input level.

6.1.1 Address Input Margin Low and High

The address input margin test measured the VIL and VIH level on all address pins (A0-A14). Since all addresses were margined at the same time, the margin value represents the worst address threshold value.

Results of the testing are shown in Figures 5 and 6 which show the effect that VCC and temperature have on the device threshold value. As expected, and indicated by the data, threshold increases with VCC. In addition, changes in temperature have little effect (0.08 volts) on the threshold.

6.1.2 Chip Enable, Output Enable Margin Low and High

The Chip and Output Enable test measures the VIL and VIH level on the -CE (Chip Enable) and -OE (Output Enable) pins. Only the -CE and -OE pins are margined, all other input voltage levels are kept at nominal.

Results of these tests are shown in Figures 7 and 8. As in the address threshold test, the threshold values increase with VCC.

6.2 TEST SUMMARY

In both tests, address and -CE/-OE measured values were within their proposed limits. The maximum VIL level as specified was 0.8 volts. The measured value showed a worst case VIL of 1.25V. This gives a VIL margin of 0.45 volts. The minimum VIH level as specified was 2.0 volts. The measured value showed 1.9 volts. Although close to the 2.0 volt minimum, the measured VIH value was within the proposed limit.

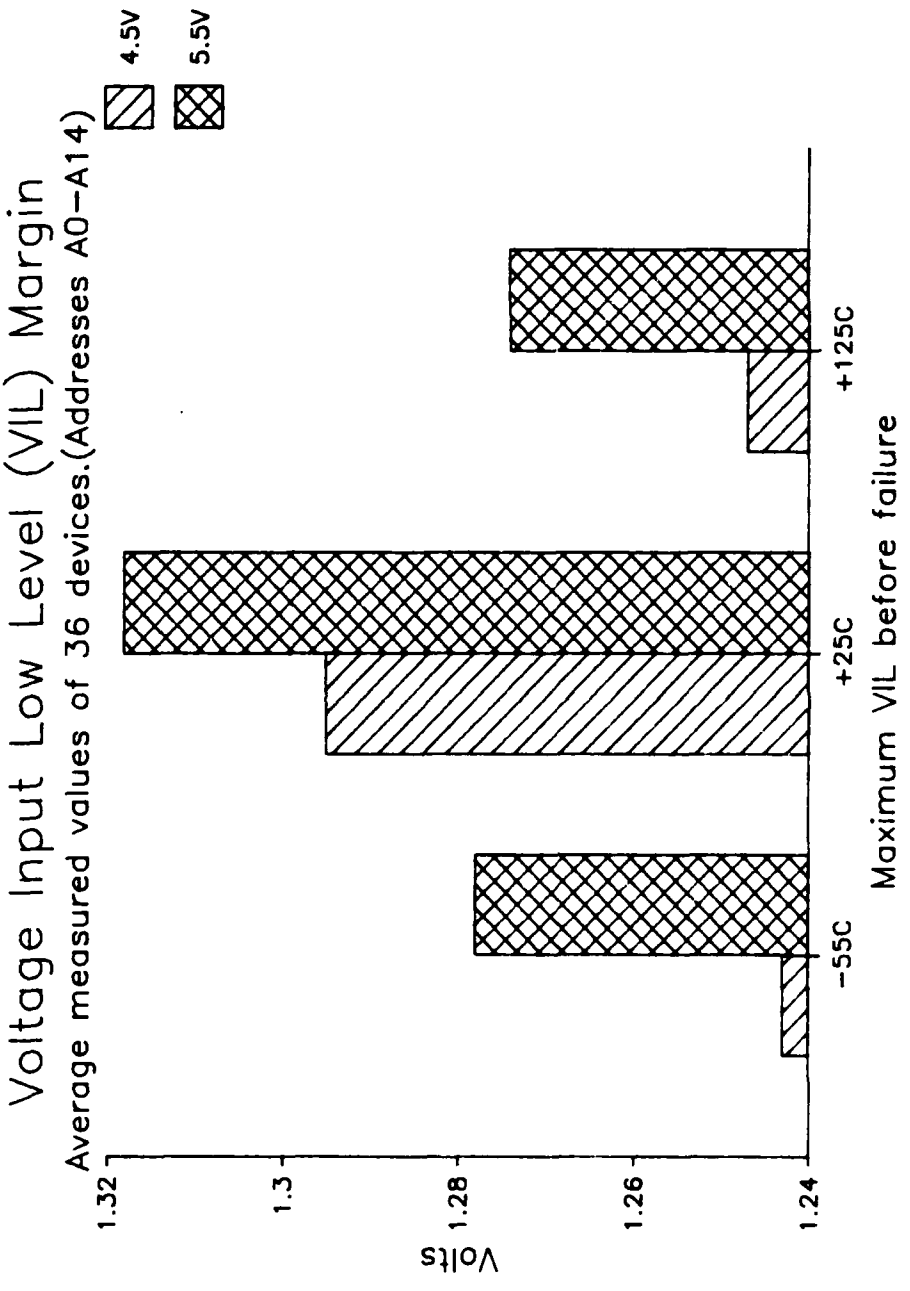

Figure 5: Voltage Input Low Level Margin (VIL) Addresses

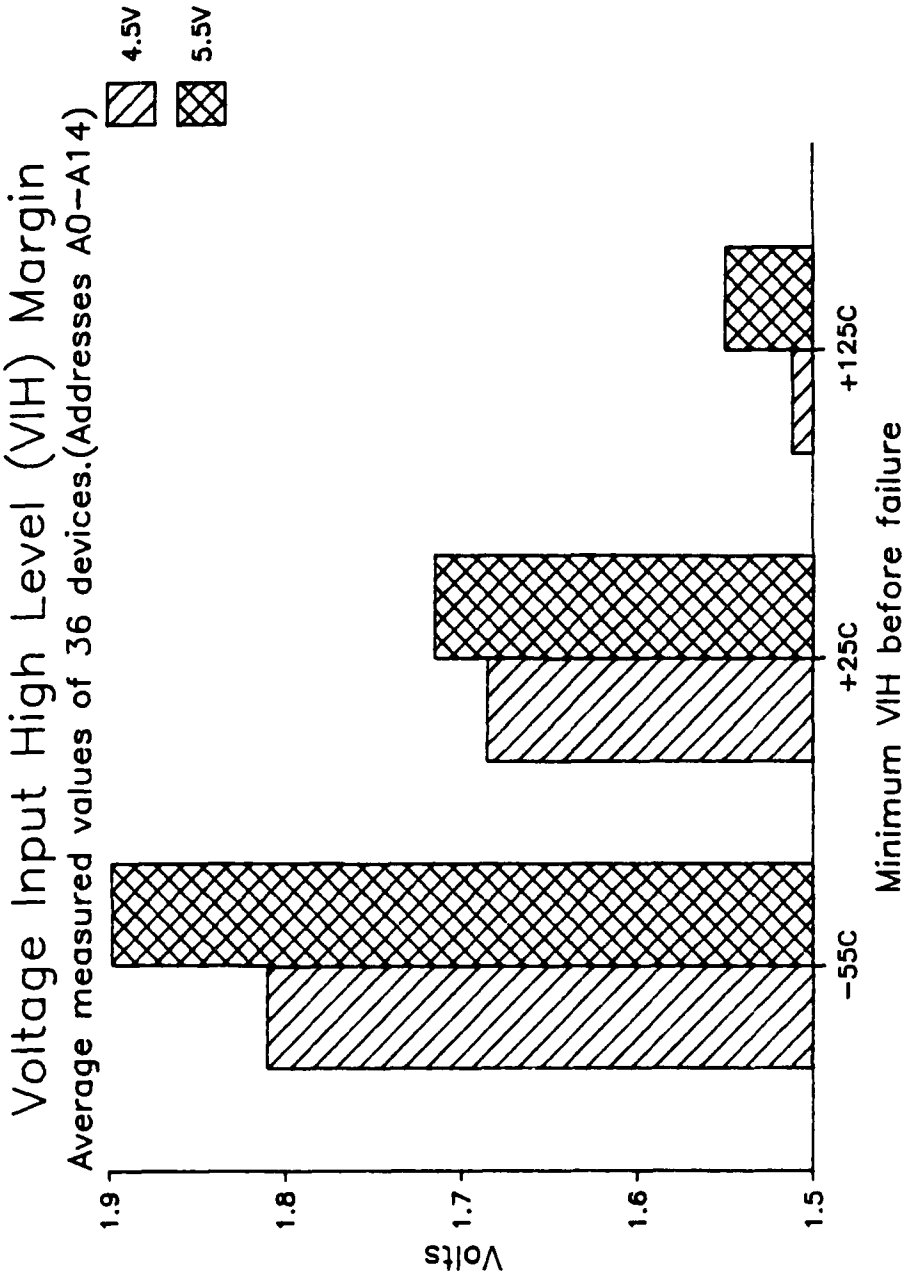

Figure 6: Voltage Input High Level Margin (VIH) Addresses

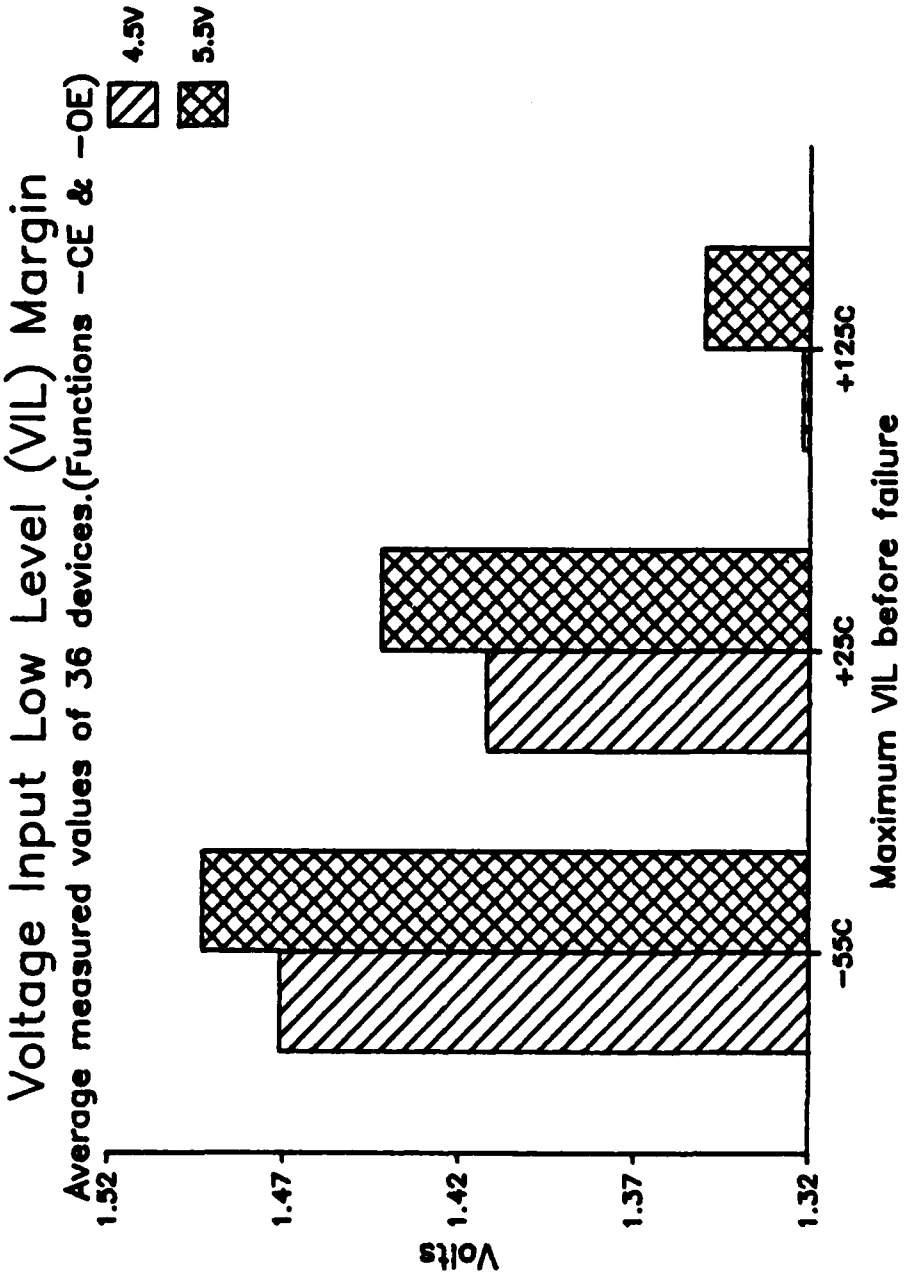

Figure 7: Voltage Input Low Level Margin (VIL) -CE & -OE

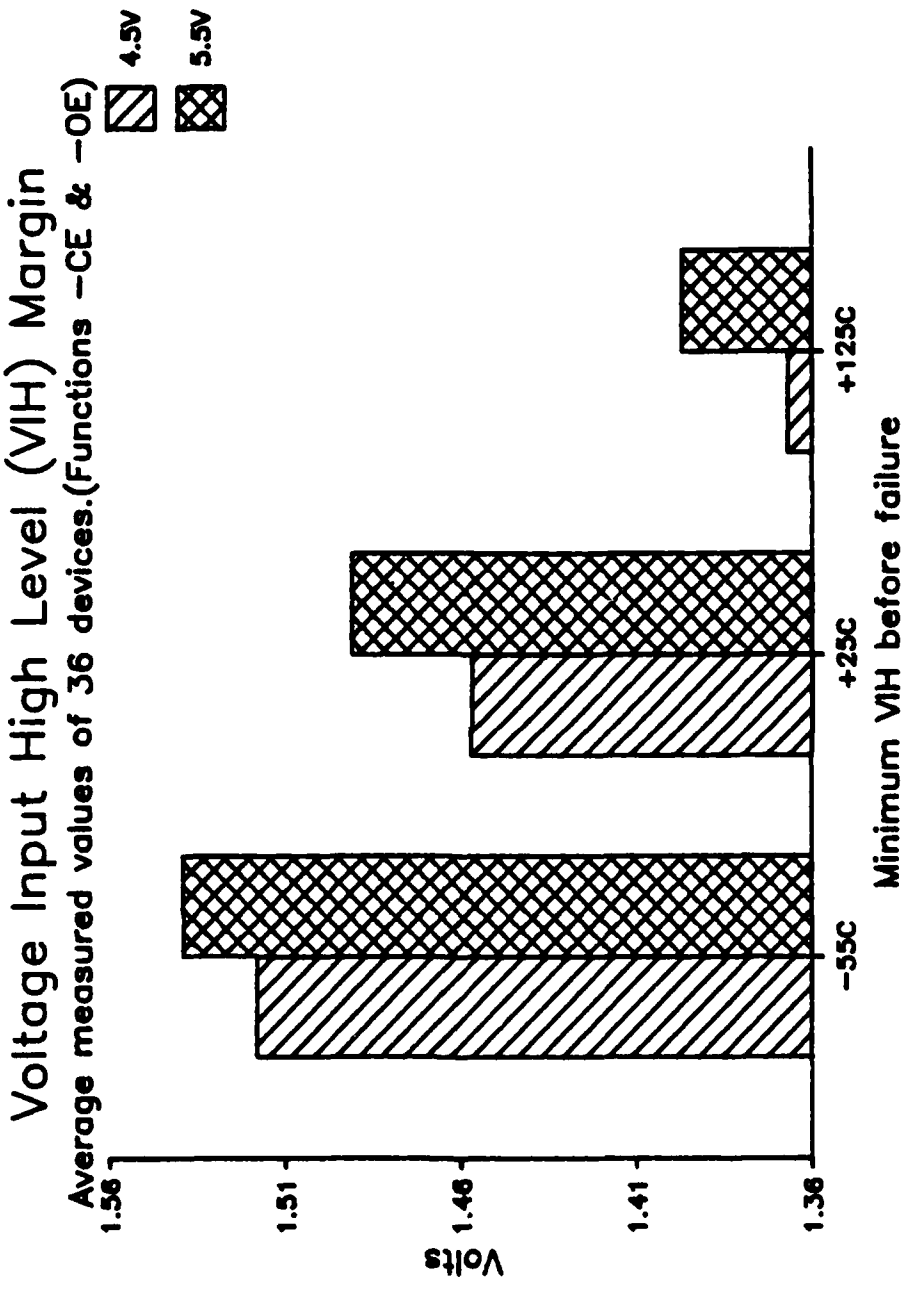

Figure 8: Voltage Input High Level Margin (VIH) -CE & -OE

7. INPUT/OUTPUT CAPACITANCE MEASUREMENTS

7.1 TEST METHODS

Capacitance measurements were performed on six devices. Both input and output pin capacitance measurements were made.

The procedure used was to place the capacitance meter on the input/output pin and measure its capacitance with respect to the device's ground pin. During testing, all pins not under test are left open.

The meter parameters were set as follows:

Frequency = 1MHz
AC RMS amplitude = 50 millivolts
DC bias = 0 volts
Parallel equivalent circuit

Refer to MIL-STD-883C method 3012.1.

7.2 TEST SUMMARY

As a result of the measurements, the data showed that the devices did not have a uniform capacitance with respect to adjacent pins. Referring to Figures 9 and 10, these graphs show input pins 2, 20 and 27 have consistently higher capacitance values then their adjacent inputs. As specified in the proposed slash sheet, the maximum input capacitance is 6pF. In all cases the measured values were below this value.

As compared to the inputs, the measured output capacitance was higher. Refer to Figures 11 and 12 . Again, the test results showed the devices did not have a uniform capacitance. Output pin 15 had the highest measured value but, it was within the maximum specification of 10pF.

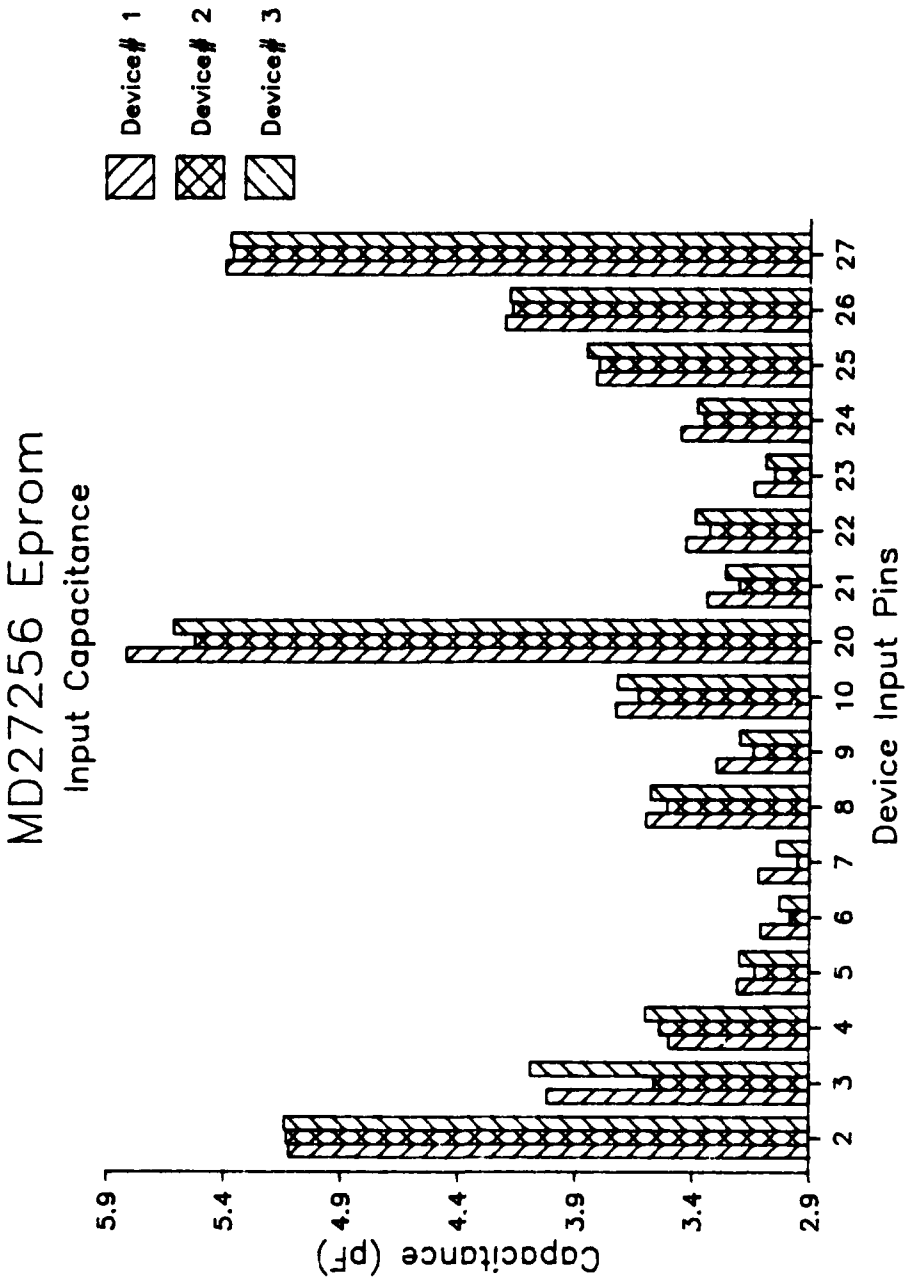

Figure 9: Input Capacitance Measurement Devices 1,2,3

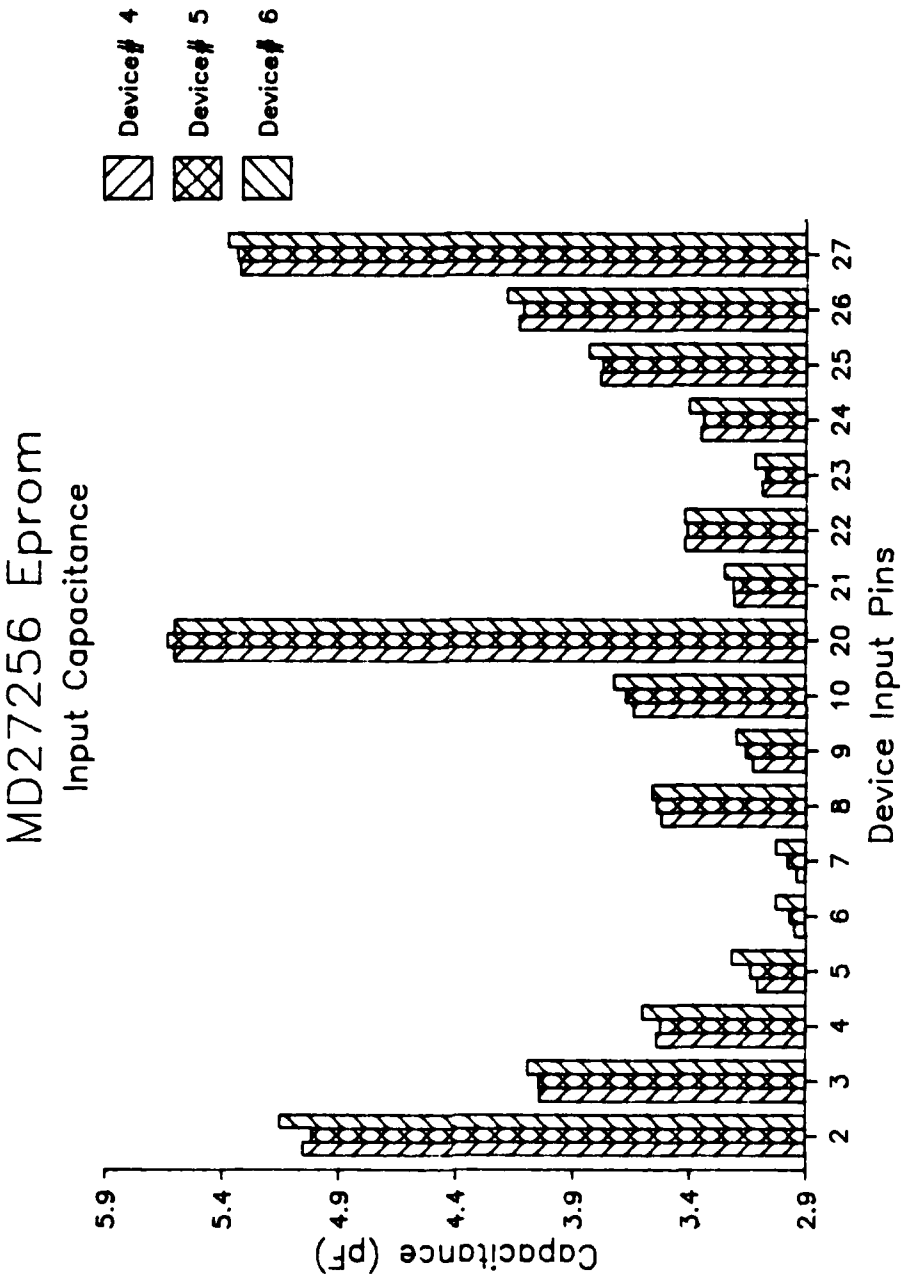

Figure 10: Input Capacitance Measurement Devices 4,5,6

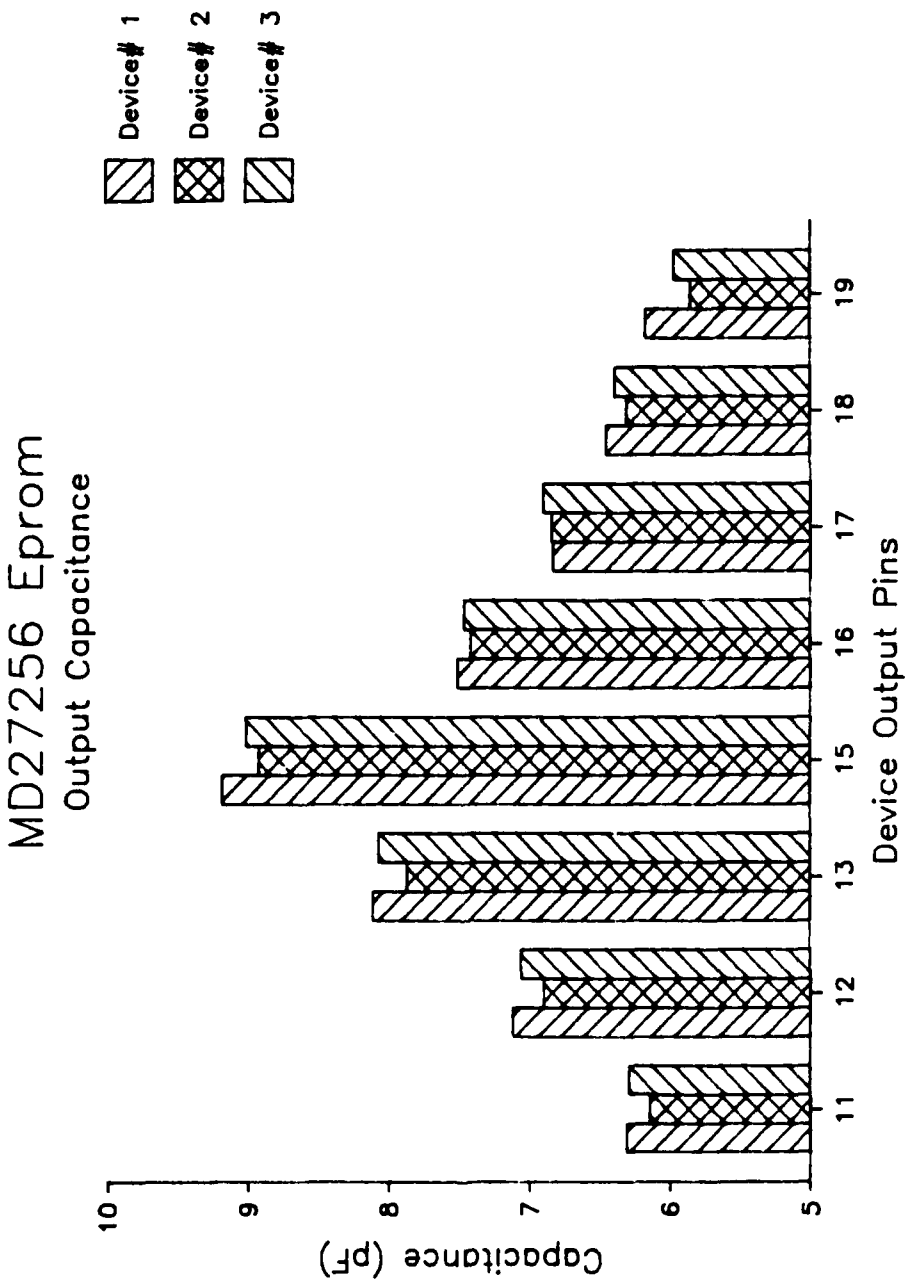

Figure 11: Output Capacitance Measurement Devices 1,2,3

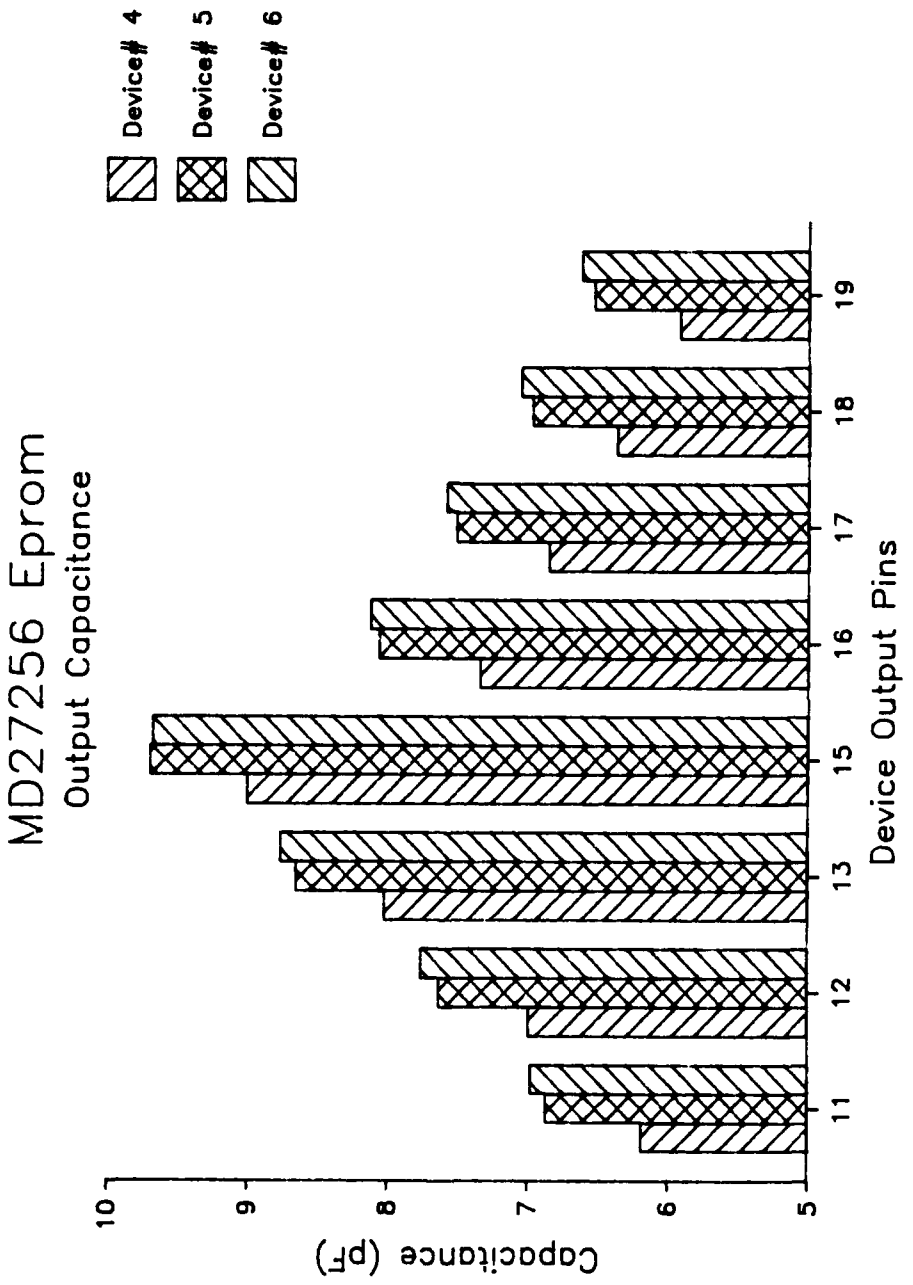

Figure 12: Output Capacitance Measurement Devices 4,5,6

8. ELECTROSTATIC DISCHARGE, VZAP TESTS

8.1 TEST METHODS

This test is performed to measure the electrostatic discharge sensitivity of the devices' input pins. Testing was performed in accordance with MIL-STD-883C method 3015.2 using IMCS model 2400C ESD simulator. After each exposure to an ESD pulse, the devices were analyzed on the Xincom 5588 test system for leakage parameters.

At the onset of this test, the breakdown voltage of the device was unknown. The approach taken was to step the voltage in 250 volt increments until the leakage current exceeded the maximum current of +/- 10uA. After this voltage level was found, it could be used as a starting point for further testing.

Each device pin under test was pulsed until a failure (>10uA) was measured. As the testing progressed, the ESD voltage pulse continually was increased until a failure could be obtained with only one pulse.

8.2 TEST SUMMARY

As described in the test methods, a starting voltage point was determined. From that voltage level, a worst case ESD voltage pulse is determined.

Figure 13 shows input leakage versus applied ESD voltage level. The ESD voltage was applied to the same device pin in steps of 250 volts until the leakage current exceeded the 10uA limit. The Xincom 5588 tester was used to measure leakage measurements after the ESD pulse was applied. The Xincom's PMU (Precision Measurement Unit) current limit was set to 20.5uA. When a value of 20.5uA is shown on a figure, assume the input is shorted. This device showed a breakdown when the voltage exceeded 4000 volts.

Figure 14 shows the leakage versus ESD voltage. The starting ESD voltage voltage level began at 4000 volts. The 4000 volt starting point was determined by Figure 13 's failure point. Notice that the amount of trials before failure has been reduced from sixteen (Figure 13) to six (Figure 14).

The goal is to determine the voltage level required to short or open the input pin with only a single high voltage pulse applied.

Figure 15 shows the effect of starting the ESD voltage at 5250 volts. Notice that the 5250 volt starting point was the failure point on graph 2. The total amount of trials was reduced from six to five, hence, we are zeroing in on the single pulse failure level.

Figures 16 and 17 show the effect of starting the ESD voltage at 6250 and 6500 volts. Notice, it takes only two pulses at these levels to short the device.

Figures 18 and 19 show the effect of one 7000 volt pulse applied to an input. In both cases, the inputs were shorted.

Finally, Figure 20 shows the effect of pulsing 7 different inputs with increasing voltages, in steps of 100 volts up to 6950 volts. Four more pulses with smaller voltage steps were applied as the voltage approached 7000 volts. In all cases a 7000 volt pulse caused the device's inputs to be shorted.

In summary, this device can be rated in category "B" (>2000 volts ESD). The ESD voltage level which causes input leakage failures (shorts) must be greater than or equal to 7000 volts.

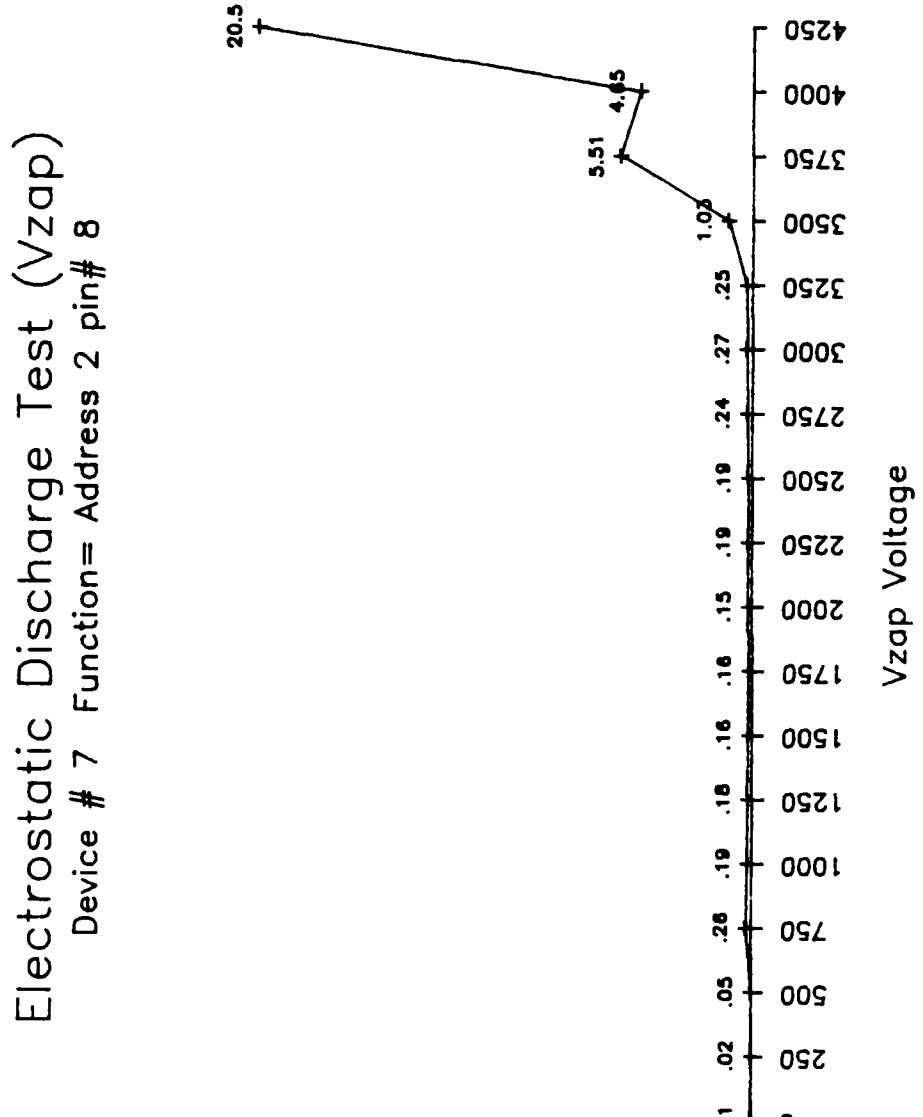

Figure 13: Electrostatic Discharge Test Device#7 Pin#8

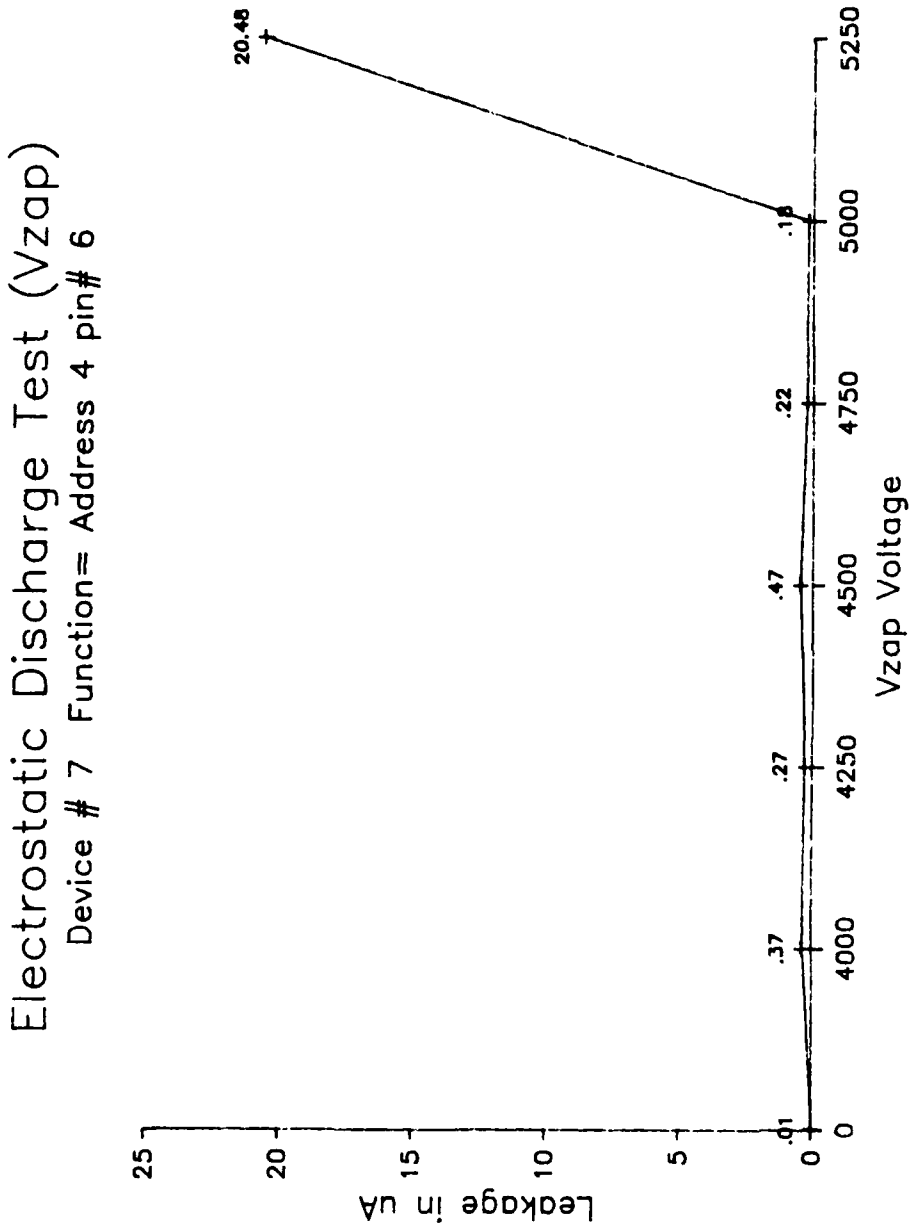

Figure 14: Electrostatic Discharge Test Device#7 Pin#6

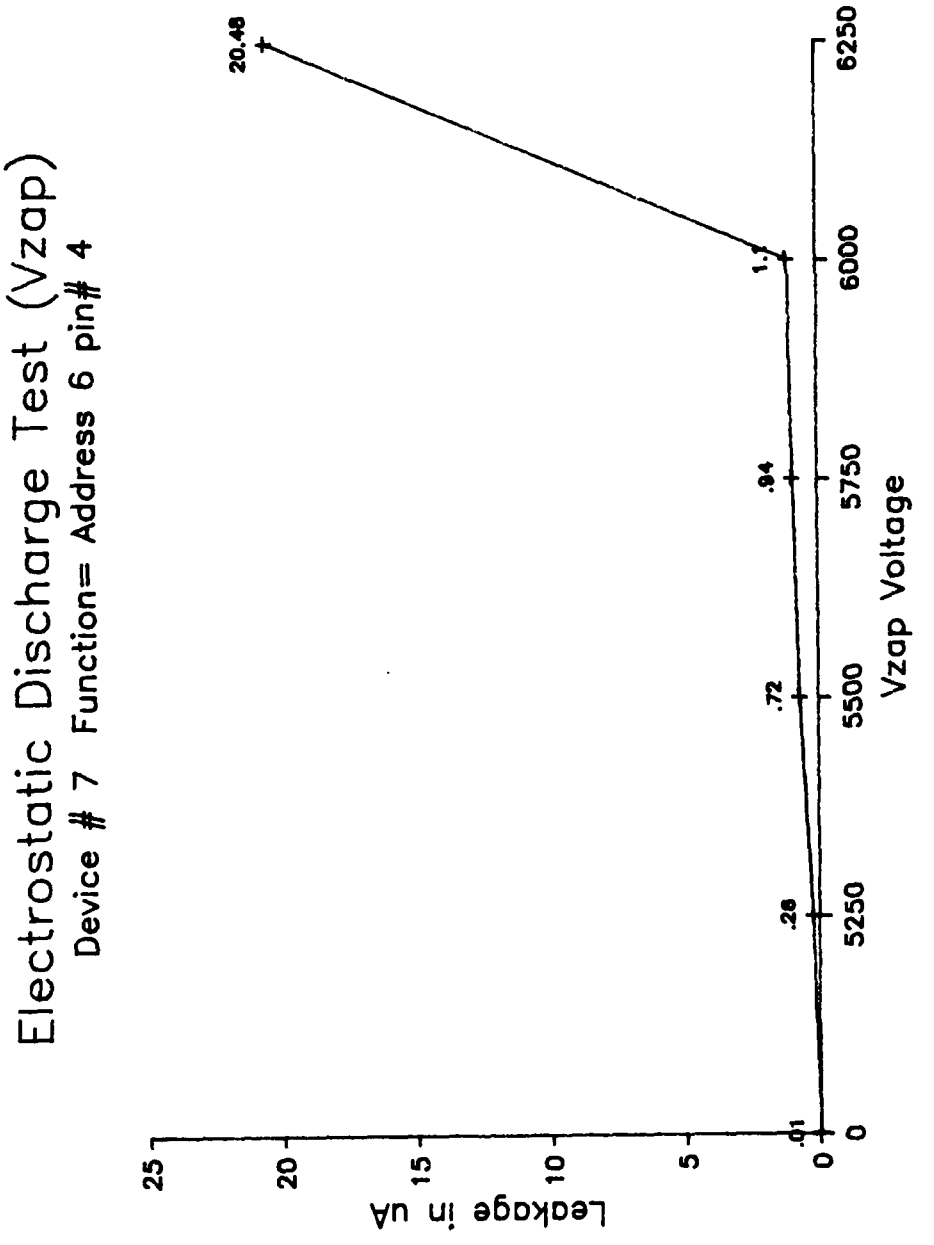

Figure 15: Electrostatic Discharge Test Device#7 Pin#4

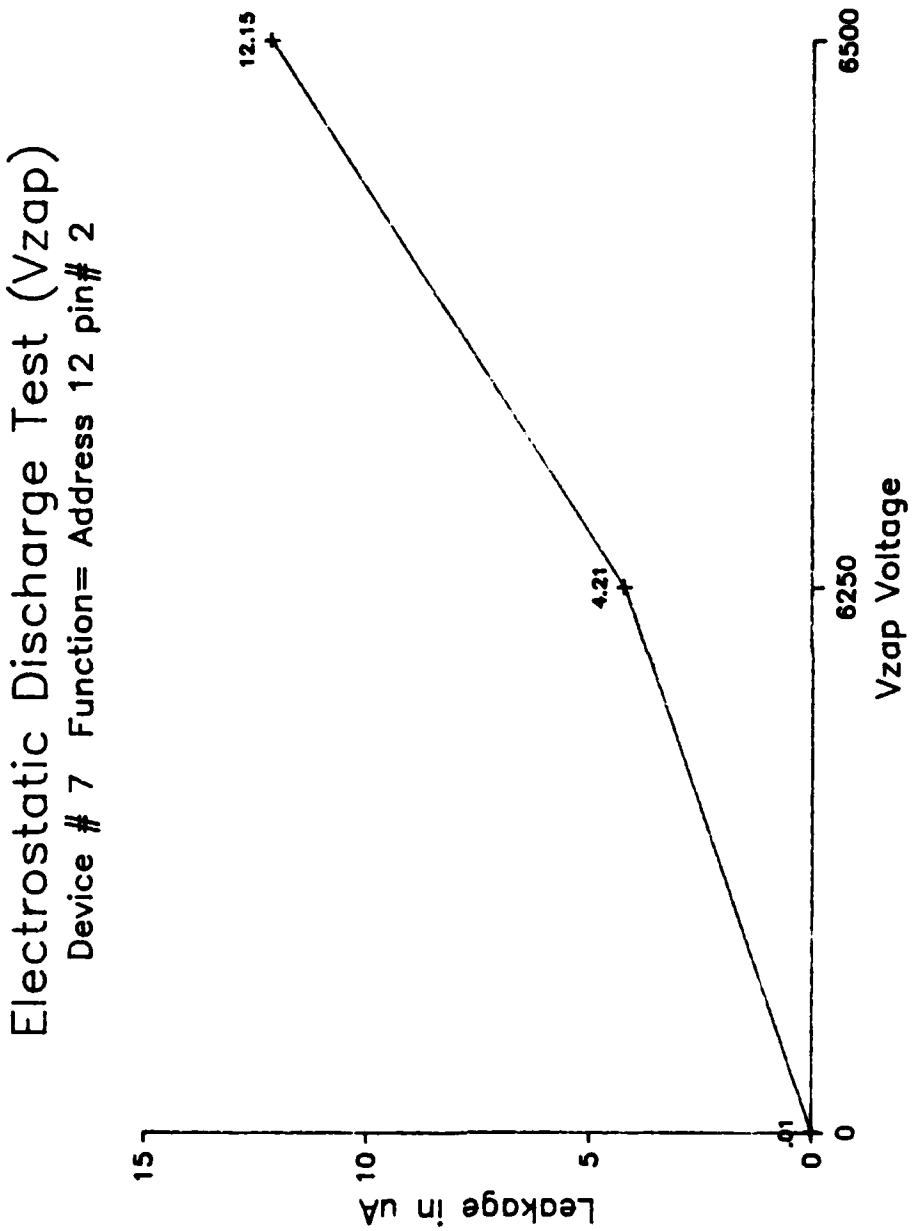

Figure 16: Electrostatic Discharge Test Device#7 Pin#2

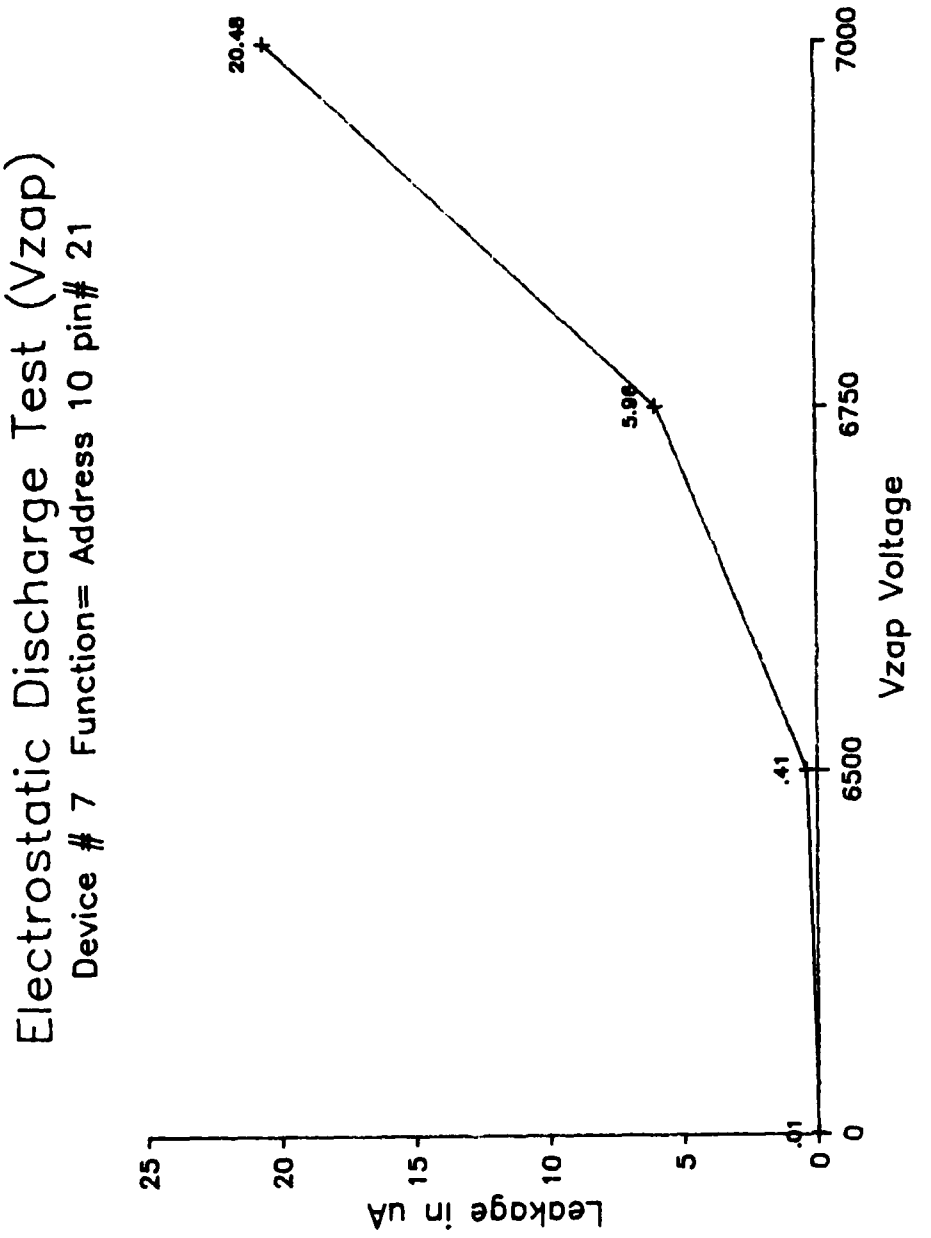

Figure 17: Electrostatic Discharge Test Device#7 Pin#21

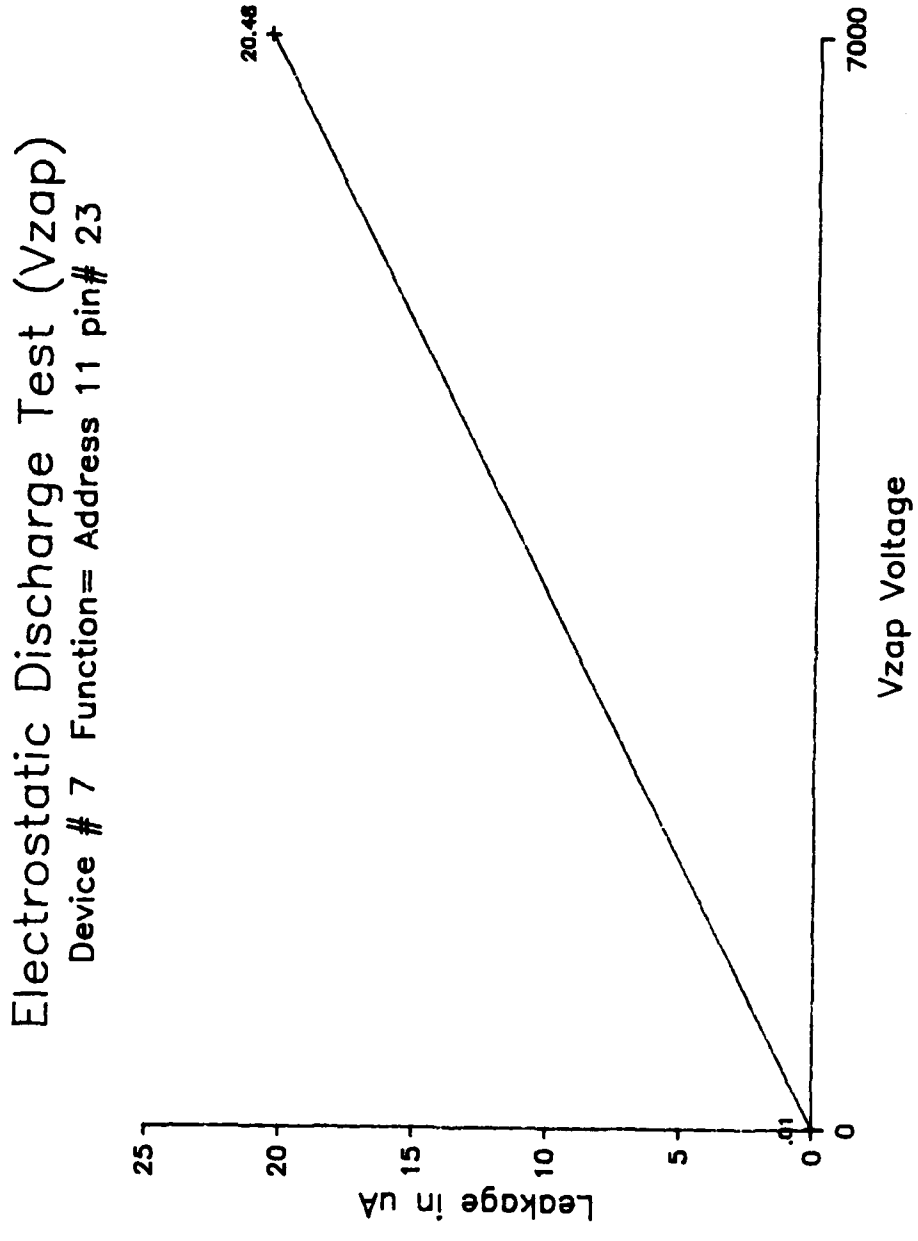

Figure 18: Electrostatic Discharge Test Device#7 Pin#23

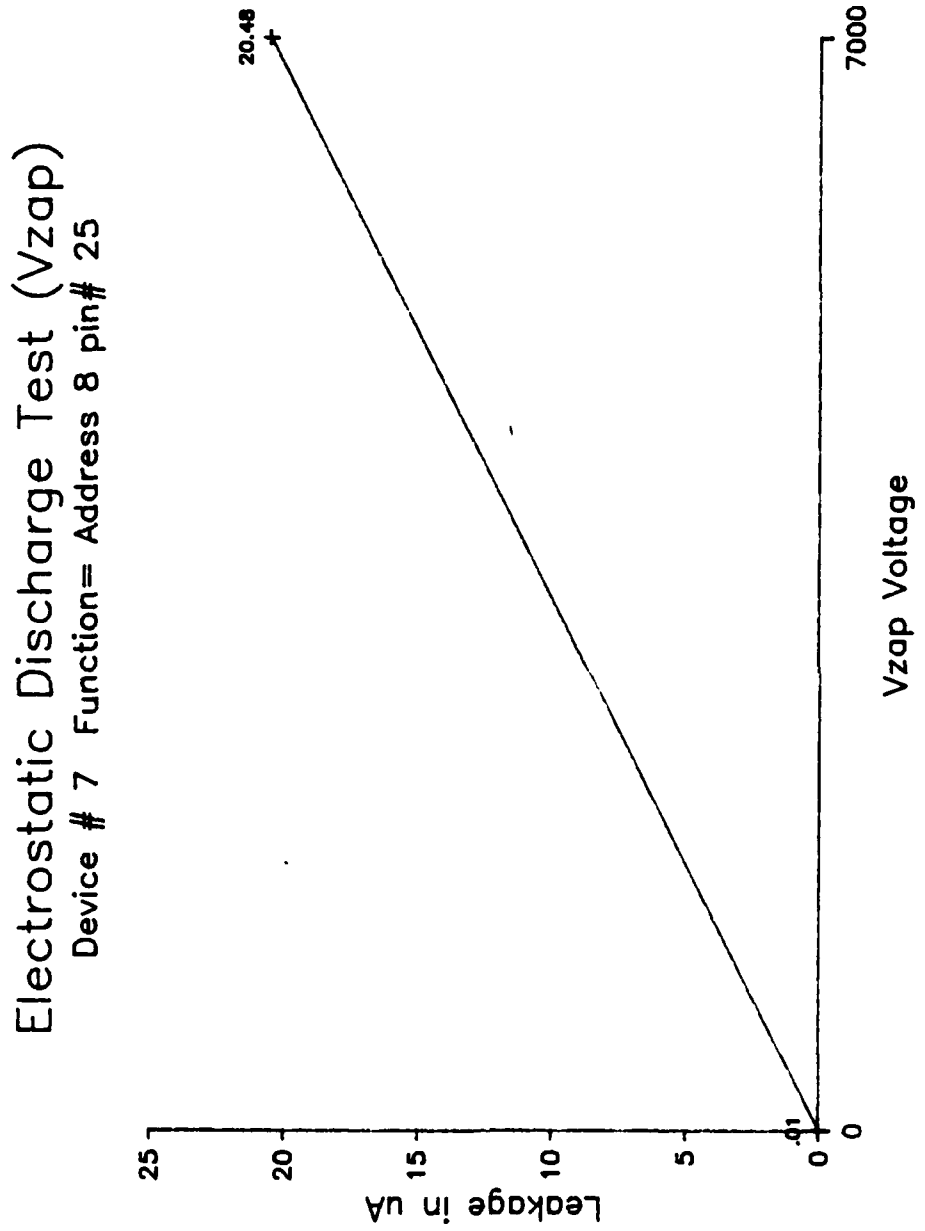

Figure 19: Electrostatic Discharge Test Device#7 Pin#25

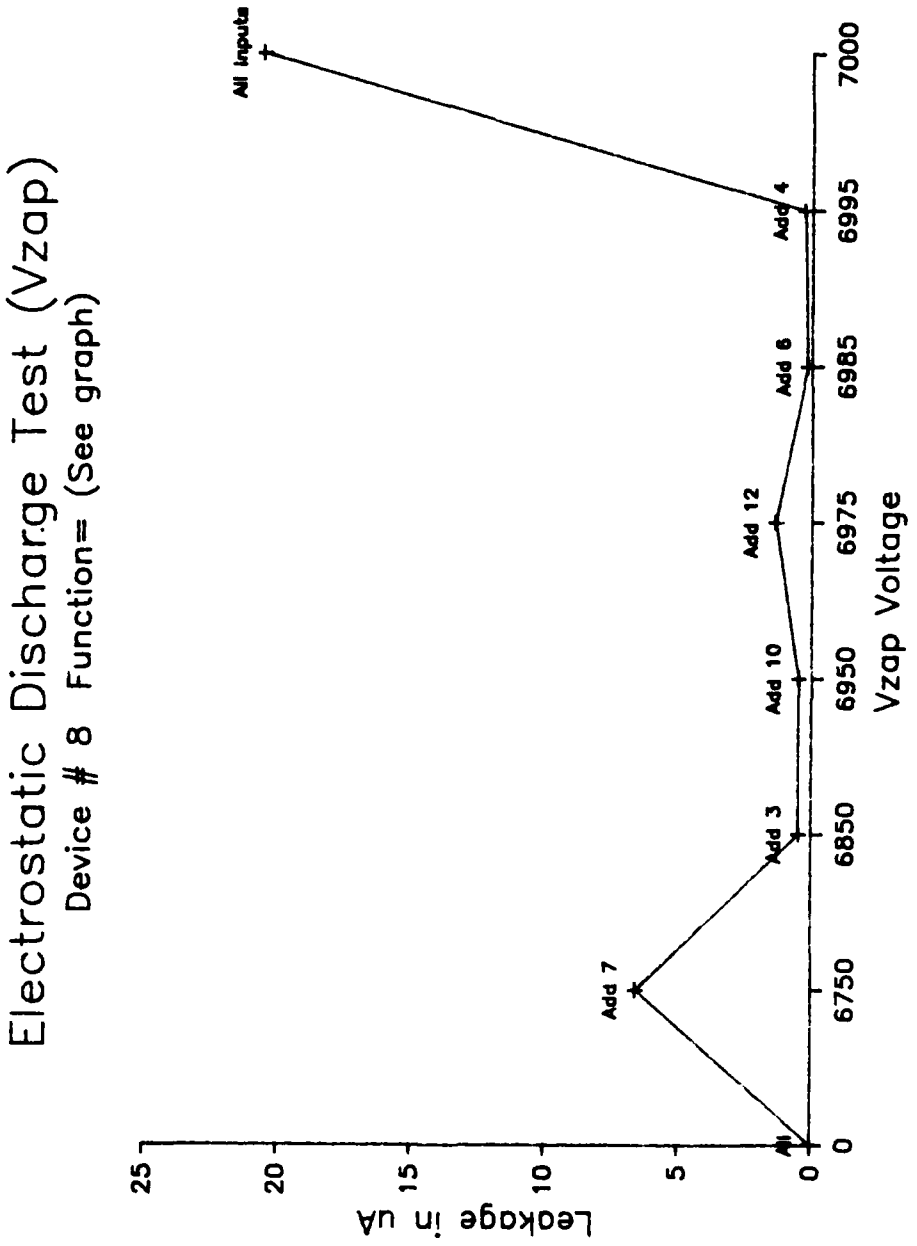

Figure 20: Electrostatic Discharge Test Device#8

9. DYNAMIC CHARACTERISTICS

9.1 TEST METHODS

The Xincom 5588 memory test system was used to collect data on the AC timing parameters. During the characterization of a particular timing parameter, all other parameters were set to their nominal limit or less stringent value. Following this technique guarantees that as the selected parameter is adjusted toward its operating limit, a failure is due to that parameter.

In addition to timing parameters, the capability to program every cell in the device was also checked. All 36 sample devices were characterized over the $-55^{o}C$ to $125^{o}C$ temperature range. The VCC was varied from 4.5 to 5.5 volts. During timing parameter measurements, a load circuit was connected to the outputs. This circuit can be found in Figure 21.

9.2 TEST PATTERNS

To allow functional testing of an EPROM device, a pattern must be programmed into the memory array. Three patterns were used as test patterns for the device.

The first pattern was designed by the vendor to program the worst cells with regards to internal address decoder delays. This pattern consists of programming 95% of the locations in the array with zeros with the remaining locations programmed to ones. The 5% of the locations which have been programmed to ones were selected to provide the worst case address access time delays.

The next pattern consisted of random data. This pattern was generated on GTE's IBM 370 mainframe computer. The random data pattern simulates the eventual data which will be programmed into the device. In this document, the random data pattern is called "TRUE Pattern."

To ensure that every cell can be programmed to a "1" and a "0" another pattern was created by inverting the TRUE Pattern. This pattern is called "FALSE Pattern."

The effectiveness of the vendor pattern versus the random data patterns will be addressed in the AC Test results section.

9.3 A.C. PARAMETRIC MEASUREMENTS

The A.C. characterization not only determines the operating limits of the timing parameters but also verifies the integrity of the internal functions under dynamic conditions. The internal functions of the memory can be divided into the following blocks:

- o Address Decoders
- o Sense Amps
- o Memory Array
- o Data I/O Circuitry

During the A.C. parametric measurements, all of the functional blocks are being verified. For example, when the device's address access time is being measured at $-55^{o}C$, all functional blocks are being subjected to the same extreme temperature.

9.3.1 Address Access Time

The address access time measurement technique used was to first lower the -CE and -OE signals of the device, then 20ns later change the address to a specific location, then check for valid data. The point at which the valid data was verified was determined by a programmable timing generator.

The initial value of the timing generator was set to a known failure point (40ns after address change). The access time measurement loop was setup to increment the timing generator in 1ns steps on failure. This loop continued until the device passed. The criteria for pass/fail was the data outputs of the device matching a known pattern in the tester for the entire address span of the device.

The testing was run at $-55^{o}C$, $25^{o}C$ and $125^{o}C$. In addition, the VCC of the device was changed from between 4.5 and 5.5 volts for each temperature.

Three test patterns were evaluated. All three patterns (INTEL, TRUE, FALSE) were programmed into the device. The effect of temperature, VCC voltage and pattern are shown in Figure 22. As shown, the worst case condition for address access time was high temperature ($125^{o}C$) and low voltage (4.5V). In addition, the INTEL pattern in all cases was less stringent then the FALSE Pattern.

9.3.2 Chip Enable Access Time

As in the address access time measurements, the measurement technique used for the Chip Enable parameter was the same except that both the addresses and -OE (Output Enable) were valid first, then 20ns later the Chip Enable was brought low.

As in the address access time measurements, the worst case temperature ($125^{o}C$) and voltage (4.5V) were the same. Refer to Figure 23. Again, as previously noted, the FALSE Pattern proved to be worst case.

9.3.3 Output Enable Access Time

A prime concern in the design of systems is bus contention. To avoid potential damage to outputs connected to a bus, system timing must be such that each line is driven by only one output at a time. The system designer must therefore know how long it takes a device to respond to an enable signal.

The Output Enable access time measurement shows the effect of temperature, pattern and VCC voltage on this parameter. The measurement technique used was the same as in the address and Chip Enable test with the following exceptions. The addresses and Chip Enable signals become valid first, then Output Enable is brought low after the worst case address access time has been met. This technique allows the data to be waiting for the Output Enable signal instead of causing a possible race condition which would give uncertainty in parametric values.

Figure 24 shows the measured results. Note that the INTEL pattern caused worst case measurements at $125^{o}C$ and 4.5 Volts.

After analyzing the data, it was determined that because the INTEL pattern was comprised of 95% zeros, the capacitors in the load circuit were discharged to a lower level; hence, it took the outputs longer to rise to the VOH comparator level.

9.3.4 Address Hold Time

This test measures the amount of time the data is valid after the addresses change state, assuming that Chip Enable and Output Enable are still active. Using the same technique as performed for access time measurements, the average measured value was 30.7ns at 4.5 volts. When the VCC was changed to 5.5 volts the measured value decreased to 21.5ns.

9.3.5 Chip Enable/Output Enable Float Time

This test mea ures the amount of time required to tri-state the data outputs from an active ..ate. Two control pins (-OE and -CE) have this same function. The voltage at the output pin, at turn off, largely becomes a function of the time constant of the capacitance and load resistances. The output stage actually turns off long before the voltage on the output pin reaches its stable high impedance state.

The technique used to measure this value has typically been to disable the outputs and wait for a 0.5 volt change in voltage level. The 0.5 volt level typically is determined by an arbitrary method. Because of minor variations in the VOH and VOL levels from die to die, the 0.5 volt level is acceptable to many vendors.

The float time when measured on automatic test equipment and using the above method gives inconsistent results. If a device had a lower VOL level it would appear to be slower because the output level had farther to rise, hence, more time was required to reach the absolute D.C. level.

The method used in this characterization is an enhancement from the conventional measurement techniques by the following procedures. First, the device output levels (VOH and VOL) are measured with the output load connected. Then the values are averaged into a VOH average and a VOL average. The comparator limits are set to VOL +100mV and VOH -100mV. The modified VOL and VOH levels are used to determine the float condition.

By using this method, a standardized measurement can be made with high accuracy. When testing this parameter over temperature with the old method, float times would change not only due to the effect of temperature on this parameter but also because the VOL and VOH levels would shift. Using the new method the measurements are self calibrated for the shift in VOH and VOL and give a true measurement of the parametric variation over temperature.

The Chip Enable float time was measured to be 51.6ns with VCC at 4.5 volts. The float time decreased to 47.0ns when VCC was raised to 5.5 volts. The Output Enable float time measured 28.4ns with VCC at 4.5 volts. The float time had a minimal change (-0.2ns) when the VCC was increased to 5.5 volts.

9.4 TEST SUMMARY

During the A.C. measurements, 1 device failed address access time. The address access time exceeded the proposed limit when the temperature was reduced to $-55^{O}C$ and the voltage was 4.6 volts. The device only failed this parameter when it was programmed with the FALSE Pattern.

The address access time was plotted to show the effect of varying the VCC from 5.5 to 4.0 volts. Figure 25, shows the device no longer was able to match the test pattern in the Xincom when the voltage dropped below 4.7 volts.

The access time failure occurred with the FALSE Pattern only. The other two patterns (INTEL, TRUE) were run, but no failures were detected. The failure was caused by a faulty address decoder. This failure was not detected by the other two patterns, because the locations which were selected by the faulty decoder had the same data that the tester was comparing for.

If only one test pattern would have been used, this error would have been masked. To increase device integrity, the use of multiple patterns being programmed into the device during A.C. parametric measurements is recommended.

In general, the measured A.C. parametric values were within the maximum and minimum limits set by the proposed slash sheet.

A.C. TESTING LOAD CIRCUIT

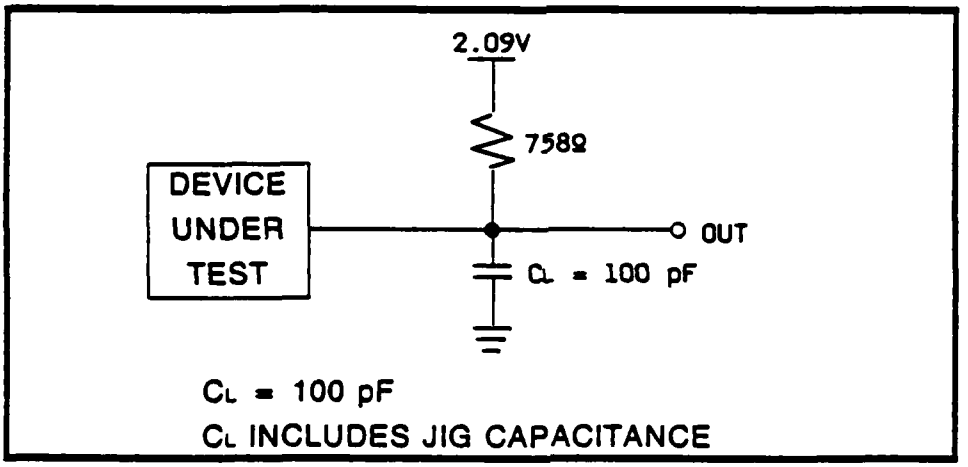

Figure 21: Output Load Circuit

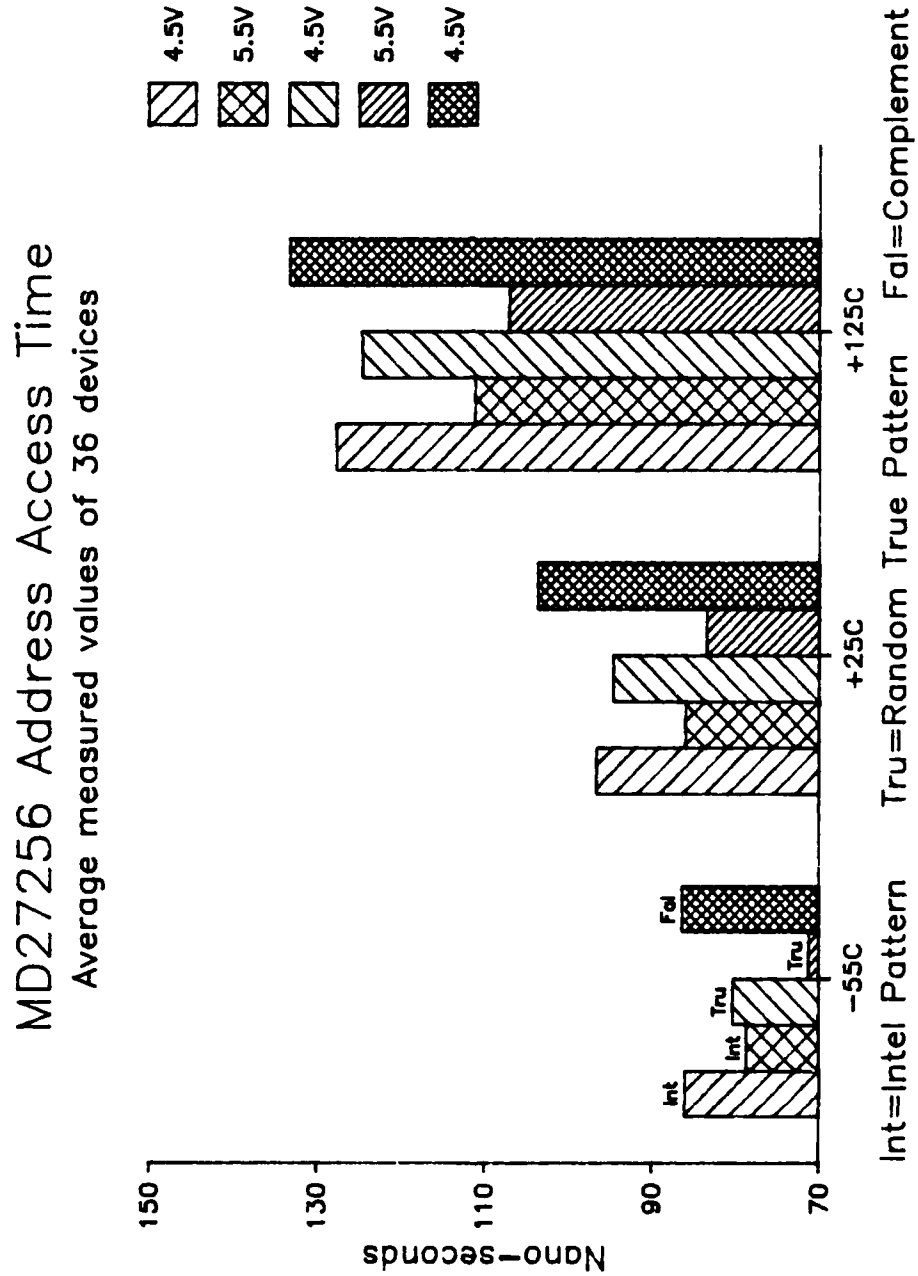

Figure 22: Address Access Time VS Temperature and Pattern

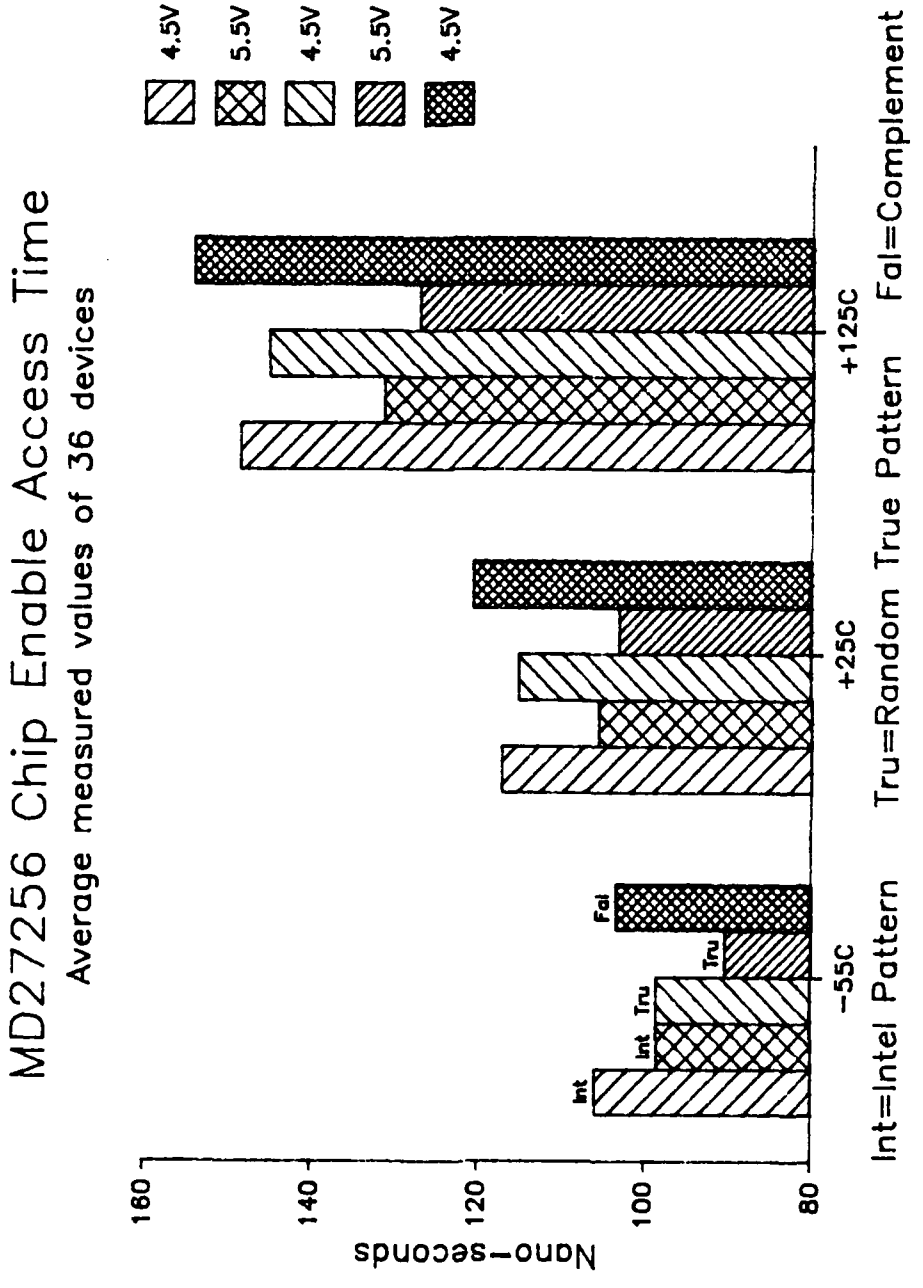

Figure 23: Chip Enable Access Time VS Temperature and Pattern

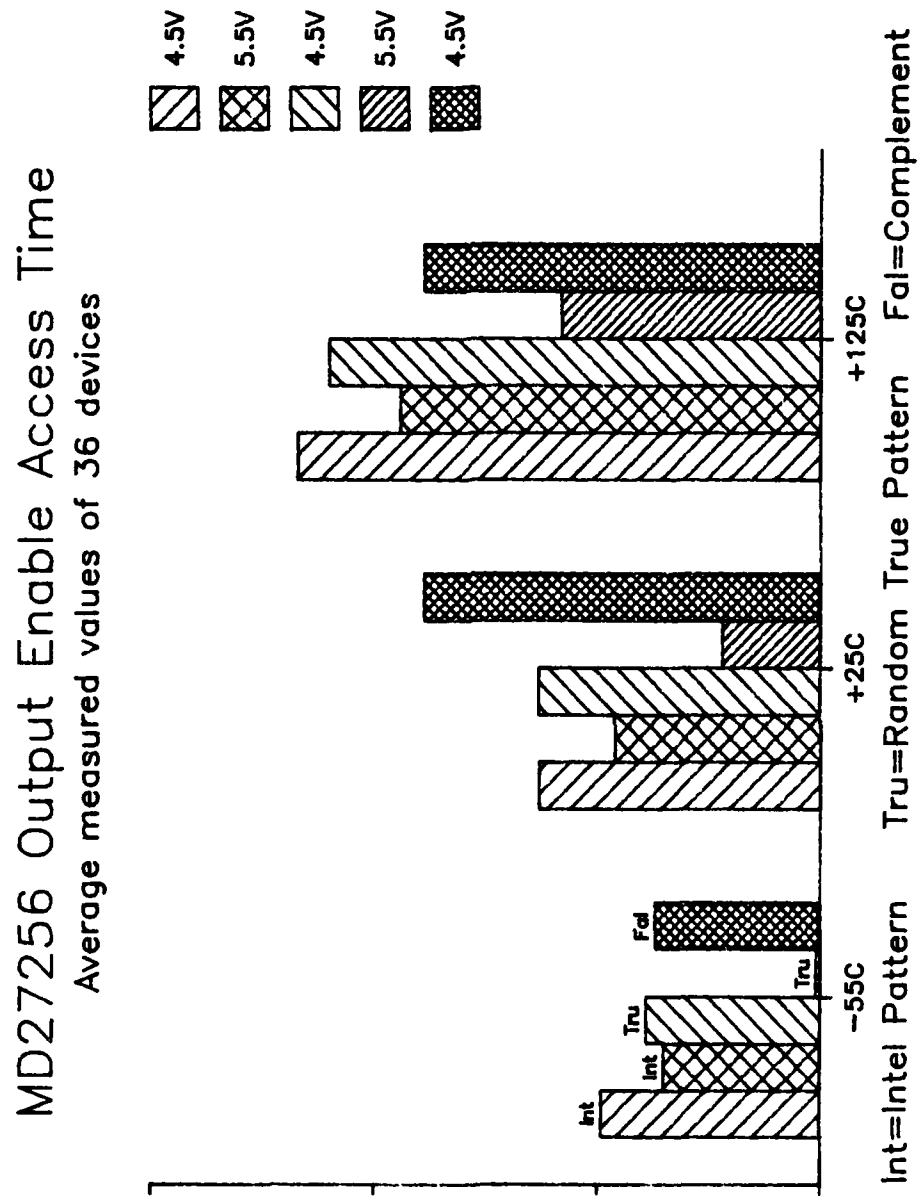

Figure 24: Output Enable Access Time VS Temperature

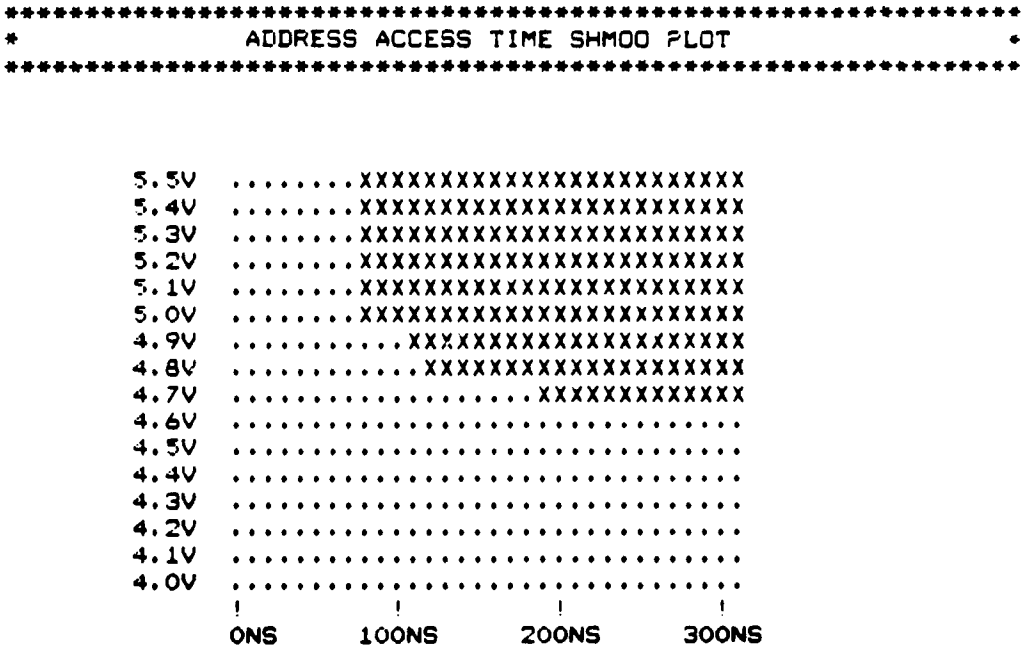

Figure 25: Address Access Time SHMOO Plot Device# 12

10. FLOATING GATE MARGIN MEASUREMENTS

10.1 OBJECTIVES

This test is used to determine the amount of trapped charge (margin) stored on the floating gate of the EPROM cell. The principles of UVEPROM [2] are best explained by the operation of the floating gate storage cell. The storage cell consists of two polysilicon gates, a conventional control gate, and an electrically isolated floating gate. The floating gate has two stable states, an erased state, and a programmed state. Programming is accomplished by raising both the drain and control gate to a high voltage causing a high electric field. Electrons traveling in the channel are accelerated by the field and some gain enough energy to leave the channel, transverse the oxide, and become trapped on the floating gate. Once trapped on the floating gate, they remain there, unless erased by exposure to UV light.

The threshold voltage of a cell properly programmed as a "0" is greater than approximately 7.0 volts, while that of a properly erased "1" is approximately 1.5 volts. During a read operation, the control gate is biased to approximately 5.0 volts (determined by VCC and the read mode program voltage VPP). IDS will flow only for a VT < 5.0 volts, providing the basis for sensing the cell's state. The difference between the programmed (or erased) threshold voltage and the 5.0 volts sense voltage will be called the margin of the device.

Three tests were performed to measure margin. The first test measured the effect of a high temperature bake (90 hrs. at 140^{o}C) and dynamic burn-in (168 hrs at 140^{o}C) on margin value. The second test measured the amount of time required under a known UV lamp intensity to cause a programmed cell to erase. This test will show the weakest cell in the array. The last test performed measures the amount of time required to erase the entire array.

10.2 TEST METHODS

To measure margin values, a test was developed to run on the Xincom 5588 test system. Because the test was implemented on an automatic test system, the accuracy and repeatability of measurement values could be done with high levels of confidence.

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[2] Excerpt from RADC-TR-80-401, Part 2. A096065.

Because of the structure of the EPROM cell, the test could be implemented with minimal effort. Basically, the voltage on the control gate in the EPROM cell is directly linked to the VCC and VPP pins of the device. The device is first programmed with all zeros, to place the maximum amount of potential on the floating gate. Then, the VCC and VPP are raised until the outputs switch state (0 to 1). The voltage at which the outputs switch can be directly correlated to the margin value. The technique used during the testing was to run a function test (nominal timing) which verified all locations before stepping the voltage. The voltage step was set to 0.05 volts. The maximum voltage limit must be observed. Typically, the voltage can be raised to 8 volts without damage to the device. If the 8 volt limit is reached, the assumption can be made that the margin is greater than 2.5 volts which gives more than adequate data retention. The above method was used for all the margin tests performed.

10.3 MARGIN TESTS

10.3.1 Margin VS Burn-in and Bake.

This test measures the effect of a bake (90hrs/140^{o}C) and dynamic burn-in (168hrs/140^{o}C) on the EPROM's floating gate margin value. Initially, the devices were programmed with all zeros. Then the margin values were measured and recorded. Next, the devices were baked at 140^{o}C for 90 hours, and again, the margin values were measured. Lastly, the devices were subjected to a dynamic burn-in of 140^{o}C for 168 hours. In Figures 26 thru 32, the burn-in test will be represented by the "DBRN" symbol. The margin values again, were measured and recorded.

Refer to Figures 26 thru 32. As shown, 24 of the 36 devices showed no degradation of their margin values. Ten devices had their margin values decrease as expected. Two devices, 20 and 30, gained charge on their floating gates after bake and dynamic burn-in. At present, the gaining of charge on a floating gate, induced by high temperature and bake, is a phenomenon which warrants additional investigation.

In all cases, the margins on the floating gates of the devices tested were all well above the recommended 0.5 volt limit to ensure extended data retention.

10.3.2 Margin VS UV Light Exposure (Weakest Cell)

This test measures the amount of time required to erase the weakest cell in the memory array. The device is programmed with all zeros and a UV lamp is placed 1 inch above the device while the measurements are being taken.

Refer to Figures 33, 34 and 35. The test procedure is the same as described in measuring the floating gate trapped charge margin test. A system timer in the Xincom is started when the test begins. Referring to the graphs, when the margin value drops below the zero level, the device no longer is fully programmed with zeros. The zero level correlates to the 5.5 volts on the VCC and VPP of the device.

Device# 11, as shown in Figure 33, takes 1 minute 9 seconds before the weakest cell loses sufficient charge to fail the all zeros test.

The UV lamp intensity measured 2380 uW/cm^2. If this intensity were multiplied by the 69 seconds (1 minute 9 seconds), the required dosage to cause a pattern failure could be as low as 0.164Wsec/cm^2.

As a result of the exposure test, low doses of UV light, for a short amount of time, can cause data loss. Extreme caution should be used when the programmed device does not have a window cover applied.

10.3.3 Margin VS UV Light Exposure (Total Erasure)

This test measures the amount of time required to lower the floating gate margin sufficiently enough to cause an all zeros pattern to be read as all ones, by exposing the device to a UV lamp with an intensity of 2380 uW/cm^2. Again, the testing procedure is the same as the floating gate margin test.

The device is first programmed to all zeros. The Xincom tester is loaded with a test pattern of all ones. The UV lamp is placed on the device while the measurement is being made. The system timer is started and the test begins. When the device passes the functional test pattern in the Xincom system, it has been erased. Let it be stated that, because the device is erased enough to pass an all one's pattern, it does not necessarily mean the device has been fully erased. What is shown is that the margin of the cells has dropped below the threshold of the sense amplifiers. Additional erasure is recommended.

Typical test results show an exposure time of 2 minutes and 30 seconds to lower the margin enough to read all ones.

Again, this does not mean the device has been fully erased. It only means that the time required to change the floating gate margin to a point which is just below the sense amplifiers threshold level is small, when compared to the recommended exposure dose of 15 to 20 minutes with a UV lamp intensity of 12000 uW/cm^2.

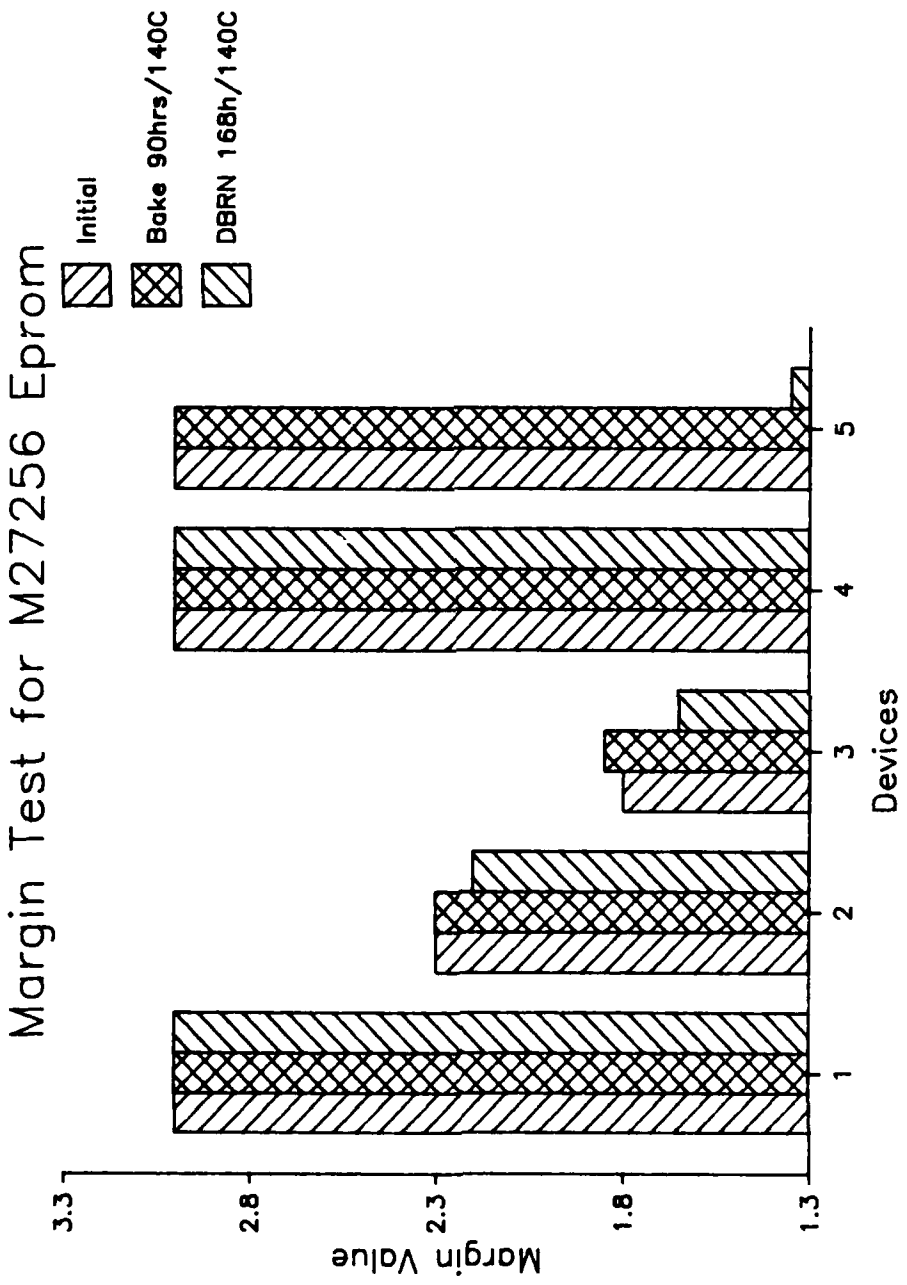

Figure 26: Floating Gate Margin Test Device#'s 1 thru 5

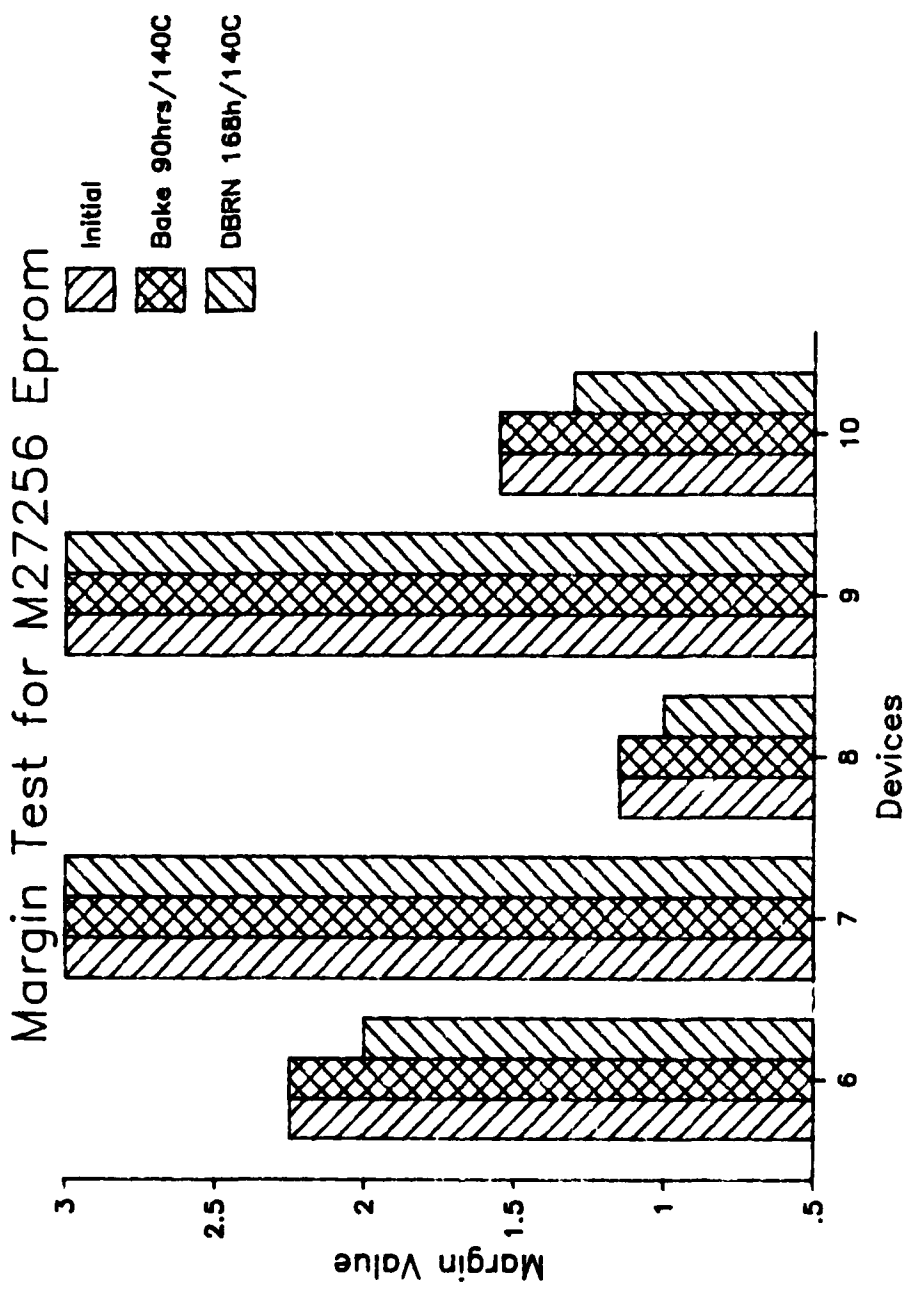

Figure 27: Floating Gate Margin Test Device#'s 6 thru 10

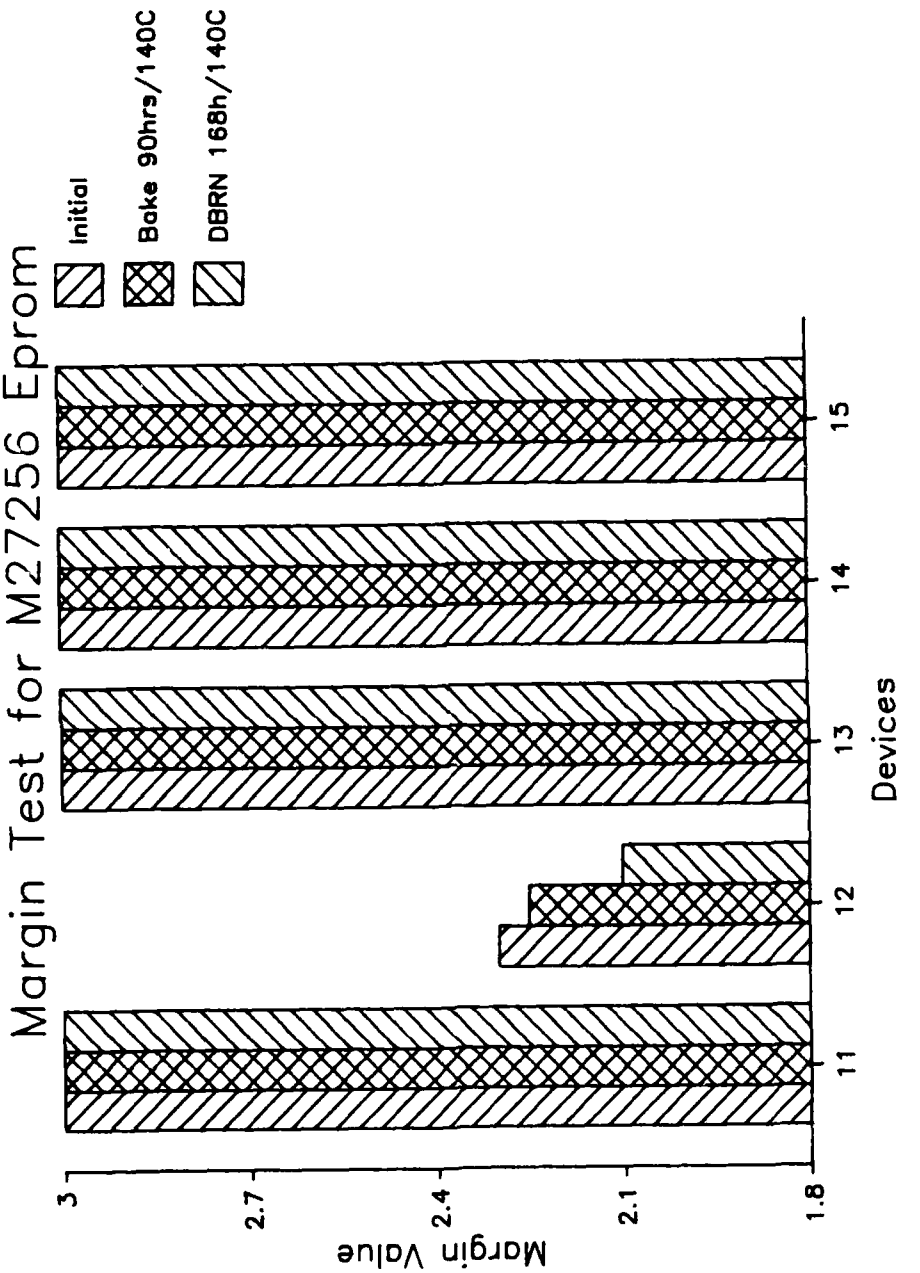

Figure 28: Floating Gate Margin Test Device#'s 11 thru 15

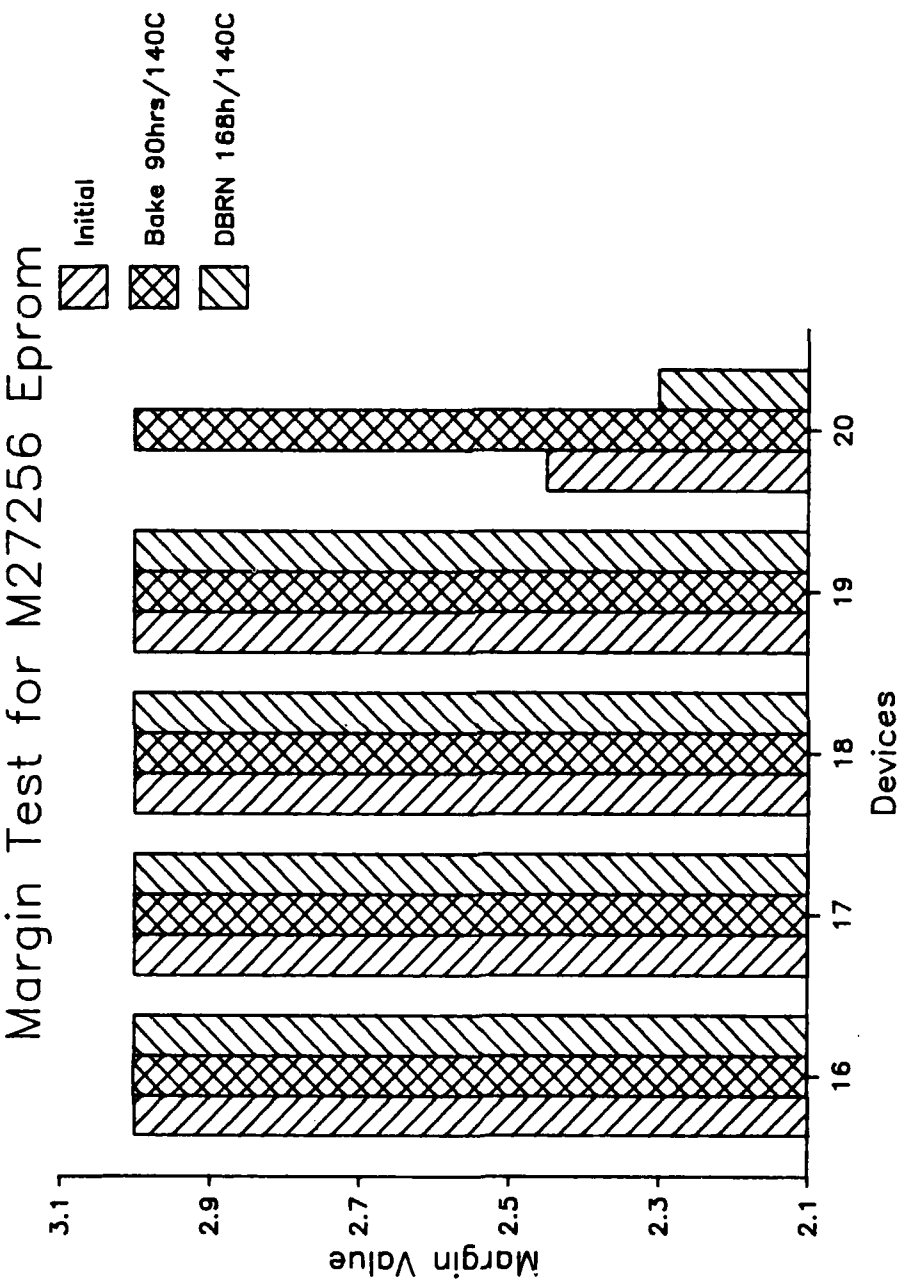

Figure 29: Floating Gate Margin Test Device#'s 16 thru 20

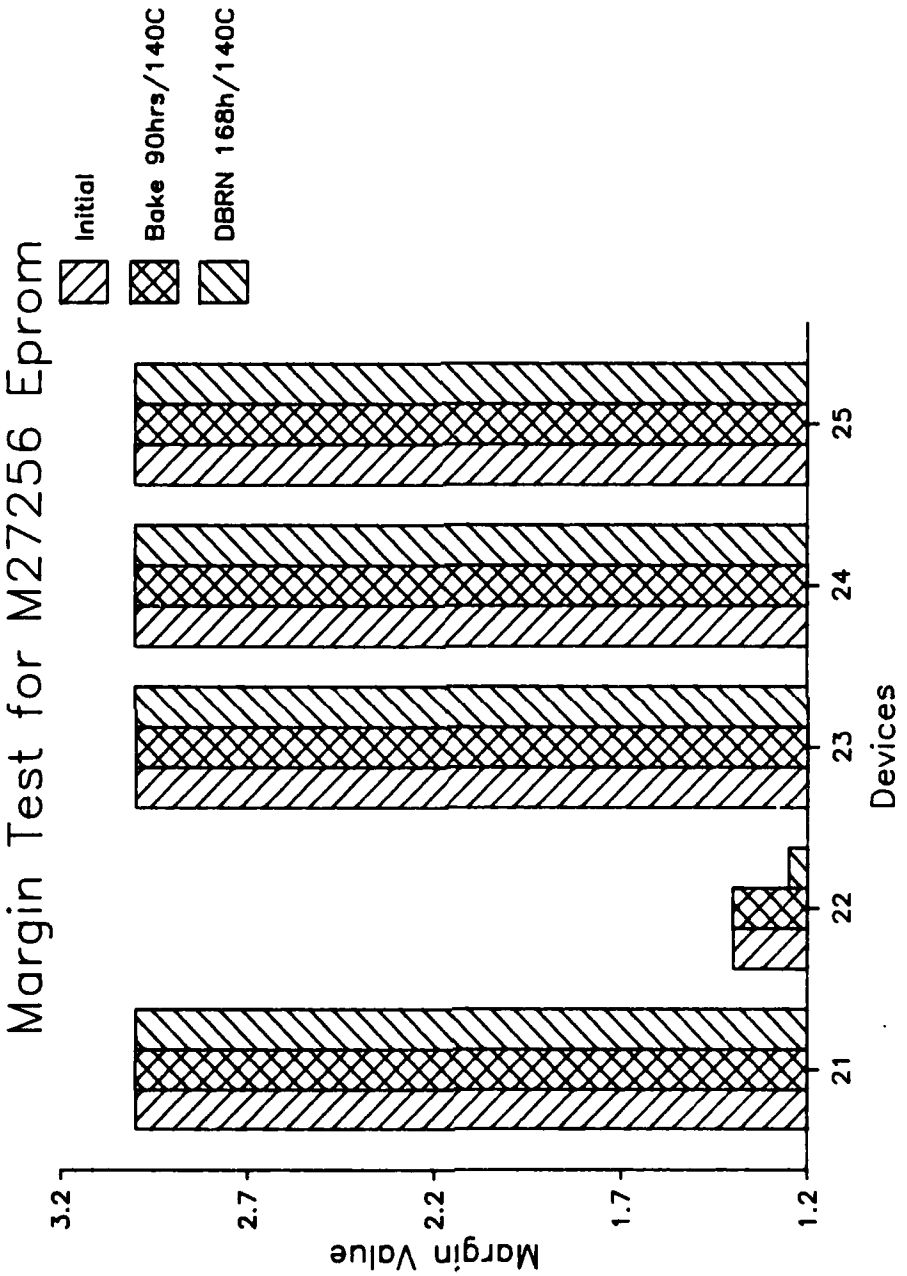

Figure 30: Floating Gate Margin Test Device#'s 21 thru 25

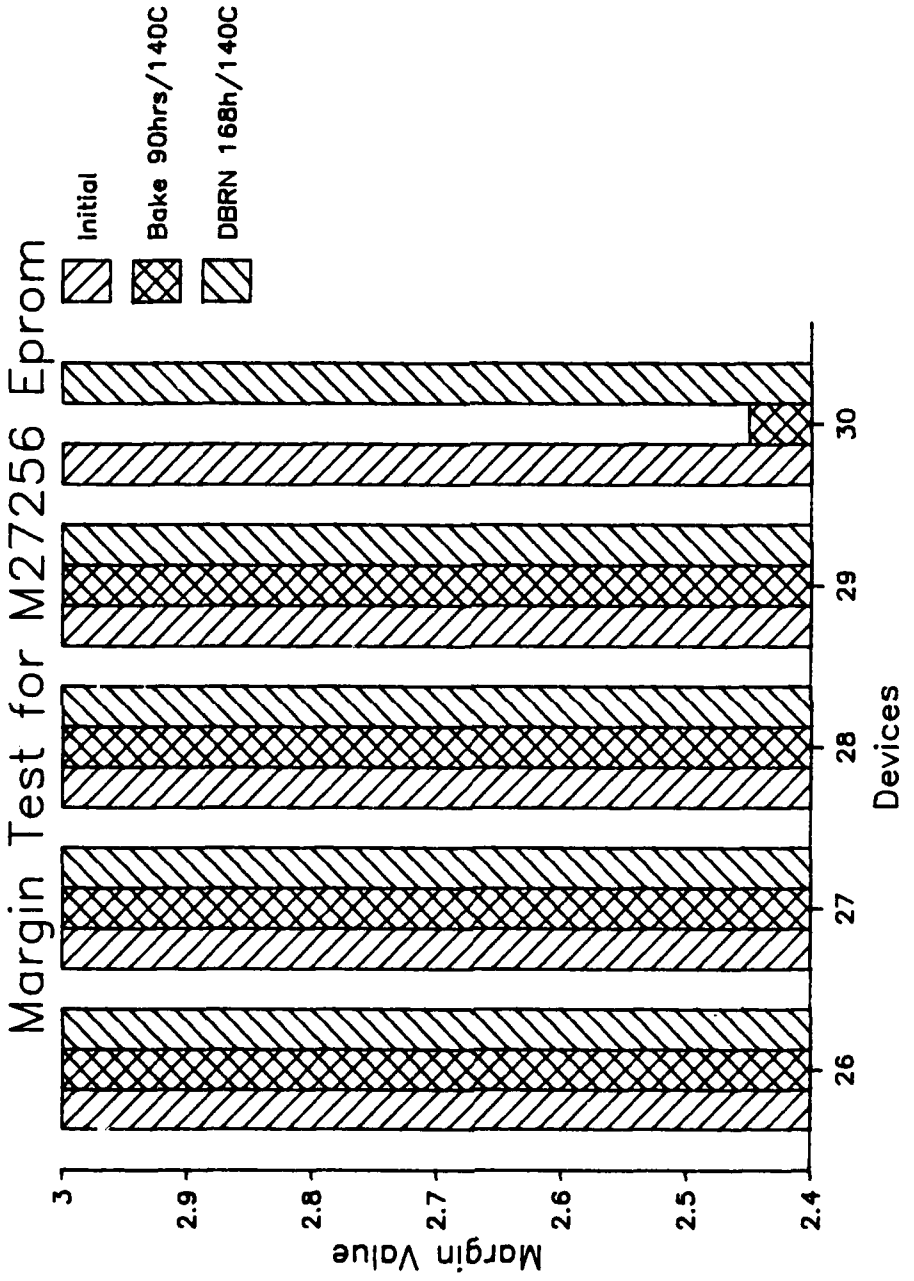

Figure 31: Floating Gate Margin Test Device#'s 26 thru 30

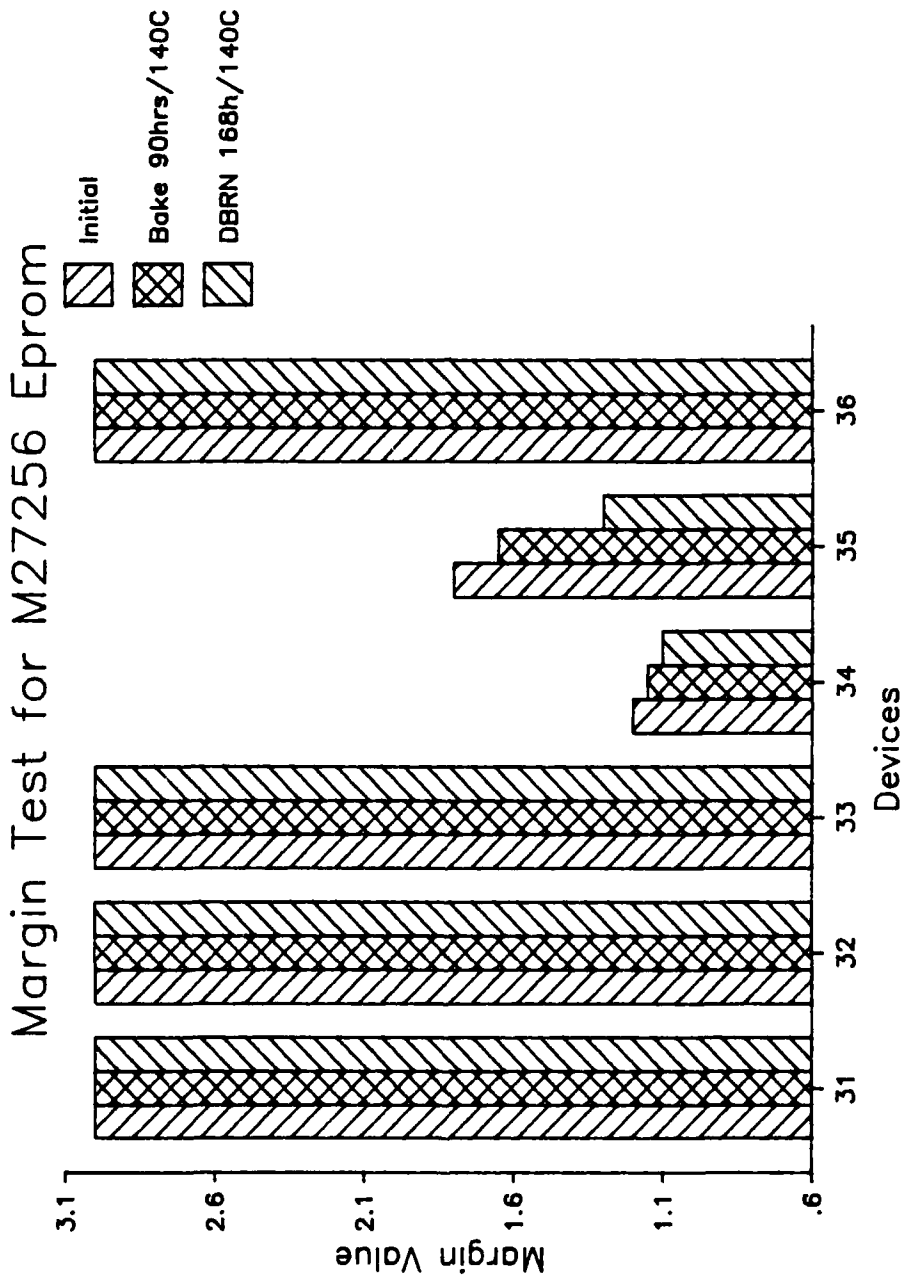

Figure 32: Floating Gate Margin Test Device#'s 31 thru 36

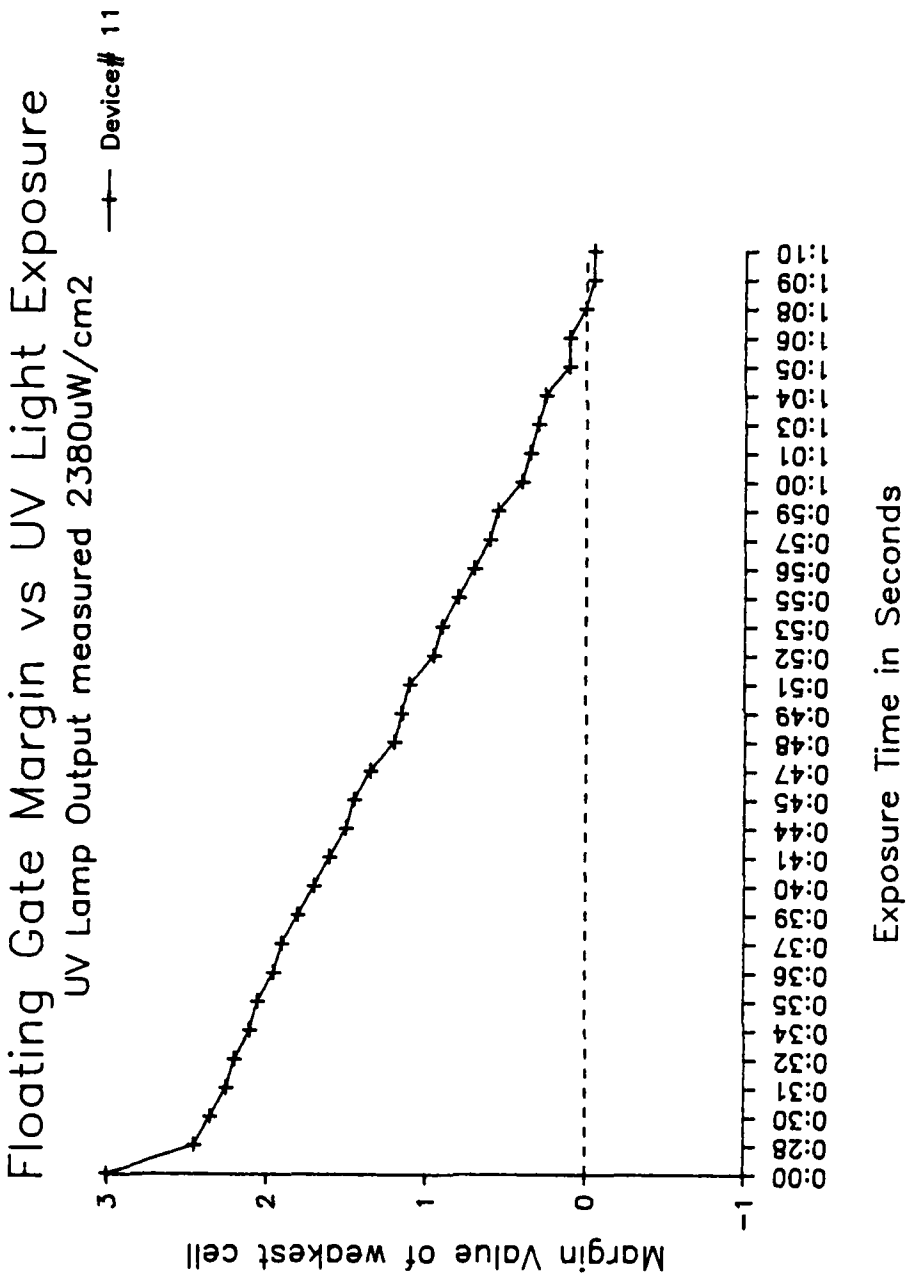

Figure 33: Floating Gate Margin VS UV Light .Device#11

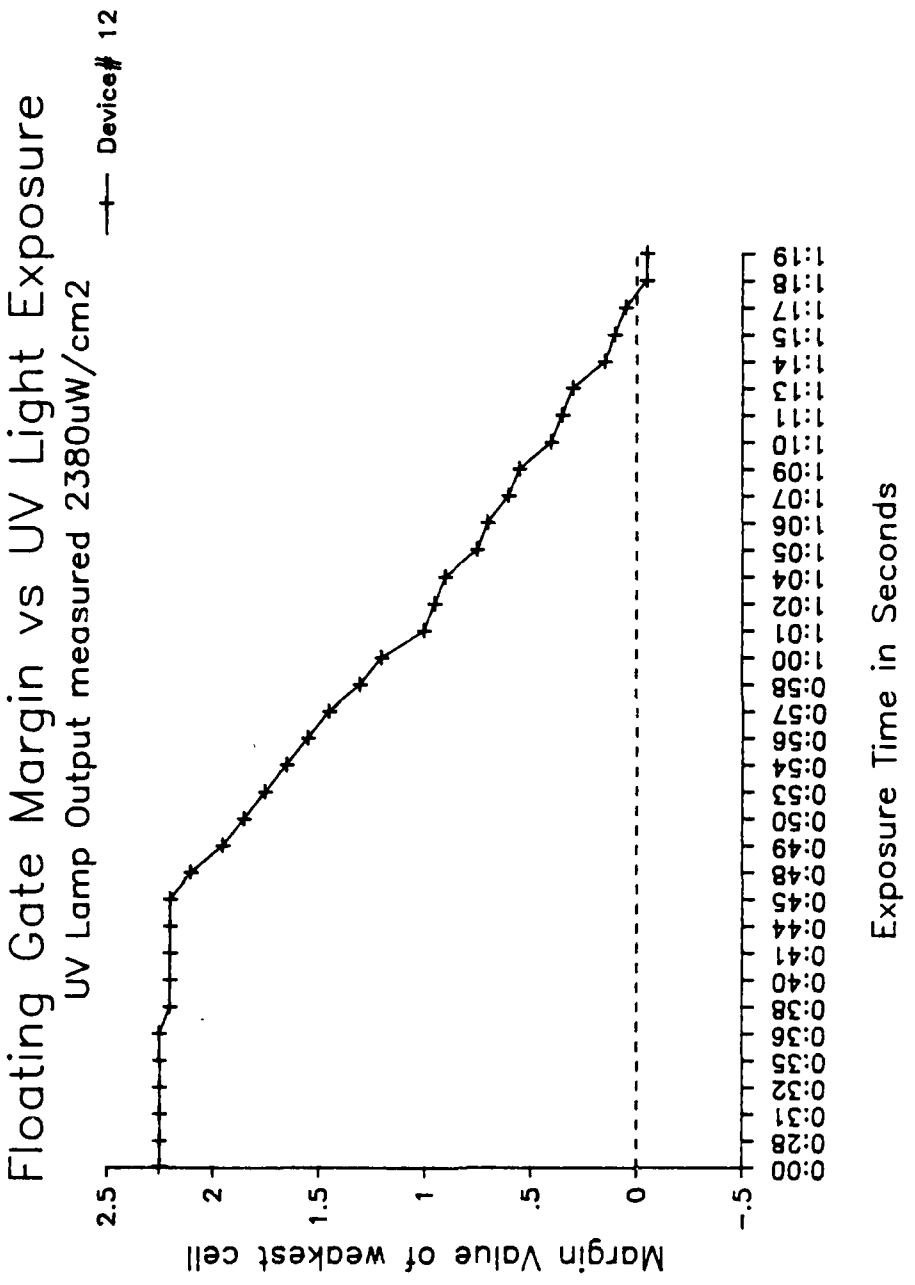

Figure 34: Floating Gate Margin VS UV Light .Device#12

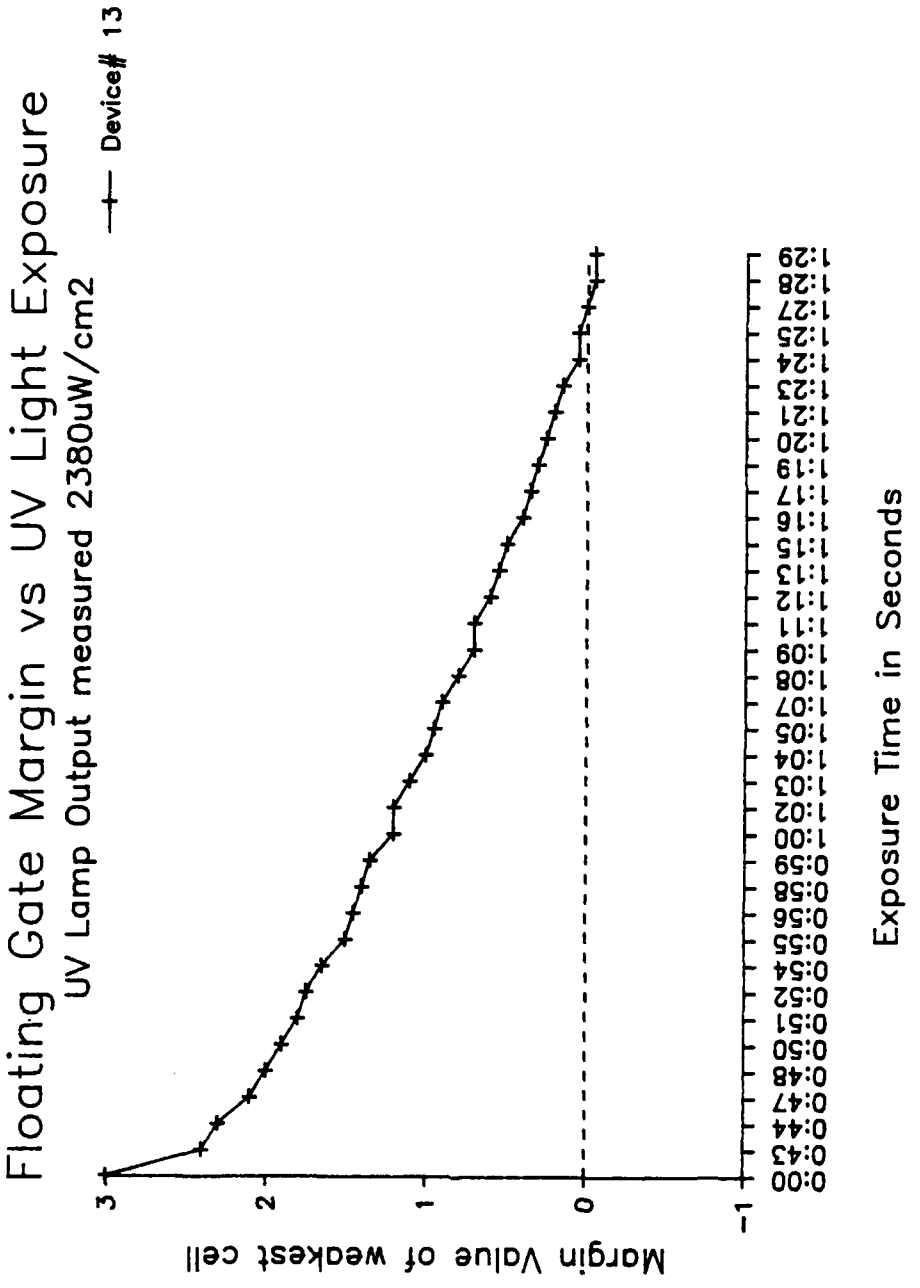

Figure 35: Floating Gate Margin VS UV Light .Device#13

11. CONCLUSIONS

As a result of the device characterization, the following conclusions can be made:

- o The worst case supply current occurs at -55^{O}C.
- o IIH and IIL measurements yielded extremely low current of 400nA or less over the full temperature range.
- o VOL and VOH measurements were within the proposed slash sheet limits.
- o Addresses, -CE and -OE thresholds increase with VCC. Changes in temperature had little effect on the threshold levels.
- o In all cases, the measured input and output capacitance values were below the specified limits.
- o This device can be rated in ESD category "B" (>2000 volts).
- o Worst case conditions for A.C. parameters were high temperature (125^{O}C) and low voltage (4.5 volts).
- o In all cases, the margins on the floating gates of the devices were all above the 0.5 volt limit, as specified for HMOS-IIE in the proposed slash sheet.
- o To increase device integrity, the use of multiple data patterns during A.C. parametric measurements is recommended.
- o As part of a future comprehensive characterization effort, it is recommended that an in-depth study be done on the effects of floating gate margin on data retention.

TABLE OF CONTENTS

512K UVEPROM

LIST OF FIGURES

1. SUMMARY

1.1 OBJECTIVES/RESULTS

The objective of this portion of the contract with Rome Air Development Center was to perform and present the results of a detailed electrical characterization of a 512K (64K X 8) NMOS UVEPROM. In addition, a preliminary MIL-M-38510 slash sheet was developed.

This report documents the results of the electrical characterization on Intel's "MD27512" UVEPROM. Full AC and DC electrical testing was performed over the full military temperature range. A margin test for the floating gate trapped charge on a EPROM cell was developed. This new test has been included in the slash sheet.

In summary, the device performed as expected, per the proposed slash sheet with the exception of propagation delays, which were noticeably shorter.

Details and test data documenting the above findings are presented and summarized in this report and the slash sheet.

2. INTRODUCTION

2.1 OBJECTIVES

The major objective of this effort was to electrically characterize a 512K (64K X 8) UVEPROM and develop a preliminary MIL-M-38510 slash sheet. In general, the effort involved:

- o Memory market survey to determine production status of candidate devices.
- o Selection and procurement of candidate device types for characterization.
- o Development of test procedures compatible with automatic test systems.
- o Determination/verification of limits and test circuits via device characterization.
- o Investigation of margin testing as a viable means of determining the trapped charge on a floating EPROM cell.
- o Development of a preliminary slash sheet based on device analysis and vendor comments.

2.2 BACKGROUND

The original RFP response called for a 32R16 PAL device. However, after contract award, RADC expressed a strong desire to pursue the 512K EPROM which became available from Intel midway through the contract period. It was mutually decided that the PAL device, which was plagued with problems and not available from the vendor, be dropped in favor of this EPROM device.

3. DESCRIPTION OF DEVICE TYPE

3.1 GENERAL ASPECTS OF 512K EPROMS

The 512K EPROM is a 5 volt only, 524,288-bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM), which is organized as 64K words by 8 bits. The by 8, or bytewide configuration is intended primarily for use with byte oriented microprocessor systems. The two-line (Chip Enable & Output Enable) control and JEDEC-approved, 28-pin package assures easy microprocessor interfacing and minimum design effort when upgrading, adding or choosing between nonvolatile memory alternatives. The 27512's large storage capability of 64K X 8 enables it to function as a high density software carrier.

3.2 ASPECTS OF SPECIFIC DEVICE TYPE

The Intel MD27512 EPROM has several advanced features that allow programming equipment to identify the MD27512 and then rapidly program it using an efficient programming method. The MD27512 is manufactured using HMOS II-E [1] process

3.3 SYSTEM APPLICATION CONSIDERATIONS

The power switching characteristics of HMOS II-E [1] EPROMs require careful decoupling of the devices. The supply current, ICC, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. It is recommended that a 0.1uF ceramic capacitor be used on every device between VCC and GND. In addition, a 4.7uF bulk electrolytic capacitor should be used between VCC and GND for every eight devices. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board traces.

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[1] HMOS II-E is a patented process of Intel Corporation

4. DEVELOPMENT OF AUTOMATIC AND BENCH TESTS

4.1 AUTOMATIC TEST EQUIPMENT

The test equipment used to characterize the 512K EPROM is a Fairchild Xincom 5588 Automatic Test System. The system's main processor is a Zilog Z8000 microprocessor. This processor handles all test sequences and test processes. Included in the system is a subsystem which is called the Test Pattern Computer (TPC).

The TPC is a modular subassembly which has the capability to microprogram an assortment of test patterns including such popular industry standards as: Ping Pong, Checkerboard, and March. Patterns are defined by a set of 48-bit microcoded instructions executed within the TPC at functional rates up to 25MHz (40ns cycle time). Upon command from the main processor, the TPC generates the desired pattern and sends this pattern to the system for use in the stimulus of input pins and response checking of output pins.

Some additional features of the TPC are:

- o ECL Construction
- o Topological Address Scrambler
- o Address Indexing, Refresh Testing, Butterfly Patterns
- o Truth-Table RAM (Pattern RAM For EPROMS)
- o Algorithmic Pattern Generation
- o Loop Counters
- o Timing Set Selection on the fly

In addition to the TPC other system capabilities include:

- o 14 programmable clock phases
- o 4 programmable power supplies
- o 24 address lines
- o 16 data comparators
- o Parametric Measurement Unit (PMU)
- o Advanced Error Logging System (AELS)
- o IEEE 488 Bus Interface
- o Color Computer Graphics Display
- o Auto Data Logging to Data General Eclipse Host Computer

To interface the device under test (DUT) to the test system, an interface board is used to electrically connect the DUT's pins to the specific test system pin electronic cards. A zero insertion force socket is used to allow for fast removal and insertions of the DUT without causing lead damage.

4.2 BENCH TEST EQUIPMENT

Two instruments were required to perform the Electrostatic Discharge and Capacitance Measurement tests.

The Electrostatic Discharge unit used is a IMCS Corporation, Model number 2400C.

Features include:

- o 0-10,000 Volt Continuously Adjustable
- o 4.5 Digital Display of HV
- o Programmable Pulse Sequence
- o Curve Tracer Output

- o 1-128 pin Configuration
- o Applicable to MIL-STD-883 and STD-1686

The Capacitance Analyzer used is a Hewlett Packard, Model number 4192A, probe model number HP-16048C.

Features include:

- o 5 Hz to 13MHz variable measuring frequency
- o Gain-Phase measurement: amplitude, phase and delay
- o Floating or Grounded devices
- o Frequency accuracy +/- 50ppm

4.3 EPROM PROGRAMMING EQUIPMENT

A Data I/O, model 29A was used to program the test patterns into the EPROM device. The 29A is a microprocessor-based system which is designed around a 6802 microprocessor. The programmer allows the user to create and program unique data patterns. A master device which contains a predetermined pattern can also be copied and programmed. The system has many editing features which enable the user to modify patterns quickly.

A programming pack was required for the 512K EPROM device. This pack is a plug-in module which has the ability to program up to 200 different EPROM and PROM types. This programming pack can be identified as "Uni-Pak," model number 950-0099-10, Software revision V10.

Some features of the system are:

- o 64K X 8 (512K bits) RAM for pattern storage
- o Hexadecimal keyboard with alphanumeric display
- o Automatic check-sum calculation
- o Automatic error routine monitors device integrity
- o 16 switch selectable baud rates for remote terminal and data transfer

5. STATIC CHARACTERISTICS

5.1 OBJECTIVES

During this characterization, several goals were set forth. One of these was to reliably and efficiently characterize the D.C. parameters of the 512K EPROM device. This was accomplished by utilizing Automatic Test Equipment (ATE). This equipment could reliably execute a group of measurements and test conditions with accuracy and repeatability.

5.2 TEST METHODS

The Xincom 5588 memory test system was used to collect data on the D.C. parametric measurements. The tester allowed data to be taken on each device in an accelerated and accurate manner. The sample size for the D.C. measurements was 36 devices. By using a typically larger sample size, we were able to average measurement values to get a basic feel for the "trend" or average values for a specific parameter. The tests performed on the Xincom were: VOH, VOL, IIH, IIL, IOZH, IOZL, ICC and ISB parameter. Test temperatures used were $-55^{o}C$, $+25^{o}C$ and $+125^{o}C$. Note that every test was performed at each temperature and worst case voltage.

5.2.1 VOH, VOL TEST

This test is performed to measure the resultant voltage level on the output when driving a load. For this, test currents are forced into the output and the resulting voltage is measured. The forcing current used for the VOH test is -400uA with VCC equaling 4.5V. The current used for the VOL measurement is 2.1mA with VCC equal to 5.5V. Note that VCC is raised to 5.5 volts when measuring the low output voltage level and is reduced to 4.5 volts when measuring the high output level. By margining VCC in this manner, the worst case conditions are tested.

The average values versus temperature are plotted in Figures 1 and 2. Note that in both tests the maximum VOL (max VOL=0.45V) and the minimum VOH (min VOH=2.4V) as specified in the proposed slash sheet were never exceeded.

5.2.2 IIH, IIL TEST

The IIH and IIL tests are done to determine the amount of current drawn when the inputs have a specified voltage applied to them. This test is conducted by driving an input high and low and measuring the resultant current. Test levels for this parameter were Vin=0V (for IIL) and Vin=5.5V (for IIH), where VCC equals 5.5V. The worst case condition for leakage is when Vin equals 5.5 volts.

Leakage measurements were performed at $-55^{o}C$, $+25^{o}C$ and $+125^{o}C$. The specified limits were +/- 10uA. In general, all measurements yielded extremely low currents of 100nA or less. Currents of these magnitudes are typical in LSI devices using NMOS technology.

5.2.3 IOZH, IOZL TEST

This test measures the output leakage current of the device when its outputs are in the high impedance state. The procedure for this test is to set the device's outputs in the high impedance state by applying a logic "1" to either -CE or -OE/VPP input pins. Then force a voltage on the output under test and measure the resultant current.

Two forcing voltages are applied. In the IOZH test, 5.5 volts are applied and in the IOZL test, 0 volts are applied. During this test VCC is set to 5.5 volts which is the worst case condition.

As in the IIH and IIL test (section 5.2.2), the specified limits were +/- 10uA. In general, all measurements yielded extremely low currents of 400nA or less over the full temperature range.

5.2.4 ICC, ISB TEST

This test measures the amount of supply current required by the device for two different operating modes. The first mode is device active (ICC). This mode is the typical operating mode when the device is being accessed. The second mode is standby (ISB). During standby, the device's maximum active current is reduced by almost 33%.

The device is piaced in the standby mode by applying a logic "1" to the -CE input. When in the standby mode, the outputs are in the high impedance state, independent of -OE/VPP input.

To perform the active test, all address inputs and control signals (-OE/VPP,-CE) are placed at logic "0." The VCC of the device is at maximum (5.5V). The resulting current is then measured and recorded. The Standby test places a logic "1" on the -CE pin and keeps all other inputs low. The resulting current is measured and recorded.

Refer to Figure 3 (Average Supply Current) and Figure 4 (Average Standby Current) for measured values.

In general, -55°C caused worst case supply current for the active state, while +125°C showed an increase in the standby current. The percentage of the change in the standby current was small compared to the overall range. In both cases, the measured values were within their maximum limits as specified in the proposed slash sheet.

5.3 TEST SUMMARY

During the -55°C testing, a problem occurred with moisture condensing on, in and under the device socket and thermal insulating pad. This moisture caused false leakage measurements. The devices which failed due to this moisture buildup were retested. The false leakage measurements were not considered valid, hence, they were not included in the overall leakage averages.

In general, the measured DC parameters were within the maximum and minimum limits set by the proposed slash sheet.

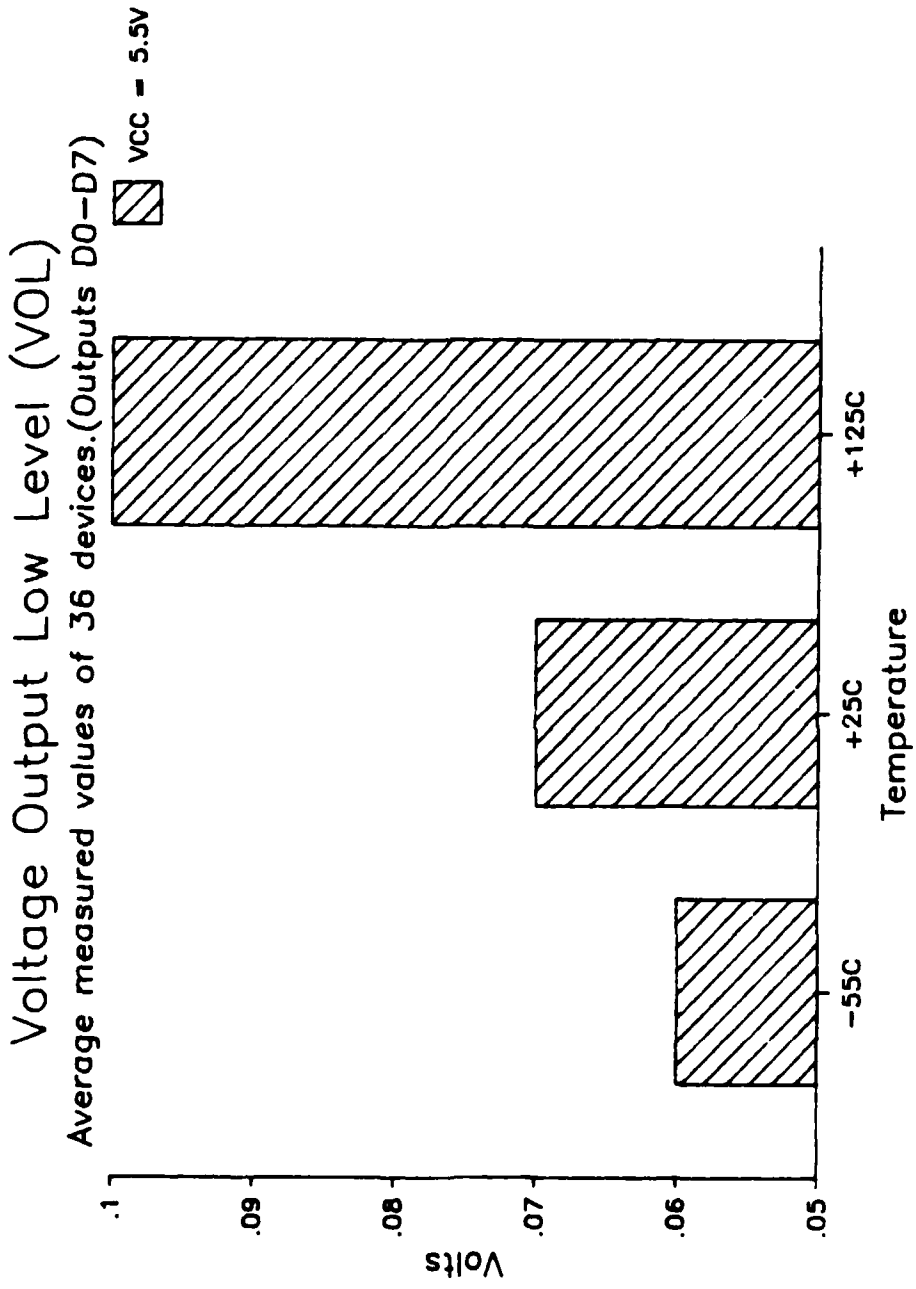


Figure 1: Voltage Output Low Level (VOL)

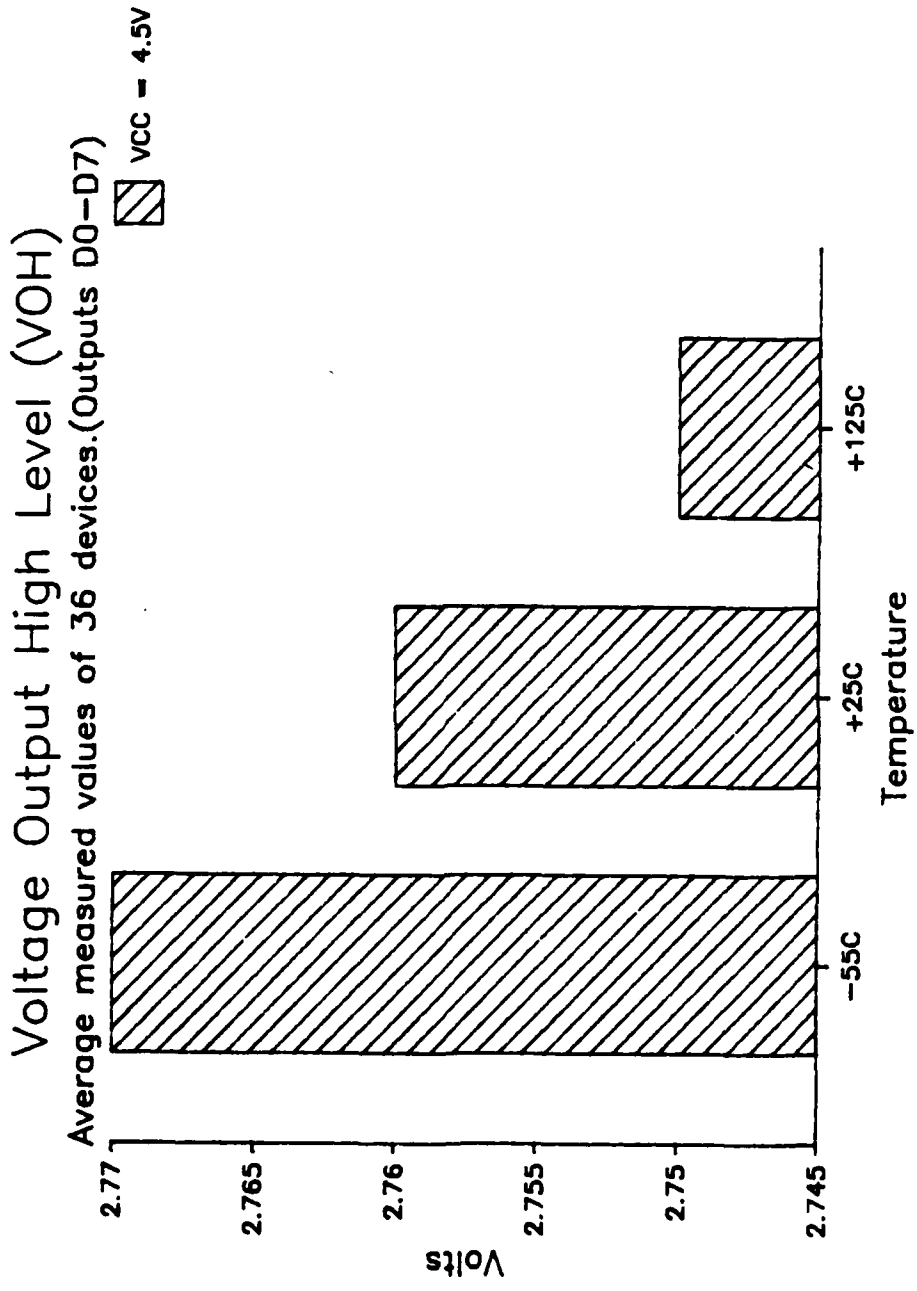


Figure 2: Voltage Output High Level (VOH)

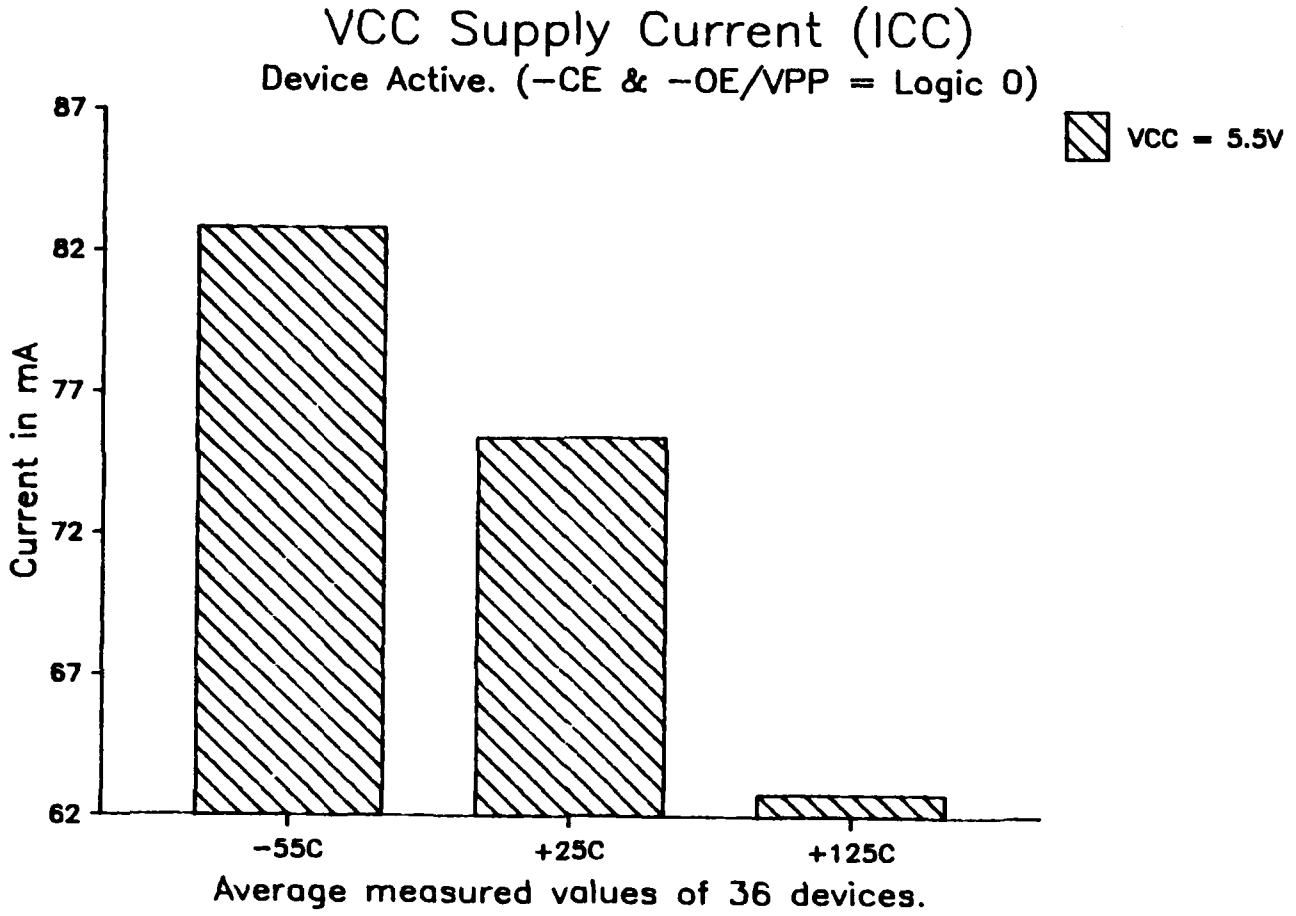


Figure 3: VCC Supply Current (ICC)

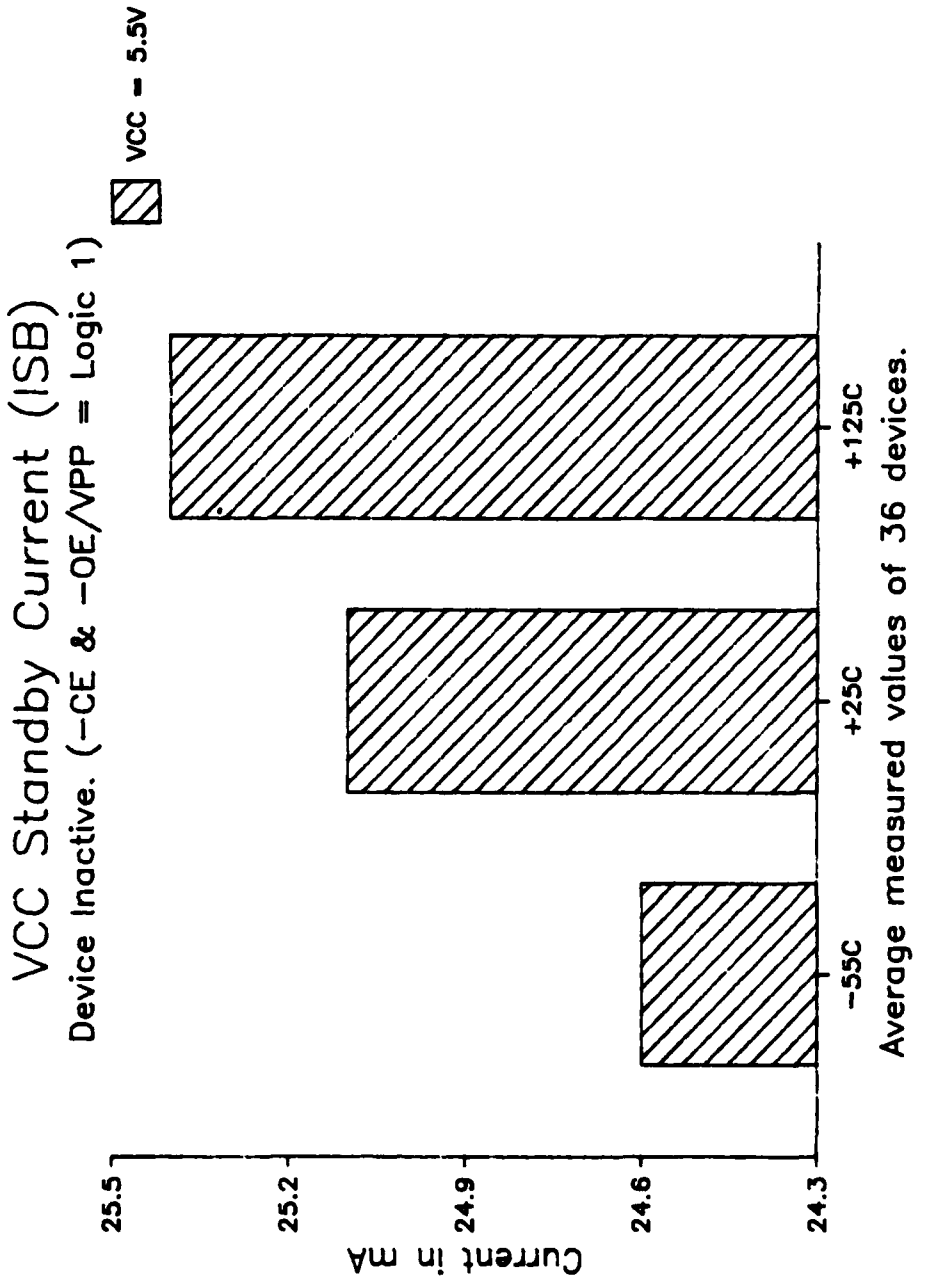


Figure 4: VCC Standby Current (ISB)

6. DEVICE THRESHOLD TESTS

6.1 TEST METHODS

The device threshold test is performed to measure the minimum and maximum margins on the VIL (Voltage Input Low) and VIH (Voltage Input High) levels. These measurements are taken over temperature and min (4.5V) and max (5.5V) VCC levels.

The test consists of programming the device with a pattern and functionally verifying the pattern while varying the input voltage levels. The margin values are measured when the device's outputs no longer match the test pattern.

During this test, the timing parameters are set to a nominal value. Because the timing parameters are set to nominal, the failure can be attributed to the input level.

6.1.1 Address Input Margin Low and High

The address input margin test measured the VIL and VIH level on all address pins (A0-A15). Since all addresses were margined at the same time, the margin value represents the worst address threshold value.

Results of the testing are shown in Figures 5 and 6 which show the effect that VCC and temperature have on the device threshold value. As expected, and indicated by the data, threshold increases with VCC.

6.1.2 Chip Enable, Output Enable Margin Low and High

The Chip and Output Enable test measures the VIL and VIH level on the -CE (Chip Enable) and -OE/VPP (Output Enable) pins. Only the -CE and -OE/VPP pins are margined, all other input voltage levels are kept at nominal.

Results of these tests are shown in Figures 7 and 8. As in the address threshold test, the threshold values increase with VCC.

6.2 TEST SUMMARY

In both tests, address, -CE and -OE/VPP measured values were within their proposed limits. The maximum VIL level as specified was 0.8 volts. The measured value showed a worst case VIL of 1.58V. This gives a VIL margin of 0.78 volts. The minimum VIH level as specified was 2.0 volts. The measured value showed 1.92 volts. Although close to the 2.0 volt minimum, the measured VIH value was within the proposed limit.

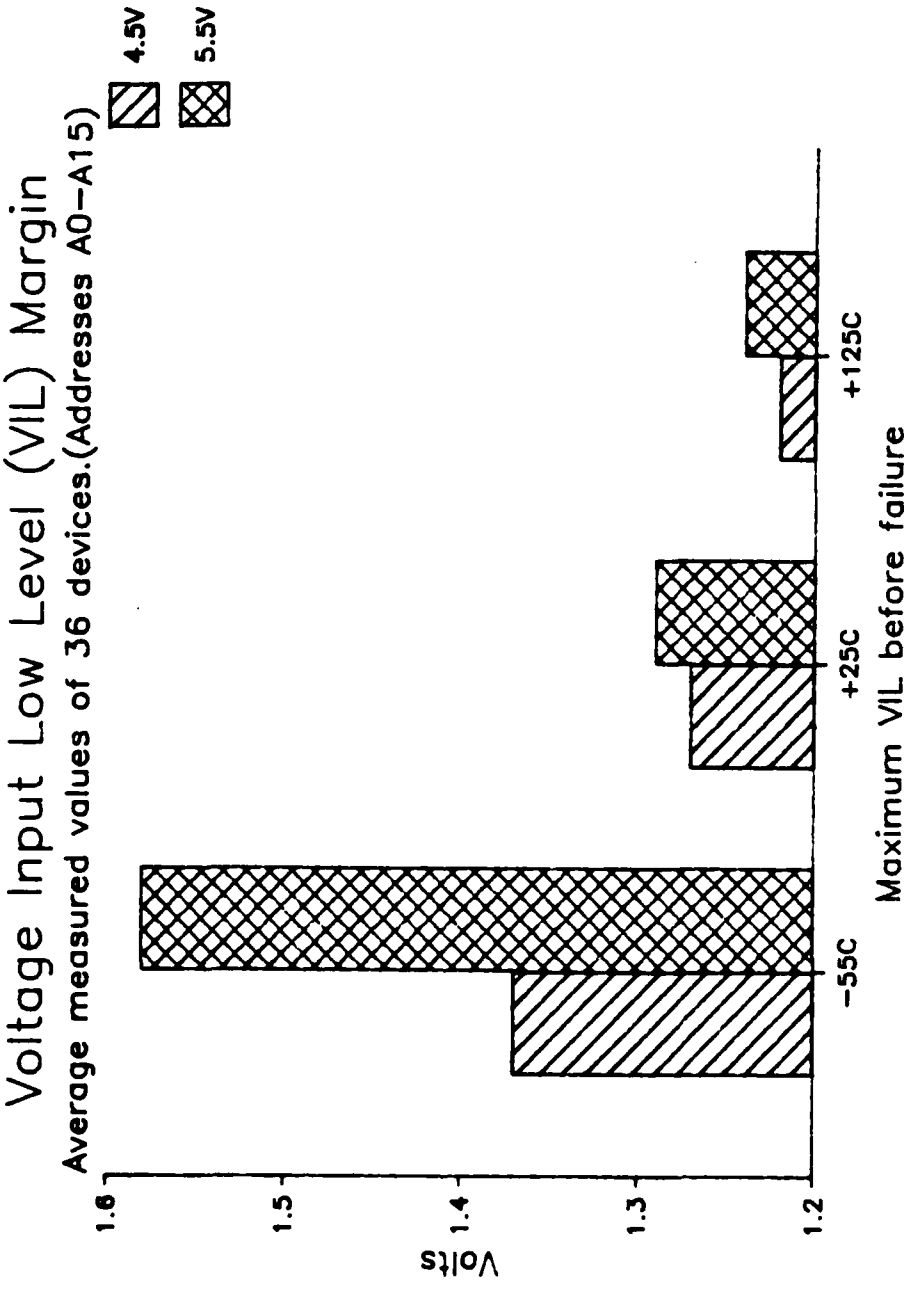


Figure 5: Voltage Input Low Level Margin (VIL) Addresses

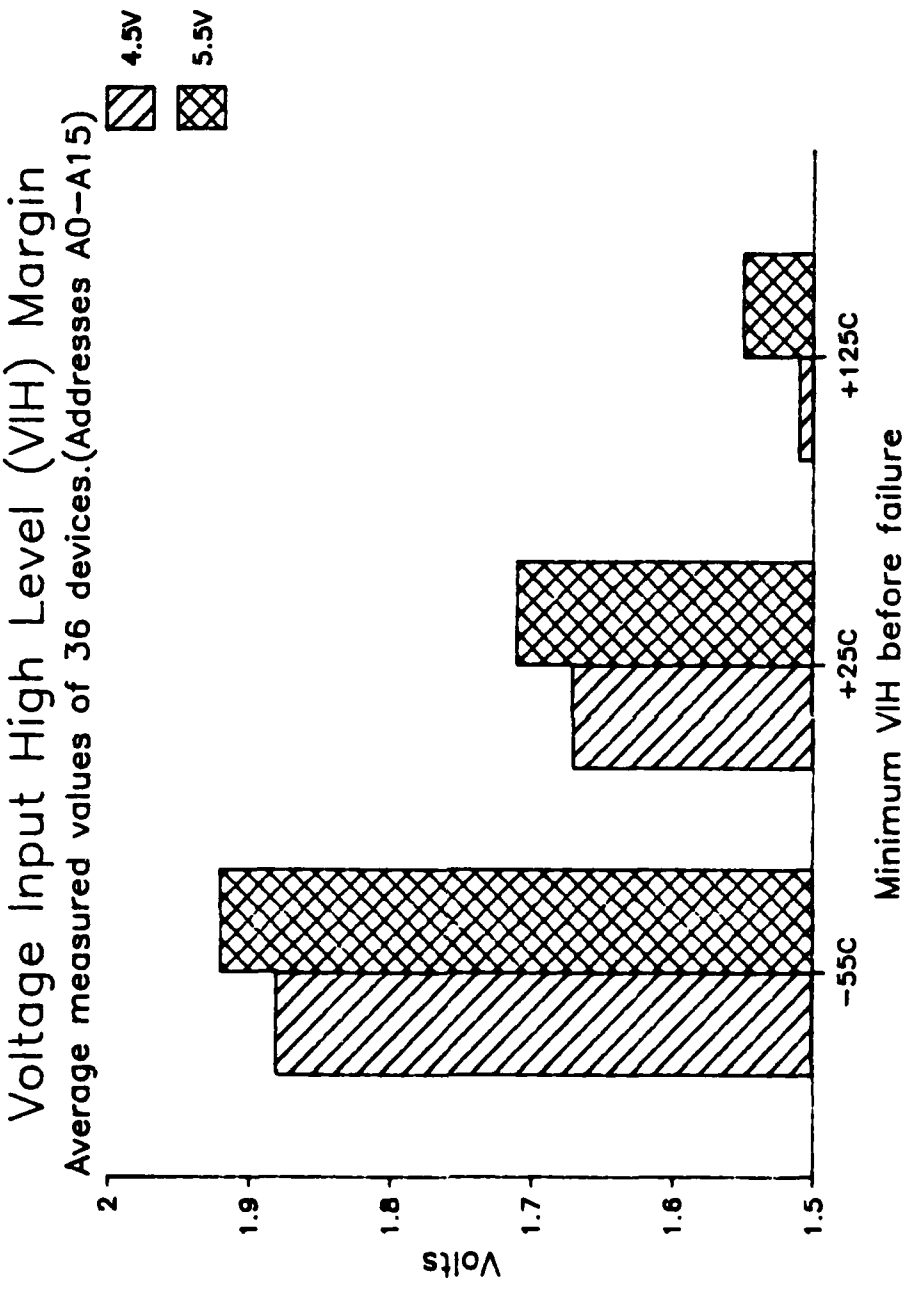


Figure 6: Voltage Input High Level Margin (VIH) Addresses

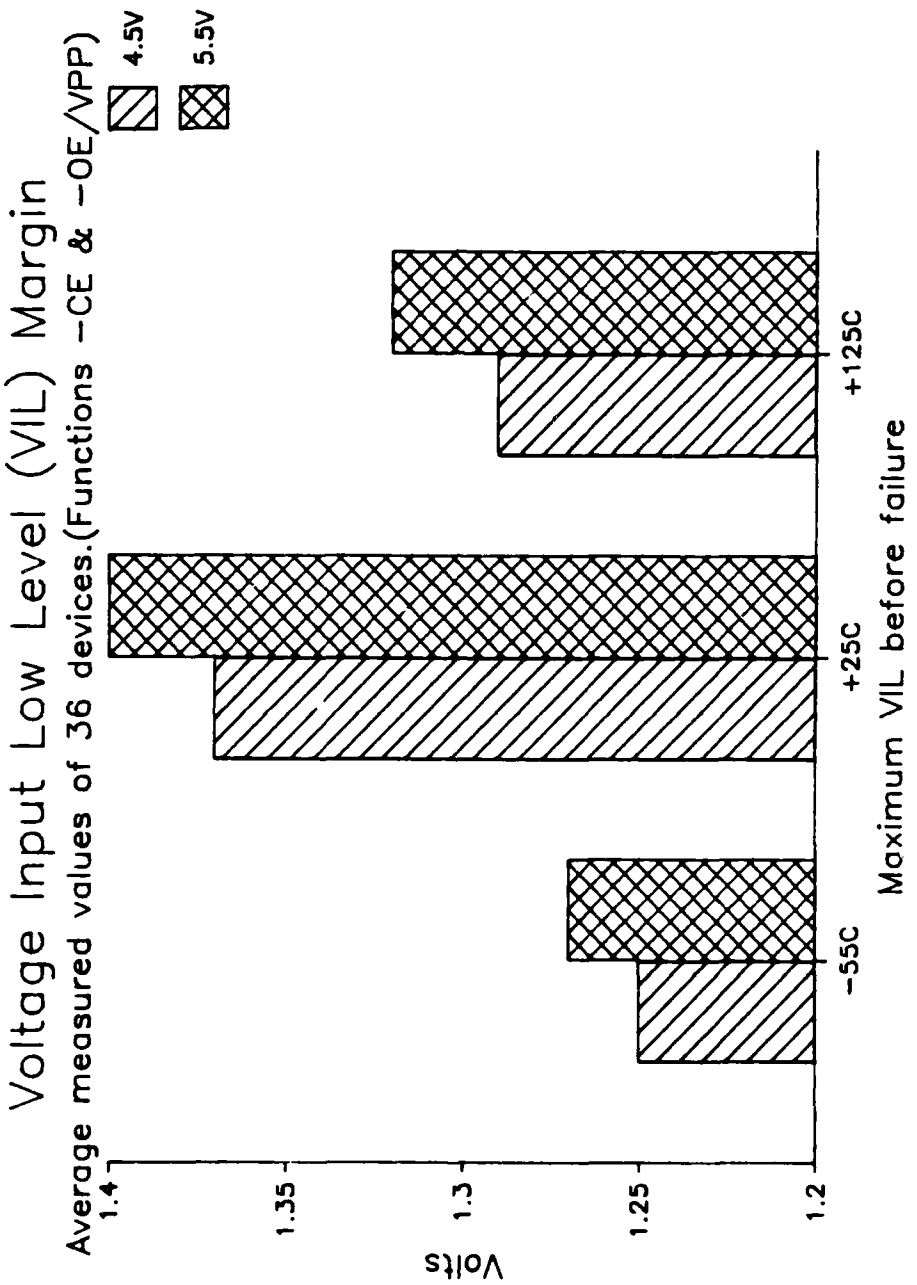


Figure 7: Voltage Input Low Level Margin (VIL) -CE & -OE/VPP

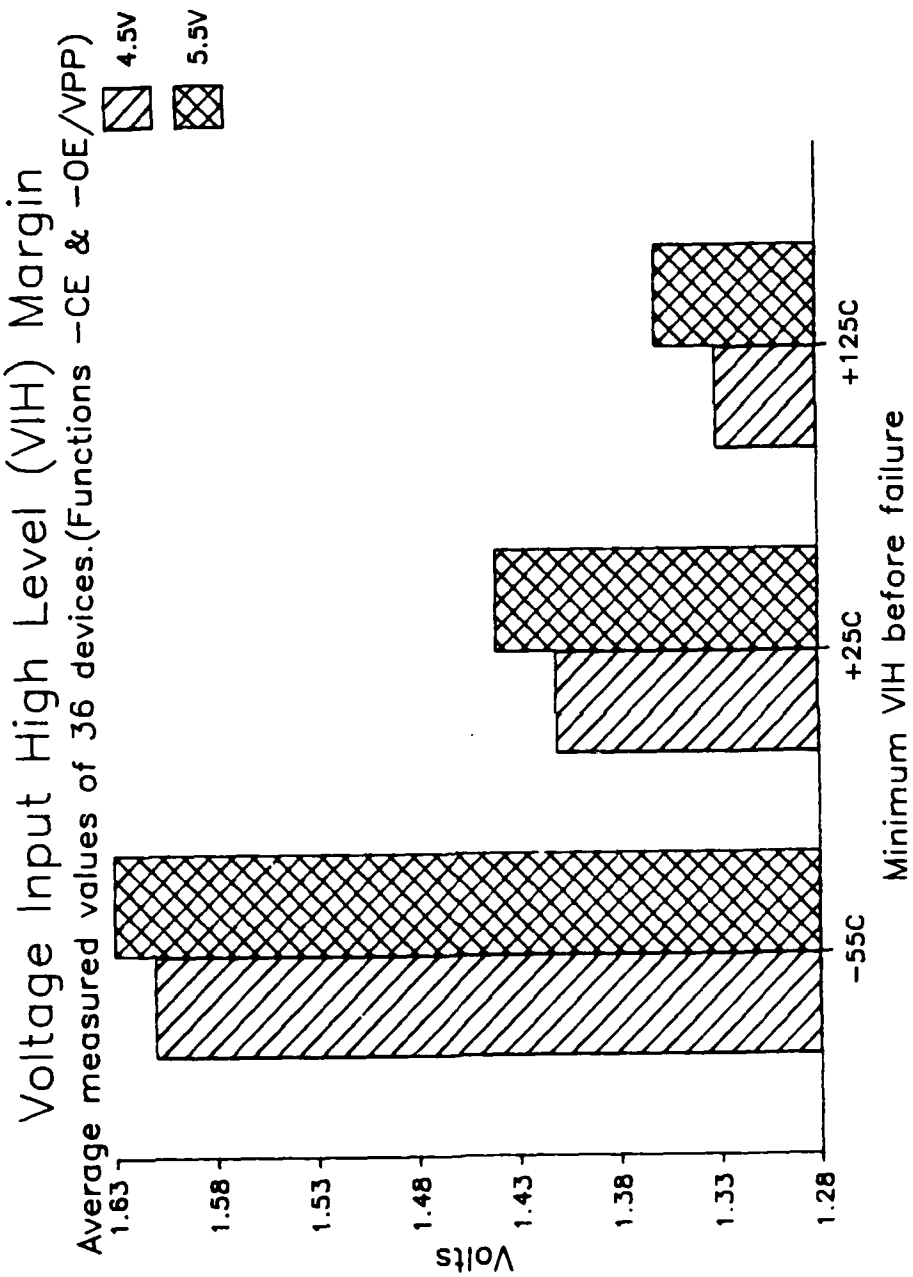


Figure 8: Voltage Input High Level Margin (VIH) -CE & -OE/VPP

7. INPUT/OUTPUT CAPACITANCE MEASUREMENTS

7.1 TEST METHODS

Capacitance measurements were performed on six devices. Both input and output pin capacitance measurements were made.

The procedure used was to place the capacitance meter on the input/output pin and measure its capacitance with respect to the device's ground pin. During testing, all pins not under test are left open.

The meter parameters were set as follows:

Frequency = 1MHz
AC RMS amplitude = 50 millivolts
DC bias= 0 volts
Parallel equivalent circuit

Refer to MIL-STD-883C method 3012.1.

7.2 TEST SUMMARY

As a result of the measurements, the data showed that the devices did not have a uniform capacitance with respect to adjacent pins. Referring to Figures 9 and 10, these graphs show input pins 20, 22 and 27 have consistently higher capacitance values then their adjacent inputs. As specified in the proposed slash sheet, the maximum input capacitance for all pins except 22 is 6pF. The maximum input capacitance for pin 22 is 20pf. In all cases the measured values were below this value.

As compared to the inputs, the measured output capacitance was higher. Refer to Figure 11 and 12 . Again, the test results showed the devices did not have a uniform capacitance. Output pin 15 had the highest measured value but, it was within the maximum specification of 10pF.

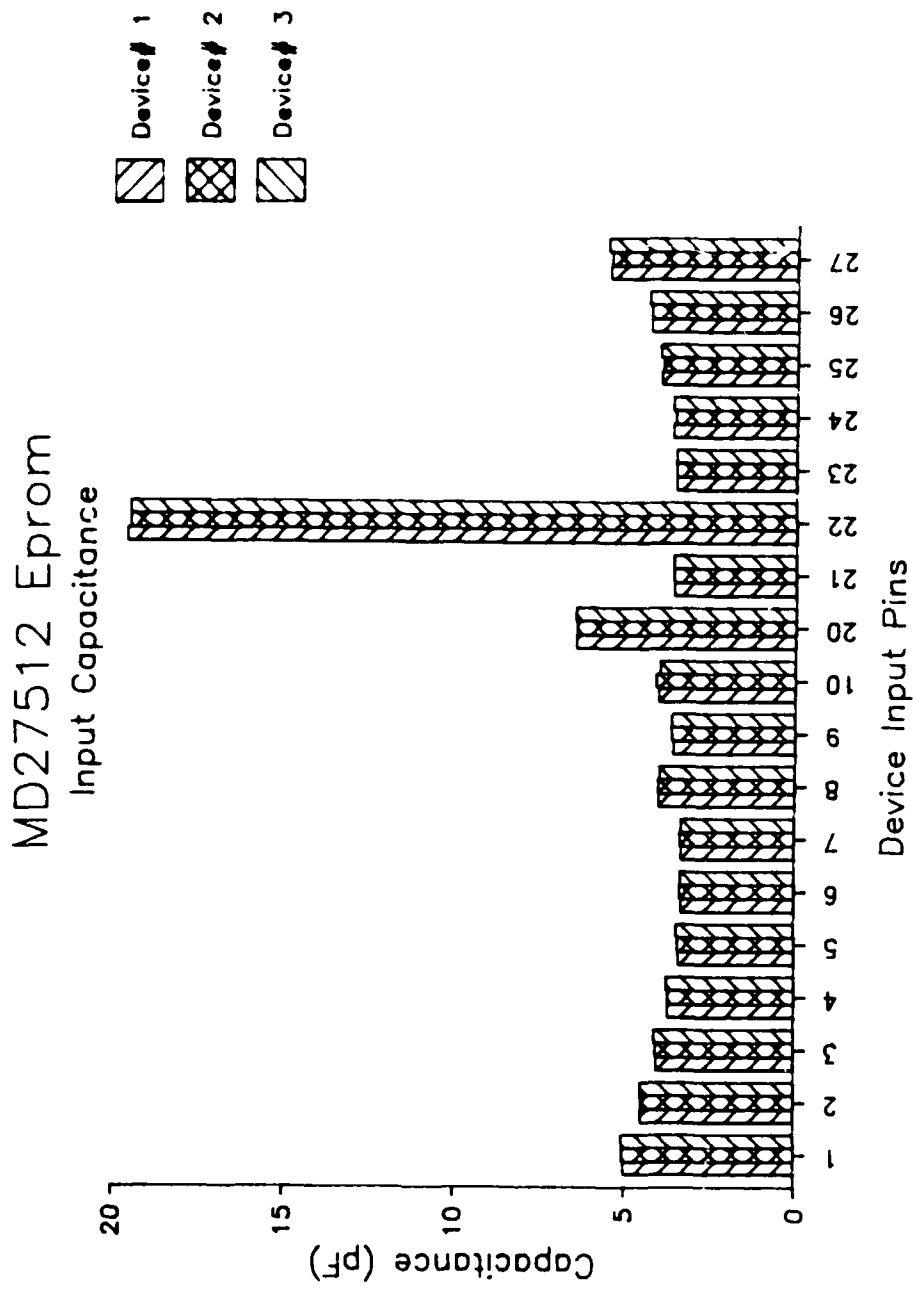
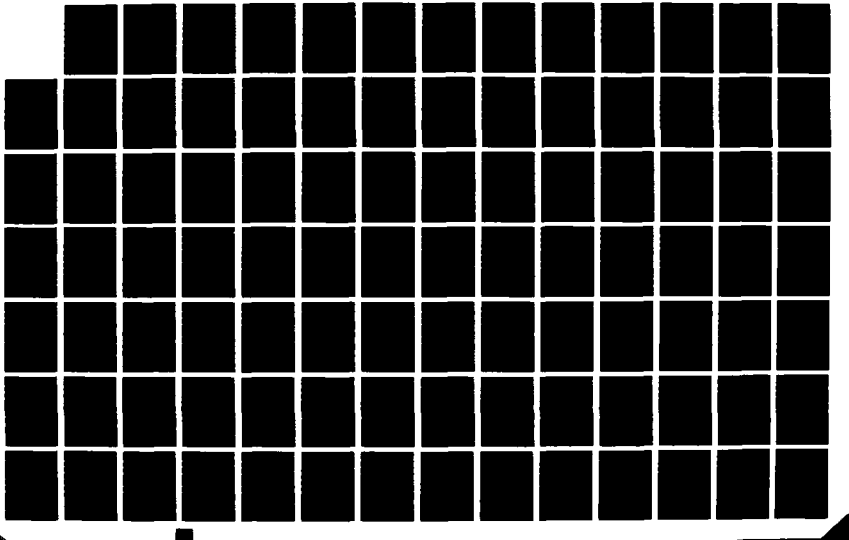
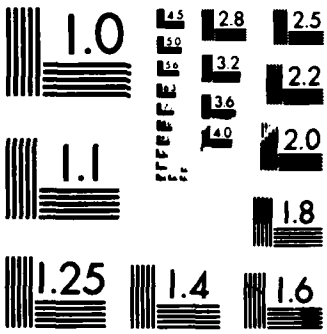


Figure 9: Input Capacitance Measurement Devices 1 2 3

AD-A180 114 ELECTRICAL CHARACTERIZATION OF VLSI RAMS AND PROMS(U) 2/3
GTE COMMUNICATIONS SYSTEMS CORP PHOENIX AZ
M FORMOSO ET AL. OCT 86 RADC-TR-86-180 F30602-84-C-0070
UNCLASSIFIED F/G 12/6 NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

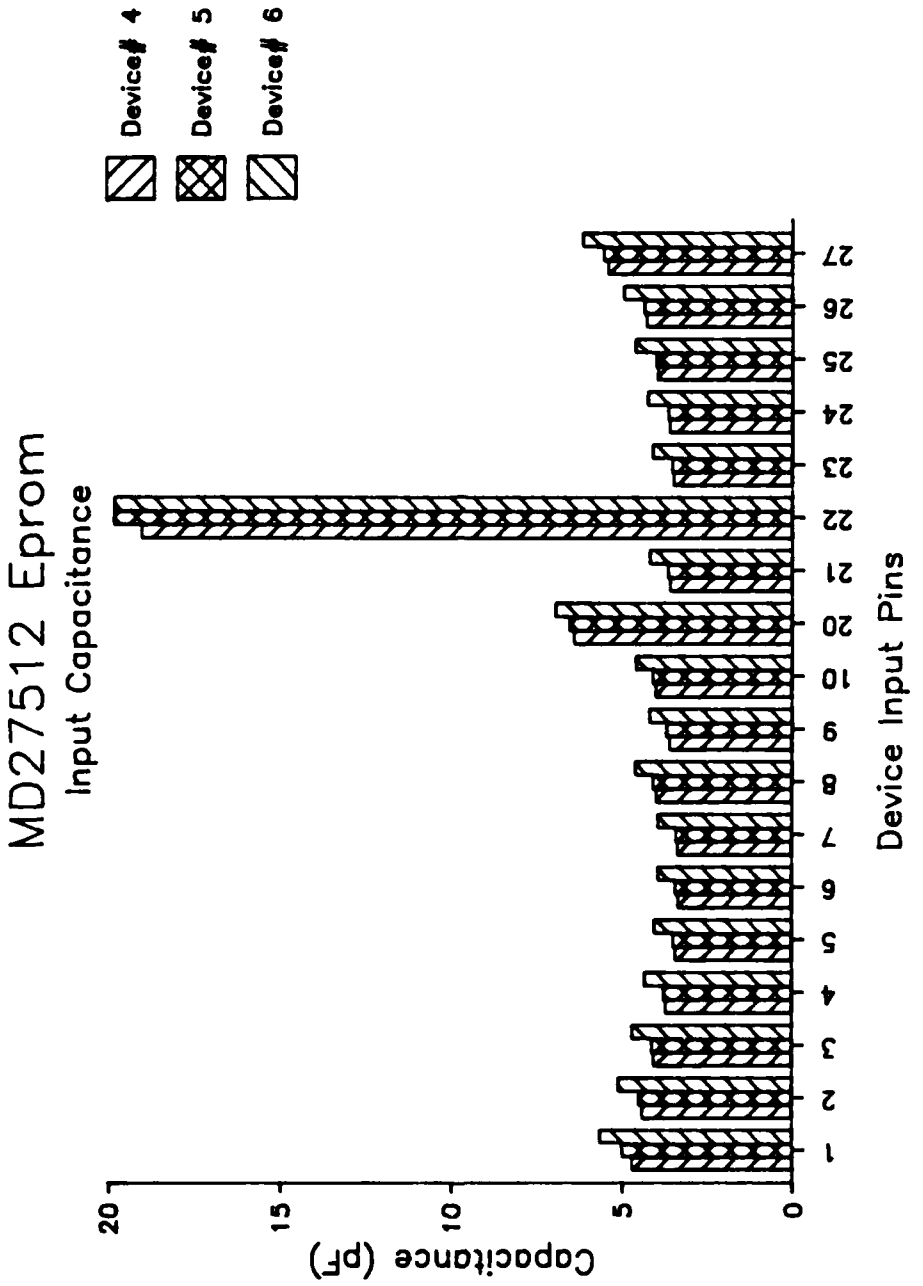


Figure 10: Input Capacitance Measurement Devices 4,5,6

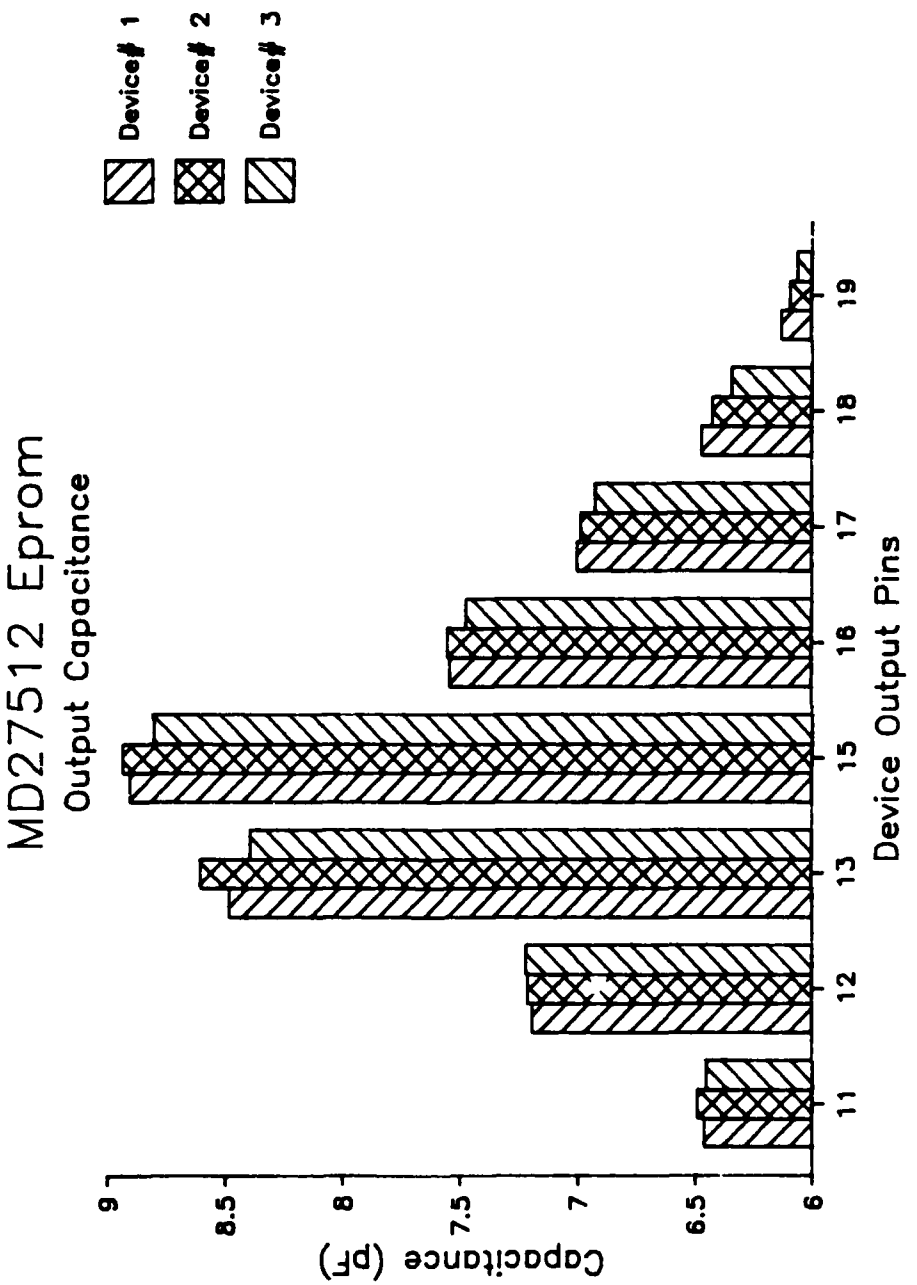


Figure 11: Output Capacitance Measurement Devices 1,2,3

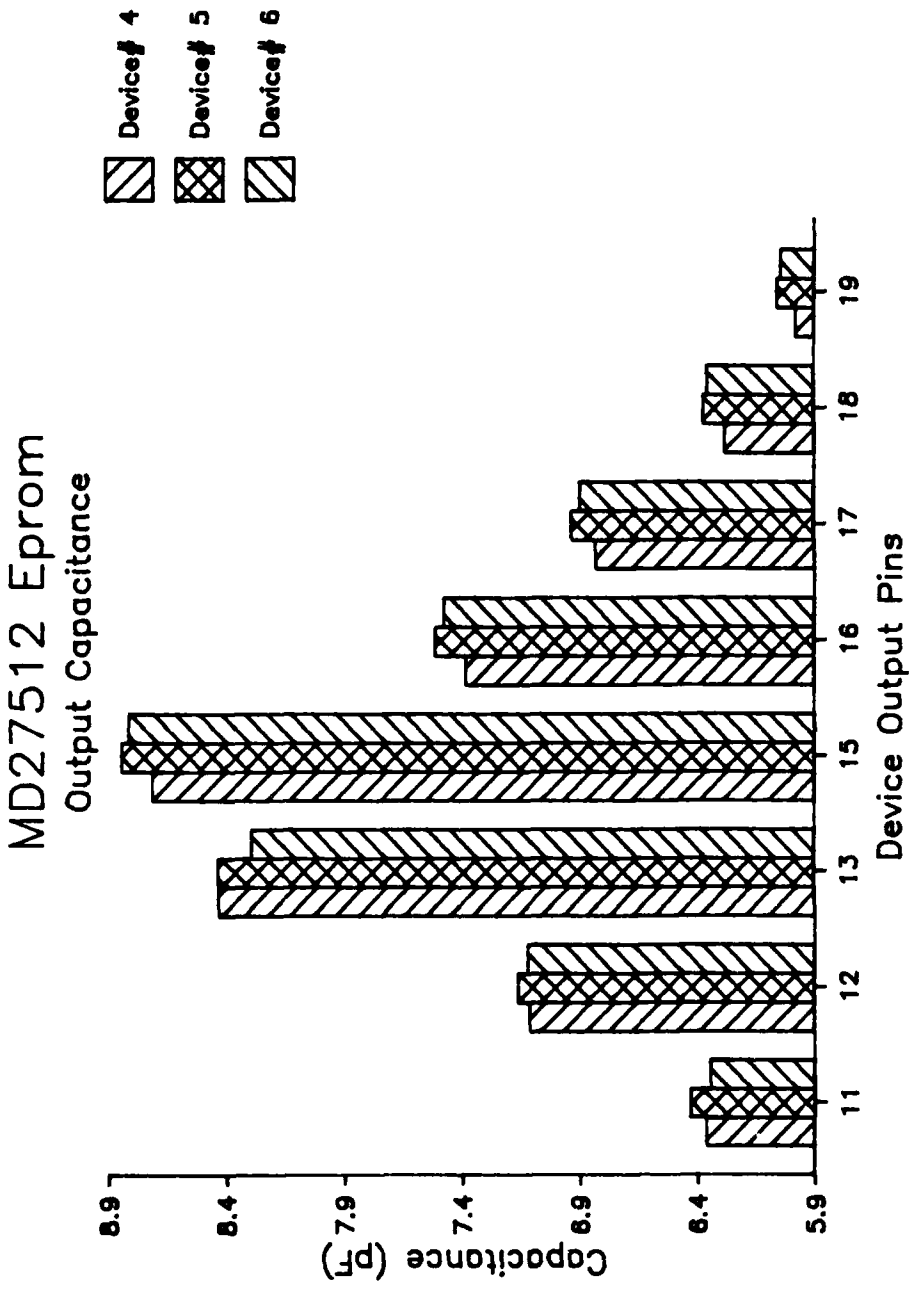


Figure 12: Output Capacitance Measurement Devices 4,5,6

8. ELECTROSTATIC DISCHARGE, VZAP TESTS

8.1 TEST METHODS

This test is performed to measure the electrostatic discharge sensitivity of the devices' input pins. Testing was performed in accordance with MIL-STD-883C method 3015.2 using IMCS model 2400C ESD simulator. After each exposure to an ESD pulse, the devices were analyzed on the Xincom 5588 test system for leakage parameters.

At the onset of this test, the breakdown voltage of the device was unknown. The approach taken was to step the voltage in 250 volt increments until the leakage current exceeded the maximum current of +/- 10uA. After this voltage level was found, it could be used as a starting point for further testing.

Each device pin under test was pulsed until a failure (>10uA) was measured. As the testing progressed, the ESD voltage pulse continually was increased until a failure could be obtained with only one pulse.

8.2 TEST SUMMARY

As described in the test methods, a starting voltage point was determined. From that voltage level, a worst case ESD voltage pulse is determined.

Figure 13 shows input leakage versus applied ESD voltage level. The ESD voltage was applied to the same device pin in steps of 250 volts until the leakage current exceeded the 10uA limit. The Xincom 5588 tester was used to measure leakage measurements after the ESD pulse was applied. The Xincom's PMU (Precision Measurement Unit) current limit was set to 20.5uA. When a value of 20.5uA is shown on a figure, assume the input is shorted. This device showed a breakdown when the voltage exceeded 6250 volts.

Figure 14 shows the leakage versus ESD voltage. The starting ESD voltage voltage level began at 6250 volts. The 6250 volt starting point was determined by Figure 13 's failure point. Notice that the amount of trials before failure has been reduced from fifteen (Figure 13) to three (Figure 14).

The goal is to determine the voltage level required to short or open the input pin with only a single high voltage pulse applied.

Figure 18 shows the effect of starting the ESD voltage at 6750 volts. Notice that the 6750 volt starting point was the failure point on graph 2. The maximum leakage limit of 10uA was exceeded when the voltage was increased to 7750 volts.

Figure 16 shows the effect of starting the ESD voltage at 7750 volts. Notice, it takes only two pulses at these levels to short the device.

Figures 17 and 18 show the effect of one 8000 volt pulse applied to an input. In both cases, the inputs were shorted.

Finally, Figure 19 shows the effect of pulsing 7 different inputs with increasing voltages, up to 8000 volts. In all cases a 8000 volt pulse caused the device's inputs to exceed the maximum limit (10uA) as specified in the proposed slash sheet.

In summary, this device can be rated in category "B" (>2000 volts ESD). The ESD voltage level which causes input leakage failures (shorts) must be greater than or equal to 8000 volts.

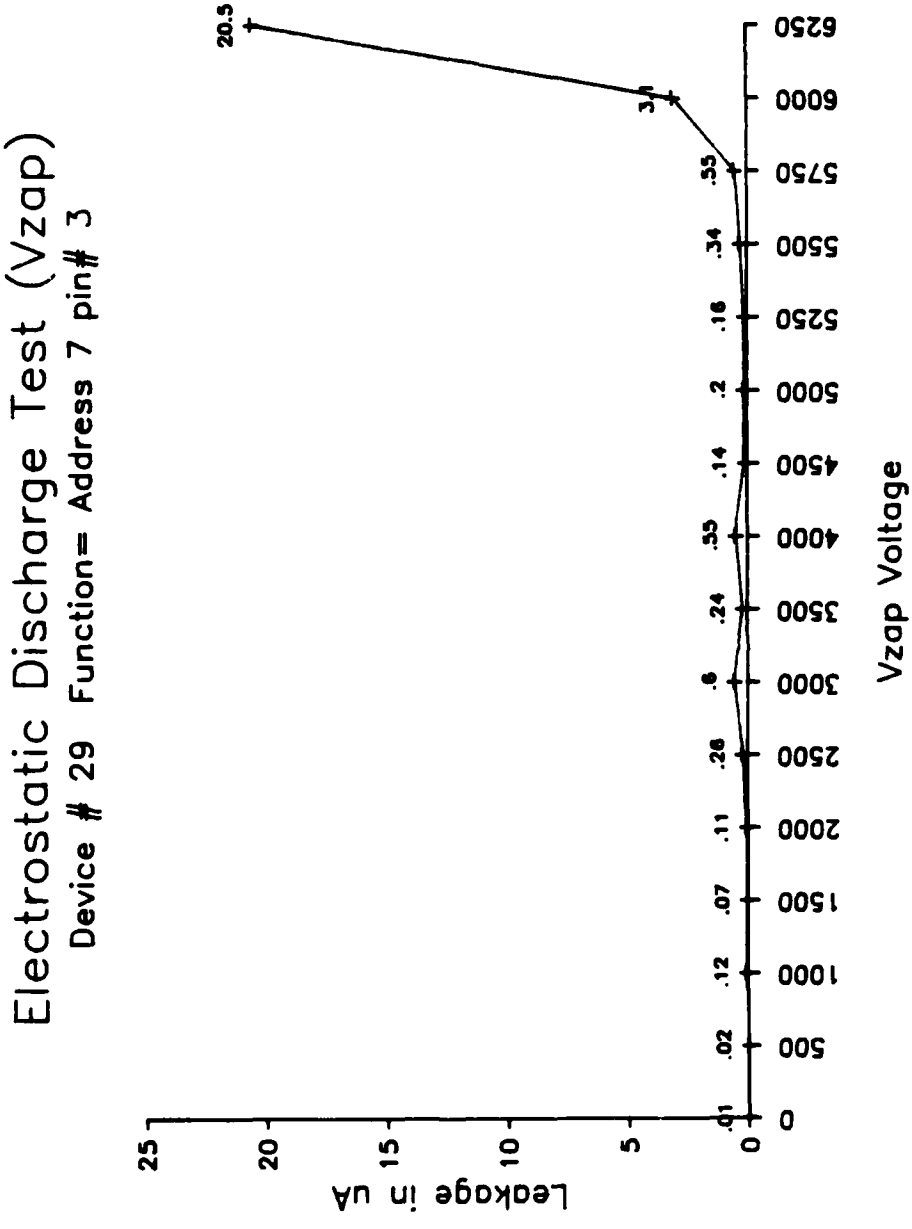


Figure 13: Electrostatic Discharge Test Device#29 Pin#3

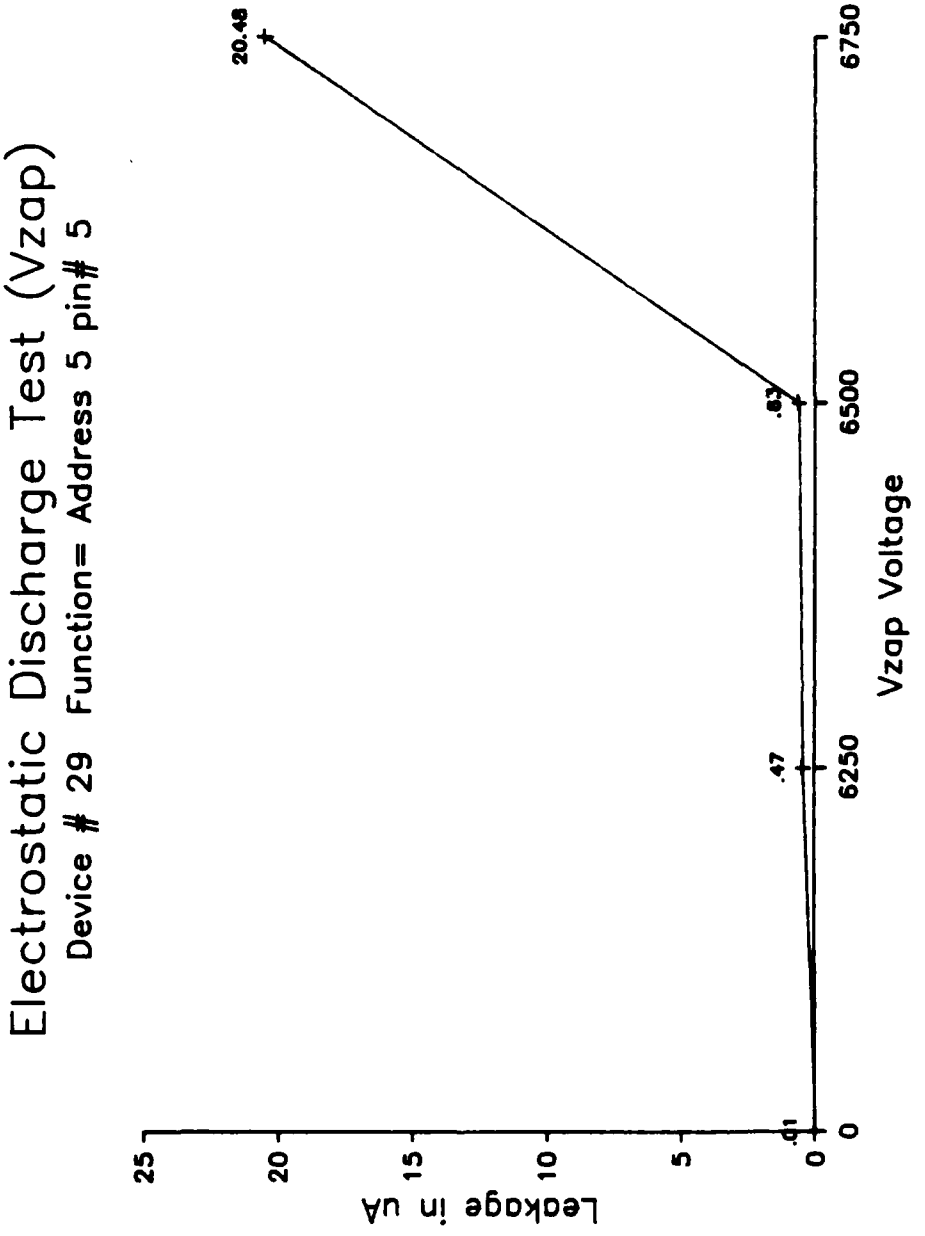


Figure 14: Electrostatic Discharge Test Device#29 Pin#5

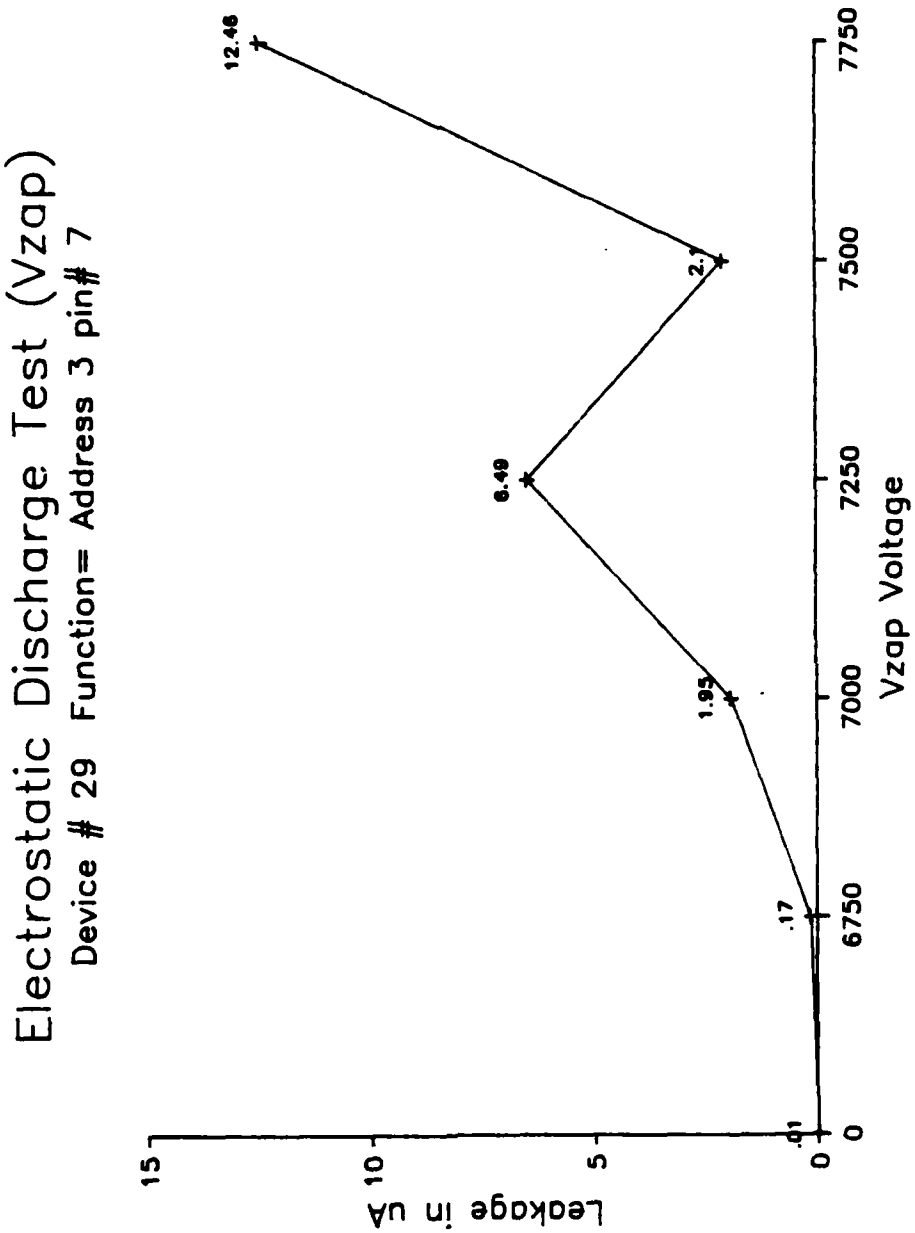


Figure 15: Electrostatic Discharge Test Device#29 Pin# 7

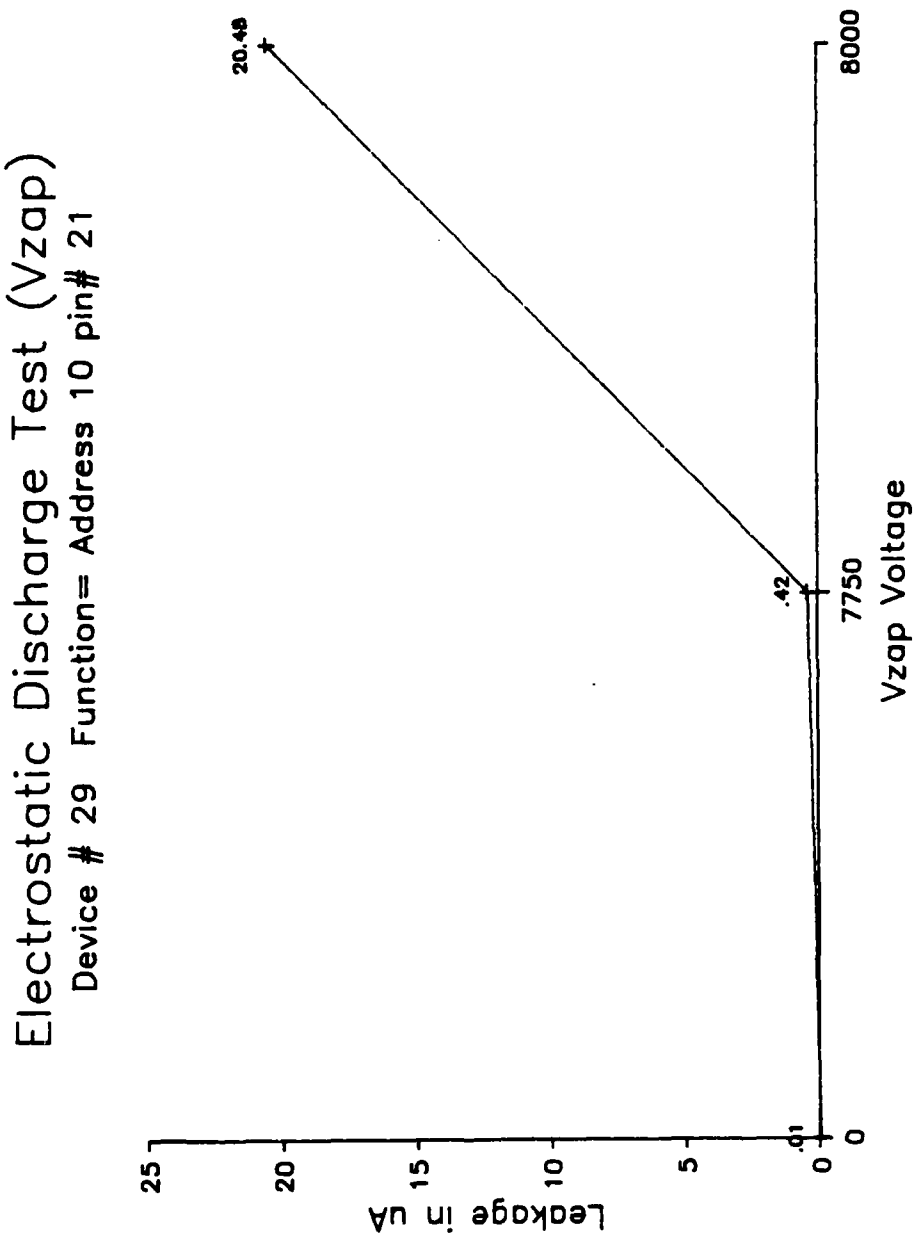


Figure 16: Electrostatic Discharge Test Device#29 Pin#21

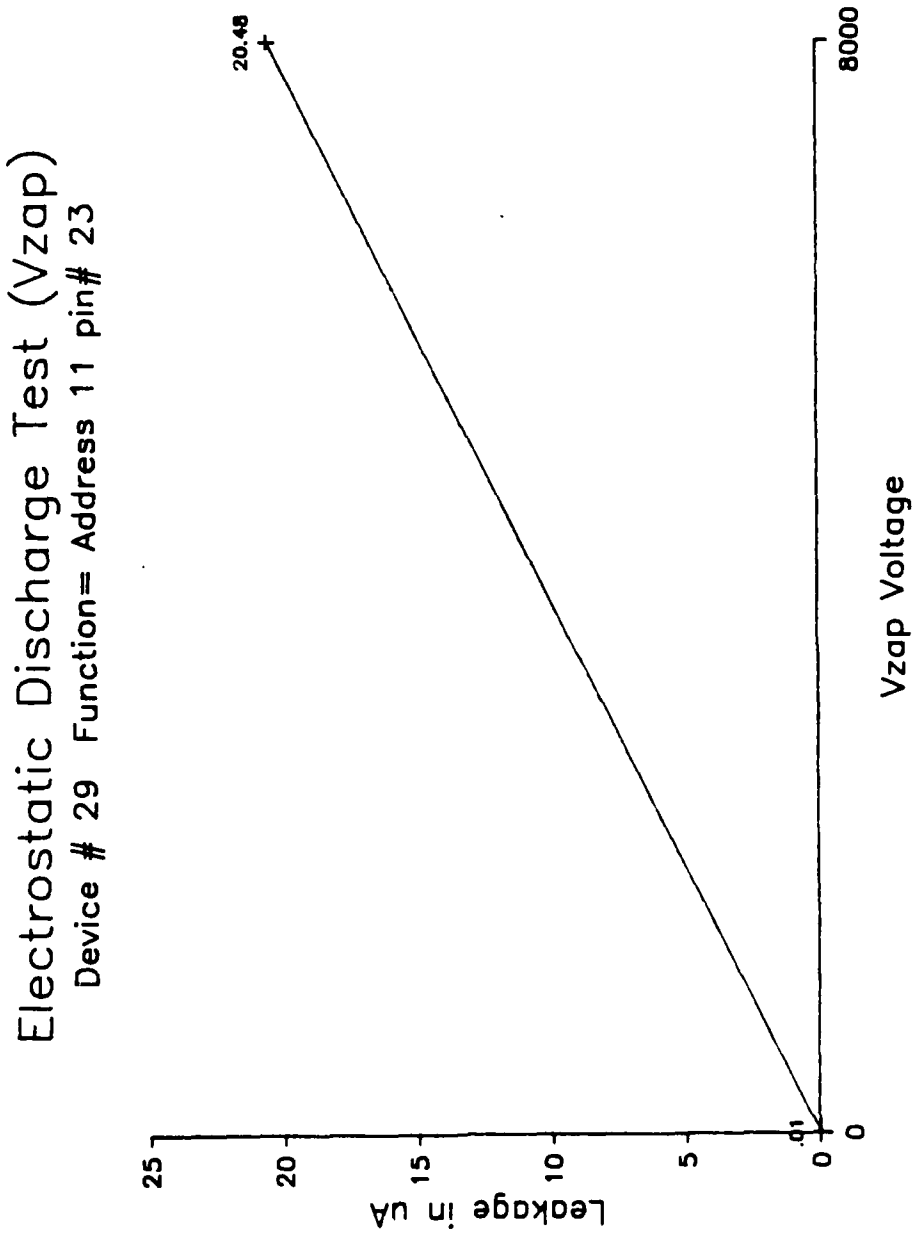


Figure 17: Electrostatic Discharge Test Device#29 Pin#23

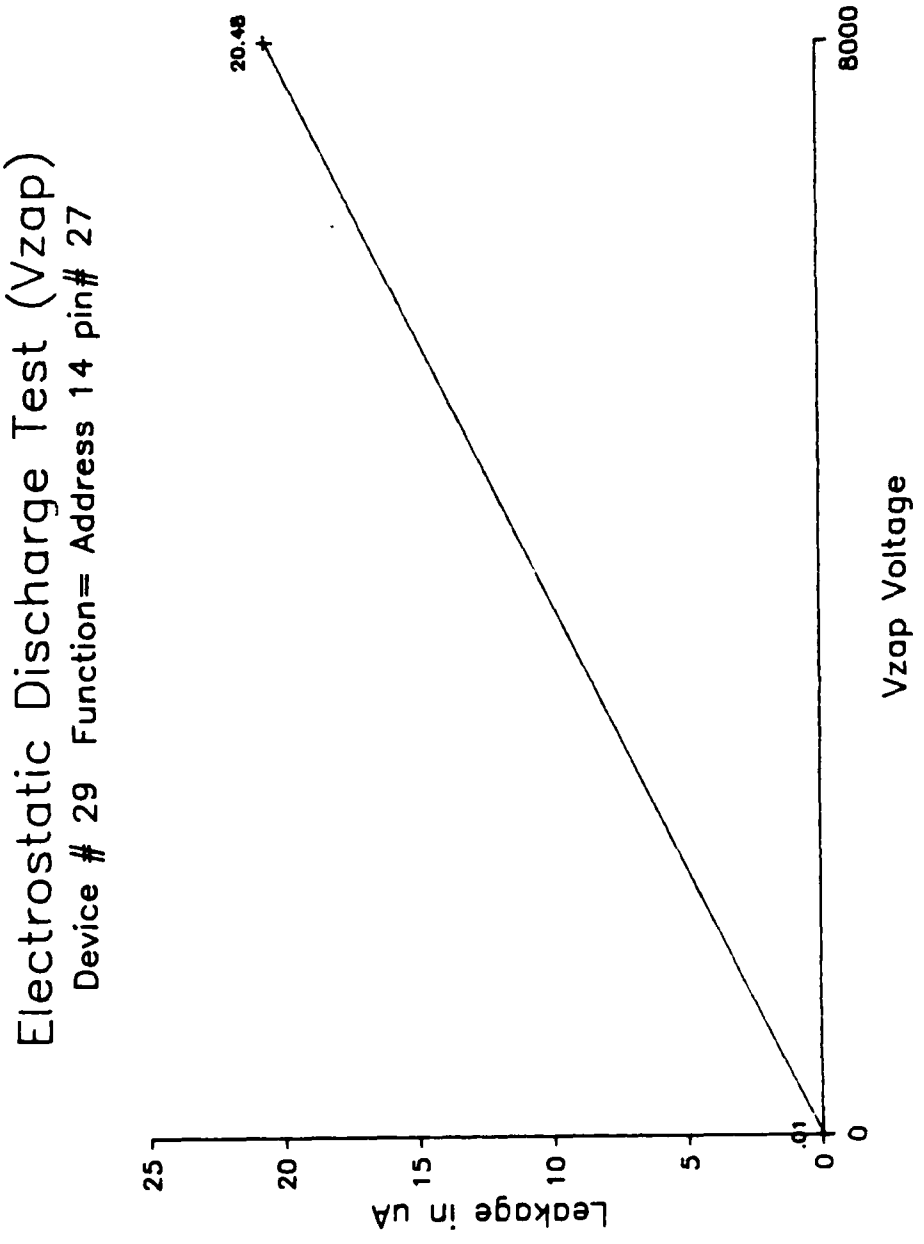


Figure 18: Electrostatic Discharge Test Device#29 Pin#27

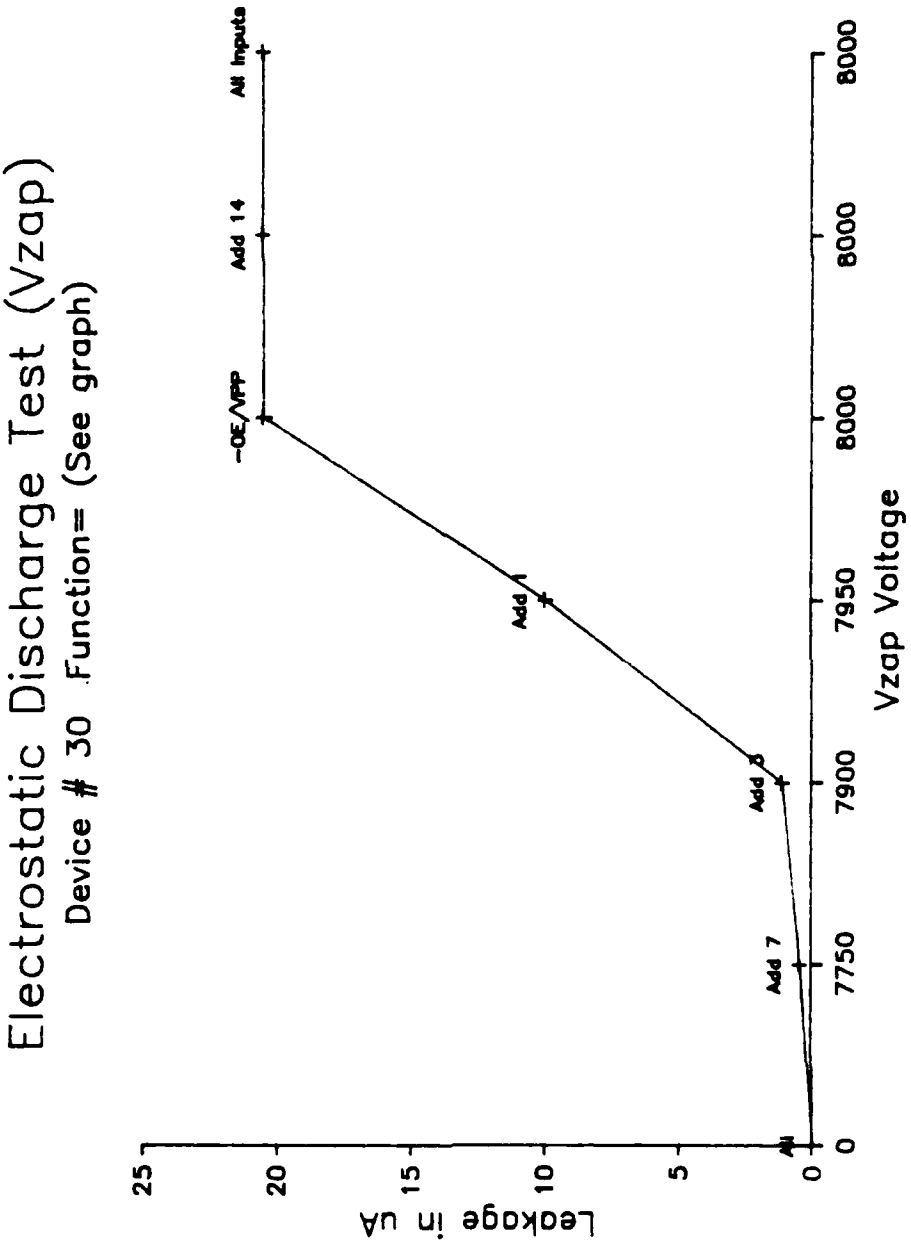


Figure 19: Electrostatic Discharge Test Device#30

9. DYNAMIC CHARACTERISTICS

9.1 TEST METHODS

The Xincom 5588 memory test system was used to collect data on the AC timing parameters. During the characterization of a particular timing parameter, all other parameters were set to their nominal limit or less stringent value. Following this technique guarantees that as the selected parameter is adjusted toward its operating limit, a failure is due to that parameter.

In addition to timing parameters, the capability to program every cell in the device was also checked. All 36 sample devices were characterized over the $-55^{o}C$ to $125^{o}C$ temperature range. The VCC was varied from 4.5 to 5.5 volts. During timing parameter measurements, a load circuit was connected to the outputs. This circuit can be found in Figure 20.

9.2 TEST PATTERNS

To allow functional testing of an EPROM device, a pattern must be programmed into the memory array. Two patterns were used as test patterns for the device.

The first pattern consists of random data. This pattern was generated on GTE's IBM 370 mainframe computer. The random data pattern simulates the eventual data which will be programmed into the device. In this document, the random data pattern is called "TRUE Pattern."

To ensure that every cell can be programmed to a "1" and a "0," another pattern was created by inverting the TRUE Pattern. This pattern is called "FALSE Pattern."

The effectiveness of the random data patterns will be addressed in the AC Test results section.

9.3 A.C. PARAMETRIC MEASUREMENTS

The A.C. characterization not only determines the operating limits of the timing parameters but also verifies the integrity of the internal functions under dynamic conditions. The internal functions of the memory can be divided into the following blocks:

- o Address Decoders
- o Sense Amps
- o Memory Array
- o Data I/O Circuitry

During the A.C. parametric measurements, all of the functional blocks are being verified. For example, when the device's address access time is being measured at $-55^{o}C$, all functional blocks are being subjected to the same extreme temperature.

9.3.1 Address Access Time

The address access time measurement technique used was to first lower the -CE and -OE/VPP signals of the device, then 20ns later change the address to a specific location, then check for valid data. The point at which the valid data was verified was determined by a programmable timing generator.

The initial value of the timing generator was set to a known failure point (40ns after address change). The access time measurement loop was setup to increment the timing generator in 1ns steps on failure. This loop continued until the device passed. The criteria for pass/fail was the data outputs of the device matching a known pattern in the tester for the entire address span of the device.

The testing was run at $-55^{o}C$, $25^{o}C$ and $125^{o}C$. In addition, the VCC of the device was changed from between 4.5 and 5.5 volts for each temperature.

Two test patterns were evaluated. Both patterns (TRUE, FALSE) were programmed into the device. The effect of temperature, VCC voltage and pattern are shown in Figure 21. As shown, the worst case condition for address access time was high temperature ($125^{o}C$) and low voltage (4.5V).

9.3.2 Chip Enable Access Time

As in the address access time measurements, the measurement technique used for the Chip Enable parameter was the same except that both the addresses and -OE/VPP (Output Enable) were valid first, then 20ns later the Chip Enable was brought low.

As in the address access time measurements, the worst case temperature (125°C) and voltage (4.5V) were the same. Refer to Figure 22. The FALSE Pattern proved to be worst case.

9.3.3 Output Enable Access Time

A prime concern in the design of systems is bus contention. To avoid potential damage to outputs connected to a bus, system timing must be such that each line is driven by only one output at a time. The system designer must therefore know how long it takes a device to respond to an enable signal.

The Output Enable access time measurement shows the effect of temperature, pattern and VCC voltage on this parameter. The measurement technique used was the same as in the address and Chip Enable test with the following exceptions. The addresses and Chip Enable signals become valid first, then output enable is brought low after the worst case address access time has been met. This technique allows the data to be waiting for the output enable signal instead of causing a possible race condition which would give uncertainty in parametric values.

Figure 23 shows the measured results. Note that the FALSE pattern caused worst case measurements at 125°C and 4.5 Volts.

9.3.4 Address Hold Time

This test measures the amount of time the data is valid after the addresses change state, assuming that Chip Enable and Output Enable are still active. Using the same technique as performed for access time measurements, the worst case measured value was 58ns at 4.5 volts at a temperature of 125°C. Refer to Figure 24.

9.3.5 Chip Enable/Output Enable Float Time

This test measures the amount of time required to tri-state the data outputs from an active state. Two control pins (-OE/VPP and -CE) have this same function. The voltage at the output pin, at turn off, largely becomes a function of the time constant of the capacitance and load resistances. The output stage actually turns off long before the voltage on the output pin reaches its stable high impedance state.

The technique used to measure this value has typically been to disable the outputs and wait for a 0.5 volt change in voltage level. The 0.5 volt level typically is determined by an arbitrary method. Because of minor variations in the VOH and VOL levels from die to die, the 0.5 volt level is acceptable to many vendors.

The float time when measured on automatic test equipment and using the above method gives inconsistent results. If a device had a lower VOL level it would appear to be slower because the output level had farther to rise, hence, more time was required to reach the absolute D.C. level.

The method used in this characterization is an enhancement from the conventional measurement techniques by the following procedures. First, the device output levels (VOH and VOL) are measured with the output load connected. Then the values are averaged into a VOH average and a VOL average. The comparator limits are set to VOL+100mV and VOH-100mV. The modified VOL and VOH levels are used to determine the float condition.

By using this method, a standardized measurement can be made with high accuracy. When testing this parameter over temperature with the old method, float times would change not only due to the effect of temperature on this parameter but also because the VOL and VOH levels would shift. Using the new method the measurements are self calibrated for the shift in VOH and VOL and give a true measurement of the parametric variation over temperature.

The Chip Enable float time (Figure 25) was measured to be 60ns with VCC at 4.5 volts. The float time decreased to 52.7ns when VCC was raised to 5.5 volts. The Output Enable float time (Figure 26) measured 33.3ns with VCC at 4.5 volts. The float time decreased to 25.4ns when the VCC was increased to 5.5 volts. In both measurements, 125^{o}C caused the worst case values.

9.4 TEST SUMMARY

In general, the measured A.C. parameter values were within the maximum and minimum limits set by the proposed slash sheet. A sample SHMOO plot (Figure 27) is included to show the effect of varying the device's VCC with respect to address access time.

A.C. TESTING LOAD CIRCUIT

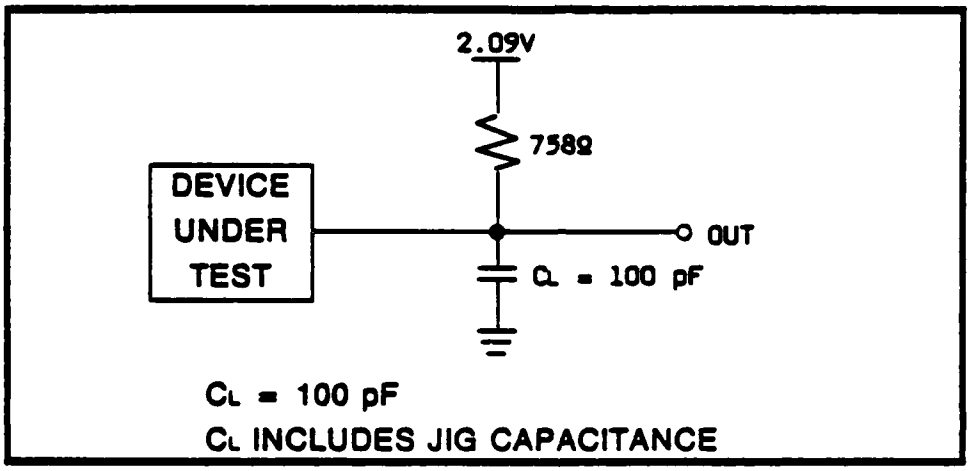


Figure 20: Output Load Circuit

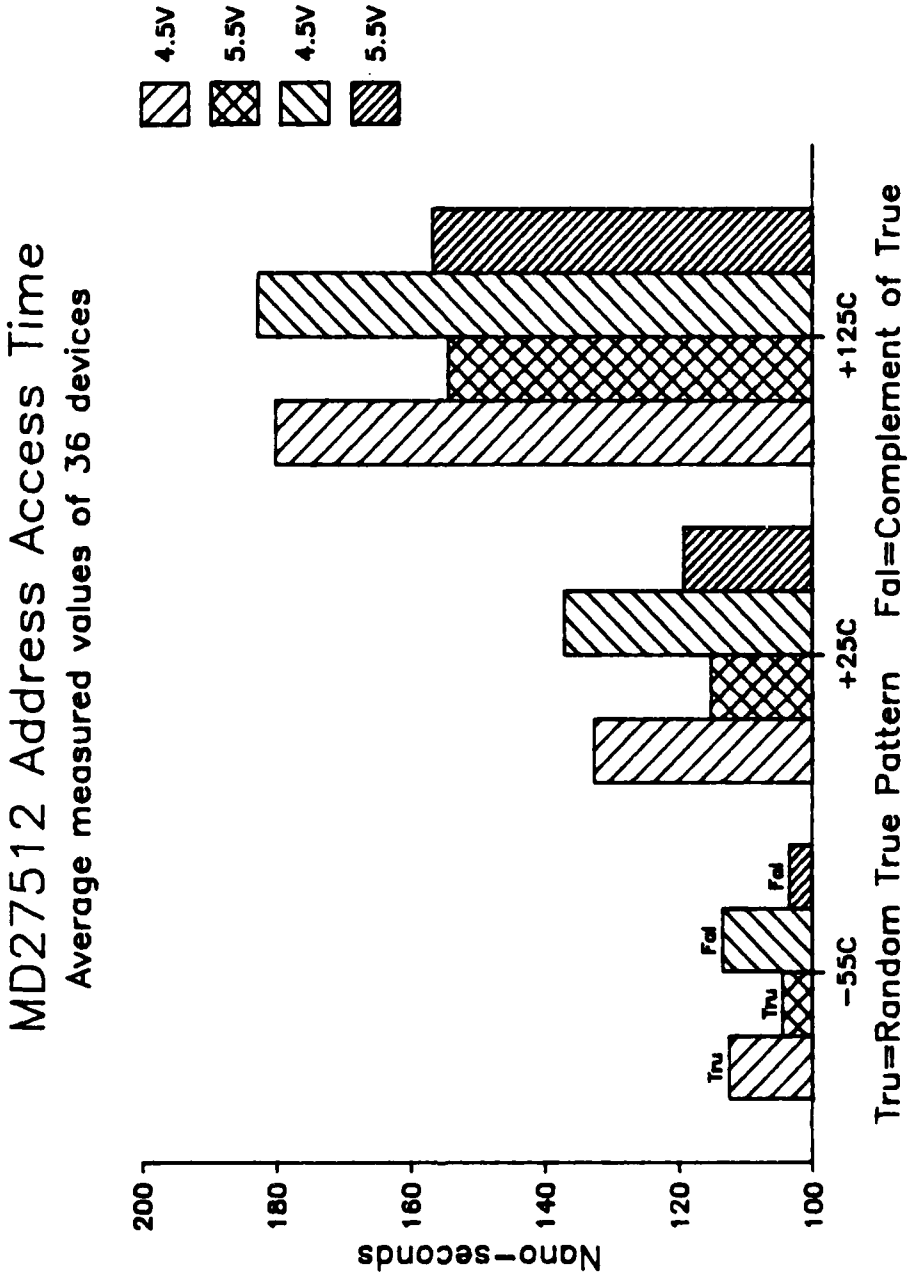


Figure 21: Address Access Time VS Temperature and Pattern

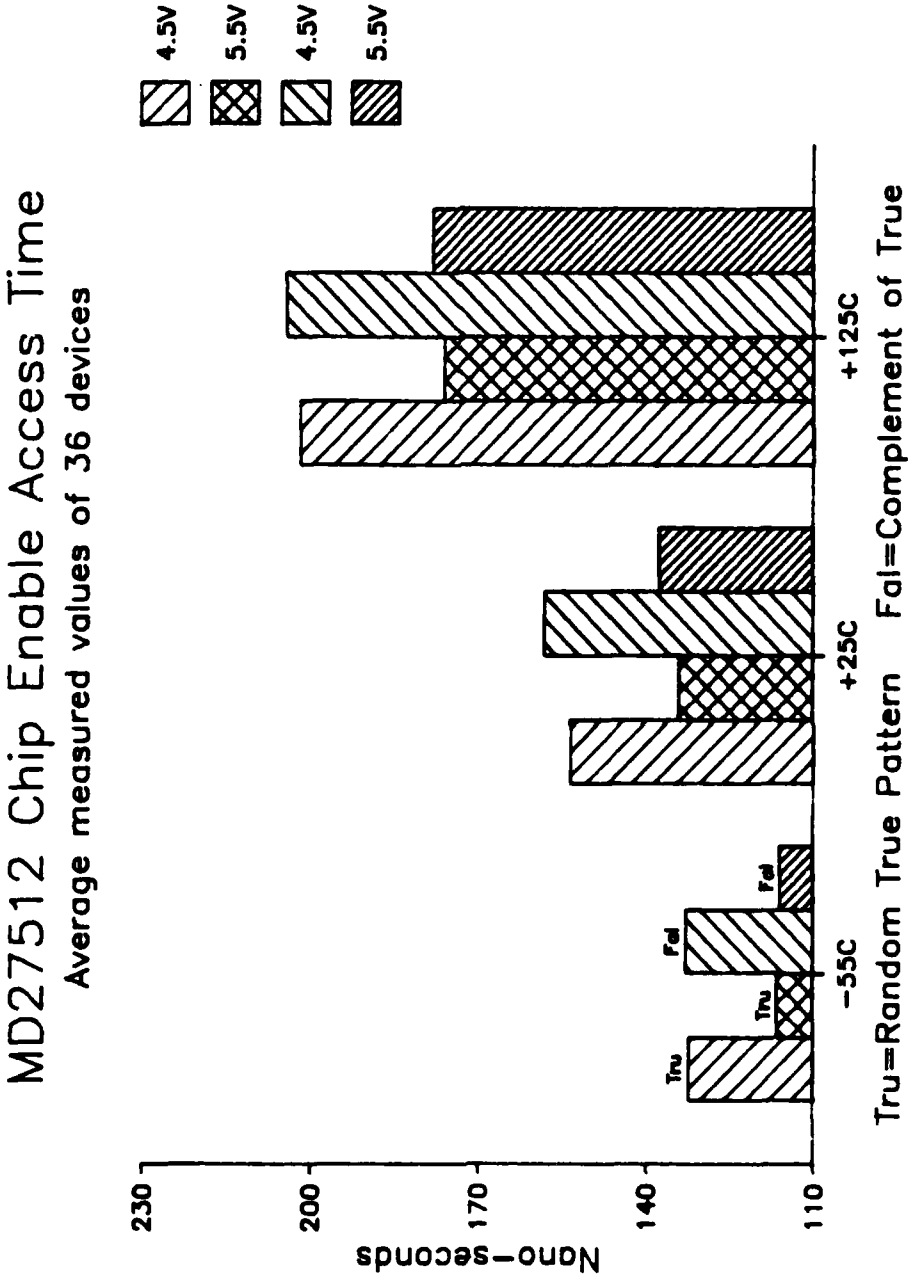


Figure 22: Chip Enable Access Time VS Temperature and Pattern

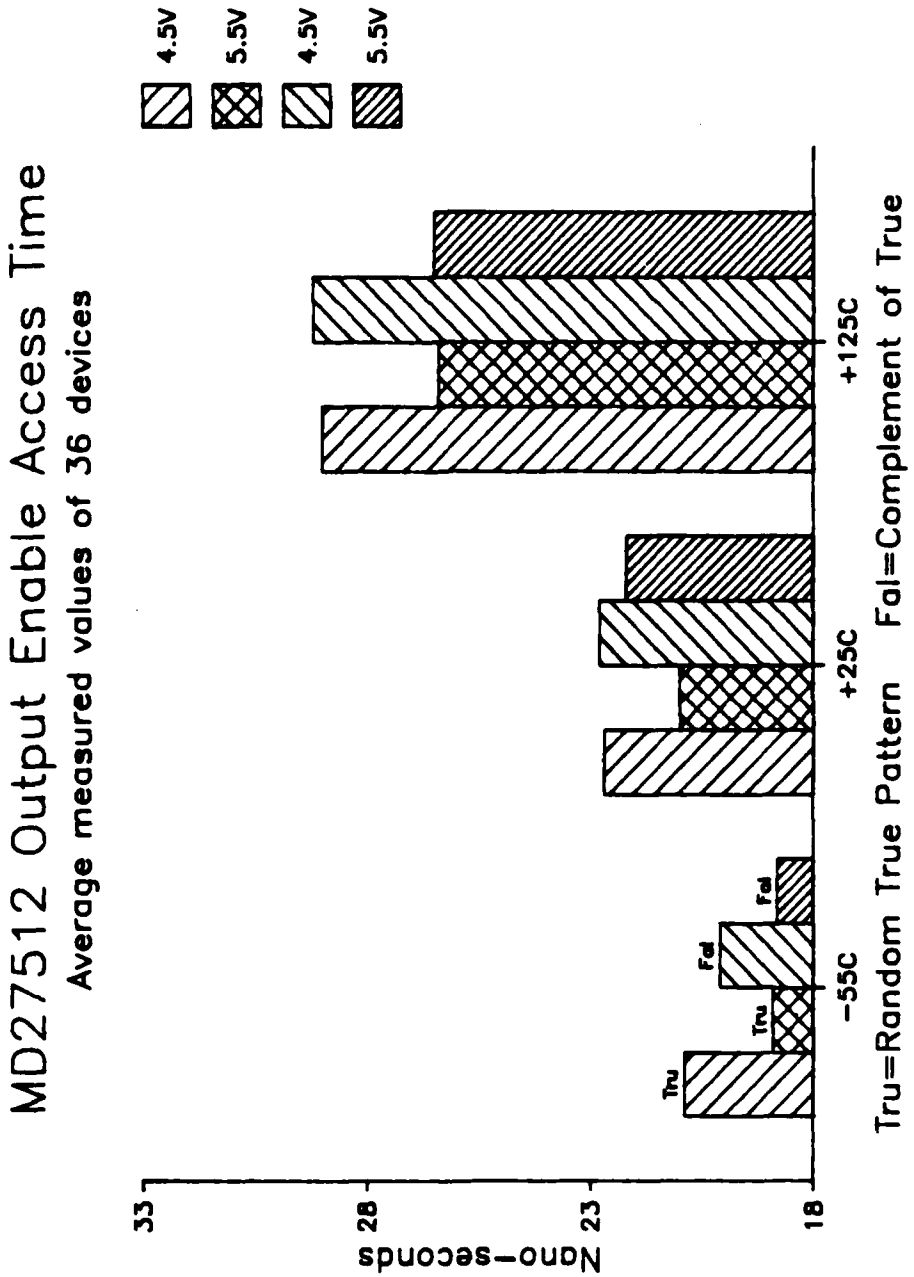


Figure 23: Output Enable Access Time VS Temperature

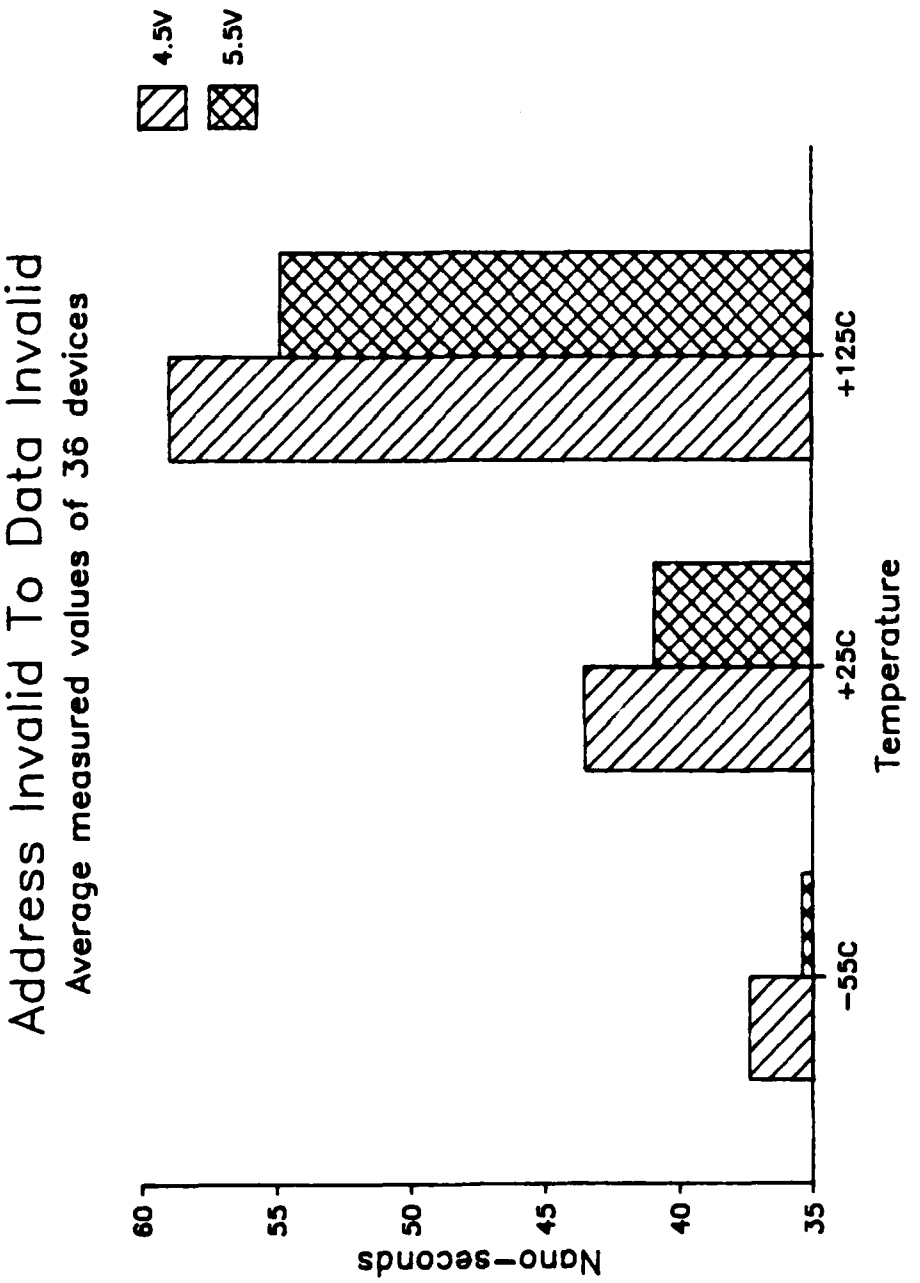


Figure 24: Address Hold Time

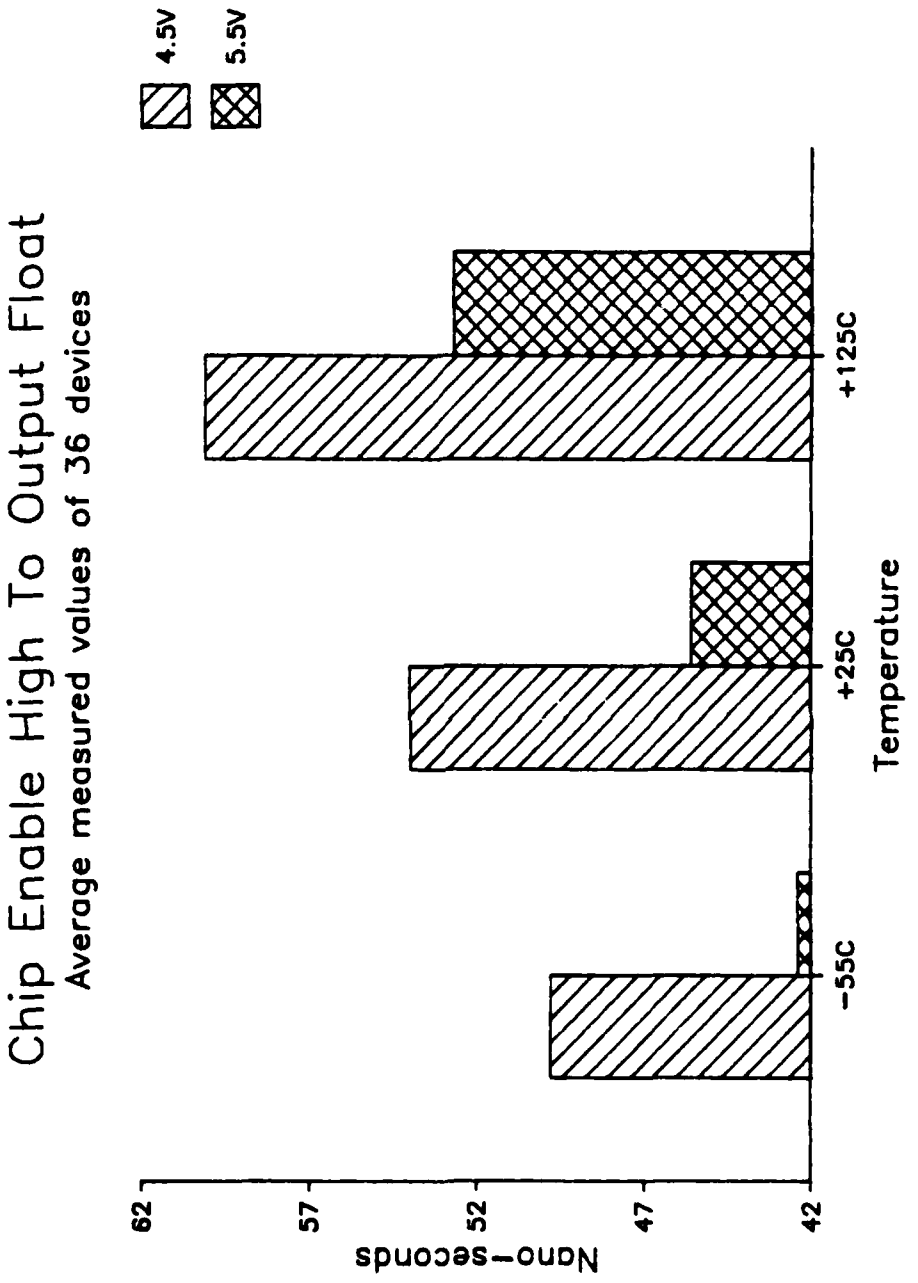


Figure 25: Chip Enable High to Output Float

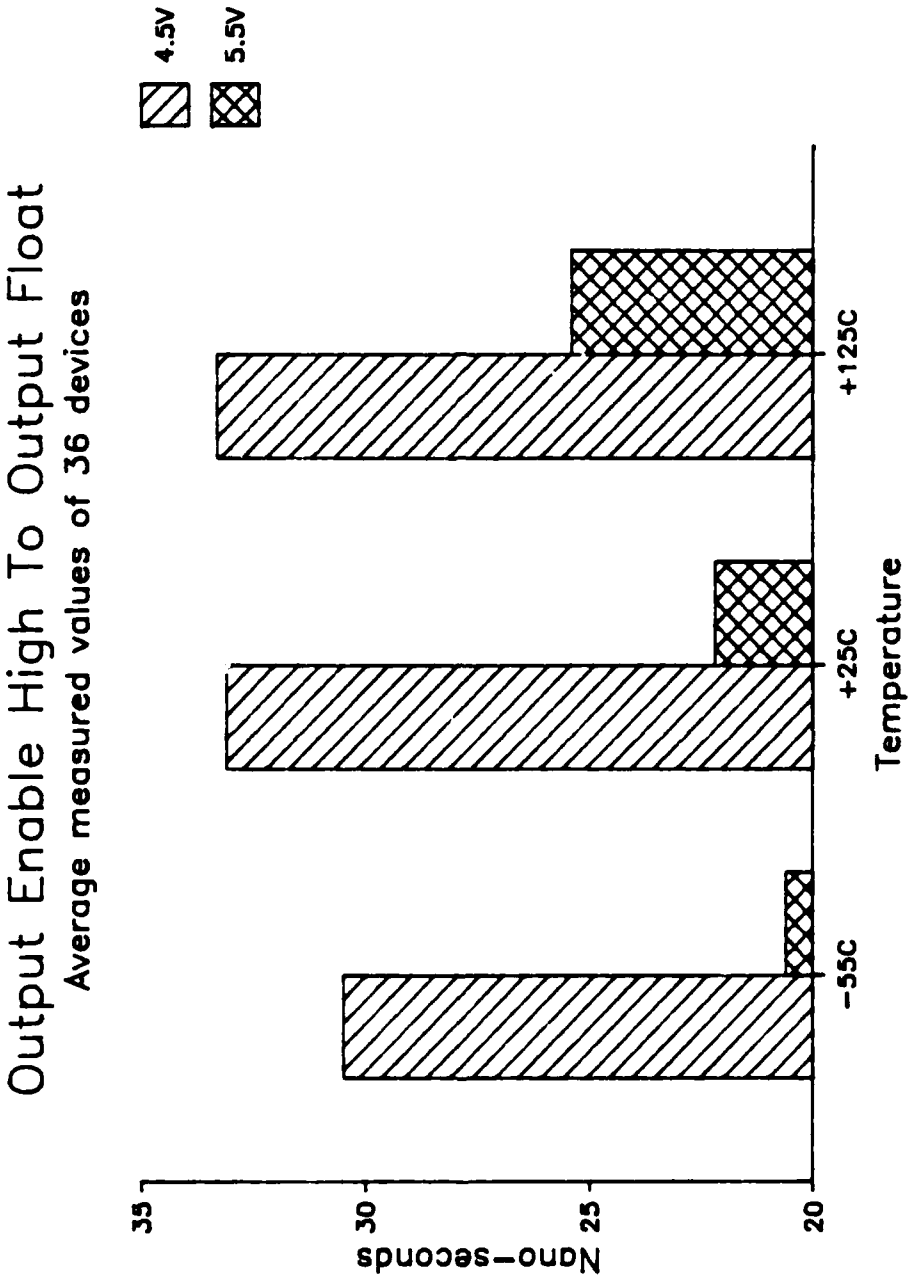


Figure 26: Output Enable High to Output Float

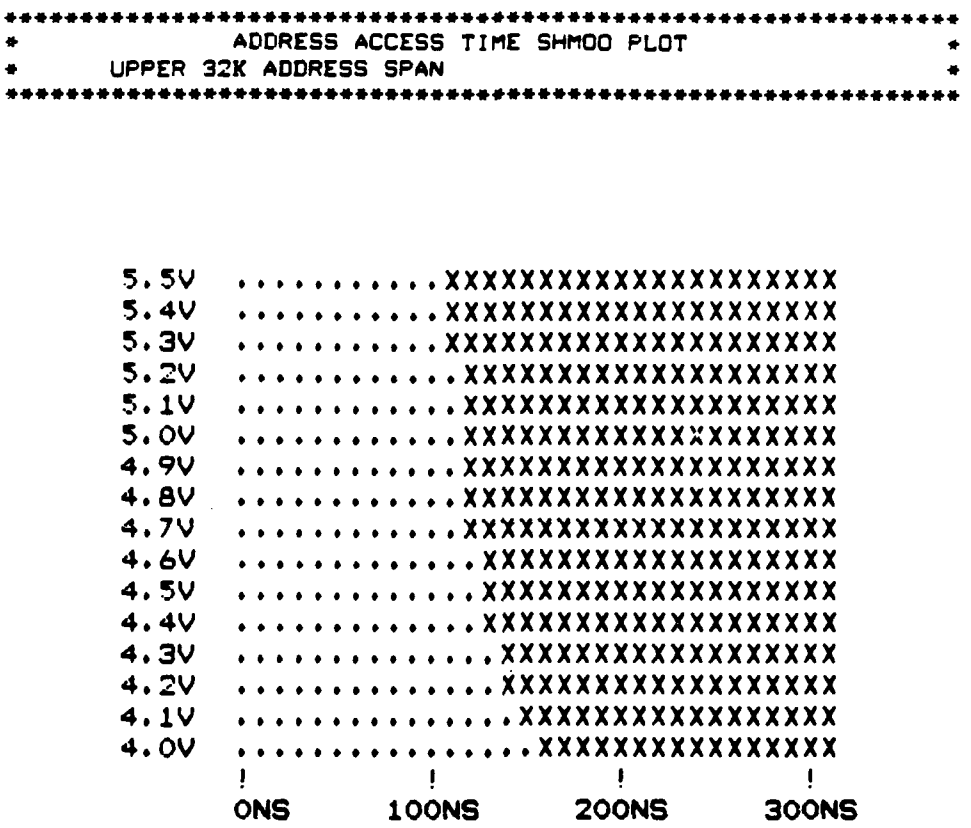


Figure 27: Address Access Time SHMOO Plot

10. FLOATING GATE MARGIN MEASUREMENTS

10.1 OBJECTIVES

This test is used to determine the amount of trapped charge (margin) stored on the floating gate of the EPROM cell. The principles of UVEPROM [2] are best explained by the operation of the floating gate storage cell. The storage cell consists of two polysilicon gates, a conventional control gate, and an electrically isolated floating gate. The floating gate has two stable states, an erased state, and a programmed state. Programming is accomplished by raising both the drain and control gate to a high voltage causing a high electric field. Electrons traveling in the channel are accelerated by the field and some gain enough energy to leave the channel, transverse the oxide, and become trapped on the floating gate. Once trapped on the floating gate, they remain there, unless erased by exposure to UV light.

The threshold voltage of a cell properly programmed as a "0" is greater than approximately 7.0 volts, while that of a properly erased "1" is approximately 1.5 volts. During a read operation, the control gate is biased to approximately 5.0 volts (determined by VCC and the read mode program voltage VPP). IDS will flow only for a VT < 5.0 volts, providing the basis for sensing the cell's state. The difference between the programmed (or erased) threshold voltage and the 5.0 volts sense voltage will be called the margin of the device.

A test method was developed to measure the effect of a high temperature bake (90 hrs. at 140°C) and dynamic burn-in (168 hrs at 140°C) on margin values.

10.2 TEST METHODS

To measure margin values, a test was developed to run on the Xincom 5588 test system. Because the test was implemented on an automatic test system, the accuracy and repeatability of measurement values could be done with high levels of confidence.

Because of the structure of the EPROM cell, the test could be implemented with minimal effort. Basically, the voltage on the control gate in the EPROM cell is directly linked to the VCC and VPP pins of the device. The device is first

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[2] Excerpt from RADC-TR-80-401, Part 2. A096065.

programmed with all zeros, to place the maximum amount of potential on the floating gate. Then, the VCC and VPP are raised until the outputs switch state (0 to 1). The voltage at which the outputs switch can be directly correlated to the margin value. The technique used during the testing was to run a functional test (nominal timing) which verified all locations before stepping the voltage. The voltage step was set to 0.05 volts. The maximum voltage limit must be observed. Typically, the voltage can be raised to 8 volts without damage to the device. If the 8 volt limit is reached, the assumption can be made that the margin is greater than 2.5 volts which gives more than adequate data retention. The above method was used for all the margin tests performed.

10.3 MARGIN TEST

10.3.1 Margin VS Burn-in and Bake

This test measures the effect of a bake (90hrs/140^{O}C) and dynamic burn-in (168hrs/140^{O}C) on the EPROM's floating gate margin value. Initially, the devices were programmed with all zeros. Then the margin values were measured and recorded. Next, the devices were baked at 140^{O}C for 90 hours, and again, the margin values were measured. Lastly, the devices were subjected to a dynamic burn-in of 140^{O}C for 168 hours. In Figures 28 thru 33, the burn-in test will be represented by the "DBRN" symbol. The margin values again, were measured and recorded.

Refer to Figures 28 thru 33. As shown, 18 of the 24 devices showed no degradation of their margin values. Two devices had their margin values decrease as expected. Four devices, (1,5,14,17) gained charge on their floating gates after bake and dynamic burn-in. At present, the gaining of charge on a floating gate, induced by high temperature and bake, is a phenomenon which warrants additional investigation.

In all cases, the margins on the floating gates of the devices tested were all well above the recommended 0.5 volt limit to ensure extended data retention.

10.3.2 Margin VS UV Light Exposure

The UV light exposure test consists of measuring the amount of time required to erase either the entire array or the weakest cell with a UV light source placed 1 inch above the device.

The UV light exposure test could not be performed because of the Xincom's 32K X 8 pattern memory (TTRAM) limitations. When testing this device, two TTRAM loads are required. While the second 32K pattern is being loaded, the UV light would still be erasing the array; hence, two separate tests would need to be performed. The fact that two separate tests are required is not the limiting factor; however, because several variables, such as UV light intensity and programming equipment variance, would directly effect the measurements, it was decided not to run the test.

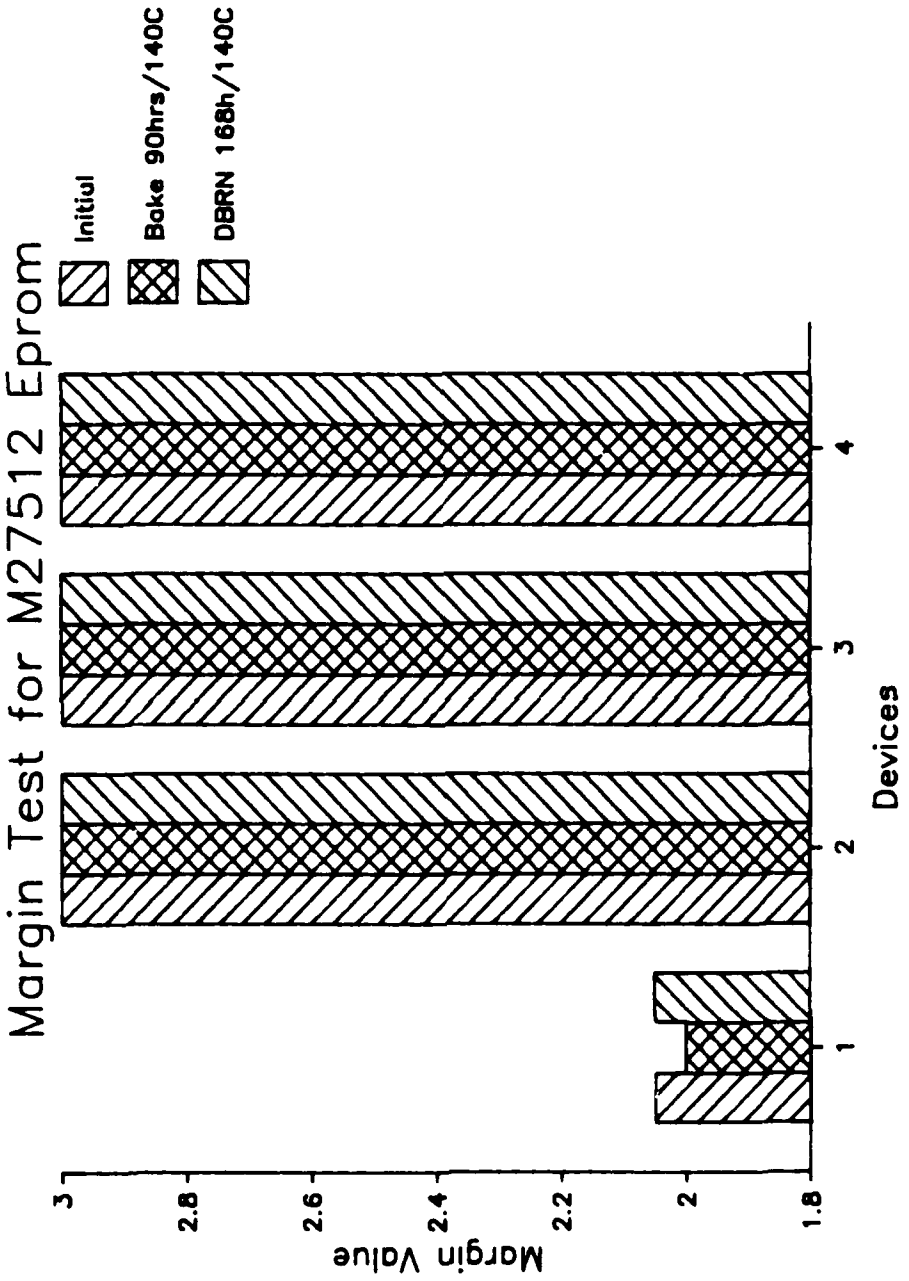


Figure 28: Floating Gate Margin Test Device#'s 1 thru 4

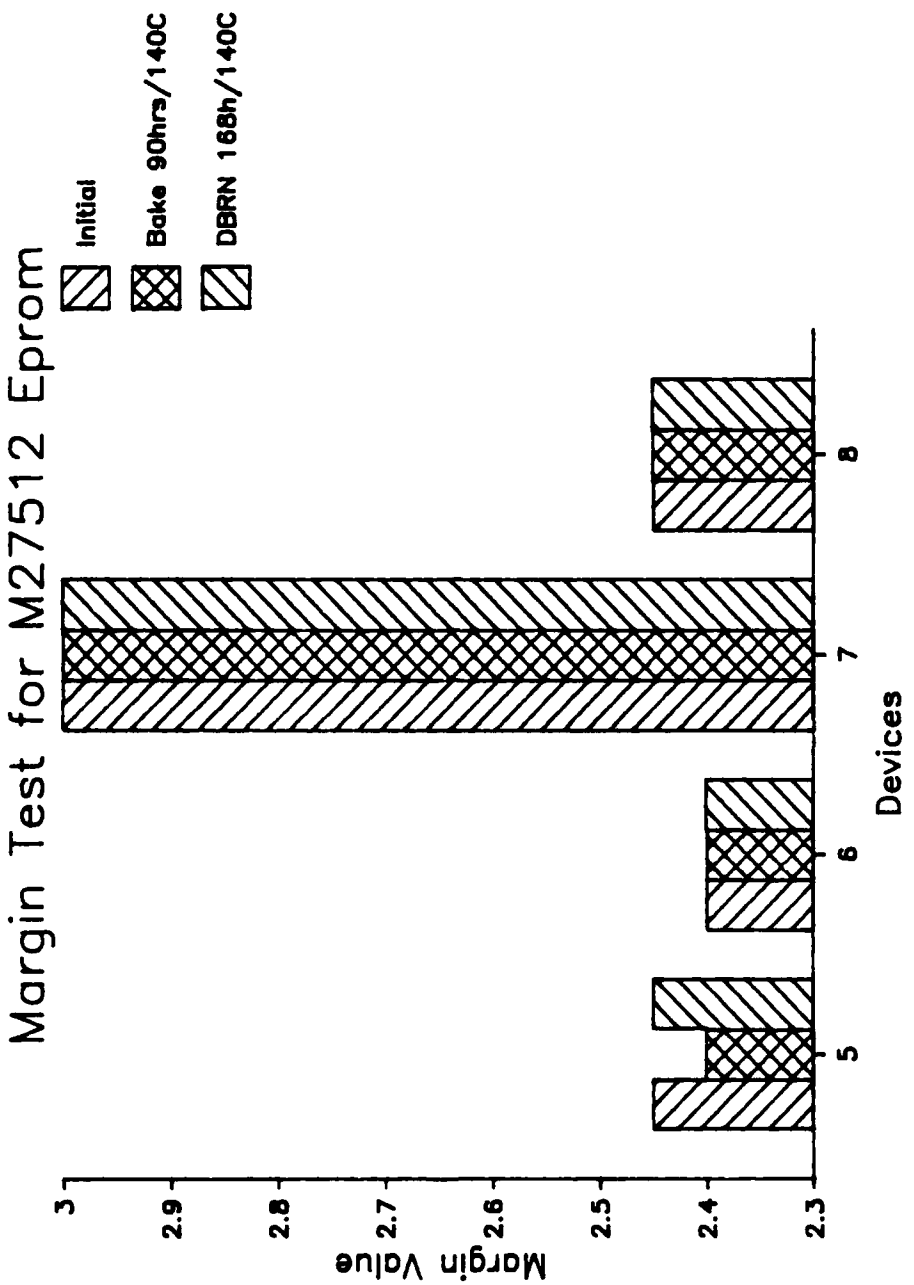


Figure 29: Floating Gate Margin Test Device#'s 5 thru 8

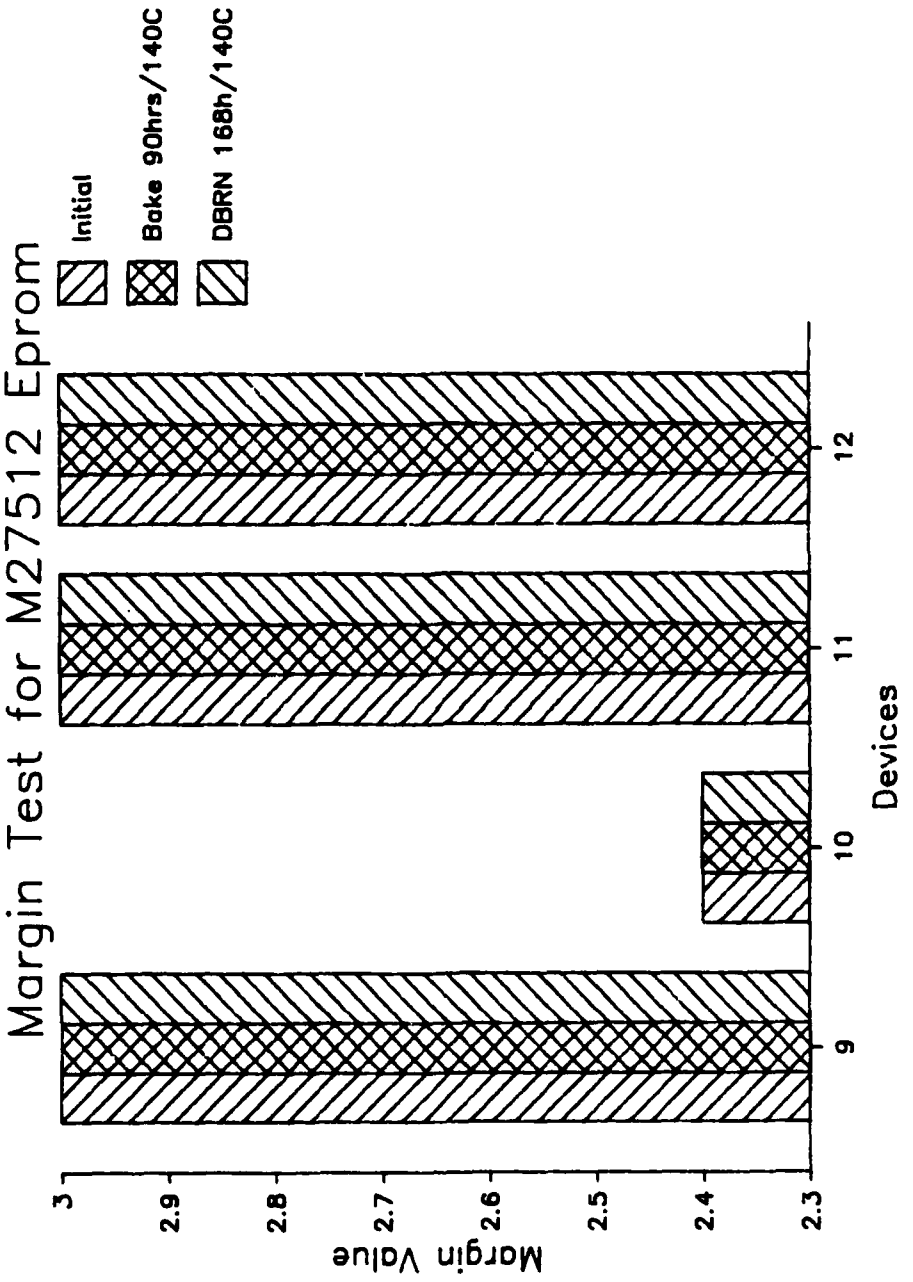


Figure 30: Floating Gate Margin Test Device#'s 9 thru 12

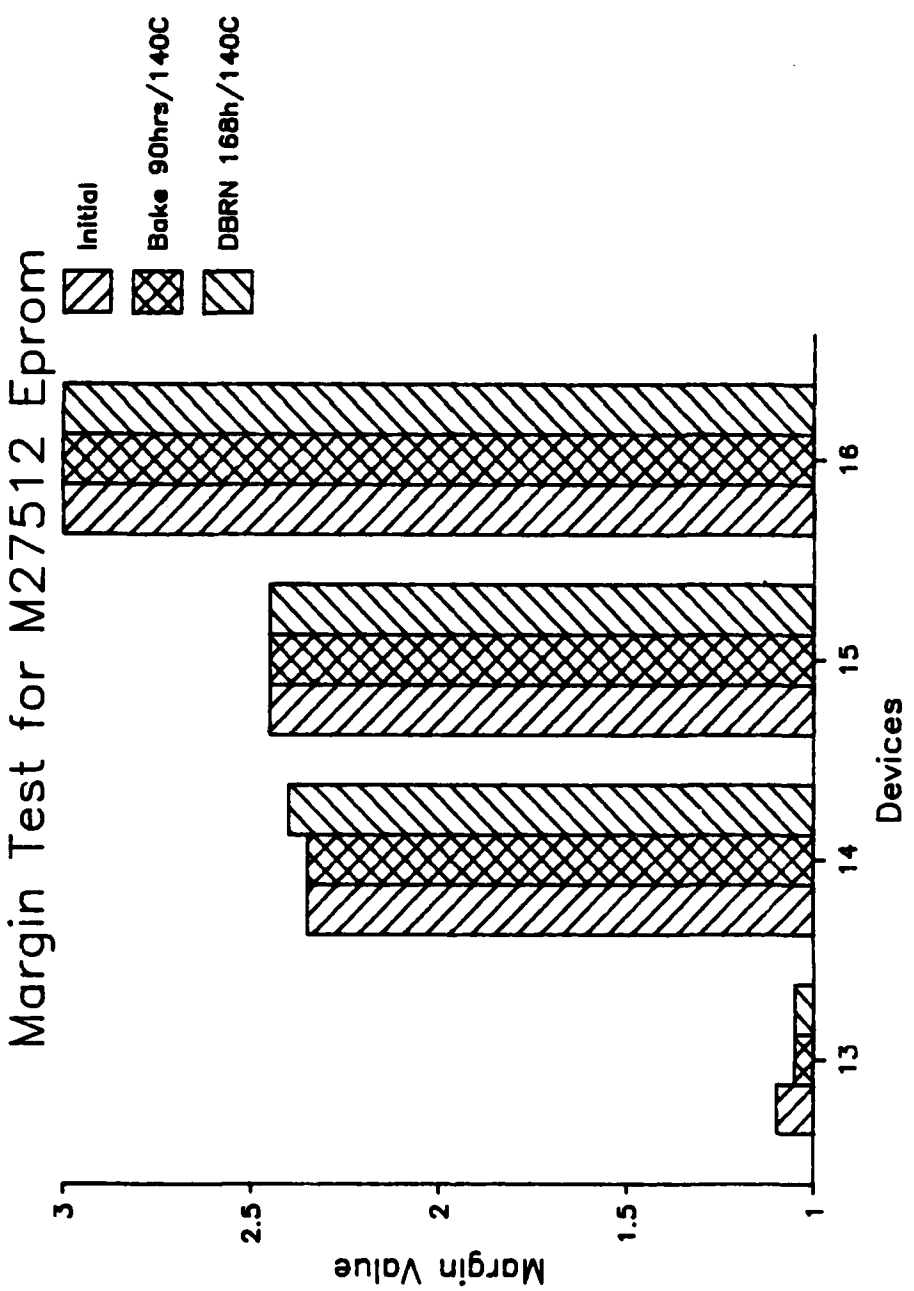


Figure 31: Floating Gate Margin Test Device#'s 13 thru 16

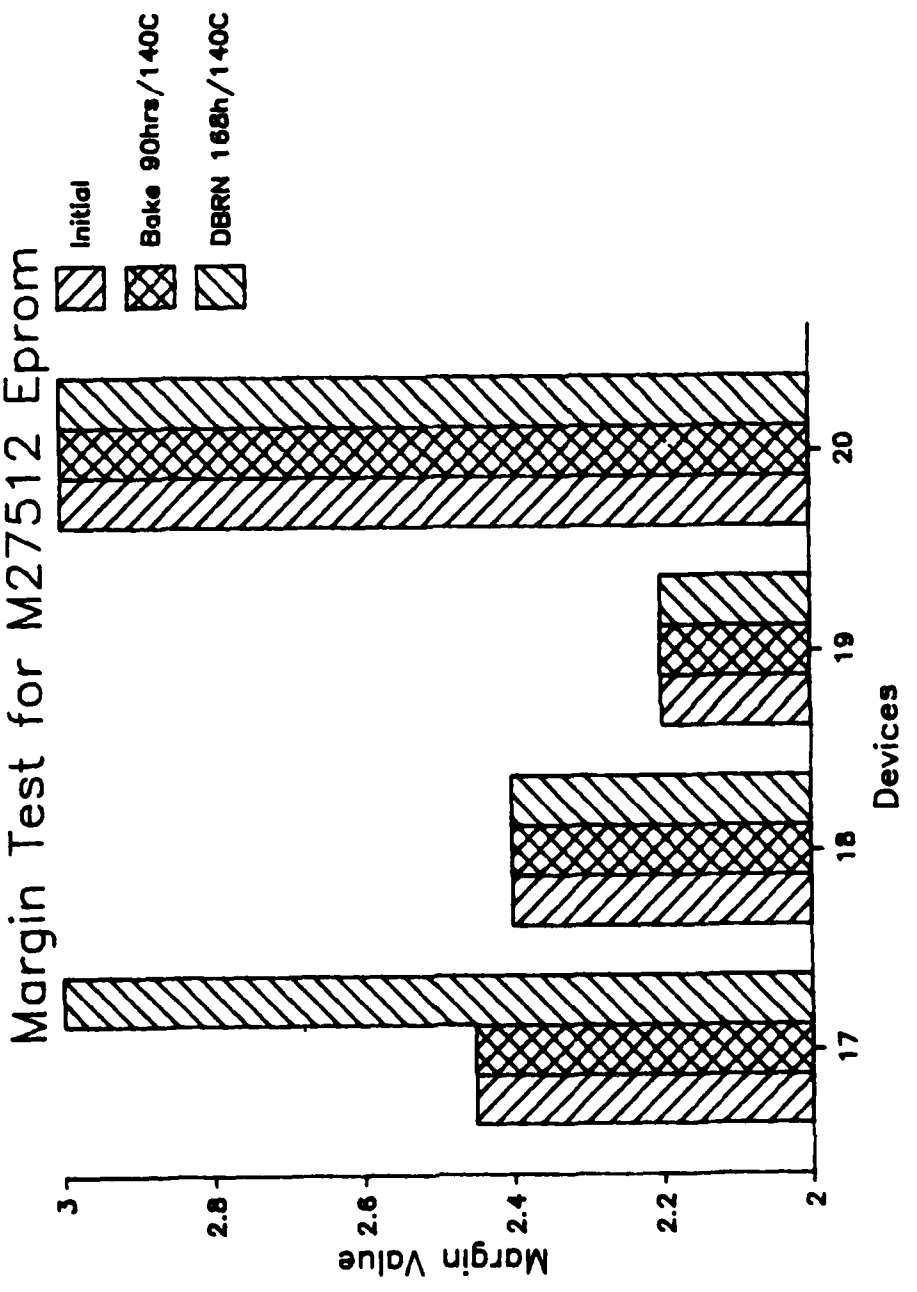


Figure 32: Floating Gate Margin Test Device#'s 17 thru 20

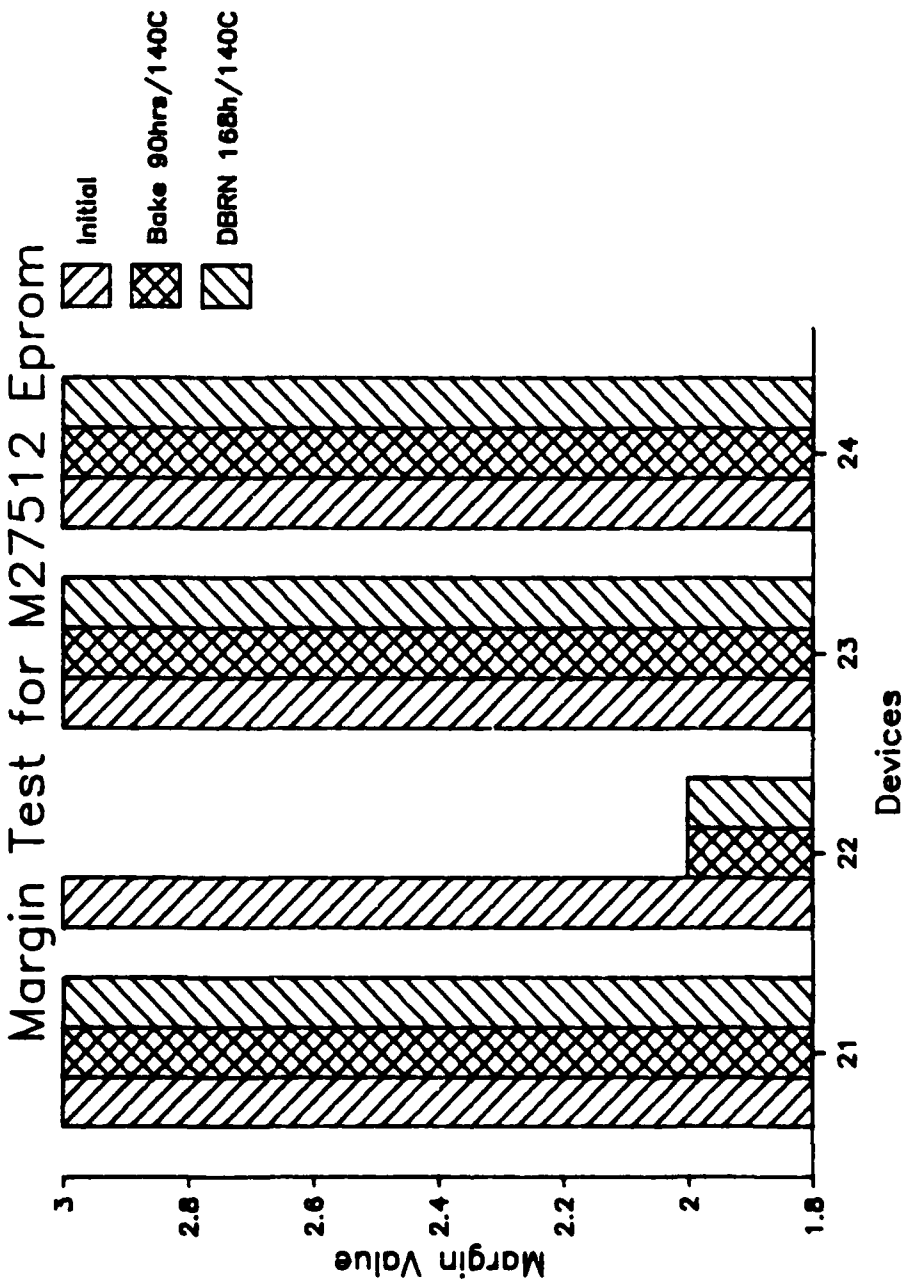


Figure 33: Floating Gate Margin Test Device#'s 21 thru 24

11. CONCLUSIONS

As a result of the device characterization, the following conclusions can be made:

- o The worst case supply current occurs at -55°C.
- o IIH and IIL measurements yielded extremely low current of 400nA or less over the full temperature range.
- o VOL and VOH measurements were within the proposed slash sheet limits.
- o Addresses, -CE and -OE/VPP thresholds increase with VCC. Changes in temperature had little effect on the threshold levels.
- o In all cases, the measured input and output capacitance values were below the specified limits.
- o This device can be rated in ESD category "B" (>2000 volts).
- o Worst case conditions for A.C. parameters were high temperature (125°C) and low voltage (4.5 volts).
- o In all cases, the margins on the floating gates of the devices were above the 0.5 volt limit as specified for HMOS-IIE in the proposed slash sheet.
- o To increase device integrity, the use of multiple data patterns during A.C. parametric measurements is recommended.
- o As part of a future comprehensive characterization effort, it is recommended that an in-depth study be done on the effects of floating gate margin on data retention.

TABLE OF CONTENTS

64K EEPROM

LIST OF FIGURES

LIST OF TABLES

1. SUMMARY

1.1 OBJECTIVES/RESULTS

The objective of this portion of the contract with Rome Air Development Center was to perform and present the results of a detailed electrical characterization of a 64K (8K X 8) NMOS EEPROM. This characterization was the basis for the development of a preliminary MIL-M-38510 slash sheet.

This report documents the test procedures and test results of the electrical characterization of the "X2864ADM-45" EEPROM offered by Xicor, Inc. Full A.C. and D.C. electrical testing was performed at +25°C and the extremes of the military temperature range (-55°C and +125°C). DATA polling, a method to decrease write cycle time, was extensively investigated and two timing constraints, not specified in the vendor's datasheet, were discovered.

In summary, the device performed as expected, per the proposed slash sheet with the exception of propagation delays, which were noticeably shorter.

Details and test data documenting the above findings are presented and summarized in this report and the slash sheet. This document contains composite SHMOO plots for 36 devices at the 3 test temperatures.

A summary sheet, generated by the host computer for the 5588, displays the average, standard deviation, and 95% limits for every measured A.C. and DC parameter. A summary sheet is presented for each test temperature (see Tables 1, 2, and 3). The 95% limits are the average plus twice the standard deviation, and the average minus twice the standard deviation. They are not the limits in the slash sheet, but the 95% limits are presented here as a statistical aid in displaying and understanding the data. A datalog and SHMOO plots for one device are included as an example of the data collected on every device.

1.2 TERMS AND DEFINITIONS

The following terms are used in Tables 1, 2, and 3.

ADACC1.....Address access time, VCC=4.5V
ADACC2.....Address access time, VCC=5.5V
CSACC1.....Chip Enable access time, VCC=4.5V
CSACC2.....Chip Enable access time, VCC=5.5V.
HZACC1.....Output disable time from Chip Enable, VCC=4.5V.
HZACC2.....Output disable time from Chip Enable, VCC=5.5V.
ICC.....Active supply current.
IIH.....High level input leakage current.
IIL.....Low level input leakage current.
IOZH.....Output leakage current, high level voltage applied.
IOZL.....Output leakage current, low level voltage applied.
ISB.....Standby supply current.
LZACC1.....Output active from Chip Enable, VCC=4.5V.
LZACC2.....Output active from Chip Enable, VCC=5.5V.
OHACC1.....Output hold from address change, VCC=4.5V.
OHACC2.....Output hold from address change VCC=5.5V.
TAVWL1.....Address set-up time, VCC=4.5V.
TAVWL2.....Address set-up time, VCC=5.5V
TCLWH1.....Minimum write pulse width (-CE low to -WE high), VCC=4.5V.
TCLWH2.....Minimum write pulse width (-CE low to -WE high), VCC=5.5V.
TDVWH1.....Data set-up time, VCC=4.5V
TDVWH2.....Data set-up time, VCC=5.5V.
TOHQZ1.....Output disable time from Output Enable, VCC=4.5V.
TOHQZ2.....Output disable time from Output Enable, VCC=5.5V.
TOHWL1.....Output Enable set-up time, VCC=4.5V.
TOHWL2.....Output Enable set-up time, VCC=5.5V.
TOLQV1.....Output Enable access time, VCC=4.5V.
TOLQV2.....Output Enable access time, VCC=5.5V.
TOLQX1.....Output active from Output Enable, VCC=4.5V.
TOLQX2.....Output active from Output Enable, VCC=5.5V.
TQVWL1.....DATA polling finished to the next write cycle, VCC=4.5V.
TQVWL2.....DATA polling finished to the next write cycle, VCC=5.5V.
TWHDX1.....Data hold time, VCC=4.5V.
TWHDX2.....Data hold time, VCC=5.5V.
TWHOL1.....Output Enable hold time, VCC=4.5V.
TWHOL2.....Output Enable hold time, VCC=5.5V.
TWHQC1.....Write Enable high to DATA polling start, VCC=4.5V.
TWHQC2.....Write Enable high to DATA polling start, VCC=5.5V.
TWLAX1.....Address hold time, VCC=4.5V.
TWLAX2.....Address hold time, VCC=5.5V.
TWLCH1.....Minimum write pulse width (-WE low to -CE high), VCC=4.5V.
TWLCH2.....Minimum write pulse width (-WE low to -CE high), VCC=5.5V.

TWLWH.....Minimum Write Enable pulse width, VCC=4.5V.
TWLWL.....Minimum write cycle time, VCC=4.5V.
VCCACC.....VCC sense voltage.
VOH.....High level output voltage.
VOL.....Low level output voltage.

TABLE 1
DEVICE PERFORMANCE SUMMARY AT 25°C

PART NUMBER: X2864A BATCH:
DEVICE TYPE: 8KX8EEPROM STAGE:
TEST PROGRAM: M2864MAIN.TP GROUP: SUM2864
ADAPTER NO.: X2864A

Xicor, X2864A-45, Temp. = 25°C.

TEST SUMMARY
==========

ACCUM	COUNT	AVERAGE	STD DEV	95% LIMITS
ADACC1	36	182.6NS	5.8NS	171.1 to 194.2
ADACC2	36	174.9NS	10.9NS	153.1 to 196.8
CSACC1	36	190.4NS	5.6NS	179.3 to 201.6
CSACC2	36	184.0NS	7.4NS	169.2 to 198.8
HZACC1	36	40.6NS	2.4NS	35.8 to 45.4
HZACC2	36	48.1NS	2.8NS	42.5 to 53.6
ICC	36	67.1MA	6.0MA	55.2 to 79.1
IIH	576	0.05UA	0.13UA	-0.21 to 0.30
IIL	576	0.00UA	0.05UA	-0.11 to 0.11
IOZH	288	0.04UA	0.06UA	-0.09 to 0.17
IOZL	288	0.00UA	0.04UA	-0.07 to 0.07
ISB	36	33.3MA	2.7MA	27.9 to 38.7
LZACC1	36	53.6NS	3.3NS	47.0 to 60.2
LZACC2	36	44.8NS	2.8NS	39.2 to 50.5
OHACC1	36	41.8NS	7.9NS	26.0 to 57.7
OHACC2	36	37.4NS	2.7NS	32.0 to 42.8
TAVWL1	36	-68.5NS	7.0NS	-54.5 to -82.5
TAVWL2	36	-95.0NS	10.8NS	-73.3 to -116.7
TCLWH1	36	43.4NS	4.5NS	34.4 to 52.3
TCLWH2	36	61.4NS	7.3NS	46.8 to 75.9
TDVWH1	36	28.6NS	2.1NS	24.3 to 32.8
TDVWH2	36	28.5NS	3.4NS	21.8 to 35.3
TOHQZ1	36	33.3NS	1.7NS	30.0 to 36.7
TOHQZ2	36	39.3NS	2.2NS	34.9 to 43.7
TOHWL1	36	-92.5NS	11.4NS	-69.7 to -115.3
TOHWL2	36	-140.5NS	19.4NS	-101.7 to -179.3
TOLQV1	36	39.4NS	2.1NS	35.2 to 43.5
TOLQV2	36	36.4NS	2.1NS	32.2 to 40.7
TOLQX1	36	28.2NS	1.6NS	25.0 to 31.3
TOLQX2	36	29.5NS	1.6NS	26.2 to 32.8

TABLE 1 (continued)
DEVICE PERFORMANCE SUMMARY AT 25°C

Xicor, X2864A-45, Temp. = 25°C.

TEST SUMMARY

ACCUM	COUNT	AVERAGE	STD DEV	95% LIMITS
TQVWL1	36	0.170MS	0.090MS	0.0 to 0.34
TQVWL2	36	0.030MS	0.000MS	0.030 to 0.030
TWHDX1	36	-8.9NS	5.3NS	1.7 to -19.4
TWHDX2	36	2.5NS	1.3NS	-0.2 to 5.1
TWHOL1	36	-153.6NS	4.9NS	-143.9 to -163.4
TWHOL2	36	-134.8NS	7.8NS	-119.2 to -150.5
TWHQC1	36	93.0NS	4.6NS	83.9 to 102.1
TWHQC2	36	94.9NS	3.9NS	87.1 to 102.7
TWLAX1	36	77.9NS	7.5NS	62.9 to 92.9
TWLAX2	36	104.2NS	11.3NS	81.6 to 126.8
TWLCH1	36	29.7NS	3.3NS	23.0 to 36.4
TWLCH2	36	45.5NS	6.1NS	33.3 to 57.6
TWLWH	36	48.2NS	5.2NS	37.9 to 58.6
TWLWL	36	2.78MS	0.58MS	1.62 to 3.95
VCCACC	36	3.21 V	0.08 V	3.05 to 3.37
VOH	288	2.99 V	0.04 V	2.91 to 3.07
VOL	288	0.137 V	0.005 V	0.126 to 0.148

TABLE 2
DEVICE PERFORMANCE SUMMARY AT 125°C

PART NUMBER: X2864A BATCH:
DEVICE TYPE: 8KX8EEPROM STAGE:
TEST PROGRAM: M2864MAIN.TP GROUP: SUM2864
ADAPTER NO.: X2864A

XICOR, X2864A-45 , TEMP. = 125°C.

TEST SUMMARY
============

ACCUM	COUNT	AVERAGE	STD DEV	95% LIMITS
ADACC1	36	253.1NS	8.2NS	236.8 to 269.5
ADACC2	36	233.3NS	8.2NS	216.8 to 249.8
CSACC1	36	257.5NS	10.0NS	237.5 to 277.5
CSACC2	36	248.0NS	10.4NS	227.1 to 268.8
HZACC1	36	52.4NS	3.3NS	45.7 to 59.1
HZACC2	36	59.4NS	4.0NS	51.4 to 67.3
ICC	36	46.5MA	4.0MA	38.4 to 54.6
IIH	576	0.05UA	0.29UA	-0.53 to 0.63
IIL	576	0.01UA	0.17UA	-0.33 to 0.35
IOZH	288	0.03UA	0.17UA	-0.30 to 0.37
IOZL	288	0.01UA	0.12UA	-0.23 to 0.24
ISB	36	24.4MA	2.2MA	20.1 to 28.7
LZACC1	36	72.7NS	4.3NS	64.1 to 81.3
LZACC2	36	61.4NS	4.2NS	53.0 to 69.7
OHACC1	36	68.5NS	2.9NS	62.7 to 74.4
OHACC2	36	63.0NS	5.9NS	51.1 to 74.8
TAVWL1	36	-98.1NS	9.4NS	-79.3 to -116.8
TAVWL2	36	-132.4NS	12.8NS	-106.8 to -158.0
TCLWH1	36	63.2NS	6.2NS	50.7 to 75.6
TCLWH2	36	87.4NS	10.0NS	67.4 to 107.5
TDVWH1	36	43.0NS	3.5NS	36.0 to 50.0
TDVWH2	36	43.2NS	4.6NS	34.1 to 52.4
TOHQZ1	36	41.1NS	2.3NS	36.4 to 45.8
TOHQZ2	36	46.7NS	3.0NS	40.7 to 52.8
TOHWL1	36	-136.9NS	16.0NS	-104.8 to -169.0
TOHWL2	36	-198.2NS	20.6NS	-157.1 to -239.3
TOLQV1	36	53.3NS	2.7NS	47.9 to 58.7
TOLQV2	36	48.9NS	2.8NS	43.2 to 54.6
TOLQX1	36	38.4NS	1.9NS	34.5 to 42.3
TOLQX2	36	39.6NS	2.4NS	34.9 to 44.4

TABLE 2 (continued)
DEVICE PERFORMANCE SUMMARY AT 125°C

XICOR, X2864A-45 , TEMP. = 125°C.

TEST SUMMARY

ACCUM	COUNT	AVERAGE	STD DEV	95% LIMITS
TQVWL1	36	0.03MS	0.000MS	0.03 to 0.03
TQVWL2	36	0.03MS	0.000MS	0.03 to 0.03
TWHDX1	36	-15.2NS	5.0NS	-5.3 to -25.1
TWHDX2	36	-4.3NS	2.2NS	0.1 to -8.8
TWHOL1	36	-132.7NS	6.8NS	-119.2 to -146.3
TWHOL2	36	-107.2NS	10.6NS	-85.9 to -128.4
TWHQC1	36	116.9NS	6.0NS	105.0 to 128.9
TWHQC2	36	113.0NS	2.2NS	108.6 to 117.5
TWLAX1	36	112.9NS	10.5NS	92.0 to 133.9
TWLAX2	36	148.0NS	15.5NS	117.0 to 179.1
TWLCH1	36	43.3NS	4.9NS	33.4 to 53.1
TWLCH2	36	65.2NS	8.5NS	48.2 to 82.2
TWLWH	36	69.6NS	7.5NS	54.6 to 84.6
TWLWL	36	3.49MS	0.41MS	3.12 to 4.76
VCCACC	36	3.09 V	0.09 V	2.92 to 3.26
VOH	288	2.99 V	0.04 V	2.91 to 3.07
VOL	288	0.192 V	0.009 V	0.175 to 0.210

TABLE 3
DEVICE PERFORMANCE SUMMARY AT -55°C

PART NUMBER: X2864A BATCH:
DEVICE TYPE: 8KX8EEPROM STAGE:
TEST PROGRAM: M2864MAIN.TP GROUP: SUM2864
ADAPTER NO.: X2864A

XICOR, X2864A-45, TEMP. = -55°C

TEST SUMMARY
============

ACCUM	COUNT	AVERAGE	STD DEV	95% LIMITS
ADACC1	36	143.6NS	3.6NS	136.4 to 150.9
ADACC2	36	135.9NS	5.0NS	125.9 to 146.0
CSACC1	36	149.7NS	4.5NS	140.6 to 158.7
CSACC2	36	143.8NS	5.6NS	132.7 to 155.0
HZACC1	36	35.1NS	2.3NS	30.5 to 39.7
HZACC2	36	39.6NS	2.5NS	34.7 to 44.5
ICC	36	76.5MA	6.0MA	64.6 to 88.5
IIH	576	0.04UA	1.72UA	-3.39 to 3.47
IIL	576	-0.20UA	1.48UA	-3.17 to 2.77
IOZH	288	0.13UA	0.63UA	-1.14 to 1.39
IOZL	288	-0.00UA	0.04UA	-0.08 to 0.07
ISB	36	40.9MA	3.3MA	34.4 to 47.4
LZACC1	36	39.5NS	12.6NS	14.4 to 64.6
LZACC2	36	34.2NS	10.5NS	13.2 to 55.2
OHACC1	36	28.9NS	2.1NS	24.7 to 33.2
OHACC2	36	28.4NS	1.9NS	24.6 to 32.2
TAVWL1	36	-49.8NS	5.5NS	-38.7 to -60.8
TAVWL2	36	-70.2NS	8.6NS	-53.0 to -87.5
TCLWH1	36	32.0NS	3.4NS	25.1 to 38.8
TCLWH2	36	45.7NS	5.6NS	34.6 to 56.9
TDVWH1	36	18.7NS	1.6NS	15.5 to 22.0
TDVWH2	36	19.2NS	2.1NS	14.9 to 23.4
TOHQZ1	36	31.4NS	1.9NS	27.6 to 35.2
TOHQZ2	36	32.4NS	1.8NS	28.9 to 36.0
TOHWL1	36	-67.7NS	8.5NS	-50.6 to -84.8
TOHWL2	36	-103.6NS	14.8NS	-74.0 to -133.3
TOLQV1	36	31.2NS	1.8NS	27.7 to 34.8
TOLQV2	36	29.0NS	2.2NS	24.6 to 33.4
TOLQX1	36	21.2NS	6.4NS	8.5 to 34.0
TOLQX2	36	21.7NS	7.8NS	6.2 to 37.2

TABLE 3 (continued)
DEVICE PERFORMANCE SUMMARY AT -55°C

XICOR, X2864A-45, TEMP. = -55°C

TEST SUMMARY

ACCUM	COUNT	AVERAGE	STD DEV	95% LIMITS
TQVWL1	36	0.29MS	0.07MS	0.15 to 0.43
TQVWL2	36	0.03MS	0.000MS	0.03 to 0.03
TWHDX1	36	-3.1NS	4.1NS	5.1 to -11.4
TWHDX2	36	1.4NS	0.8NS	-0.3 to 3.0
TWHOL1	36	-159.3NS	4.7NS	-149.9 to -168.7
TWHOL2	36	-151.3NS	6.0NS	-139.4 to -163.2
TWHQC1	36	83.9NS	0.6NS	82.6 to 85.1
TWHQC2	36	82.6NS	1.4NS	79.7 to 85.5
TWLAX1	36	57.8NS	5.7NS	46.5 to 69.1
TWLAX2	36	77.6NS	8.7NS	60.2 to 95.0
TWLCH1	36	22.2NS	2.7NS	16.7 to 27.6
TWLCH2	36	34.0NS	4.5NS	25.0 to 43.1
TWLWH	36	36.8NS	4.1NS	28.6 to 44.9
TWLWL	36	2.31MS	0.42MS	1.46 to 3.15
VCCACC	36	3.30 V	0.09 V	3.12 to 3.48
VOH	288	3.00 V	0.04 V	2.92 to 3.08
VOL	288	0.107 V	0.005 V	0.096 to 0.117

```
        DATALOG I                                                    XINCOM

PART NUMBER:    X2864A              BATCH:                  LOG DATE:   06/03/86
DEVICE TYPE:    8KX8EEPROM          STAGE:                  LOG TIME:   08:54:18
TEST PROGRAM:   M2864MAIN.TP        GROUP:   DATA2864       PRT DATE:   06/03/86
ADAPTER NO.:    X2864A              HEAD:    13             PRT TIME:   16:28:40
**********************************************************************************
COMNT    XICOR, TEMP=25C
DSN      DEVICE SERIAL NO.      1
COMNT       INPUT LEAKAGE CURRENT, VIN = 5.5V
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 10
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 09
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 08
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 07
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 06
PARM(P) IIHPM  =    0.03UA     MAX =   10.00UA     MIN = -10.00UA     PIN 05
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 04
PARM(P) IIHPM  =    0.03UA     MAX =   10.00UA     MIN = -10.00UA     PIN 03
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 25
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 24
PARM(P) IIHPM  =    0.03UA     MAX =   10.00UA     MIN = -10.00UA     PIN 21
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 23
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 02
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 22
PARM(P) IIHPM  =    0.61UA     MAX =   10.00UA     MIN = -10.00UA     PIN 20
PARM(P) IIHPM  =    0.04UA     MAX =   10.00UA     MIN = -10.00UA     PIN 27
COMNT       INPUT LEAKAGE CURRENT, VIN = 0V
PARM(P) IILPM  =    0.00UA     MAX =   10.00UA     MIN = -10.00UA     PIN 10
PARM(P) IILPM  =    0.00UA     MAX =   10.00UA     MIN = -10.00UA     PIN 09
PARM(P) IILPM  =    0.00UA     MAX =   10.00UA     MIN = -10.00UA     PIN 08
PARM(P) IILPM  =    0.00UA     MAX =   10.00UA     MIN = -10.00UA     PIN 07
PARM(P) IILPM  =    0.00UA     MAX =   10.00UA     MIN = -10.00UA     PIN 06
PARM(P) IILPM  =   -0.01UA     MAX =   10.00UA     MIN = -10.00UA     PIN 05
PARM(P) IILPM  =   -0.01UA     MAX =   10.00UA     MIN = -10.00UA     PIN 04
PARM(P) IILPM  =    0.00UA     MAX =   10.00UA     MIN = -10.00UA     PIN 03
PARM(P) IILPM  =    0.00UA     MAX =   10.00UA     MIN = -10.00UA     PIN 25
PARM(P) IILPM  =    0.00UA     MAX =   10.00UA     MIN = -10.00UA     PIN 24
PARM(P) IILPM  =    0.00UA     MAX =   10.00UA     MIN = -10.00UA     PIN 21
PARM(P) IILPM  =    0.00UA     MAX =   10.00UA     MIN = -10.00UA     PIN 23
PARM(P) IILPM  =   -0.01UA     MAX =   10.00UA     MIN = -10.00UA     PIN 02
PARM(P) IILPM  =    0.00UA     MAX =   10.00UA     MIN = -10.00UA     PIN 22
PARM(P) IILPM  =    0.03UA     MAX =   10.00UA     MIN = -10.00UA     PIN 20
PARM(P) IILPM  =   -0.01UA     MAX =   10.00UA     MIN = -10.00UA     PIN 27
COMNT                  OUTPUT HIGH VOLTAGE
PARM(P) VOHPM  =    2.95 V     MAX =    5.00 V     MIN =    2.40 V     PIN 11
PARM(P) VOHPM  =    2.95 V     MAX =    5.00 V     MIN =    2.40 V     PIN 12
PARM(P) VOHPM  =    2.95 V     MAX =    5.00 V     MIN =    2.40 V     PIN 13
PARM(P) VOHPM  =    2.93 V     MAX =    5.00 V     MIN =    2.40 V     PIN 15
PARM(P) VOHPM  =    2.96 V     MAX =    5.00 V     MIN =    2.40 V     PIN 16
PARM(P) VOHPM  =    2.95 V     MAX =    5.00 V     MIN =    2.40 V     PIN 17
PARM(P) VOHPM  =    2.95 V     MAX =    5.00 V     MIN =    2.40 V     PIN 18
PARM(P) VOHPM  =    2.94 V     MAX =    5.00 V     MIN =    2.40 V     PIN 19
```

Figure 1: Sample Datalog, Device #1 at 25°C

```
COMNT                OUTPUT LOW VOLTAGE
PARM(P) VOLPM  =  0.133 V     MAX =  0.400 V     MIN =  0.000 V     PIN 11
PARM(P) VOLPM  =  0.135 V     MAX =  0.400 V     MIN =  0.000 V     PIN 12
PARM(P) VOLPM  =  0.135 V     MAX =  0.400 V     MIN =  0.000 V     PIN 13
PARM(P) VOLPM  =  0.140 V     MAX =  0.400 V     MIN =  0.000 V     PIN 15
PARM(P) VOLPM  =  0.137 V     MAX =  0.400 V     MIN =  0.000 V     PIN 16
PARM(P) VOLPM  =  0.136 V     MAX =  0.400 V     MIN =  0.000 V     PIN 17
PARM(P) VOLPM  =  0.136 V     MAX =  0.400 V     MIN =  0.000 V     PIN 18
PARM(P) VOLPM  =  0.137 V     MAX =  0.400 V     MIN =  0.000 V     PIN 19
COMNT       OUTPUT LEAKAGE CURRENT, VOUT = 5.5V
PARM(P) IOZHPM =   0.04UA     MAX =  10.00UA     MIN = -10.00UA     PIN 11
PARM(P) IOZHPM =   0.04UA     MAX =  10.00UA     MIN = -10.00UA     PIN 12
PARM(P) IOZHPM =   0.03UA     MAX =  10.00UA     MIN = -10.00UA     PIN 13
PARM(P) IOZHPM =   0.04UA     MAX =  10.00UA     MIN = -10.00UA     PIN 15
PARM(P) IOZHPM =   0.04UA     MAX =  10.00UA     MIN = -10.00UA     PIN 16
PARM(P) IOZHPM =   0.03UA     MAX =  10.00UA     MIN = -10.00UA     PIN 17
PARM(P) IOZHPM =   0.03UA     MAX =  10.00UA     MIN = -10.00UA     PIN 18
PARM(P) IOZHPM =   0.04UA     MAX =  10.00UA     MIN = -10.00UA     PIN 19
COMNT       OUTPUT LEAKAGE CURRENT, VOUT = 0V
PARM(P) IOZLPM =  -0.01UA     MAX =  10.00UA     MIN = -10.00UA     PIN 11
PARM(P) IOZLPM =   0.00UA     MAX =  10.00UA     MIN = -10.00UA     PIN 12
PARM(P) IOZLPM =   0.00UA     MAX =  10.00UA     MIN = -10.00UA     PIN 13
PARM(P) IOZLPM =   0.00UA     MAX =  10.00UA     MIN = -10.00UA     PIN 15
PARM(P) IOZLPM =   0.00UA     MAX =  10.00UA     MIN = -10.00UA     PIN 16
PARM(P) IOZLPM =   0.00UA     MAX =  10.00UA     MIN = -10.00UA     PIN 17
PARM(P) IOZLPM =   0.00UA     MAX =  10.00UA     MIN = -10.00UA     PIN 18
PARM(P) IOZLPM =   0.00UA     MAX =  10.00UA     MIN = -10.00UA     PIN 19
COMNT    STANDBY POWER SUPPLY CURRENT, VIH=2.0V, VIL=0.8V
PARM(P) ISBPM  =   31.1MA     MAX =   70.0MA     MIN =   -1.0MA     PIN 28
COMNT    OPERATING POWER SUPPLY CURRENT,CE AND OE = .8V
PARM(P) ICCPM  =   59.1MA     MAX =  140.0MA     MIN =   -1.0MA     PIN 28
```

Figure 1: Sample Datalog, Device #1 at 25°C (continued)

```
************************  VCC SENSE  ***********************************
AT VCC=    3.18V  A WRITE CYCLE OCCURRED

*****************  DATA POLLING AC PARAMETERS  ************************
  PARAMETER                                    !  VCC=4.5V  ! VCC=5.5V  !
***********************************************!************!************!
TIME FROM DATA POLL FINISHED TO NEXT WRITE !    0.240MS  !    30.0US  !
TIME FROM WRITE HIGH TO START OF DATA POLL !     96.3NS  !    97.5NS  !
***********************************************!************!************!

*****************  MINIMUM WRITE PULSE WIDTH TEST  ********************
AT TWP=    52.5NS A WRITE CYCLE OCCURRED

********************  FUNCTIONAL TEST  ***********************************
        XXXXXXXXXX     VCC = 4.5V     XXXXXXXXXX
WRITE/READ ALL 0'S AND ALL 1'S
GALLOPING PATTERN. READ ALL 0'S
CHECKERBOARD PATTERN (TRUE AND COMPLEMENT DATA)
WIRTE/READ COLUMNS WITH ALTERNATING DATA
READ WORAD ACROSS DIAGONALS.
BIT UNIQUE TEST PATTERN
WRITE/READ ALL 1'S
GALLOPING PATTERN. READ ALL 1'S
MARCH PATTERN. BYTE WRITE.
        XXXXXXXXXX     VCC = 5.5V     XXXXXXXXXX
WRITE/READ ALL 0'S AND ALL 1'S
GALLOPING PATTERN. READ ALL 0'S
CHECKERBOARD PATTERN (TRUE AND COMPLEMENT DATA)
WIRTE/READ COLUMNS WITH ALTERNATING DATA
READ WORAD ACROSS DIAGONALS.
BIT UNIQUE TEST PATTERN
WRITE/READ ALL 1'S
GALLOPING PATTERN. READ ALL 1'S
MARCH PATTERN. BYTE WRITE.
```

Figure 1: Sample Datalog, Device #1 at 25°C (continued)

```
********** READ CYCLE MEASUREMENTS **********
  PARAMETER              !VCC=4.5V  ! VCC=5.5V  ! MIN  !  MAX  !      !
************************!**********!***********!******!******!******!
ADDRESS ACCESS TIME      !  178.8NS !   173.8NS !       !450NS !PASS  !
CHIP SELECT ACCESS TIME  !  183.8NS !   180.0NS !       !450NS !PASS  !
OUTPUT ENAB ACCESS TIME  !   40.0NS !    37.5NS !       !150NS !PASS  !
ADDRESS HOLD TIME        !   37.5NS !    37.5NS ! 20NS  !       !PASS  !
DATA FLOAT TIME FROM CE  !   41.3NS !    50.0NS ! 10NS  ! 100NS!PASS  !
DATA FLOAT TIME FROM OE  !   33.8NS !    41.3NS ! 10NS  ! 100NS!PASS  !
CS TO OUTPUT IN LOW Z    !   57.5NS !    47.5NS ! 10NS  !       !PASS  !
OE TO OUTPUT IN LOW Z    !   28.8NS !    30.0NS ! 10NS  !       !PASS  !
************************!**********!***********!******!******!******!

********** BYTE WRITE CYCLE MEASUREMENTS **********
  PARAMETER              !  VCC=4.5V  ! VCC=5.5V  ! MIN  !  MAX  !      !
************************!************!***********!******!******!******!
DATA SET-UP TIME         !     27.5NS !    27.5NS ! 100NS!       !PASS  !
DATA HOLD TIME           !  -   8.8NS ! +   1.3NS ! 20NS  !       !PASS  !
ADDRESS SET-UP TIME      !  -  75.0NS ! - 103.8NS ! 10NS  !       !PASS  !
ADDRESS HOLD TIME        !     83.8NS !   113.8NS ! 200NS!       !PASS  !
OE SET_UP TIME TO W      !  - 100.0NS ! - 155.0NS ! 10NS  !       !PASS  !
OE HOLD TIME FROM W      !  - 150.0NS ! - 128.8NS ! 10NS  !       !PASS  !
W LOW TO CE HIGH (TWP)!     46.3NS !    67.5NS ! 20NS  ! 210NS!PASS  !
CE LOW TO W HIGH (TWP)!     32.5NS !    50.0NS ! 20NS  ! 210NS!PASS  !
************************!************!***********!******!******!******!

********** DATA RETENTION, VCC=0V FOR 30 SECONDS **********
DUT PASSED DATA RETENTION.
********** WRITE CYCLE TIME, VCC=4.5V **********
   TWC=   3.50MS
******** VERIFY TWPH, TBLC, AND TPLW OF PAGE MODE WRITE CYCLE ********
CHECKERBOARD PATTERN (TRUE AND COMPLEMENT DATA)
        XXXXXXXXXXX     VCC = 4.5V     XXXXXXXXXXX
AC PARAMETERS WERE VERIFIED
        XXXXXXXXXXX     VCC = 5.5V     XXXXXXXXXXX
AC PARAMETERS WERE VERIFIED
********** CHIP MASS ERASE TEST **********
     XXXXXXXXXXXXXX      VCC=4.5V     XXXXXXXXXXXXXXXXXXXX
*** DEVICE COULD NOT BE INITIAZLIED ***
```

Figure 1: Sample Datalog, Device #1 at 25°C (continued)

```
        TWO AXIS SHMOO PLOT                                        XINCOM

PART NUMBER:    X2864A              BATCH:                  LOG DATE:   07/01/86
DEVICE TYPE:    8KX8EEPROM          STAGE:                  LOG TIME:   09:01:58
TEST PROGRAM:   M2864MAIN.TP        GROUP:   SM2864         PRT DATE:   07/01/86
ADAPTER NO.:    X2864A              HEAD:    13             PRT TIME:   09:28:53
**************************************************************************
                              TEST CONDITIONS

COMNT   X2864AM-45 CHARACTERIZATION TESTING
COMNT   XICOR, TEMP =  25C
COMNT   DEVICE SERIAL NO.  1
COMNT   2 AXIS SHMOO: VCC VS. ADDRESS ACCESS TIME USING RDRAD PATTERN
COMNT    'X' INDICATES A PASS
COMNT   VIL=0V, VIH=3V, VOL=1.5V, VOH=1.5V
**************************************************************************

SHVCC ( V)

  4.00   .    .    .    .    .    .XXXXXXXXXXXXXXX
  4.10   .    .    .    .    .    XXXXXXXXXXXXXXXX
  4.20   .    .    .    .    .   XXXXXXXXXXXXXXXXX
  4.30   .    .    .    .    . XXXXXXXXXXXXXXXXXX
  4.40   .    .    .    .    .XXXXXXXXXXXXXXXXXXX
  4.50   .    .    .    .    .XXXXXXXXXXXXXXXXXXX
  4.60   .    .    .    .   XXXXXXXXXXXXXXXXXXXX
  4.70   .    .    .    .   XXXXXXXXXXXXXXXXXXXX
  4.80   .    .    .    .  X XXXXXXXXXXXXXXXXXXX
  4.90   .    .    .    .    XXXXXXXXXXXXXXXXXXX
  5.00   .    .    .    .    XXXXXXXXXXXXXXXXXXX
  5.10   .    .    .    .   XXXXXXXXXXXXXXXXXXX
  5.20   .    .    .    .  XXXXXXXXXXXXXXXXXXXX
  5.30   .    .    .    .  XXXXXXXXXXXXXXXXXXXX
  5.40   .    .    .    .  XXXXXXXXXXXXXXXXXXXX
  5.50   .    .    .    .   XXXXXXXXXXXXXXXXXXX
  5.60   .    .    .    .   XXXXXXXXXXXXXXXXXXX
  5.70   .    .    .    .   XXXXXXXXXXXXXXXXXXX
  5.80   .    .    .    .  XXXXXXXXXXXXXXXXXXXX
  5.90   .    .    .    .   XXXXXXXXXXXXXXXXXXX
  6.00   .    .    .    .   XXXXXXXXXXXXXXXXXXX
         ^.........^.........^.........^.........^
       125.0     150.0     175.0     200.0     225.0
                          ADACC (NS)
```

Figure 2: SHMOO Plot, Device #1 at 25°C

```
        TWO AXIS SHMOO PLOT                                        XINCOM

PART NUMBER:    X2864A              BATCH:                 LOG DATE:   06/09/86
DEVICE TYPE:    8KX8EEPROM          STAGE:                 LOG TIME:   09:40:26
TEST PROGRAM:   M2864MAIN.TP        GROUP:   SM2864        PRT DATE:   06/11/86
ADAPTER NO.:    X2864A              HEAD:    13            PRT TIME:   09:27:40
**************************************************************************
                              TEST CONDITIONS

COMNT    X2864AM-45 CHARACTERIZATION TESTING
COMNT    XICOR, TEMP = 125C
COMNT    DEVICE SERIAL NO.  1
COMNT    2 AXIS SHMOO: VCC VS. ADDRESS ACCESS TIME USING RDRAD PATTERN
COMNT     'X' INDICATES A PASS
COMNT    VIL=0V, VIH=3V, VOL=1.5V, VOH=1.5V
**************************************************************************

SMVCC ( V)

  4.00   .    .    .    .     .XXXXXXXXXXXXXXXXXXX
  4.10   .    .    .    .    XXXXXXXXXXXXXXXXXXXX
  4.20   .    .    .    .  XXXXXXXXXXXXXXXXXXXXXX
  4.30   .    .    .    .  XXXXXXXXXXXXXXXXXXXXXX
  4.40   .    .    .    .  XXXXXXXXXXXXXXXXXXXXXX
  4.50   .    .    .    .  XXXXXXXXXXXXXXXXXXXXXX
  4.60   .    .    .   .XXXXXXXXXXXXXXXXXXXXXXXX
  4.70   .    .    .   XXXXXXXXXXXXXXXXXXXXXXXX
  4.80   .    .    .  XXXXXXXXXXXXXXXXXXXXXXXXX
  4.90   .    .    .  XXXXXXXXXXXXXXXXXXXXXXXXX
  5.00   .    .    .  XXXXXXXXXXXXXXXXXXXXXXXXX
  5.10   .    .    . XXXXXXXXXXXXXXXXXXXXXXXXXX
  5.20   .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXX
  5.30   .    .    . XXXXXXXXXXXXXXXXXXXXXXXXXX
  5.40   .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXX
  5.50   .    .    . XXXXXXXXXXXXXXXXXXXXXXXXXX
  5.60   .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXX
  5.70   .    .    . XXXXXXXXXXXXXXXXXXXXXXXXX
  5.80   .    .    .XXXXXXXXXXXXXXXXXXXXXXXXX
  5.90   .    .    XXXXXXXXXXXXXXXXXXXXXXXXX
  6.00   .    .    .XXXXXXXXXXXXXXXXXXXXXXXXX
         ^.........^.........^.........^.........^
       210.0     235.0     260.0     285.0     310.0
                          ADACC (NS)
```

Figure 3: SHMOO Plot, Device #1 at 125°C

```
        TWO AXIS SHMOO PLOT                                        XINCOM

PART NUMBER:    X2864A            BATCH:                  LOG DATE:   06/14/86
DEVICE TYPE:    8KX8EEPROM        STAGE:                  LOG TIME:   10:08:07
TEST PROGRAM:   42864MAIN.TP      GROUP:   SM2864         PRT DATE:   06/28/86
ADAPTER NO.:    X2864A            HEAD:    13             PRT TIME:   09:22:54
**************************************************************************
                              TEST CONDITIONS

COMNT   X2864AM-45 CHARACTERIZATION TESTING
COMNT   XICOR, TEMP = -55C
COMNT   DEVICE SERIAL NO.  1
COMNT   2 AXIS SHMOO: VCC VS. ADDRESS ACCESS TIME USING RDRAD PATTERN
COMNT    'X' INDICATES A PASS
COMNT   VIL=0V, VIH=3V, VOL=1.5V, VOH=1.5V
**************************************************************************

  VCC ( V)

  4.00   .    .    .    .     . XXXXXXXXXXXXXXXXXX
  4.10   .    .    .    .     .XXXXXXXXXXXXXXXXXX
  4.20   .    .    .    .     XXXXXXXXXXXXXXXXXXX
  4.30   .    .    .    .    XXXXXXXXXXXXXXXXXXX
  4.40   .    .    .    .   XXXXXXXXXXXXXXXXXXX
  4.50   .    .    .    .  XXXXXXXXXXXXXXXXXXX
  4.60   .    .    .    .  XXXXXXXXXXXXXXXXXXX
  4.70   .    .    .    .XXXXXXXXXXXXXXXXXXX
  4.80   .    .    .    .XXXXXXXXXXXXXXXXXXX
  4.90   .    .    .    .XXXXXXXXXXXXXXXXXXX
  5.00   .    .    .    .XXXXXXXXXXXXXXXXXXX
  5.10   .    .    .    .XXXXXXXXXXXXXXXXXXX
  5.20   .    .    .    XXXXXXXXXXXXXXXXXXX
  5.30   .    .    .    .XXXXXXXXXXXXXXXXXXX
  5.40   .    .    .    .XXXXXXXXXXXXXXXXXXX
  5.50   .    .    .    XXXXXXXXXXXXXXXXXXX
  5.60   .    .    .    XXXXXXXXXXXXXXXXXXX
  5.70   .    .    .    XXXXXXXXXXXXXXXXXXX
  5.80   .    .    .    XXXXXXXXXXXXXXXXXXX
  5.90   .    .    .    XXXXXXXXXXXXXXXXXXX
  6.00   .    .    .    XXXXXXXXXXXXXXXXXXX
         ^.........^.........^.........^.........^
       100.0      125.0      150.0      175.0      200.0
                  ADDRESS ACCESS TIME (NS)
```

Figure 4: SHMOO Plot, Device #1 at -55°C

2. INTRODUCTION

2.1 OBJECTIVES

The major objective of this effort was to electrically characterize a 64K (8K X 8) EEPROM and develop a preliminary MIL-M-38510 slash sheet. In general, the effort involved:

- o Memory market survey to determine production status of candidate devices.
- o Selection and procurement of candidate device types for characterization.
- o Development of test procedures compatible with automatic test systems. These tests include:
  - Standard A.C. and D.C. parameters.
  - Special features of the X2864A: DATA polling, mass chip erase and program modes, VCC sense, and page write operation.
- o Determination/verification of limits and test circuits via device characterization.
- o Development of a preliminary slash sheet based on device analysis and vendor comments.

2.2 BACKGROUND

An intensive study of the commercial market resulted in the selection of Xicor's X2864ADM-45 as the EEPROM to be characterized. The device provides byte and page write modes with automatic erase before write, write glitch protection, low voltage write inhibit, and operates on a single 5 volt supply. Also, samples would be available early in the contract period. In our opinion, Xicor is currently at the leading edge of EEPROM technology. During our selection process, Xicor stated they were pursuing a full MIL approval for their fab facility and, during the contract period, the DESC audit process was initiated.

To date, no two EEPROM vendors make identical components. Seeq Technology Inc. makes an M2864 which supports some of the X2864A features, but does not have page mode or DATA polling. It also has a different mass erase mode. Since the Seeq M2864 and X2864A may not always be interchangeable in any given application, it was decided not to include Seeq in the slash sheet.

A more promising second source is Intel Corporation. During the contract period, Intel and Xicor announced a joint development agreement. Intel plans to introduce an M2864A, which will be a second source for the X2864ADM.

3. DESCRIPTION OF DEVICE TYPE

3.1 GENERAL ASPECTS OF 64K EEPROMS

The 64K EEPROM is a 5 volt only, 65,536-bit Electrically Erasable and Electrically Programmable Read Only Memory (EEPROM), organized 8K words by 8 bits. The by 8, or bytewide configuration is intended primarily for use with byte oriented microprocessor systems. The two-line (Chip Enable & Output Enable) control and JEDEC-approved, 28-pin package assures easy microprocessor interfacing and minimum design effort when upgrading, adding or choosing between nonvolatile memory alternatives.

This device has all the features of the current EEPROMs. The address and data are latched by the write signal. A self-timed operation automatically erases before writing the latched data into the memory array. The self-timed operation, which is referred to as the internal write cycle in this report, requires the bulk of the 10ms write cycle time. While the internal write cycle is in process, the EEPROM requires no input from the host system.

3.1.1 EEPROM Technology

The EEPROM uses the floating gate structure like an EPROM. Both the EEPROM and EPROM trap electrons on the floating gate via tunnelling current. Electrons will tunnel through the silicon dioxide if a high voltage (20V) is applied to the top gate of the floating gate transistor. EPROMs require an external power supply, whereas, the EEPROM has a high voltage pump on-chip. The high voltage pump generates the necessary high voltage from the VCC voltage. The high voltage write shaper, also on-chip, controls the rise time, fall time, and pulse width of the high voltage applied to the top gate during write cycles. The floating gate on EEPROMS is stripped of electrons by the high voltage generated on-chip. The value of the high voltage is proportional to the thickness of the tunnelling oxide. Thinner oxides require smaller voltages, but the thin oxide is difficult to fabricate with acceptable yields. Larger voltages are needed for thicker oxides, but more current and more time are needed to generate larger voltages. This increases the supply current and write cycle time.

Xicor's process uses thicker tunnel oxides and smaller voltages. A textured poly-silicon surface is used to enhance the electric field across the tunnel oxide. The electric field produces the tunnel current. For the same applied voltage and oxide thickness, the electric field at the tips of the bumps will be greater than the field present on a flat surface. Therefore, electrons will tunnel from the bumpy surface to the floating gate at a lower voltage. This allows Xicor to use a lower voltage and a thicker tunnel oxide.

3.2 ASPECTS OF SPECIFIC DEVICE TYPE

The XICOR X2864A EEPROM has several special features that allow faster write cycles and protection against inadvertent writes.

- o Mass chip program mode. All 8K bytes can be written to the same value in one 10ms write cycle. This is ideal for writing all 0's or 1's into every memory cell. Mass mode requires a high voltage (18V to 22V) on the Output Enable pin.

- o Page mode. Sixteen locations can be written with unique data in 10ms. When using page mode, only address lines A0 through A3 can change while address lines A4 through A12 remain constant.

- o DATA polling. Byte write and page mode write have a software controlled write completion indicator. DATA polling may be used to inform the host system (microprocessor) that the internal write cycle is complete. The host system may now perform another write cycle or a read operation. To use DATA polling, the host system must periodically read the last written address. If the internal write cycle is in progress, the X2864A, at I/O7, outputs the complement of the data present on I/O7 during the previous write cycle. The other seven I/O pins are not defined. If the internal write cycle is complete, the data at I/O7 is the data present on I/O7 during the previous write cycle. DATA polling allows the user to take advantage of the typical write cycle times as opposed to waiting 10ms for every write cycle to complete.

Write protection features include:

- o Write inhibit. A write cycle cannot be initiated if Output Enable is low, or Chip Enable is high, or Write Enable is high.

- o Noise protection. A Write Enable pulse of less than 20ns will not initiate a write cycle.

- o VCC sense. A write cycle cannot occur if VCC is less than 3V. The 3V limit is typical.

3.3 SYSTEM CONSIDERATIONS

As noted above, a write cycle cannot occur if VCC is less than 3V. However, when VCC is between 3V and 4V, other components on the card function in a degraded manner, and they can inadvertently command the EEPROM to perform an undesired write cycle. To avoid this situation, the vendor recommends additional circuitry which will hold -OE low, or hold -WE or -CE high, during power up and power down. The vendor could raise the VCC sense voltage, but this impacts applications which require a write cycle if power is lost. The supply voltage could drop below the VCC sense before the write cycle is initiated. The vendor will be offering a device in the near future with a programmable VCC sense voltage.

4. DEVELOPMENT OF AUTOMATIC AND BENCH TESTS

4.1 AUTOMATIC TEST EQUIPMENT

The test equipment used to characterize the 64K EEPROM is a Fairchild Xincom 5588 Automatic Test System. The system's main processor is a Zilog Z8000 microprocessor. This processor handles all test sequences and test processes. Included in the system is a subsystem which is called the Test Pattern Computer (TPC).

The TPC is a modular subassembly which can be loaded with a microprogram and will output data and address patterns for the main purpose of testing memory devices. Fairchild has developed many popular industry patterns; e.g., Ping Pong, Checkerboard, March. The user may microprogram other patterns. Patterns are defined by a set of 48-bit microcoded instructions executed within the TPC at functional rates up to 25MHz (40ns cycle time). Upon command from the main processor, the TPC generates the desired pattern and sends this pattern to the system for use in the stimulus of input pins and response checking of output pins.

Some additional features of the TPC are:

- o ECL Construction
- o Topological Address Scrambler
- o Address Indexing, Refresh Testing, Butterfly Patterns
- o Truth-Table RAM (Pattern RAM For EPROMS)
- o Algorithmic Pattern Generation
- o Loop Counters
- o Timing Set Selection on-the-fly

In addition to the TPC, other system capabilities include:

- o 14 programmable clock phases
- o 4 programmable power supplies
- o 24 address lines
- o 16 data comparators
- o Parametric Measurement Unit (PMU)
- o Advanced Error Logging System (AELS)
- o IEEE 488 Bus Interface
- o Color Computer Graphics Display
- o Auto Data Logging to Data General Eclipse Host Computer

To interface the device under test (DUT) to the test system, an interface board is used to electrically connect the DUT's pins to the specific test system pin electronic cards. A zero insertion force socket is used to allow for fast removal and insertions of the DUT without causing lead damage.

4.2 BENCH TEST EQUIPMENT

Bench instruments were required to perform the Electrostatic Discharge and Capacitance Measurement tests.

The Electrostatic Discharge unit used is a IMCS Corporation, Model number 2400C. This instrument uses the human body model.

Features include:

- o 0-10,000 Volt Continuously Adjustable
- o 4.5 Digital Display of HV
- o Programmable Pulse Sequence
- o Curve Tracer Output

- o 1-128 pin Configuration
- o Applicable to MIL-STD-883 and STD-1686

The Capacitance Analyzer used is a Hewlett Packard, Model number 4192A, probe model number HP-16048C.

Features include:

- o 5Hz to 13MHz variable measuring frequency
- o Gain-Phase measurement: amplitude, phase and delay
- o Floating or Grounded devices
- o Frequency accuracy +/- 50ppm

4.3 EEPROM PROGRAMMING EQUIPMENT

The 5588 was used for all device programming. The test program treated the EEPROM like a static RAM and time delays were used after each write cycle to permit the internal write cycle to complete.

Some vendors of EPROM programmers offer programming packages for EEPROMs. Such programmers would be advantageous if several devices need to be programmed with the same data since EEPROMs can be "gang" programmed. These programmers are targeted for device programming prior to card insertion which could be useful for burn-in and bit retention tests.

5. STATIC CHARACTERISTICS

5.1 OBJECTIVES

During this characterization, several goals were set forth. One of these was to reliably and efficiently characterize the D.C. parameters of the 64K EEPROM device. This was accomplished by utilizing Automatic Test Equipment (ATE). This equipment could reliably execute a group of measurements and test conditions with accuracy and repeatability.

5.2 TEST METHODS

The Xincom 5588 memory test system was used to collect data on the D.C. parametric measurements. The tester allowed data to be taken on each device in an accelerated and accurate manner. The sample size for the D.C. measurements was 36 devices. The tests performed on the Xincom were: VOH, VOL, IIH, IIL, IOZH, IOZL, ICC, and ISB. The test temperatures were $-55^{o}C$, $+25^{o}C$, and $+125^{o}C$. Note that every test was performed at each temperature and worst case voltage.

The results of the measurements were datalogged to the host computer, a Data General Eclipse minicomputer. Commands were added to the 5588 program to log data to the host and to create a summary sheet. The Data Reduction System (DREX), a software package resident on the Eclipse, stores and prints the datalog for each device and generates a summary sheet based on data gathered from all 36 devices. The test summary contains the average, standard deviation, and 95% limits for every measured parameter. A test summary was generated for every test temperature.

5.2.1 VOH, VOL TEST

This test measures the output logic "1" voltage and the output logic "0" voltage. For this test, the PMU (precision measurement unit of the 5588) forces a current and measures the resulting voltage. The forcing current for the VOH test is -400uA. The current for the VOL measurement is 2.1mA. During both measurements, VCC is 4.5V.

The device was preconditioned by performing a byte write of all 0's at the first address location and a byte write of all 1's at the last address location. During the VOH test, the last address was read and, during the VOL test, the first address was read.

The low limits and high limits versus temperature are plotted in a high-low graph in Figure 5. The high limits and low limits were obtained from the 95% limits calculated in the test summary sheets (see VOH and VOL in Tables 1, 2, and 3). Note that VOH is insensitive to temperature, while VOL increases as the temperature increases. In all cases, the measured VOH and VOL meet the limits specified in the proposed slash sheet. The small standard deviations indicate the vendor has a stable process.

5.2.2 IIH, IIL TEST

The IIH and IIL tests determine the current load an input presents to the driving output. The IIH test is conducted by driving one input high (5.5V) and measuring the current. Other inputs are tied to ground. The IIL test is conducted by driving one input low (0V) and measuring the current. Other inputs are tied to VCC. The inputs not under test are held in the opposite state to the input under test so that a leakage path between two inputs will be detected. IIH and IIL are measured with VCC at 5.5V to maximize the voltage across reverse biased junctions.

Leakage measurements were performed at -55^{o}C, +25^{o}C, and +125^{o}C. The specified limits were +/- 10uA. In general, all measurements yielded extremely low currents of 100nA or less. The upper high-low graph in Figure 6 displays the averages and low limits for IIL. The low values are from the 95% limits calculated in the test summaries (see IIL in Tables 1 and 2). The lower high-low graph in Figure 6 displays the averages and high limits for IIH. The high values are from the 95% limits in the test summaries (see IIH in Tables 1 and 2). The currents were largest at -55^{o}C due to leakage paths created by moisture on the adapter board and thermal pad. These currents were not displayed in the graphs. The 25^{o}C and 125^{o}C are realistic and indicate that IIL and IIH increase as the temperature increases. Currents of these magnitudes are typical in LSI devices using NMOS technology.

5.2.3 IOZH, IOZL TEST

This test measures the output leakage current of the I/O pins when they are in the high impedance state. The procedure for this test is to set the device's I/O pins in the high impedance state by applying 2.0V to the -CE input pin. Other input conditions are: 0.8V on -OE; 2V on -WE; 0.8V on the address lines. A voltage is applied to the I/O pin under test and the current is measured. I/O pins not under test are open.

Two forcing voltages are applied. During the IOZH test, 5.5V is applied and, during the IOZL test, 0V is applied. VCC is set to 5.5 volts which is the worst case condition.

As in the IIH and IIL test (section 5.2.2), the output leakage currents were largest at $-55^{O}C$ due to leakage paths created by moisture and they were not plotted in Figure 7. As expected, the leakage current increased as the temperature increased from $25^{O}C$ to $125^{O}C$. Figure 7 shows the averages and low values for IOZL (IOZL in Tables 1 and 2) and the averages and high values for IOZH (IOZH in Tables 1 and 2).

5.2.4 ICC, ISB TEST

This test measures the amount of supply current required by the device for two different operating modes. The first mode is device active (ICC). This mode corresponds to a read operation. The second mode is standby (ISB). During standby, the device's supply current is reduced to 50% of the active supply current.

The device is placed in the standby mode by applying a logic "1" (2.0V) to the -CE input. When in the standby mode, the outputs are in the high impedance state, independent of -OE input.

To perform the active test, -CE and -OE are at 0.8V and the other inputs are at 2.0V. The I/O pins are open and VCC is at the maximum value (5.5V). The current sourced by the VCC power supply is measured and recorded. The standby test places a logic "1" (2V) on all inputs, except -OE, which is tied to 0.8V. The I/O pins are open and VCC is at 5.5V. The resulting current is measured and recorded.

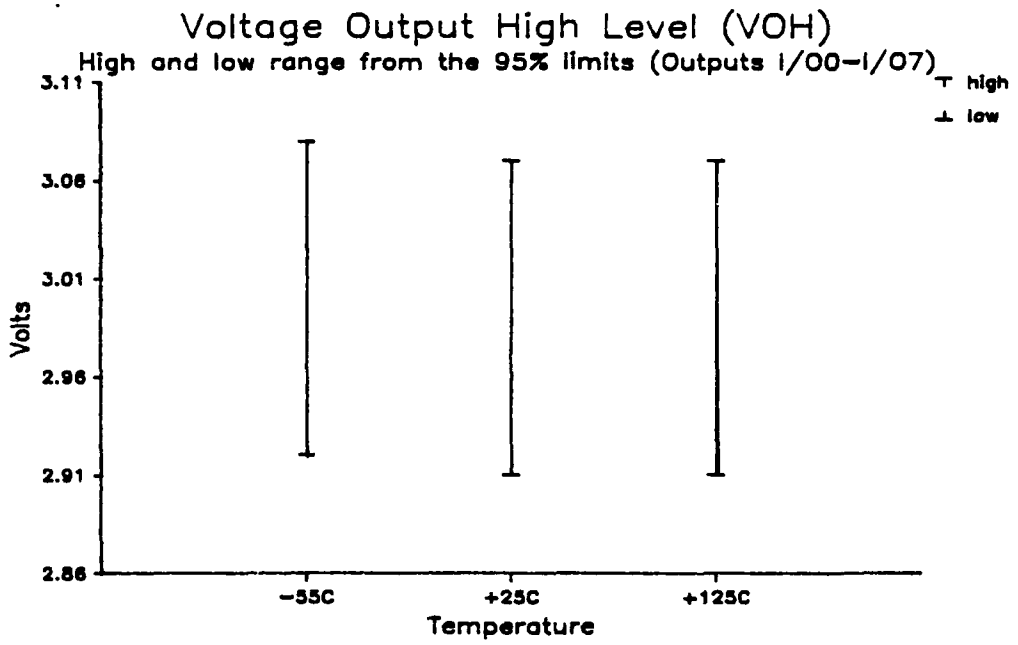
Refer to Figure 8 where the data in the test summary is plotted as a function of temperature. The high and low were obtained from the 95% limits calculated in the test summary. These are not intended to be the specified limits, but are displayed to indicate the spread in the data obtained for 36 devices.

As expected, the active and standby power supply currents are highest at $-55^{O}C$ and decrease as the temperature increases. Note that the standby current is approximately half the active current at all three temperatures.

5.3 TEST SUMMARY

While testing at -55^{o}C, a problem occurred with moisture condensing on the top and bottom of the thermal insulating pad and the adapter board. This moisture caused false leakage measurements. The devices which failed due to condensation were retested. However, it was impossible to eliminate all the condensation, and leakage paths were present on the adapter board during the input leakage current and output leakage current tests. These undesired leakage paths did not generate a failure, but they increased the measured current resulting in larger currents at the lowest temperature which is contrary to the physical model.

The measured D.C. parameters, as well as the 95% limits calculated in the test summaries, were within the maximum or minimum limit specified in the proposed slash sheet.



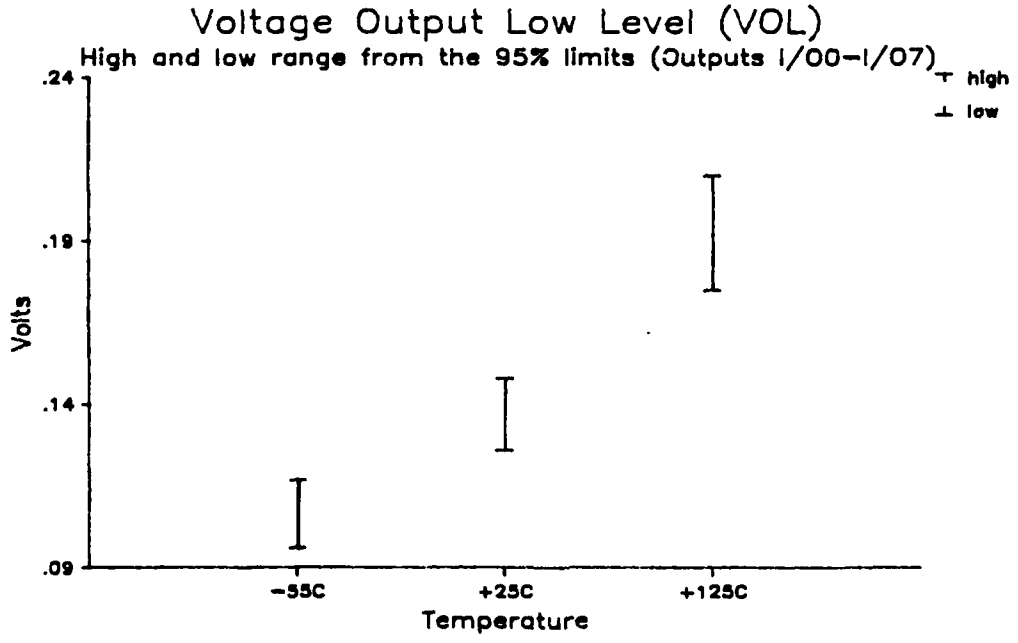


Figure 5: Output Voltage Levels, VOH and VOL

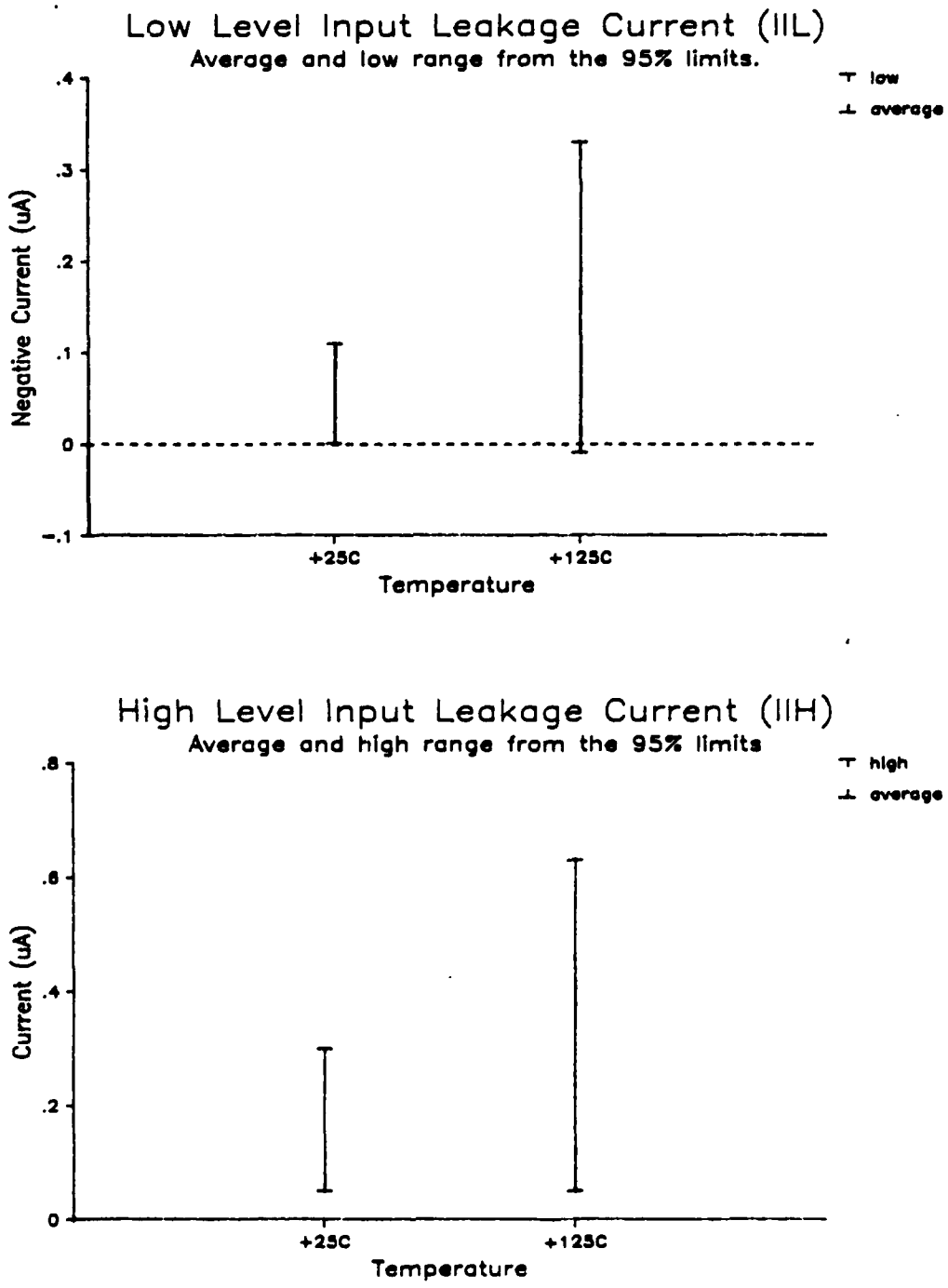
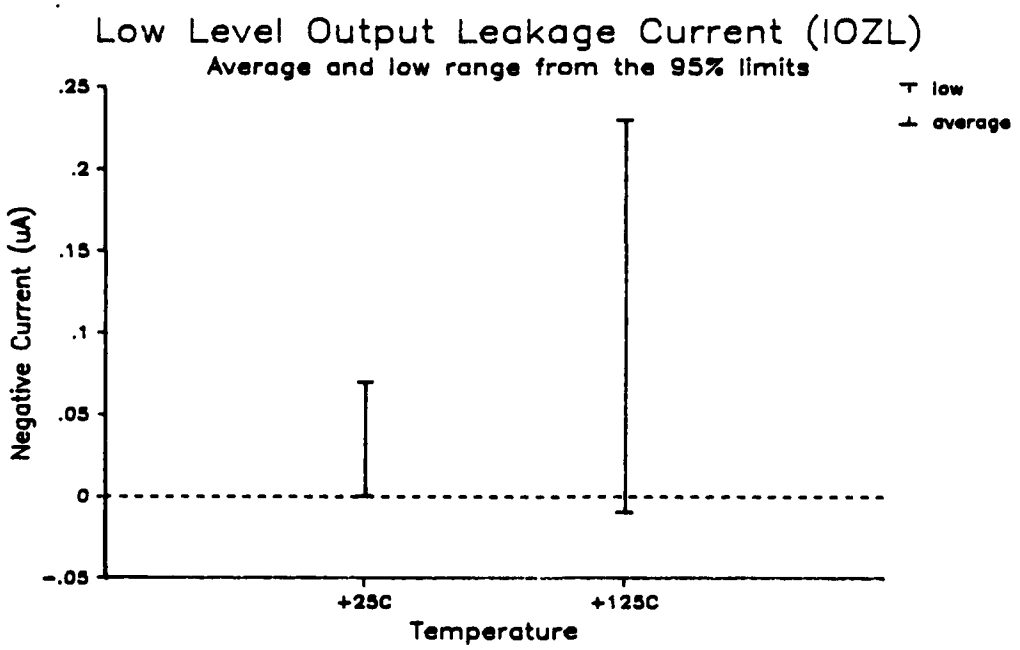


Figure 6: Input Leakage Currents, IIL and IIH



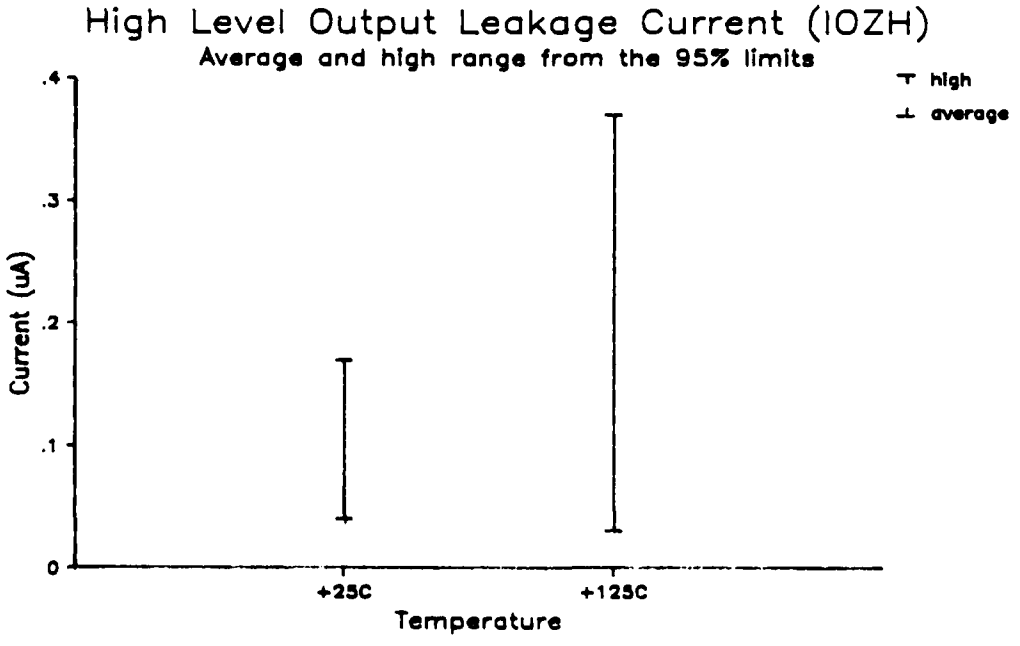
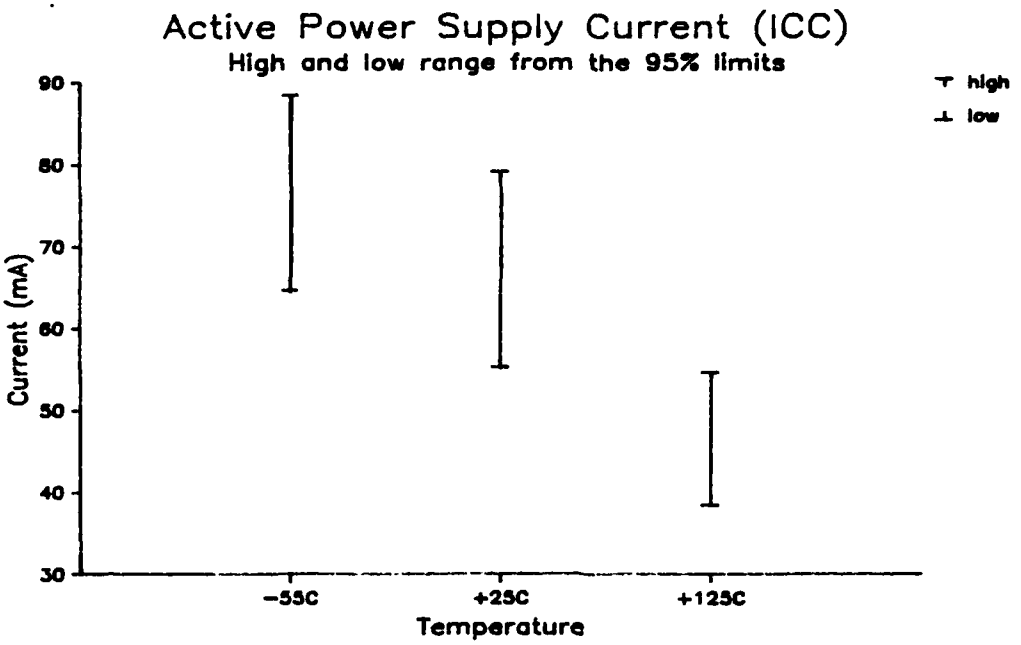


Figure 7: Output Leakage Currents, IOZL and IOZH



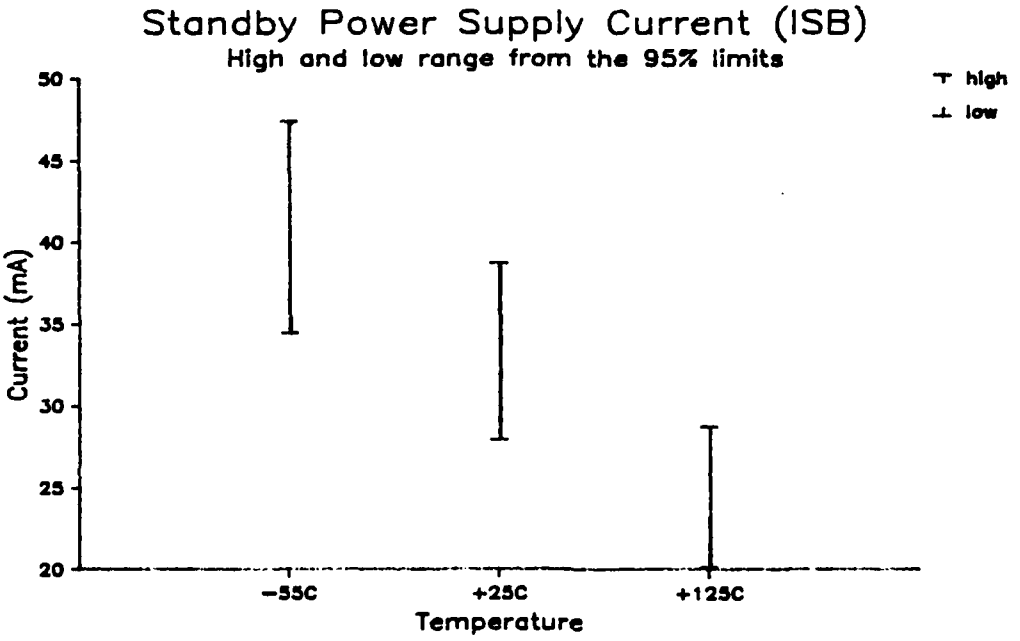


Figure 8: VCC Supply Current, ICC and ISB

6. INPUT/OUTPUT CAPACITANCE MEASUREMENTS

6.1 TEST METHODS

Capacitance measurements were performed on six devices using an HP4192A impedance analyzer. Both input and I/O pin capacitances were measured.

The test procedure was:

- o Set up the meter parameters. Zero adjust the HP4192A to account for any stray capacitance.
- o Connect the OSC OUT probe of the impedance analyzer to the pin under test.
- o Connect the LOW probe to the device's GND pin.
- o Record the capacitance.

The meter parameters were set as follows:

Frequency = 1MHz.
AC RMS amplitude = 50mV.
DC bias = 0V.
The parallel equivalent circuit was used because the series resistance was negligible compared to the impedance of the capacitance.

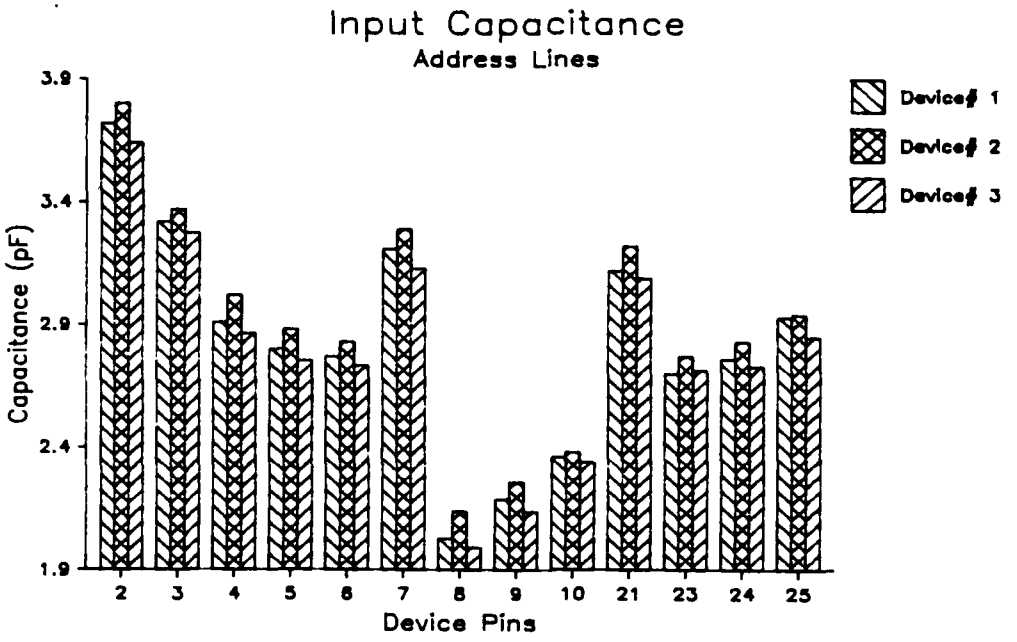
Refer to MIL-STD-883C method 3012.1.

6.2 TEST SUMMARY

The measured data shows that the address lines did not have a uniform capacitance. In Figure 9, the capacitance of the address input pins varies from 2pF to 3.8pF. This is probably due to the difference in the distances from the bond pads to the device pins.

The input capacitance of the control input pins is shown in Figure 10. The Write Enable pin has the highest capacitance, but it is within the specified 6pF.

Figure 11 shows the capacitance of the I/O pins for six devices. The capacitance is highest at the corner pins where the distance from the pin to the bond pad is the greatest. As specified in the proposed slash sheet, the maximum I/O capacitance is 10pF. In all cases, the measured values were below the limit.



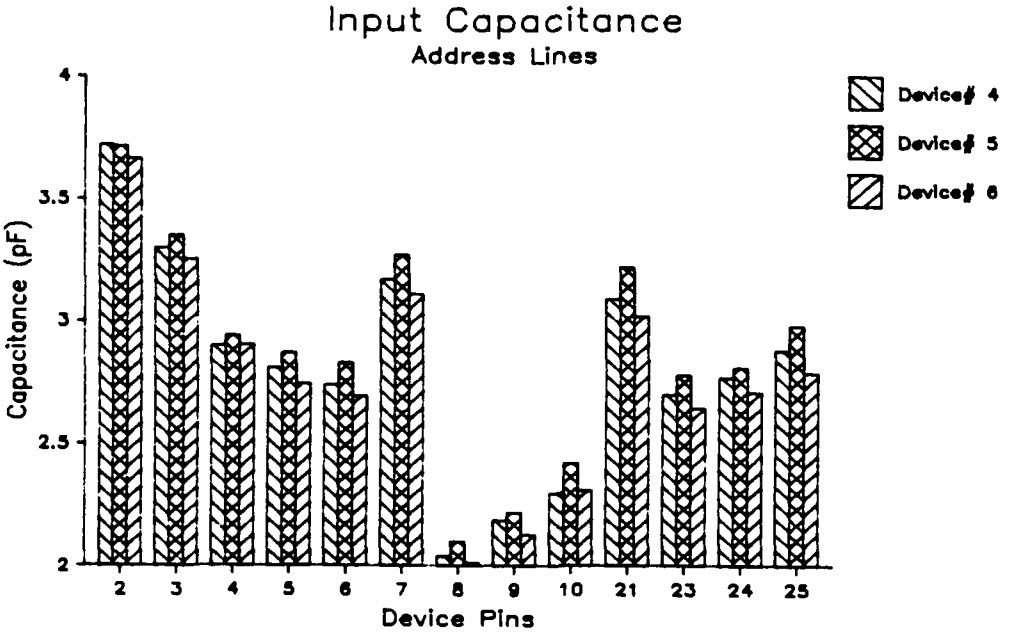
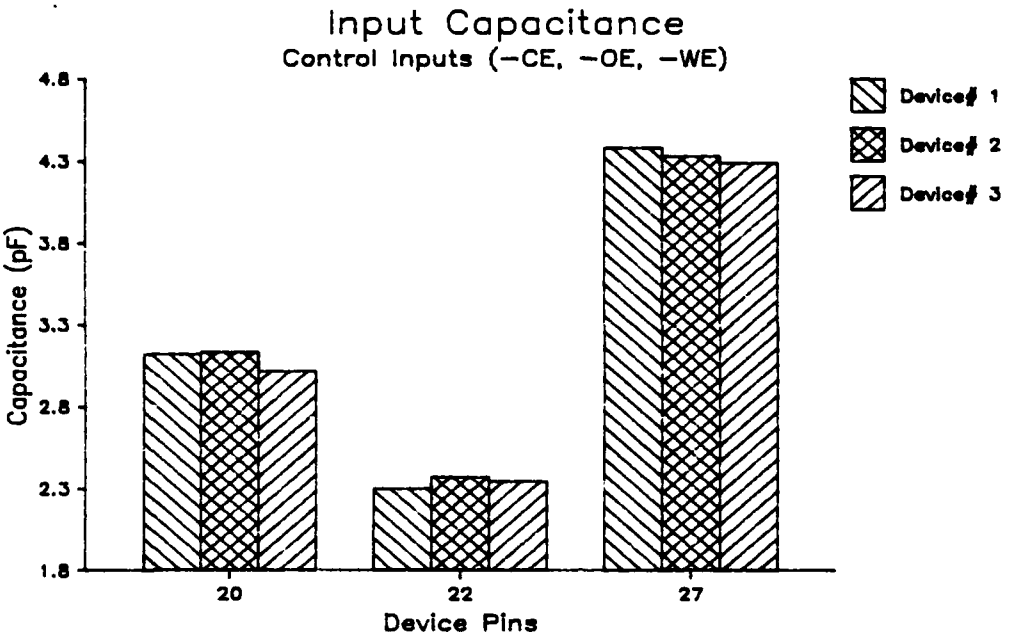


Figure 9: Input Capacitance Measurement



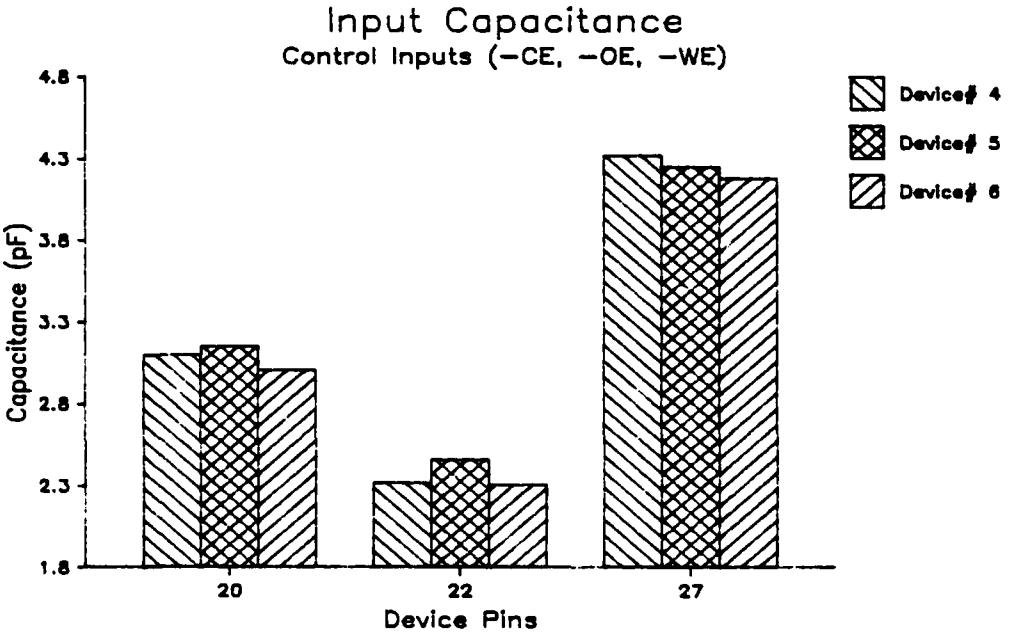


Figure 10: Input Capacitance Measurement (continued)

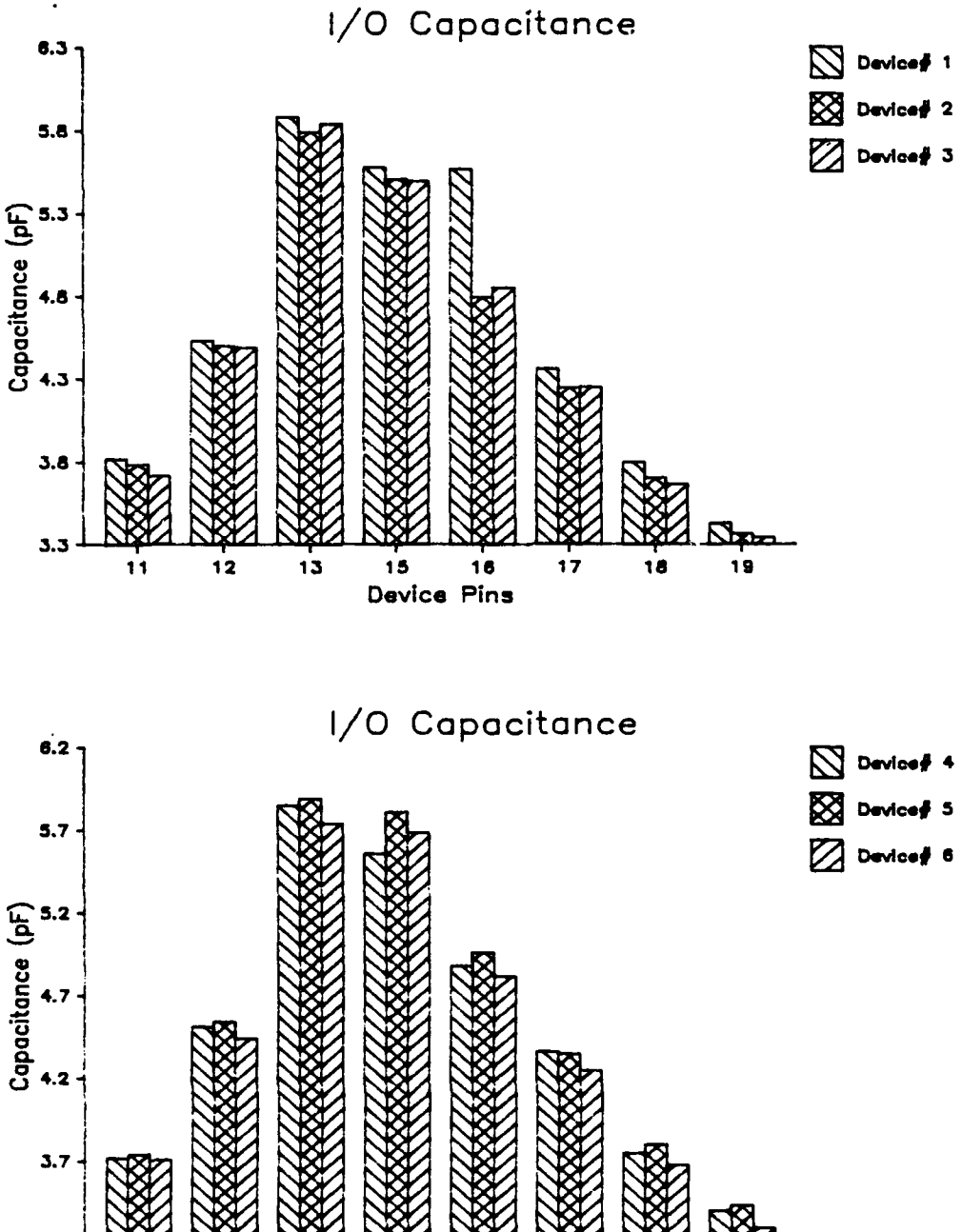


Figure 11: I/O Capacitance Measurement

7. ELECTROSTATIC DISCHARGE, VZAP TESTS

7.1 TEST METHOD

This test is performed to measure the electrostatic discharge sensitivity of the device's input pins. Testing was performed in accordance with MIL-STD-883C method 3015.2 using IMCS model 2400C ESD simulator. After each exposure to an ESD pulse, the devices were analyzed on the Xincom 5588 test system for leakage parameters.

At the onset of this test, the breakdown voltage of the device was unknown. The approach taken was to step the voltage in 1,000 volt increments, until the leakage current exceeded the maximum current of +/- 10uA. After this voltage level was found, it was used as the starting point for further testing with smaller voltage increments.

Each device pin under test was pulsed until a failure (input leakage current exceeded 10uA) occurred. As the testing progressed, the ESD voltage was increased until a failure was obtained with only one pulse.

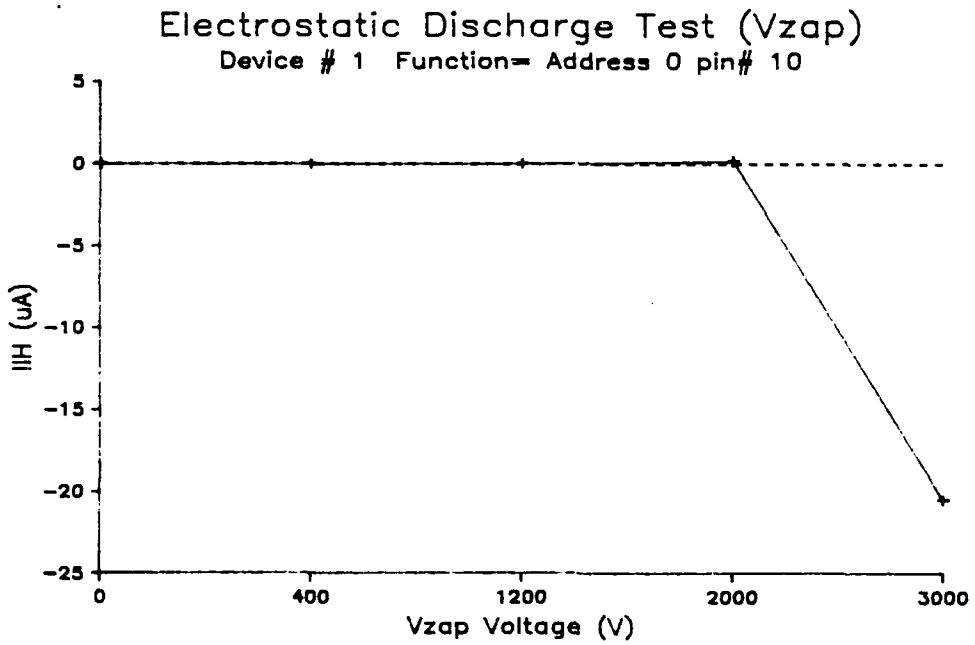
7.2 TEST SUMMARY

The upper graph in Figure 12 shows the input leakage (IIH) versus applied voltage. The ESD voltage was applied to the same device pin in steps of 1,000V, until the leakage current exceeded the 10uA limit. The Xincom 5588 tester was used to measure leakage currents after the ESD pulse was applied. The Xincom's PMU (Precision Measurement Unit) current limit was set to 20.5uA. When a value of -20.5uA is shown on a figure, the input is resistively shorted to VCC (verified using a curve tracer). This device failed IIH after a 3,000V pulse. A starting ESD voltage of 2,500V was selected, since the pin passed after the 2,000V pulse, but failed after the 3,000V pulse.

The goal was to determine the voltage level required to short the input pin with only a single high voltage pulse applied.

The lower graph in Figure 12 (Device #2, pin 6) shows the effect of starting the ESD voltage at 2,500 volts. This device passed after the 2,750V pulse, but failed after the 2,900V pulse. Pin 24 (A9) of the same device failed both IIH and IIL after one pulse at 2,900V. Pin 10 (A21) failed IIH after one pulse at 2,800V. Pin 12 (A2) failed IIL after one pulse at 2,700V. Since one pin passed leakage currents tests after a 2,750V pulse, the 2,700V was the lowest voltage to produce a failure.

In summary, this device can be rated in category "B" (>2000 volts ESD). The ESD voltage level, which causes input leakage failures (shorts), must be greater than or equal to 2,700 volts.



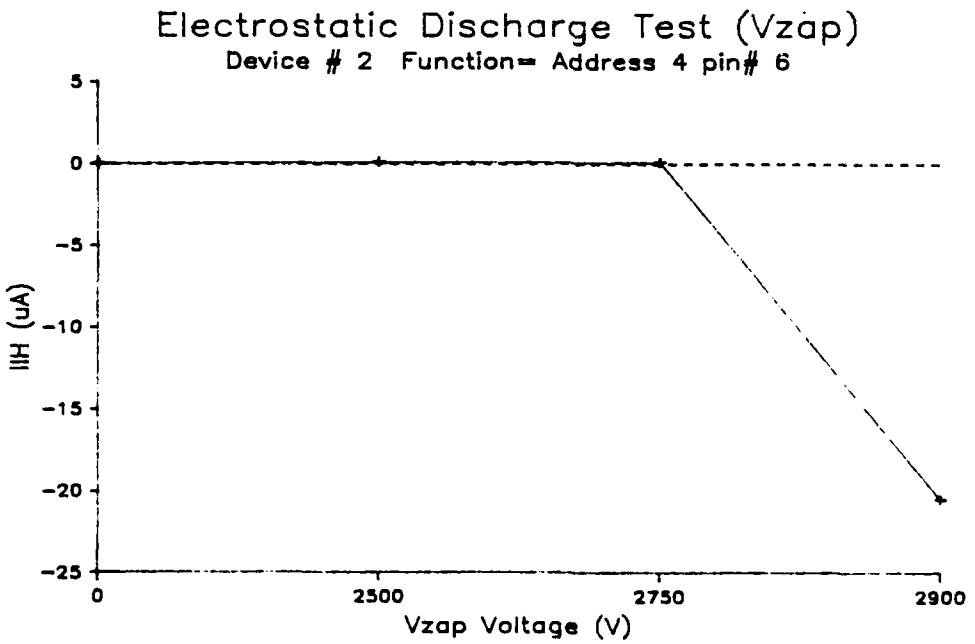


Figure 12: Electrostatic Discharge Test

8. FUNCTIONAL TESTING

8.1 OBJECTIVE

The functional tests verify the integrity of the internal functions under dynamic conditions and ensure every memory cell can be programmed to a "1" and a "0." Several different patterns exercised the device to detect address sequencing sensitivities and data pattern sensitivities. The input timing relationships were set to verify the AC parameters during the write cycle and the output strobe delay was set to verify the Address access time during the read cycle.

8.2 TEST METHOD

Functional testing consisted of seven patterns which exercised the device with VCC at 4.5V and 5.5V. The EEPROM was tested like a static RAM; i.e., the functional patterns contained write cycles and read cycles. All programming was done via the TPC generated patterns on the 5588.

During the functional tests, the outputs were loaded as follows:

- o An 806 Ohm resistor was between each output and 2.09V.
- o A 47pF capacitor was connected from each output to ground. The stray capacitance of the adapter board is approximately 50pF. Therefore, the total capacitance driven by each output was nearly 100pF.

It was necessary to alter the Fairchild supplied TPC patterns to accommodate page mode and the long write cycle (10ms). A 10ms delay after each page write cycle was inserted into the pattern. During this delay, the control lines (-CE, -OE, and -WE) were inactive and the I/O pins were open. In GALPAT0 and GALPAT1, the entire memory array was programmed using page mode and the memory locations were read in a particular order, as opposed to a sequence of write, then read operations. This was acceptable because GALPAT0 and GALPAT1 were implemented to detect read disturb failures.

Functional testing consumed the bulk of the total test time. Mass chip erase and program modes and DATA polling can be used to decrease this time. However, it was necessary to distinguish between failures due to pattern sensitivities and failures due to mass programming modes or DATA polling. For example, if mass

chip erase mode failed to precondition a device prior to the GALPAT1 pattern, a read disturb problem could not be detected. Separate tests were developed to study mass chip program and erase modes and DATA polling.

The functional patterns are described in the Appendix to this part of the report. This section will describe the read and write timings, highlight important patterns, and discuss the test results.

8.2.1 Timing

The read cycle timing is shown in Figure 13. The output strobe delay was set to verify the 450ns Address access time. The byte write timing is shown in Figure 14. The surround by complement format was used on the Address lines and I/O pins to verify the specified set-up and hold times. Figure 15 shows the timing for the page mode write. Only the minimum A.C. parameters are verified. A separate test was run to verify the maximum limits.

Every pattern, except MARCH, used the page mode write cycle. Page mode allows 16 locations to be programmed in 10ms. Only addresses A0 through A3 change during the page write cycle and the time between 2 write pulses must be less than 20us. Using page mode, the entire device was programmed in 5.12s (10ms/page x 512pages).

8.2.2 Patterns

The byte write cycle was used for the MARCH pattern. This pattern took 2 minutes and 45 seconds to execute, but it was necessary to ensure address uniqueness and verify that every cell can be programmed using the byte write. The GALPAT1 pattern ensures the floating gate does not become negatively charged as a result of several read cycles. The GALPAT0 pattern ensures trapped electrons do not escape from the floating gate as a result of several read cycles. Early EEPROM technologies had read disturb problems. The Appendix contains the purpose and the description of all the patterns.

8.3 TEST SUMMARY

The 36 devices passed the functional test at 25°C and 125°C. At -55°C, many devices failed the last two patterns executed at VCC=4.5V and/or most of the patterns executed at VCC=5.5V. Since the devices were tested at 4.5V first, the failures were believed to be caused by moisture condensing on the adapter board and the thermal pad. The failing devices were retested with an abridged version of the program, which only contained the functional tests. Test time was reduced from 12 minutes to 8 minutes, but devices continued to fail, and the test was split in half. All devices were tested with VCC=4.5V, then with VCC=5.5V. Six devices failed at 4.5V and 3 devices failed at 5.5V. Only device #18 failed at both supply voltages. The six failing devices failed the MARCH pattern, which is the last pattern and takes the most time to execute. It is difficult to determine if the failures were valid or moisture induced. Additional studies are required to distinguish between valid failures and moisture induced failures. Once DATA polling is fully understood, it can be used to decrease the test time of the patterns, especially MARCH.

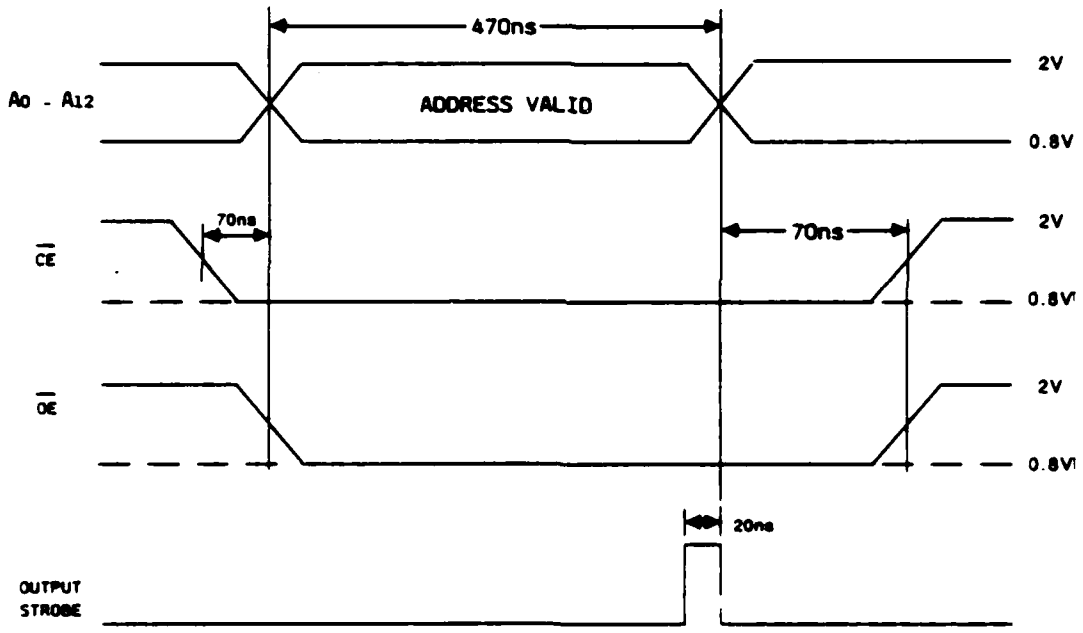


Figure 13: Read Cycle Timing

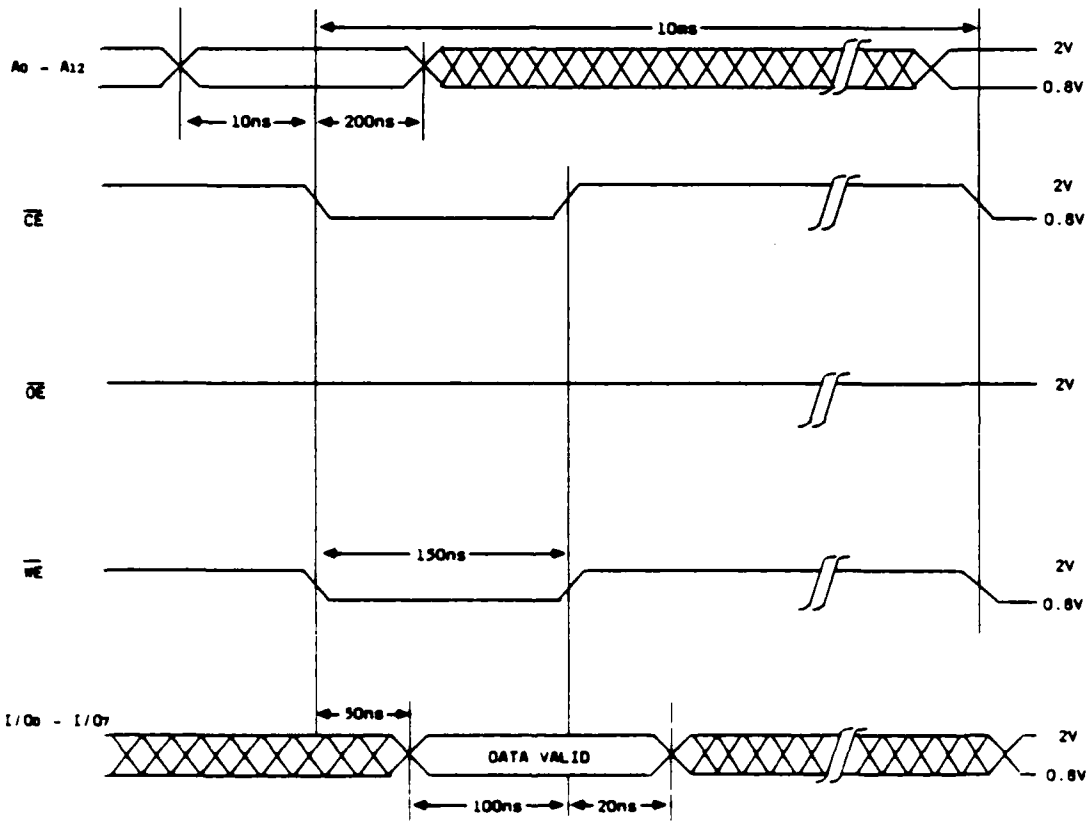
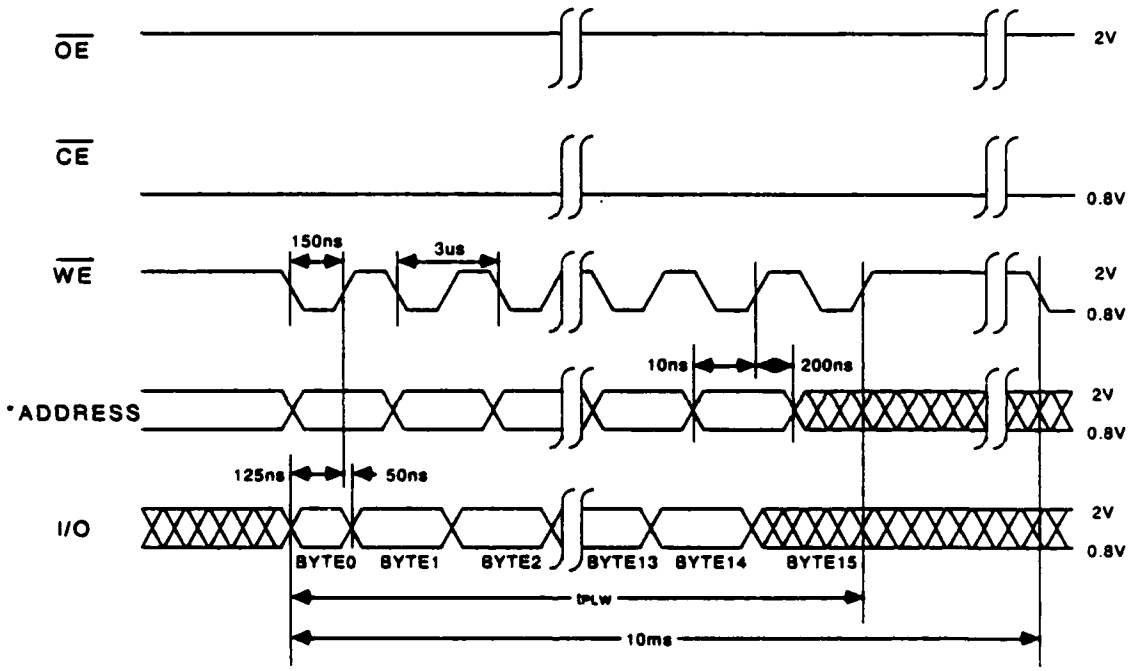


Figure 14: Timing for the Byte Write Cycle



* The page address, addresses $A_4 - A_{12}$ must remain the same throughout the page write cycle (t_{PLW}).

Figure 15: Timing for the Page Mode Write Cycle

9. DYNAMIC CHARACTERISTICS

9.1 OBJECTIVE

The dynamic characterization consisted of measuring the read cycle A.C. parameters and the byte write cycle A.C. parameters. Most of these parameters were verified during the functional test, but they were measured to determine the margin between the actual value and the limit.

9.2 TEST METHODS

The Xincom 5588 memory test system was used to collect data on the A.C. timing parameters. During the characterization of a particular timing parameter, all other parameters were set to their nominal limit or less stringent value. Following this technique guaranteed that as the selected parameter was adjusted toward its operating limit, a failure was due to that parameter.

All 36 sample devices were characterized at -55^{o}C, +25^{o}C, and +125^{o}C. All measurements were made with VCC at 4.5V and 5.5V. During timing parameter measurements, the load specified in section 8.2 was connected to the I/O pins. The test conditions are:

- o VIL = 0V,
- o VIH = 3V,
- o Output comparator level was VOH = VOL = 1.5V,
- o Output capacitive load was approximately 100pF,
- o IOH = -400uA and IOL = 2.1mA.

9.3 READ CYCLE A.C. PARAMETRIC MEASUREMENTS

9.3.1 Pattern

The device under test was programmed with alternating columns of "FF" and "00" using page mode. A TPC pattern was written that read the data along the diagonals of the memory array. Incrementing both row and address locations checks for worst case Address access time and reading alternating data requires the sense amplifiers to respond with complement data every cycle. Also, all eight outputs are switching every cycle.

9.3.2 Access Times

Three access times were measured: Address, Chip Enable, and Output Enable. During the Address access time measurement, Chip Enable and Output Enable were low before the Address lines were valid. For the Chip Enable access time measurement, Output Enable was low and the Address lines were valid 500ns before the falling edge of the -CE signal. For the Output Enable access time measurement, Chip Enable was low and the Address lines were valid 500ns before the falling edge of the -OE signal.

The initial delay time of the output strobe was set to a known failure point (for example, 50ns after the address was valid). The pattern was executed. If the device failed, the delay time of the output strobe was incremented by 1.25ns and the pattern was executed again. The access time was found when the device passed the pattern.

Address access time as a function of temperature and supply voltage is shown in the upper graph in Figure 16. As expected, the access time increased with increasing temperature. The access time also increased as VCC increased, but to a much lesser extent. SHMOO plots (VCC vs. Address access time) were generated for all 36 devices at the three test temperatures. Figures 2, 3, and 4 display the 3 SHMOO plots for device 1. A composite SHMOO plot for each temperature is shown in Figures 17, 18, and 19. Note that the access time is insensitive to VCC, especially for VCC greater than 4.5V. Xicor explained that this apparent anomaly is due to a floating differential sense amplifier. The X2864A has a differential sense amplifier scheme. A voltage below the reference level is sensed as a "0" and a voltage above the reference level is sensed as a "1". The reference level increases as VCC increases. Therefore, as VCC increases, the voltage of the cell being read must rise to a higher voltage before the sense amplifier detects a "1". Thus, the time to detect a "1" will increase and the decreased access time due to a higher supply voltage will be cancelled.

The lower graph in Figure 16 displays the Chip Enable access time versus temperature and VCC. As in the Address access time, the Chip Enable access time is very dependent on temperature and insensitive to VCC. The Chip Enable access time is slightly longer than the Address access time at all temperatures and power supply voltages. Both access times are much faster than the 450ns specified in the slash sheet.

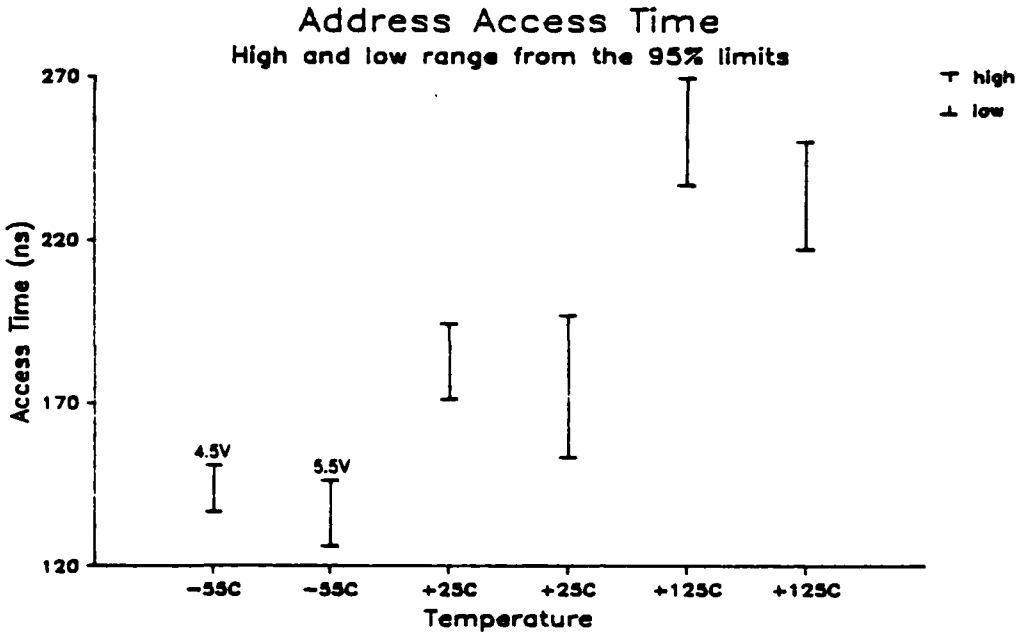
Tables 1, 2, and 3 indicate the Output Enable access time (TOLQV1 and TOLQV2) increases as the temperature increases. This access time is much shorter than Address and Chip Enable access times because the data is present at the output registers. The measured time is only the delay required for the tri-stated I/O pins to display valid data.

9.3.3 I/O Enable Times

The Chip Enable to output active and the Output Enable to output active times were also measured. These delays are important in the prevention of bus contention. For these tests, the time interval from the enable line low to the I/O pins active is measured. This interval is the time required for the tri-stated outputs to become active.

9.3.3.1 TEST METHOD: The input conditions and output loading were as specified in section 8.2. The output strobe was operated in the tri-state mode. A pass occurred when the output voltage was between the comparator voltages and a fail occurred when the output voltage was below the comparator low voltage or above the comparator high voltage. The comparator low voltage was 1.78V, 310mV below 2.09V, and the comparator high voltage was VOH, 2.4V (310mV above 2.09V). The comparator low level was not set to VOL, 0.4V, because the delay time of the 100pF capacitor to decay from 2.09V to 0.4V would be much larger than the delay time of the output going from tri-state to active. Using this mode, the device passed the pattern when the outputs were tri-stated and failed if any output was active.

The start edge of the output strobe was set to a known pass value (it coincided with the falling edge of the enable pin under test) and the stop edge of the output strobe was set to a known pass value (5ns after the start edge). The enable input not under test was active 100ns before the falling edge of the enable input under test. The pattern was executed until a failure occurred. Each time the device passed, the stop edge of the output strobe was incremented by 1.25ns. The failure occurred when the voltage of an I/O pin was above 2.4V or below 1.78V.



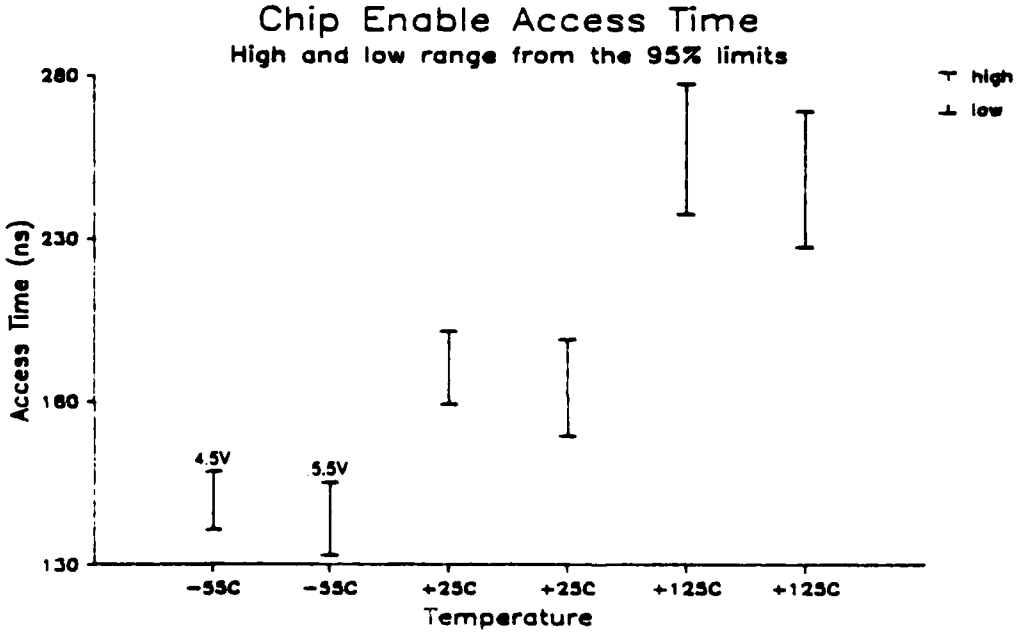
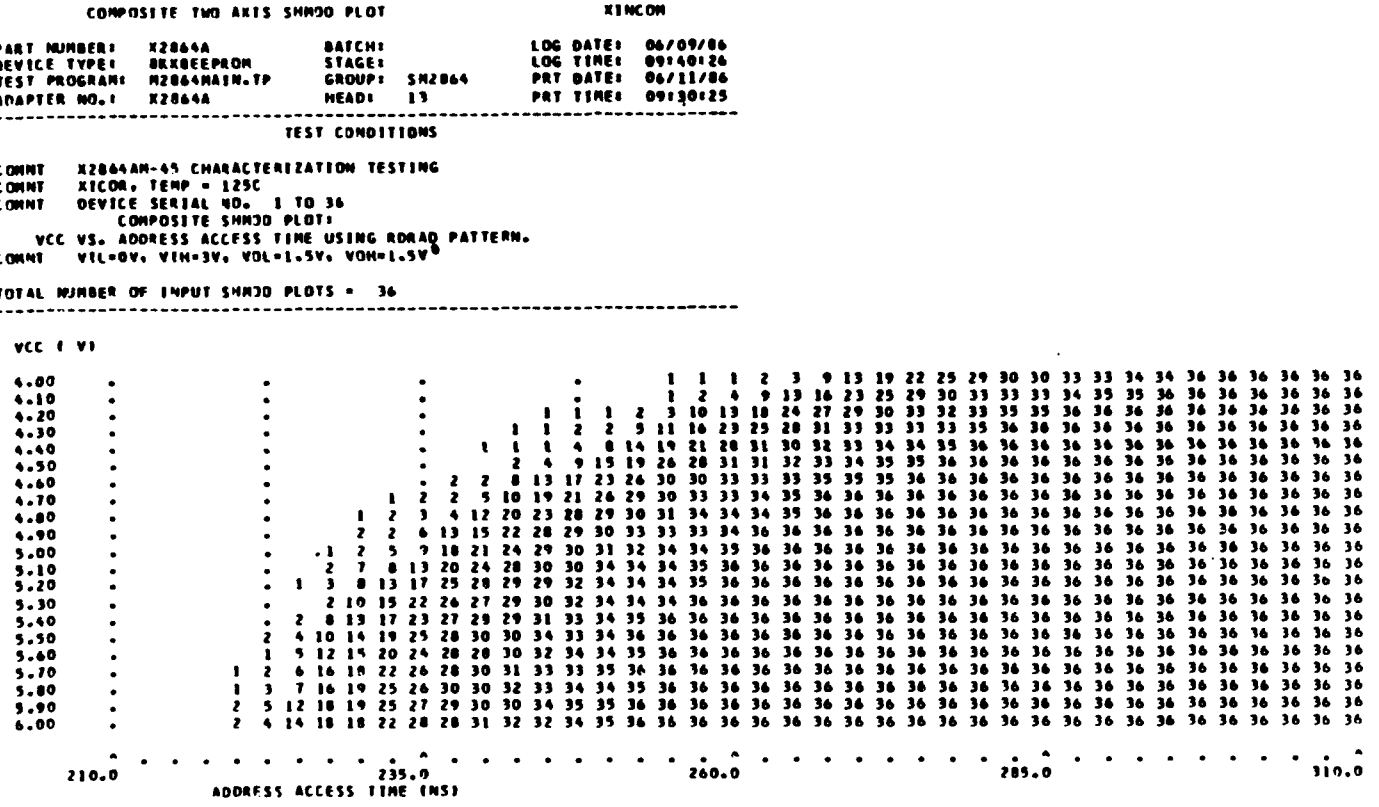


Figure 16: Access Times VS Temperature and VCC

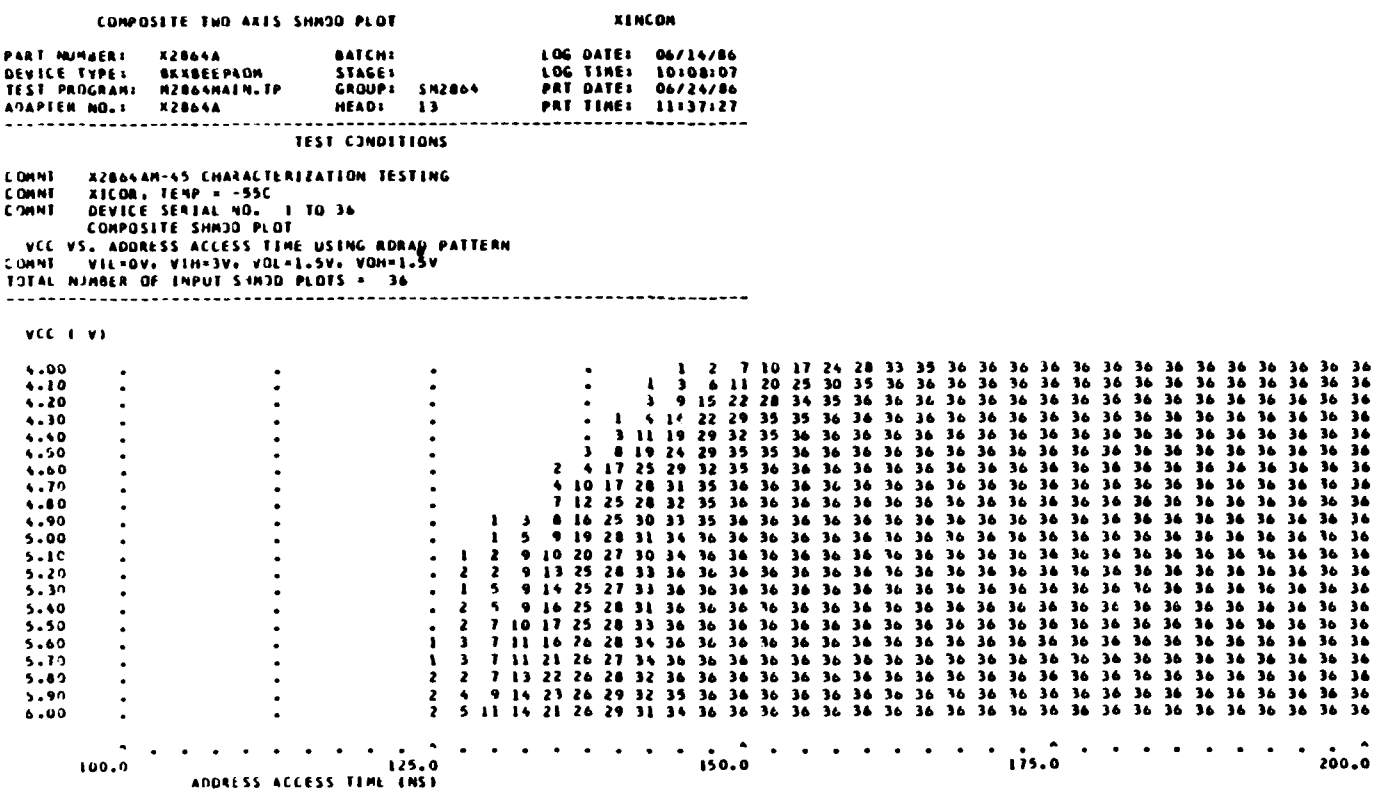
```
        COMPOSITE TWO AXIS SHMOO PLOT                     XINCON

PART NUMBER:    X2864A          BATCH:                 LOG DATE:  07/01/86
DEVICE TYPE:    8KX8EEPROM      STAGE:                 LOG TIME:  09:01:58
TEST PROGRAM:   M2864MAIN.TP    GROUP:  SM2864         PRT DATE:  07/01/86
ADAPTER NO.:    X2864A          HEAD:   13             PRT TIME:  09:24:45
------------------------------------------------------------------------------
                              TEST CONDITIONS

COMNT    X2864AM-45 CHARACTERIZATION TESTING
COMNT    XICOR, TEMP =  25C
COMNT    DEVICE SERIAL NO.  1 TO 36
COMPOSITE 2 AXIS SHMOO: VCC VS. ADDRESS ACCESS TIME USING RDRAD PATTERN
COMNT    VIL=0V, VIH=3V, VOL=1.5V, VOH=1.5V

TOTAL NUMBER OF INPUT SHMOO PLOTS =  36
------------------------------------------------------------------------------

VCC ( V)

4.00  .              .              .              .              .           1  1  4 10 19 24 29 32 33 35 35 36 36 36 36 36 36
4.10  .              .              .              .              .     1  1  2 10 15 22 27 31 32 34 35 35 36 36 36 36 36 36 36
4.20  .              .              .              .              .  1  1  2 12 19 25 28 30 33 35 35 36 36 36 36 36 36 36 36 36
4.30  .              .              .              .              1  1  5 13 20 25 28 33 33 35 35 35 36 36 36 36 36 36 36 36 36
4.40  .              .              .              .              1  5 15 22 25 28 31 34 35 35 36 36 36 36 36 36 36 36 36 36 36
4.50  .              .              .              .        1  1  7 20 24 25 29 31 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36
4.60  .              .              .              .        1  4 13 21 26 27 31 32 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36
4.70  .              .              .              .     1  2 10 19 24 27 30 32 35 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36
4.80  .              .              .              .  1  2  7 15 22 26 29 32 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
4.90  .              .              .              .     3 10 20 25 27 30 30 34 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
5.00  .              .              .              .     6 13 20 27 28 30 31 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
5.10  .              .              .              .  1  6 14 21 28 30 30 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
5.20  .              .              .              .  4 10 18 22 28 29 31 33 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
5.30  .              .              .              .  2 12 20 22 28 29 30 33 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
5.40  .              .              .              .  5 13 20 24 28 30 32 33 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
5.50  .              .              .              .  7 14 21 22 27 30 31 32 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
5.60  .              .              .              1  7 13 20 22 28 30 32 33 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
5.70  .              .              .              1  9 13 17 23 29 29 30 33 34 36 36 36 36 36 36 35 36 36 36 36 36 36 36 36 36
5.80  .              .              .              2  7 15 20 23 28 29 32 33 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
5.90  .              .              .              .  5 13 18 22 27 29 29 32 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
6.00  .              .              .              .  8 13 19 22 28 29 29 32 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36

      ^  .  .  .  .  .  .  .  .  .  ^  .  .  .  .  .  .  .  .  .  ^  .  .  .  .  .  .  .  .  .  ^  .  .  .  .  .  .  .  .  .  ^
    125.0                         150.0                         175.0                         200.0                         225.0
                        ADDRESS ACCESS TIME (NS)
```

Figure 17: Composite SHMOO plot at 25°C



```
        COMPOSITE TWO AXIS SHMOO PLOT                                XINCOM

PART NUMBER:   X2864A            BATCH:              LOG DATE:   06/09/86
DEVICE TYPE:   8KX8EEPROM        STAGE:              LOG TIME:   09:40:26
TEST PROGRAM:  M2864MAIN.TP      GROUP:  SM2864      PRT DATE:   06/11/86
ADAPTER NO.:   X2864A            HEAD:   13          PRT TIME:   09:30:25
-------------------------------------------------------------------------
                              TEST CONDITIONS

COMMT   X2864AM-45 CHARACTERIZATION TESTING
COMMT   XICOR, TEMP = 125C
COMMT   DEVICE SERIAL NO.  1 TO 36
          COMPOSITE SHMOO PLOT:
    VCC VS. ADDRESS ACCESS TIME USING ROMAD PATTERN.
COMMT   VIL=0V, VIH=3V, VOL=1.5V, VOH=1.5V

TOTAL NUMBER OF INPUT SHMOO PLOTS =  36
-------------------------------------------------------------------------

 VCC ( V)

 4.00     .           .           .                       .           1  1  1  2  3  9 13 19 22 25 29 30 30 33 33 34 34 36 36 36 36 36 36
 4.10     .           .           .                       .           1  2  4  9 13 16 23 25 29 30 33 33 33 34 35 35 36 36 36 36 36 36
 4.20     .           .           .                       .        1  1  1  2  3 10 13 18 24 27 29 30 33 32 33 35 35 36 36 36 36 36 36 36 36 36
 4.30     .           .           .                       .     1  1  2  2  5 11 16 23 25 28 31 33 33 33 33 35 36 36 36 36 36 36 36 36 36 36
 4.40     .           .           .                       .     1  1  1  4  8 14 19 21 28 31 30 32 33 34 34 35 36 36 36 36 36 36 36 36 36 36
 4.50     .           .           .                       .        2  4  9 15 19 26 28 31 31 32 33 34 35 35 36 36 36 36 36 36 36 36 36 36 36
 4.60     .           .           .                    .  2  2  8 13 17 23 26 30 30 33 33 33 35 35 35 36 36 36 36 36 36 36 36 36 36 36
 4.70     .           .           .                 1  2  2  5 10 19 21 26 29 30 33 33 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 4.80     .           .           .              1  2  3  4 12 20 23 28 29 30 31 34 34 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 4.90     .           .           .              2  2  6 13 15 22 28 29 30 33 33 33 34 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 5.00     .           .           .           .1 2  5  9 18 21 24 29 30 31 32 34 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 5.10     .           .           .           2  7  8 13 20 24 28 30 30 34 34 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 5.20     .           .           .  1  3  8 13 17 25 28 29 29 32 34 34 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 5.30     .           .           .     2 10 15 22 26 27 29 30 32 34 34 34 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 5.40     .           .           .  2  8 13 17 23 27 29 29 31 33 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 5.50     .           .           .  4 10 14 19 25 28 30 30 34 33 34 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 5.60     .           .           .  5 12 15 20 24 28 28 30 32 34 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 5.70     .           .        1  2  6 16 18 22 26 28 30 31 33 33 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 5.80     .           .        1  3  7 16 19 25 26 30 30 32 33 34 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 5.90     .           .        2  5 12 18 19 25 27 29 30 30 34 35 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
 6.00     .           .        2  4 14 18 18 22 28 28 31 32 32 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
          ^           ^           ^           ^           ^           ^           ^           ^           ^           ^           ^
        210.0                  235.0                  260.0                  285.0                  310.0
                          ADDRESS ACCESS TIME (NS)
```

Figure 18: Composite SHMOO plot at 125°C



```
        COMPOSITE TWO AXIS SHMOO PLOT                                XINCON

PART NUMBER:   X2864A          BATCH:              LOG DATE:  06/16/86
DEVICE TYPE:   8KX8EEPROM      STAGE:              LOG TIME:  10:08:07
TEST PROGRAM:  M2864MAIN.TP    GROUP:  SM2864      PRT DATE:  06/24/86
ADAPTER NO.:   X2864A          HEAD:   13          PRT TIME:  11:37:27
-------------------------------------------------------------------------
                          TEST CONDITIONS

COMMT   X2864AM-45 CHARACTERIZATION TESTING
COMMT   XICOR, TEMP = -55C
COMMT   DEVICE SERIAL NO.  1 TO 36
        COMPOSITE SHMOO PLOT
  VCC VS. ADDRESS ACCESS TIME USING ADRAD PATTERN
COMMT   VIL=0V, VIH=3V, VOL=1.5V, VOH=1.5V
TOTAL NUMBER OF INPUT SHMOO PLOTS =  36
-------------------------------------------------------------------------

  VCC ( V)

  4.00     .       .       .                       .           1  2  7 10 17 24 28 33 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  4.10     .       .       .                       .        1  3  6 11 20 25 30 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  4.20     .       .       .                       .        3  9 15 22 28 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  4.30     .       .       .                       .     1  6 14 22 29 35 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  4.40     .       .       .                       .     3 11 19 29 32 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  4.50     .       .       .                       3     8 19 24 29 35 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  4.60     .       .       .                    2  4 17 25 29 32 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  4.70     .       .       .                    4 10 17 28 31 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  4.80     .       .       .                    7 12 25 28 32 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  4.90     .       .       .           1  3     8 16 25 30 33 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  5.00     .       .       .           1  5  9 19 28 31 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  5.10     .       .       .        1  2  9 10 20 27 30 34 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  5.20     .       .       .     2  2  9 13 25 28 33 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  5.30     .       .       .     1  5  9 14 25 27 33 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  5.40     .       .       .     2  5  9 16 25 28 31 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  5.50     .       .       .     2  7 10 17 25 28 33 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  5.60     .       .       .     3  7 11 16 26 28 34 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  5.70     .       .       .     3  7 11 21 26 27 34 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  5.80     .       .       .     2  7 13 22 26 28 32 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  5.90     .       .       .     4  9 14 23 26 29 32 35 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
  6.00     .       .       .     5 11 14 21 26 29 31 34 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36 36
           .       .       .     .       .       .       .       .       .       .       .       .       .       .       .       .
         100.0           125.0                   150.0                   175.0                   200.0
                  ADDRESS ACCESS TIME (NS)
```

Figure 19: Composite SHMOO plot at -55°C

9.3.3.2 TEST SUMMARY: Figure 20 contains plots of the enable times (LZACC1, LZACC2, TOLOX1, and TOLOX2 in Tables 1, 2, and 3) as a function of temperature and power supply voltage. The data at -55°C is not accurate because 4 devices recorded 0ns delays. This was due to condensed moisture on the adapter board resulting in leakage paths to ground which held the tri-stated I/O pins at 0V. Thus, the I/O pins appeared to be active. Referring to the data at 25°C and 125°C, the enable times increased with temperature and the enable times from Chip Enable are more sensitive to VCC than the enable times from Output Enable. Also, note the enable times from -CE are twice as long as those from -OE and that all enable times easily meet the 10ns minimum specified in the proposed slash sheet.

9.3.4 I/O Disable Times

This test measures the amount of time required to tri-state an output from an active state. The delays from -CE to all I/O pins tri-stated and from -OE to all I/O pins tri-stated were measured.

9.3.4.1 TEST METHOD: The input conditions and output loading were as specified in section 8.2. The output strobe was operated in the tri-state mode. The voltage at the I/O pins, after tri-stating, becomes a function of the time constant of the load capacitor and resistor. The output stage actually turns off long before the voltage on the output pin reaches the load voltage (2.09V). Normally, the comparator high and low voltages are set to the load voltage plus 500mV and the load voltage minus 500mV, respectively. Preliminary test results (delay measurements and scope verification) indicated the time required to charge the capacitor from VOL to 1.59V (load voltage - 500mV) was much greater than the disable time. The following method for selecting the comparator voltages was adopted:

- o Take all outputs high.
- o Connect the output loads.
- o Measure each output voltages using the PMU which is forcing zero current.
- o Calculate the average VOH. Set the comparator high voltage to the average VOH-100mV.
- o Repeat above steps with all outputs low. Set the comparator low voltage to the average VOL+100mV.

By using this method, the measured disable times are less dependent on RC time constants. It is important to have a wide strobe window to ensure the output has

indeed tri-stated. A wide output strobe window prevents VOL to VOH transitions, VOH to VOL transitions, and noise spikes from being interpreted as the voltage on a tri-stated output moving towards the load voltage.

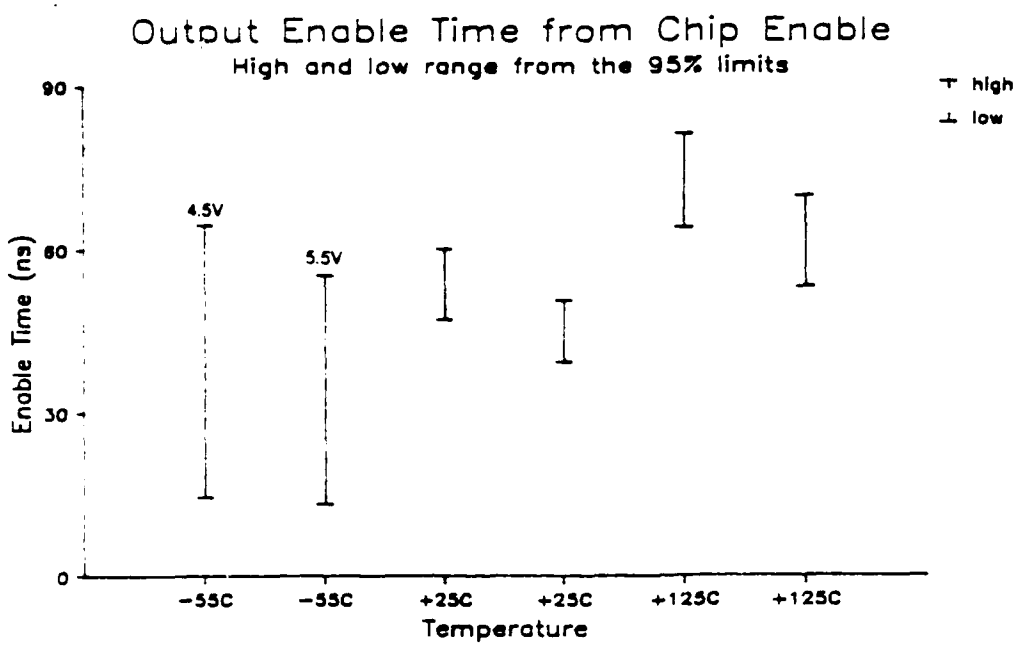
The start edge of the output strobe was set to a known fail value (it coincided with the rising edge of the enable pin under test) and the stop edge of the output strobe was set to a known pass value (300ns after the rising edge of the enable input under test). The enable input not under test was inactive 300ns after the rising edge of the enable input under test. The pattern was executed until the device passed. Each time the device failed, the start edge of the output strobe was incremented by 1.25ns. The pass occurred when the voltage on every I/O pin was above the average VOL+100mV and below the average VOH-100mV during the entire strobe window.

9.3.4.2 TEST SUMMARY: The data from the device summaries (HZACC1, HZACC2, TOHQZ1, and TOHQZ2) is graphed in Figure 21. Similar the other propagation delays, the disable time increased as the temperature increased. The disable times also increased as VCC increased. This was not expected since most delay times decrease with increasing power supply voltage. This was probably due to the average VOH exceeding 4.1V. The largest comparator high voltage on the 5588 is 4V. Thus, if the average VOH-100mV was greater than 4V, the comparator level would be set to 4V. The voltage on the I/O pins would need to decrease by more than 100mV to be in the pass region. This requires more time and yields longer delays at VCC = 5.5V. As in the enable times, the disable time from -CE is greater than the disable time from -OE and both are within the specified limits of 10ns and 100ns.

One more item needs to be mentioned about enable and disable times. From the system designer's viewpoint, it is desirable for the disable time to be less than the enable time. This will eliminate bus contentions since the previously selected device's outputs will tri-state before the newly selected device's outputs become active. Comparing the data at VCC = 4.5V, the enable and disable times from -CE meet this system requirement. However, the disable time from -OE is longer than the enable time from -OE This is probably necessary to minimize the access time from -OE and is acceptable to the system designer, because the devices are selected via the Chip Enable pin.

9.4 BYTE WRITE CYCLE A.C. PARAMETRIC MEASUREMENTS

All specified A.C. parameters for the byte write cycle were measured. This section describes eight of the thirteen A.C. parameters. The byte write cycle parameters were measured because most of the functional tests used page mode. During the functional testing, the timing and waveshapes were assigned in such a manner that the page write cycle parameters were verified. It was decided not to



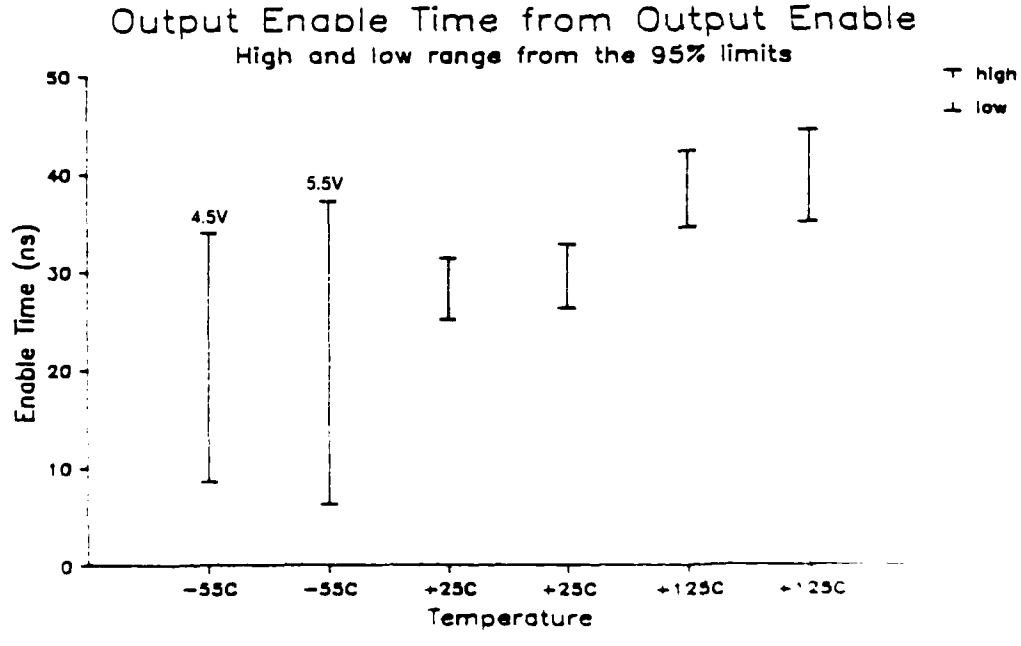
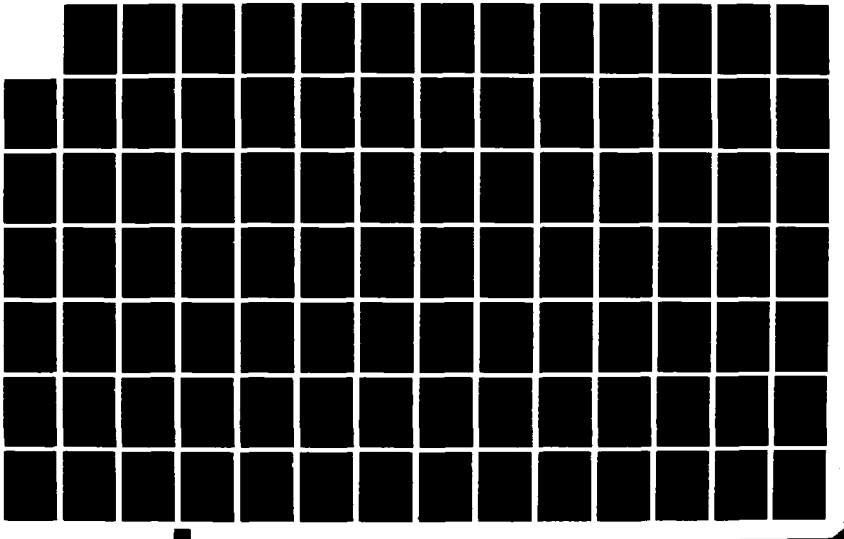
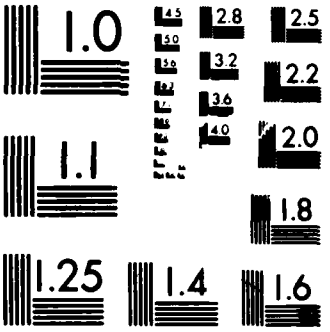
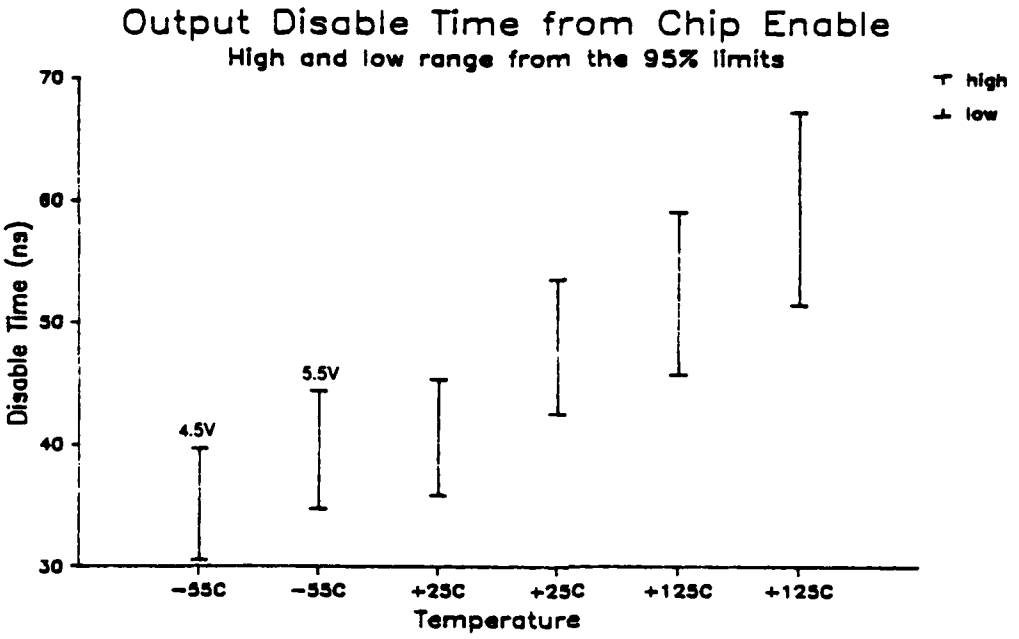


Figure 20: Output Enable Times VS Temper[illegible]

AD-A180 114 ELECTRICAL CHARACTERIZATION OF VLSI RAMS AND PROMS(U) 3/5
GTE COMMUNICATIONS SYSTEMS CORP PHOENIX AZ
M FORMOSO ET AL. OCT 86 RADC-TR-86-180 F30602-84-C-0070
UNCLASSIFIED F/G 12/6 NL







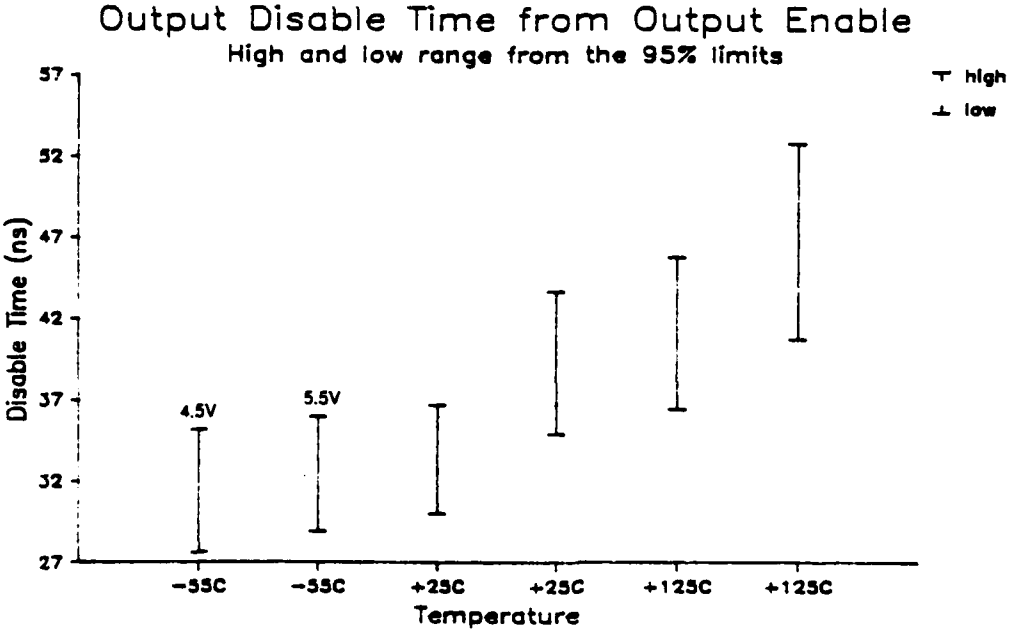


Figure 21: Output Disable Times VS Temperature and VCC

measure the A.C. parameters for the page write cycle, since they were adequately tested by six of the seven functional patterns.

9.4.1 Test Method

Figure 22 contains the flow chart of the 5588 routine used to measure the A.C. parameters. Note that data is only written into one address location during the search. Since the data on the I/O pins and address inputs are latched by the -WE pulse, the set-up and hold times are not dependent on the memory cells written. The set-up and hold times for the Chip Enable and Output Enable pins are independent of the memory cell written because they initiate the internal write cycle.

The test conditions specified in section 9.2 were applied during these measurements.

9.4.2 Address Set-up Time and Hold Time

The address is latched by the falling edge of the -WE signal. During this test, half the address lines were at VIH and the other half were at VIL, and the surround by complement format was used. This allowed the worst case set-up time and hold time to be measured. The data in Figure 23 indicates that the address is actually latched several nanoseconds after the falling edge of the -WE signal. This was verified by Xicor. They stated the device must first ensure the write pulse is valid. Also, the input data at the Address lines takes about 60ns to reach the latches.

9.4.3 Data Set-up Time and Hold Time

The input data on the I/O pins is latched by the rising edge of the -WE signal. During the test, the data was alternating 1's and 0's and the surround by complement format was used. The measured set-up and hold times are displayed in Figure 24. The negative hold time indicates the data is latched prior to the rising edge of the -WE signal.

According to Xicor, the X2864A automatically loads all 1's into the internal data latch when the address is latched. This latch is then written with the data on the I/O pins when the -WE signal goes high. This agrees with preliminary measurements, which showed the set-up time to be much less if the data was all 1's than if the data was all 0's.

9.4.4 Output Enable Set-up Time and Hold Time

The -OE set-up time is referenced to the falling edge of the -WE signal and the -OE hold time is referenced to the rising edge of the -WE signal. This test produced unexpected results (see TOHWL1, TOHWL2, TWHOL1, and TWHOL2 in

Tables 1,2, and 3). The measured set-up and hold times were negative and large. This means the rising edge of -OE could occur several nanoseconds after the falling edge of -WE or the falling edge of -OE could occur before the rising edge of -WE and a valid byte write cycle would execute. This seemed to disagree with the truth table and Xicor was asked to explain. Xicor agreed with the data, stating that the internal timers take over once -OE is high and -WE is low. The rising edge of the -OE signal sets a flip-flop which allows a write cycle. Xicor also stated that once a write cycle is initiated, the internal timers control the device and it is impossible to interrupt or halt the write. Designers should be aware of this.

9.4.5 Chip Enable Set-up Time and Hold Time

The -CE set-up time is referenced to the falling edge of the -WE signal and the -CE hold time is reference to the rising edge of the -WE signal. The results were similar to the Output Enable set-up and hold time measurements. However, a more interesting result was the minimum pulse width of the write pulse. During the set-up time measurement, the write pulse was created by the falling edge of -CE and the rising edge of -WE. During the hold time measurement, the write pulse was created by the falling edge of -WE and the rising edge of -CE. The set-up and hold time measurement routine was also measuring the minimum write pulse width formed by -CE and -WE. It was decided to datalog the minimum pulse widths, rather than the set-up time and hold time, because the minimum pulse widths formed by -CE and -WE signals were smaller than the minimum pulse width for the -WE signal. The minimum pulse widths as a function of temperature and power supply voltage are shown in Figure 25. The write pulse formed by the falling edge of -CE and the rising edge on -WE was the narrowest pulse to initiate a write cycle. At $-55^{o}C$, the measured minimum pulse width, TCLWH1, was less than 20ns (17.5ns was the smallest) for seven devices.

9.5 TEST SUMMARY

All the measured access times were less than the 450ns specified in the proposed slash sheet. The access times are more sensitive to temperature than to VCC. SHMOO plots of Address access time vs. VCC indicated little or no variation in access time over a wide variation of power supply voltage.

All of the measured A.C. parameters meet the specifications. It is important to know that once -OE is high and -WE is low (and -CE is low), internal timers control the device and the write cycle cannot be aborted. A write pulse formed by -WE and -CE does not have noise protection (a pulse less than 20ns wide may initiate a write cycle).

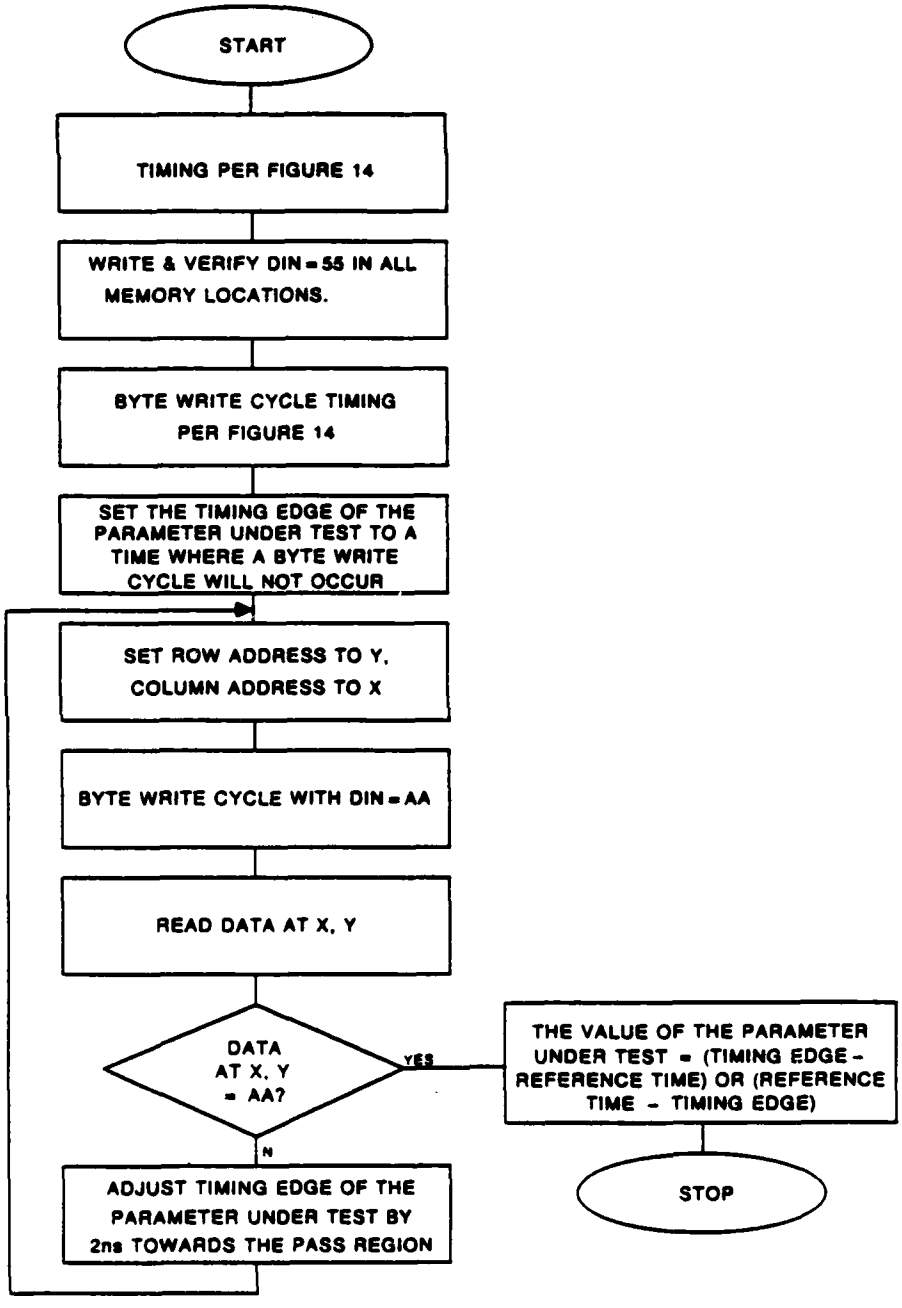
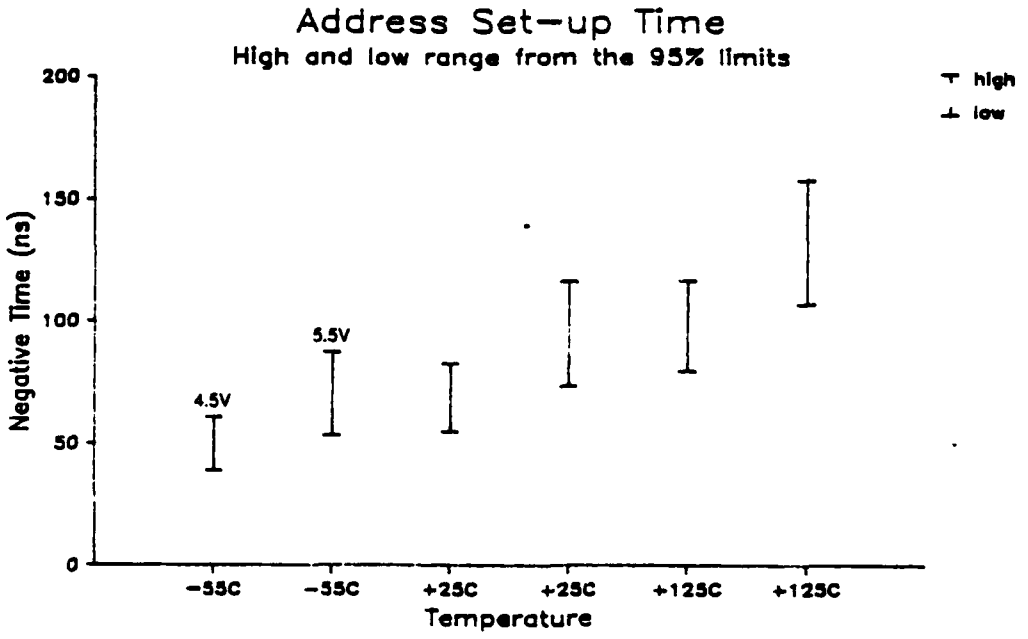


Figure 22: Flow Chart of the A.C. Parametric Measurement Test



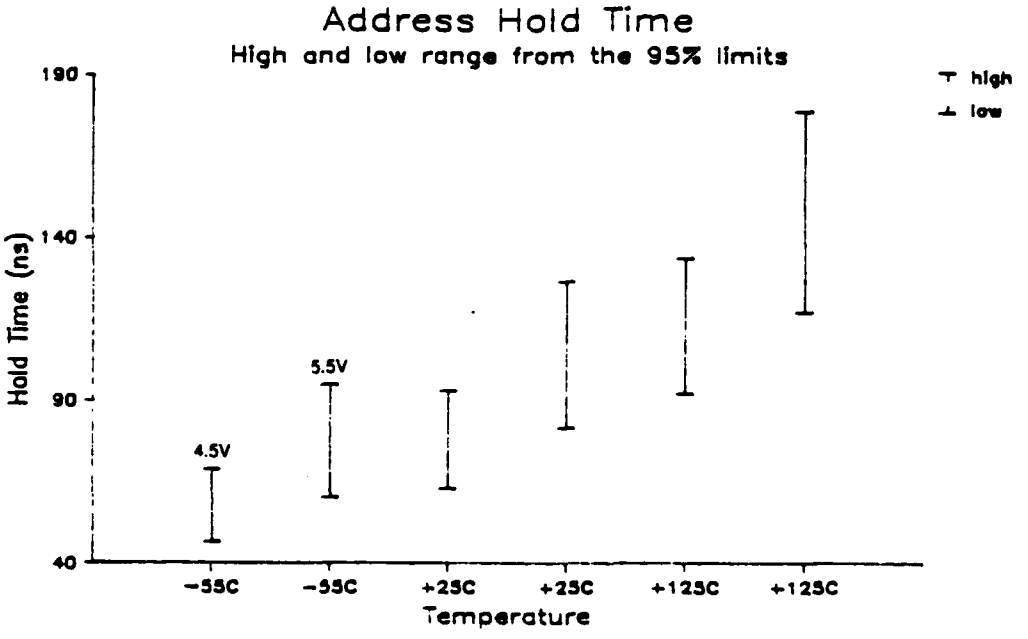


Figure 23: Address Set-up Time and Hold Time VS Temperature and VCC

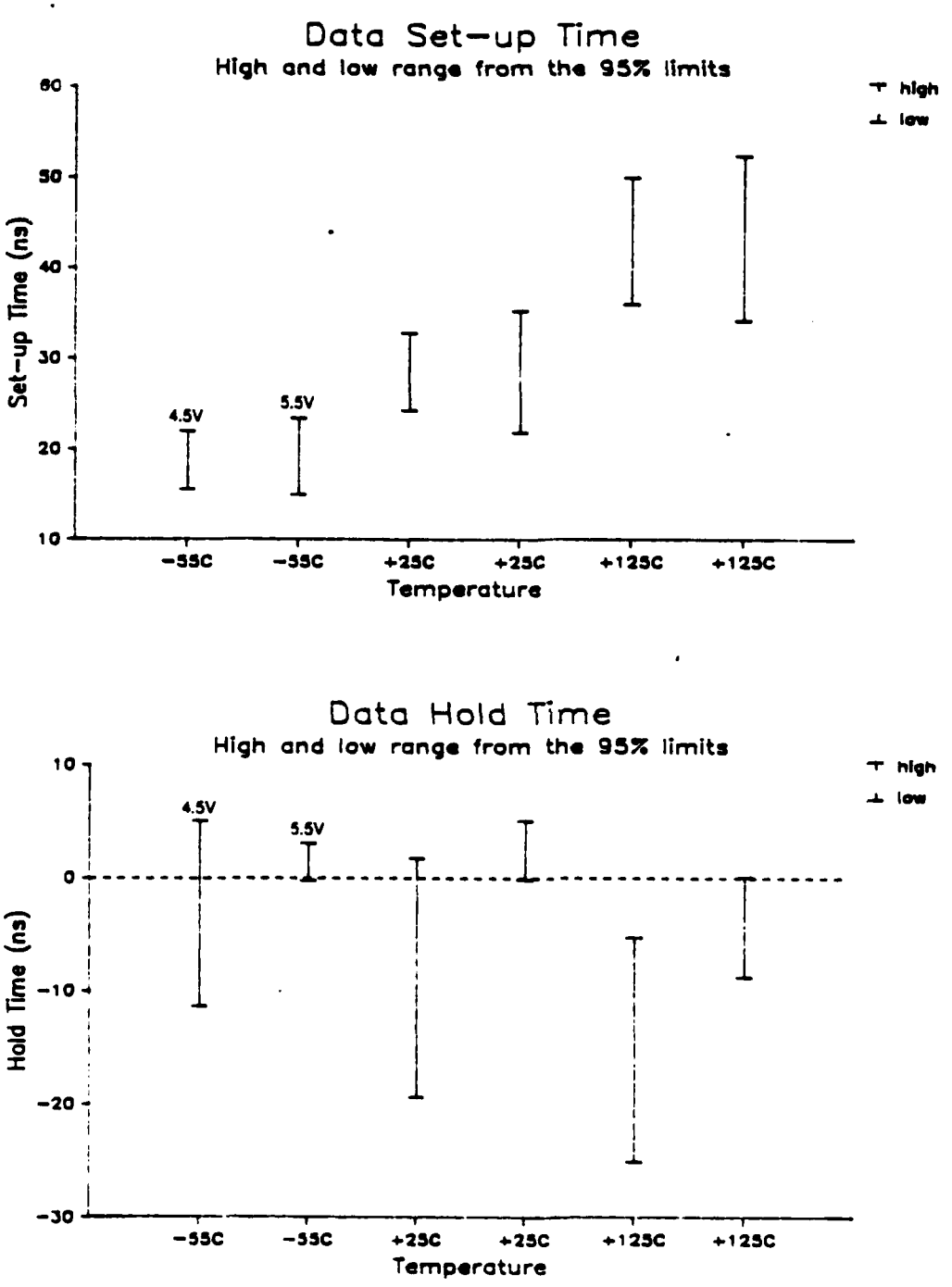
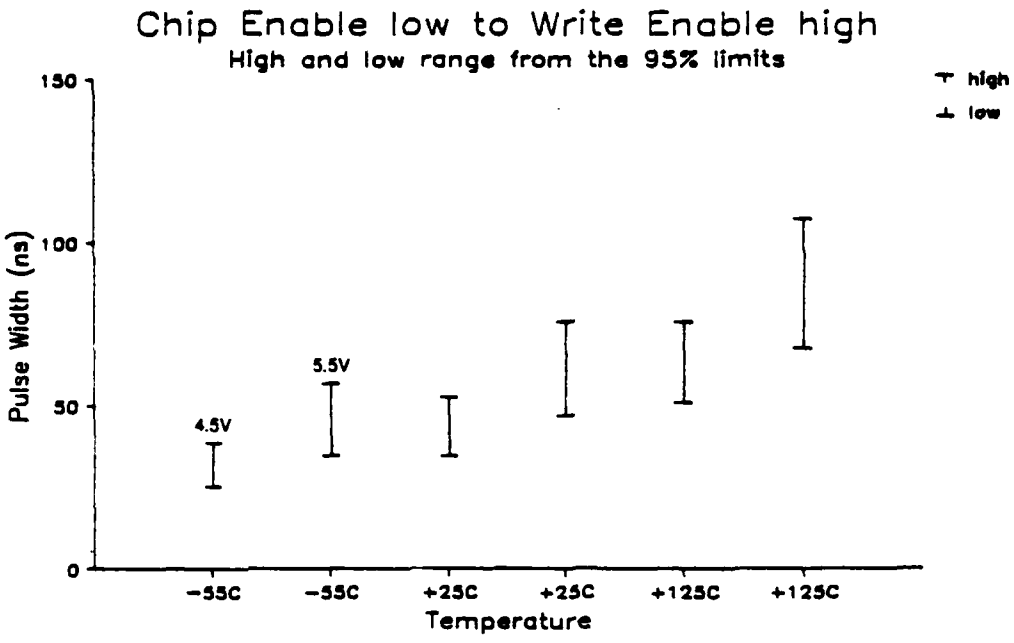


Figure 24: Data Set-up Time and Hold Time VS Temperature and VCC



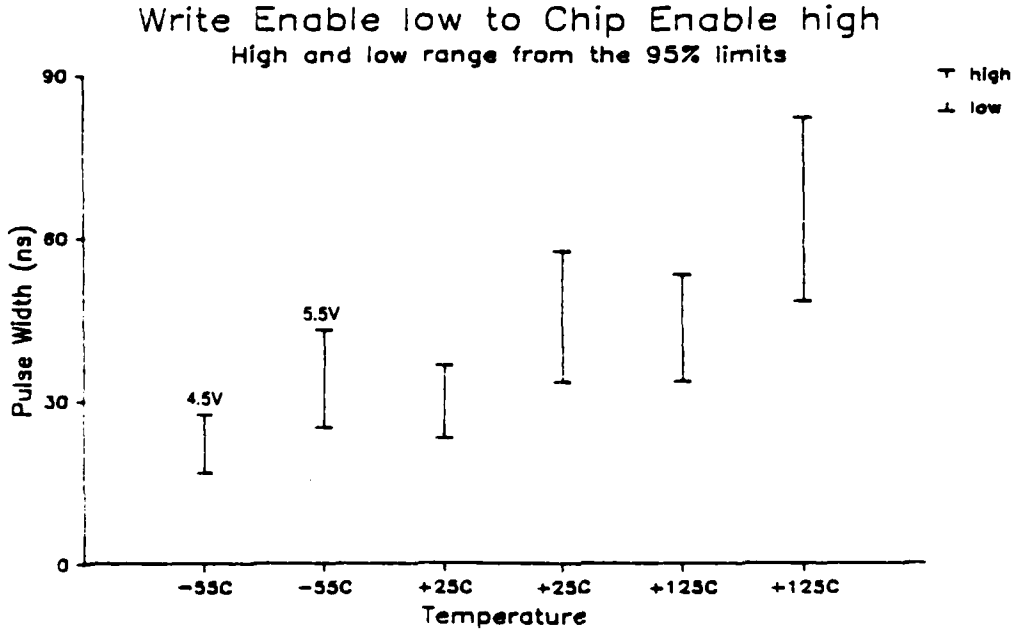


Figure 25: Minimum Write Pulse Widths VS Temperature and VCC

10. SPECIAL FEATURES OF THE X2864A

10.1 OBJECTIVES

Every EEPROM vendor advertises the special features incorporated in his device. The special features attempt to overcome the negative aspects of an EEPROM: long write cycles and inadvertent write cycles. Xicor offers three techniques to decrease the effective write cycle time and a noise protection feature on the Write Enable input, which ensures glitches do not initiate a write cycle.

This section describes the test procedures used to evaluate the special features.

10.2 MASS ERASE AND PROGRAM

The mass erase/program feature of the EEPROM allows the user to erase or program the entire device in one write cycle. To erase all bits in the memory, the I/O pins are at VIH, -WE pin is at VIL, and -OE is at 18V to 22V. Mass programming is performed by taking the I/O pins and -WE pin to VIL, while -OE is at 18V to 22V. After a mass erase cycle, all memory locations contain FFh (floating gates are stripped of electrons and are positively charged), after the mass program all memory locations contain 00h (floating gates trap electrons and a net negative charge). The states of the address lines are not important, as all locations are programmed to the same state.

The mass program write cycle differs from the byte write or page write cycle, in that a cell is not erased before it is programmed. This is desirable because the test results indicate it may be necessary to perform several sequential mass program cycles to ensure all bits are cleared. This is especially true at low VCC or at low temperature.

10.2.1 Test Procedure

The mass erase test was performed in the following manner:

a. Precondition all bytes to 00h (00 hex). Program all memory cells by executing six sequential mass program write cycles (VCC = 5.5V, I/O = 0.8V, -CE = -WE = 0.8V, and -OE = 18V). Six program write cycles are performed to ensure the floating gate is negatively charged. Since a margin test for the floating gate does not exist for Xicor's X2864A, it was assumed 6 sequential mass program cycles, at the best case VCC, would

result in a floating gate with the same negative charge as it would have after a byte write cycle. The byte write cycle and page mode were not used, because it would take at least 5 seconds to precondition the device, as opposed to 60 milliseconds using 6 mass program cycles.

b. Verify all zeroes in all locations. If any failure, abort the test and consider the device to be not mass programmable nor mass erasable. If no failures, the preconditioning was successful and the mass erase test was continued.

c. Perform one mass erase write cycle (VCC = 4.5V, I/O = 2.0V, -CE = -WE = 0.8V, and -OE = 18V).

d. Read and expect FFh in all locations.

e. If a failure, repeat a through d with VCC = 5.0V in c.

f. If a failure, repeat a through d with VCC = 5.5V in c.

g. If a failure, abort the test and consider the device to be not mass erasable.

The mass program test was performed in the following manner:

a. Precondition all bytes to FFh. Erase all memory cells by executing six sequential mass erase write cycles (VCC = 5.5V, I/O = 2.0V, -CE = -WE = 0.8V, and -OE = 18V). Six erase write cycles are performed to ensure the floating gate is devoid of electrons. Since a margin test for the floating gate does not exist for Xicor's 2864, it was assumed 6 sequential mass erase cycles, at the best case VCC, would result in a floating gate with the same positive charge as it would have after a byte write cycle.

b. Verify FFh in all locations. A failure should not occur because the previous test proved the device could be mass erased.

c. Perform one mass program write cycle (VCC = 4.5V, I/O = 0.8V, -CE = -WE = 0.8V, and -OE = 18V).

d. Read and expect 00h in all locations.

e. If a failure, repeat a through d with VCC = 5.0V in c.

f. If a failure, repeat a through d with VCC = 5.5V in c.

g. If a failure, abort the test and consider the device to be not mass programmable.

10.2.2 Test Summary

The results of this test are shown in Figure 26. Each bar represents the number of devices that passed the test at a particular VCC. Fail means the device could not be initialized by the 6 programming pulses. The mass program test results contain fewer devices, because devices that could not be initialized for the mass erase test were not considered. Figure 26 indicates that most devices will not be erased by a single mass erase cycle at VCC = 4.5V. This is the only parameter that did not meet the specification.

10.3 VCC SENSE

The X2864A has a VCC sense circuit which will not allow a write cycle to initiate if VCC is less than 3V (typical value; a minimum is not specified by Xicor). The VCC sense circuitry protects against inadvertent write cycles during device power up and power down.

10.3.1 Test Procedure

The lowest VCC level at which a write cycle occurred was determined in the following manner:

a. VCC = VIH = 5V. Erase all locations using page mode and verify.

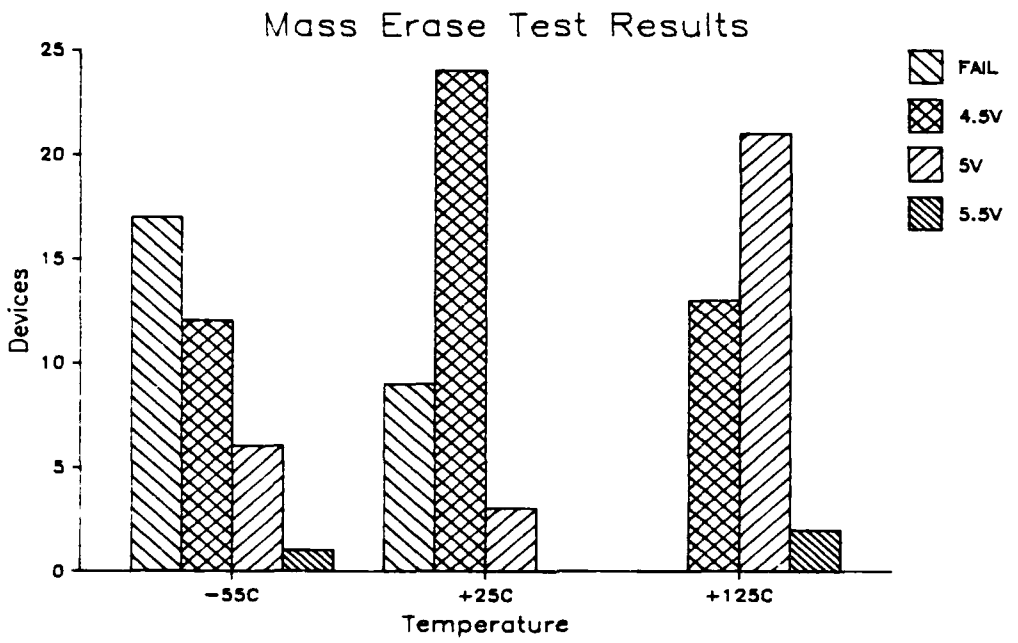
b. VCC = VIH = 2.4V. Write 00h in all locations using page mode. At VCC = 2.4V, it is anticipated that a write cycle will not occur. VIH is set equal to VCC during the entire test because VIH must not exceed VCC.

c. VCC = VIH = 5V. Read the page under test and expect FFh in all locations.

d. If no failures, a write cycle did not occur. Go to e. A failure indicates a write cycle did occur and the lowest VCC at which a write will occur has been found.

e. Repeat a through d and increment the VCC and VIH voltages in b by 0.125V every iteration until a failure occurs in d.

Nominal timing is used for the read and write cycles. VIL = 0V; VOH = VOL = 1.5V for the comparator levels.



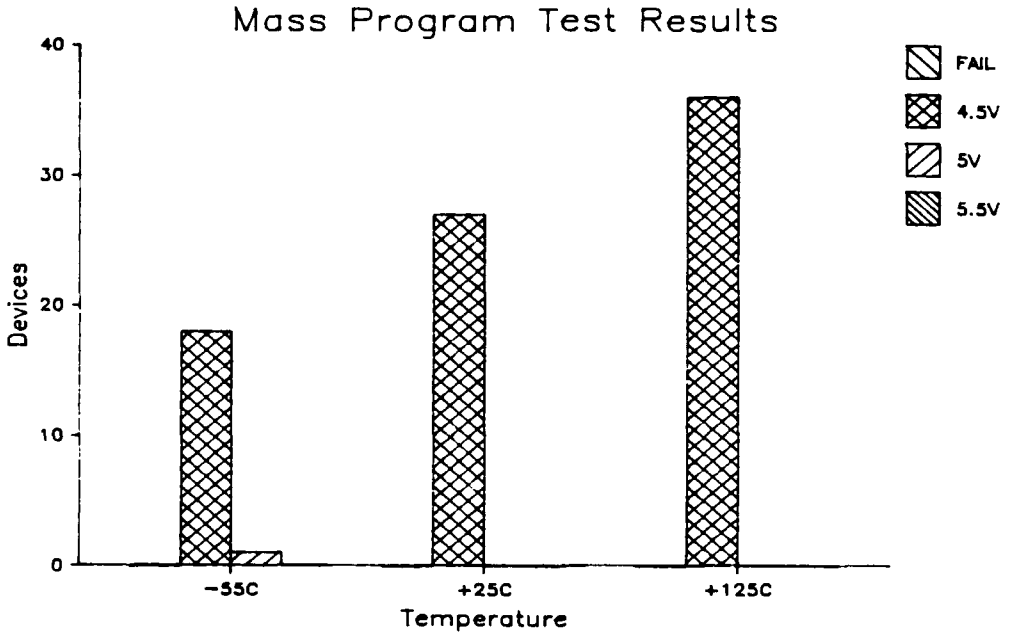


Figure 26: Supply Voltage for Mass Erase and Mass Program

10.3.2 Test Summary

The high and low limits from the 95% limits (VCCACC in Tables 1, 2, and 3) are plotted in a high-low graph shown in Figure 27. The VCC sense voltage decreased as the temperature increased and it was generally above 3V.

10.4 DATA POLLING

DATA polling is a special feature which allows the system software to monitor the status of a write cycle. During a read cycle, the most significant bit of the last byte written indicates when the write operation is complete. While the internal write cycle is in process, I/O7 will be the complement of the data written at bit 7. The completion of the internal write cycle is detected when I/O7 reflects the true data. The other I/O pins are not defined while the internal write cycle is in process.

DATA polling allows the user to take advantage of the typical byte write time or page write time without the expense of added hardware or extra outputs.

Two tests were run to verify the proper operation of DATA polling and to determine the following two parameters. A write recovery test was developed to measure the delay required between DATA polling finished (reading true data at I/O7) and the next write cycle. A second test measured the delay from the rising edge of the Write Enable signal to the start of DATA polling (reading complement data at I/O7).

10.4.1 Write Recovery

A write cycle should not be executed immediately after DATA polling is finished (reading true data at I/O7), because the charge pump of the X2864A is still recovering from the previous write. The back bias generator on the device, which should be at -3V, is at -6V or -7V. According to Xicor, the back bias generator requires 50us to 500us to rise to -3V. During this time, the threshold voltage increases. The on-chip latches, which are set at the initiation of a new write pulse, are not reset by the falling edge of the write pulse. Therefore, if a write cycle occurs before the back bias generator reaches -3V, all 1's will be written independent of the data on the I/O pins.

Refer to Figure 28 for the flow chart of the 5588 test used to measure the write recovery time. The timer is required because the output latch, which holds the complement of the data written at I/O7, will flip if the bias generator is below -3V. This means, even though a "1" is being written at data bit 7 (the internal data latch did not reset), a "1" is read at I/O7 and, when the write cycle is over, a "1" is still read at I/O7. If the timer is not used, an infinite loop will exist. This test was performed with VCC at 4.5V and 5.5V.

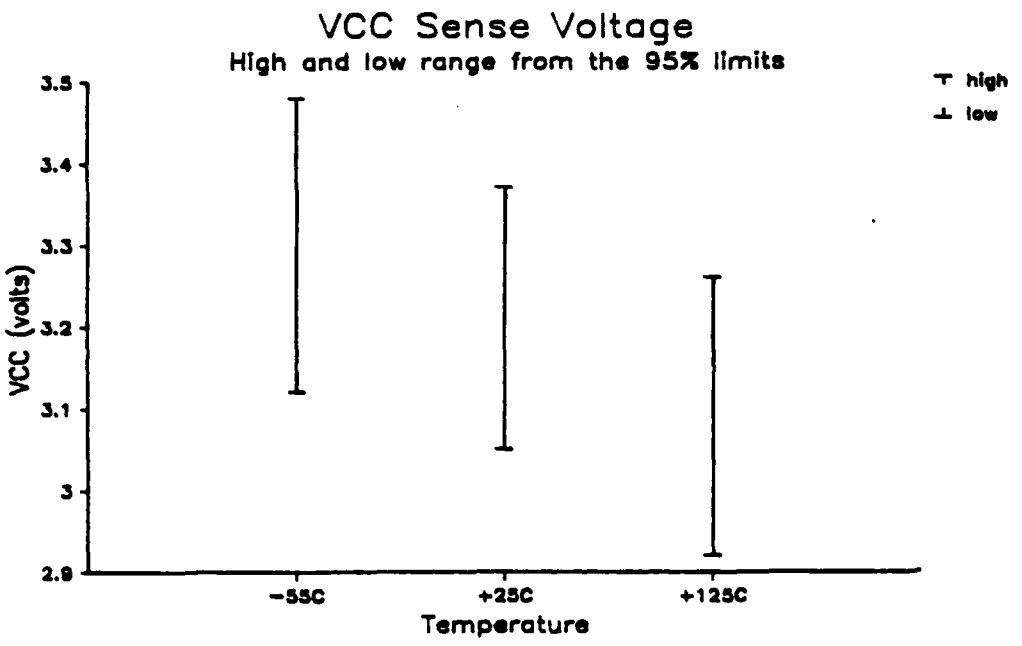


Figure 27: VCC Sense Voltage VS Temperature

In Tables 1, 2, and 3, TQVWL1 is the write recovery time at the minimum VCC and TQVWL2 is the write recovery time at maximum VCC. With VCC at 5.5V, the actual write recovery time was not found because the devices passed the first time. The 30us starting value was selected based on Xicor's claim that the write recovery time was between 50us and 500us. The data indicates that the write recovery time is maximum at low VCC (4.5V) and at -55^{o}C.

10.4.2 Time from Write Enable High to DATA Polling

This test measures the time delay from Write Enable high (end of the write pulse) to complement data on I/O7. The flow chart of the test routine used in the 5588 program is in Figure 29. This test was run with VCC at 4.5V and 5.5V.

Figure 30 plots the high and low range obtained from the 95% limits. The plotted data is TWHQC1 and TWHQC2 in Tables 1, 2, and 3. The -WE high to DATA polling delay is less than the measured address access time. As expected, the delay increased as the temperature increased.

10.4.3 Test Summary

These two tests prove that DATA polling does work. The system application designer should be aware of the write recovery time. Also, DATA polling should not be initiated immediately after the rising edge of the -WE signal. Test engineers should revise functional patterns to use DATA polling. As will be noted later, the measured write cycle time was less than one half the specified 10ms. The use of DATA polling in test programs may cut the test time in half, as functional testing consumes most of the test time.

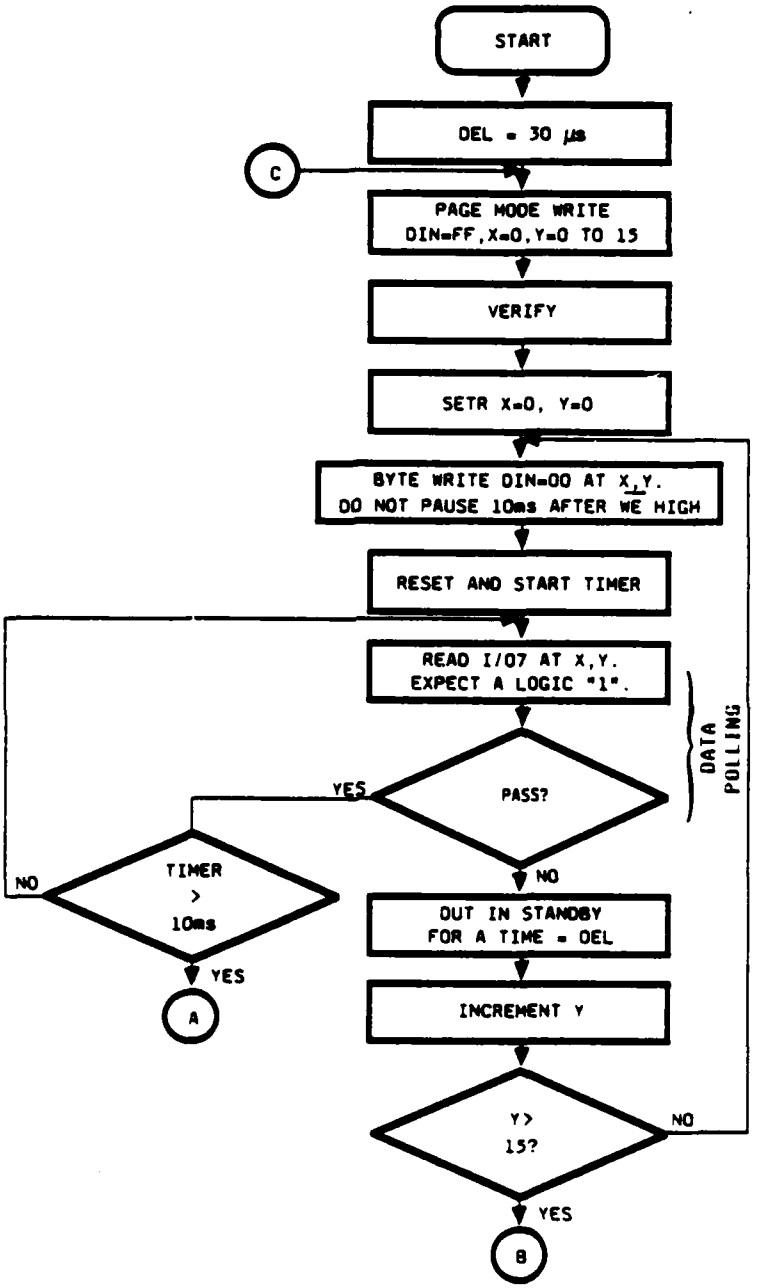


Figure 28: Flow Chart of the Write Recovery Time Test

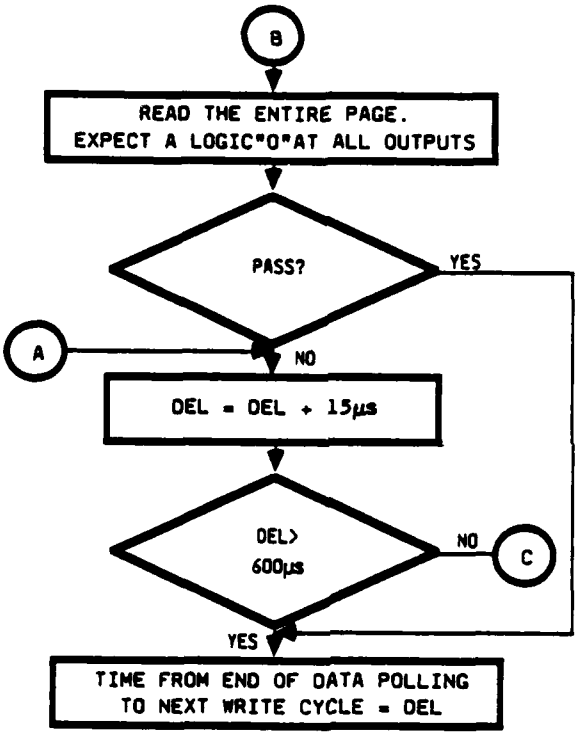


Figure 28: Flow Chart of the Write Recovery Time Test (continued)

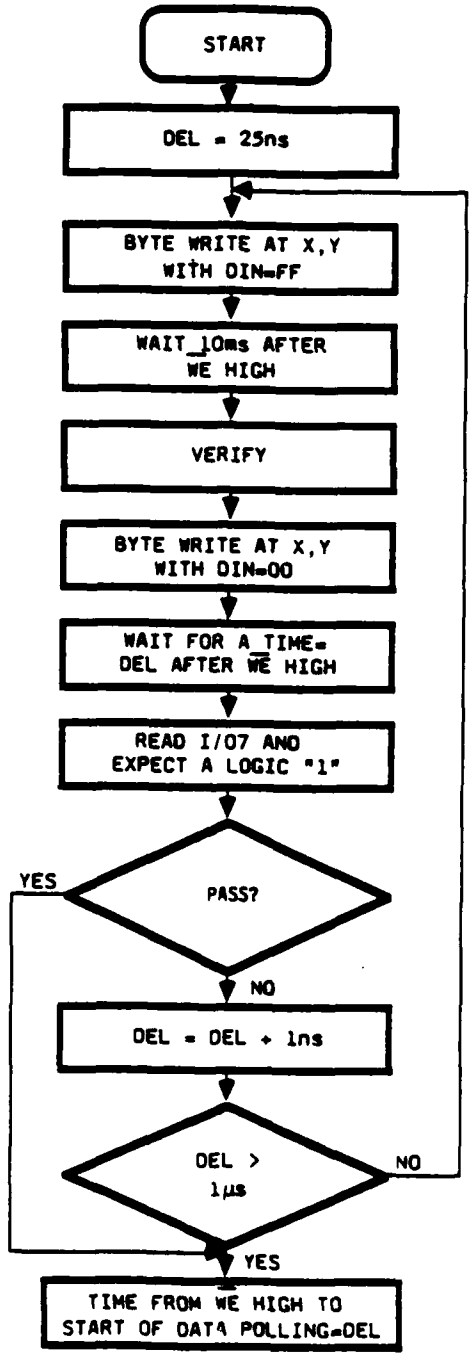


Figure 29: Flow Chart of the -WE high to DATA Polling Test

10.5 MINIMUM WRITE PULSE WIDTH

An EEPROM must be able to distinguish between a valid write pulse and a glitch on the -WE pin. Otherwise, a glitch on the -WE pin will cause an inadvertent write cycle to occur. The device eliminates this problem by ignoring any write pulse that is less than 20ns wide. This is called noise protection and this feature specifies that a write cycle will not be initiated if the pulse width of the -WE signal is less than 20ns.

Note that this feature explicitly refers to the -WE pin. However, a valid write pulse can be generated in the following manners:

a. The falling edge of -WE and the rising edge of -CE. The rising edge of -WE occurs after the rising edge of -CE. The falling edge of -CE occurs before the falling edge of -WE.

b. The falling edge of -CE and the rising edge of -WE. The rising edge of -CE occurs after the rising edge of -WE. The falling edge of -OE occurs before the falling edge of -CE.

c. The falling and rising edge of -CE if -WE is low.

The minimum write pulses that were generated by points a and b were determined during the -CE set-up time and -CE hold time measurement tests. Since the -CE set-up and hold times were much better than their specifications, it was decided to datalog the minimum write pulse widths. Furthermore, these pulse widths were narrower than the minimum -WE pulse width. See section 9.4.5 for more details.

The pulse width generated by point c was similar to the results for -WE at 25^{o}C and it was not investigated over temperature. Preliminary testing also showed that the measured minimum pulse width on -WE was the same for a page mode write and a byte write. The test was performed using the byte write. It was faster than a page write and writing to one location was sufficient, since the -WE signal latches the address data and I/O data into internal registers. The internal write cycle copies the data in the register into the memory array at the location specified by the address latch. Therefore, minimum write pulse width is not a function of the address.

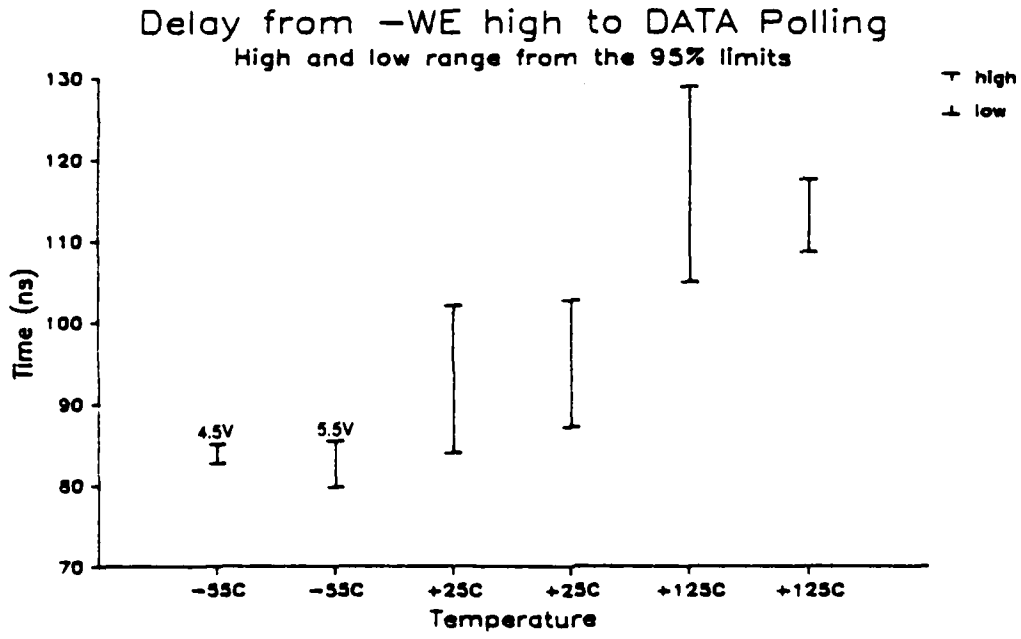


Figure 30: Delay Times (-WE High to DATA Polling) VS Temperature

10.5.1 Test Procedure

a. Byte write background data and verify.

b. Set the write pulse width to 15ns. Byte write complement of background data. Read and expect background data (anticipate that a write cycle did not occur).

c. If no failure, a write cycle did not occur, go to d.
A failure indicates that the minimum pulse width has been found.

d. Repeat b and c, increase the pulse width by 1.25ns every iteration until a failure occurs.

Nominal timing is used for the read and write cycle (except the write pulse width in b). VIL=0V, VIH=3V, VOL=VOH=1.5V.

10.5.2 Test Summary

Figure 31 is a high-low graph using the 95% limits for TWLWH in Tables 1, 2, and 3. As anticipated, the minimum pulse width increased as the temperature increased. None of the measured pulse widths were less than 20ns.

10.6 MINIMUM WRITE CYCLE TIME

The write cycle for EEPROMs actually consists of an automatic erase cycle before the desired data is written. For example, if 00001111 (0Fh) is written at address location 0, every bit at location 0 is automatically erased (floating gates stripped of electrons) before 0Fh is written. Based on theoretical calculations of charge transfer via tunnel current, the vendor has determined the maximum time to charge or erase the floating gate is 5ms. Since a write cycle consists of an erase cycle and a program cycle, the maximum write cycle time is 10ms.

DATA polling was used to measure the write cycle time. As was mentioned earlier, I/O7 will be the complement of the data written at bit 7, if the last address written is read while the internal write cycle is in process. The completion of the internal write cycle is detected when I/O7 reflects the true data. The write cycle time was considered the time from -WE signal high to the time when I/O7 switched from complemented data to true data.

In strict terms, the write cycle time is defined as the time from the falling edge of -WE for the first valid write cycle to the falling edge of -WE for the second

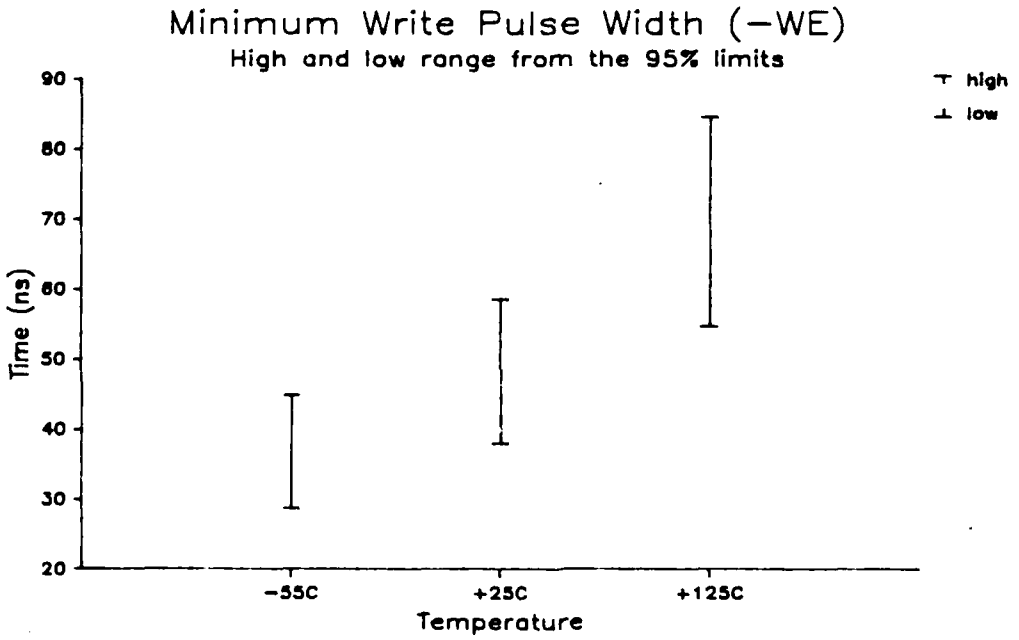


Figure 31: Minimum Write Pulse Width VS Temperature

valid write cycle. The data presented in this section is not the true write cycle time, as a delay is required from DATA polling finished (I/O7 reflects true data) to the falling edge of -WE to execute a valid write operation.

10.6.1 Test Procedure

a. Byte write and verify 00h at one location. Use nominal timing. The all 0's data pattern was used because the device will automatically erase (write all 1's) then write all 0's. Therefore, the all 0's data pattern should result in the longest write cycle time.

b. Set the output strobe start edge two access times (900ns) after the rising edge of -WE. Set the output strobe stop edge 50us after the rising edge of -WE.

c. Byte write 00h, wait one address access time (450ns), and perform a read cycle. Expect a "1" on I/O7 and don't care for the other outputs.

d. If no failure, the internal write cycle is in process. Repeat a through c, increase the output strobe stop edge by 50us every iteration.

e. A failure indicates that the internal write cycle has gone to completion. Read and expect 00h on I/O0 through I/O7. The write cycle time = time of output strobe stop edge minus time of -WE rising edge.

10.6.2 Test Summary

The 95% limits for TWLWL (see Tables 1, 2, and 3) are displayed in a high-low graph in Figure 32. The data indicates that a write cycle takes less than 10ms at all temperatures. Even with the 500us delay after DATA polling, another write cycle can be started within 10ms of the previous write pulse. This does not imply that the write cycle time can be measured, add a 500us delay, and use this number as a write cycle time in a design. This test is meant to show that write cycle times can be significantly decreased if DATA polling is implemented in the design and the component test program.

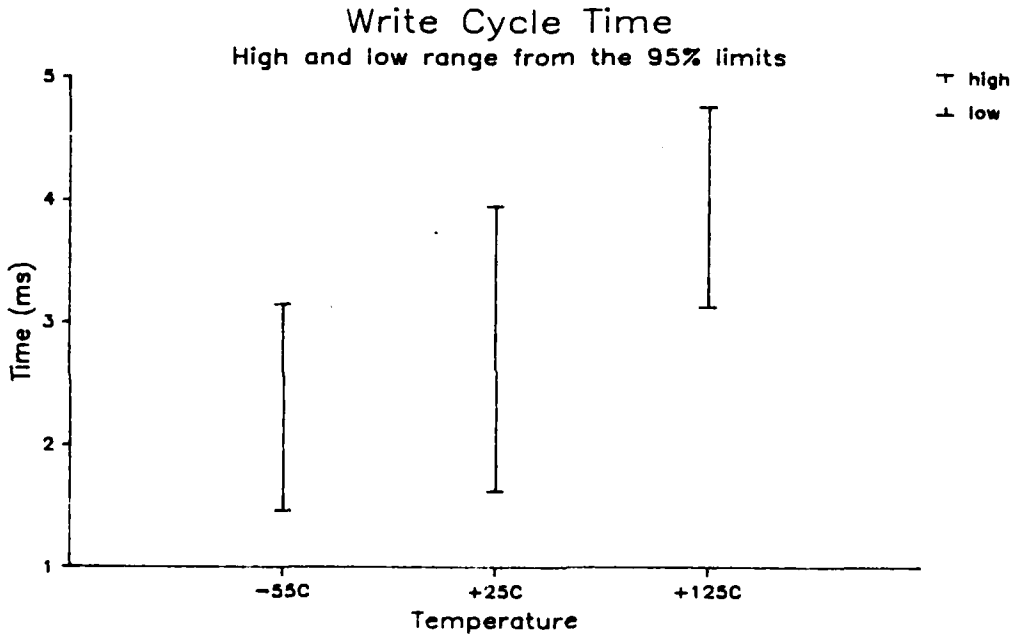


Figure 32: Write Cycle Time VS Temperature

10.7 NONVOLATILITY

An EEPROM must retain data when power is removed. The device's ability to retain data with no power (VCC=0) was tested on the 5588. The power was removed for 30 seconds as this was sufficient time for VCC to drop to 0V and it did not immensely increase the total test time of over 12 minutes. The power up and power down sequences are critical during this test to avoid inadvertent writes.

10.7.1 Test Procedure

This test was performed in the following manner.

a. VCC=4.5V; VIL=0V; VIH=2V; VOH=VOL=1.5V. Timing per the page mode write cycle. Write and verify a checkerboard by bit pattern. This pattern was selected because it proves the EEPROM memory cells can retain a "0" and a "1". Also, if a leakage path existed between two cells, it would be detected.

b. Output Enable, Chip Enable, and Write Enable = 2V.

c. Take address inputs to 0V.

d. Take data inputs to 0V.

e. Take Output Enable to 0V. As long as -OE is low, a write cycle cannot occur.

f. Take Chip Enable to 0V.

g. Turn off data drivers. I/O0 through I/O7 are floating.

h. Take Write Enable to 0V.

i. Take VCC to 0V.

j. Pause 30 seconds.

k. Take VCC to 4.5V.

l. Take Chip Enable and Write Enable to 2V.

m. The power up sequence of the remaining inputs is not important. Read the checkerboard by bit pattern. A failure indicates that the device did not retain data.

10.7.2 Test Results

All 36 devices retained data at the three temperatures. This test is a good screen for nonvolatility, but it does not verify the vendor's claim that the device will retain data for more than 100 years.

10.8 VERIFICATION OF MAXIMUM A.C. LIMITS

The following A.C. parameters were verified during a functional test using page mode.

- o Maximum time between two write pulses (byte load cycle) = 20us.
- o Maximum time in which 16 write pulses can occur (page load width) = 150us.
- o Maximum time from -WE low to data in valid (data valid time) = 300ns.
- o Minimum time from -WE low to -WE high = 50ns.

The checkerboard pattern was used and the test was executed with VCC at 4.5V and 5.5V. Other test conditions: VIH=2V; VIL=0.8V; VOL=0.4V; VOH=2.4V; and the outputs were loaded per section 8.2.

10.8.1 Test Summary

All devices passed at the three temperatures.

11. CONCLUSIONS

The objectives of this project were met in that the sample devices from Xicor, Inc. were characterized and the slash sheet for the 8K X 8 NMOS EEPROM was prepared. The device characterization can be summarized as follows:

- o All D.C. parametric measurements yielded results within the minimum or maximum limit specified in the proposed slash sheet. Care must be taken when testing at $-55^{O}C$ to minimize moisture condensation, which will increase the measured leakage currents.

- o This device can be rated in ESD category "B" (>2,000V).

- o Functional testing dominates the total test time due to the long write cycle time. Functional patterns should be revised to utilize DATA polling.

- o The measured access times were less than half of the specified 450ns at all three temperatures. SHMOO plots indicated that address access time is not sensitive to VCC.

- o The measured A.C. parameters for the byte write cycle were within the minimum or maximum limit specified in the proposed slash sheet.

- o A write cycle cannot be aborted once -OE is high, -WE low, and -CE is low.

- o The writes pulses generated by one edge of the Chip Enable signal and one edge of the Write Enable signal are not noise protected. Pulses narrower than 20ns may initiate a write cycle.

- o Most devices could not be mass erased with VCC at 4.5V. Some devices could not be mass programmed even though six programming pulses were applied. This is the only parameter which did not meet the specification.

- o VCC sense inhibits a write cycle if VCC is below 3V.

- o There are two important, unspecified timing parameters associated with DATA polling. The write recovery time, which is the time from DATA polling finished to the falling edge of the next write pulse, was found to be between 30us and 300us. The time from the rising edge of the Write Enable signal to the start of DATA polling was less than 150ns over temperature and power supply voltage.

- The minimum write cycle time was measured using DATA polling. The measured cycle time was less than half the specified 10ms over the military temperature range. This indicates that DATA polling can drastically reduce test time.

APPENDIX A

FUNCTIONAL ALGORITHMS

The functional algorithms described in the Appendix are test patterns which define the exact sequence of events used to verify proper operation of an electrically erasable PROM (EEPROM). Each algorithm serves a specific purpose for the testing of the device. These algorithms were applied to the device in a topologically pure fashion. During the functional test, the patterns were applied to the device in the order they appear in the Appendix.

PATTERN 1

Write all 0's, Read all 0's

The purpose of this pattern was to prove that page mode worked. Most of the other patterns were developed from this pattern. This pattern remained in the program because it preconditioned the device for GALPAT0.

Step 1 - Write "00" into a page. A page is defined by address lines A4 through A12, which are not changed during the page write.
Step 2 - Read "00" in the page under test.
Step 3 - Repeat steps 1 and 2 until all 255 pages have been tested.

PATTERN 2

GALPAT0 , DATA BACKGROUND = ALL "00"

This pattern tests for read disturbance. The byte under test is read alternately with other bytes in the same column and the same row. It is performed in the following manner:

Step 1 - Load memory with background data (done in the previous pattern).
Step 2 - Read location 0 (cell under test).
Step 3 - Read a location in the same row as the cell under test.
Step 4 - Repeat steps 2 and 3, sequentially reading all other locations in the same row as the cell under test.
Step 5 - Read location 0 (cell under test).
Step 6 - Read a location in the same column as the cell under test.
Step 7 - Repeat steps 5 and 6, sequentially reading all other locations in the same column as the cell under test.
Step 8 - Repeat steps 2 through 8 until every location has been the cell under test.

PATTERN 3

CHECKERBOARD

This pattern ensures every cell can be written to a "1" and a "0" and adjacent cells (which are programmed to the opposite state) do not affect the cell under test. It is desirable to have a checkerboard by bit, that is, every bit in every byte is programmed to the opposite state of the bits above and below it and the bits to the right and left of it. Page mode was used. It is performed in the following manner:

Step 1 - Write "AA" in all the columns of the even row numbers and write "55" in all the columns of the odd row numbers.
Step 2 - Sequentially read the entire memory across the rows.
Step 3 - Write "55" in all the columns of the even row numbers and write "AA" in all the columns of the odd row numbers.
Step 4 - Sequentially read the entire memory across the rows.

PATTERN 4

Write Alternating Columns of "00" and "FF" and Verify

This pattern loaded the data that was read during the A.C. parametric tests. Page mode was used.

Step 1 - Write "FF" into a page.
Step 2 - Read "FF" in the page under test.
Step 3 - Write "00" into the next page.
Step 4 - Read "00" in the page under test.
Step 5 - Repeat steps 1 through 4 until all pages have been tested.

PATTERN 5

Diagonal Read of Alternating Data (DRAD)

This pattern reads the data loaded during the previous pattern. DRAD has no write cycles, it only reads the data along the diagonals. This pattern was used during the measurement of the read cycle A.C. parameters. It generates worst case access times because the address decoders change every cycle and the data complements every cycle.

Step 1 - Read the diagonal starting at X=0, Y=0.
Step 2 - Read the diagonal starting at X=X+1, Y=0.
Step 3 - Repeat step 2 until X exceeds (XMAX/2) + 1. XMAX is the number of rows in the memory array.

PATTERN 6

BIT UNIQUE TEST

This pattern verifies that every bit within a byte is unique (two bits in a byte are not shorted). Page mode was used. It is performed in the following manner:

Step 1 - Write data = 00000001 (1 hex) in the entire device.
Step 2 - Sequentially read the device.
Step 3 - Write data = 00000010 (2 hex) in the entire device.
Step 4 - Sequentially read the device.
Step 5 - Write data = 00000100 (4 hex) in the entire device.
Step 6 - Sequentially read the device.
Step 7 - Write data = 00001000 (8 hex) in the entire device.
Step 8 - Sequentially read the device.
Step 9 - Write data = 00010000 (10 hex) in the entire device.
Step 10- Sequentially read the device.
Step 11- Write data = 00100000 (20 hex) in the entire device.
Step 12- Sequentially read the device.
Step 13- Write data = 01000000 (40 hex) in the entire device.
Step 14- Sequentially read the device.
Step 15- Write data = 10000000 (80 hex) in the entire device.
Step 16- Sequentially read the device.

PATTERN 7

GALPAT1 , DATA BACKGROUND = ALL "FF"

This pattern tests for read disturbance. The byte under test is read alternately with other bytes in the same column and the same row. Page mode was used. It is performed in the following manner.

Step 1 - Load memory with background data.
Step 2 - Read location 0 (cell under test).
Step 3 - Read a location in the same row as the cell under test.
Step 4 - Repeat steps 2 and 3, sequentially reading all other locations in the same row as the cell under test.
Step 5 - Read location 0 (cell under test).
Step 6 - Read a location in the same column as the cell under test.
Step 7 - Repeat steps 5 and 6, sequentially reading all other locations in the same column as the cell under test.
Step 8 - Repeat steps 2 through 8 until every location has been the cell under test.

PATTERN 8

MARCH DATA, DATA BACKGROUND = ALL "FF"

This pattern tests for address uniqueness and multiple selection. Byte write was used. It is performed in the following manner:

Step 1 - Load memory with background data.
Step 2 - Read location 0.
Step 3 - Write data complement in location 0 (byte write cycle).
Step 4 - Repeat steps 2 and 3 for all other locations in memory (sequentially).
Step 5 - Read data complement at location 0.
Step 6 - Write data at location 0 (byte write cycle).
Step 7 - Repeat steps 5 and 6 for all other locations in memory (sequentially).

TABLE OF CONTENTS

64K SRAM

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1. SUMMARY

1.1 OBJECTIVES/RESULTS

The objectives of this portion of the contract with Rome Air Development Center were as follows:

- o Develop and refine a test philosophy for 64K (8K X 8) CMOS Static RAMs which can be used for preparing a MIL-M-38510 detail specification.
- o Perform an electrical characterization on a sample group of devices over the military temperature range
- o Generate a draft MIL-M-38510 slash sheet specification for the Static RAM using characterization data as a basis for establishing performance limits.

This report documents the results of the electrical characterization on Advanced Micro Devices (AMD) Am99C88-10DM (100ns) CMOS SRAM and the Toshiba TC5564PL-15 (150ns) CMOS SRAM. Full AC and DC electrical testing was performed over the military temperature range.

AMD guarantees the Am99C88-10DM to meet or exceed MIL-STD-883C only, but does not recommend this device for MIL-M-38510 status. In the first quarter of 1987, AMD will offer a 45ns, Am99C88H 8K X 8 SRAM, which they may recommend for MIL-M-38510.

In summary, the devices performed as expected, per the proposed slash sheet, with the exception of functional and A. C. parametric failures at VDD = 5.5V at $-40^{o}C$ and $-55^{o}C$ for one of the two AMD devices.

Details and test data, documenting the above findings, are presented and summarized in this report.

2. INTRODUCTION

2.1 OBJECTIVES

The major objective of this effort was to establish the electrical characteristics of the CMOS 64K (8K X 8) Static RAM and use this data to develop a preliminary MIL-M-38510 slash sheet. In general, the effort involved:

- o Memory market survey to determine production status of candidate devices.
- o Selection and procurement of candidate device types for characterization.
- o Development of test procedures compatible with automatic test systems.
- o Determine and verify parametric limits through device characterization.
- o Development of a preliminary slash sheet based on device testing and vendor information.

2.2 BACKGROUND

The vendor survey, performed during test development phases of the contract, identified six potential 64K (8K X 8) CMOS Static RAMs as potential candidates for the MIL-M-38510 specification. Of the six vendors, only two, AMD and National, were selected, based on their promised availability of samples, data sheets, and actual production schedules. However, through the remainder of the contract period, both vendors incurred repeated delays in delivering samples and data sheets, and in meeting production start dates. This was due to low yields, which required both vendors to make adjustments to their new CMOS processes.

To counteract these problems, twelve TC5564PL-15 (150ns) full CMOS, -30°C to +85°C 8K X 8 SRAMs from Toshiba, a Japanese vendor, were obtained. These samples were used for program development and attempted device characterization over the full military temperature range. At the beginning of the last three months of the contract, National could not deliver any parts or data sheet to military specifications. AMD was only able to deliver two engineering samples and a data sheet to military specifications.

Thus, the preliminary slash sheet was eventually developed and released to RADC, based on the limited characterization of the Am99C88-10DM (100ns) CMOS SRAM.

2.3 SUMMARY

AMD guarantees the Am99C88-10DM to meet or exceed MIL-STD-883C only, but does not recommend it for MIL-M-38510 status. In the first quarter of 1987, AMD will offer a 45ns, Am99C88H 8K X 8 SRAM, which they may recommend for MIL-M-38510.

3. DESCRIPTION OF DEVICE TYPE

3.1 GENERAL ASPECTS OF 64K SRAMS

The 64K SRAM is a 5 volt only, 65,536-bit Static Random Access Memory, utilizing CMOS technology. The device is organized as 8192 words by 8 bits. The by 8, or bytewide, configuration is intended primarily for use with byte oriented microprocessor systems. The four-line (-E1, E2, -G1, and -W) control and JEDEC-approved 28-pin package assures easy microprocessor interfacing and minimum design efforts when upgrading, adding or choosing between RAM, ROM, and EPROM devices. The JEDEC 8K X 8 SRAM pinout is shown in Figure 1. To upgrade to a 32K X 8 SRAM, pin 1 (NC) and pin 26 (E2) become A14 and A13, respectively.

3.2 ASPECTS OF SPECIFIC DEVICE TYPE

The Am99C88 Chip Enables (-E1 and E2) provide a low power standby mode, when the device is deselected. Control pins -G and -W facilitate read and write operations, respectively, and along with the tri-state data inputs/outputs, allow similar devices to be connected to a common bus.

The device features a data retention mode, whereby data is retained at VDD as low as 2V. When controlled by -E1 or E2, all other inputs are tri-stated, thus preventing input levels from exceeding the VDD rail as it is reduced to 2V.

3.3 SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS SRAMs require careful decoupling of the devices. The supply current, IDD, has three segments that are of interest to the system designer: the standby current level, the active current level and the transient current peaks that induce noise on the VDD/GND line. It is recommended that a 0.1uF ceramic capacitor, between VDD and GND, be used on every device. In addition, a 4.7uF bulk electrolytic capacitor, between VDD and GND, should be used for every eight devices. The purpose of the bulk capacitor is to overcome the voltage droop caused by inductive effects of the PC board traces.

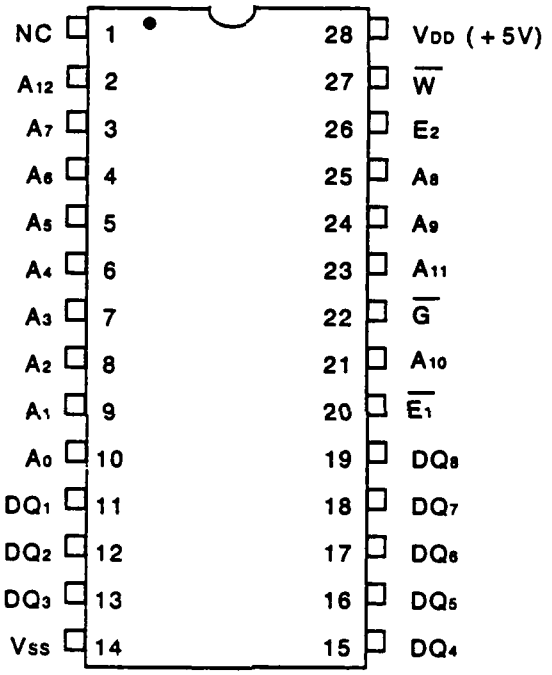


Figure 1: Terminal Connections

4. DEVELOPMENT OF AUTOMATIC AND BENCH TESTS

4.1 AUTOMATIC TEST EQUIPMENT

The test equipment used to characterize the 64K SRAM is a Fairchild Xincom 5588 Automatic Test System. The system's main processor is a Zilog Z8000 microprocessor. This processor handles all test sequences and test processes. Included in the system is a subsystem which is called the Test Pattern Computer (TPC).

The TPC is a modular subassembly which can be loaded with a microprogram and subsequently outputs the data and address patterns for the purpose of testing memory devices. The TPC has the capability to microprogram an assortment of test patterns. These include such popular industry standards as Checkerboard, March, and Masest, as well as other patterns that produce special effects on the DUT to evaluate specific circuit capabilities or constraints. Patterns are defined by a set of 48-bit microcoded instructions executed within the TPC at functional rates up to 25MHz (40ns cycle time). Upon command from the main processor, the TPC generates the desired pattern and sends this pattern to the system to drive the input pins and check the output pins for the proper data.

Some additional features of the TPC are:

- o ECL Construction
- o Topological Address Scrambler
- o Address Indexing, Refresh Testing, Butterfly Patterns
- o Truth-Table RAM (Pattern RAM For EPROMS)
- o Algorithmic Pattern Generation
- o Loop Counters
- o Timing Set Selection on-the-fly

In addition to the TPC other system capabilities include:

- o 14 programmable clock phases
- o 4 programmable power supplies
- o 24 address lines
- o 16 data comparators
- o Parametric Measurement Unit (PMU)
- o Advanced Error Logging System (AELS)
- o IEEE 488 Bus Interface
- o Color Computer Graphics Display
- o Auto Data Logging to Data General Eclipse Host Computer

To interface the device under test (DUT) to the test system, an interface board is used to electrically connect the DUT's pins to the specific test system pin electronic cards. A zero insertion force socket is used to allow for fast removal and in ertion of the DUT without causing lead damage.

4.2 BENCH TEST EQUIPMENT

Some non-ATE instruments were required to perform the Electrostatic Discharge and Capacitance Measurement tests.

The Electrostatic Discharge test unit used is an IMCS Corporation, Model number 2400C.

Features include:

- o 0-10,000 Volt Continuously Adjustable
- o 4.5 Digital Display of HV
- o Programmable Pulse Sequence
- o Curve Tracer Output

- o 1-128 pin Configuration
- o Applicable to Mil-STD-883 and MIL-STD-1686

The Capacitance Analyzer used is a Hewlett Packard, Model number 4192A, probe model number HP-16048C.

Features include:

- o 5Hz to 13MHz variable measuring frequency
- o Gain-Phase measurement: amplitude, phase and delay
- o Floating or Grounded devices
- o Frequency accuracy +/- 50ppm

5. STATIC CHARACTERISTICS

5.1 OBJECTIVES

During this characterization, several goals were set forth. One of these was to reliably and efficiently characterize the D.C. parameters of the 64K SRAM device. This was accomplished by utilizing Automatic Test Equipment (ATE). This equipment can reliably execute a group of measurements and test conditions with accuracy and repeatability.

5.2 TEST METHODS

The Xincom 5588 memory test system was used to collect data on the D.C. parametric measurements. The tester allowed data to be taken on each device in an accelerated and accurate manner. The desired sample size for the D.C. measurements was 36 devices. By using a typically larger sample size, one can average measurement values to get a basic feel for the "trend" or average values for a specific parameter. However, due to a lack of domestic vendors during the contract, the actual sample size was considerably reduced. Twelve Toshiba TC5564PL-15 (150ns), $-35^{o}C$ to $+85^{o}C$, devices were first tested to aid in establishing a "trend" in device performance over the $-55^{o}C$ to $+125^{o}C$ military temperature range. Later, in the final three months of the contract, two AMD Am99C88 military temperature engineering samples were received and tested; the proposed slash sheet is based on the characterization of these two samples.

The tests performed on the Xincom were: IIH, IIL, IOZH, IOZL, VOH, VOL, IDD, IDD1, ISB, ISB1, and ISB2 parameters. The test temperature sequence was $+25^{o}C$, $+70^{o}C$, $0^{o}C$, $+85^{o}C$, $-40^{o}C$, $+125^{o}C$, $-55^{o}C$, and ending at $+85^{o}C$. This sequence prevented moisture from condensing on device and socket pins, which thus eliminated erroneous leakage current measurements. Note that every test was performed at each temperature and worst case voltage.

5.2.1 IIH, IIL TEST

The IIH and IIL tests are done to determine the amount of current drawn when the inputs have a specified voltage applied to them. This test is conducted by driving an input high and low and measuring the resultant current. Test levels for this parameter were Vin = 0V (for IIL) and Vin = 5.5V (for IIH), with VDD = 5.5V. To induce the worst case input leakage on a device pin at Vin = 0V or 5.5V, all other input pins were forced to the opposite state of 5.5V or 0V, respectively, during the test. The worst case condition for leakage on a device pin is when Vin equals 5.5 volts.

Leakage measurements were performed in the temperature sequence stated in section 5.2. The specified limits were +/- 2uA for AMD and +/- 1uA for Toshiba. In general, all measurements yielded extremely low currents of 33nA or less for AMD over the full temperature range. Toshiba device #12 failed IIH at +125^{o}c for two pins (A10 and -OE). Currents of these magnitudes are typical in LSI devices using CMOS technology.

5.2.2 IOZH, IOZL TEST

This test measures the output leakage current when the outputs are in the high impedance state. The procedure for this test is to set the device's outputs in the high impedance state by applying a logic "1" to either -E1 or -G or a logic "0" to E2 input pins. A voltage is then forced on the output under test and the resultant current is measured.

Two forcing voltages are applied. In the IOZH test, 5.5 volts are applied and in the IOZL test, 0 volts are applied. During this test, VDD is set to 5.5 volts which is the worst case condition.

As in the IIH and IIL test (section 5.2.1), the specified limits were +/- 2uA and +/- 1uA, respectively, for AMD and Toshiba. In general, all measurements yielded extremely low currents of 40nA or less for AMD over the full temperature range.

5.2.3 VOH, VOL TEST

This test is performed to measure the resultant voltage level on the output when driving a load. For this test, currents are forced into the output and the resultant voltage is measured. The forcing current used for the VOH test is -2mA and -1mA, respectively, for AMD and Toshiba, with VDD equaling 4.5V. The current used for the VOL measurement is 4mA for both vendors with VDD equal to 5.5V. Note that VDD is raised to 5.5 volts when measuring the low output voltage level and is reduced to 4.5 volts when measuring the high output level.

The average values versus temperature are plotted in Figures 2 and 3. Note that in both tests the maximum VOL (max VOL=0.4V) and the minimum VOH (min VOH=2.4V), as specified in the proposed slash sheet, were never exceeded.

5.2.4 IDD, IDD1, ISB, ISB1, ISB2 TEST

This test measures the amount of supply current required by the device for five different operating modes. The first two modes are device active (IDD, IDD1). These modes are the typical operating modes when the device is being accessed. The other three modes are standby (ISB, ISB1, ISB2). During standby the device's maximum active current can be reduced by almost 100%.

The operating supply current is categorized into two current levels: static and dynamic. Static current, IDD, is measured with inputs at D.C. levels. Dynamic current, IDD1, with inputs using general address and data formats and timing levels, is measured at the device's minimum cycle time (100ns for AMD and 150ns for Toshiba). For these tests, VDD = 5.5V, VIH = 2.6V, and VIL = 0.4V. Dynamic current, IDD1, is greater than static current, IDD, and is also pattern dependent. It was determined that a Galloping Columns test pattern produced the greatest dynamic IDD1 current. For AMD, the measured static operating currents were approximately 59% to 73% of the measured dynamic operating currents. However, for Toshiba, under the same test conditions, the static operating currents were approximately 1.8% to 3% of the dynamic operating currents.

Standby mode is categorized into two current levels, depending on whether it is established with -E1 and E2 at TTL or CMOS input drive levels. When in the standby mode, the outputs are in the high impedance state, independent of the -G input. The standby current, ISB, is established with -E1 at TTL logic "1" = 2.2V and E2 at TTL logic "0" = 0.8V, which gives the highest current measurement. All other inputs are at VIH = 2.6V and VIL = 0.4V. The ISB1 and ISB2 standby currents are established with -E1 at CMOS logic "1" = VDD-0.2V and E2 at CMOS logic "0" = 0.2V, which give the lowest current measurements. ISB1 is controlled by -E1 and ISB2 is controlled by E2. All other inputs are at VIH = 2.6V and VIL = 0.4V. In general, the resultant measured and recorded standby currents yielded values of 32nA or less, which are typical of CMOS technology.

Refer to Figure 4 (Static Operating Supply Current) and Figure 5 (Dynamic Average Operating Current) for measured AMD values.

All worst case standby and operating supply currents occurred at -55^{o}C. In all cases, the measured values were well within their maximum limits as specified in the proposed slash sheet.

5.3 TEST SUMMARY

The measured D.C. parameters were within the maximum and minimum limits set by the proposed slash sheet.

- o VOL changed significantly with changes in temperature.
- o VOH changes were negligible with changes in temperature.
- o Input and output leakage currents are the greatest at VIH and VOH levels, respectively.
- o Standby currents are negligible, regardless of whether -E1 or E2 is used to deactivate the chip, or when either -E1 or E2 are at TTL or CMOS input levels.
- o The Galloping Columns test pattern generated the largest dynamic supply current.

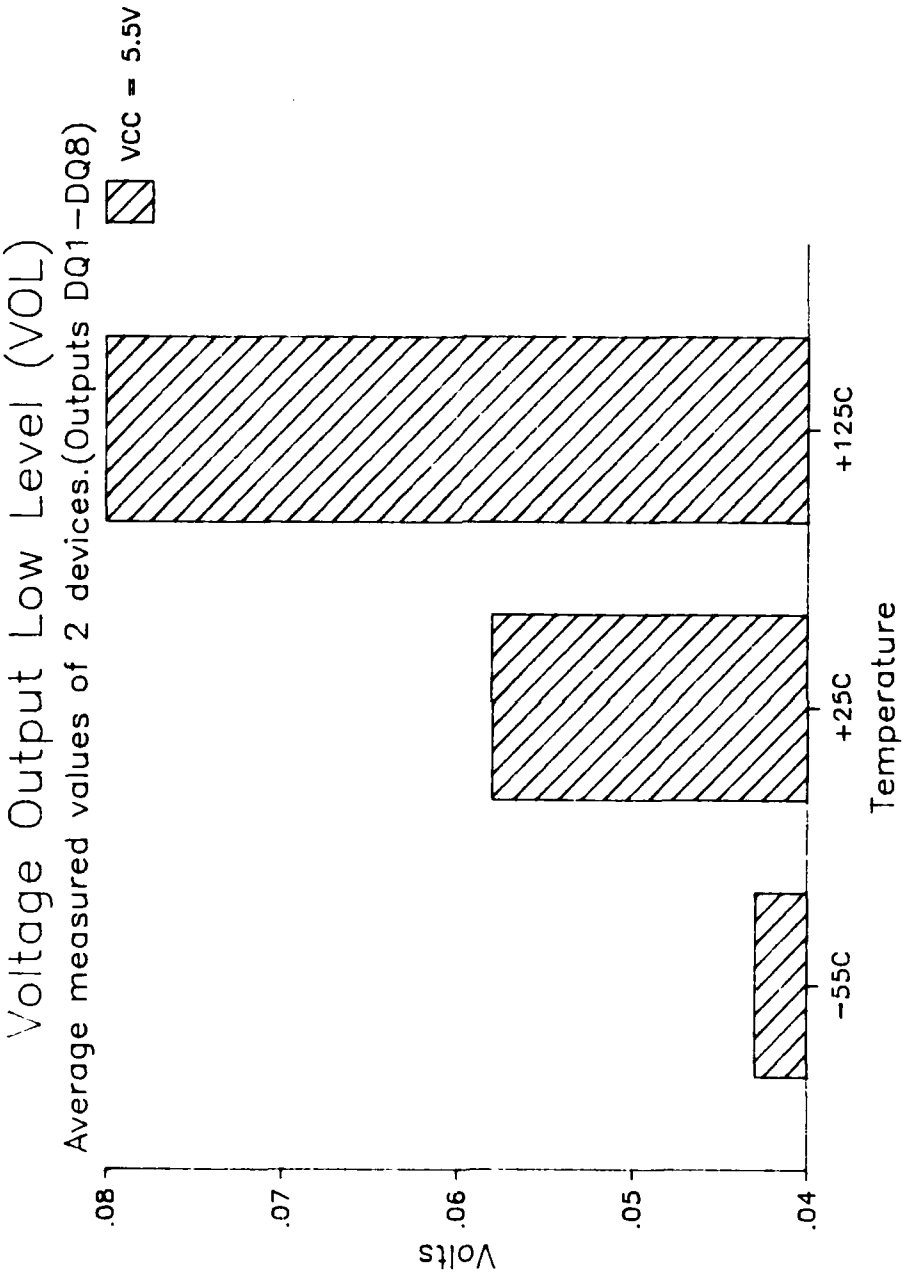


Figure 2: Voltage Output Low Level (VOL)

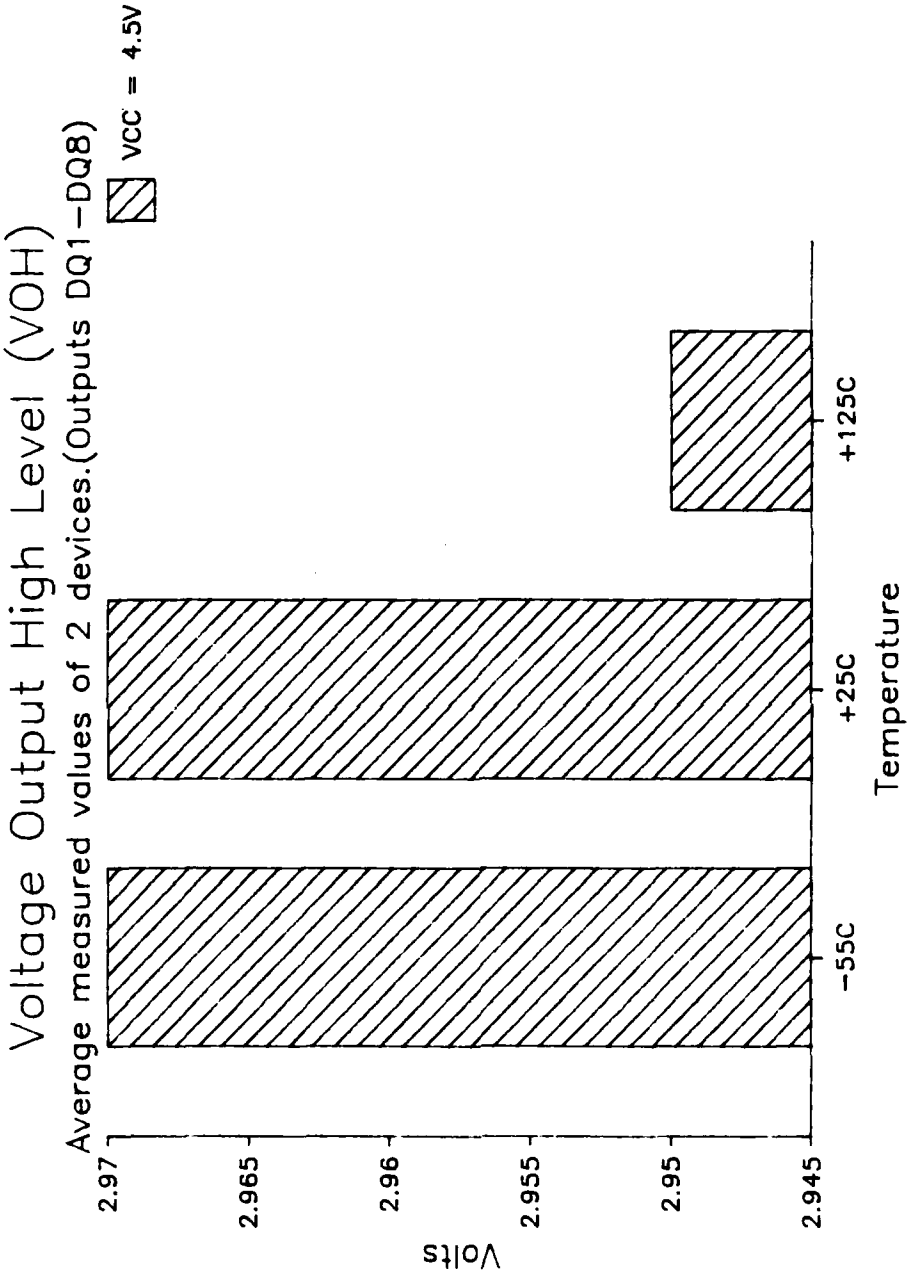


Figure 3: Voltage Output High Level (VOH)

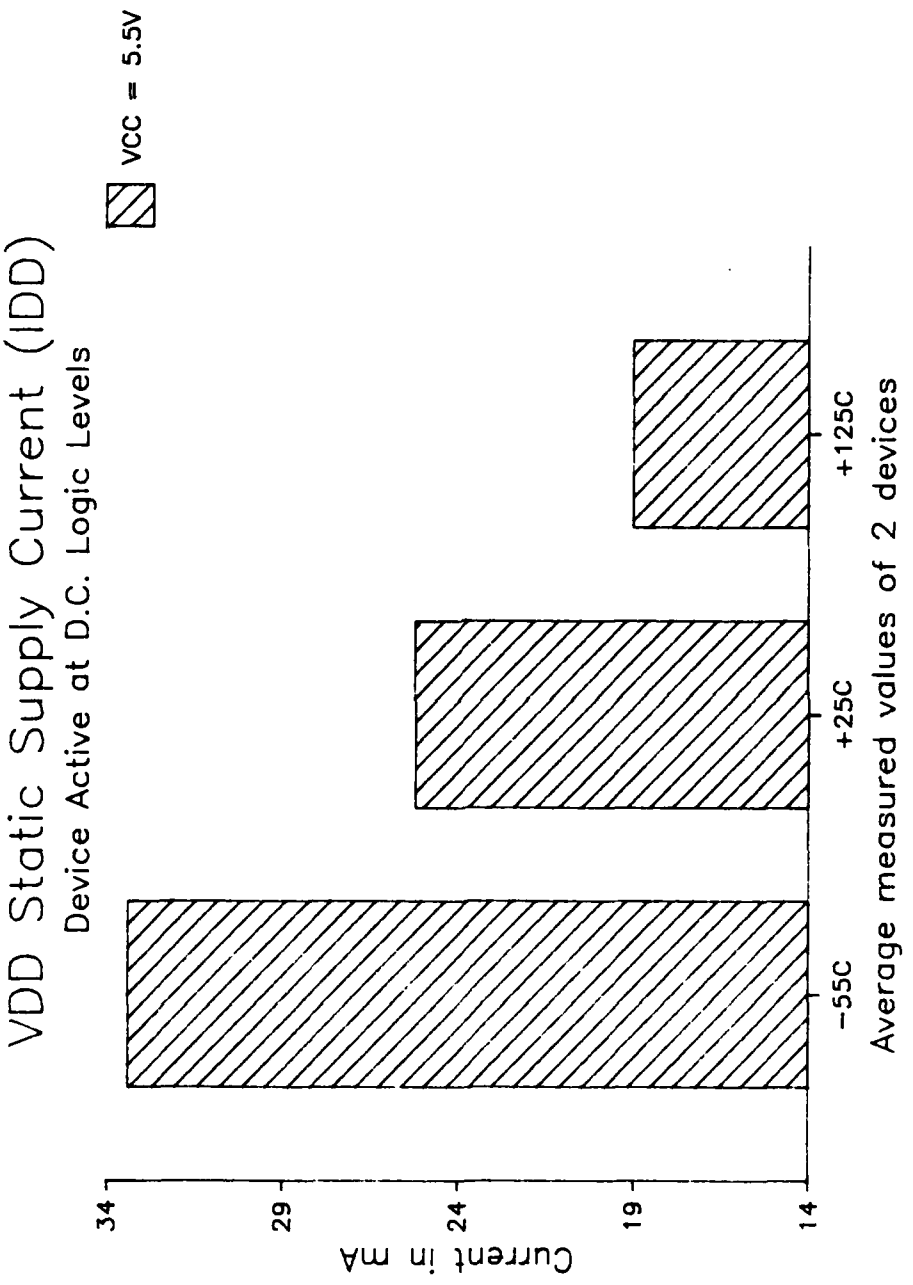


Figure 4: VDD Static Supply Current (IDD)

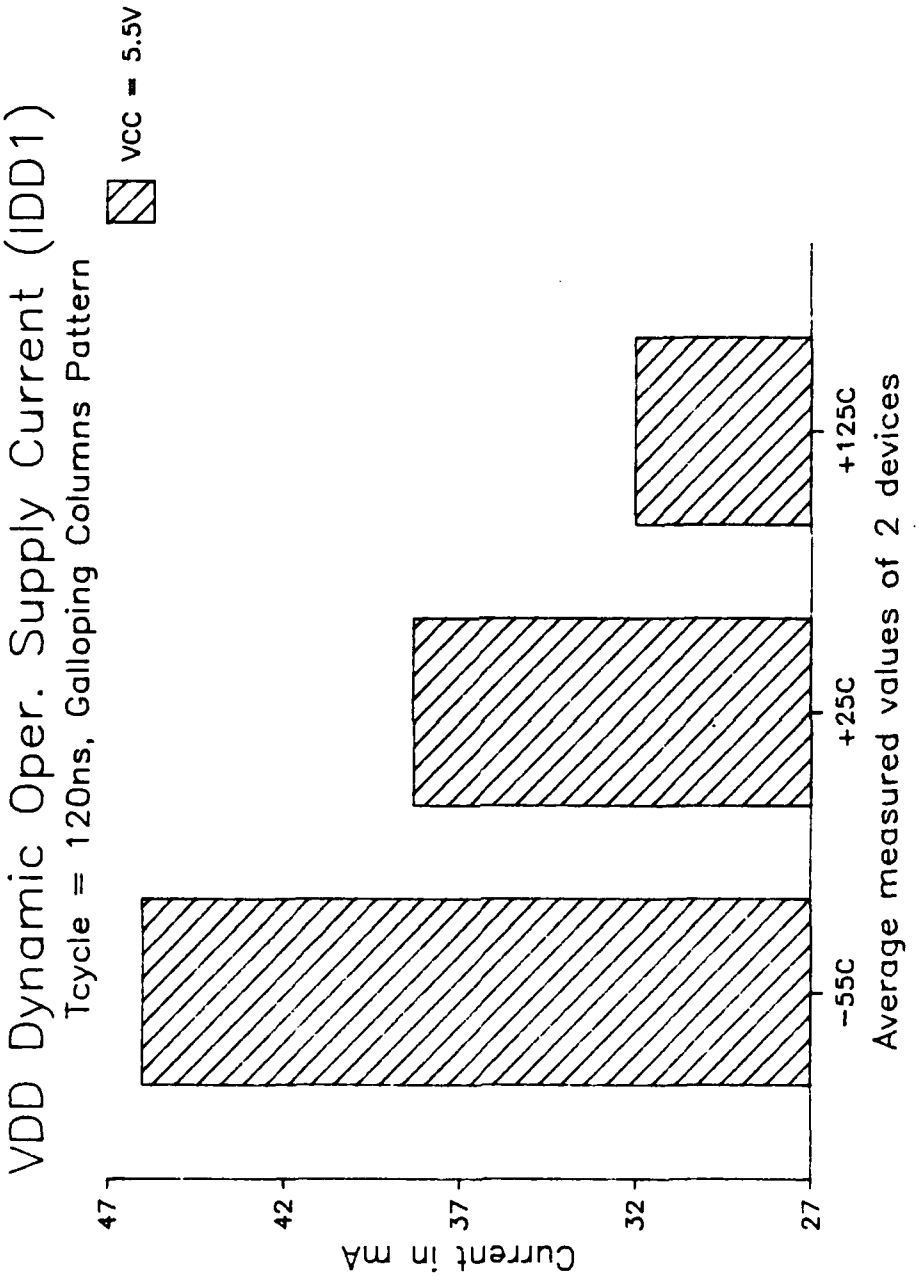


Figure 5: VDD Dynamic Operating Supply Current (IDD1)

6. INPUT / OUTPUT CAPACITANCE MEASUREMENTS

6.1 TEST METHODS

Capacitance measurements were performed on the two AMD Am99C88 and six Toshiba TC5564 devices. Both input and output pin capacitance measurements were made. The procedure used was to place the capacitance meter on the input/output pin and measure its capacitance with respect to the device's ground pin. During testing, all pins not under test are left open.

The meter parameters were set as follows:

Frequency = 1MHz
AC RMS amplitude = 50 millivolts
DC bias = 0 volts
Parallel equivalent circuit

Refer to MIL-STD-883C method 3012.1.

6.2 TEST SUMMARY

As a result of the measurements between both vendors' devices, the data showed that the devices did not have a uniform capacitance with respect to adjacent pins. However, for each vendor, the same device pin number for all devices had nearly uniform measurements. Referring to Figure 6, this graph shows that input pins 20 (-E1), 26 (E2), and 27 (-W) have consistently higher capacitance values than their adjacent inputs. As specified in the proposed slash sheet, the maximum input capacitance for AMD is 8pF. In all cases, the measured values were below this value. Measurements for TC5564 devices were less than Toshiba's input capacitance value of 10pF.

As compared to the inputs, the measured output capacitance among both vendors' devices was higher. Referring to Figure 7, the test results showed the devices did not have a uniform capacitance between adjacent pins. Output pin 13 for both devices had the highest measured value. For AMD, the proposed slash sheet value is 8pf; measurements were below this value. Measurements for TC5564 devices were below the Toshiba maximum specification of 10pF.

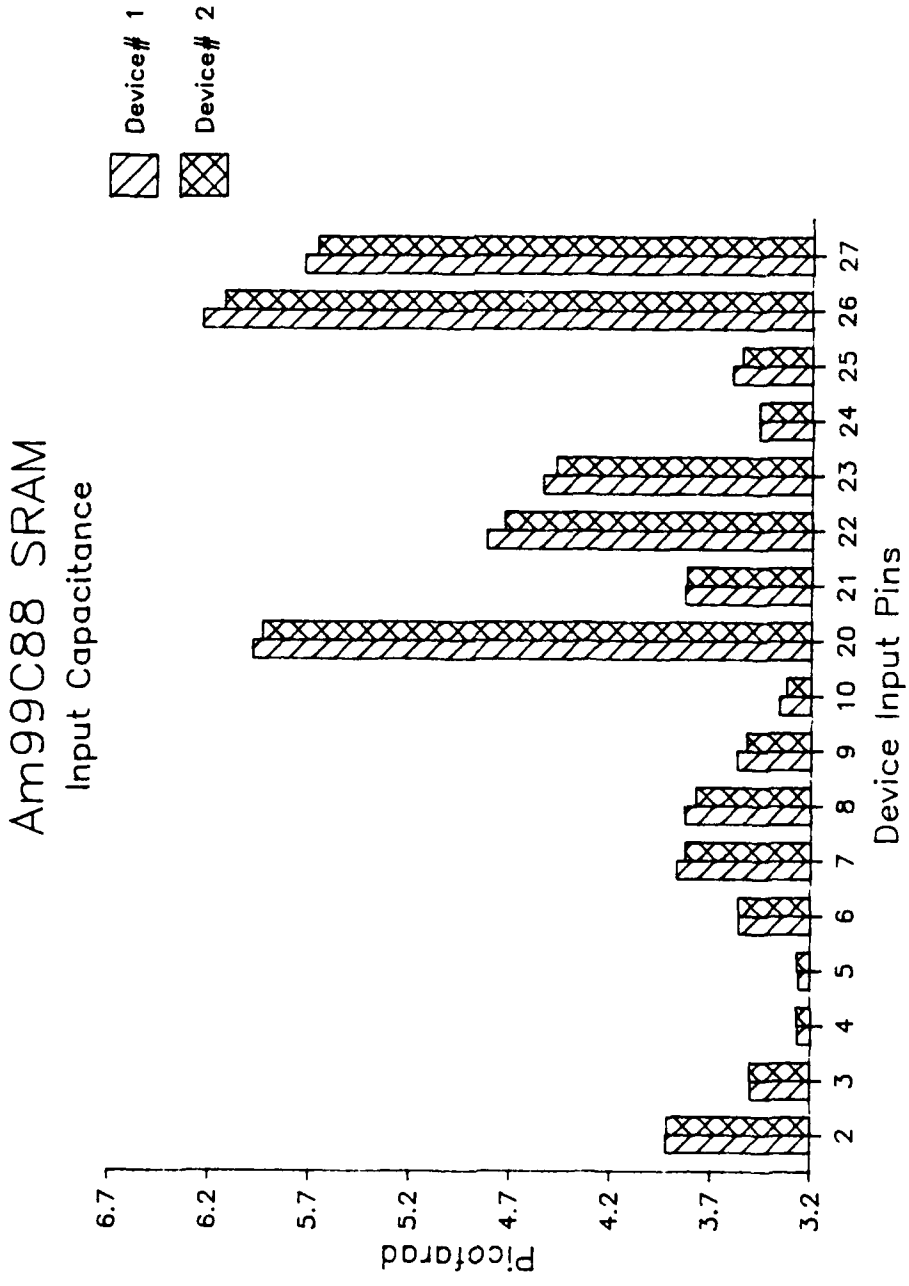


Figure 6: AMD Input Capacitance Measurement Devices 1,2

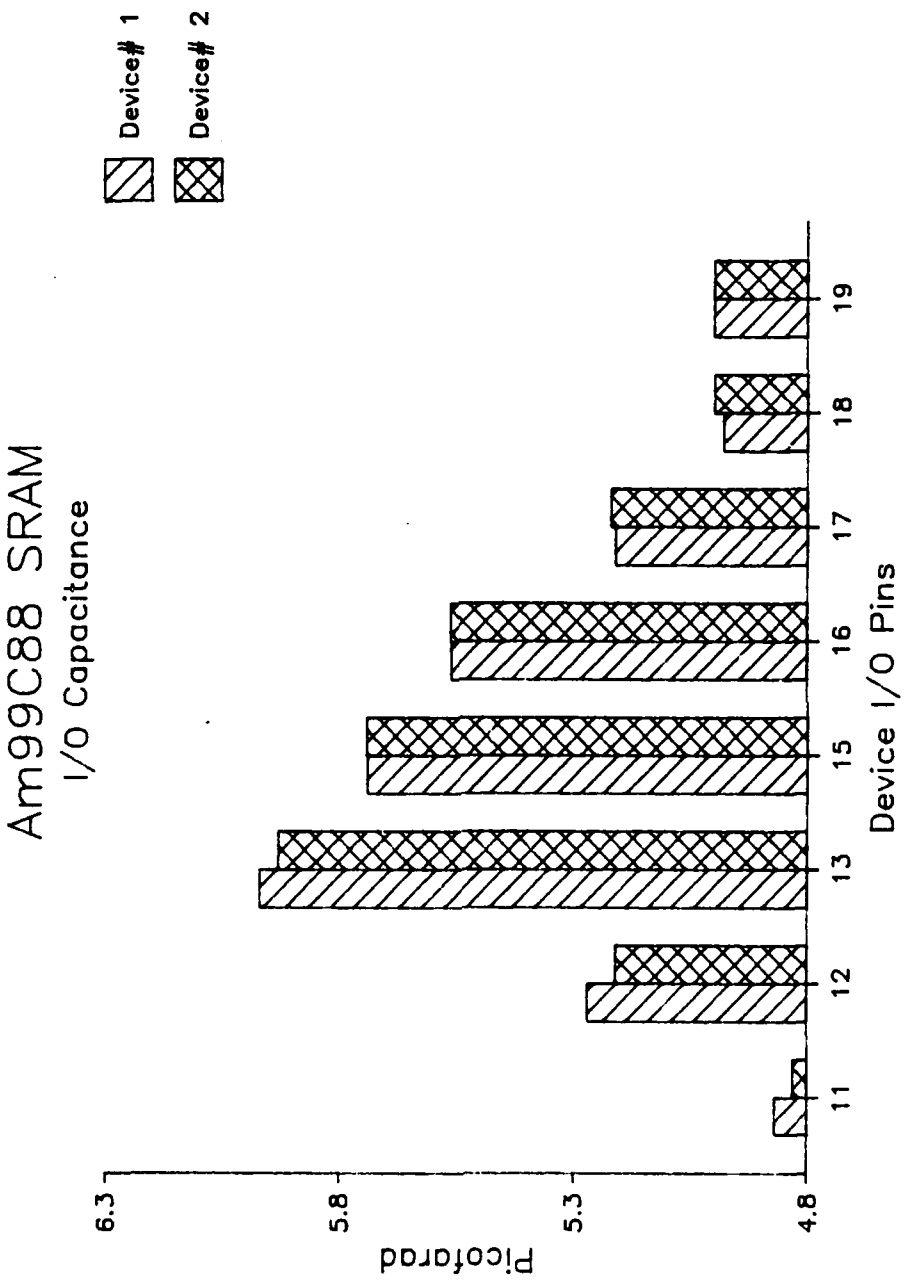


Figure 7: AMD Output Capacitance Measurement Devices 1,2

7. ELECTROSTATIC DISCHARGE, VZAP TESTS

7.1 TEST METHODS

This test is performed to measure the electrostatic discharge sensitivity of a device's input pins. Testing is performed in accordance with MIL-STD-883C method 3015.2 on an ESD simulator. After each exposure to an ESD pulse, the device is analyzed on an ATE system for leakage parameters.

7.2 TEST SUMMARY

Since this test can be electrically destructive to the device under test, it was decided not to perform this test due to the small sample size from AMD (2) and Toshiba (12). The necessity to use the devices in other D.C. and A.C. characterization testing outweighed the necessity for ESD testing. Also, due to the late arrival of these samples from the vendors, the time to perform this test could not be justified.

8. DYNAMIC CHARACTERISTICS

8.1 TEST METHODS

The Xincom 5588 memory test system was also used to perform A.C. Functional Tests and A.C. Timing Measurements on each device. Each device was characterized over the $-55^{o}C$ to $+125^{o}C$ temperature range. The temperature sequence was the same as stated in Section 5.2. All testing was performed first at VDD = 4.5V, then repeated for VDD = 5.5V. During these tests, a load circuit was connected to each I/O pin. This circuit can be found in Figure 8.

During the majority of the contract period, a firm commitment to a minimum cycle time of the expected samples was unavailable. Therefore, it was decided to create two test program versions in a parallel effort. One version was set for a 120ns cycle time and the other version for a 150ns cycle time. The two AMD Am99C88-10DM samples are 100ns devices and were tested to the 120ns program. There was insufficient time to change the program timing edges to 100ns cycle timing. However, this ran the device only 20ns slower during the functional pattern sensitivity tests. The twelve Toshiba TC5564PL-15 samples are 150ns devices and were tested with the 150ns version program.

8.1.1 Timing Symbols and Definitions

The Toshiba samples and data sheet were received first. Therefore, all symbol names for the timing parameters shown in the following referenced timing diagrams, datalogs, and SHMOO plots are with respect to the Toshiba data sheet. These symbol names are cross-referenced to the AMD symbol names in the timing diagrams of Figures 11 and 12. The AMD symbol names were also used in the proposed slash sheet.

The timing symbols and definitions are listed in the sequence in which they were used in the test programs as follows:

TAVQV (TAA)	Address access time
TE1LQV (TCO1)	-E1 Chip enable access time
TE2HQV (TCO2)	E2 Chip enable access time
TGLQV (TOE)	-G Output enable access time
TWLWH (TWP)	-W Write pulse width
TWHAX (TWR)	Address write recovery time
TWHAX (TWR1)	-E1 Write recovery time
TE2LAX (TWR2)	E2 Write recovery time
TWHDX (TDH)	Data hold after end of write
TAVWH (TAW)	Address setup to end of write

TAVWL (TAS)	Address setup before write enable low
TE1LWH (TCW1)	-E1 Chip enable to end of write setup time
TE2HWH (TCW2)	E2 Chip enable to end of write setup time
TDVWH (TDW)	Data setup to end of write
TAXQX (TOH)	Output hold after address change
TE1LQX (TLZ1)	-E1 Chip enable to output active time
TE2HQX (TLZ2)	E2 Chip enable to output active time
TGLQX (TOLZ)	-G Output enable to output active time
TE1HQZ (THZ1)	-E1 Chip enable to output disable time
TE2LQZ (THZ2)	E2 Chip enable to output disable time
TGHQZ (TOHZ)	-G Output enable to output disable time

8.2 A.C. FUNCTIONAL TESTS

This section of the test program contains four types of tests: pattern sensitivity, data retention, bit-unique, and slow cycle. These four types of tests are pass/fail, and the results are in the form of the appropriate pass/fail messages. The timings for these tests, with the exception of the slow cycle test, are shown in the Functional Write Cycle timing diagram of Figure 9 and the Functional Read Cycle timing diagram of Figure 10 for the 120ns program version. For both cycles, the format for Addresses is XYBAR, XY, XYBAR and the format for input Data is DBAR, D, DBAR. These formats were created to provide worst case operation. That is, complement addresses occur before and after valid addresses and complement data occur before and after valid data, all within each cycle. Valid addresses are XY and valid data are D.

The Write and Read cycles exist as individual timing sets in the test program. In Figures 9 and 10, the symbol names PH1 through PH9 are Xincom 5588 timing generator edges, used to create addresses, input data, the -E1, E2, -G and -W controls, and the strobes to read output data from the device. PH1 and PH9 form the addresses for the XYBAR, XY, XYBAR format (Read and Write cycle), and DIE (PH8), DIN (PH2) and DIN (PH14) form the DBAR, D, DBAR format (Write cycle only) for the I/O pins. Write and Read cycles are implemented in certain sequences, depending on the pattern used. The Write and Read timings for these four types of tests are fixed, and the Read strobe is set close to the specified Address and Chip Enable access times.

The input threshold levels are VIH = 2.6V and VIL = 0.4V. The output comparator sense levels are VOH = 2.4V and VOL = 0.4V. These are worst case device specification levels, which are guard-banded to eliminate the effect of A.C. noise created by the Xincom test head and device adapter board.

The above referenced timing and threshold levels were all verified with an oscilloscope.

8.2.1 Pattern Sensitivity Tests

A wide variety of address sequence and data patterns were used in the evaluation of the devices to determine if there was any specific sensitivity within the device or if there was any interaction or crosstalk between sections of the on-chip circuitry. These tests include such data patterns as Checkerboard, and X and Y Parity, with address sequences including Up and Down Count, Address Complement, Surround Disturb, and March. These patterns and sequences were combined in various ways along with timing and voltage variations to evaluate each device's capabilities. Patterns 1 through 10, listed in the Appendix to this part of the report, were supplied in sequence to the device. Included is a description of Patterns 1 and 4.

8.2.2 Data Retention Test

This test checks the retention of data when VDD is reduced to VDDR = 2V. After being at VDDR = 2V for a length of time, the VDD supply is returned to a 4.5V or a 5.5V level, and the pattern is read to verify that no data was lost.

For this test, a checkboard pattern was written into the device at VDD = 4.5V. Then, in sequence, E2 was decreased from 2.4V to 0.2V and VDD was decreased to 2.0V, such that E2 never exceeded VDD. During this sequence, E2 automatically tri-states all other device inputs so that they do not exceed VDD. The device is powered down for 5 seconds (the length of time to decrement an internal tester register). The device is powered up in the reverse sequence (E2 increased after VDD is increased). The pattern is then verified. The test is repeated for VDD = 5.5V.

This test gives only a go-no-go assessment of data retention properties of the device. Due to a shortage of time, the Data Retention D.C. and A.C. parameters were not measured.

8.2.3 Bit-Unique Test

This test supplies a One-Zero pattern to the device, which verifies that every bit within a byte is unique (two bits in a byte are not shorted). The data written into the DUT for the bit being tested is the complement of the other seven bits. This pattern is described in detail in the Appendix to this part of the report. This test is performed at VDD = 4.5V and 5.5V.

8.2.4 Slow Cycle Test

This test checks for lost data due to long time intervals between Read and Write cycles. The timing is the same as shown in Figures 9 and 10, except that the Read Cycle time is extended to 10us, and the trailing edges of addresses, chip enables, and output enable are extended to 9.8us. The 20ns comparator strobe is delayed to 9.6us. A checkerboard pattern is used during this test.

8.3 A.C. TIMING MEASUREMENTS

The twenty-one timing parameters, listed in section 8.1.1, were measured in this test section using the A.C. characterization Write and Read Cycle Timing diagrams of Figure 11 and Figure 12. Each cycle exists as a unique timing set in the test program, and each is used in sequences determined by the test patterns supplied to the device. These timing sets are similar to those of Figures 9 and 10, except that each test cycle is extended to 600 ns to create nominal timing relationships, while a particular timing parameter is being measured. This technique guarantees that as the selected parameter is adjusted toward its operating limit, a failure is due to that parameter.

Each timing measurement is performed in a structured routine, and all twenty-one routines are structured the same. Within each routine, both Write and Read cycle timing sets are implemented to establish the timing edges (shown as solid lines in Figure 11 and Figure 12). For the parameter being measured, some of the edges are relocated to establish the worst case timing for that parameter. These edges (shown as lighter dotted lines in the figures) have circled numbers adjacent to them, showing their position during the test and the numbers correspond to the timing symbols shown in the figure notes.

At the start of each timing parameter measurement routine, the initial timing is set, to force a functional failure when a test pattern is applied to the device. Upon failure, a timing edge is moved in increments toward a selected reference timing edge until the device passes; the pattern is reapplied to the device after each increment. The advantage of this test method is that a device will progress to a passing condition from a failing condition sooner than from a passing to a failing condition, because not all of the device memory will be accessed during each timing edge increment.

Once the device passes, a more complex pattern is applied, without changing the timing, to determine if the device is pattern sensitive. If so, the timing edge is further incremented until the device passes. The final placement of that timing edge is saved, calculations are made and the timing value is logged.

Two test patterns used in each timing routine were the March and Rowbar. A March is applied first to obtain the first passing value, and Rowbar, a more complex pattern, is applied next to adjust to a new value. The selection of these two patterns was based on measurements taken among ten test patterns for all twenty-one A.C. timing parameters. These measurements are shown in Table 1 and Table 2 for supply voltages VDD = 4.5V and VDD = 5.5V, respectively. Optimum test time was also a consideration in selecting these two patterns.

All twenty-one timing parameters were measured in sequence at VDD = 4.5V. The sequence was then repeated for VDD = 5.5V. The timing measurement datalogs

for AMD devices #1 and #2 are shown in Figures 14 and 18, respectively, for -55°C and in Figures 16 and 20, respectively for 125°C.

Special consideration had to be given to the proper selection of output comparator levels, VOH and VOL, for the THZ1, THZ2 and TOHZ measurements. This was necessary, because of the iong time required for an output to discharge from its VOH voltage level to a high impedance voltage level (1.77V), and to charge from its VOL voltage level to a high impedance voltage level (1.77V). Therefore, prior to these timing measurements, each output pin was measured for its VOL and VOH levels with its output load applied. Referring to the AC Timing Parameter datalogs of Figures 14, 16, 18, and 20, these measurements are recorded in the top two rows of numbers above each voltage supply label: VCC = 4.5V and VCC = 5.5V. In the top row, from left to right, the first eight numbers are the VOH measurements for outputs 1 through 8, respectively. The next number to the right is the lowest VOH value, VOHMIN, selected from among the eight measurements. The final number to the right is VOHMIN-0.3V, the level to which the comparator for VOH is set. Likewise, in the second row of numbers from left to right, the first eight numbers are the VOL measurements for outputs 1 through 8, respectively. The next number to the right is the highest VOL value, VOLMAX, selected from among the eight measurements. The final number to the right is VOLMAX+0.3V, the level to which the comparator is set for VOL. An output is considered tri-stated (passing condition), when it is less than VOHMIN-0.3V or greater than VOLMAX+0.3V.

Referring to the timing diagrams of Figures 11 and 12, the setups for some of the AC timing parameters are briefly described in the following sections. In the descriptions, the abbreviation L.E. means "Leading Edge" and T.E. means "Trailing Edge."

8.3.1 Test #01, Address Access Time - TAVQV (TAA)

Address edge AADST (PH9) is set to 200ns, Strobe (PH6) L.E. is set to 230ns, and Strobe (PH6) T.E. is set to 500ns. The Strobe (PH6) L.E. is incremented until a "PASS" occurs. TAA = Strobe (PH6) L.E.-AADST (PH9) L.E.

Note that the routines for Test #2 Chip Enable (-E1) Access Time (TCO1), Test #3 Chip Enable (E2) Access Time (TCO2), and Output Enable (-G) Access Time are identical to the routine for TAA. TAA vs. Temperature is shown in Figure 21.

8.3.2 Test #05, Write Pulse Width - TWLWH (TWP)

Write (PH5) L.E. is set to 300ns and Write (PH5) T.E. is set to 320ns, initially. Write (PH5) T.E. is incremented until a "PASS" occurs. TWP = Write (PH5) T.E.-Write (PH5) L.E. TWP vs. Temperature is shown in Figure 22.

8.3.3 Test #06, Write Recovery Time - TWHAX (TWR1), Address

This timing parameter is also known as Address Hold Time. Address edge ADDSP (PH1) and AADSP (PH9) are set to 400ns. Write (PH5) T.E. is set to 440ns, giving an initial TWR1 of -40ns. Write (PH5) T.E. is decremented until a "PASS" occurs. TWR1 = ADDSP (PH1),AADSP (PH9)-Write (PH5) T.E. A negative number is a valid result.

Note that the routines for Test #7, Chip Enable (-E1) Hold Time (or Write Recovery), labeled TWHAX (TWR1), and Test #8, Chip Enable (E2) Hold Time (or Write Recovery), labeled TE2LAX (TWR2), are similar to the routine for TWR1, Address. TWR1 vs. Temperature is shown in Figure 23.

8.3.4 Test #09, Data Hold Time - TWHDX (TDH)

DIN (PH2) T.E. and DIN (PH14) T.E. are set to 400ns to form the trailing edge of valid data. Write (PH5) T.E. is set to 430ns, giving an initial TDH of -30ns. Write (PH5) T.E. is decremented until a "PASS" occurs. TDH = DIN (PH2), DIN (PH14)-Write (PH5) T.E. A negative number is a valid result. TDH vs. Temperature is shown Figure 24.

8.3.5 Test #10, Address Setup Time - TAVWH (TAW), TAVWL (TAS)

This test measures the Address Setup time with respect to the Write (PH5) T.E. (TAW), and with respect to the Write (PH5) L.E. (TAS), all in the same routine. Address AADST (PH9) is set to 360ns and Write (PH5) L.E. is set to 280ns. Write (PH5) T.E. is at 380ns, therefore, the initial TAW is 20ns. AADST (PH9) is decremented until a "PASS" occurs. TAW = Write (PH5) T.E.-AADST (PH9). TAS = Write (PH5) L.E.-AADST (PH9). A negative number for TAS is a valid result.

Note that the routines for Test #11, Chip Enable (-E1) Setup Time, labeled TE1LWH (TCW1), and Test #12 Chip Enable (E2) Setup Time, labeled TE2HWH (TCW2), are similar to the routine for TAVAH (TAW). TAW vs. Temperature is shown in Figure 25 and TAS vs. Temperature is shown in Figure 26.

8.3.6 Test #13, Data Setup Time - TDVWH (TDW)

DIN (PH14) L.E. is set to 360ns. Write (PH5) T.E. is fixed at 380ns. DIN (PH14) L.E. is decremented until a "PASS" occurs. TDW = Write (PH5) T.E.-DIN (PH14) L.E.

8.3.7 Test #14, Output Hold Time - TAXQX (TOH)

Address ADDSP (PH1) and AADSP (PH14) are set to 400ns. Strobe (PH6) T.E. is set to 540ns, then is decremented until a "PASS" occurs. TOH = Strobe (PH6) T.E.-ADDSP (PH1), AADSP (PH14). TOH vs. Temperature is shown in Figure 27.

8.3.8 Test #15, Chip En (-E1) to Output Act Time - TE1LQX (TLZ1)

Chip Enable (-E1) (PH3) L.E. is set to 400ns. Strobe (PH6) L.E. is set to 380ns and Strobe (PH6) T.E. is set to 450ns. The comparator for VOH = 2.0V and the comparator for VOL = 1.5V. A "PASS" occurs when an output's VOL > 1.5V and VOH < 2.0V, indicating a tri-stated condition. The Strobe (PH6) T.E. is decremented until a "PASS" occurs. TLZ1 = Strobe (PH6) T.E.-Chip Enable (-E1) (PH3) L.E.

Note that the routines for Test #16 - TE2HQX (TLZ2) and for Test #17 - TGLQX (TOLZ) are similar to the routine for TE1LQX (TLZ1). TLZ1 vs. Temperature is shown in Figure 28.

8.3.9 Test #18, Chip Enable (-E1) Deselect Time - TE1HQZ (THZ1)

Chip Enable (-E1) (PH3) T.E. is set to 230ns. Strobe (PH6) L.E. is set to 230ns and Strobe (PH6) T.E. is set to 400ns. Refer to section 8.3 for discussion of comparator levels for this test. Strobe (PH6) T.E. is decremented until a "PASS" occurs, when VOL > VOLMAX +0.3V and VOH < VOHMIN-0.3V.

Note that the routines for Test #19 - TE2LQZ (THZ2) and #20 - TGHQZ (TOHZ) are similar to the routine for TE1HQZ (THZ1). THZ1 vs. Temperature is shown in Figure 29.

8.4 TEST SUMMARY

Both AMD devices passed testing over the full military temperature range, except device #2 at -40°C and -55°C. At these two temperatures, it failed pattern sensitivity and timing parameter tests at VDD=5.5V. However, whenever the temperature was raised above -40°C, device performance was restored to a full passing condition.

Timing parameter measurements, which had negative numbers (refer to the AC parameter datalog figures) are good results. The more negative the number, the better the device is. Chip Enable and Output Enable deselect times are very dependent on the resistance/capacitance loading on each output, and therefore, meaningful measurements are difficult to obtain.

Toshiba device #8 failed four patterns and the Data Retention and Bit-Unique tests at VDD = 4.5V at +125°C.

A.C. TESTING LOAD CIRCUIT

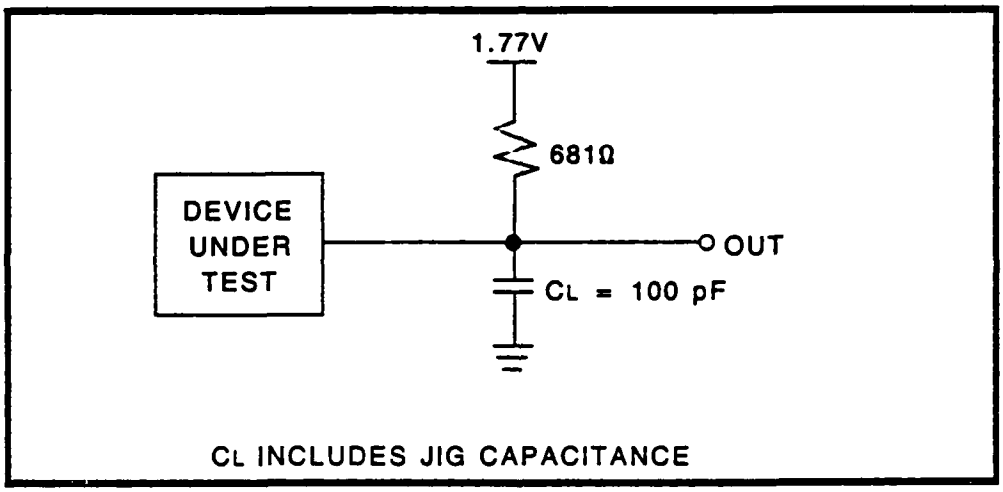
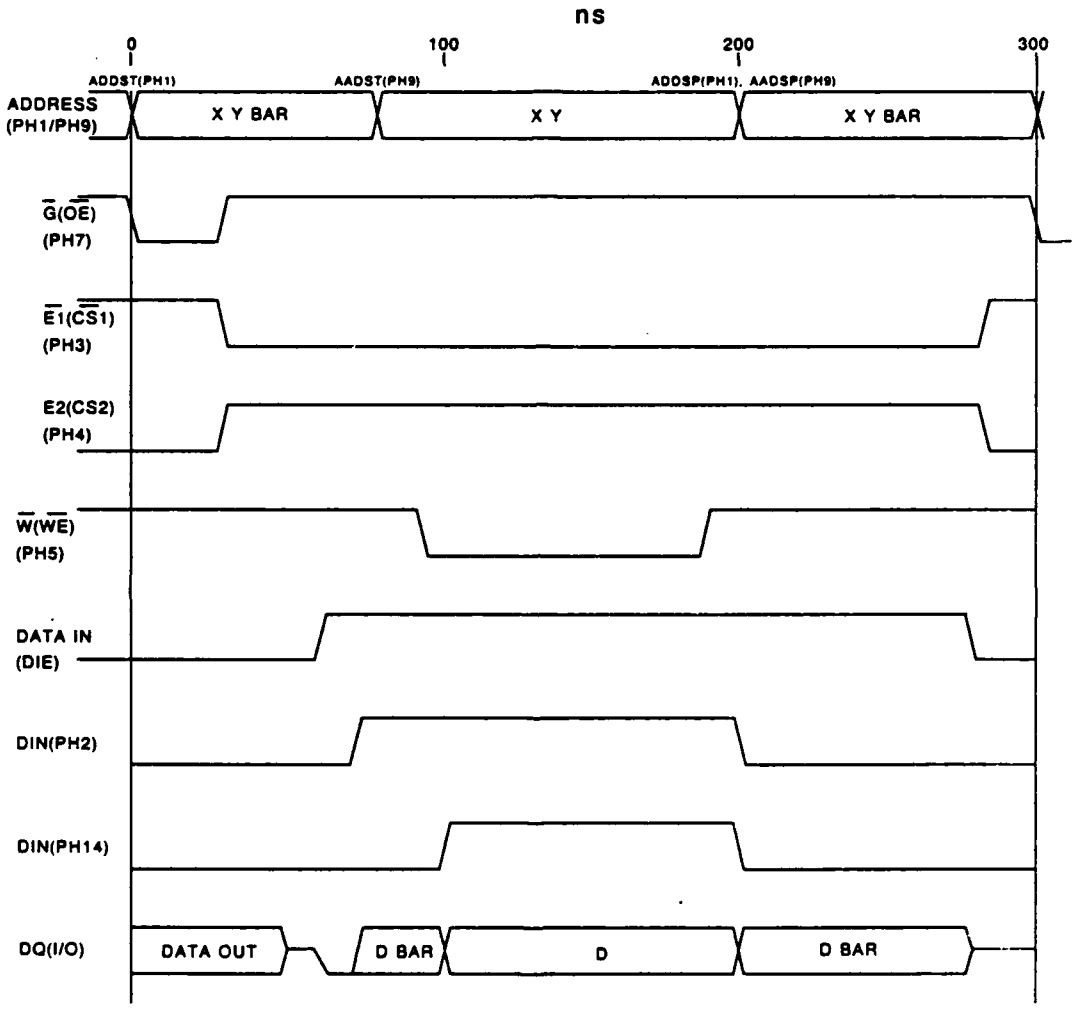
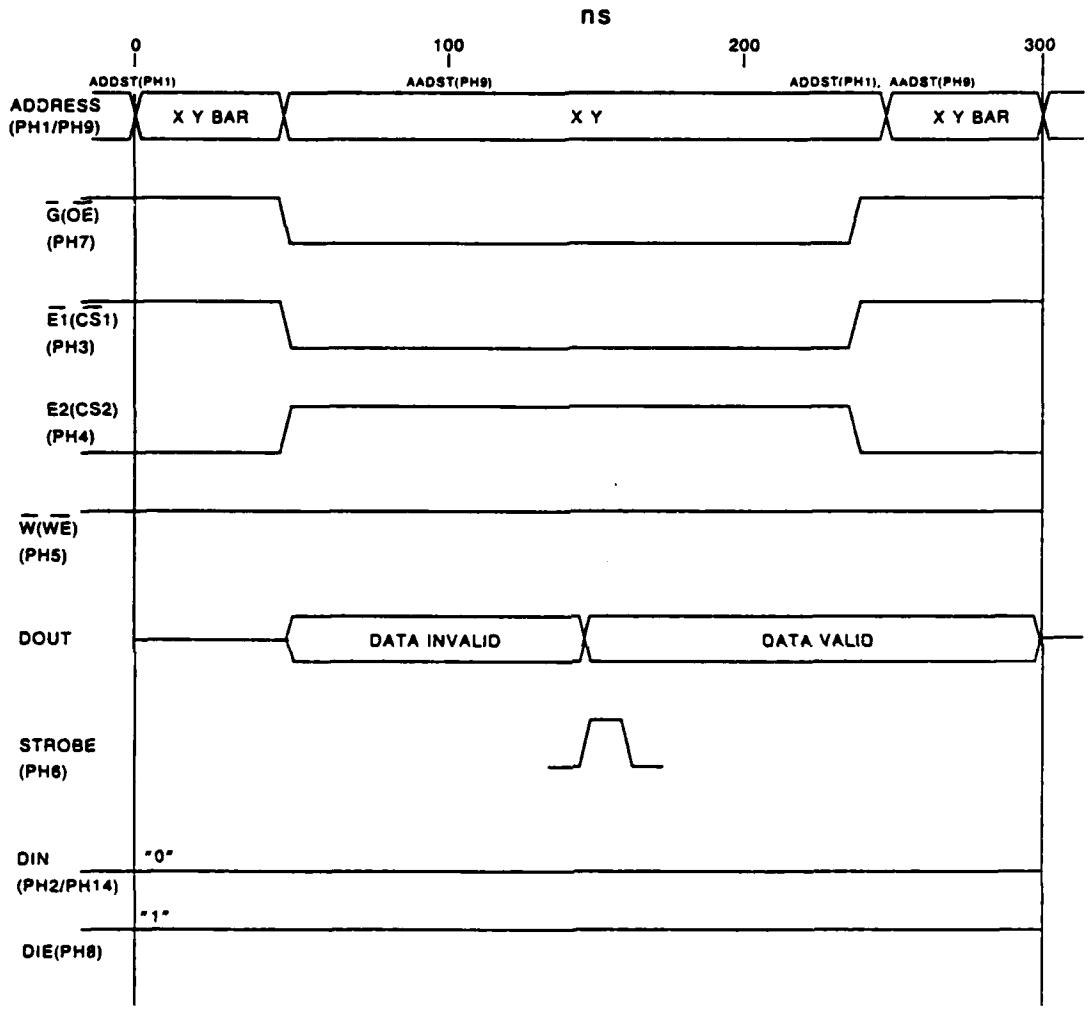


Figure 8: A.C. Output Load Circuit



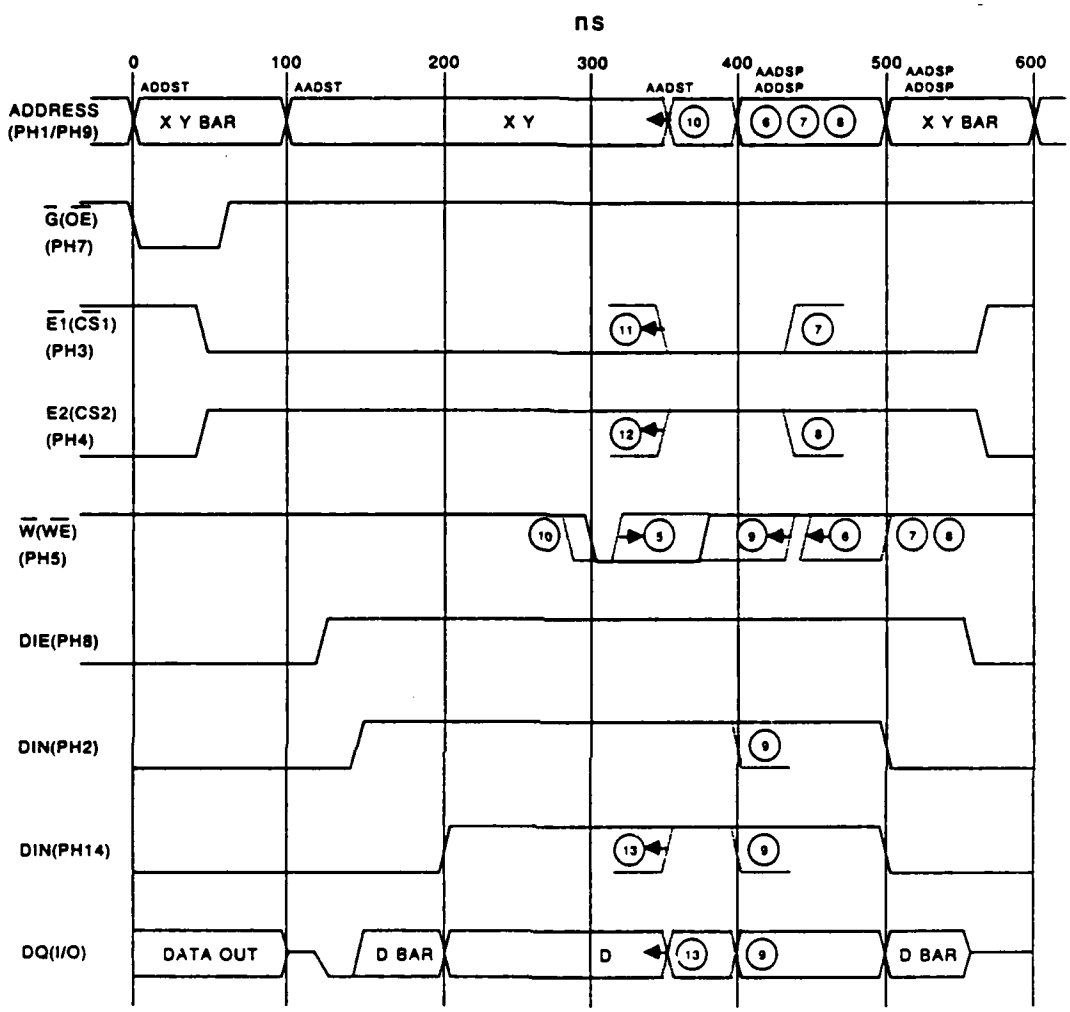
A.C. GENERAL FUNCTION
WRITE CYCLE (120 ns)

Figure 9: A.C. General Function Write Timing Diagram



A.C. GENERAL FUNCTION
READ CYCLE (120 ns)

Figure 10: A.C. General Function Read Timing Diagram



A.C. CHARACTERIZATION
WRITE CYCLE

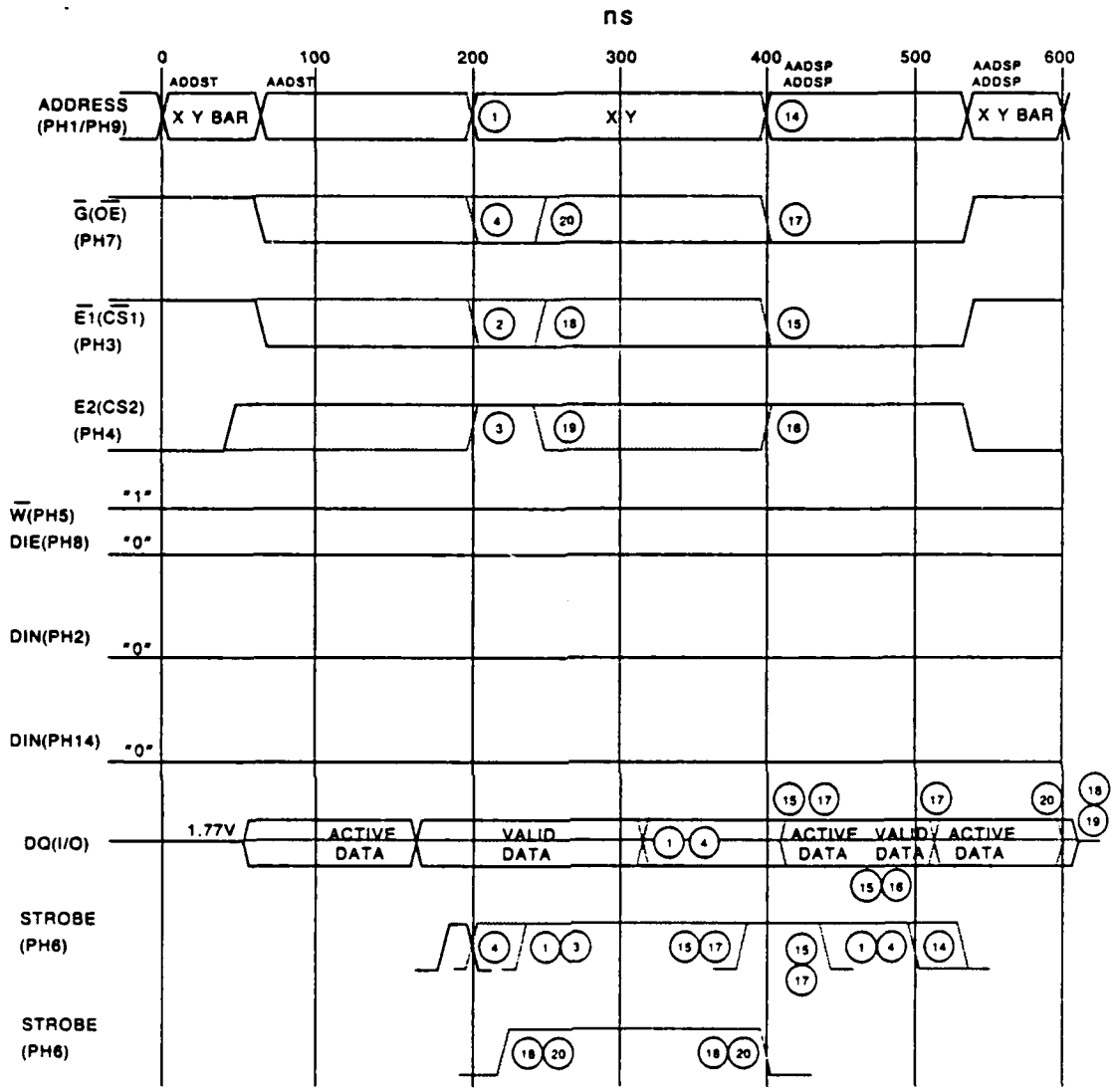
NOTES:

(1) ADDST & ADDSP = PH1
AADST & AADSP = PH9

(2) DIE (PH8), DIN(PH2), & DIN(PH14)
FORM THE DBAR/D/DBAR DATA IN FORMAT

(5) TWLWH (tWP)
(6) TWHAX (tWR1) ADDRESS
(7) TWHAX (tWR1) $\overline{E1}$
(8) TE2LAX (tWR2) E2
(9) TWHDX (tDH)
(10) TAVWH (tAW), TAVWL (tAS)
(11) TE1LWH (tCW1)
(12) TE2HWH (tCW2)
(13) TDVWH (tDW)

Figure 11: A.C. Characterization Write Timing Diagram



A.C. CHARACTERIZATION
READ CYCLE

1. TAVQV (tAA)
2. TE1LQV (tC01)
3. TE2HQV (tC02)
4. TGLQV (tOE)
14. TAXQX (tOH)
15. TE1LQX (tLZ1)
16. TE2HQX (tLZ2)
17. TGLQX (tOLZ)
18. TE1HQZ (tHZ1)
19. TE2LQZ (tHZ2)
20. TGHQZ (tOHZ)

Figure 12: A.C. Characterization Read Timing Diagram

```
80Z90561  REV. A                                    Date: 07/08/86 Time: 14:18:04
          VENDOR =      AMD            SN=      1      AM99C8810DM @ -55 C

TESTS #1-17      CONTINUITY TEST
  A0       A1       A2       A3       A4       A5       A6       A7       A8
 -0.77V   -0.77V   -0.77V   -0.77V   -0.77V   -0.77V   -0.77V   -0.77V   -0.77V
  A9       A10      A11      A12      CS1      CS2      OE       WE
 -0.77V   -0.77V   -0.77V   -0.77V   -0.75V   -0.75V   -0.77V   -0.77V


TEST  #18        GROSS FUNCTIONAL TEST

TESTS #20-36     INPUT LEAKAGE HIGH TEST
  A0       A1       A2       A3       A4       A5       A6       A7       A8
 0.015UA 0.017UA 0.012UA 0.013UA 0.013UA 0.014UA 0.014UA 0.014UA 0.013UA
  A9       A10      A11      A12      CS1      CS2      OE       WE
 0.015UA 0.014UA 0.014UA 0.014UA 0.014UA 0.012UA 0.014UA 0.015UA


TESTS #37-53     INPUT LEAKAGE LOW TEST
  A0       A1       A2       A3       A4       A5       A6       A7       A8
-0.001UA-0.003UA-0.003UA-0.001UA 0.000UA-0.001UA-0.001UA-0.003UA-0.003UA
  A9       A10      A11      A12      CS1      CS2      OE       WE
-0.002UA-0.002UA-0.001UA-0.002UA-0.003UA-0.002UA 0.000UA 0.000UA


TESTS #54-61     OUTPUT LEAKAGE HIGH TEST
  IO/1     IO/2     IO/3     IO/4     IO/5     IO/6     IO/7     IO/8
 0.019UA 0.016UA 0.014UA 0.016UA 0.017UA 0.015UA 0.013UA 0.014UA


TESTS #62-69     OUTPUT LEAKAGE LOW TEST
  IO/1     IO/2     IO/3     IO/4     IO/5     IO/6     IO/7     IO/8
-0.002UA-0.001UA 0.000UA 0.000UA-0.001UA-0.002UA-0.001UA-0.001UA


TESTS #70-77     OUTPUT VOLTAGE HIGH TEST
  IO/1     IO/2     IO/3     IO/4     IO/5     IO/6     IO/7     IO/8
  2.96V    2.96V    2.96V    2.97V    2.98V    2.98V    2.98V    2.98V


TESTS #78-85     OUTPUT VOLTAGE LOW TEST
  IO/1     IO/2     IO/3     IO/4     IO/5     IO/6     IO/7     IO/8
 0.044V   0.043V   0.043V   0.043V   0.044V   0.044V   0.045V   0.045V


TESTS #90-94     ICC CURRENT TESTS(OP/STDBY)
  ICC      ICC1     ISB      ISB1     ISB2
  35.9MA   47.2MA 0.032UA 0.032UA 0.032UA


*** A.C. FUNCTIONAL PATTERN TESTS ***

ALL 10 PATTERNS PASS AT VCC=4.5V AND 5.5V
DATA RETENTION TEST PASSES AT VCC=4.5V AND 5.5V
BIT-UNIQUE TEST PASSES AT VCC=4.5V AND 5.5V
SLOW CYCLE TEST PASSES AT VCC=4.5V AND 5.5V
```

Figure 13: Dev. #1 D.C. and A.C. Funct. Datalog at -55^{o}C

```
************************************************************
*                AC TIMING MEASUREMENTS                    *
************************************************************
  2.97V   2.97V   2.97V   2.97V   2.98V   2.98V   2.98V   2.98V   2.97V   2.67V

 0.034V  0.033V  0.032V  0.033V  0.033V  0.035V  0.035V  0.036V  0.036V  0.336V


VCC = 4.5V

  TAA        TCO1       TCO2       TOE        TWP        TWR        TWR1
  68.8NS     60.0NS     60.0NS     13.8NS     16.3NS   - 7.5NS    -10.0NS

  TWR2       TDH        TAS        TAW        TCW1       TCW2       TDW
- 8.8NS    - 6.3NS    -16.3NS     86.3NS     38.8NS     38.8NS     20.0NS

  TOH        TLZ1       TLZ2       TOLZ       THZ1       THZ2       TOHZ
  16.3NS     15.0NS     16.3NS     10.0NS     23.8NS     26.3NS     25.0NS


  3.85V   3.85V   3.84V   3.84V   3.85V   3.85V   3.85V   3.85V   3.84V   3.54V

 0.033V  0.033V  0.032V  0.033V  0.033V  0.034V  0.034V  0.035V  0.035V  0.335V


VCC = 5.5V

  TAA        TCO1       TCO2       TOE        TWP        TWR        TWR1
  63.8NS     76.3NS     76.3NS     12.5NS     13.8NS   - 5.0NS    - 8.8NS

  TWR2       TDH        TAS        TAW        TCW1       TCW2       TDW
- 7.5NS    - 3.8NS    -15.0NS     87.5NS     37.5NS     38.8NS     20.0NS

  TOH        TLZ1       TLZ2       TOLZ       THZ1       THZ2       TOHZ
  15.0NS     12.5NS     13.8NS      8.8NS     26.3NS     27.5NS     27.5NS

  ********************************
  *   DEVICE PASSES ALL TESTS    *
  ********************************
```

Figure 14: Dev. #1 A.C. Timing Parameter Datalog at -55°C

```
GOZ90561  REV. A                                    Date: 07/08/86 Time: 14:12:25
          VENDOR =      AMD          SN=      1     AM99C8810DM @ +125 C

TESTS #1-17     CONTINUITY TEST
  A0      A1      A2      A3      A4      A5      A6      A7      A8
 -0.46V  -0.46V  -0.46V  -0.46V  -0.46V  -0.46V  -0.46V  -0.46V  -0.46V
  A9      A10     A11     A12     CS1     CS2     OE      WE
 -0.46V  -0.46V  -0.46V  -0.46V  -0.43V  -0.43V  -0.47V  -0.46V


TEST  #18       GROSS FUNCTIONAL TEST

TESTS #20-36    INPUT LEAKAGE HIGH TEST
  A0      A1      A2      A3      A4      A5      A6      A7      A8
 0.016UA 0.016UA 0.018UA 0.016UA 0.016UA 0.016UA 0.015UA 0.015UA 0.016UA
  A9      A10     A11     A12     CS1     CS2     OE      WE
 0.016UA 0.016UA 0.015UA 0.015UA 0.017UA 0.016UA 0.015UA 0.010UA


TESTS #37-53    INPUT LEAKAGE LOW TEST
  A0      A1      A2      A3      A4      A5      A6      A7      A8
-0.002UA-0.002UA-0.002UA-0.001UA 0.000UA 0.001UA-0.001UA-0.002UA-0.003UA
  A9      A10     A11     A12     CS1     CS2     OE      WE
-0.003UA-0.002UA-0.001UA-0.001UA 0.000UA-0.001UA-0.002UA-0.002UA


TESTS #54-61    OUTPUT LEAKAGE HIGH TEST
  IO/1    IO/2    IO/3    IO/4    IO/5    IO/6    IO/7    IO/8
 0.027UA 0.024UA 0.024UA 0.022UA 0.023UA 0.023UA 0.023UA 0.024UA


TESTS #62-69    OUTPUT LEAKAGE LOW TEST
  IO/1    IO/2    IO/3    IO/4    IO/5    IO/6    IO/7    IO/8
-0.008UA-0.007UA-0.006UA-0.007UA-0.007UA-0.007UA-0.006UA-0.006UA


TESTS #70-77    OUTPUT VOLTAGE HIGH TEST
  IO/1    IO/2    IO/3    IO/4    IO/5    IO/6    IO/7    IO/8
  2.94V   2.94V   2.94V   2.95V   2.95V   2.95V   2.96V   2.96V


TESTS #78-85    OUTPUT VOLTAGE LOW TEST
  IO/1    IO/2    IO/3    IO/4    IO/5    IO/6    IO/7    IO/8
 0.080V  0.079V  0.076V  0.077V  0.078V  0.078V  0.079V  0.081V


TESTS #90-94    ICC CURRENT TESTS(OP/STDBY)
  ICC     ICC1    ISB     ISB1    ISB2
  20.9MA  34.5MA 0.024UA 0.024UA 0.024UA


*** A.C. FUNCTIONAL PATTERN TESTS ***

ALL 10 PATTERNS PASS AT VCC=4.5V AND 5.5V
DATA RETENTION TEST PASSES AT VCC=4.5V AND 5.5V
BIT-UNIQUE TEST PASSES AT VCC=4.5V AND 5.5V
SLOW CYCLE TEST PASSES AT VCC=4.5V AND 5.5V
```

Figure 15: DEV. #1 D.C. and A.C. Funct. Datalog at +125^{O}C

```
**********************************************************
*              AC TIMING MEASUREMENTS                    *
**********************************************************
  2.95V   2.95V   2.95V   2.95V   2.96V   2.96V   2.96V   2.96V   2.95V   2.65V

 0.066V  0.064V  0.062V  0.063V  0.063V  0.065V  0.067V  0.068V  0.068V  0.368V

VCC = 4.5V

  TAA       TCO1      TCO2      TOE       TWP       TWR       TWR1
  82.5NS    87.5NS    87.5NS    20.0NS    27.5NS   -12.5NS   -15.0NS

  TWR2      TDH       TAS       TAW       TCW1      TCW2      TDW
 -11.3NS   -11.3NS   -25.0NS    77.5NS    52.5NS    52.5NS    21.3NS

  TOH       TLZ1      TLZ2      TOLZ      THZ1      THZ2      TOHZ
  23.8NS    25.0NS    25.0NS    16.3NS    31.3NS    33.8NS    30.0NS

  3.77V   3.77V   3.77V   3.76V   3.78V   3.77V   3.78V   3.77V   3.76V   3.46V

 0.061V  0.061V  0.058V  0.060V  0.060V  0.062V  0.063V  0.063V  0.065V  0.365V

VCC = 5.5V

  TAA       TCO1      TCO2      TOE       TWP       TWR       TWR1
  70.0NS    73.8NS    75.0NS    17.5NS    22.5NS   -10.0NS   -12.5NS

  TWR2      TDH       TAS       TAW       TCW1      TCW2      TDW
 -11.3NS    - 8.8NS  -21.3NS    81.3NS    47.5NS    47.5NS    20.0NS

  TOH       TLZ1      TLZ2      TOLZ      THZ1      THZ2      TOHZ
  20.0NS    21.3NS    21.3NS    13.8NS    32.5NS    33.8NS    31.3NS

  **********************************
  *   DEVICE PASSES ALL TESTS      *
  **********************************
```

Figure 16: Dev. #1 A.C. Timing Parameter Datalog at +125^{o}C

```
80Z90561  REV. A                                    Date: 07/08/86 Time: 14:57:46
          VENDOR =      AMD            SN=      2     AM99C8810DM @ -55 CC

TESTS #1-17     CONTINUITY TEST
  A0      A1      A2      A3      A4      A5      A6      A7      A8
 -0.77V  -0.77V  -0.77V  -0.77V  -0.77V  -0.77V  -0.77V  -0.77V  -0.77V
  A9      A10     A11     A12     CS1     CS2     OE      WE
 -0.77V  -0.77V  -0.77V  -0.77V  -0.75V  -0.75V  -0.77V  -0.77V


TEST  #18       GROSS FUNCTIONAL TEST

TESTS #20-36    INPUT LEAKAGE HIGH TEST
  A0      A1      A2      A3      A4      A5      A6      A7      A8
 0.033UA 0.033UA 0.017UA 0.015UA 0.017UA 0.016UA 0.016UA 0.015UA 0.014UA
  A9      A10     A11     A12     CS1     CS2     OE      WE
 0.015UA 0.041UA 0.017UA 0.015UA 0.039UA 0.014UA 0.012UA 0.013UA


TESTS #37-53    INPUT LEAKAGE LOW TEST
  A0      A1      A2      A3      A4      A5      A6      A7      A8
-0.017UA-0.020UA-0.002UA 0.000UA-0.002UA-0.002UA-0.001UA-0.002UA-0.001UA
  A9      A10     A11     A12     CS1     CS2     OE      WE
-0.002UA-0.031UA-0.002UA-0.002UA-0.031UA-0.001UA-0.005UA 0.000UA


TESTS #54-61    OUTPUT LEAKAGE HIGH TEST
  IO/1    IO/2    IO/3    IO/4    IO/5    IO/6    IO/7    IO/8
 0.018UA 0.019UA 0.019UA 0.017UA 0.016UA 0.016UA 0.016UA 0.016UA


TESTS #62-69    OUTPUT LEAKAGE LOW TEST
  IO/1    IO/2    IO/3    IO/4    IO/5    IO/6    IO/7    IO/8
-0.013UA 0.000UA 0.001UA 0.000UA 0.000UA 0.000UA 0.001UA 0.000UA


TESTS #70-77    OUTPUT VOLTAGE HIGH TEST
  IO/1    IO/2    IO/3    IO/4    IO/5    IO/6    IO/7    IO/8
  2.96V   2.97V   2.97V   2.97V   2.98V   2.98V   2.98V   2.98V


TESTS #78-85    OUTPUT VOLTAGE LOW TEST
  IO/1    IO/2    IO/3    IO/4    IO/5    IO/6    IO/7    IO/8
 0.043V  0.042V  0.040V  0.041V  0.042V  0.043V  0.043V  0.044V


TESTS #90-94    ICC CURRENT TESTS(OP/STDBY)
  ICC     ICC1    ISB     ISB1    ISB2
  30.8MA  44.8MA 0.000UA 0.000UA 0.000UA


*** A.C. FUNCTIONAL PATTERN TESTS ***
  CHECKERBOARD PATT. UPCNT FAILURE  @VCC=  5.50V
  X-PARITY PATT. FAILURE            @VCC=  5.50V
  Y-PARITY PATT. FAILURE            @VCC=  5.50V
  MARCH PATT. FAILURE               @VCC=  5.50V
  MULTI-READ MARCH PATT. FAILURE    @VCC=  5.50V
  ROWBAR PATT. FAILURE              @VCC=  5.50V
  GALLOPING COLUMN PATT. FAILURE    @VCC=  5.50V
  GALLOPING ROW PATT. FAILURE       @VCC=  5.50V
  DATA RETENTION TEST FAILURE       @VCC=  5.50V
  BIT-UNIQUE TEST FAILURE           @VCC=  5.50V

SLOW CYCLE TEST PASSES AT VCC=4.5V AND 5.5V
```

Figure 17: Dev. #2 D.C. and A.C. Funct. Datalog at -55°C

```
**********************************************************
*              AC TIMING MEASUREMENTS                    *
**********************************************************
  2.97V   2.97V   2.97V   2.97V   2.98V   2.98V   2.98V   2.98V   2.97V   2.67V

 0.032V  0.032V  0.031V  0.032V  0.032V  0.033V  0.033V  0.034V  0.034V  0.334V


VCC = 4.5V

  TAA       TCO1      TCO2      TOE       TWP       TWR       TWR1
  57.5NS    52.5NS    52.5NS    12.5NS    15.0NS   - 8.8NS   -10.0NS

  TWR2      TDH       TAS       TAW       TCW1      TCW2      TDW
 - 7.5NS   - 7.5NS   -15.0NS    87.5NS    35.0NS    35.0NS    20.0NS

  TOH       TLZ1      TLZ2      TOLZ      THZ1      THZ2      TOHZ
  18.8NS    13.8NS    13.8NS     8.8NS    25.0NS    27.5NS    25.0NS


  ADDRESS ACCESS TIME FAILURE(TAA)          @VCC=  5.50V
  CHIP SELECT1 ACCESS TIME FAILURE(TCO1)    @VCC=  5.50V
  CHIP SELECT2 ACCESS TIME FAILURE(TCO2)    @VCC=  5.50V
  OUTPUT ENABLE ACCESS TIME FAILURE(TOE)    @VCC=  5.50V
  WRITE PULSE WIDTH FAILURE(TWP)            @VCC=  5.50V
  WRITE RECOVERY(CS1) TIME FAILURE(TWR1)    @VCC=  5.50V
  DATA HOLD TIME FAILURE(TDH)               @VCC=  5.50V
  CS1 SETUP TIME FAILURE(TCW1)              @VCC=  5.50V
  CS2 SETUP TIME FAILURE(TCW2)              @VCC=  5.50V
  DATA SETUP TIME FAILURE(TDW)              @VCC=  5.50V
  CS1 OUTACT TIME FAILURE(TLZ1)             @VCC=  5.50V
  3.85V   3.85V   3.85V   3.84V   3.85V   3.85V   3.85V   3.85V   3.84V   3.54V

 0.031V  0.030V  0.030V  0.031V  0.031V  0.032V  0.032V  0.033V  0.033V  0.333V


VCC = 5.5V

  TAA       TCO1      TCO2      TOE       TWP       TWR       TWR1
 122.5NS   122.5NS   122.5NS    62.5NS    82.5NS   -40.0NS   + 5.0NS

  TWR2      TDH       TAS       TAW       TCW1      TCW2      TDW
 -40.0NS   + 2.5NS   -82.5NS    20.0NS   102.5NS   102.5NS    52.5NS

  TOH       TLZ1      TLZ2      TOLZ      THZ1      THZ2      TOHZ
  15.0NS    12.5NS    12.5NS     7.5NS    26.3NS    27.5NS    26.3NS


  ********************************
  *   DEVICE FAILURE             *
  ********************************
```

Figure 18: Dev. #2 A.C. Timing Parameter Datalog at -55°C

```
G0Z90561  REV. A                                    Date: 07/08/86 Time: 14:51:07
          VENDOR =      AMD            SN=     2     AM99C8810DM @ +125 C

TESTS #1-17      CONTINUITY TEST
  A0       A1       A2       A3       A4       A5       A6       A7       A8
-0.43V   -0.43V   -0.43V   -0.44V   -0.44V   -0.44V   -0.44V   -0.44V   -0.44V
  A9       A10      A11      A12      CS1      CS2      OE       WE
-0.44V   -0.43V   -0.44V   -0.44V   -0.4QV   -0.40V   -0.44V   -0.44V


TEST  #18        GROSS FUNCTIONAL TEST

TESTS #20-36     INPUT LEAKAGE HIGH TEST
  A0       A1       A2       A3       A4       A5       A6       A7       A8
0.019UA  0.019UA  0.019UA  0.020UA  0.018UA  0.016UA  0.017UA  0.017UA  0.018UA
  A9       A10      A11      A12      CS1      CS2      OE       WE
0.018UA  0.018UA  0.016UA  0.017UA  0.020UA  0.020UA  0.013UA  0.016UA


TESTS #37-53     INPUT LEAKAGE LOW TEST
  A0       A1       A2       A3       A4       A5       A6       A7       A8
-0.001UA-0.002UA-0.003UA-0.002UA 0.001UA 0.000UA-0.001UA-0.001UA-0.003UA
  A9       A10      A11      A12      CS1      CS2      OE       WE
-0.003UA-0.001UA-0.001UA-0.001UA 0.000UA 0.000UA-0.002UA-0.002UA


TESTS #54-61     OUTPUT LEAKAGE HIGH TEST
  IO/1     IO/2     IO/3     IO/4     IO/5     IO/6     IO/7     IO/8
0.040UA  0.037UA  0.036UA  0.035UA  0.035UA  0.035UA  0.036UA  0.034UA


TESTS #62-69     OUTPUT LEAKAGE LOW TEST
  IO/1     IO/2     IO/3     IO/4     IO/5     IO/6     IO/7     IO/8
-0.018UA-0.019UA-0.019UA-0.017UA-0.017UA-0.018UA-0.019UA-0.018UA


TESTS #70-77     OUTPUT VOLTAGE HIGH TEST
  IO/1     IO/2     IO/3     IO/4     IO/5     IO/6     IO/7     IO/8
  2.94V    2.94V    2.94V    2.95V    2.95V    2.95V    2.95V    2.95V


TESTS #78-85     OUTPUT VOLTAGE LOW TEST
  IO/1     IO/2     IO/3     IO/4     IO/5     IO/6     IO/7     IO/8
 0.082V   0.080V   0.078V   0.078V   0.078V   0.079V   0.081V   0.083V


TESTS #90-94     ICC CURRENT TESTS(OP/STDBY)
  ICC      ICC1     ISB      ISB1     ISB2
  17.1MA   29.5MA 0.005UA  0.005UA  0.005UA


*** A.C. FUNCTIONAL PATTERN TESTS ***

ALL 10 PATTERNS PASS AT VCC=4.5V AND 5.5V
DATA RETENTION TEST PASSES AT VCC=4.5V AND 5.5V
BIT-UNIQUE TEST PASSES AT VCC=4.5V AND 5.5V
SLOW CYCLE TEST PASSES AT VCC=4.5V AND 5.5V
```

Figure 19: Dev. #2 D.C. and A.C. Funct. Datalog at +125^{O}C

```
**************************************************************
*                  AC TIMING MEASUREMENTS                    *
**************************************************************
  2.95V   2.95V   2.95V   2.95V   2.96V   2.96V   2.96V   2.96V   2.95V   2.65V

 0.065V  0.064V  0.061V  0.063V  0.063V  0.065V  0.066V  0.068V  0.068V  0.368V

VCC = 4.5V

  TAA       TCO1      TCO2      TOE       TWP       TWR       TWR1
  77.5NS    82.5NS    82.5NS    18.8NS    27.5NS   -15.0NS   -16.3NS

  TWR2      TDH       TAS       TAW       TCW1      TCW2      TDW
 -12.5NS   -13.8NS   -23.8NS    78.8NS    50.0NS    50.0NS    22.5NS

  TOH       TLZ1      TLZ2      TOLZ      THZ1      THZ2      TOHZ
  28.8NS    23.8NS    23.8NS    16.3NS    30.0NS    33.8NS    28.8NS


  3.77V   3.77V   3.77V   3.77V   3.77V   3.77V   3.78V   3.77V   3.77V   3.47V

 0.060V  0.059V  0.057V  0.058V  0.058V  0.061V  0.062V  0.064V  0.064V  0.364V

VCC = 5.5V

  TAA       TCO1      TCO2      TOE       TWP       TWR       TWR1
  63.8NS    67.5NS    68.8NS    16.3NS    23.8NS   -12.5NS   -12.5NS

  TWR2      TDH       TAS       TAW       TCW1      TCW2      TDW
 -10.0NS   -11.3NS   -20.0NS    82.5NS    45.0NS    45.0NS    20.0NS

  TOH       TLZ1      TLZ2      TOLZ      THZ1      THZ2      TOHZ
  23.8NS    20.0NS    20.0NS    12.5NS    31.3NS    33.8NS    31.3NS


  ********************************
  *   DEVICE PASSES ALL TESTS    *
  ********************************
```

Figure 20: Dev. #2 A.C. Timing Parameter Datalog at +125^{o}C

AMD #1 @ VDD = 4.5V, T_A = 25°C

ns

PATTERN	TAA	TC01	TC02	TOE	TWP	TWR	TWR1	TWR2	TDH	TAS	TAW
CKBUP	63.8	65.0	65.0	16.3	10.0	-40.0	-40.0	-40.0	-8.8	-82.5	20.0
XPARTY	63.8	66.3	66.3	16.3	21.3	-40.0	-40.0	-40.0	-8.8	-82.5	20.0
YPARTY	63.8	66.3	66.3	16.3	21.3	-40.0	-40.0	-40.0	-8.8	-82.5	20.0
MRM	68.8	67.5	67.5	16.3	20.0	-12.5	-12.5	-11.3	-8.8	-21.3	81.3
SURDSB	66.3	65.0	65.0	16.3	21.3	-10.0	-10.0	-8.8	-8.8	-21.3	81.3
ROWBAR	67.5	68.8	68.8	16.3	21.3	-10.0	-10.0	-11.3	-10.0	-20.0	82.5
GALCOL	68.8	67.5	68.8	16.3	21.3	-40.0	-40.0	-40.0	-8.8	-65.0	37.5
GALROW	68.8	67.5	67.5	16.3	21.3	-40.0	-40.0	-40.0	-8.8	-63.8	38.8
ADDCMP	67.5	67.5	67.5	16.3	20.0	-10.0	-10.0	-8.8	-8.8	-21.3	81.3
MARCH	67.5	66.3	66.3	16.3	20.0	-11.3	-12.5	-11.3	-8.8	-21.3	81.3
PATTERN	TCW1	TCW2	TDW	TOH	TLZ1	TLZ2	TOLZ	THZ1	THZ2	TOHZ	
CKBUP	20.0	20.0	20.0	20.0	20.0	20.0	13.8	22.5	23.8	21.3	
XPARTY	45.0	45.0	20.0	20.0	20.0	20.0	13.8	22.5	23.8	23.8	
YPARTY	45.0	45.0	20.0	20.0	20.0	20.0	13.8	22.5	23.8	23.8	
MRM	42.5	43.8	20.0	20.0	20.0	20.0	13.8	22.5	23.8	23.8	
SURDSB	43.8	43.8	20.0	20.0	20.0	20.0	13.8	22.5	23.8	21.3	
WROBAR	45.0	45.0	45.0	20.0	20.0	20.0	13.8	22.5	23.8	23.8	
GALCOL	45.0	45.0	20.0	20.0	20.0	20.0	13.8	22.5	25.0	25.0	
GALROW	45.0	45.0	20.0	20.0	20.0	20.0	13.8	22.5	23.8	23.8	
ADDCMP	43.8	43.8	20.0	20.0	20.0	20.0	13.8	22.5	23.8	21.3	
MARCH	42.5	45.0	20.0	20.0	20.0	20.0	13.8	22.5	23.8	21.3	

TABLE 1
Timing Measurements vs. Patterns at VDD = 4.5V

AMD #1 @ VDD = 5.5V, T_A = 25°C

ns

PATTERN	TAA	TC01	TC02	TOE	TWP	TWR	TWR1	TWR2	TDH	TAS	TAW
CKBUP	56.3	60.0	61.3	13.8	10.0	-40.0	-40.0	-40.0	-6.3	-82.5	20.0
XPARTY	56.3	62.5	63.8	15.0	17.5	-40.0	-40.0	-40.0	-6.3	-82.5	20.0
YPARTY	56.3	62.5	63.8	15.0	17.5	-40.0	-40.0	-40.0	-6.3	-82.5	20.0
MRM	60.0	63.8	63.5	15.0	17.5	-8.8	-11.3	-11.3	-6.3	-18.8	83.3
SURDSB	60.0	60.0	61.3	15.0	17.5	-7.5	-8.8	-8.8	-6.3	-18.8	83.3
ROWBAR	61.3	63.8	63.8	13.8	17.5	-7.5	-10.0	-8.8	-6.3	-17.5	85.0
GALCOL	61.3	62.5	63.8	15.0	17.5	-40.0	-40.0	-40.0	-6.3	-66.3	36.3
GALROW	61.3	63.8	65.0	15.0	17.5	-40.0	-40.0	-40.0	-6.3	-66.3	36.3
ADDCMP	58.8	62.5	63.8	15.0	17.5	-7.5	-8.8	-8.8	-6.3	-17.5	85.0
MARCH	60.0	62.5	63.8	15.0	17.5	-8.8	-11.3	-11.3	-6.3	-18.8	83.3
PATTERN	TCW1	TCW2	TDW	TOH	TLZ1	TLZ2	TOLZ	THZ1	THZ2	TOHZ	
CKBUP	20.0	20.0	20.0	17.5	16.3	17.5	11.3	35.0	36.3	35.0	
XPARTY	41.3	41.3	20.0	17.5	16.3	17.5	11.3	35.0	36.3	35.0	
YPARTY	41.3	41.3	20.0	17.5	16.3	17.5	11.3	35.0	36.3	35.0	
MRM	40.0	41.3	20.0	17.5	16.3	17.5	11.3	36.6	36.3	35.0	
SURDSB	40.0	41.3	20.0	17.5	16.3	17.5	11.3	35.0	36.3	33.8	
ROWBAR	41.3	41.3	20.0	17.5	16.3	17.5	11.3	36.3	36.3	35.0	
GALCOL	41.3	41.3	20.0	17.5	16.3	17.5	11.3	36.3	36.3	35.0	
GALROW	41.3	41.3	20.0	17.5	16.3	17.5	11.3	36.3	36.3	35.0	
ADDCMP	41.3	41.3	20.0	17.5	16.3	17.5	11.3	35.0	36.3	35.0	
MARCH	40.0	41.3	20.0	17.5	16.3	17.5	11.3	36.3	36.3	35.0	

TABLE 2
Timing Measurements vs. Patterns at VDD = 5.5V

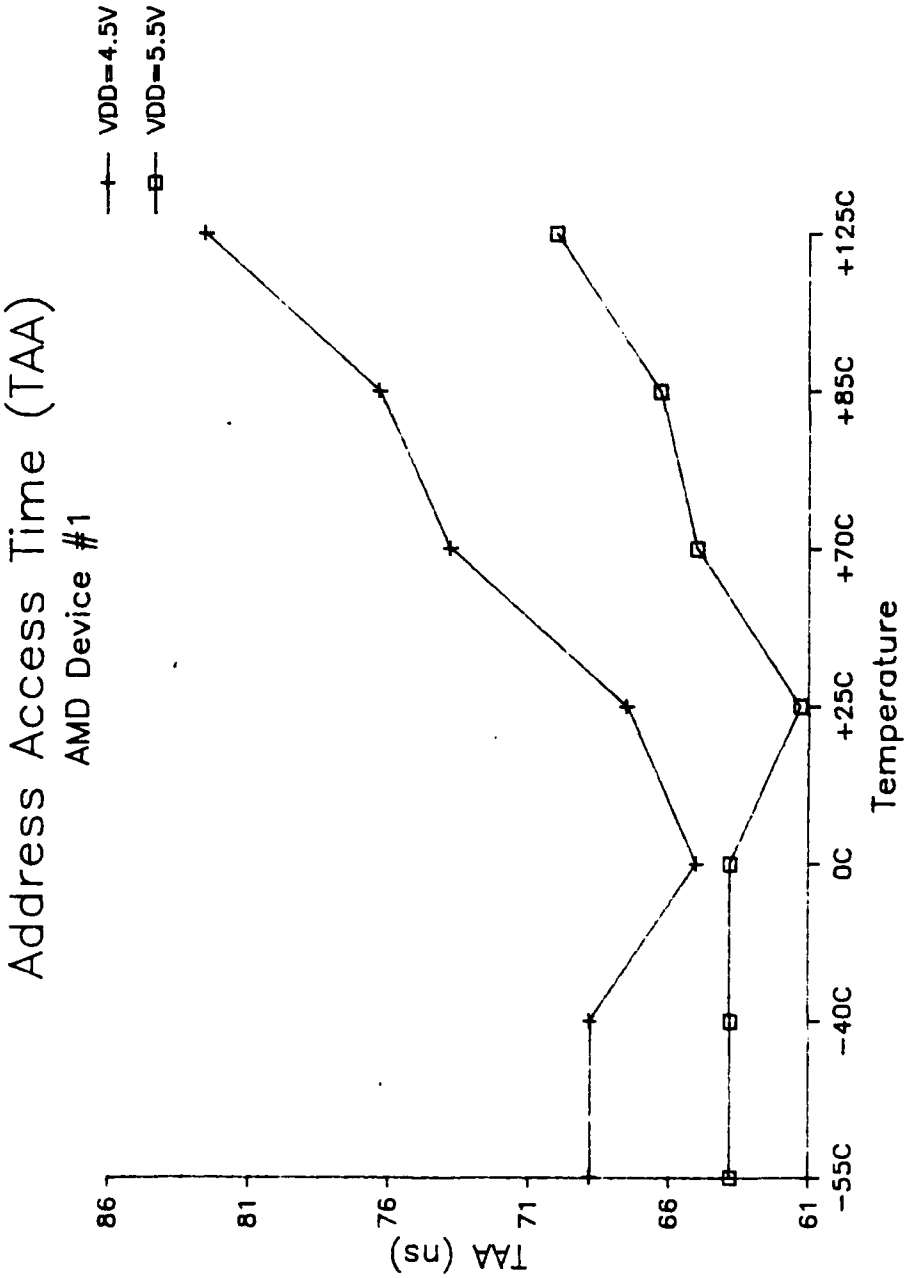


Figure 21: AMD Dev #1 Address Access Time vs Temperature

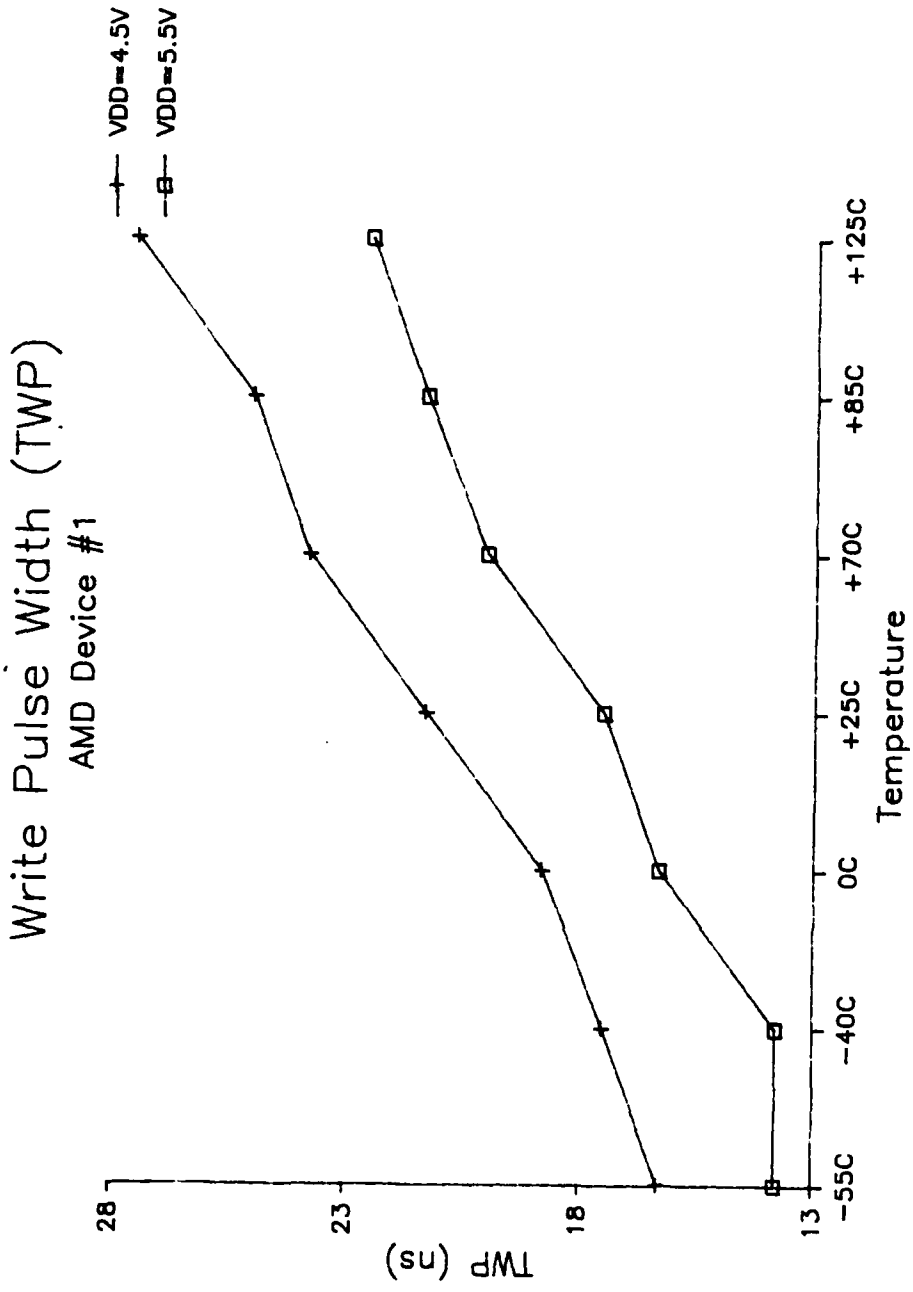


Figure 22: AMD Dev #1 Write Pulse Width vs Temperature

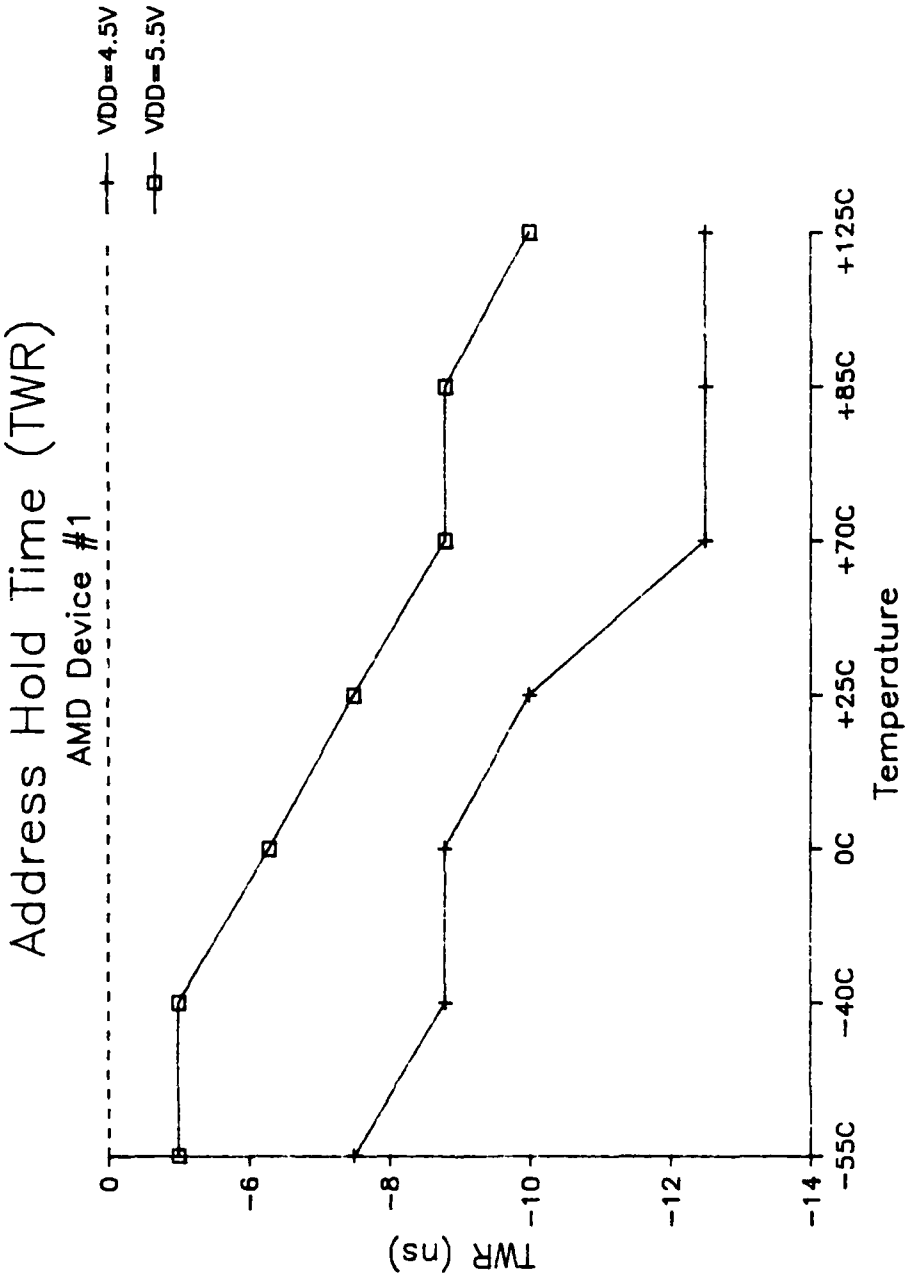


Figure 23: AMD Dev #1 Address Hold Time vs Temperature

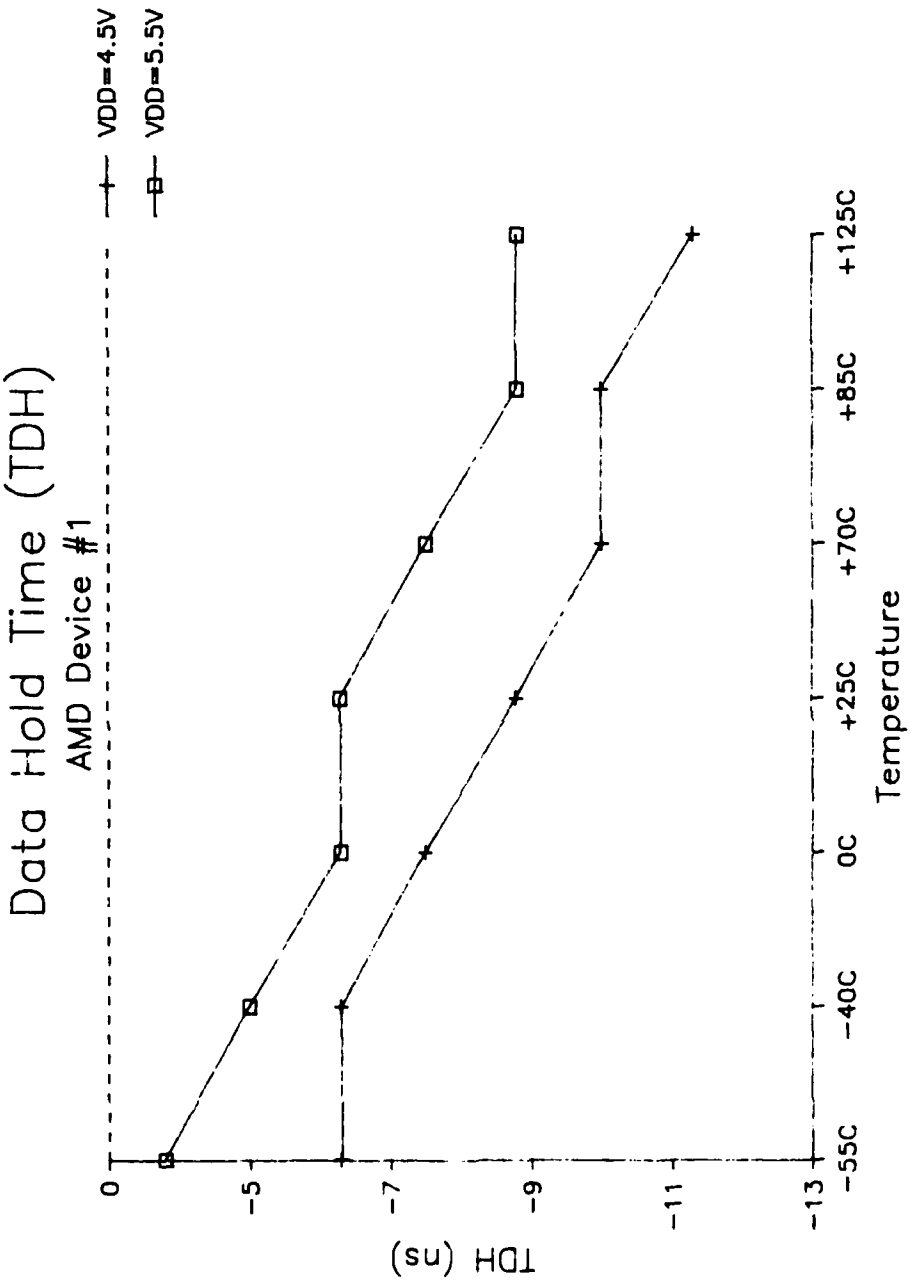


Figure 24: AMD Dev #1 Data Hold Time vs Temperature

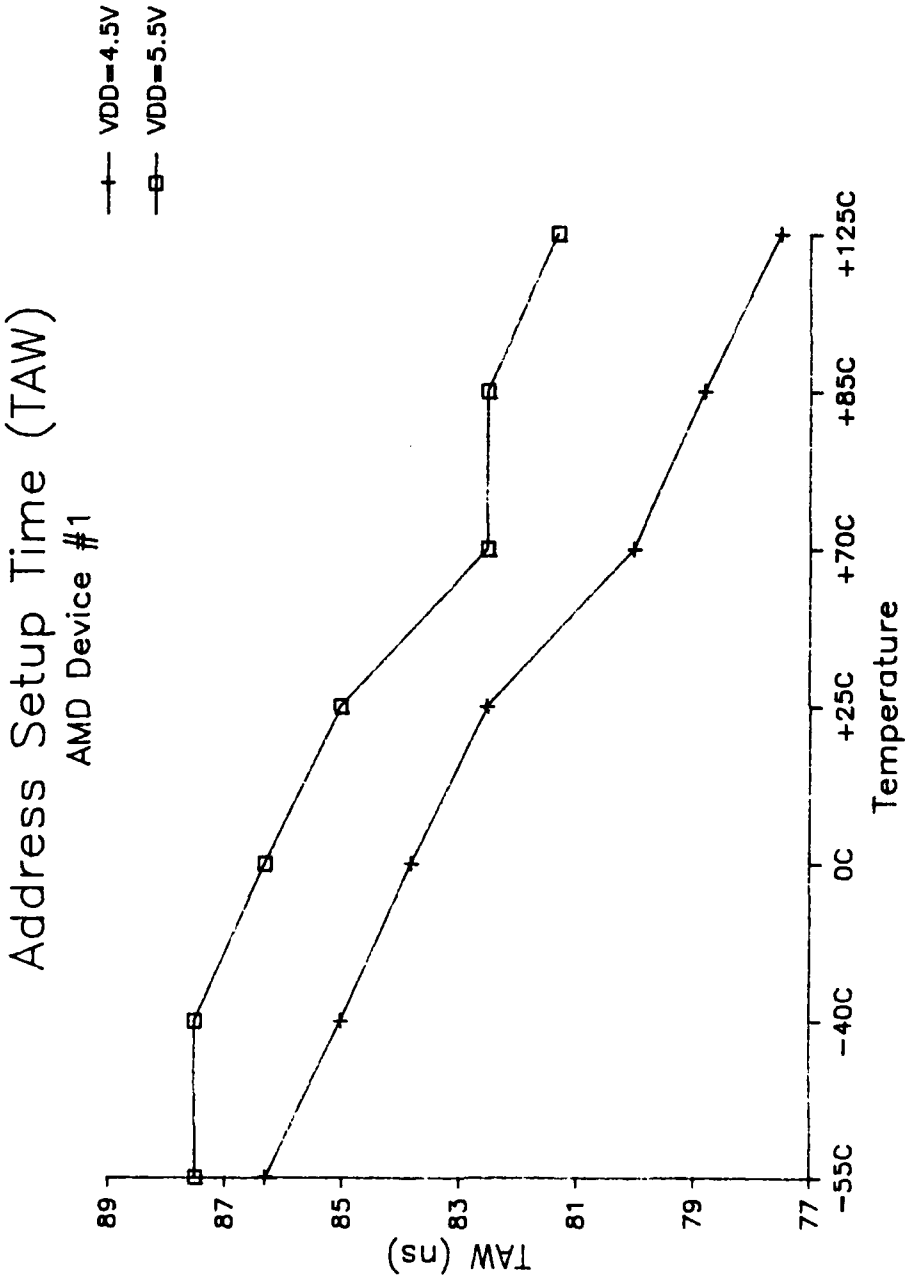


Figure 25: AMD Dev #1 Address Setup Time (TAW) vs Temperature

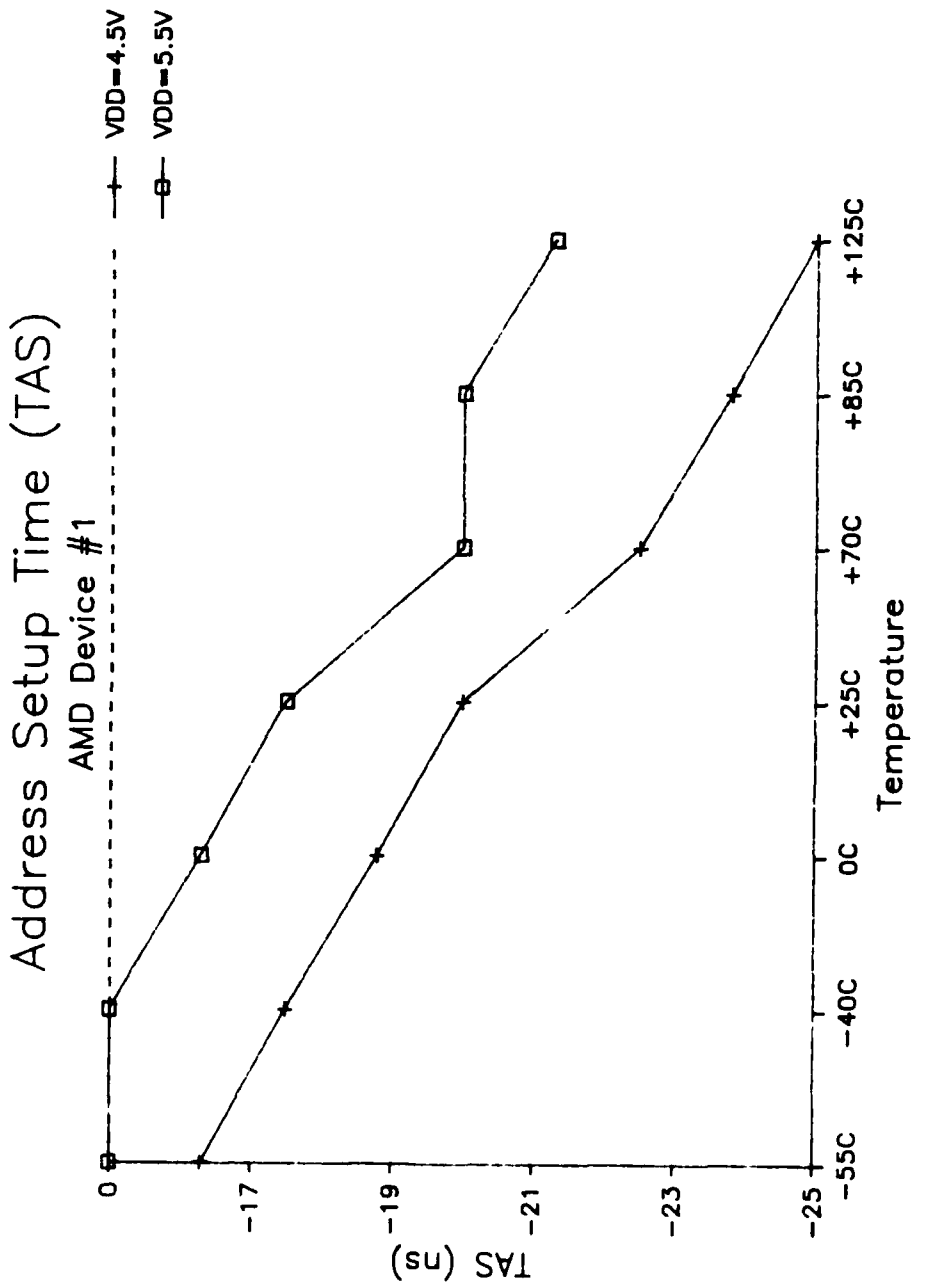


Figure 26: AMD Dev #1 Address Setup Time (TAS) vs Temperature

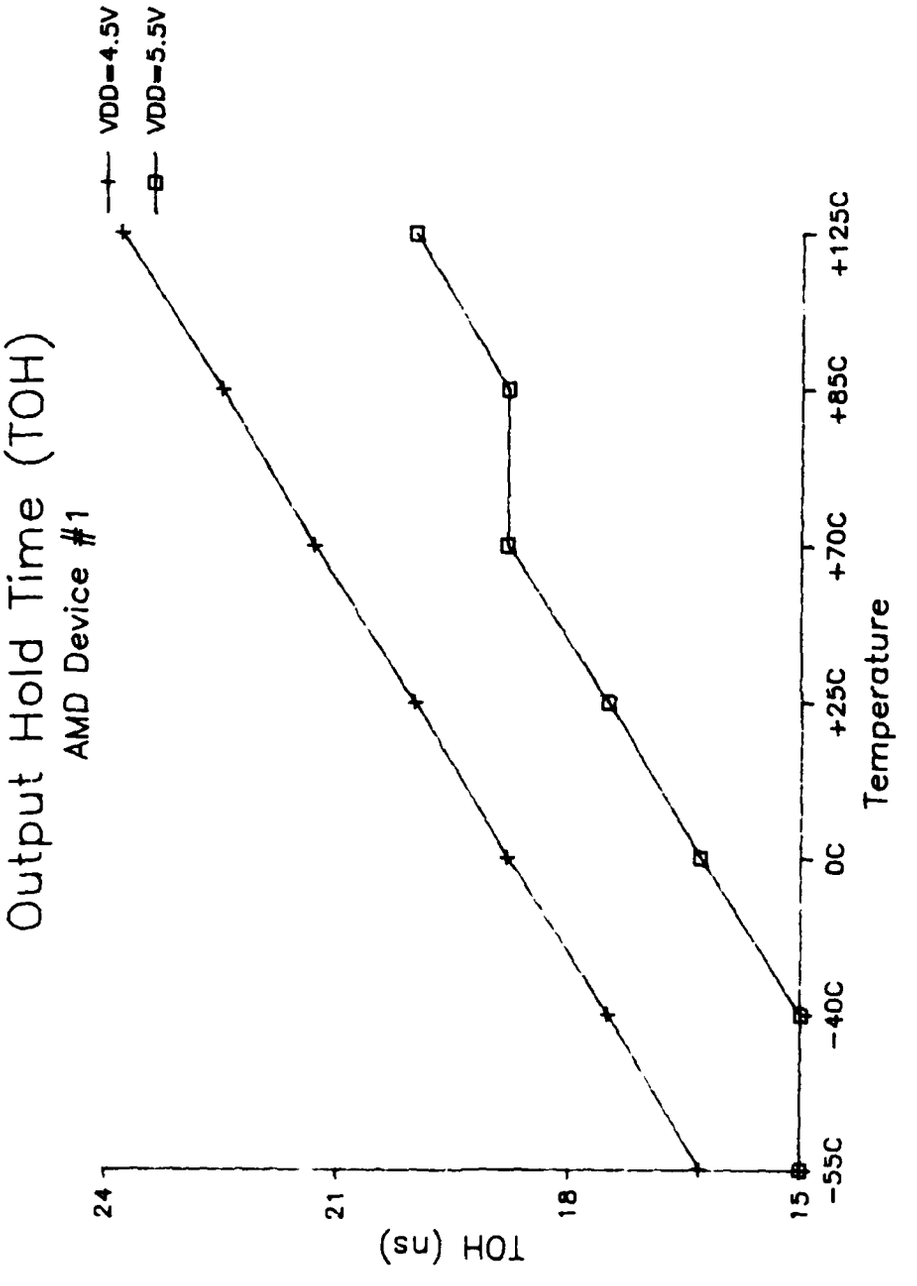


Figure 27: AMD Dev #1 Output Hold Time vs Temperature

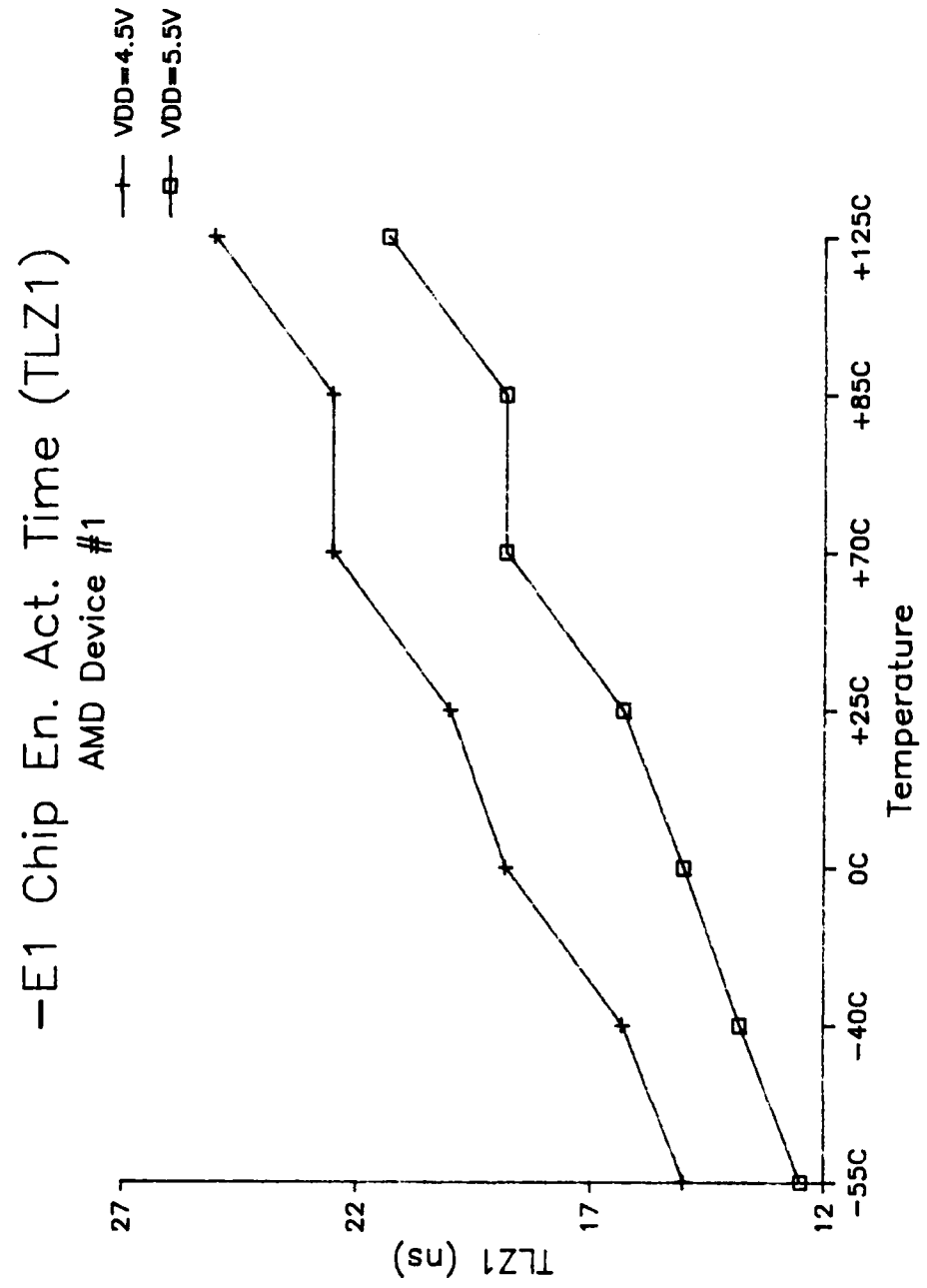


Figure 28: AMD Dev #1 Chip En. (-E1) Active Time vs Temperature

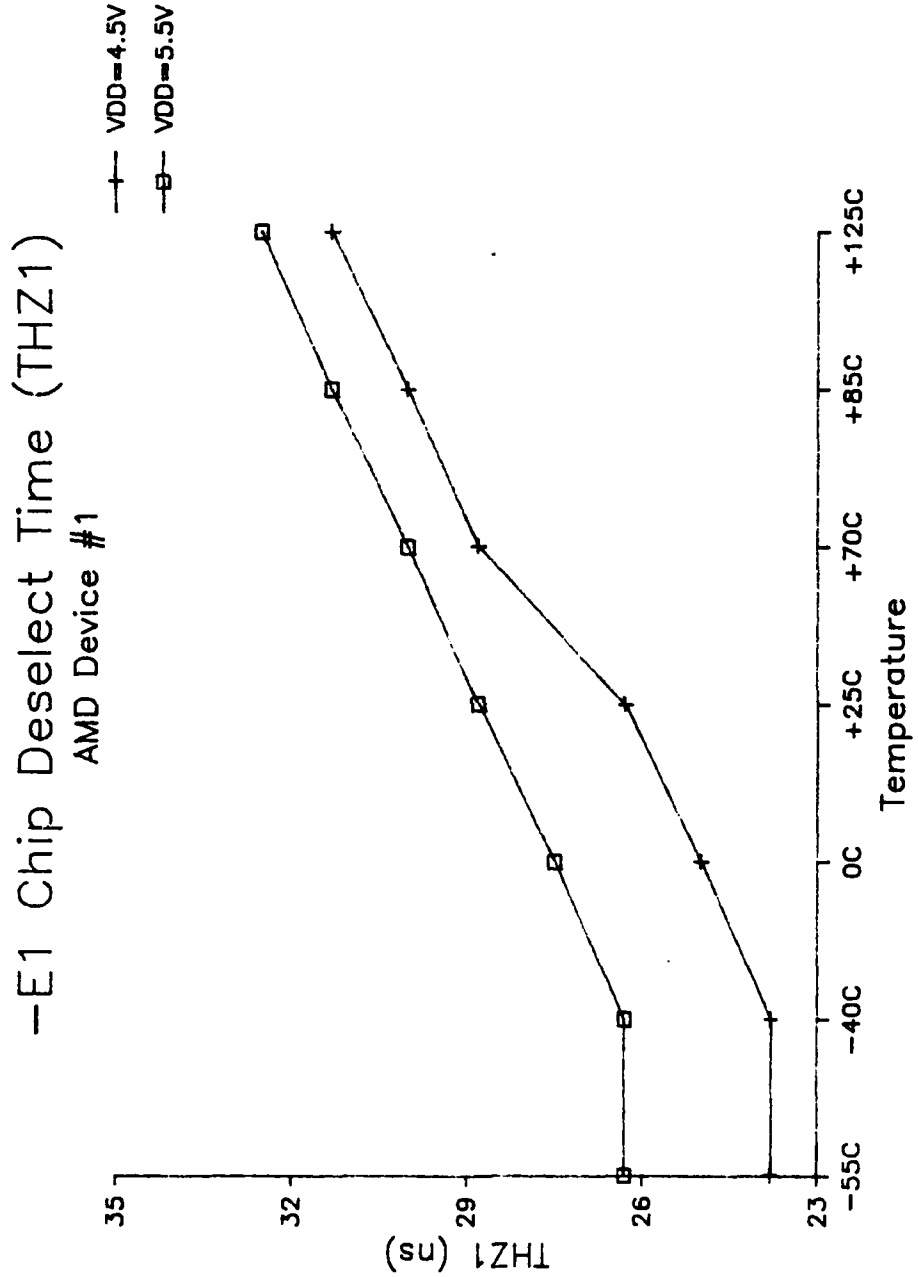


Figure 29: AMD Dev #1 Chip En. (-E1) Des Time vs Temperature

9. A.C. TIMING PARAMETER SHMOO PLOTS

9.1 TEST METHOD

SHMOO plots were taken for each of the twenty-one A.C. Timing parameters at 25°C, using a March pattern on one device each for AMD and Toshiba. These plots were accomplished using a new utility called 23SHMOO, supplied by Xincom. The utility option, which seemed to portray device performance the best, is the 3-Axis option. This utility integrates the A.C. characterization timing sets used in the test program, which are portrayed in Write and Read timing diagrams of Figures 11 and 12. The program input threshold levels were set to VIH = 2.4V and VIL = 0.6V. Output comparators were set to VOH = 1.5V and VOL = 1.5V, unless otherwise noted. These SHMOO plots were obtained interactively at the keyboard.

The following is a discussion of the SHMOO plots which are shown in Figures 30 through 43. Seven timing parameters out of twenty-one are displayed in the figures. For each plot the timing parameter is on the X-Axis, the input threshold voltage, VIL or VIH, is on the Y-Axis and VDD (VCC shown on the plot) is on the Z-Axis. Detailed information about Timing Set # (Ts), Start (St), Stop (Sp), and Step are also found on each plot.

As shown in Figures 30 through 39, PASSING > and FAILING = <. As shown in Figures 40 through 43, PASSING = > signifies that outputs are tri-stated, and FAILING = < signifies that the outputs are active. The plotting function is left to right, or from a failing to a passing condition on the X-Axis. The interpretation of the Z-Axis, unless otherwise noted, is that the first passing condition is a letter identified with a particular incremented value of VDD. Plotting is halted immediately, and the VDD supply is decremented until the next passing condition occurs and is recorded. Eventually, as the variable comparator strobe or other variable timing edge is incremented or decremented, a passing condition occurs for the respective timing parameter in the complete supply voltage range of VDD = 4.5V to VDD = 5.5V.

In addition to characterization of timing parameters with SHMOO plots, device performance is observed, with respect to input threshold voltage margins for VIL and VIH.

9.2 TEST SUMMARY

The SHMOO plots obtained for all twenty-one timing parameters gave good results and correlated closely to the measured timing parameters. The measured timing parameters may be different, because they are affected by the more complex ROWBAR test pattern, in addition to the March pattern. These plots were very helpful in establishing the Write and Read timing cycle timing sets for both General Function A.C. Pattern testing and A.C. Timing Parameter measurements.

The SHMOO plots obtained for all twenty-one timing parameters of a Toshiba device showed that the device can perform at tighter input threshold levels of VIH = 2.0V and VIL = 1.1V, as opposed to AMD input threshold levels of VIH = 2.4V and VIL = 1.0V.

The following is a discussion of seven of these plots for AMD device #1:

9.2.1 Address Access Time - TAVQV (TAA)

Figure 30 shows TAA vs VIH vs VDD, and Figure 31 shows TAA vs VIL vs VDD. The observed access time of 70.6ns is well within the spec of 100ns. The variable timing edge is the comparator strobe leading edge; the trailing edge is fixed in the passing zone.

9.2.2 Write Pulse Width - TWLWH (TWP)

Figure 32 shows TWP vs VIH vs VDD, and Figure 33 shows TWP vs VIL vs VDD. The observed Write Pulse Width is 26.3ns. The variable timing edge is the Write Pulse trailing edge; the fixed edge is Write Pulse leading edge.

9.2.3 Write Recovery Time - TWHAX (TWR)

Figure 34 shows TWR vs VIH vs VDD, and Figure 35 shows TWR vs VIL vs VDD. This timing parameter is also known as Address Hold time, which defines the minimum time that valid addresses must be presented after the Write Pulse ends. In the plots, the trailing edge of Write is moved with respect to the trailing edge of valid addresses. The plots show that TWR is -11.9ns, meaning that valid addresses can terminate at 11.9ns before the Write operation is completed, which is better than the +5ns spec.

9.2.4 Data Hold Time - TWHDX (TDH)

Figure 36 shows TDH vs VIH vs VDD, and Figure 37 shows TDH vs VIL vs VDD. This timing parameter defines the minimum time that valid input data must be present after the Write Pulse ends. In the plots, the trailing edge of Write is moved with respect to the trailing edge of valid data. The plots show that TDH

is -7.7ns, meaning that valid data can terminate 7.7ns before the Write operation is completed, which is better than the 0ns spec.

9.2.5 Data Setup Time - TDVWH (TDW)

Figure 38 shows TDW vs VIH vs VDD, and Figure 39 shows TDW vs VIL vs VDD. This timing parameter defines the minimum time that valid data must be present before the trailing edge of Write. The plots show that data setup can occur as little as 23.4ns before the end of the Write Pulse, which is better than the spec minimum of 40ns.

9.2.6 Chip Enable to Output Disable - TE1HQZ (THZ1)

Figure 40 shows THZ1 vs VIH vs VDD, and Figure 41 shows THZ1 vs VIL vs VDD. This timing parameter defines the maximum time that it takes for the device outputs to become disabled to a tri-state condition when Chip Enable -E1 is turned off. In the plots, the significance of PASSING = > means that the device is considered turned off when VOL is greater than VOLMAX +0.3V and VOH is less than VOHMIN -0.3V. The plots show that the outputs are considered to be turned off at 50.9ns after -E1 turns off, which is more than the spec value of 35ns max.

9.2.7 Chip Enable to Output Disable - TE1HQZ (THZ1)

Figure 42 shows THZ1 vs VDD vs VOH, and Figure 43 shows THZ1 vs VDD vs VOL. This is the same parameter as discussed in section 9.2.6 except that the plots show that within the supply voltage range of VDD= 4.5V to 5.5V, it takes greater than 75ns for the outputs to reach the tri-state reference VLOAD = 1.77V. This is affected by the total capacitance of the test head and performance board that are attached to each output pin.

```
3axis Shmoo Plot- NORMAL        (Date:03/20/86)        (Time:15:06:27)
-------------------------------------------------------------------------------
A=  5.50    B=  5.40    C=  5.30    D=  5.20    E=  5.10    F=  5.00
G=  4.90    H=  4.80    I=  4.70    J=  4.60    K=  4.50    L=  4.40
PASSING =)  FAILING =(
-------------------------------------------------------------------------------
Dut/Test#-    1    94

AMD AM99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=2.4V,.6V

VIH   (V )                VCC   (V )

4.000  !((((((((((((((((BDGIK))))))))))))))))))))))))))))))
3.800  !((((((((((((((((BEGIK))))))))))))))))))))))))))))))
3.600  !((((((((((((((((CEHJK))))))))))))))))))))))))))))))
3.400  !((((((((((((((((CEHJK))))))))))))))))))))))))))))))
3.200  !((((((((((((((((CFHJL))))))))))))))))))))))))))))))
3.000  !((((((((((((((((DFHJL))))))))))))))))))))))))))))))
2.800  !((((((((((((((((DFIJL))))))))))))))))))))))))))))))
2.600  !((((((((((((((((CGIKL))))))))))))))))))))))))))))))
2.400  !((((((((((((((((BFIKL))))))))))))))))))))))))))))))
2.200  !((((((((((((((((EEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEE
2.000  !((((((((((((((((JJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJ
1.800  !((((((((((((((((((((((((((((((((((((((((((((((((((
1.600  !((((((((((((((((((((((((((((((((((((((((((((((((((
       !+----+----+----+----+----+----+----+----+----+----+
       !30.0      50.3      70.6      90.9      111.3

                          TAA   (NS)

( XAXIS )       Name: TAA        Reference:  200.0NS          Steps:    46
-------------------------------------------------------------------------------
 0) Device= CMPST   @10US  Ts= 0   St= 230.0NS   Sp= 321.4NS   Step=   2.0NS

( YAXIS )       Name: VIH        Reference:  0.000V           Steps:    13
-------------------------------------------------------------------------------
 0) Device= ADDHI   @10V   Ts= 0   St= 4.000V    Sp= 1.600V    Step= 0.200V
 1) Device= DTAHI   @10V   Ts= 0   St= 4.000V    Sp= 1.600V    Step= 0.200V
 2) Device= CK1HI   @10V   Ts= 0   St= 4.000V    Sp= 1.600V    Step= 0.200V
 3) Device= CK3HI   @10V   Ts= 0   St= 4.000V    Sp= 1.600V    Step= 0.200V

( ZAXIS )       Name: VCC        Reference:  0.00V            Steps:    12
-------------------------------------------------------------------------------
 0) Device= VCC     @20V   Ts= 6   St=  5.50V    Sp=  4.40V    Step=  0.10V
```

Figure 30: SHMOO Plot Address Access Time vs VIH vs VDD Dev #1

```
3axis Shmoo Plot- NORMAL      (Date:03/19/86)       (Time:14:09:21)
-------------------------------------------------------------------------------
A=  5.50    B=  5.40    C=  5.30    D=  5.20    E=  5.10    F=  5.00
G=  4.90    H=  4.80    I=  4.70    J=  4.60    K=  4.50
PASSING =)  FAILING =(
-------------------------------------------------------------------------------
Dut/Test#-     1    94

AMD 99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=2.4V,.6V

VIL   (V )              VCC   (V )

1.500  !((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((
1.400  !((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((
1.300  !((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((
1.200  !(((((((((((((((BDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDD
1.100  !(((((((((((((((BDGIJ))))))))))))))))))))))))))))))))))))))))))
1.000  !(((((((((((((((BEGIK))))))))))))))))))))))))))))))))))))))))))
0.900  !(((((((((((((((CEHJK))))))))))))))))))))))))))))))))))))))))))
0.800  !(((((((((((((((CEHJ)))))))))))))))))))))))))))))))))))))))))))
0.700  !(((((((((((((((CFHJ)))))))))))))))))))))))))))))))))))))))))))
0.600  !(((((((((((((((CFHJ)))))))))))))))))))))))))))))))))))))))))))
0.500  !(((((((((((((((CFIK)))))))))))))))))))))))))))))))))))))))))))
0.400  !(((((((((((((((CFIK)))))))))))))))))))))))))))))))))))))))))))
0.300  !(((((((((((((((CFIK)))))))))))))))))))))))))))))))))))))))))))
0.200  !(((((((((((((((CFIK)))))))))))))))))))))))))))))))))))))))))))
0.100  !(((((((((((((((CFIK)))))))))))))))))))))))))))))))))))))))))))
0.000  !(((((((((((((((CFIK)))))))))))))))))))))))))))))))))))))))))))
       !+----+----+----+----+----+----+----+----+----+----+----+----+
       !30.0      50.3      70.6      90.9      111.3

                        TAA   (NS)

( XAXIS )       Name: TAA        Reference:  200.0NS          Steps:    46
-------------------------------------------------------------------------------
 0) Device= CMPST   @10US  Ts= 0   St= 230.0NS   Sp= 321.4NS   Step=   2.0NS

( YAXIS )       Name: VIL        Reference:  0.000V           Steps:    16
-------------------------------------------------------------------------------
 0) Device= ADDLO   @10V   Ts= 0   St= 1.500V    Sp= 0.000V    Step= 0.100V
 1) Device= DTALO   @10V   Ts= 0   St= 1.500V    Sp= 0.000V    Step= 0.100V
 2) Device= CK1LO   @10V   Ts= 0   St= 1.500V    Sp= 0.000V    Step= 0.100V
 3) Device= CK3LO   @10V   Ts= 0   St= 1.500V    Sp= 0.000V    Step= 0.100V

( ZAXIS )       Name: VCC        Reference:  0.00V            Steps:    11
-------------------------------------------------------------------------------
 0) Device= VCC     @20V   Ts= 0   St=  5.50V    Sp=  4.50V    Step=  0.10V
```

Figure 31: SHMOO Plot Address Access Time vs VIL vs VDD Dev #1

```
3axis Shmoo Plot- NORMAL      (Date:03/21/86)       (Time:11:45:44)
-------------------------------------------------------------------------------
A=  5.50    B=  5.40    C=  5.30    D=  5.20    E=  5.10    F=  5.00
G=  4.90    H=  4.80    I=  4.70    J=  4.60    K=  4.50
PASSING =)  FAILING =(
-------------------------------------------------------------------------------
Dut/Test#-     1    94

AMD AM99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=2.4V,.6V

VIH   (V )             VCC   (V )

4.000  !(((((((F)))))))))))))))))))))))))))))))
3.800  !(((((((G)))))))))))))))))))))))))))))))
3.600  !(((((((H)))))))))))))))))))))))))))))))
3.400  !(((((((BI)))))))))))))))))))))))))))))))
3.200  !((((((DK))))))))))))))))))))))))))))))))
3.000  !((((((F))))))))))))))))))))))))))))))))
2.800  !((((((H))))))))))))))))))))))))))))))))
2.600  !((((((DJ))))))))))))))))))))))))))))))))
2.400  !((((((G))))))))))))))))))))))))))))))))
2.200  !((((EK))))))))))))))))))))))))))))))))
2.000  !((((HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
1.800  !(((JJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJ
1.600  !(((((((((((((((((((((((((((((((((((((
       !+----+----+----+----+----+----+----+
       !10.0      30.3      50.6      70.9

                        TWP   (NS)

( XAXIS )       Name: TWP        Reference:  300.0NS          Steps:    36
-------------------------------------------------------------------------------
 0) Device= WENSP   @10US  Ts= 6   St= 310.0NS   Sp= 381.1NS   Step=   2.0NS

( YAXIS )       Name: VIH        Reference:  0.000V           Steps:    13
-------------------------------------------------------------------------------
 0) Device= ADDHI   @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V
 1) Device= DTAHI   @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V
 2) Device= CK1HI   @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V
 3) Device= CK3HI   @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V

( ZAXIS )       Name: VCC        Reference:   0.00V           Steps:    11
-------------------------------------------------------------------------------
 0) Device= VCC     @20V   Ts= 0   St=  5.50V    Sp=  4.50V    Step=  0.10V
```

Figure 32: SHMOO Plot Write Pulse Width vs VIH vs VDD Dev #1

```
3axis Shmoo Plot- NORMAL      (Date:03/20/86)       (Time:13:07:28)
-------------------------------------------------------------------------------
A=  5.50    B=  5.40    C=  5.30    D=  5.20    E=  5.10    F=  5.00
G=  4.90    H=  4.80    I=  4.70    J=  4.60    K=  4.50    L=  4.40
PASSING =)  FAILING =(
-------------------------------------------------------------------------------
Dut/Test=-     1    94

AMD AM99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=2.4V,.6V

VIL   (V )            VCC   (V )

1.500  !((((((((((((((((((((((((((((((((((((((((
1.400  !((((((((((((((((((((((((((((((((((((((((
1.300  !((((((((((((((((((((((((((((((((((((((((
1.200  !((((((CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
1.100  !(((((BFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
1.000  !(((((DI))))))))))))))))))))))))))))))))
0.900  !(((((FK))))))))))))))))))))))))))))))))
0.800  !(((((GL))))))))))))))))))))))))))))))))
0.700  !((((BI))))))))))))))))))))))))))))))))
0.600  !((((CJ))))))))))))))))))))))))))))))))
0.500  !((((EK))))))))))))))))))))))))))))))))
0.400  !((((FL))))))))))))))))))))))))))))))))
0.300  !((((F))))))))))))))))))))))))))))))))
0.200  !((((G))))))))))))))))))))))))))))))))
0.100  !((((H))))))))))))))))))))))))))))))))
0.000  !((((BI))))))))))))))))))))))))))))))))
       !+----+----+----+----+----+----+----+
       !10.0      30.3      50.6      70.9

                      TWP   (NS)

( XAXIS )       Name: TWP        Reference:  300.0NS          Steps:    36
-------------------------------------------------------------------------------
 0) Device= WENSP   @10US  Ts= 6   St= 310.0NS   Sp= 381.1NS   Step=   2.0NS

( YAXIS )       Name: VIL        Reference:  0.000V           Steps:  . 16
-------------------------------------------------------------------------------
 0) Device= ADDLO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 1) Device= DTALO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 2) Device= CK1LO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 3) Device= CK3LO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V

( ZAXIS )       Name: VCC        Reference:   0.00V           Steps:    12
-------------------------------------------------------------------------------
 0) Device= VCC     @20V   Ts= 6   St=  5.50V    Sp=  4.40V    Step=  0.10V
```

Figure 33: SHMOO Plot Write Pulse Width vs VIL vs VDD Dev #1

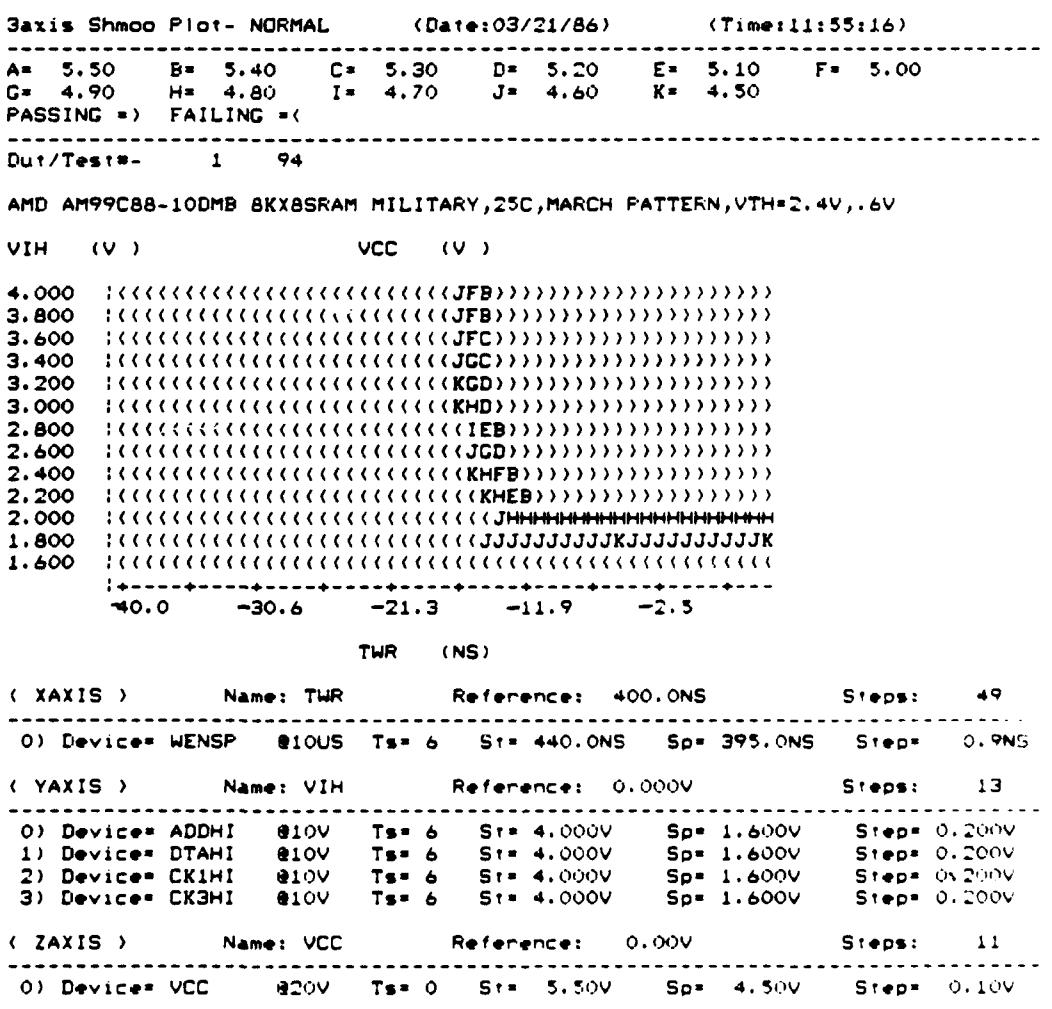
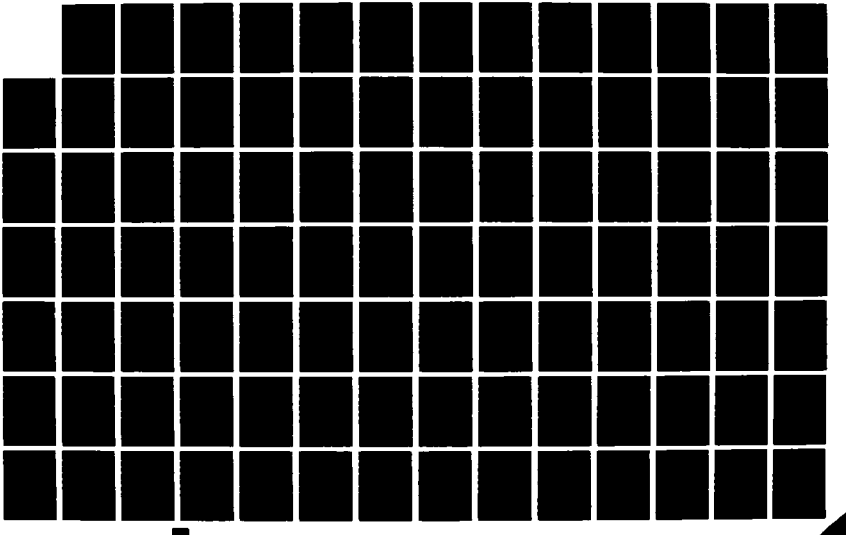


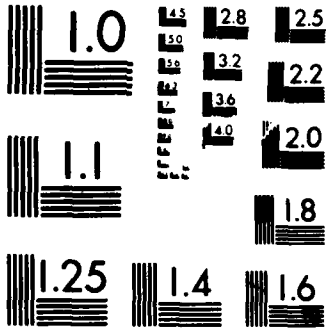
Figure 34: SHMOO Plot Write Recovery Time vs VIH vs VDD Dev #1

```
3axis Shmoo Plot- NORMAL      (Date:03/20/86)      (Time:14:20:45)
-------------------------------------------------------------------------------
A=  5.50    B=  5.40    C=  5.30    D=  5.20    E=  5.10    F=  5.00
G=  4.90    H=  4.80    I=  4.70    J=  4.60    K=  4.50    L=  4.40
PASSING =)  FAILING =(
-------------------------------------------------------------------------------
Dut/Test=-     1    94

AMD AM99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=2.4V,.6V

VIL   (V )                  VCC   (V )

1.500  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((
1.400  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((
1.300  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((
1.200  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((CCCCCCCCCCCCCCCC
1.100  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((DFFFFFFFFFFFFFFFF
1.000  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((LJGD))))))))))))))))
0.900  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((LJGE))))))))))))))))
0.800  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((JGE))))))))))))))))
0.700  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((JGE))))))))))))))))
0.600  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((JGE))))))))))))))))
0.500  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((JHE))))))))))))))))
0.400  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((JHE))))))))))))))))
0.300  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((JHE))))))))))))))))
0.200  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((KHE))))))))))))))))
0.100  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((KHE))))))))))))))))
0.000  :((((((((((((((((((((((((((((((((((((((((((((((((((((((((KHE))))))))))))))))
       :+----+----+----+----+----+----+----+----+----+----+----+----+----+----+---
       -40.0     -30.6     -21.3     -11.9     -2.5

                           TWR   (NS)

( XAXIS )       Name: TWR         Reference:  400.0NS          Steps:    49
-------------------------------------------------------------------------------
 0) Device= WENSP   @10US  Ts= 6   St= 440.0NS   Sp= 395.0NS   Step=  0.9NS

( YAXIS )       Name: VIL         Reference:  0.000V           Steps:    16
-------------------------------------------------------------------------------
 0) Device= ADDLO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 1) Device= DTALO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 2) Device= CK1LO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 3) Device= CK3LO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V

( ZAXIS )       Name: VCC         Reference:   0.00V           Steps:    12
-------------------------------------------------------------------------------
 0) Device= VCC     @20V   Ts= 6   St=  5.50V    Sp=  4.40V    Step=  0.10V
```

Figure 35: SHMOO Plot Write Recovery Time vs VIL vs VDD Dev #1

AD-A180 114 ELECTRICAL CHARACTERIZATION OF VLSI RAMS AND PROMS(U) 4/5
GTE COMMUNICATIONS SYSTEMS CORP PHOENIX AZ
M FORMOSO ET AL. OCT 86 RADC-TR-86-188 F30602-84-C-0070
UNCLASSIFIED F/G 12/6 NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

```
3axis Shmoo Plot- NORMAL      (Date:03/21/86)       (Time:12:14:56)
-------------------------------------------------------------------------------
A=  5.50    B=  5.40    C=  5.30    D=  5.20    E=  5.10    F=  5.00
G=  4.90    H=  4.80    I=  4.70    J=  4.60    K=  4.50
PASSING =)  FAILING =(
-------------------------------------------------------------------------------
Dut/Test#-     1    94

AMD AM99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=2.4V,.6V

VIH   (V )            VCC   (V )

4.000  !((((((((((((((((((((JE))))))))))))))))))))
3.800  !((((((((((((((((((((JE))))))))))))))))))))
3.600  !((((((((((((((((((((JE))))))))))))))))))))
3.400  !((((((((((((((((((((KF))))))))))))))))))))
3.200  !((((((((((((((((((((KF))))))))))))))))))))
3.000  !((((((((((((((((((((G))))))))))))))))))))
2.800  !((((((((((((((((((((H))))))))))))))))))))
2.600  !((((((((((((((((((((IC))))))))))))))))))))
2.400  !((((((((((((((((((((JE))))))))))))))))))))
2.200  !((((((((((((((((((((HC))))))))))))))))))))
2.000  !((((((((((((((((((((JHHHHHHHHHHHH
1.800  !((((((((((((((((((((JJJJJJJJJJJJ
1.600  !((((((((((((((((((((((((((((((((
       !+----+----+----+----+----+----+----
       -30.0     -20.6     -11.3     -1.9

                      TDH   (NS)

( XAXIS )       Name: TDH        Reference:  400.0NS          Steps:    35
-------------------------------------------------------------------------------
 0) Device= WENSP   @10US  Ts= 6   St= 430.0NS   Sp= 398.1NS   Step=   0.9NS

( YAXIS )       Name: VIH        Reference:  0.000V           Steps:    13
-------------------------------------------------------------------------------
 0) Device= ADDHI   @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V
 1) Device= DTAHI   @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V
 2) Device= CK1HI   @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V
 3) Device= CK3HI   @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V

( ZAXIS )       Name: VCC        Reference:  0.00V            Steps:    11
-------------------------------------------------------------------------------
 0) Device= VCC     @20V   Ts= 0   St=  5.50V    Sp=  4.50V    Step=  0.10V
```

Figure 36: SHMOO Plot Data Hold Time vs VIH vs VDD Dev #1

```
3axis Shmoo Plot- NORMAL      (Date:03/20/86)       (Time:13:45:45)
-------------------------------------------------------------------------------
A=  5.50    B=  5.40    C=  5.30    D=  5.20    E=  5.10    F=  5.00
G=  4.90    H=  4.80    I=  4.70    J=  4.60    K=  4.50    L=  4.40
PASSING =)  FAILING =(
-------------------------------------------------------------------------------
Dut/Test#-     1    94

AMD AM99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=2.4V,.6V

VIL   (V )             VCC   (V )

1.500  !((((((((((((((((((((((((((((((((
1.400  !((((((((((((((((((((((((((((((((
1.300  !((((((((((((((((((((((((((((((((
1.200  !(((((((((((((((((((((((CCCCCCCCCC
1.100  !(((((((((((((((((((((((DFFFFFFFFF
1.000  !((((((((((((((((((((((JE))))))))))
0.900  !((((((((((((((((((((((JF))))))))))
0.800  !((((((((((((((((((((((JF))))))))))
0.700  !((((((((((((((((((((((KFB)))))))))
0.600  !((((((((((((((((((((((KGB)))))))))
0.500  !((((((((((((((((((((((KGC)))))))))
0.400  !((((((((((((((((((((((LGC)))))))))
0.300  !((((((((((((((((((((((LHC)))))))))
0.200  !((((((((((((((((((((((LHD)))))))))
0.100  !(((((((((((((((((((((HD)))))))))
0.000  !((((((((((((((((((((ID)))))))))
       !+----+----+----+----+----+----+----
       -30.0     -20.6     -11.3     -1.9

                       TDH   (NS)

( XAXIS )       Name: TDH        Reference:  400.0NS          Steps:    35
-------------------------------------------------------------------------------
 0) Device= WENSP   @10US  Ts= 6   St= 430.0NS   Sp= 398.1NS   Step=  0.9NS

( YAXIS )       Name: VIL        Reference:  0.000V           Steps:    16
-------------------------------------------------------------------------------
 0) Device= ADDLO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 1) Device= DTALO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 2) Device= CK1LO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 3) Device= CK3LO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V

( ZAXIS )       Name: VCC        Reference:  0.00V            Steps:    12
-------------------------------------------------------------------------------
 0) Device= VCC     @20V   Ts= 6   St=  5.50V    Sp=  4.40V    Step=  0.10V
```

Figure 37: SHMOO Plot Data Hold Time vs VIL vs VDD Dev #1

```
3axis Shmoo Plot- NORMAL        (Date:03/24/86)        (Time:13:21:02)
-------------------------------------------------------------------------------
A=  5.50    B=  5.40    C=  5.30    D=  5.20    E=  5.10    F=  5.00
G=  4.90    H=  4.80    I=  4.70    J=  4.60    K=  4.50
PASSING =)  FAILING =(
-------------------------------------------------------------------------------
Dut/Test#-      1     94

AMD AM99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=2.4V,.6V


VIH   (V )                VCC   (V )

4.000  !))))))))))))))))))))))))))))))))))))))))))))))))))))HC((((((((((((((((((((
3.800  !))))))))))))))))))))))))))))))))))))))))))))))))))))ID((((((((((((((((((((
3.600  !))))))))))))))))))))))))))))))))))))))))))))))))))))KF((((((((((((((((((((
3.400  !))))))))))))))))))))))))))))))))))))))))))))))))))))GB((((((((((((((((((((
3.200  !))))))))))))))))))))))))))))))))))))))))))))))))))))ID((((((((((((((((((((
3.000  !))))))))))))))))))))))))))))))))))))))))))))))))))))KFB((((((((((((((((((((
2.800  !))))))))))))))))))))))))))))))))))))))))))))))))))))HE((((((((((((((((((((
2.600  !))))))))))))))))))))))))))))))))))))))))))))))))))))KGB((((((((((((((((((((
2.400  !))))))))))))))))))))))))))))))))))))))))))))))))))))JE((((((((((((((((((((
2.200  !))))))))))))))))))))))))))))))))))))))))))))))))))))HC((((((((((((((((((((
2.000  !HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH((((((((((((((((((((
1.800  !JJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJJ((((((((((((((((((((
1.600  !((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((
       !+----+----+----+----+----+----+----+----+----+----+----+----+----+-
       !†60.0     ‡50.6     †41.3     ‡31.9     †22.5     ‡13.1     †3.8

                              TDW   (NS)

( XAXIS )        Name: TDW          Reference:  380.0NS           Steps:     62
-------------------------------------------------------------------------------
 0) Device= DATST    @10US  Ts= 6   St= 320.0NS   Sp= 377.2NS   Step=   0.9NS

( YAXIS )        Name: VIH          Reference:  0.000V            Steps:     13
-------------------------------------------------------------------------------
 0) Device= ADDHI    @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V
 1) Device= DTAHI    @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V
 2) Device= CK1HI    @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V
 3) Device= CK3HI    @10V   Ts= 6   St= 4.000V    Sp= 1.600V    Step= 0.200V

( ZAXIS )        Name: VCC          Reference:    0.00V           Steps:     11
-------------------------------------------------------------------------------
 0) Device= VCC      @20V   Ts= 6   St=  5.50V    Sp=  4.50V    Step=  0.10V
```

Figure 38: SHMOO Plot Data Setup Time vs VIH vs VDD Dev #1

```
3axis Shmoo Plot- NORMAL      (Date:03/24/86)       (Time:13:10:29)
-------------------------------------------------------------------------------
A=  5.50    B=  5.40    C=  5.30    D=  5.20    E=  5.10    F=  5.00
G=  4.90    H=  4.80    I=  4.70    J=  4.60    K=  4.50
PASSING =)  FAILING =(
-------------------------------------------------------------------------------
Dut/Test#-     1    94

AMD AM99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=2.4V,.6V


VIL  (V )              VCC  (V )

1.500  !((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((((
1.400  !(B((B(BB((BB(((B((((((B((((B((((B(((((((((((((((((((((((((((((((
1.300  !(B(B(((((((((((B((((((B(((((((((((((((((((B(((((((((((((((((((((
1.200  !FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFE(((((((((((((((((((((
1.100  !))))))))))))))))))))))))))))))))))))))))))))))))))))))JGC(((((((((((((((((((
1.000  !))))))))))))))))))))))))))))))))))))))))))))))))))))))KHD(((((((((((((((((((
0.900  !))))))))))))))))))))))))))))))))))))))))))))))))))))))JFB(((((((((((((((((((
0.800  !))))))))))))))))))))))))))))))))))))))))))))))))))))))KGD(((((((((((((((((((
0.700  !))))))))))))))))))))))))))))))))))))))))))))))))))))))HE(((((((((((((((((((
0.600  !))))))))))))))))))))))))))))))))))))))))))))))))))))))IF(((((((((((((((((((
0.500  !))))))))))))))))))))))))))))))))))))))))))))))))))))))JF(((((((((((((((((((
0.400  !))))))))))))))))))))))))))))))))))))))))))))))))))))))JG(((((((((((((((((((
0.300  !))))))))))))))))))))))))))))))))))))))))))))))))))))))KH(((((((((((((((((((
0.200  !))))))))))))))))))))))))))))))))))))))))))))))))))))))H(((((((((((((((((((
0.100  !))))))))))))))))))))))))))))))))))))))))))))))))))))))IB(((((((((((((((((((
0.000  !))))))))))))))))))))))))))))))))))))))))))))))))))))))IB(((((((((((((((((((
       !+----+----+----+----+----+----+----+----+----+----+----+----+-
       !160.0    150.6    141.3    131.9    122.5    113.1    103.8

                          TDW  (NS)

( XAXIS )       Name: TDW        Reference:  380.0NS          Steps:    62
-------------------------------------------------------------------------------
 0) Device= DATST   @10US  Ts= 6   St= 320.0NS   Sp= 377.2NS   Step=   0.9NS

( YAXIS )       Name: VIL        Reference:  0.000V           Steps:    16
-------------------------------------------------------------------------------
 0) Device= ADDLO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 1) Device= DTALO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 2) Device= CK1LO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V
 3) Device= CK3LO   @10V   Ts= 6   St= 1.500V    Sp= 0.000V    Step= 0.100V

( ZAXIS )       Name: VCC        Reference:  0.00V            Steps:    11
-------------------------------------------------------------------------------
 0) Device= VCC     @20V   Ts= 6   St=  5.50V    Sp=  4.50V    Step=  0.10V
```

Figure 39: SHMOO Plot Data Setup Time vs VIL vs VDD Dev #1

```
3axis Shmoo Plot- NORMAL      (Date:03/21/86)       (Time:11:28:08)
-------------------------------------------------------------------------------
A=  5.50    B=  5.40    C=  5.30    D=  5.20    E=  5.10    F=  5.00
G=  4.90    H=  4.80    I=  4.70    J=  4.60    K=  4.50
PASSING =)  FAILING =(
TRI-STATE    ACTIVE/VALID
-------------------------------------------------------------------------------
Dut/Test#-     1    94

AMD AM99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=2.4V,.6V

VIH   (V )            VCC   (V )

4.000  !((((((((((((((((HHFFEFECBBBB))))))))
3.800  !((((((((((((((((HHFFEEECBBBB))))))))
3.600  !((((((((((((((((HHFFEEEECBBBB))))))))
3.400  !((((((((((((((((HHFEEEECBBBB))))))))
3.200  !((((((((((((((((HHFEEEECBBBB))))))))
3.000  !((((((((((((((((HHFEEEECBBBB))))))))
2.800  !((((((((((((((((HHFEEEECBBBB))))))))
2.600  !((((((((((((((((IHFEEEECBBBB))))))))
2.400  !((((((((((((((((IHGEEEECBBBB))))))))
2.200  !((((((((((((((((IHGFFFEECCCBB))))))))
2.000  !((((((((((((((((IIIGFFFEEEEEEEEEECB
1.800  !((((((((((((((((IIIIGGHGHHGGGGGGGF
1.600  !GGGGGGGGGGGGGGGGGGGGGGGGGGGGGGGGGG
       !+----+----+----+----+----+----+----+
       !-10.0     10.3      30.6      50.9

                    THZ1  (NS)

( XAXIS )      Name: THZ1       Reference:  240.0NS          Steps:    36
-------------------------------------------------------------------------------
 0) Device= CMPST   @10US  Ts= 0   St= 230.0NS   Sp= 301.1NS   Step=  2.0NS

( YAXIS )      Name: VIH        Reference:  0.000V           Steps:    13
-------------------------------------------------------------------------------
 0) Device= ADDHI   @10V   Ts= 0   St= 4.000V    Sp= 1.600V    Step= 0.200V
 1) Device= DTAHI   @10V   Ts= 0   St= 4.000V    Sp= 1.600V    Step= 0.200V
 2) Device= CK1HI   @10V   Ts= 0   St= 4.000V    Sp= 1.600V    Step= 0.200V
 3) Device= CK3HI   @10V   Ts= 0   St= 4.000V    Sp= 1.600V    Step= 0.200V

( ZAXIS )      Name: VCC        Reference:  0.00V            Steps:    11
-------------------------------------------------------------------------------
 0) Device= VCC     @20V   Ts= 0   St=  5.50V    Sp=  4.50V    Step=  0.10V
```

Figure 40: SHMOO Plot -E1 Disable Time vs VIH vs VDD Dev #1

```
3axis Shmoo Plot- NORMAL      (Date:03/19/86)       (Time:15:10:55)
-------------------------------------------------------------------------------
A=  5.50    B=  5.40    C=  5.30    D=  5.20    E=  5.10    F=  5.00
G=  4.90    H=  4.80    I=  4.70    J=  4.60    K=  4.50
PASSING =)  FAILING =(
Test State    Active Value
-------------------------------------------------------------------------------
Dut/Test#-     1    94

AMD 99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=2.4V,.6V

VIL   (V )              VCC   (V )

1.500  !((((((((((GGGGGGGFFFFFFFFFFFFFFEDCCB)
1.400  !(((((((((((((((((KKKBKKJJBIBBBEF)))
1.300  !((((((((((((((((((BBBBBBBBCCCDI))))
1.200  !(((((((((((((((((CEEEEEEEEEEEEF)))))
1.100  !((((((((((((((((JJB)))K))K))))))))))
1.000  !(((((((((((((((II)))))))))))))))))
0.900  !(((((((((((((((JIB)))))))))))))))))
0.800  !((((((((((((((((IIB))))))))))))))))
0.700  !(((((((((((((((IIC)))))))))))))))))
0.600  !(((((((((((((((IIC)))))))))))))))))
0.500  !(((((((((((((((IIC)))))))))))))))))
0.400  !(((((((((((((((IIC)))))))))))))))))
0.300  !(((((((((((((((IID)))))))))))))))))
0.200  !(((((((((((((((IID)))))))))))))))))
0.100  !((((((((((((((((IIE))))))))))))))))
0.000  !((((((((((((((((IIE))))))))))))))))
       !+----+----+----+----+----+----+----+
       !-10.0     10.3      30.6      50.9

                        THZ1  (NS)

( XAXIS )       Name: THZ1        Reference:  240.0NS          Steps:    36
-------------------------------------------------------------------------------
 0) Device= CMPST   @10US  Ts= 0   St= 230.0NS   Sp= 301.1NS   Step=   2.0NS

( YAXIS )       Name: VIL         Reference:  0.000V           Steps:    16
-------------------------------------------------------------------------------
 0) Device= ADDLO   @10V   Ts= 0   St= 1.500V    Sp= 0.000V    Step= 0.100V
 1) Device= DTALO   @10V   Ts= 0   St= 1.500V    Sp= 0.000V    Step= 0.100V
 2) Device= CK1LO   @10V   Ts= 0   St= 1.500V    Sp= 0.000V    Step= 0.100V
 3) Device= CK3LO   @10V   Ts= 0   St= 1.500V    Sp= 0.000V    Step= 0.100V

( ZAXIS )       Name: VCC         Reference:   0.00V           Steps:    11
-------------------------------------------------------------------------------
 0) Device= VCC     @20V   Ts= 0   St=  5.50V    Sp=  4.50V    Step=  0.10V
```

Figure 41: SHMOO Plot -E1 Disable Time vs VIL vs VDD Dev #1

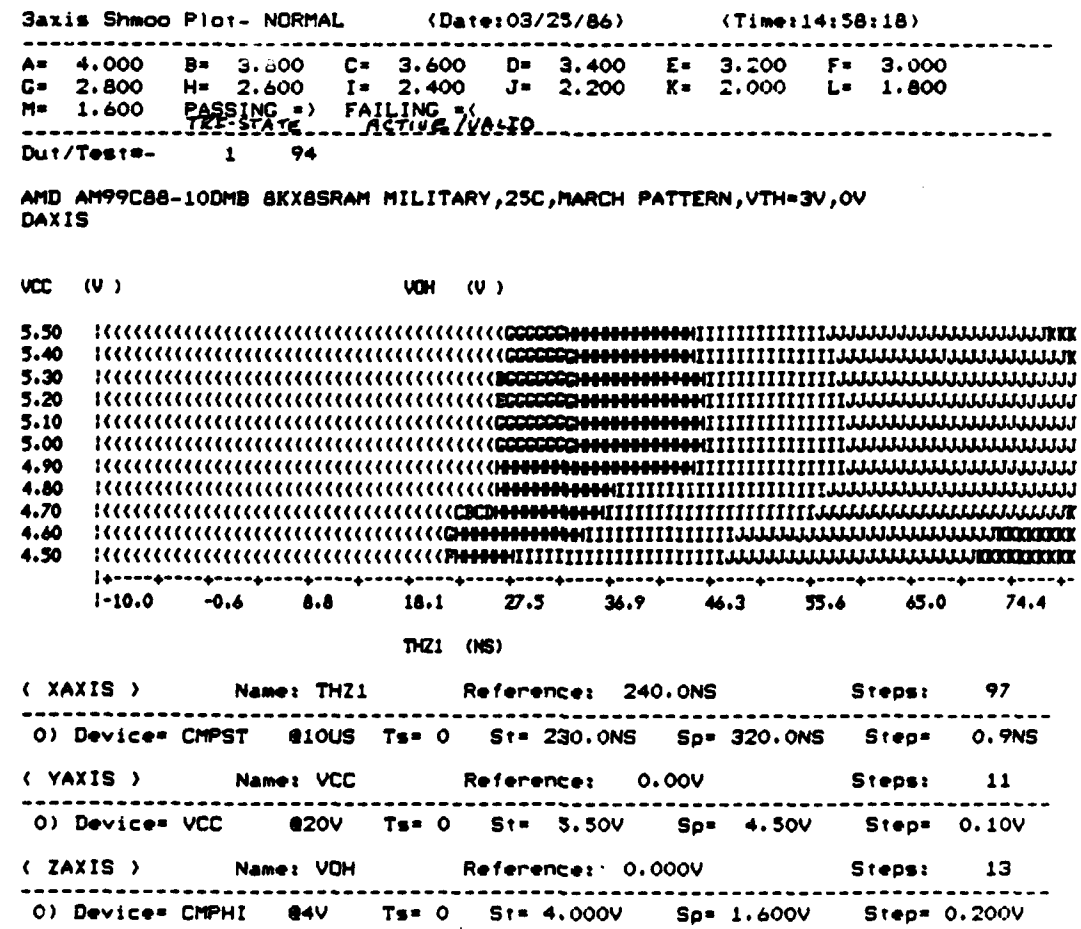


Figure 42: SHMOO Plot -E1 Disable Time vs VDD vs VOH Dev #1

```
3axis Shmoo Plot- NORMAL      (Date:03/25/86)       (Time:14:45:06)
-------------------------------------------------------------------------------
A= 2.000   B= 1.900   C= 1.800   D= 1.700   E= 1.600   F= 1.500
G= 1.400   H= 1.300   I= 1.200   J= 1.100   K= 1.000   L= 0.900
M= 0.800   N= 0.700   O= 0.600   P= 0.500   Q= 0.400   R= 0.300
S= 0.200   T= 0.100   U= 0.000   PASSING =)  FAILING =(
                                  TRI-STATE    ACTIVE/VALID
-------------------------------------------------------------------------------
Dut/Test=-     1    94

AMD AM99C88-10DMB 8KX8SRAM MILITARY,25C,MARCH PATTERN,VTH=3V,0V
DAXIS


VCC  (V )                          VOL  (V )

5.50  !(((((((((((((((((((((((((((((((((((((((((((((((SSSSSRRRQQQQQQQQPPPPOOOOOOOONNNNNNNNNNNNNNNNLLLLLLLLLLKKKKKKKK
5.40  !(((((((((((((((((((((((((((((((((((((((((((((((SSSSSRRRQQQQQQQPPPPPOOOOOOOONNNNNNNNNNNNNNNLLLLLLLLLLKKKKKKKKJ
5.30  !(((((((((((((((((((((((((((((((((((((((((((((((SSSSSRRRQQQQQQPPPPPPOOOOOOONNNNNNNNNNNNNNLLLLLLLLLKKKKKKKKJJ
5.20  !(((((((((((((((((((((((((((((((((((((((((((((((SSSSSRRRQQQQQPPPPPPOOOOOONNNNNNNNNNNNNNLLLLLLLLKKKKKKKKJJJJ
5.10  !(((((((((((((((((((((((((((((((((((((((((((((((SSSSRRRQQQQPPPPPPPOOOOONNNNNNNNNNNNNNLLLLLLLKKKKKKKKJJJJ
5.00  !(((((((((((((((((((((((((((((((((((((((((((((((SSSSRRRQQQQPPPPPPPOOOOONNNNNNNNNNNNNNLLLLLLLKKKKKKKKJJJJ
4.90  !(((((((((((((((((((((((((((UTTTSSSSSSSSRRRQQQQPPPPPPPPOOOONNNNNNNNNNNNNNLLLLLLLKKKKKKKKJJJJ
4.80  !(((((((((((((((((((((((((((UUUTTTSSSSSSSSRRRQQQQPPPPPPPPOOOONNNNNNNNNNNNNNLLLLLLLKKKKKKKKJJJJ
4.70  !(((((((((((((((((((((((((((UUUUTTSSSSSSSSRRRQQQPPPPPPPPOOOONNNNNNNNNNNNNNLLLLLLLKKKKKKKKJJJJ
4.60  !(((((((((((((((((((((((((((UUUUUTTSSSRRRRRRRQQQPPPPPPPPOOONNNNNNNNNNNNNNLLLLLLLKKKKKKKKJJJJJ
4.50  !(((((((((((((((((((((((((((UUUUUUUUUUUUUUUTTSSSSRRRRRRRQQQPPPPPPPPOOONNNNNNNNNNNNNNLLLLLLLKKKKKKKKJJJJJ
      !+----+----+----+----+----+----+----+----+----+----+----+----+----+----+----+----+----+----+-
      !-10.0    -0.6     8.8     18.1     27.5     36.9     46.3     55.6     65.0     74.4

                                THZ1  (NS)

( XAXIS )       Name: THZ1        Reference:  240.0NS          Steps:    97
-------------------------------------------------------------------------------
 0) Device= CMPST   @10US  Ts= 0   St= 230.0NS   Sp= 320.0NS   Step=  0.9NS

( YAXIS )       Name: VCC         Reference:   0.00V           Steps:    11
-------------------------------------------------------------------------------
 0) Device= VCC     @20V   Ts= 0   St=  5.50V    Sp=  4.50V    Step=  0.10V

( ZAXIS )       Name: VOL         Reference:  0.000V           Steps:    21
-------------------------------------------------------------------------------
 0) Device= CMPLO   @4V    Ts= 0   St= 2.000V    Sp= 0.000V    Step= 0.100V
```

Figure 43: SHMOO Plot -E1 Disable Time vs VDD vs VOL Dev #1

10. CONCLUSIONS

As a result of the device characterization, the following conclusions can be made:

- The worst case static and dynamic supply currents occur at -55°C.
- IIH and IIL measurements yielded extremely low current of 33nA or less over the full temperature range.
- IOZH and IOZL measurements yielded extremely low current of 40nA or less over the full temperature range.
- VOL and VOH measurements were within the proposed slash sheet limits.
- In all cases, the measured input and output capacitance values were below the specified limits.
- Worst case conditions for A.C. parameters were high temperature (125°C) and low voltage (4.5 volts).
- AMD guarantees the Am99C88-10DM to meet or exceed MIL-STD-883C only, but does not recommend the device for MIL-M-38510 status. In the first quarter of 1987, AMD will offer a 45ns, Am99C88H 8K X 8 SRAM, which they may recommend for MIL-M-38510.

APPENDIX A

FUNCTIONAL ALGORITHMS

Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. The algorithms were applied to the device in a topologically pure fashion.

Twelve test patterns were applied in sequence to the device under test (DUT) at the supply voltage, VDD = 4.5V. This sequence is repeated for VDD = 5.5V. Ten of these patterns are industry standard algorithms. Pattern 11 is derived from Pattern 1 (Checkerboard Up-count) for the Data Retention test. Pattern 12 is a One-Zero pattern for the Bit Unique test. Pattern 9 (Galloping Columns) gives the highest measured value of Average Operating current for D.C. parameter IDD1.

For A.C. Timing Parameter measurements, the March and Rowbar patterns were applied in sequence to the DUT for the timing at the supply voltage, VDD = 4.5V. This sequence was repeated for VDD = 5.5V. For each timing routine, multiple passes through memory were required, using the March address sequence for each pass. Between passes, the appropriate timing edge in the routine is incremented or decremented, as required, to cause a complete pass through memory without error. At this point, a more complex pattern, Rowbar, was applied to the DUT to further adjust the timing edge to allow the DUT to perform without error.

All twelve patterns used are listed by name as follows:

PATTERN 1 - CHECKERBOARD UPCOUNT
PATTERN 2 - X-PARITY
PATTERN 3 - Y-PARITY
PATTERN 4 - MARCH
PATTERN 5 - MULTIREAD MARCH
PATTERN 6 - SURROUND DISTURB
PATTERN 7 - ROWBAR
PATTERN 8 - GALLOPING ROWS
PATTERN 9 - GALLOPING COLUMNS
PATTERN 10 - ONE/ZERO ADDRESS COMPLEMENT
PATTERN 11 - CHECKERBOARD UPCOUNT (DATA RETENTION TEST)
PATTERN 12 - ONE-ZERO (BIT UNIQUE TEST)

Patterns 1, 4, 11, and 12 are discussed in detail as follows:

PATTERN 1

CHECKERBOARD UP-COUNT

This pattern ensures every cell can be written to a "1" and a "0" and adjacent cells (which are programmed to the opposite state) do not affect the cell under test. It is desirable to have a checkerboard by bit, that is, every bit in every byte is written to the opposite state of the bits above and below it and the bits to the right and left of it. It is performed in the following manner:

Step 1 - Write "AA" in all the columns of the even row numbers and write "55" in all the columns of the odd row numbers.
Step 2 - Sequentially read the entire memory across the rows.
Step 3 - Write "55" in all the columns of the even row numbers and write "AA" in all the columns of the odd row numbers.
Step 4 - Sequentially read the entire memory across the rows.

PATTERN 4

MARCH DATA, DATA BACKGROUND = ALL "FF"

This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1 - Load memory with background data.
Step 2 - Read location 0.
Step 3 - Write data complement in location 0.
Step 4 - Repeat steps 2 and 3 for all other locations in memory (sequentially).
Step 5 - Read data complement at location 0.
Step 6 - Write data at location 0.
Step 7 - Repeat steps 5 and 6 for all other locations in memory (sequentially).

PATTERN 11

CHECKERBOARD UP-COUNT (DATA RETENTION TEST)

This test verifies that the DUT will retain a Checkerboard pattern, while the supply voltage is reduced to the data retention level of VDR = 2V. It is performed in the following manner :

Step 1 - Write "AA" in all the columns of the even row numbers and write "55" in all the columns of the odd row numbers of the DUT at VDD = 4.5V.
Step 2 - Disable the DUT with Chip Enable control E2 = 0.2V.
Step 3 - Reduce the supply voltage to the data retention level of VDR = 2V.
Step 4 - Wait 5 seconds.
Step 5 - Restore the supply voltage to VDD = 4.5V.
Step 6 - Enable the DUT with Chip Enable control E2 = 2.4V.
Step 7 - Read the DUT for retention of the Checkerboard pattern.
Step 8 - Repeat Steps 1 through 7 for VDD = 5.5V.

PATTERN 12

ONE-ZERO (BIT UNIQUE TEST)

This algorithm is a One-Zero pattern, which verifies that every bit within a byte is unique (two bits in a byte are not shorted). The one-zero data, written in the DUT for the bit being tested, will be the complement of the other seven bits. In the following sequence of steps, a logic "0" signifies true data, and a logic "1" signifies complemented data:

Step 1 - Write data = 00000001 (1 hex) in the entire device.
Step 2 - Sequentially read the device.
Step 3 - Write data = 00000010 (2 hex) in the entire device.
Step 4 - Sequentially read the device.
Step 5 - Write data = 00000100 (4 hex) in the entire device.
Step 6 - Sequentially read the device.
Step 7 - Write data = 00001000 (8 hex) in the entire device.
Step 8 - Sequentially read the device.
Step 9 - Write data = 00010000 (10 hex) in the entire device.
Step 10- Sequentially read the device.
Step 11- Write data = 00100000 (20 hex) in the entire device.
Step 12- Sequentially read the device.
Step 13- Write data = 01000000 (40 hex) in the entire device.
Step 14- Sequentially read the device.
Step 15- Write data = 10000000 (80 hex) in the entire device.
Step 16- Sequentially read the device.

Step 17- Write data = 11111110 (FE hex) in the entire device.
Step 18- Sequentially read the device.
Step 19- Write data = 11111101 (FD hex) in the entire device.
Step 20- Sequentially read the device.
Step 21- Write data = 11111011 (FB hex) in the entire device.
Step 22- Sequentially read the device.
Step 23- Write data = 11110111 (F7 hex) in the entire device.
Step 24- Sequentially read the device.
Step 25- Write data = 11101111 (EF hex) in the entire device.
Step 26- Sequentially read the device.
Step 27- Write data = 11011111 (DF hex) in the entire device.
Step 28- Sequentially read the device.
Step 29- Write data = 10111111 (BF hex) in the entire device.
Step 30- Sequentially read the device.
Step 31- Write data = 01111111 (7F hex) in the entire device.
Step 32- Sequentially read the device.

TABLE OF CONTENTS

256K CMOS DRAM

LIST OF FIGURES

1. SUMMARY

1.1 OBJECTIVES/RESULTS

The objectives of this portion of the contract were as follows:

- o Develop and refine a test philosophy for 256K Dynamic RAMs that can be used for preparing a MIL-M 38510 detail specification.
- o Perform an electrical characterization on a sample group of devices over the military temperature range.
- o Generate a draft MIL-M-38510 slash sheet specification for the 256K dynamic RAM using characterization data as a basis for establishing performance limits.

This report summarizes the results of the testing of 36 sample devices (MC51C256-15) from Intel Corp. An extensive set of AC and DC parameters were measured utilizing the vendor's stated conditions for device characterization, and covering the military temperature range.

In general, the devices performed well within the values proposed by the vendor in his commercial device specifications, with only minor exceptions. These values were utilized in the generation of the MIL-M-38510 detail specification.

2. INTRODUCTION

2.1 OBJECTIVES

The objective of this effort is to establish the electrical characteristics of the CMOS 256K Dynamic RAM and use this data to develop a preliminary MIL-M-38510 slash sheet. Some of the specific activities involved were:

- o Establish the availability of a vendor prepared to produce a device to military requirements.
- o Select and obtain characterization sample devices.
- o Develop test programs and procedures compatible with automatic test equipment, where possible, or establish bench test setups.
- o Determine parametric limits and verify through device characterization.
- o Prepare preliminary slash sheet based on device testing and vendor information.

2.2 BACKGROUND

Originally the NMOS version of the 256K Dynamic RAM device was proposed for inclusion in this program. As a result of discussions with RADC, it was decided that the technology should be changed to the CMOS version, since the NMOS device was being characterized under another contract. At the time of the initial contract award, the only manufacturer of this device type was Intel. Subsequently, Intel made the decision to cease the production of this line of parts. The evaluation samples had, however, already been obtained. This left the program without an available source for production devices.

More recently, additional vendors, namely Advanced Micro Devices Inc., Inmos Corporation, and Micron Technology Inc., have indicated that they will be developing CMOS devices with the capability of meeting the Military requirements. They also indicated that they either had received or were in the process of obtaining MIL line certification. On the basis of this information, the program has continued with the data being taken on the only available samples from Intel.

The development of the 256K DRAM using the CMOS technology was targeted to provide the user community with added benefits that were not present in the NMOS variety of the same density DRAM. One feature of particular note is the very fast -CAS access time, which allows for a wide variation in the address multiplex and latch timing constraints. Other CMOS characteristics, such as extended refresh providing a low power mode, were among early considerations, but have not, as yet, been implemented.

Detailed explanations of the operation of dynamic RAMs are covered in many commercial publications and manufacturers' data books and will not be covered here.

This report is comprised of a quantity of reduced data which validates the limits that have been established in the proposed specification.

3. DESCRIPTION OF DEVICE TYPE

3.1 GENERAL ASPECTS OF DYNAMIC RAMS

The 256K DRAM is a 5-volt only, 262,144-bit device produced utilizing CMOS technology. The input and output signals use standard TTL signal levels rather than MOS levels. The device is organized as 262,144 words of 1 bit length. The structure is intended for such applications where large memory capability is required or where nonstandard word lengths, such 9 or 18 bits, are used.

3.2 SPECIFIC CONSIDERATIONS OF THE CMOS STRUCTURE

When using or testing devices manufactured with the CMOS process, there is a specific characteristic called latch-up that must be dealt with, which is not present with bipolar or NMOS structures. This problem can occur, and is quite destructive to the device, when care is not taken in properly applying the power or signals to the device pins. While many NMOS or bipolar type devices are not damaged by the reversal of the power pins, this condition is catastrophic to the CMOS device. Another such condition that should be avoided is the applying of signal levels, including transients, which will take an input higher than VDD. Also, line transients which drive the data output below VSS must be eliminated.

3.3 SYSTEM CONSIDERATIONS

In creating a circuit design which will be running the devices near their maximum speed, care must be taken in producing the printed circuit layout. Negative excursions on the input signals, caused by transmission line effects, must not exceed the maximum limit. This requires tight control of the printed circuit trace characteristics and the possible use of damping or terminating resistors to provide the best possible wave shape for maximum speed and minimum negative overshoot. Excessive negative potential on the input pins can cause the input structures to become conductive and cause device malfunction or destruction.

4. DEVELOPMENT OF AUTOMATIC AND BENCH TESTS

4.1 AUTOMATIC TEST EQUIPMENT

The test equipment used to characterize the 256K DRAM is a Fairchild Xincom 5588 Automatic Test System The system's main processor is a Zilog Z8000 microprocessor. This processor handles all test sequences and test processes. Included in the system is a subsystem which is called the Test Pattern Computer (TPC).

The TPC is a modular subassembly which has the capability to microprogram an assortment of test patterns, including such popular industry standards as: Ping Pong, Checkerboard and March. Patterns are defined by a set of 48-bit microcoded instructions executed within the TPC at functional rates up to 25MHz (40ns cycle time). Upon command from the main processor, the TPC generates the desired pattern and sends this pattern to the system for use in the stimulus to input pins and response checking of the output pin.

Some additional features of the TPC are

- o ECL Construction
- o Topological Address Scrambler
- o Address Indexing, Refresh Testing, Butterfly Patterns
- o Truth-Table RAM (Pattern RAM For EPROMS)
- o Algorithmic Pattern Generation
- o Loop Counters
- o Timing Set Selection on the fly

In addition to the TPC other system capabilities include:

- o 14 programmable clock phases
- o 4 programmable power supplies
- o 24 address lines

- o 16 data comparators
- o Parametric Measurement Unit (PMU)
- o Advanced Error Logging System (AELS)
- o IEEE 488 Bus Interface
- o Color Computer Graphics Display
- o Auto Data Logging to Data General Eclipse Host Computer

To interface the device under test (DUT) to the test system, an interface board is used to electrically connect the DUT's pins to the specific test system pin electronic cards. A zero insertion force socket is used to allow for fast removal and insertions of the DUT without causing lead damage.

4.2 BENCH TEST EQUIPMENT

Some non-ATE instruments were required to perform the Electrostatic Discharge and Capacitance Measurement tests.

The Electrostatic Discharge test unit used is an IMCS Corporation, Model number 2400C.

Features include:

- o 0-10,000 Volt Continuously Adjustable
- o 4.5 Digital Display of HV
- o Programmable Pulse Sequence
- o Curve Tracer Output
- o 1-128 pin Configuration
- o Applicable to MIL-STD-883 and MIL-STD-1686

The Capacitance Analyzer used is a Hewlett Packard, Model number 4192A, probe model number HP-16048C.

Features include:

- o 5Hz to 13MHz variable measuring frequency
- o Gain-Phase measurement: amplitude, phase and delay
- o Floating or Grounded devices
- o Frequency accuracy +/- 50ppm

5. STATIC CHARACTERISTICS

5.1 OBJECTIVES

A major goal of this portion of the contract was to characterize the DC parameters of the 256K DRAM device. This was accomplished by utilizing, as much as possible, Automatic Test Equipment (ATE) which could reliably execute a group of measurements and establish test conditions with accuracy and repeatability.

5.2 TEST METHODS

The Xincom 5588 memory test system previously described was used to collect data on the DC parametric measurements. The tester allowed data to be taken on each device in an accelerated and accurate manner. The DC measurements were taken on the entire sample of 36 devices. By using this size sample group the measurement values provide a better feel for the "trend" or range of values for a specific parameter than a smaller sample size. The tests performed on the Xincom were for the measurement of the VDD(oper), VIH, VIL, IIL, VOH, VOL, IOL, IDD1, IDD2, and IDD3 parameters. Test temperatures used were $-55^{o}C$, $+25^{o}C$ and $+125^{o}C$. Note that every test was performed at each temperature and worst case voltage.

5.2.1 VDD(operating) TEST

The intent of this test is to determine the voltage range over which the device will operate while staying within the maximum ratings. The acceptability of operation is established with nominal timing conditions while running a checkerboard pattern. Figure 1 shows the range of minimum operating supply voltage for the sample of 36 devices over the temperature range.

5.2.2 VIH, VIL TEST

This test is performed to determine the range of input voltages that are accepted by the individual device as valid logic "0" and logic "1." Due to the nature of this test, an actual measurement of the VIL minimum or the VIH maximum input parameters can lead to device damaging conditions. Thus, only the VIL maximum and VIH minimum values were measured, and the VIL minimum and VIH maximum values were only verified as meeting the vendor's stated limits. Figures 2 and 3 show the range of values found for the maximum logic "0" on the address and

clock inputs respectively. Figures 4 and 5 show the range of values found for the maximum logic "1" on the address and clock inputs respectively.

5.2.3 IIH, IIL TEST

The IIH and IIL tests are done to determine the amount of current drawn when the inputs have a specified voltage applied to them. This test is conducted by driving an input high or low and measuring the resultant current. Test levels for this parameter were Vin=0V (for IIL) and Vin=5.5V (for IIH), with VDD=5.5V. The worst case condition for leakage is when Vin equals 5.5 Volts.

Leakage measurements were performed at $-55^{o}C$, $+25^{o}C$ and $+125^{o}C$. The specified limits were +/- 10uA. In general, all measurements yielded extremely low currents of 200nA or less. Currents of these magnitudes are typical in LSI devices using CMOS technology.

5.2.4 VOH, VOL TEST

This test is performed to measure the resultant voltage level on the output when driving a load. For this, test currents are forced into the output and the resulting voltage is measured. The forcing current used for the VOH test is -5.0 mA with VDD=4.5 V. The current used for the VOL measurement is 4.2 mA with VDD=5.5 V. Note that the worst case condition for the output voltage is with VDD set at 4.5 Volts. This is not necessarily the worst case for other parameters.

The worst case values versus temperature are plotted in Figure 6. Note that in both tests the minimum VOH (2.4V) was never violated, however the maximum VOL (0.40V) was exceeded by seven devices at either $25^{o}C$ or $125^{o}C$. Retesting of these devices at $110^{o}C$ showed that all met the proposed specification value, *however some tighter screening by the vendor at outgoing inspection could* eliminate the $125^{o}C$ failures.

5.2.5 IOZH, IOZL TEST

This test measures the output leakage current of the device when its output is in the high impedance state. The procedure for this test is to set the device's output in the high impedance state by clocking the device through several memory cycles, and then stopping the clocks to remove data from the output pin. The appropriate voltage is forced on the output pin and the resultant current measured.

Two forcing voltages are applied. In the IOZH test, 5.5 volts are applied and in the IOZL test, 0 volts is applied. During this test, VDD is set to 5.5 volts which is the worst case condition.

As in the IIH and IIL test (section 5.2.3), the specified limits were +/- 10uA. In general, all measurements yielded extremely low currents of 400nA or less over the full temperature range.

5.2.6 IDD1, IDD2, IDD3 TESTS

These tests measure the amount of supply current required by the device for three different operating modes. The first mode (active) is with the device performing normal Read/Write cycles (IDD1) at maximum speed. To perform the active test, all address inputs and clock signals are toggled at the minimum cycle time which produces proper operation. The average power supply current into the VDD pin is measured. No significant difference was found in the power requirements for read or write cycles.

The second mode is with the device in standby (IDD2). During standby, the device's current drain is reduced to about 10%, by eliminating all dynamic currents that are present during operation. These dynamic currents are produced by the charging and discharging of capacitance nodes within the device during signal transitions. The device is placed in the standby mode by performing an adequate number of memory cycles to bring the device into proper operation, and then setting -RAS, -CAS, and -WRITE to logic "1." When in this mode, the DOUT is in the high impedance state.

The third mode of operation (RAS only refresh) produces a current that includes the standby current, as well as the usual operating dynamic current less the current required by the -CAS clock. As it turns out, this is about the same value as with the device in full active operation, and in some cases, was slightly greater. This could be accounted for by some slight variations in the internal clocks with regard to compensating charging and discharging currents.

Refer to Figures 7 (Active Supply Current), 8 (Standby Supply Current), and 9 (RAS Only Refresh Supply Current) for the worst case measured values.

In general, -55^{o}C caused worst case supply current for the active and refresh states, while +25^{o}C showed an increase in the standby current. The percentage of the change in the standby current was small compared to the overall range. In all cases, the measured values were well within their maximum limits specified in the proposed slash sheet.

5.3 TEST SUMMARY

During the -55^{o}C testing, a problem occurred with moisture condensing on, in and under the device socket and thermal insulating pad. This moisture caused false leakage measurements. Any device which failed due to this moisture

buildup was retested. The false leakage measurements were not considered valid, hence, they were not included in the overall leakage current evaluation.

The measured D.C. parameters were, in general, well within the maximum or minimum limits set by the proposed slash sheet.

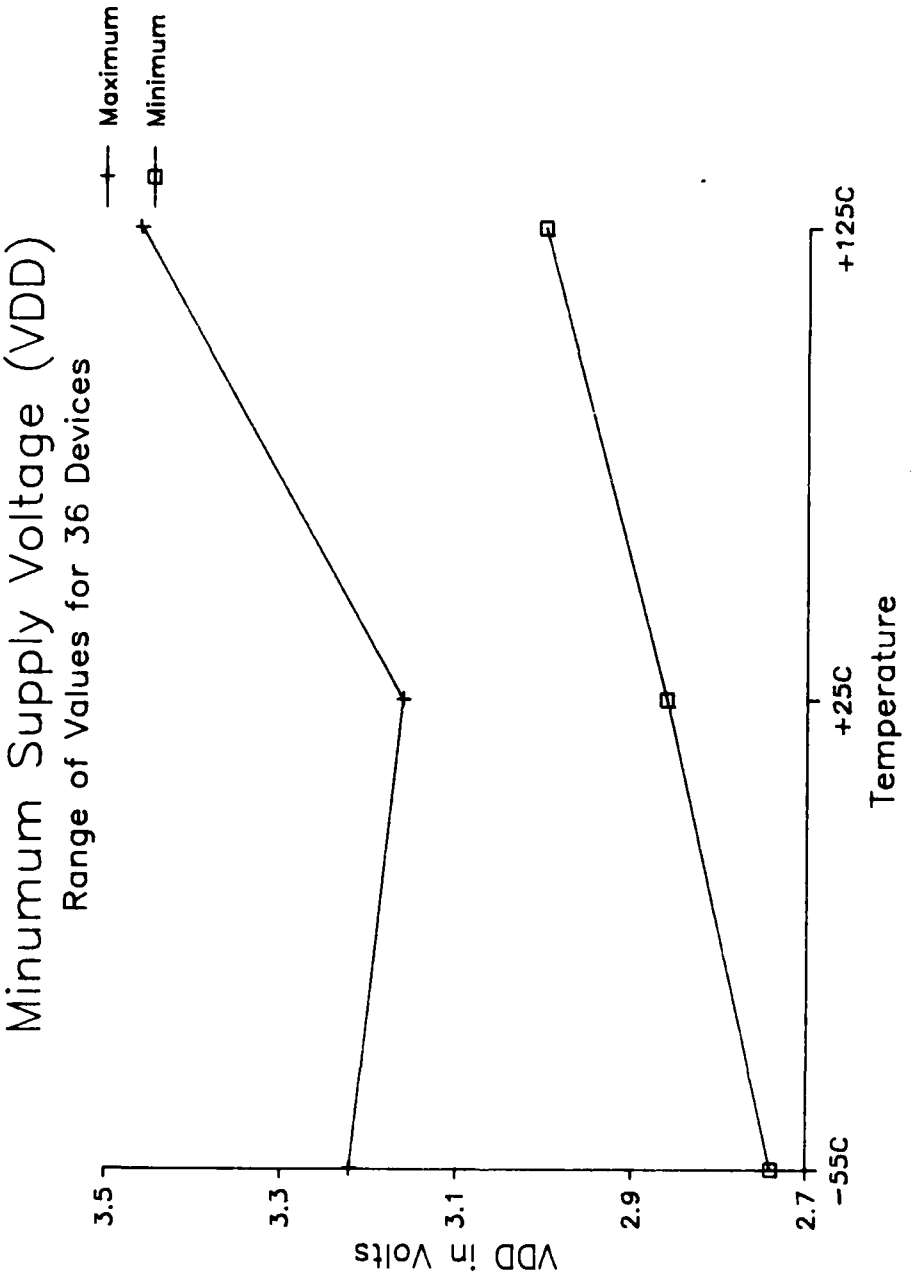


Figure 1: Minimum Supply Voltage

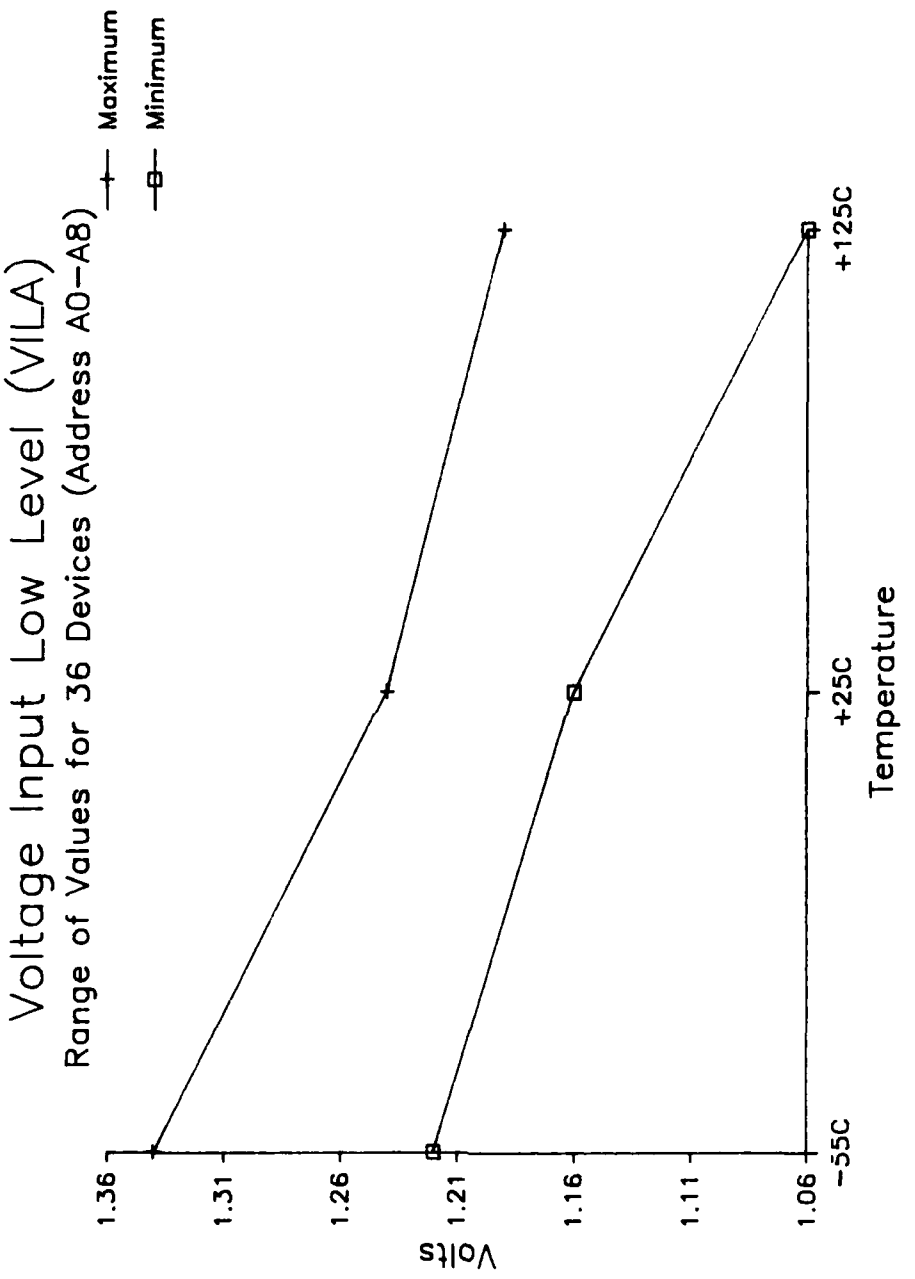


Figure 2: Address Input Voltage Logic "0"

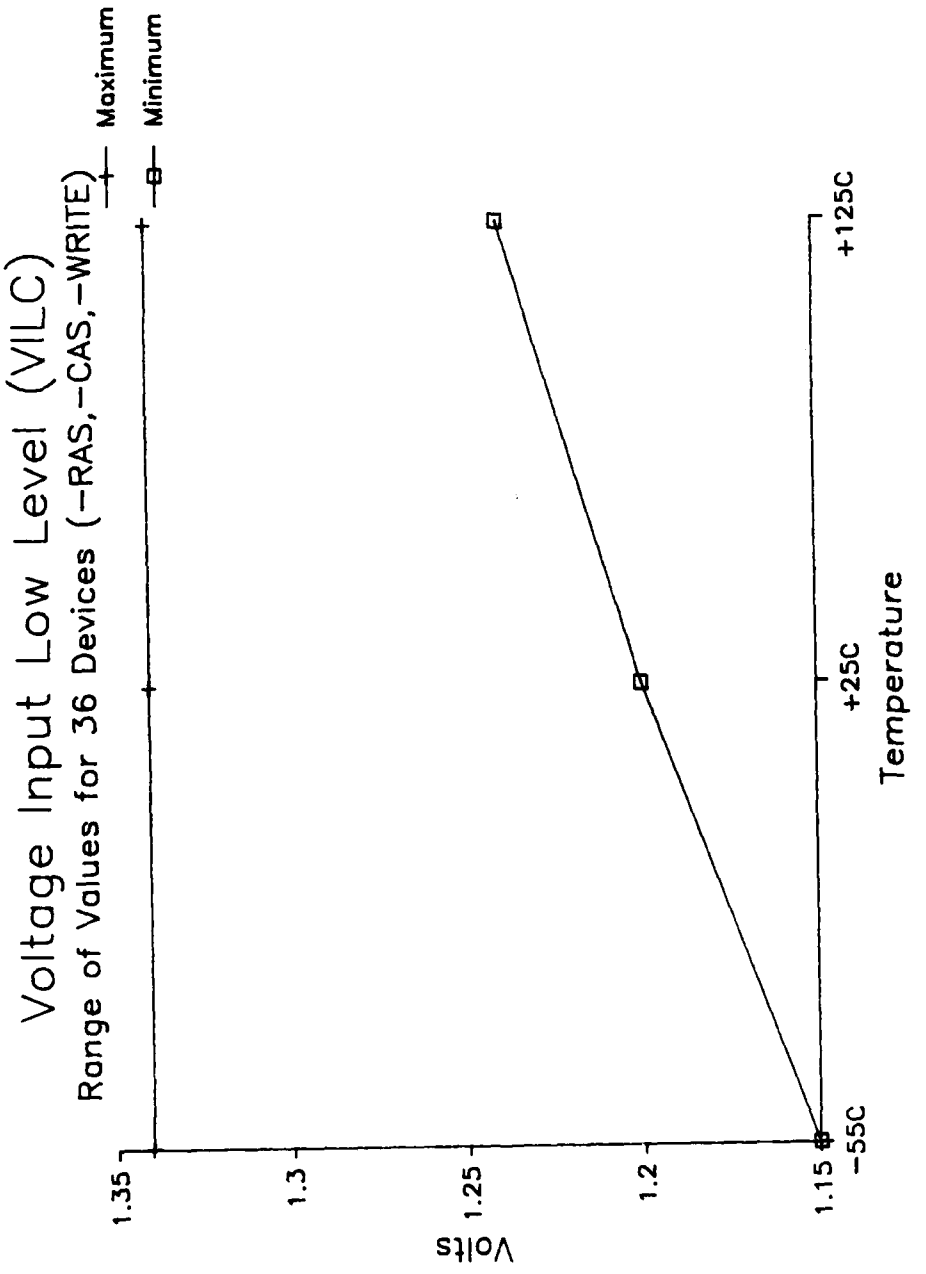


Figure 3: Clock Input Voltage Logic "0"

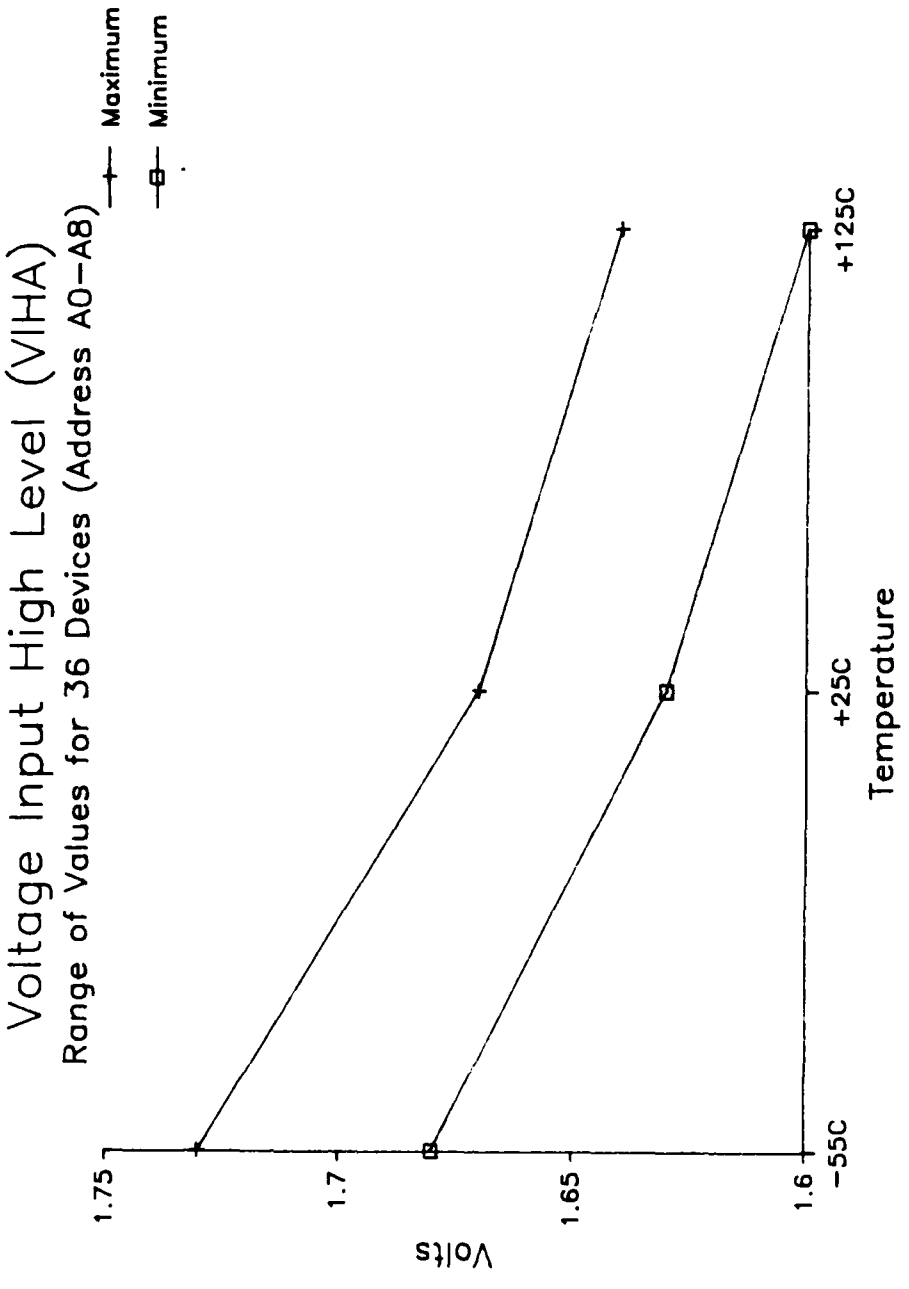


Figure 4: Address Input Voltage Logic "1"

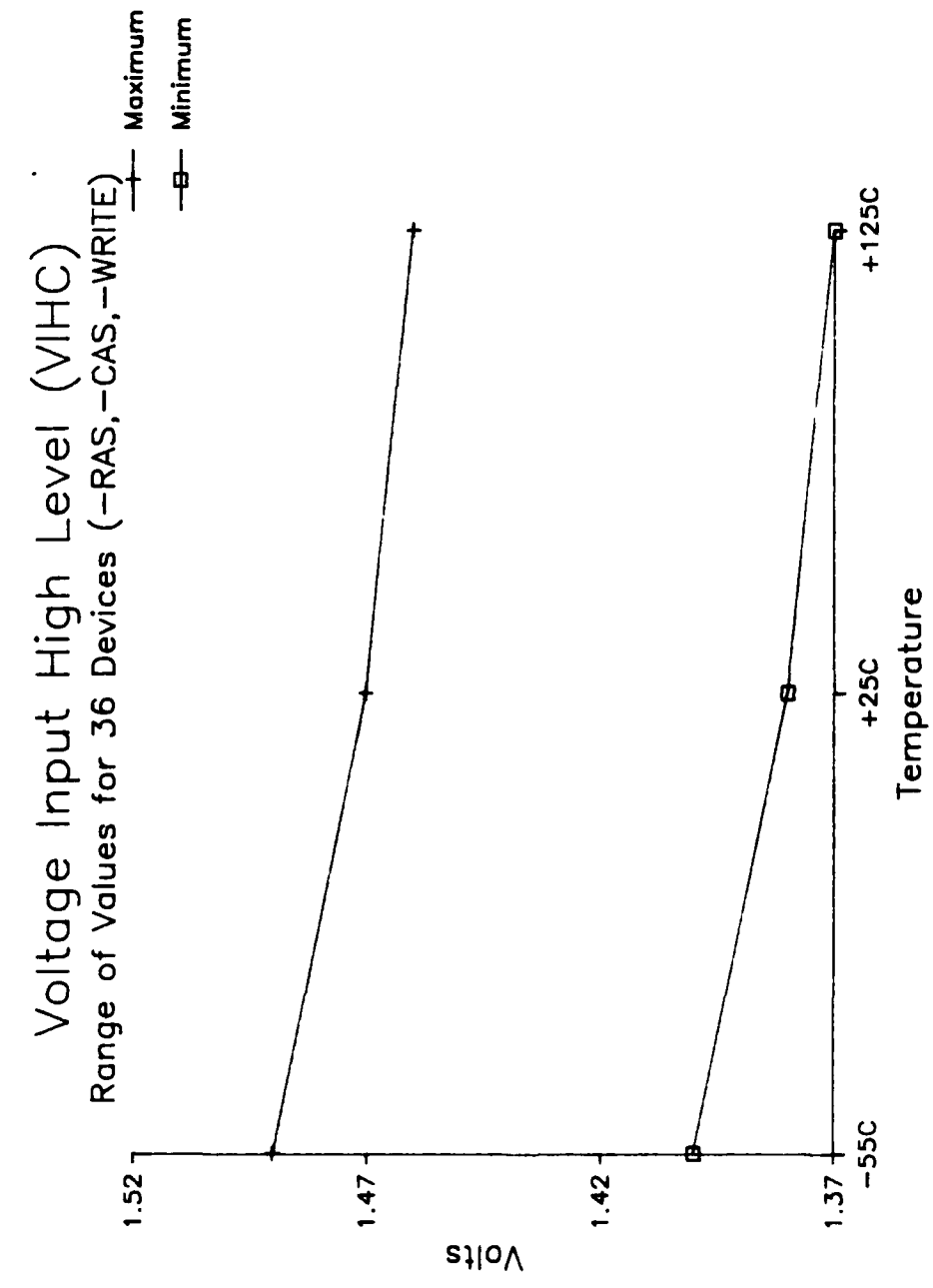


Figure 5: Clock Input Voltage Logic "1"

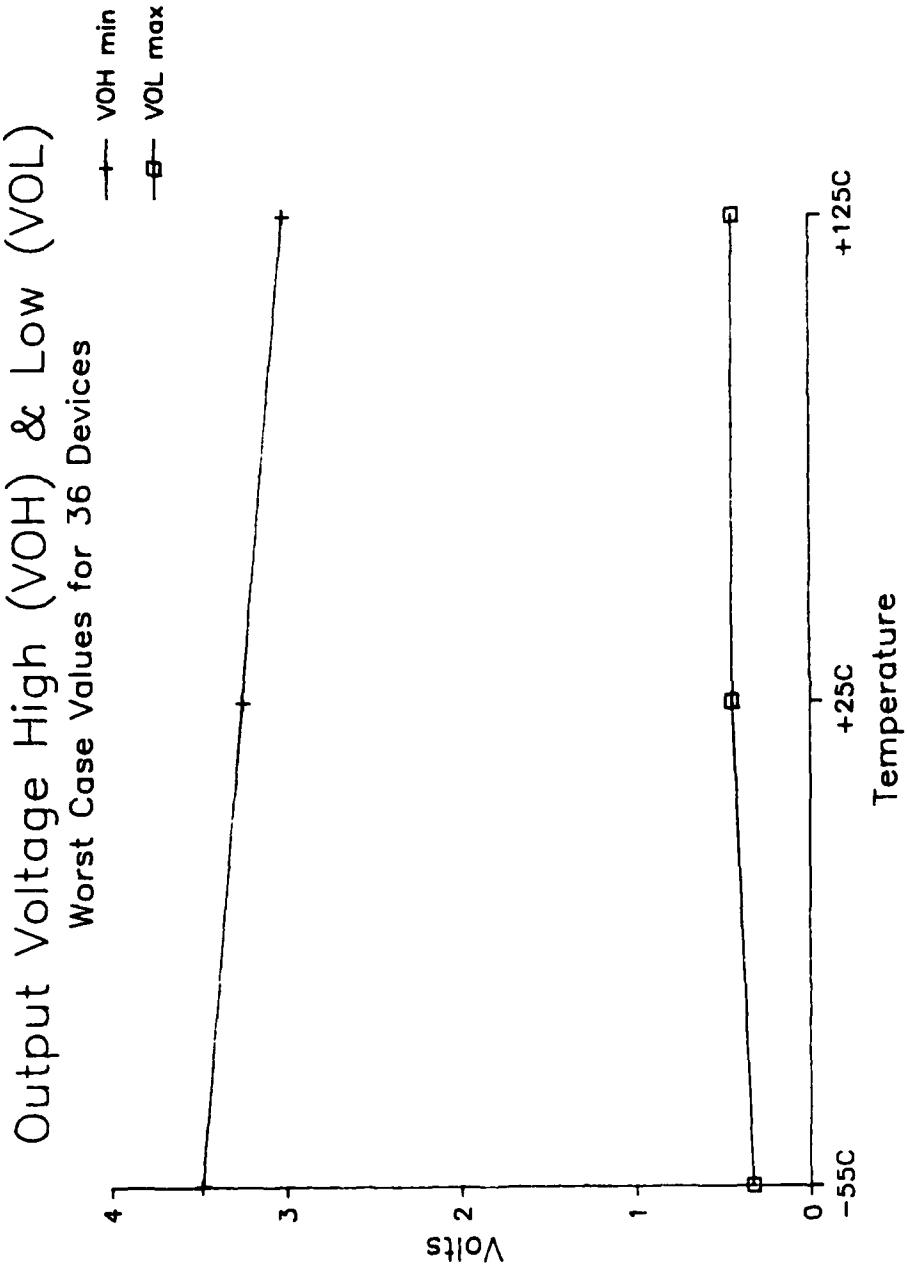


Figure 6: Output Voltage

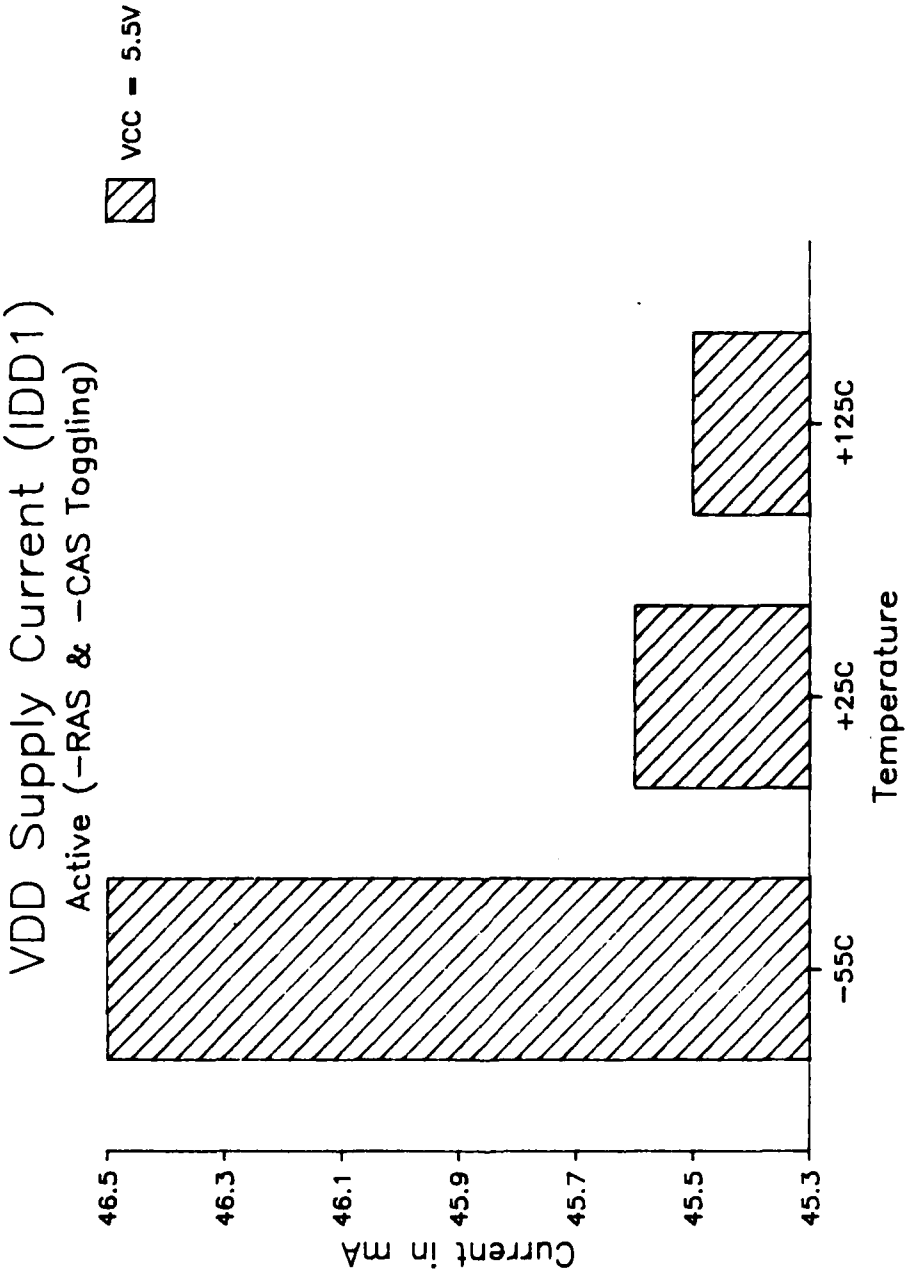


Figure 7: Active Supply Current

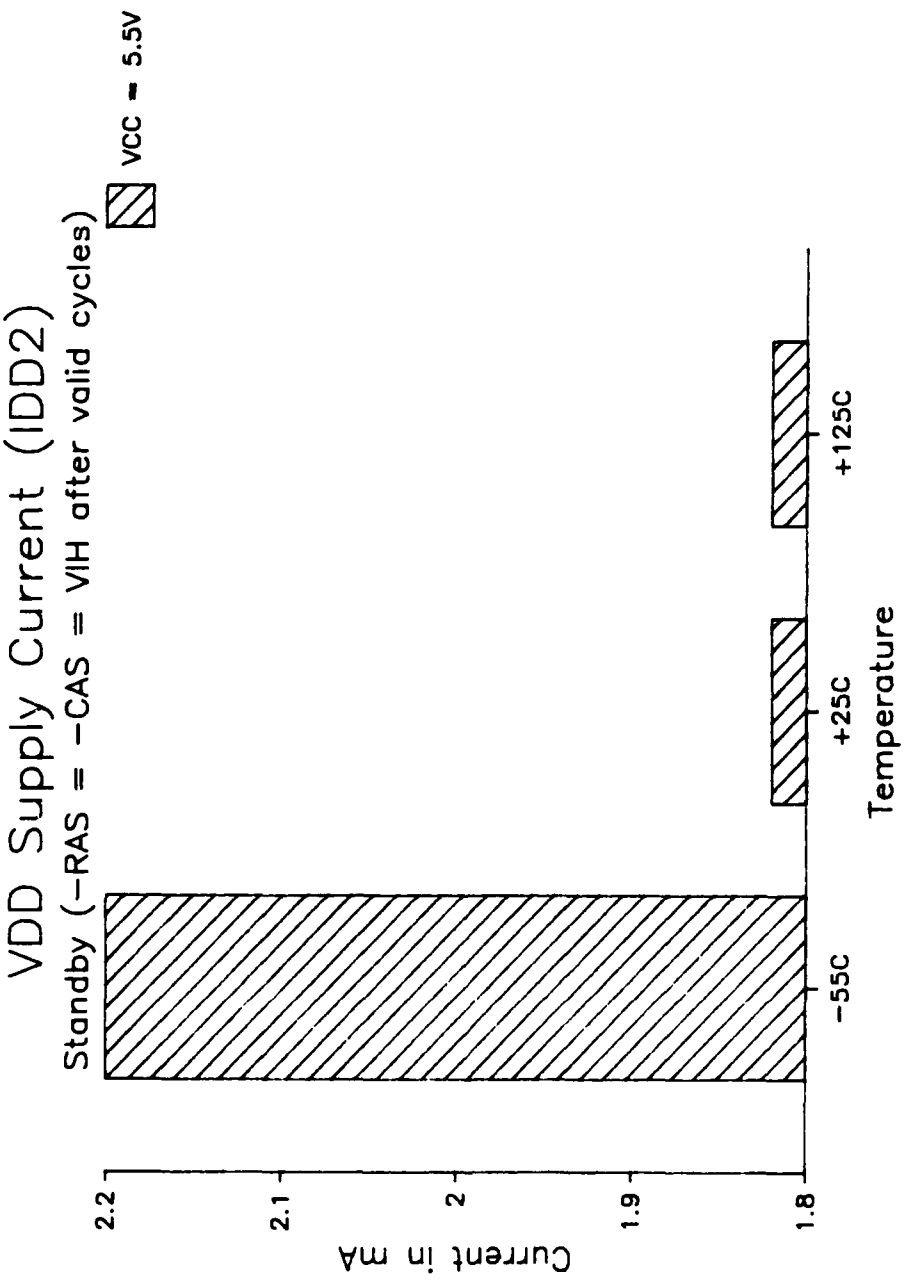


Figure 8: Standby Supply Current

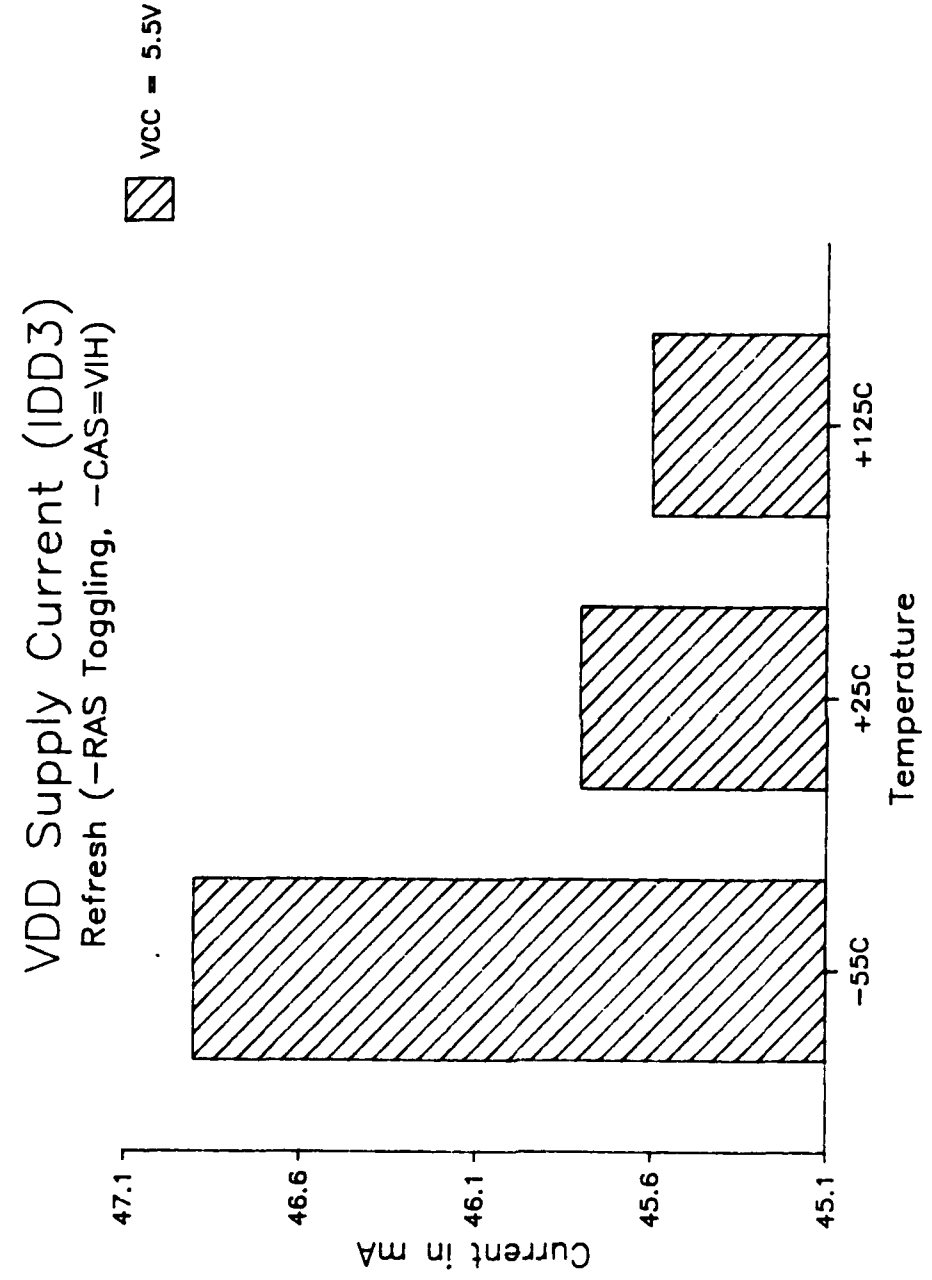


Figure 9: -RAS Only Refresh Supply Current

6. INPUT/OUTPUT CAPACITANCE MEASUREMENTS

6.1 TEST METHODS

Capacitance measurements were performed on six devices, two from each sample date code. Both input and output pin capacitance measurements were made.

The procedure used was to place the capacitance meter's probe on the input or output pin and measure its capacitance with respect to the device's ground pin (16). During testing, all pins not under test are left open.

The meter parameters were set as follows:

Frequency = 1MHz
AC RMS amplitude = 50 millivolts
DC bias = 0 volts.
Parallel equivalent circuit

Refer to MIL-STD-883C method 3012.1.

6.2 TEST SUMMARY

The data showed that the devices did not have a uniform capacitance across the range of pins. Figures 10 and 11 show that input pins 1 (A0) and 13 (A6) have consistently higher capacitance values than the other inputs. The maximum value of 5pF used in the proposed slash sheet was met in all cases.

As compared to the inputs, the measured output capacitance was higher. Referring to Figure 12, the test showed that there was a fair consistency in the values of the output capacitance from device to device. In all cases the value measured was within the maximum specification of 6pF, however, the margin was not as great as for most of the input capacitances, pins 1 & 13 being the exceptions.

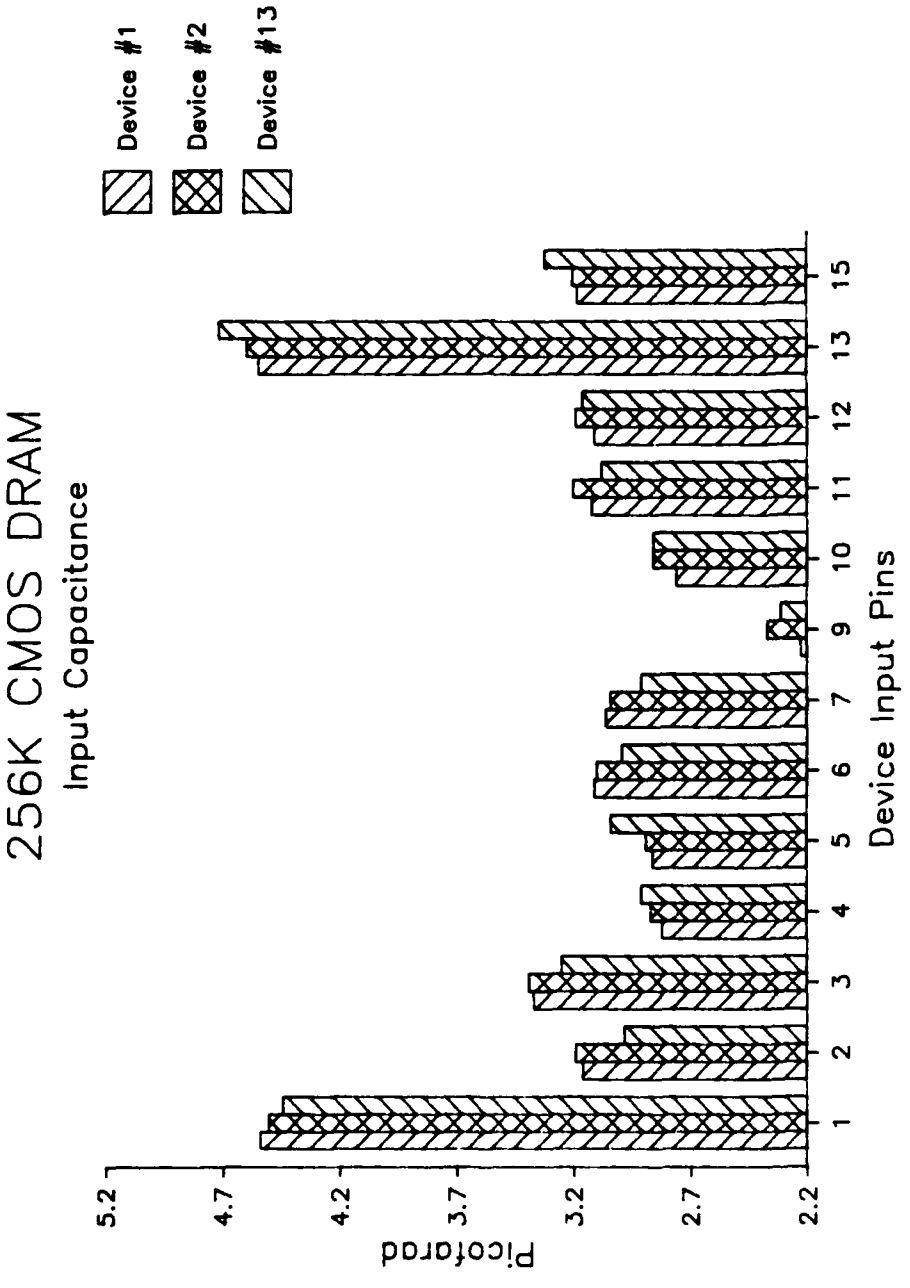


Figure 10: Input Capacitance for Devices 1, 2 & 13

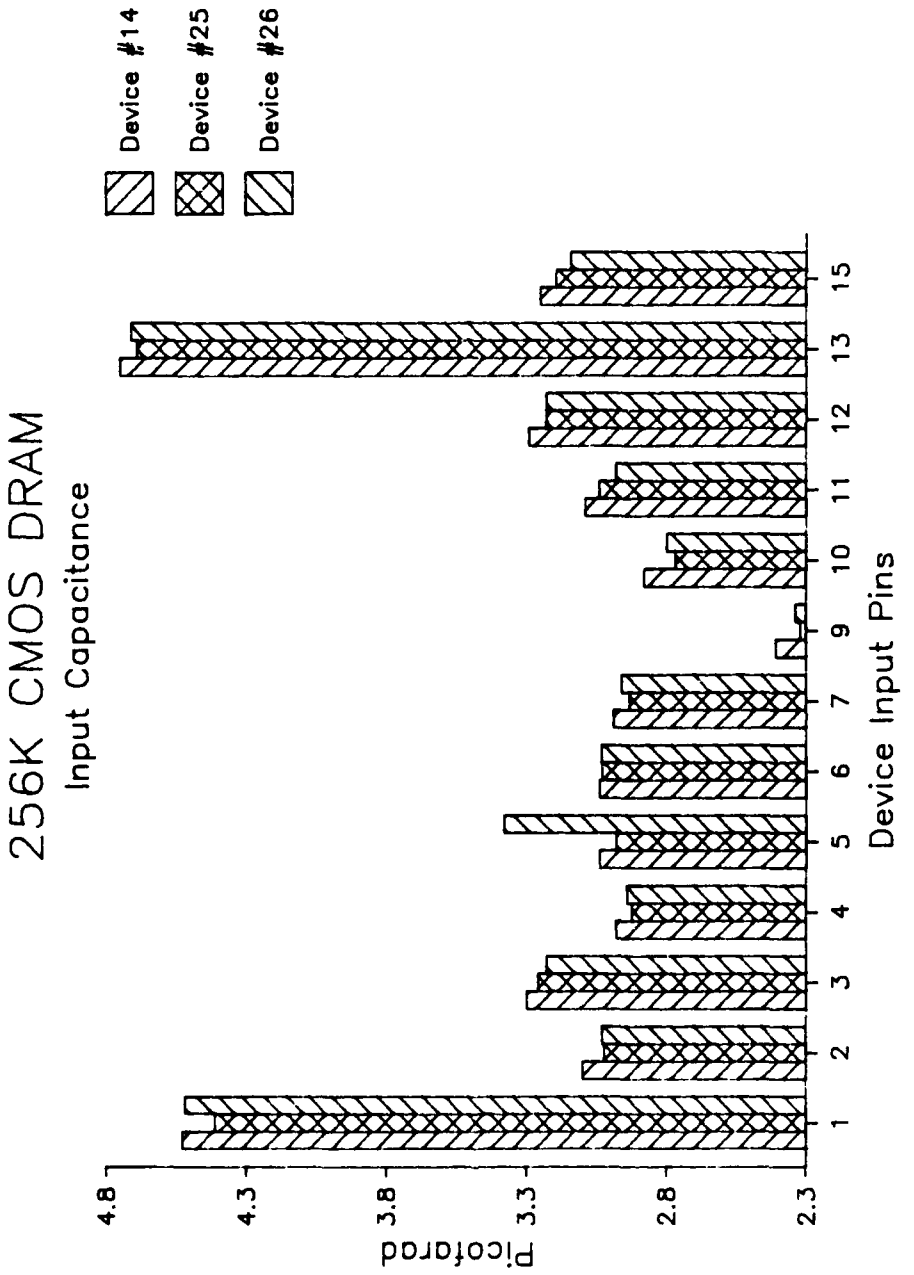


Figure 11: Input Capacitance for Devices 14, 25 & 26

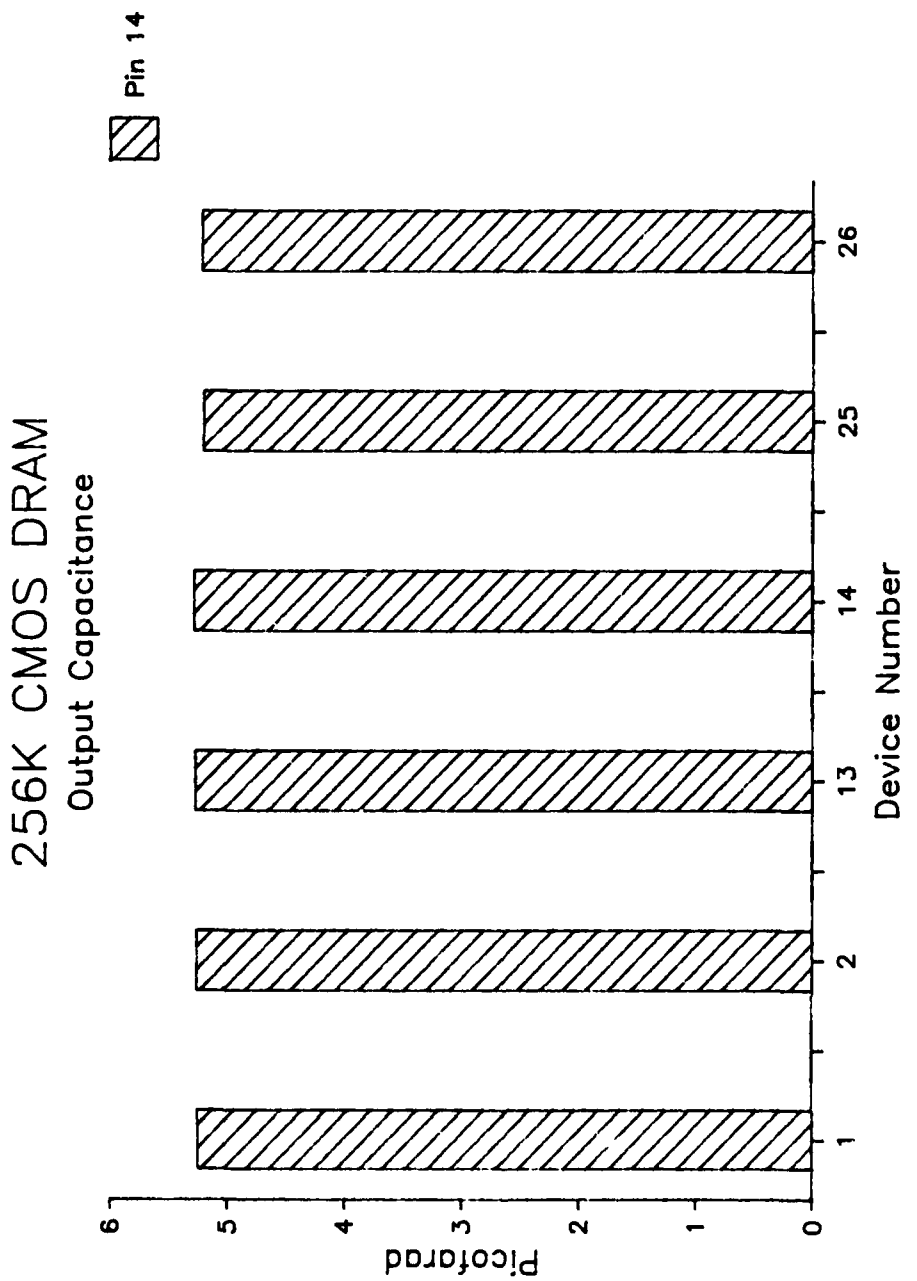


Figure 12: Output Capacitance for Six Devices

7. ELECTROSTATIC DISCHARGE, VZAP TESTS

One of the greatest hazards of microelectronic devices, especially those using VLSI MOS technology, is the destructive capability of Electrostatic Discharges (ESD.) The damage caused by ESD may be the instantaneous complete destruction of the device or just a reduction in its performance with failure to occur later. To improve the device's capacity to withstand ESD, the manufacturers have added complex input structures to shunt much of the destructive energy contained in the pulse. There is even a limit to what these can do.

7.1 TEST METHODS

This test is performed to measure the electrostatic discharge sensitivity of the device's input pins. Testing was performed in accordance with MIL-STD-883C method 3015.2 using IMCS model 2400C ESD simulator. After each exposure to an ESD pulse, the devices were analyzed on the Xincom 5588 test system for continuity and leakage parameters.

At the beginning of this test, the actual breakdown voltage of the device was unknown. The approach taken was to step the voltage in 200 volt increments, until the leakage current exceeded the maximum current of +/- 10uA or input continuity was destroyed. After this voltage level was found, it could be used as a starting point for further testing.

Each device pin under test was pulsed until a failure (lack of continuity or leakage current > 10uA) was measured. As the testing progressed, the ESD voltage pulse was incrementally increased until a failure was obtained.

7.2 TEST SUMMARY

As described in the test methods, some preliminary testing using device #36 produced a first breakdown at 800 volts and thus a starting point of 400 volts was selected to provide a buffer and be sure to find the lowest value on the devices selected for characterization. From that voltage level, a worst case ESD voltage pulse to cause damage was determined.

Figure 13 shows the variation of the breakdown voltage across the different input pins on device number 12, when subjected to negative input pulses. The first pulse applied was at 400 volts, with each succeeding pulse 200 volts greater in magnitude, until 2800 volts was reached. At this point the interval was

reduced to 100 volts. It is apparent that there is a large variation in the level of protection across the inputs of a given device. The failure mode of pins 5 and 15 was excessive leakage current, whereas all other inputs failed continuity.

Figure 14 shows the variation in the breakdown voltage when device number 24 was subjected to positive input pulses using this same technique. There is not the wide variation in device protection capability as with the negative excursion and the average value is much lower in magnitude. The minimum breakdown value is, however, significantly greater than for the negative pulse.

After evaluating the values of protection measured for these devices, it was determined that a limit of 400 volts for the minimum ESD protection would be in line with the process capability. This would place the device in the ESD category "A."

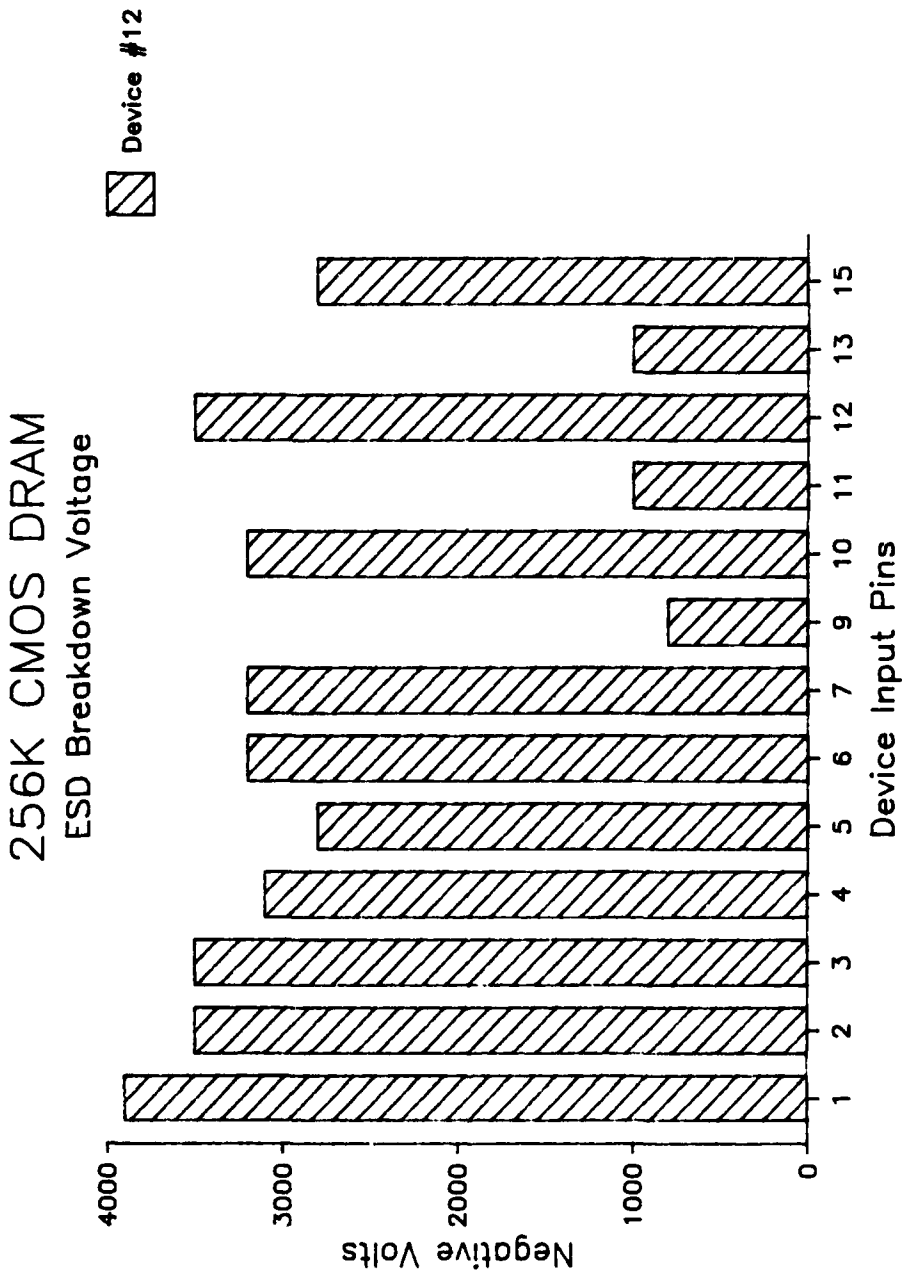


Figure 13: Electrostatic Discharge Test Device #12

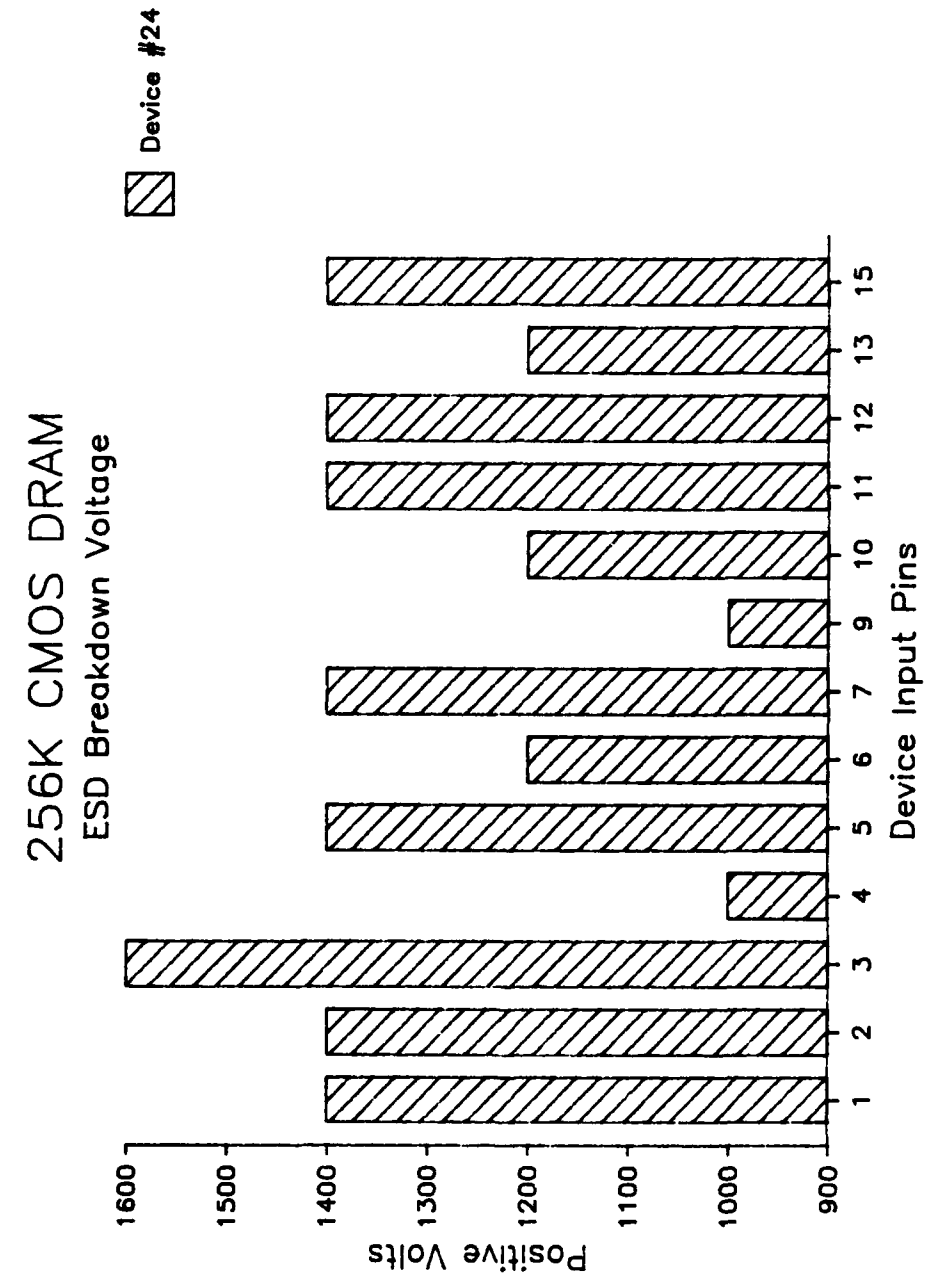


Figure 14: Electrostatic Discharge Test Device #24

8. DYNAMIC CHARACTERISTICS

8.1 TEST METHODS

The Xincom 5588 memory test system was also used to collect data on the A.C. timing parameters. During the characterization of a particular timing parameter, all other parameters were set to their nominal or a less stringent value. Following this technique guarantees that as the selected parameter is adjusted toward its operating limit, a failure is due to that parameter.

In addition to timing parameters, the capability to write and read every cell in the device was also checked. All 36 sample devices were characterized over the $-55^{o}C$ to $+125^{o}C$ temperature range and VDD was varied from 4.5 to 5.5 volts. During timing parameter measurements a load circuit, equivalent to 50pF capacitance and 2 standard TTL device inputs, was connected to the output pin.

8.2 PATTERN SENSITIVITY TESTS

A wide variety of address sequence and data patterns were used in the evaluation of the devices to determine if there was any specific sensitivity within the device, or if there was any interaction or crosstalk between sections of the on-chip circuitry. These tests included such data patterns as Checkerboard, X- and Y-Parity, and Diagonal, with address sequences including Up and Down Count, Address Complement, Surround Disturb, and March. These patterns and sequences were combined in various ways along with timing and voltage variations to evaluate each device's capabilities. No pattern sensitivities were detected. The Appendix to this part of the report includes descriptions of some of the test patterns used.

8.3 A.C. PARAMETRIC MEASUREMENTS

The A.C. characterization not only determines the operating limits of the timing parameters, but also verifies the integrity of the internal functions under dynamic conditions. The internal functions of the dynamic memory can be divided into the following blocks.

- o Address Decoders
- o Clock Phase Generators
- o Sense Amps
- o Memory Array
- o Data I/O Circuitry

The tests were run over the full -55°C to +125°C temperature range. In addition, the VDD of the device was ranged between 4.5 and 5.5 Volts for each temperature. In general, the standard March pattern was used for making the timing measurements. Those exceptions are when address transitions become part of the timing function, e.g., Column Address Access time, at which time the Address Complement sequence was used.

8.3.1 RAS Access Time

The RAS access time (tRAC) measurement technique requires that the device timings of all the controlling signals be set as tight as possible at the start of a cycle utilizing the values for the shortest cycle time. This will place the valid data output under the control of the -RAS clock. The data output strobe of the tester is then gradually increased from a known failing value until the device passes. Figure 15 shows the range of values over the temperature range.

8.3.2 CAS Access Time

To establish the access time referenced to the falling edge of -CAS (tCAC), the timings of the cycle are extended to the point beyond the values where access is controlled by -RAS. With sufficient column address setup time established to prevent the interference of the address transitions from affecting the output data, the access time from the falling edge of -CAS to valid data is measured. Figure 16 shows the range of values of the tCAC parameter.

8.3.3 Address Access Time

The Column Address Access time (tCAA) measurement technique used was to establish a timing set, such that valid data output was well beyond the point where it is controlled by the tRAS parameter, and is strictly a function of the -CAS clock. With the column address setup time set at its minimum, the access time from the point of column address stability to valid data is determined. Figure 17 shows the range of values of the tCAA parameter.

8.3.4 Row Address Setup Time

This test measures the amount of time required for the row addresses to be valid before the fall of -RAS, to ensure that the proper row of memory cells is accessed. With the other timings set at nominal, the row address was stabilized after the falling edge of -RAS, and then gradually stepped earlier until the device passed. Figure 18 shows the range of values for the tASR parameter.

8.3.5 Row Address Hold Time

This test measures the amount of time required for the row addresses to remain valid after the fall of -RAS, to ensure that the proper row of memory cells is accessed. With all other timings at nominal and an adequate setup time, the termination of valid row address was set at a position prior to the falling edge of -RAS and then stepped later until the device passed. Figure 19 shows the range of values of the tRAH parameter.

8.3.6 Column Address Setup Time

This test measures the amount of time required for the column addresses to be valid before the fall of -CAS, to ensure that the proper column of memory cells is accessed. With the other timings set at nominal, the column address was stabilized after the falling edge of -CAS and then gradually stepped earlier until the device passed. Figure 20 shows the range of values for the tASC parameter.

8.3.7 Column Address Hold Time

This test measures the amount of time required for the column addresses to remain valid after the fall of -CAS, to ensure that the proper row of memory cells is accessed. With all other timings at nominal and an adequate setup time, the termination of valid column address was set at a position prior to the falling edge of -CAS and then stepped later until the device passed. Figure 21 shows the range of values of the tCAH parameter.

8.3.8 Column Address to -RAS Setup Time

This test measures the amount of time required for the column addresses to be valid before the rise of -RAS, to ensure that the proper column of memory cells is accessed. With the other timings set at nominal, the column address was stabilized just prior to the falling edge of -CAS (still meeting the minimum tASC requirement). The -RAS width is set near the minimum required to meet the tRSH requirement, and then it was increased until valid memory cycles were obtained. Figure 22 shows the range of values for the tCAR parameter.

8.3.9 RAS to CAS Delay Time

Both a maximum and minimum value are placed on this parameter. The evaluation of the minimum value requires that the addresses change from the row to column at the earliest time possible after the fall of -RAS. Then the falling edge of -CAS is continuously made earlier until device failure occurs. This then defines the earliest time at which -CAS can occur following -RAS, while allowing enough time for all internal device clock phases to be properly generated.

Although a maximum value of tRCD is specified, it is not a limitation of the device operation, but a defined point at which the control of valid data out must have been transferred from the -RAS clock to the -CAS clock. For most circuit applications of this type of device this upper limit is not a point of concern, but rather it is the minimum that is important for the fastest possible operation. Figure 23 shows the range of values of the tRCDmin parameter.

8.3.10 -RAS Pulse Width

The maximum length of time that -RAS can remain in the active low state is largely determined by the ability of the internal nodes to hold their charge. Once this charge has depleted below the upper threshold limit, the proper operation of the device is no longer guaranteed, and a variety of faulty conditions may result, e.g., the next operational cycle may not be properly initiated. Figure 24 shows the range of values of the tRAS parameter.

8.3.11 -CAS Pulse Width

The maximum length of time that -CAS can remain in the active low state is largely determined by the ability of the internal nodes in the -CAS clock chain to hold their charge. Once this charge has depleted below the upper threshold limit, the proper operation of the device is no longer guaranteed, and a variety of faulty conditions may result, e.g., the data at the output pin may no longer be valid. Figure 25 shows the range of values of the tCAS parameter.

8.3.12 -RAS Precharge Time

This test determines the minimum time required for -RAS to be in the off state for all internal nodes to become adequately charged, so as to be ready for the next operational cycle, whether it is Read, Write, or Refresh. This time, in conjunction with the minimum -RAS Pulse Width, determines the minimum cycle time or the maximum operating speed of the device. Figure 26 shows the range of values of the tRP parameter.

8.3.13 -RAS Hold Time

The -RAS hold time parameter, which is the time delay from the falling edge of -CAS to the rising edge of -RAS, i.e., both clocks are low, is a function of the type of cycle taking place. The time required for both signals to be low is longer during a write cycle than during a read cycle. Figures 27 and 28 show the range of values of the tRSHR (Read Cycle) and tRSHW (Write Cycle) parameters respectively.

8.3.14 DATA-IN Setup Time

This test determines the minimum time that valid data must be applied to the DIN terminal before the latter falling edge of -CAS or -WRITE occurs. This is accomplished by having the timings set at a loose nominal value with the falling and rising edges of -WRITE a considerable distance from the falling edge of -CAS. The leading edge of valid data is then progressively moved earlier from its starting value after the falling edge of -CAS. The point at which a valid write cycle takes place gives the Data In setup time referenced to -CAS.

This same relationship is applicable to the setup time for valid data referenced to the falling edge of -WRITE. In this case a delayed write cycle set of timing considerations is used, and the valid data edge is moved in reference to -WRITE. Figure 29 shows the range of values of the tDS parameter.

8.3.15 DATA-IN Hold Time

This test determines the length of time that data must remain valid after the falling edge of -CAS. With the timings set at nominal, and adequate data setup time given, the trailing edge of the valid data is iterated from a point just prior to the falling edge of -CAS to that point later in time when valid write cycles occur. Figure 30 shows the range of values of the tDH parameter.

8.3.16 Output Disable Time

This test measures the amount of time required for the device output to become high impedance following the rising edge of -CAS. The voltage at the output pin, at turn off, largely becomes a function of the time constant of the load capacitance and resistance. The output stage actually turns off long before the voltage on the output pin reaches its stable high impedance state.

The technique used to measure this value establishes the sense levels for the output comparators to be 100mV above VOL and 100mV below VOH. The tOFF time is established as the time from when -CAS rises to the point at which the DOUT level has moved 100mV from its VOL or VOH value.

This measurement technique provides a means of accurately determining the point at which the output actually turns off. This provides for self calibrating the individual device's output to its particular values of VOL and VOH. Figure 31 shows the range of values for the tOFF parameter.

8.3.17 -WRITE Command Hold Time

This test measures the amount of time required for -WRITE to remain at logic "0" after the fall of -CAS for the proper write cycle operation to take place. With all other timings at nominal and an adequate setup time, the rising edge of -WRITE is moved from its starting point just following the fall of -CAS (a failing condition) to a later time where proper operation occurs. Figure 32 shows the range of values of the tWCH parameter.

8.3.18 -WRITE Pulse Width

This test determines the minimum width of the active low -WRITE signal to produce a valid write operation. With the timings set at nominal values and the fall of -WRITE occurring after the fall of -CAS, the rising edge of -WRITE is increased from its starting value of 5ns after the fall to the point where a valid write cycle takes place. Figure 33 shows the range of values of the tWP parameter.

8.3.19 -WRITE to -RAS Lead Time

This test measures the minimum time required for the falling edge of -WRITE to precede the rising edge of -RAS. To obtain this reading the general timings are set to nominal values with the relationship of -WRITE and DIN to -CAS, such as to create a delayed write type of cycle. While keeping adequate width of the -WRITE pulse, the falling edge is stepped earlier in time from a starting point just prior to the rising edge of -RAS until a valid cycle is produced. Figure 34 shows the range of values of the tRWL parameter.

8.3.20 -WRITE to -CAS Lead Time

This test measures the minimum time required for the falling edge of -WRITE to precede the rising edge of -CAS. To obtain this reading the general timings are set to nominal values with the relationship of -WRITE and DIN to -CAS, such as to create a delayed write type of cycle. While keeping adequate width of the -WRITE pulse, the falling edge is stepped earlier in time from a starting point just prior to the rising edge of -CAS until a valid cycle is produced. Figure 35 shows the range of values of the tCWL parameter.

8.3.21 Time Between Refresh

The maximum time allowed between refresh cycles is very critical at the higher operating temperatures. At room, or normal operating conditions, this time stretches out to a point of being completely impractical to measure. This being the case, the evaluation of this parameter was only done to verify that the minimum requirement of four milliseconds was met at the maximum temperature of 125°C. During the wait time all of the input signals are active, with the exception of -RAS, to create the worst case of on-chip noise possible. All of the devices were tested and met this characteristic.

8.4 TEST SUMMARY

During the AC measurements, the only parameter that did not meet the vendors commercial limits over the full military temperature range was the -CAS Access Time (-tCAC) and the -CAS Pulse Width (tCAS). Seven of the devices failed to meet the maximum tCAC limit of 30 nanoseconds at 125°C, with three of these still failing at 110°C. Four of these same devices failed the -CAS Pulse Width (tCAS) minimum limit at 125°C with two continuing to fail at 110°C. These are screenable parameters and can be dealt with at the manufacturing site producing only a small yield loss. The limits as stipulated for this device in the detail specification for MIL-M-38510 are considered valid.

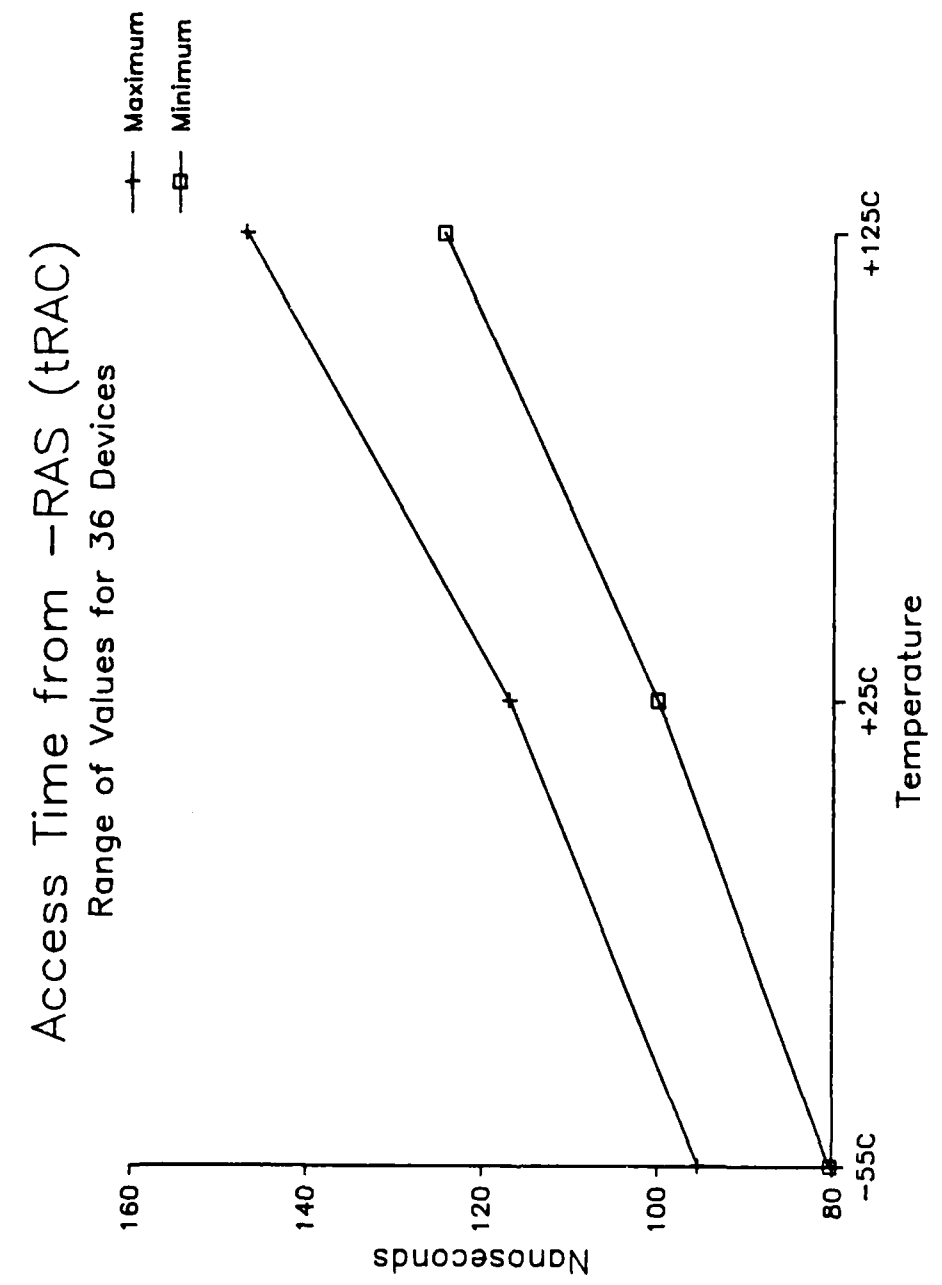


Figure 15: -RAS Access Time

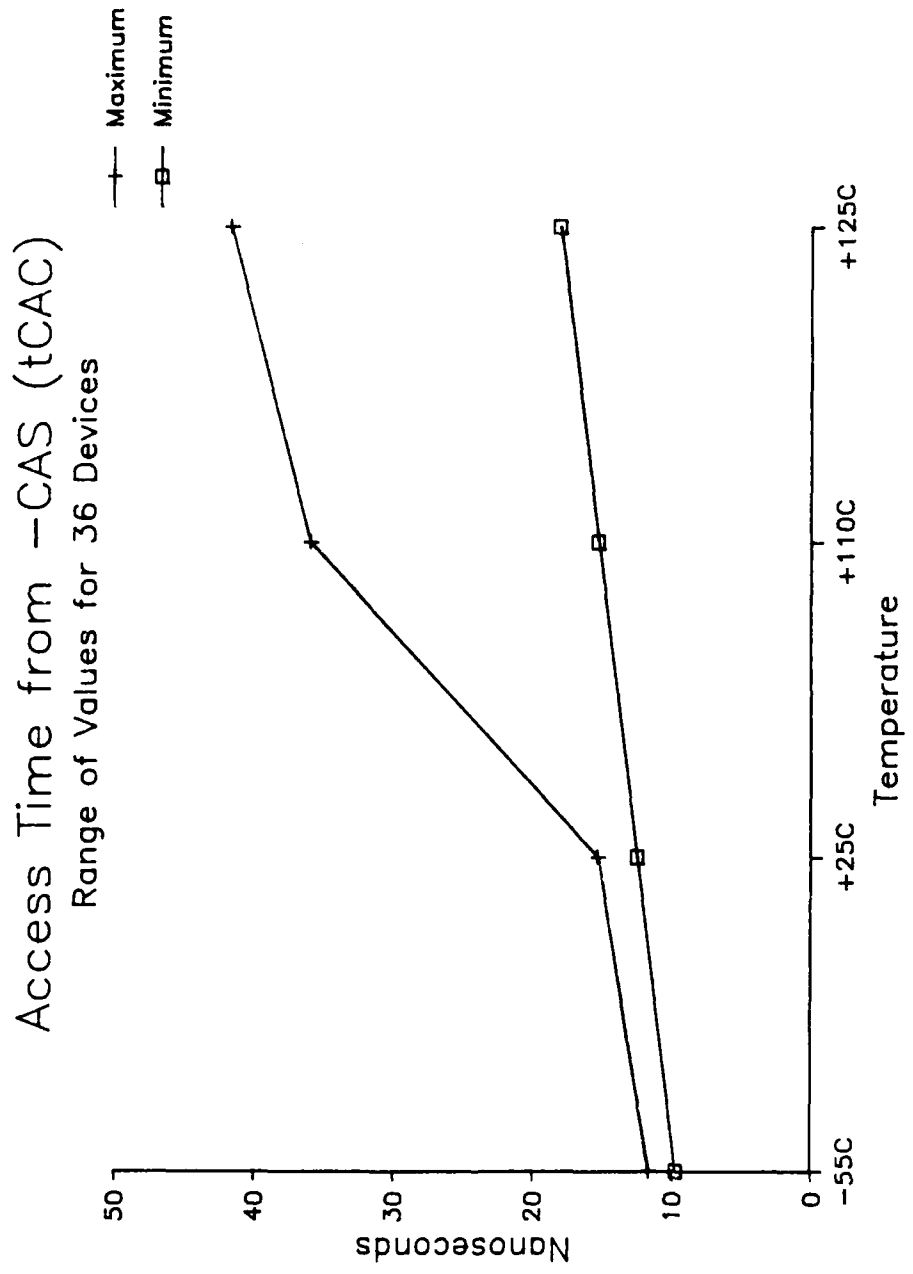


Figure 16: -CAS Access Time

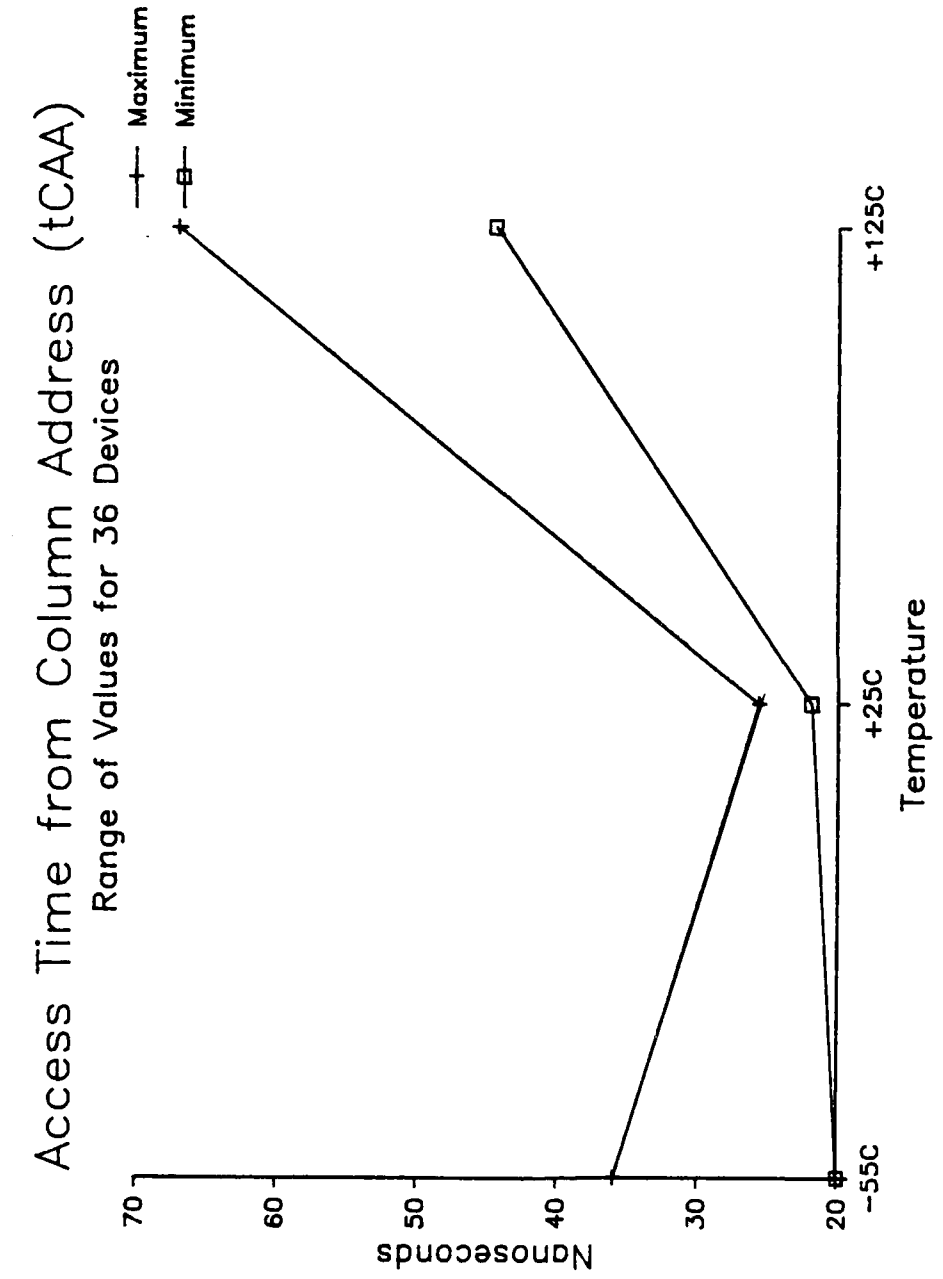


Figure 17: Column Address Access Time

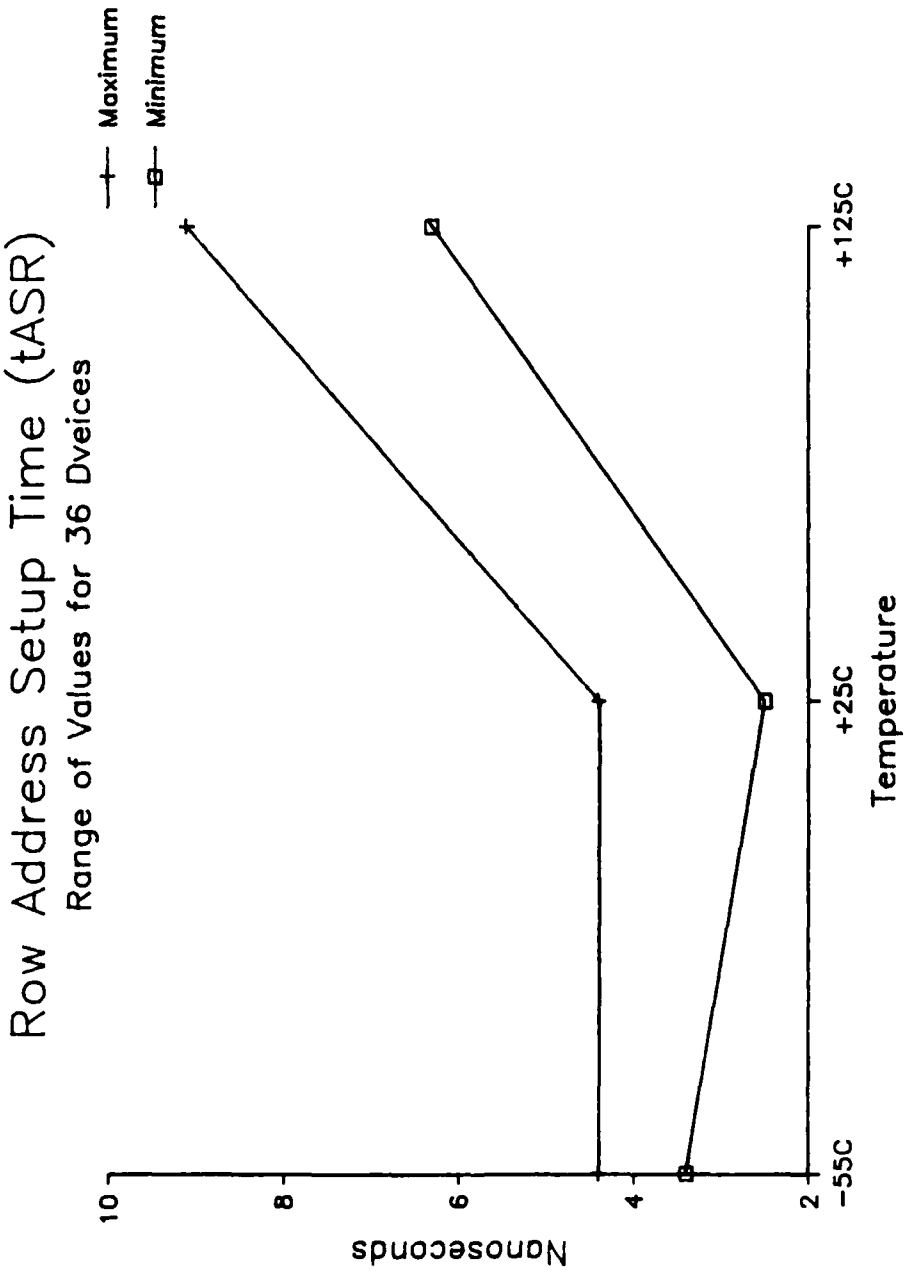


Figure 18: Row Address Setup Time

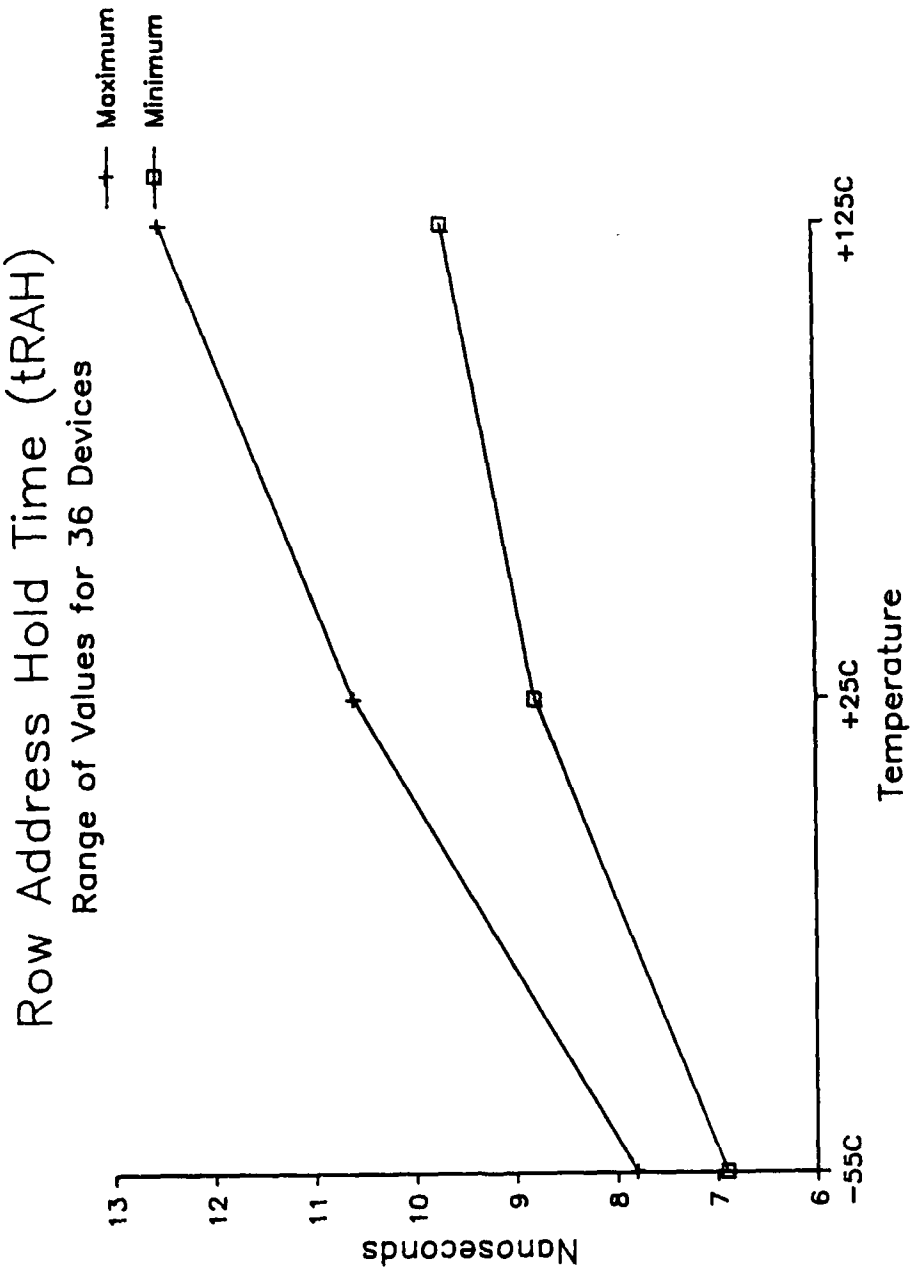


Figure 19: Row Address Hold Time

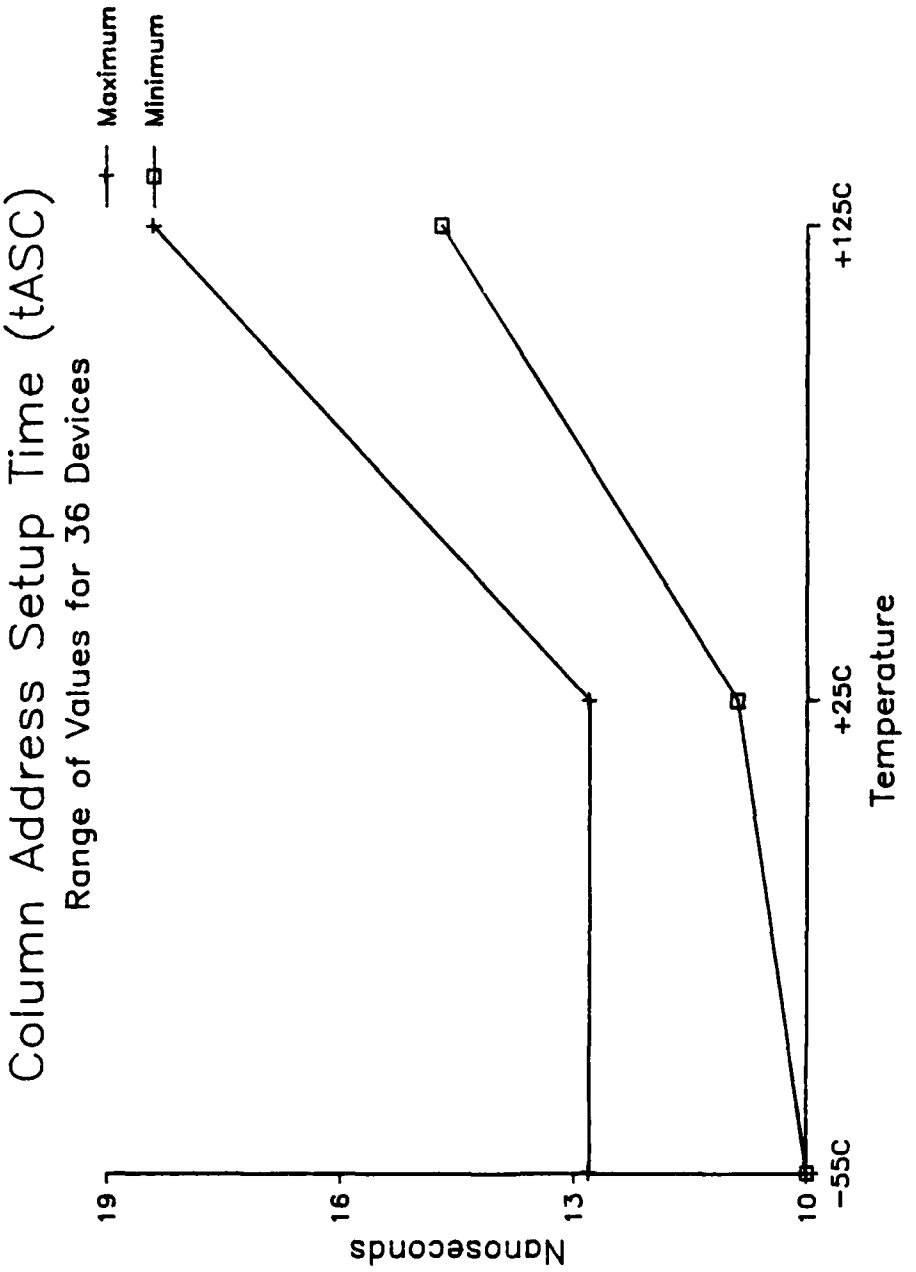


Figure 20: Column Address Setup Time

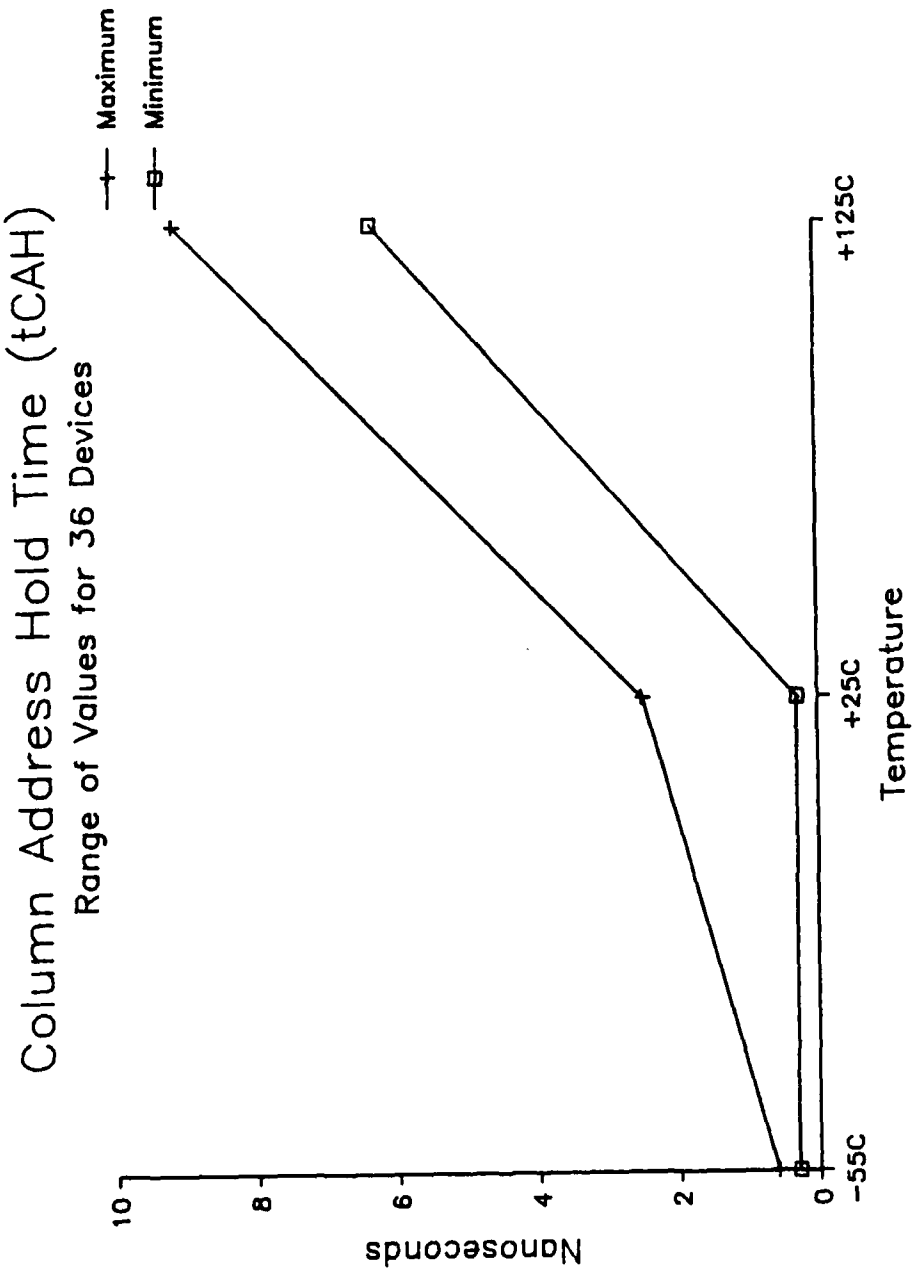


Figure 21: Column Address Hold Time

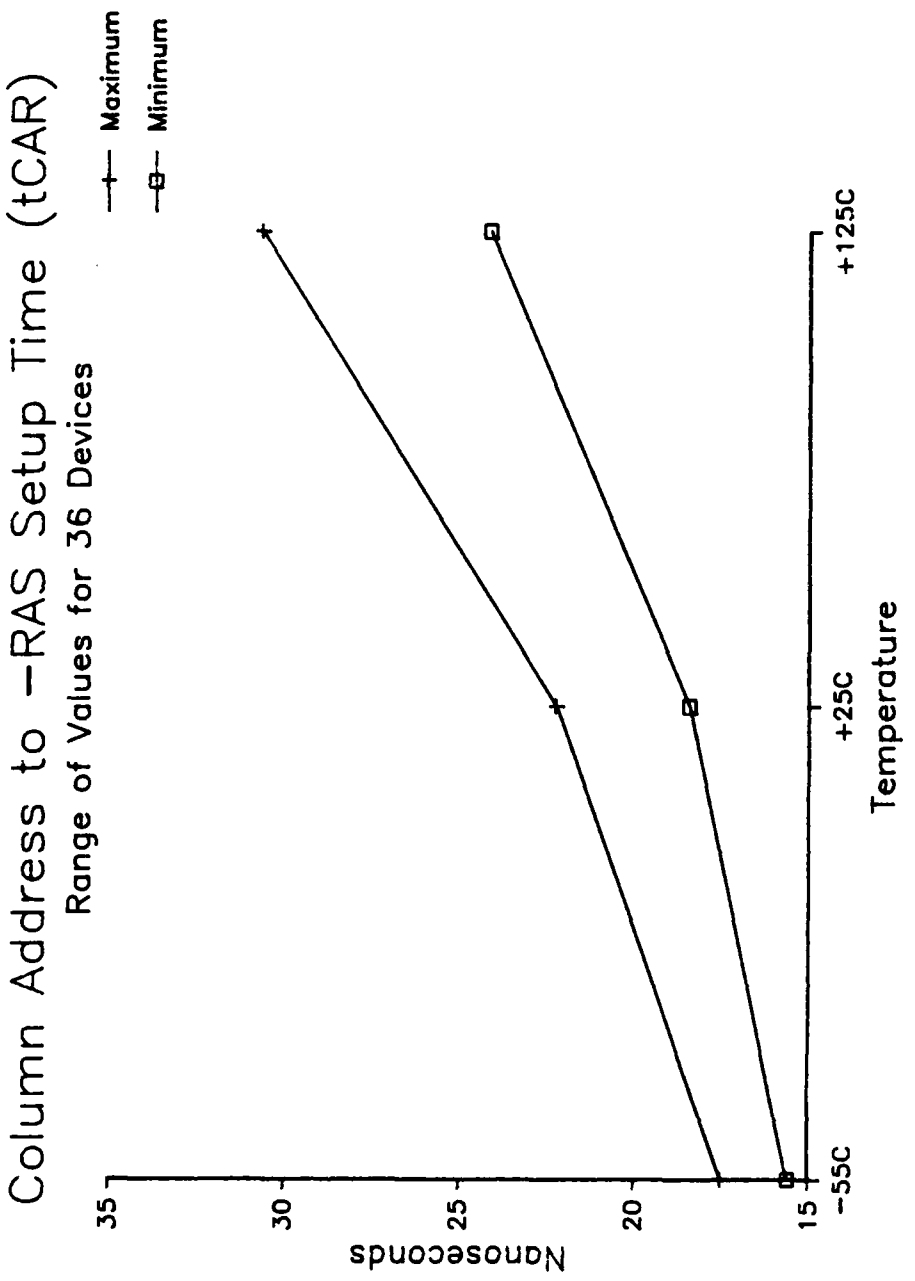


Figure 22: Column Address to -RAS Setup Time

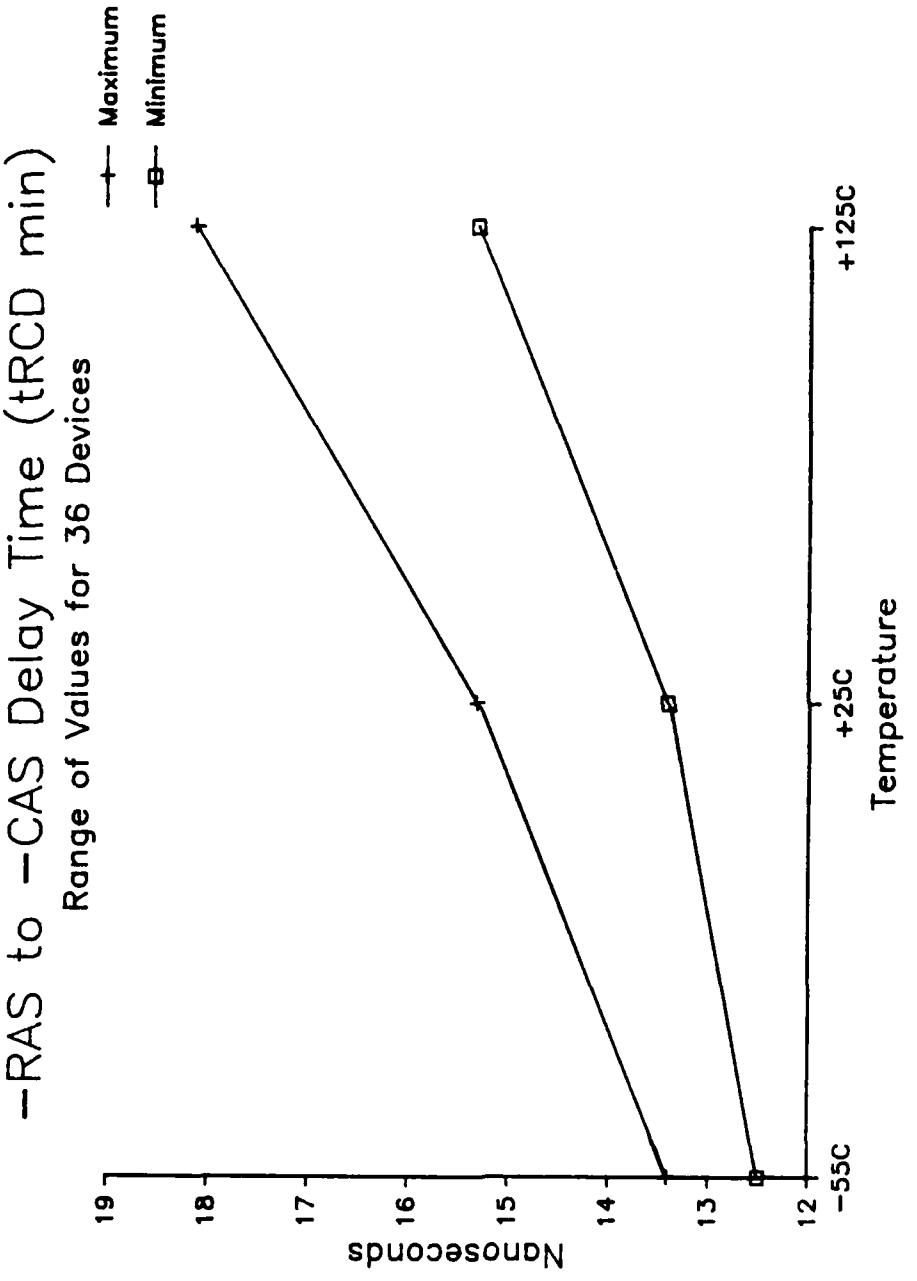


Figure 23: -RAS to -CAS Delay Time

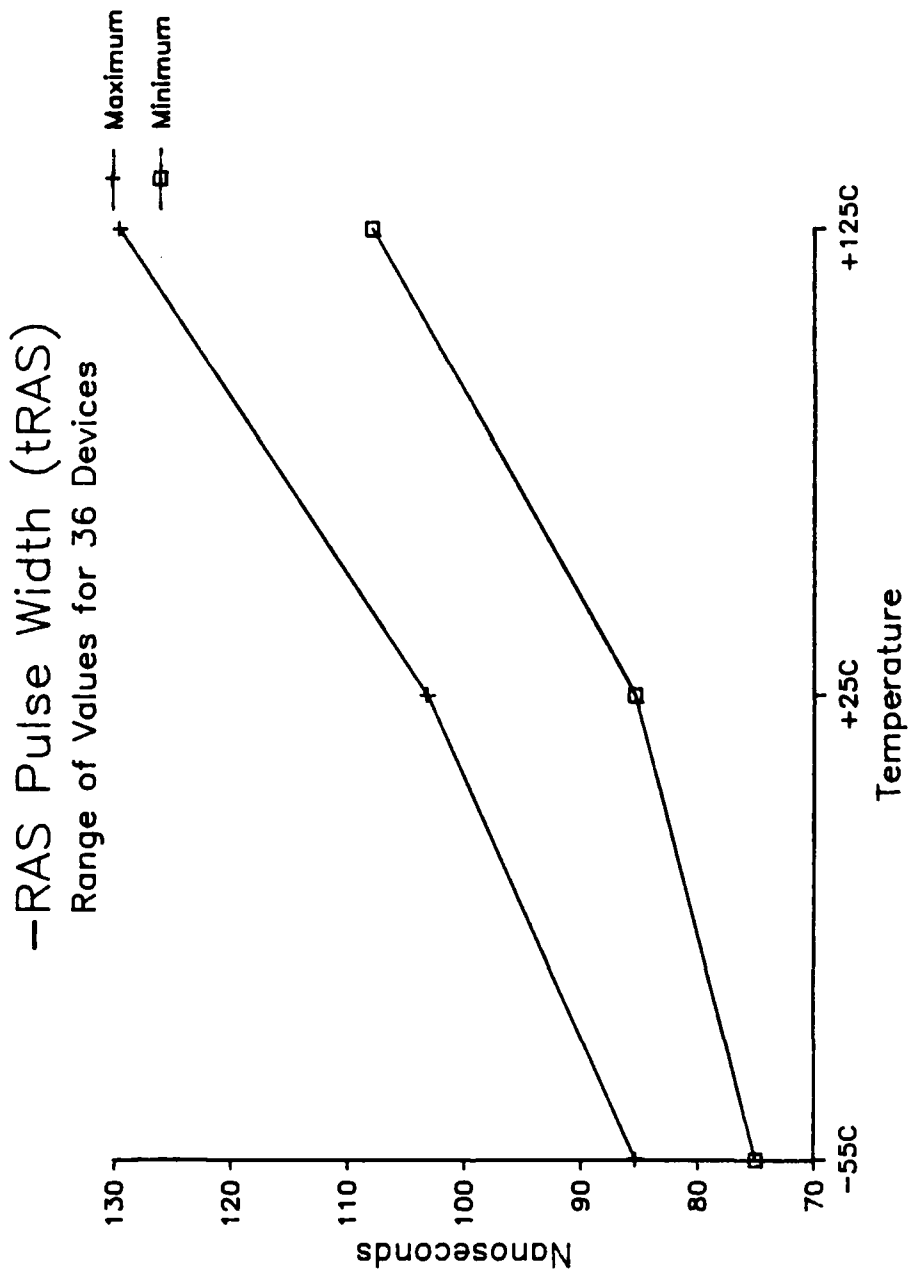


Figure 24: -RAS Pulse Width

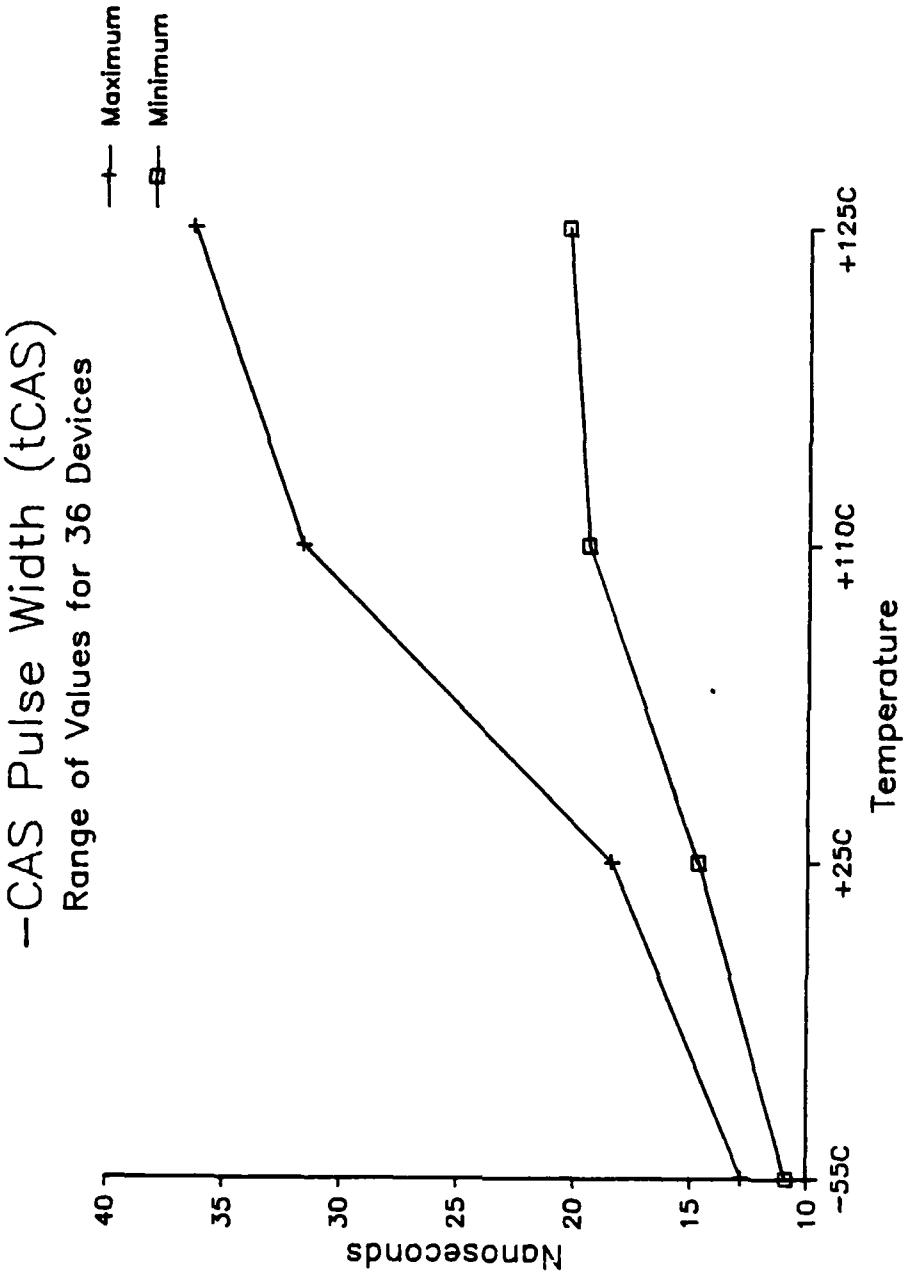


Figure 25: -CAS Pulse Width

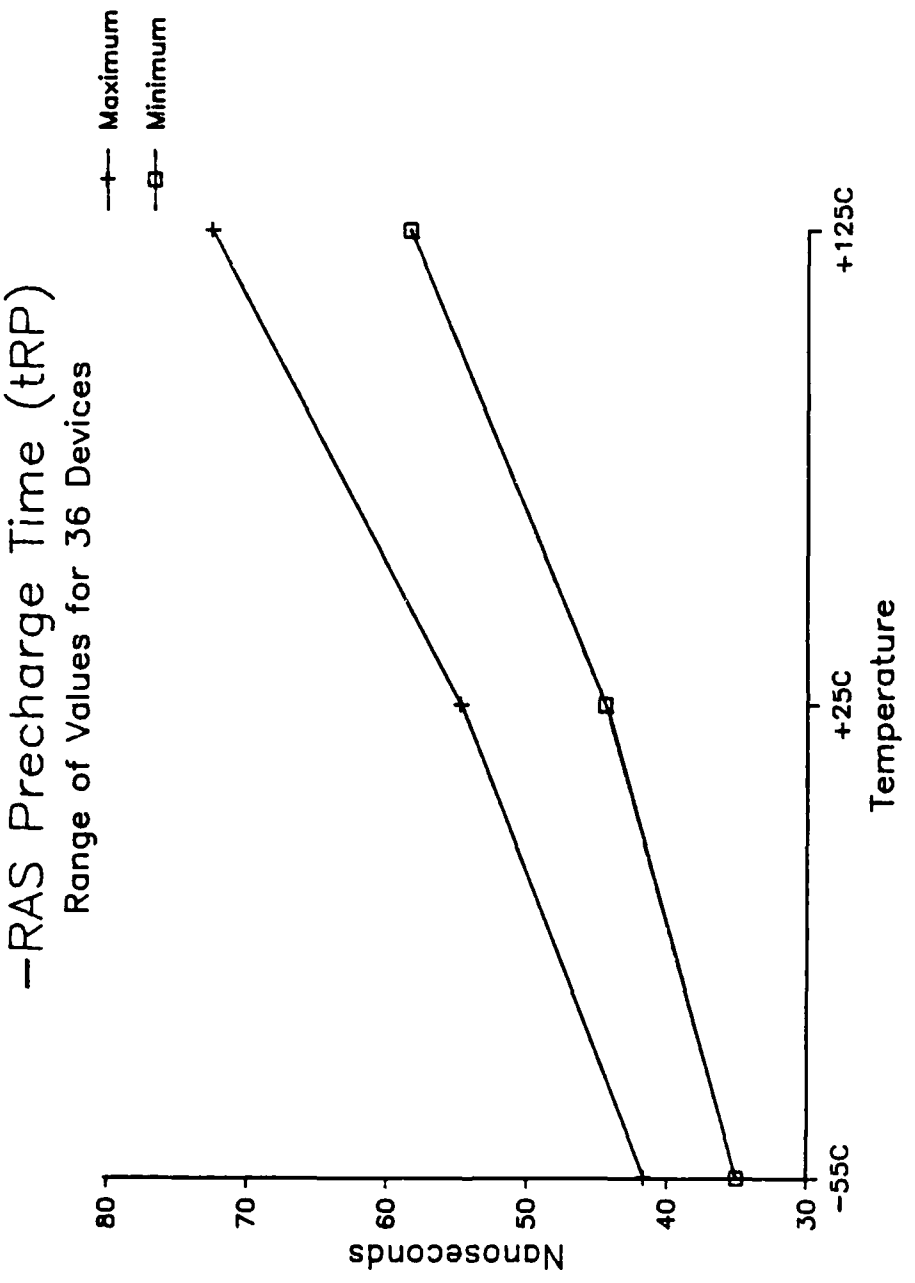


Figure 26: -RAS Precharge Time

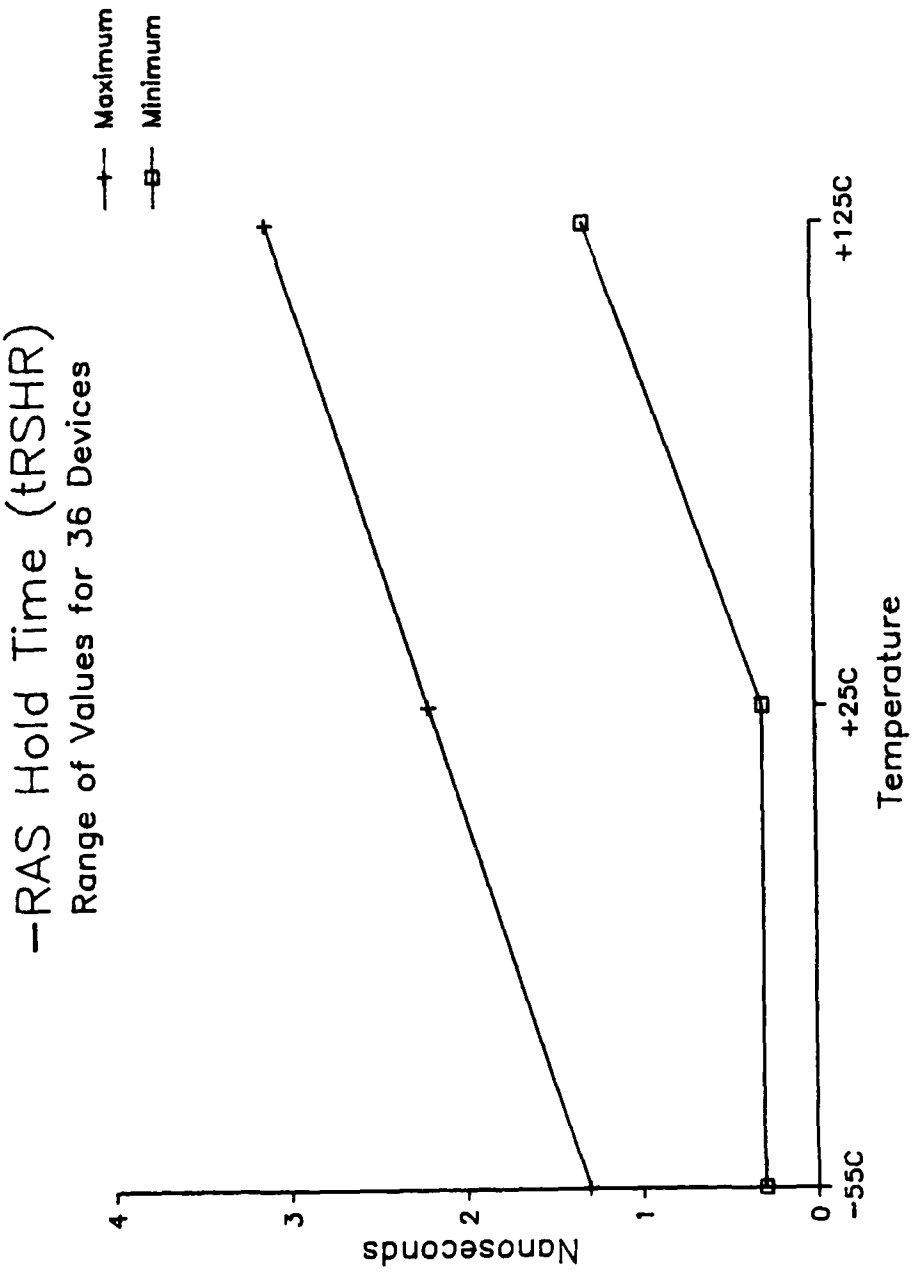


Figure 27: -RAS Hold Time (Read Cycle)

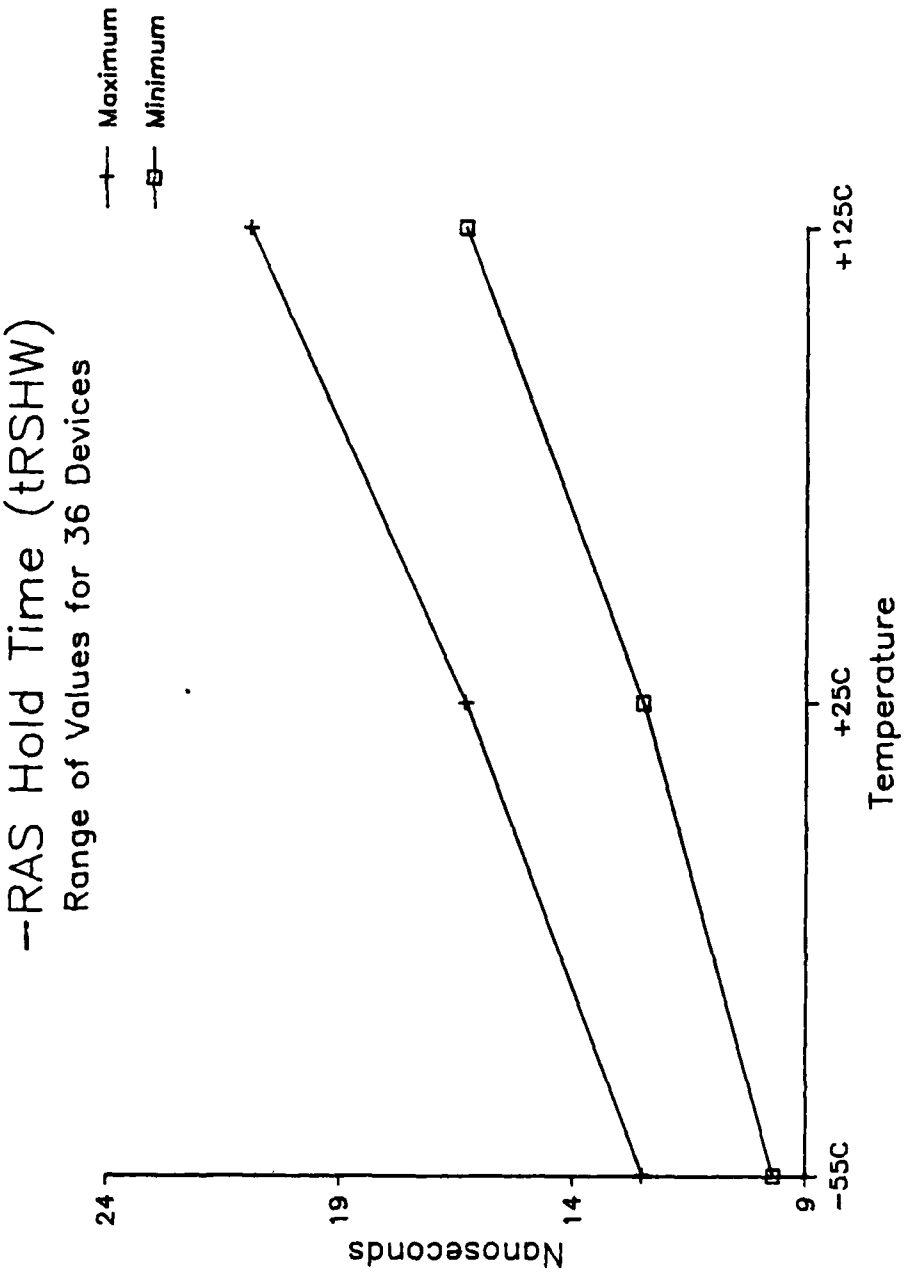


Figure 28: -RAS Hold Time (Write Cycle)

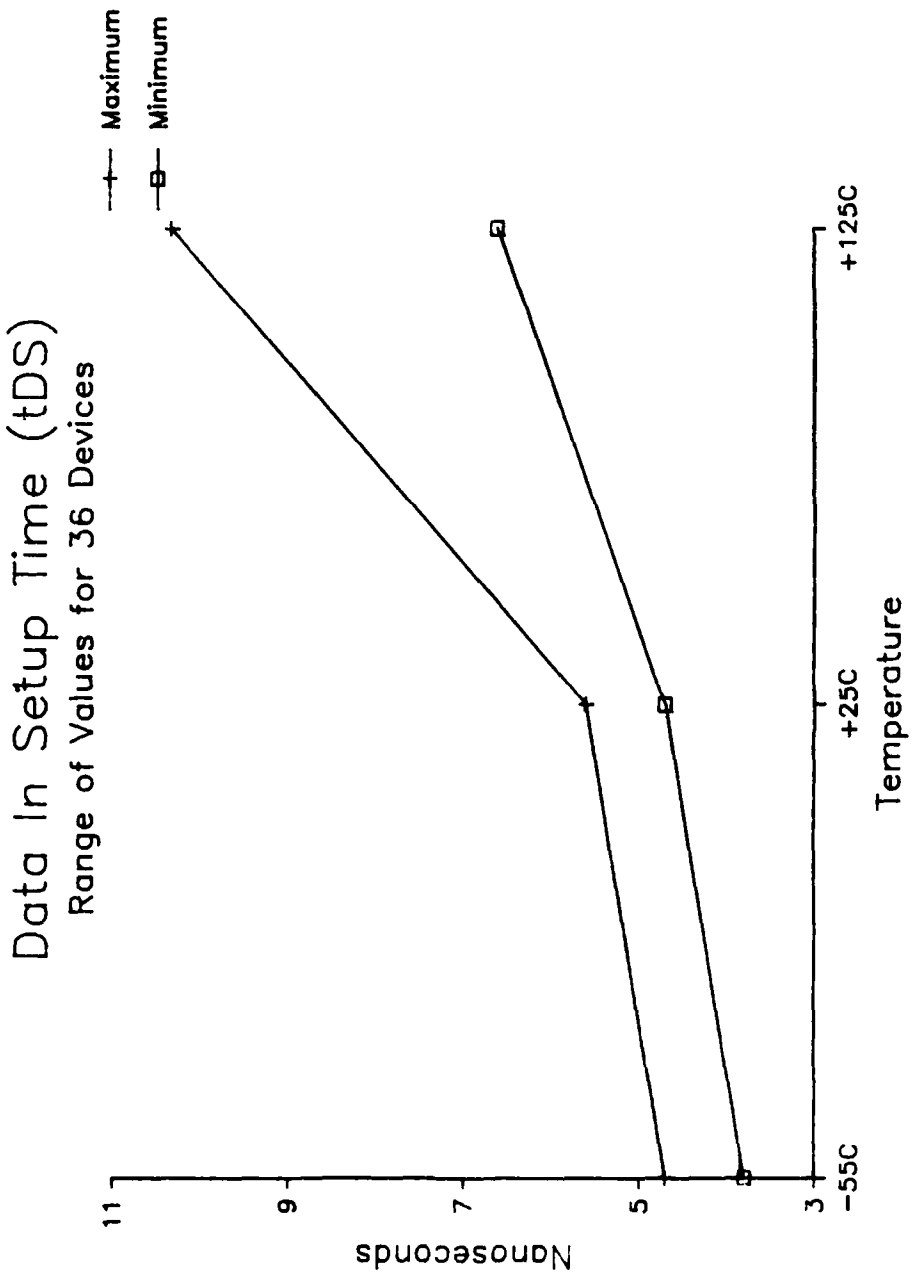


Figure 29: Data In Setup TIme

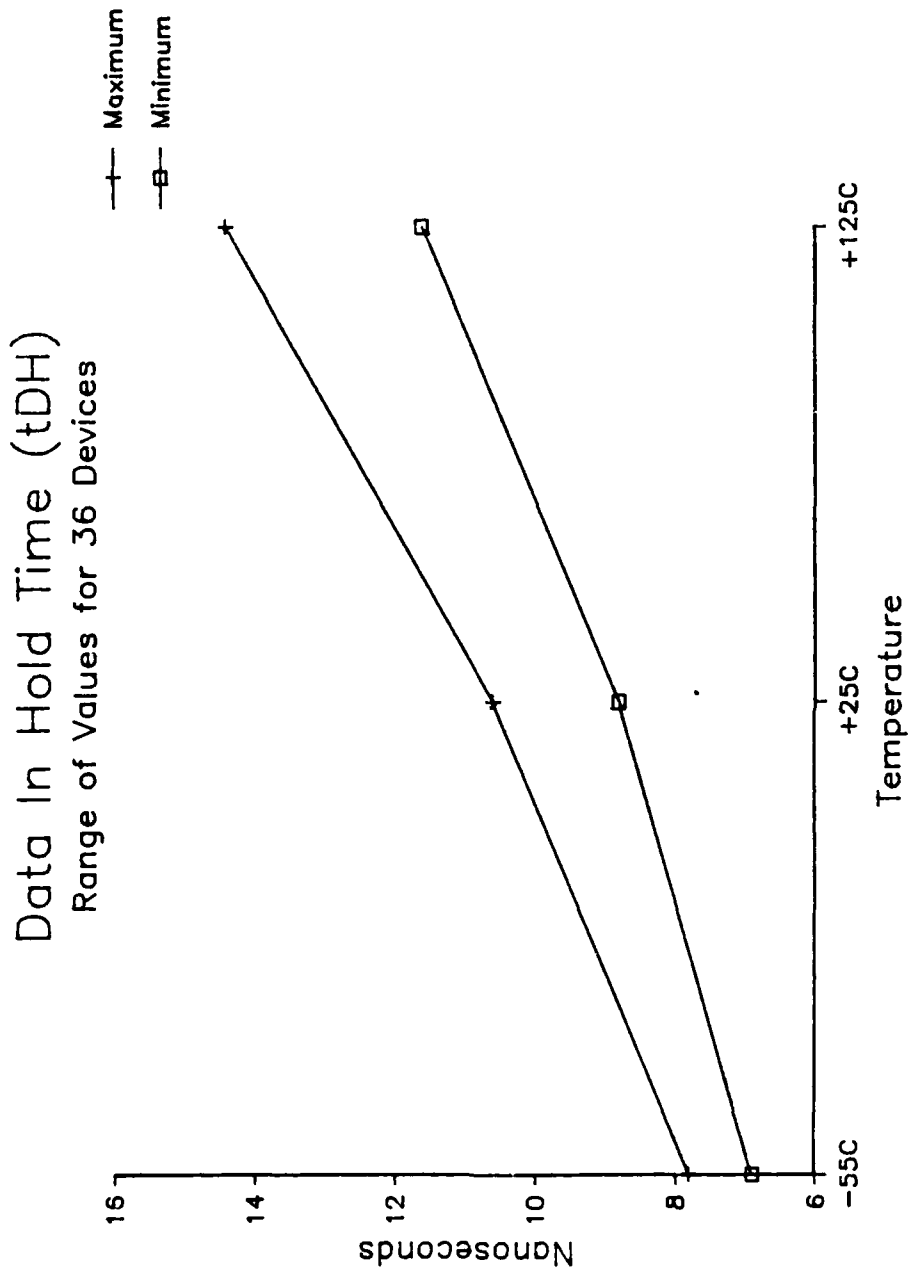


Figure 30: Data In Hold Time

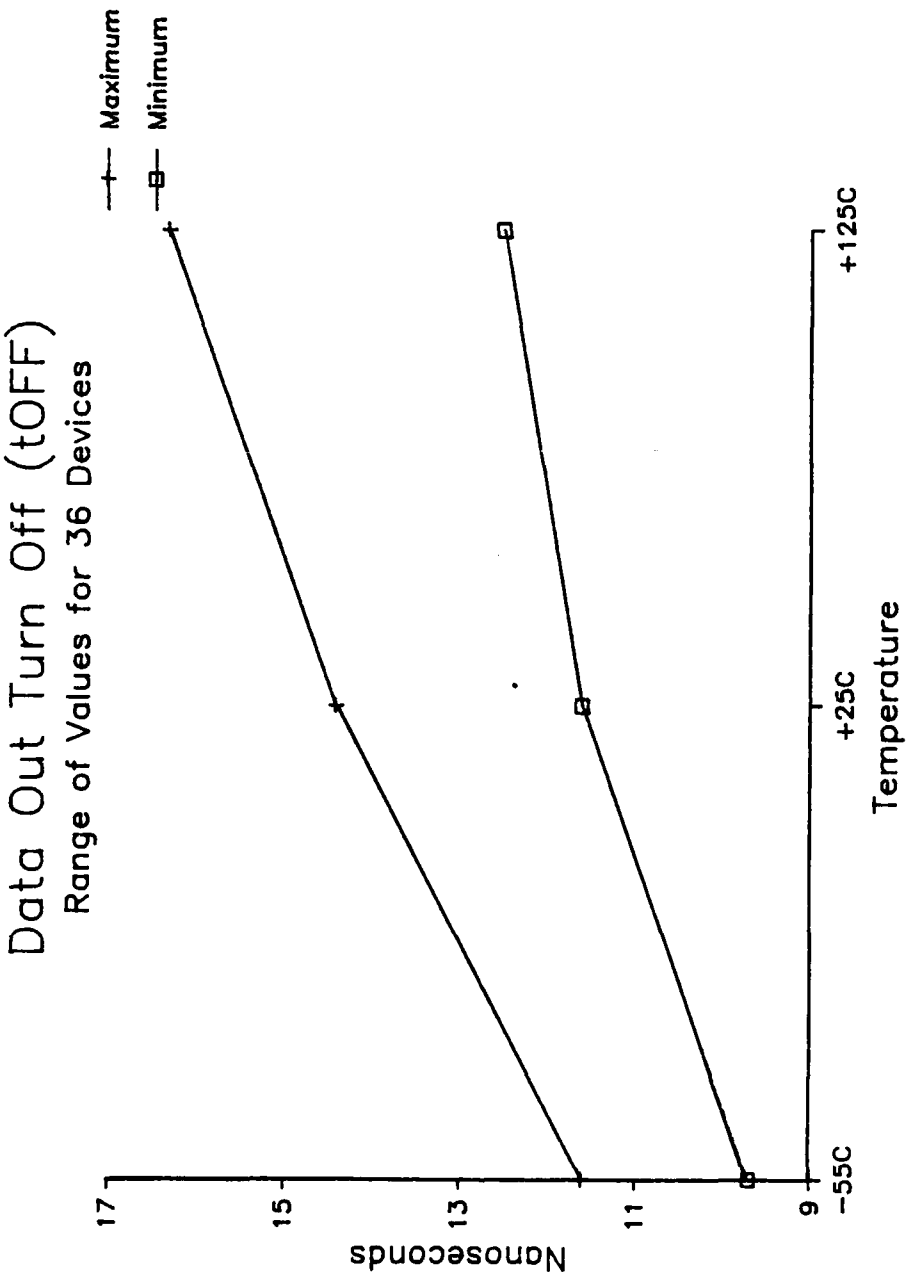


Figure 31: Data Out Turn Off Time

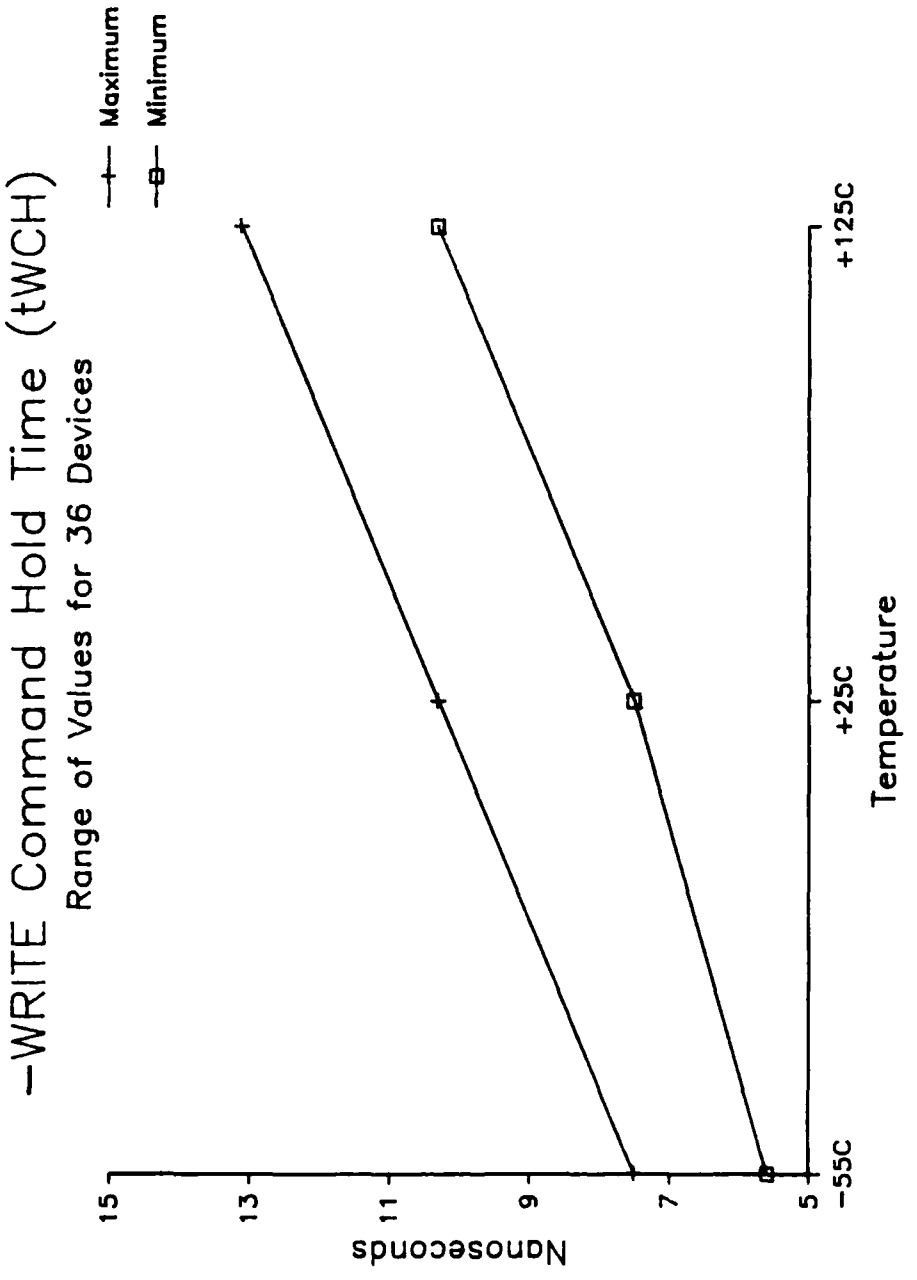


Figure 32: -WRITE Command Hold Time

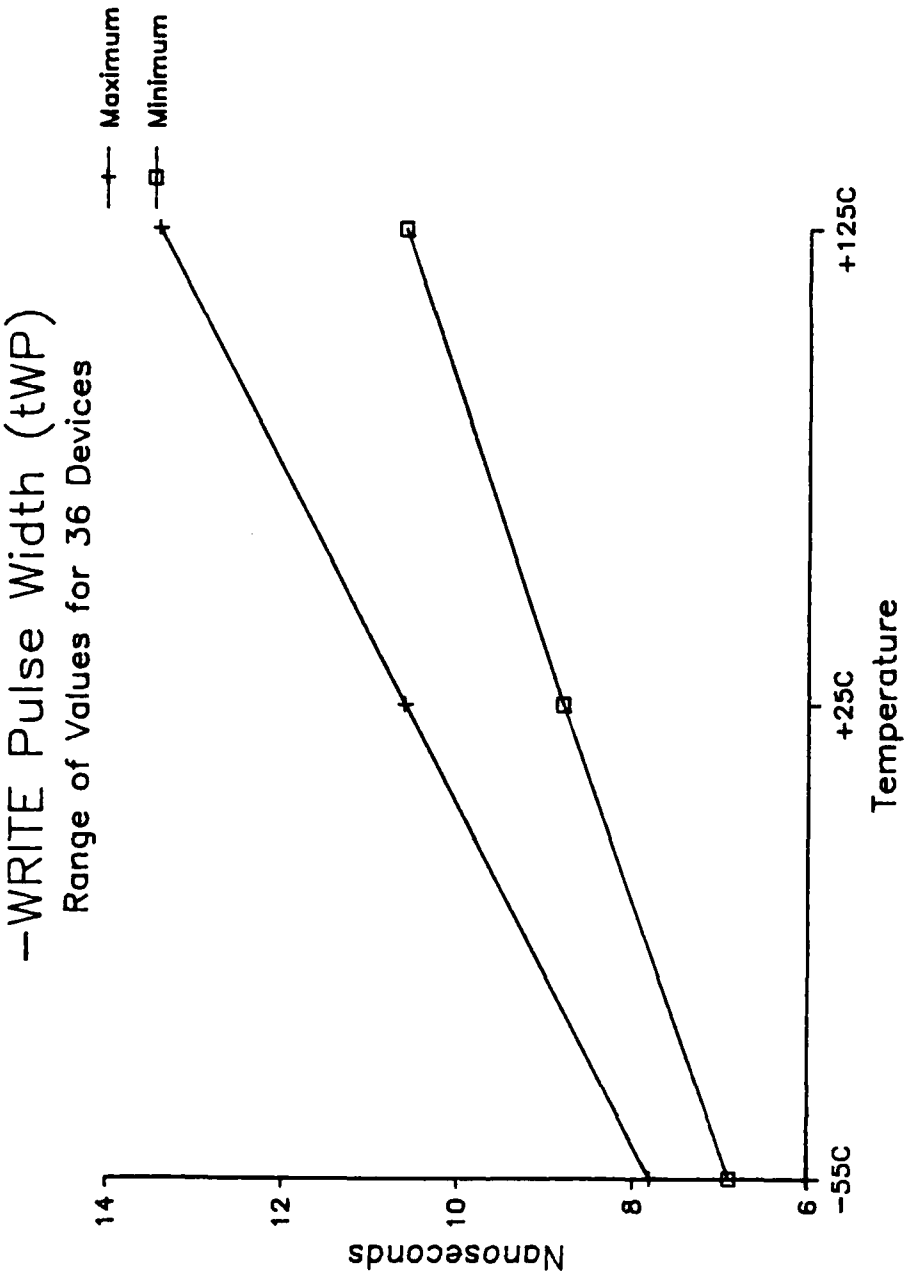


Figure 33: -Write Pulse Width

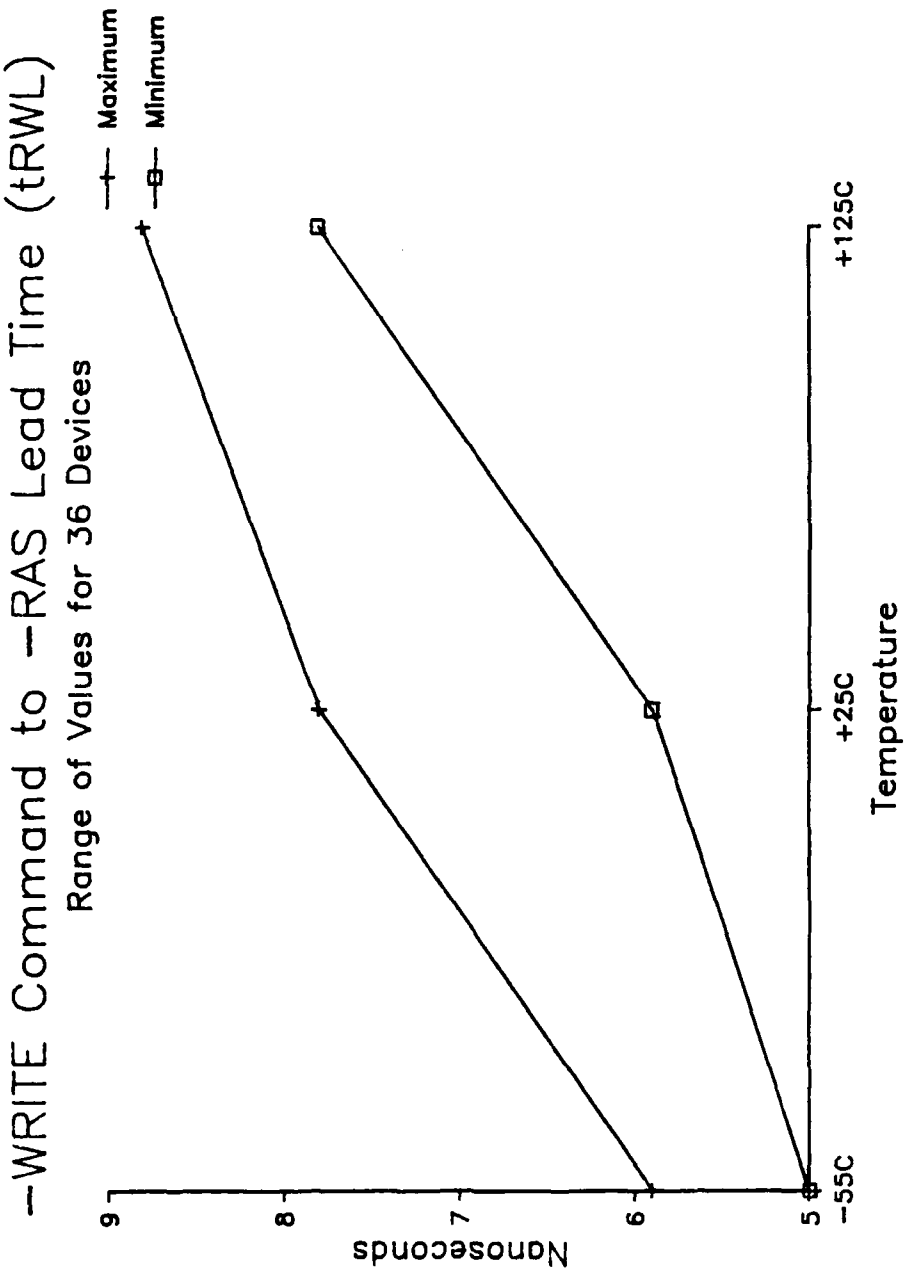


Figure 34: -Write to -RAS Lead Time

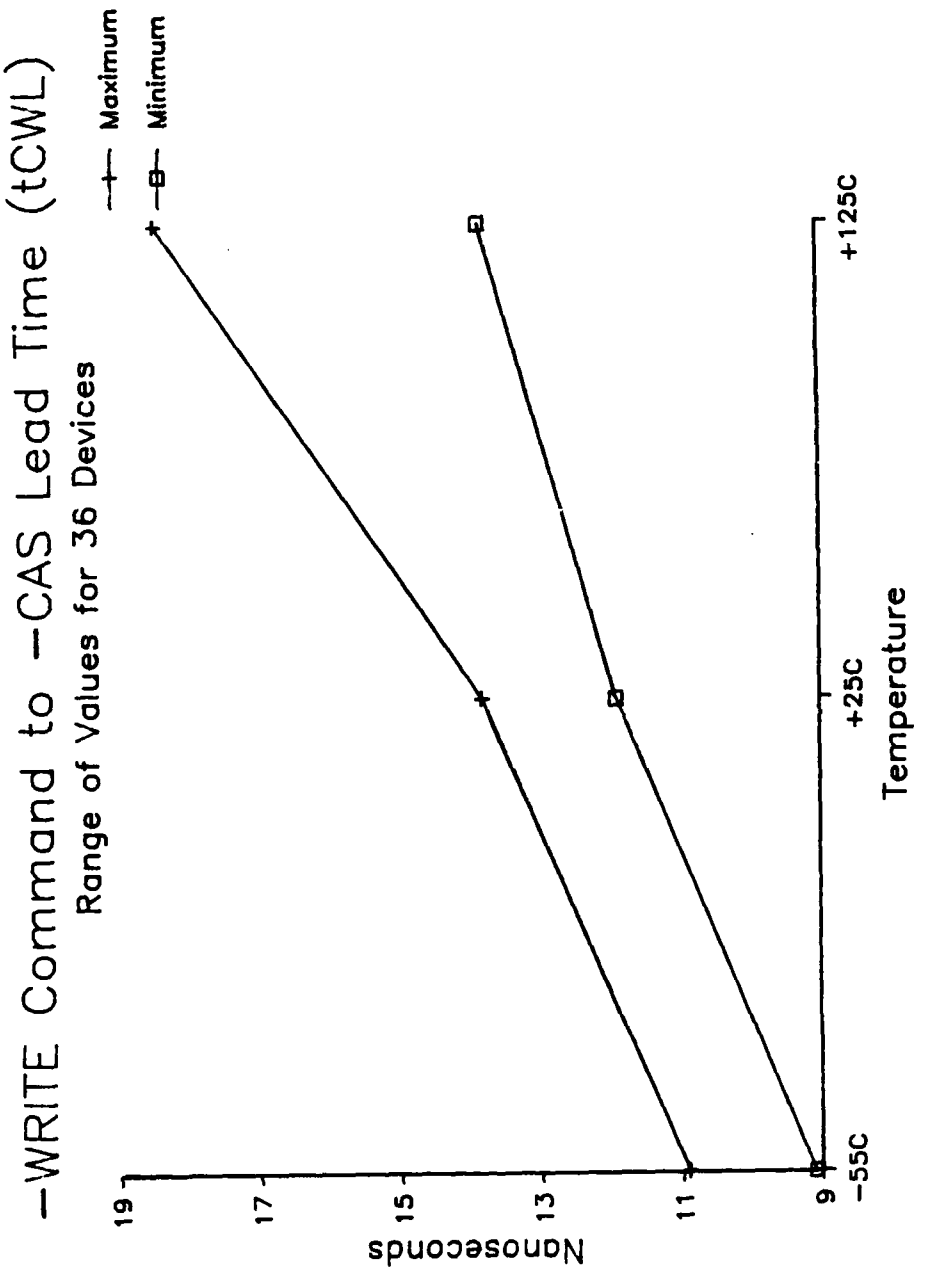


Figure 35: -Write to -CAS Lead Time

9. CONCLUSIONS

The objectives of this project were met in that the sample devices from one manufacturer, Intel, were characterized and the draft detail specification for the CMOS 256K dynamic RAM was prepared. Although the devices characterized were from only one vendor, which no longer manufacturers the device, it is felt that, once the other potential vendors have stabilized their product lines and established their individual device specifications, a compromise slash sheet can be created with minimum changes to the proposed one. Many of the characteristics of the measured devices are similar to those offered in preliminary data sheets from the possible future sources. The device characterization can be summarized as follows:

- o All DC parameters were met over the temperature range. Extreme care must be taken when characterizing devices at -55^{O}C to reduce the problems caused by the development of moisture at the test site causing excessive leakage currents.

- o The device can be rated in ESD category "A" (20V to 2000V).

- o The measured access times were, for the most part, well within the limits of the proposed slash sheet. However care must be taken to tighten up the screening limits on the Column Address Access time measurement to guarantee that the limit is met at high temperature.

- o There is considerable margin in the VDD operating range of the devices, which can be beneficial in device application in systems using battery power or low regulation power supplies.

- o The devices showed no tendencies toward pattern sensitivity.

- o The timing parameters met the predicted limits with two minor exceptions, which can be caught by tighter vendor out-going screens. These parameters, which should be watched, are -CAS Access Time (tCAC) and -CAS Pulse Width (tCAS), both of which exceeded the specified limit at 125^{O}C.

APPENDIX A

FUNCTIONAL ALGORITHMS AND TIMING SETS

Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. The algorithms were applied to the device in a topologically pure fashion. The timing conditions and input levels were established to properly evaluate specific parameters or characteristics.

In the following descriptions the term "pump cycle" refers to any type of cycle (read, write, or -RAS only) that produces refresh action. N = number of bits in the memory device.

PATTERN 1
CONTINUOUS READ, BACKGROUND DATA = X-BAR

This pattern is used to allow the maximum amount of current IDD to be drawn from the VDD power supply. It is performed in the following manner with minimum cycle timing:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Sequentially read entire memory
Step 4 - Repeat step 3 as many times as necessary to achieve a reading

Test time - Undefined

PATTERN 2
OUTPUT HIGH IMPEDANCE (tOFF.)

This pattern verifies the output buffer switches to high impedance (tri-state) within the specified 25 ns after the rise of -CAS. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load minimum address location with "0"
Step 3 - Read minimum address location and measure VOL
Step 4 - Raise -CAS and measure VOUT > VOL +0.1 V after 25 ns delay
Step 5 - Load minimum address location with "1"
Step 6 - Read minimum address location and measure VOH
Step 7 - Raise -CAS and measure VOUT < VOH -0.1 V after 25 ns delay

Test time = 12 x cycle time

PATTERN 3
VBUMP DATA BACKGROUND = ALL "0" (discharged state)

This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

Step 1 - Perform 8 pump cycles with VDD set at 4.5 V
Step 2 - Load memory row with background data
Step 3 - Pause 100 us ramping VDD to 5.5 V inhibiting all clocks
Step 4 - Read memory row with background data
Step 5 - Load memory row with background data
Step 6 - Pause 100 us ramping VDD to 4.5 V inhibiting all clocks
Step 7 - Read memory row with background data
Step 8 - Repeat steps 2 through 7 for remaining rows
Step 9 - Repeat steps 2 through 8 for background data complement

Test time = (8N + 8) x cycle time + 204.8 ms

PATTERN 4
ADDRESS COMPLEMENT, BACKGROUND DATA = CHECKERBOARD

This pattern produces maximum address line noise and checks the decoder dynamic response times. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Read minimum address location
Step 4 - Write minimum address location with complement data
Step 5 - Read maximum address location
Step 6 - Write maximum address location with complement data
Step 7 - Read minimum address location + 1
Step 8 - Write minimum address location + 1 with complement data
Step 9 - Read maximum address location -1
Step 10 - Write maximum address location -1 with complement data
Step 11 - Repeat steps 3 through 10 until all address locations have been read and loaded with complement data
Step 12 - Repeat steps 3 through 11 reading complement data and writing data
Step 13 - Read memory for data

Test time = (6N + 8) x cycle time

PATTERN 5
SHIFTING DIAGONAL, INITIAL BACKGROUND DATA = MAJOR DIAGONAL

This pattern tests for sense line imbalance and response plus the data restore noise. In addition, it tests for multiple selection and is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with data background, scan from minimum address location to maximum address location
Step 3 - Read data in the memory, scan from maximum address location to minimum address location
Step 4 - Repeat steps 2 and 3, each time shifting the diagonal by one until it has occupied every position in the memory (512 load/read scans)
Step 5 - Repeat steps 2 through 4 with complement data

Test time = (1024N + 8) x cycle time

PATTERN 6
MARCH DATA, BACKGROUND DATA = ALL "0"

This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Read location 0
Step 4 - Write data complement in address location 0
Step 5 - Read data complement in address location 0
Step 6 - Repeat steps 3 through 5 for all other locations in memory (sequentially)
Step 7 - Read data complement in address location 0
Step 8 - Write data in address location 0
Step 9 - Read data in address location 0
Step 10 - Repeat steps 7 through 9 for all other locations in the memory (sequentially)
Step 11 - Repeat steps 2 through 10 with data background of all "1"

Test time = (14N + 8) x cycle time

PATTERN 7
CHECKERBOARD REFRESH TEST (CELL RETENTION)

This test is used to check the retention time of memory cells under static and dynamic conditions. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with Checkerboard data
Step 3 - Pause 4 ms with -RAS = VIH and all other inputs cycling
Step 4 - Read data in all locations
Step 5 - Load memory with complement Checkerboard data
Step 6 - Pause 4 ms with -RAS = VIH and all other inputs cycling
Step 7 - Read complement data in all locations

Test time = (4N + 8) x cycle time + 8 ms

PATTERN 8
EXTENDED CYCLE TEST (10us), BACKGROUND DATA = X-PARITY/Y-PARITY

This test is used to verify the 10us maximum limit on -RAS or -CAS pulse widths. Front and back edge timings are held to normal cycle timing in relation to the beginning and end, respectively, of the particular cycle. The middle of the cycle, where -RAS and -CAS are held low, is increased to allow 10 us of -RAS and -CAS active time (low level). It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Write X-Parity data in location 0
Step 3 - Read X-Parity in location 0
Step 4 - Repeat steps 2 and 3 for all other locations in the memory (sequentially)
Step 5 - Repeat steps 2 through 4 with complement data
Step 6 - Write Y-Parity data in location 0
Step 7 - Read Y-Parity in location 0
Step 8 - Repeat steps 6 and 7 for all other locations in the memory (sequentially)
Step 9 - Repeat steps 6 through 8 with complement data

Test time = (8N + 8) x cycle time

PATTERN 9
RAS-ONLY/REFRESH TEST

This test is used to verify the functionality of the RAS-only mode of cell refreshing. It is done at high temperature only and is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with all "0"s
Step 3 - Perform 128 RAS-only cycles (-CAS = -WRITE = "1")
Step 4 - Repeat step 3 for 0.5 seconds
Step 5 - Read memory, all "0"s
Step 6 - Repeat steps 2 through 5 with all "1"s

Test time = (4N + 8) x cycle time + 20 seconds

PATTERN 10
SURROUND DISTURB TEST

This test is used to check for adjacent cell influence on the contents in the cell of interest.

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with all "0"
Step 3 - Set test address to 0
Step 4 - Write "1" into test cell
Step 5 - Write "0" into all adjacent (one row and/or one column address different) four times
Step 6 - Read test cell
Step 7 - Increment test bit address
Step 8 - Repeat steps 2 through 7 for all locations of test bit
Step 9 - Repeat steps 2 through 8 for complement data

Test time = (70N + 8) x cycle time

TABLE OF CONTENTS

32R16 PAL

1. SUMMARY

This report covers the investigations made regarding programmable logic devices with respect to the contract. The objective of this portion of the contract with RADC was to select and electrically characterize a high-density, state-of-the-art programmable logic device (PLD). In addition, a preliminary MIL-M-38510 slash sheet was to be developed for the selected device.

The device selected for evaluation was the PAL32R16 "MegaPAL" from Monolithic Memories, Inc. The PLD evaluation project was later dropped from the contract work primarily due to the unavailability of MIL version PAL32R16 devices for a majority of the contract time period. (PAL and MegaPAL are registered trademarks of Monolithic Memories Incorporated.)

This report summarizes the work done towards meeting the above stated objectives; in addition, it gives an overview of PLD products and device programming systems which are currently available.

2. INTRODUCTION

The two major topics covered in this report are the contract work done on programmable logic devices and an overview of PLDs which are currently on the market. The contract activities are reviewed from the contract proposal stage through the eventual termination of the PLD evaluation project. The review of current PLD options gives an overview of device types and device programming systems which are currently available to PLD circuit designers.

3. CONTRACT PROGRAMMABLE LOGIC DEVICE ACTIVITIES

The programmable logic device evaluation project work which was completed under this contract consisted mainly of manufacturer and literature surveys to select a device for evaluation, the identification and allocation of equipment needed to program and test the device, and numerous attempts to obtain military-grade device samples.

3.1 BACKGROUND, MANUFACTURER SURVEY, AND DEVICE SELECTION

Per the contract proposal, the device selection process used information from a vendor survey, a literature survey, MIL requirements, and GTE data from related component evaluations. The selection process was not finalized prior to the beginning of the contract. The intent was to continue the survey during the early part of the contract in order to select a state-of-the-art programmable logic device for evaluation. Emphasis was given to device complexity and technology, balanced against sample availability and domestic manufacture of product. Other selection criteria included multiple sourcing and manufacturer intent to fabricate product to MIL specifications.

3.1.1 Initial Manufacturer Survey

In early 1984, the selection of programmable logic device products was limited. At that time, only six manufacturers offered PLDs. Monolithic Memories Incorporated (MMI) was the leader in PAL (registered trademark of MMI) products. Three of the manufacturers (Fairchild Semiconductor Corporation, Signetics Corporation, and Texas Instruments Incorporated) limited their PLD products to Field Programmable Logic Array or Field Programmable Logic Sequencer (FPLA/FPLS) devices. Of these three, Texas Instruments was then in the process of developing PAL products to second source, small, standard MMI PALs. Advanced Micro Devices was relatively new to the PLD market and offered Programmable Array Logic (PAL) devices with relatively low circuit complexity; however, Advanced Micro Devices had a more versatile PAL device under development. National Semiconductor Corporation was the main second-source for MMI PAL products.

The initial vendor and literature search for a state-of-the-art PLD, which was conducted for the contract proposal, indicated that multiple sourcing (Fairchild Semiconductor Corporation and Signetics Corporation) was available for an FPLA with a 16X48X8 configuration (16 inputs, 48 product terms, and 8 outputs). The other prime candidate device per the initial survey was the PAL22V10 which was soon to be manufactured by AMD. The PAL22V10 device has eleven dedicated input pins and eleven dual-function pins (one clock/logic and ten programmable

input/output pins). This device incorporates the capability of defining and programming the architecture of each output.

3.1.2 Device Selection

An additional vendor survey was made after the start of the contract in the second quarter of 1984. At that time, all PLDs were fabricated using bipolar TTL integrated circuit technology. The manufacturers of PLDs at the time of the second survey were: Advanced Micro Devices Incorporated (AMD), Fairchild Semiconductor Corporation (FSC), Monolithic Memories Incorporated (MMI), National Semiconductor Corporation (NSC), Signetics Corporation, and Texas Instruments Incorporated (TI). The only significant difference from the results of the first survey was that MMI was planning to release their "MegaPAL" (registered trademark of MMI) series devices in the near future.

3.1.3 Summary

The following comments summarize the manufacturer surveys which were made prior to device selection in May of 1984.

- Although the AMD PAL22V10 was one of the initial candidates, it was not selected because its architecture did not follow the standard PAL architecture of MMI and was not alternately sourced. AMD did not have any immediate plans to alternately source the MMI complex PAL products.

- Fairchild manufactured one FPLA device which was of a 16X48X8 (inputs, transition terms, and outputs) structure like one of the Signetics FPLAs.

- MMI was considered to be the industry leader in PAL device products and already had a rather large product base of SSI/MSI PAL devices. Their PAL32R16 and PAL64R32 "MegaPAL" products represented the maximum PAL device complexity available at that time. MMI indicated plans to offer MIL versions of these products. The PAL32R16 with 32 inputs (16 dedicated and 16 feedback) and 16 registered outputs was selected for evaluation under this contract.

- National Semiconductor expressed an interest in being involved in the MIL PAL evaluation project and indicated plans to alternately source the MMI "MegaPAL" products. At that time, commercial-grade PAL32R16 parts were not due to be available until fourth quarter 1985, and MIL version product was scheduled for third quarter 1986 availability. The National Semiconductor PAL32R16 would therefore not be available for evaluation in this project.

- o Signetics offered an assortment of FPLA and FPLS devices. The largest of these arrays was a 16X48X8 structure. Signetics did not manufacture any PAL devices like those made by MMI. In addition, Signetics did not provide a positive indication regarding developing MIL version PLD products.

- o Texas Instruments manufactured an FPLA, and several versions of FOA (Fixed-OR-Array) products. The FPLA product (14X32X6) was less complex than the FPLAs made by Signetics. Three versions of Fixed-OR-Array products were offered. The basic FOA products were essentially alternate source versions of MMI small-complexity PAL devices. The other two sets of FOA products were latched input and registered input versions of the basic Fixed-OR-Array products.

Based upon the survey of PLD manufacturers in the first half of 1984, MMI was the leader in PAL products, and Signetics was the leader in PLA products. The MMI PAL32R16 and PAL64R32 "MegaPAL" devices represented the maximum complexity in PAL device architectures at the time of the survey. The PAL32R16 was selected for evaluation under this contract since it was further along in development than the PAL64R32.

3.2 DESCRIPTION OF THE PAL32R16

The PAL32R16, manufactured by Monolithic Memories Incorporated, is a high-density programmable array logic device which is fabricated using an advanced Schottky TTL process and utilizes PROM fusible link technology. This device has 32 inputs and 16 registered outputs. Sixteen of the 32 inputs are via feedback or Input/Output paths. All 32 inputs are separately buffered to provide complementary drive to the AND array. The 16 outputs are configurable to allow the implementation of an active high or low output, registered or combinatorial logic output modes, an I/O mode (output buffer can be placed in a high-impedance state), and output feedback to the array. The output registers are D-type flip-flop structures. The PAL32R16 AND-OR array has 8,192 fuses which accommodate 64 input lines (32 input pins via buffers with complementary outputs to the AND array) and 128 product lines. The 8K AND-OR array and the output modes are configured by selectively blowing fusible links to obtain semicustom logic functions. Per MMI, the PAL32R16 can implement up to 1,500 equivalent logic gates.

The PAL device transfer function is a sum-of-products expression. The logic matrix consists of a programmable AND array driving a fixed OR array. The PAL32R16 is a synchronous state-machine that implements the state equation Y:=f(X,Y) , where the state vector Y is replaced by a Boolean function of Y and the input vector X, on the rising edge of the clock signal. As previously stated,

each of the 16 output cells can be configured to provide a registered or combinatorial logic output mode with active high or low outputs. Registers can be bypassed in groups of eight to yield a bank of eight combinatorial outputs. Bypassing a bank of registers eliminates the feedback lines for those outputs. Outputs within a bank must be either all registered or all combinatorial. Two separate clock pins and two preload pins permit independent clocking and preloading of register banks. The preload operation is asynchrounous with respect to the clock. The registers are loaded on the low-to-high clock transition. In addition, each output can be placed into a high-impedance mode and can serve as an input node. The outputs also are available for feedback to the input AND array.

The outputs of the PAL32R16 can accommodate product term sharing between two output cells. For a typical output pair, each product term can be used by either output. Since the product term sharing is exclusive, a product term can be used by only one output, i.e., product terms are available to both, but can be connected to only one of the outputs in a pair. If equations call for an output pair to use the same product term, a separate product term is generated for each output. The product term sharing architecture permits product term editing, i.e., the user can delete an unwanted product term and reprogram a previously unused product term to the desired new fuse pattern. A disabled product term is powered down and typically yields a reduction of 250 microamperes in supply current drain. The PAL32R16 operates with a supply voltage of 5 VDC +/- 10% and draws a maximum of 280 milliamperes. The output buffers can source 2 mA and sink 8 mA of current at 2.4 and 0.5 V, respectively. The propagation delay is 50 nanoseconds for combinatorial and 30 nanoseconds for registered output modes.

Package options for the PAL32R16 include a 40-pin ceramic or plastic dual-in-line package, a 44-pin ceramic leadless chip-carrier, and a 44-pin plastic leaded chip carrier.

3.3 DEVICE PROGRAMMING AND TEST EQUIPMENT

The equipment identified for use in programming the MMI PAL32R16 was the Data I/O Corporation 303A-008A Programming/Testing adapter which was to be used with a Data I/O LogicPak (registered trademark of Data I/O Corporation) and a model 29A Universal Programmer. This selection was made because a model 29A programmer and a LogicPak were already available for use. The 29A Universal Programmer, LogicPak, and appropriate Programming/Testing adapter serve as part of a programmable logic development system. This set of equipment can serve as a stand-alone system when a Data I/O "PALASM" (registered trademark of MMI) adapter is connected to the LogicPak and a video terminal is connected to the programmer mainframe (29A). An alternative

Programmable Logic Design System (PLDS) may be completed by connecting the 29A, with LogicPak, to a host computer system such as an IBM-PC and running PALASM and communications software programs on the PC. PALASM stands for Programmable Array Logic ASseMbler and is a registered trademark of MMI.

For the PAL32R16 evaluation project, a Data I/O model 29A Universal Programmer with LogicPak was to be linked to an IBM personal computer. The logic circuit fuse map files were to be generated by using MMI's PALASM2 (programmable array logic assembler, version 2) software to process the PAL design specification files. The resultant fuse map files could then be downloaded to the Data I/O device programming system from the host personal computer. The PALASM software serves to process PAL device logic circuit design specification files to produce documentation, assemble the design data, perform circuit function simulation and verification, and to produce a device programming fuse map file. The fuse map files are arranged into a standardized JEDEC format (JEDEC STD. JC-42.1-81-62) which is compatible for downloading to the Data I/O system. This JEDEC format has become the industry standard for use in the transmission of PLD fuse map data, and optionally appended test vector, files.

The electrical characterization testing of the PAL32R16 was planned to be done on a Fairchild Sentry VII digital integrated circuit automatic test equipment system.

3.4 SUMMARY OF PLD CONTRACT ACTIVITY

The initial work on this project involved the review of manufacturers and literature in order to select a high-density, state-of-the-art programmable logic device for electrical characterization testing. When the MMI PAL32R16 was selected for evaluation in May of 1984, fully tested military version product was due to be available in September of that same year. MMI reportedly made a revision to military version PAL32R16 product in December of 1984. Even though commercial MMI PAL32R16 product was on the market, fully tested military version product remained unavailable throughout most of 1985.

When the MIL version product was still unavailable in August of 1985, a final survey was made regarding sourcing of the subject device. The results of that survey indicated that MMI was still the only manufacturer of the PAL32R16. National Semiconductor was the only remaining manufacturer with any plans to alternately source this device. National's plans were tentative with respect to this device at that time, and availability of their PAL32R16 product was to be near the end of 1986, if at all. Six other manufacturers were contacted regarding the possibility of alternately sourcing the PAL32R16. None of these manufacturers had any definite plans to make this device since they reportedly did not perceive a sufficient market for this device. The fixed PAL structure tends to limit larger

circuit applications, and the maximum supply current drain of 280 milliamperes is also a deterrent. Most of these manufacturers were pursuing new PLD designs which deviated from the fabrication processing technology and architecture of the PAL32R16, *i.e., they did not think that the PAL32R16 was a viable product.*

In October of 1985, MMI stated that military version PAL32R16 product would not be available until mid November. Because of several previous delays in MIL version product availability, it seemed doubtful that MIL version devices would be available in time to allow device characterization before the end of the contract period. In consideration of the sample procurement problems and of the fact that RADC had expressed a strong interest in evaluating the 512K EPROM, which became available from Intel midway through the contract period, it was mutually decided to drop the PAL device in favor of this EPROM device.

4. OVERVIEW OF APPLICATION-SPECIFIC IC DEVICES

Application Specific Integrated Circuit (ASIC) devices are generically composed of two major device categories namely, custom and semicustom integrated circuits. The custom integrated circuit category may be further subdivided into full custom and standard cell designs. The semicustom category of ICs can be subdivided into gate array (mask programmable) and programmable logic devices. The use of ASIC devices provides increased circuit density, higher reliability, and better circuit performance. Redesign of existing circuit assemblies using ASIC designs can yield cost reductions for medium to high volume electronic products. An additional benefit from using ASIC devices is greater security for proprietary circuit designs.

Application specific ICs comprise one of the fastest growing portions of the semiconductor product spectrum. The selection of a particular design approach involves tradeoffs which must be uniquely considered for each design case. The choice of either full custom, standard cell, gate array, or programmable logic devices corresponds to a descending scale of design time and fabrication complexity. The array of ASIC design tradeoffs includes time-to-market (design/prototype cycle time and production cycle time), nonrecurring engineering charges, design tools (availability, flexibility, ease of use, adequate documentation, and clearly defined methodology), device performance (process technology, speed, and power consumption), device architecture, device constraints (die size, gate count, logic product matrix size, and circuit density), device cost (low quantity and production volume), and alternate sourcing. Process technologies include bipolar (TTL and ECL), CMOS, and GaAs (future products).

Major differences between the four ASIC design approaches are evident in the areas of design methodology, device cost, development time, and development cost. Full custom ICs do not use predefined circuit function blocks and are generated from scratch by IC designers. For a given design, full custom ICs normally require development times in excess of one year and involve high nonrecurring engineering (NRE) charges. Standard cell ICs may be designed by system designers by utilizing predesigned and characterized logic circuit building blocks. Months may be required to implement a given standard cell design. Full custom and standard cell ICs are customized at all mask layers and generally have no alternate source of manufacture. Design revisions to full custom and standard cell products are not easily accommodated; moreover, nonstandard pinouts, nonstandard wire-bonding, and testing may present problems.

A gate array is composed of a prefabricated matrix of logic gates. Gate array logic circuit designs are implemented by appropriately interconnecting selected logic gates and associated I/O structures via one or two final metal mask layers. Gate array designs may be implemented faster and at less cost than full custom or standard cell designs. Gate array development requires a few months and

or standard cell designs. Gate array development requires a few months and costs tens of thousands of dollars to implement; in addition, gate array design changes are difficult to implement.

Designing with standard cells or gate arrays requires the designer to be proficient in CAD system use, to have access to an expensive computer-based work station, and to develop a comprehensive set of test vectors to satisfy fault coverage testing requirements. Logic and timing requirements must be simulated and verified for each design implementation. CAD (Computer-Aided-Design) tools are continuing to improve while becoming less expensive and are thereby becoming available to a growing user community.

Programmable logic devices have been generally considered to be at the low end of the ASIC spectrum. However, significant changes have occurred in PLD products over the past two years. First generation PLDs consisted primarily of a large assortment of PAL devices and a small assortment of FPLA devices. PLD devices were not widely used for a few years largely due to the limitations in design and programming software and documentation for these components. This problem has been virtually eliminated over the past two years, and PLDs are rapidly growing in use. Some of the newer PLDs now can serve to fill the gap between gate arrays and first generation PLDs or even replace smaller gate arrays in certain applications.

Shrinking integrated circuit device geometries and changes in device process technologies are significantly affecting ASIC devices. Due to reduced feature sizes, designs are becoming constrained more by bonding pad and I/O space requirements than by cell/die size limitations, and circuit density is increasing significantly for given die size products. Along with the inherent low power consumption and high noise immunity, CMOS devices are continuing to realize reduced propagation delays and higher density circuitry as device geometries continue to shrink.

5. OVERVIEW OF PROGRAMMABLE LOGIC DEVICES

The generic category of programmable logic devices currently includes Programmable Logic Elements (PLE,PROM), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Erasable Programmable Logic Device (EPLD), Electrically Erasable PLD (EEPLD), Electrically Reprogrammable Application Specific IC (ERASIC), Generic Array Logic (GAL), and dynamically-reconfigurable SRAM-based logic cell arrays. Included under the category of PLA devices are FPLA (Field Programmable Logic Array - combinatorial logic) and FPLS (Field Programmable Logic Sequencers - sequential logic) devices. The acronyms PAL and PLE, ERASIC, and GAL are registered trademarks of Monolithic Memories Incorporated, Exel Microelectronics, and Lattice Semiconductor Corporation, respectively.

Programmable logic devices are basically multiple input/output structures which contain field-programmable AND-OR logic arrays. Some PLD structures augment the basic combinatorial AND-OR arrays by providing features such as *programmable output polarity, XOR functions, programmable I/O modes* (three-state output buffers), registered outputs, feedback to the AND array, and arithmetic gated feedback to accommodate a variety of combinatorial and sequential logic designs. PLD products have changed significantly from the first-generation FPLA/S and PAL products to the current third-generation PLDs which feature CMOS process fabrication, reprogrammability, and macrocell building blocks.

Programmable logic devices accommodate the implementation of the sum-of-products form of logic equations via a basic architecture of an AND array driving an OR array. The distinction between PLE/PROM, PLA, and PAL devices is determined by whether the AND and OR arrays are programmable or fixed.

PLE/PROM devices feature a fixed AND array driving a programmable OR array, PLA devices have both AND and OR arrays programmable, and PAL devices have a programmable AND array driving a fixed OR array. PLE/PROM devices are used when a large number of input combinations or a large number of product terms per output are needed. PLA devices have the most general architecture in comparison to PLE/PROM and PAL devices. PLA devices often have longer propagation delays since signal paths traverse two large programmable arrays. PLE/PROM and PAL devices are structurally and functionally complementary. A PLE/PROM device has few inputs and many product terms, whereas a PAL device has many inputs and only a few product terms. PLEs have many product terms per output with product term sharing available, but PALs have few product terms per output with no product term sharing. PAL devices constitute the most widely used category of programmable logic devices.

Second-generation PAL products are typified by process revisions or process plus architectural enhancements. The process revision category includes enhanced bipolar processing technology to affect speed improvements and CMOS versions of first-generation PAL product designs. The bipolar products consist primarily of TTL structures; however, a few manufacturers have or will offer ECL versions as well. Many of the process enhancement versions use the same PAL architectures as MMI's original PAL product line. Other second-generation PLDs are expanded architectures in bipolar designs or range from CMOS versions of standard first-generation bipolar PALs to UV erasable or electrically erasable PALs with enhanced logic circuit functions and array sizes. Some second-generation PALs feature a generic architecture which permits a given device to emulate many of the first-generation standard bipolar PAL device types. Some of the first-generation FPLA and FPLS devices can also emulate several first-generation PAL products. Still other second-generation PLDs are larger versions of first-generation PALs or are unique, more complex bipolar PAL designs. The MMI "MegaPAL" products are examples of the latter category. Many of the second-generation PLD products are fabricated with a CMOS process.

Third-generation PLDs feature logic macrocells and high-density, complex logic circuit arrays. One of the newest PLDs features an SRAM-based architecture with reconfigurable logic macrocell arrays (Logic Cell Array, LCA, is a registered trademark of Xilinx) and reconfigurable interconnections. Virtually all third-generation PLD products are fabricated with CMOS processing technology.

The use of first-generation standard bipolar PALs and PLAs can serve to reduce required inventories of standard SSI and MSI TTL integrated circuit devices and to increase the density of logic circuit designs since one PLD can replace from three to twenty (estimates vary) standard SSI/MSI devices. The use of some second-generation "generic" PLDs can serve to further reduce inventory of first-generation PALs since one PLD can emulate any one of several first-generation PAL architectures. The use of third-generation PLDs can further bridge the gap between standard SSI/MSI ICs and gate arrays and can even replace small gate arrays in some cases. Device programming is implemented via fusible links in first generation bipolar PLDs, via EPROM cells in many second-generation devices, and via EEPROM or SRAM cells in third-generation PLDs.

The use of PLDs offers many advantages to logic circuit designers as outlined per the following points:

- o One PLD can replace from a few to many standard SSI/MSI digital ICs in a given circuit design, thereby:
  - Reducing the number of different, standard SSI/MSI digital ICs which must be inventoried.

- Reducing overall system cost via lower net IC count, reduced connector requirements, and reduced assembly labor per given design.

- Enhancing product packaging density.

- Increasing circuit and product reliability due to fewer parts and fewer interconnections (for both IC fabrication and circuit board assembly).

- Enabling the implementation of higher complexity logic circuit designs due to increased circuit density.

o In some cases, one PLD can, in turn, replace several first-generation PLDs, thereby, further reducing parts inventories and yielding greater circuit efficiency.

o Minor logic circuit revisions can be quickly implemented without necessitating printed circuit board revisions by merely programming a new fusible-link or reprogramming an erasable or electrically erasable PLD. The third-generation SRAM-based logic cell array can be reconfigured merely via a new memory load operation.

o Short cycle time for design-to-prototype and production revision cycles via the use of CAD tools.

o Wide availability of standard CAD and device programming tools - PLD design subsystems operate in conjunction with a host computer system (the ubiquitous IBM-PC series products are widely used for PLD design).

o Fills the gap between standard logic and LSI devices - wide application for "glue logic" - accommodates the implementation of nonstandard logic structures.

o Viable, low-cost, quickly implemented alternative to small-sized gate arrays. Various PLDs can serve to implement from a few hundred to a few thousand equivalent logic gates.

o Multiple sourcing of product.

o PLDs are becoming easier to use due to improved design and programming software and equipment systems; moreover, improvements in standardization, features, and price are continuing to evolve.

o The selection of PLD variations in process technology, architecture, and manufacturers is in a growth mode thereby presenting a wide array of options.

- o Relatively low design and development costs. Depending upon available device programming and host computer facilities, the NRE costs can range from moderate to virtually zero. Under certain circumstances, PLD design software may be available free of charge from some device manufacturers.

5.1 PLD FABRICATION TECHNOLOGIES AND CIRCUIT ARCHITECTURES

Programmable logic device technology has changed significantly over the past two years. Until 1985, all PLDs were fabricated via bipolar processing technology and used fusible links. The architectures of early PLDs were of PROM, and then PLA, and finally of PAL structures. The first of these to be marketed for logic circuit implementation were PLA devices. Previously, PLA devices did not gain wide acceptance among logic circuit designers because they were regarded by some designers as difficult to use; in addition, PLA design and development software and documentation were not fully refined or widely available. MMI simplified the use of field-programmable logic by modifying the basic PLA structure to have a fixed OR array thus yielding the PAL product. Fixing the OR array reduces the overall PLD size and lowers the propagation delay; however, this structure has a limited number of product terms and does not allow product term sharing. MMI also helped to alleviate the perceived design "bottleneck" by developing and making available its PALASM software. PALASM processes Boolean logic equations to generate a program pattern file to implement the expressions into a PAL device fuse map file. MMI then proceeded to release an array of PAL products to further enhance the utilization of programmable logic devices. Since the beginning of 1985, many new PLD products have entered the marketplace, and many more PLD manufacturers have emerged as well. The majority of the new PLDs are fabricated using CMOS technology and most of them are reprogrammable. Over the past two years, bipolar speeds have doubled and CMOS PLDs offer four times the circuitry per chip over first-generation bipolar devices.

PLD products can be generally regarded as already consisting of three generations of products. All three generation versions are currently available for use. The first-generation PLDs are composed primarily of FPLA, FPLS, and PAL devices with PAL device structures predominating. All first-generation PLDs are fabricated using bipolar process technology and used TTL structures. The series 20 and 24 PALS from MMI have become the de facto industry standard PAL architectures. These architectures are typified by devices with ten to twenty inputs and one to ten outputs. The basic architecture is a programmable AND array feeding a fixed OR array. The variations are primarily in the combination of the quantity of inputs and outputs and in modifications in the output structure. Output structure variations include fixed active high or low output, feedback,

direct or programmable three-state control, and registered (D flip-flop) outputs. Other manufacturers which have been the primary alternate sources for the first-generation MMI PAL products are Advanced Micro Devices, National Semiconductor, and Texas Instruments.

Second-generation PLDs consist of a mixture of device processing technologies and an even wider assortment of device architectures. Second-generation PLDs are virtualy all of PAL configurations. The fabrication processes consist of reduced power versions (one-half and one-quarter power - with attendant slower speeds) advanced bipolar processes to reduce propagation delays, ECL versions for further speed enhancements, and CMOS processing. The architectures of many of the bipolar devices are the same as the first-generation MMI PALs. Other second-generation bipolar PAL devices were essentially identical to first-generation designs but had the additional feature of programmable output polarity. Other architectural revisions include XOR outputs, power-up reset and direct set and clear for registered outputs, and selectable direct or program controlled clocking of registers. However, another segment of the second-generation bipolar PALs is composed of more complex versions of first-generation architectures. The MMI MegaPAL devices are examples of this category. The AMD PAL22V10 is another bipolar PAL with expanded architecture featuring macrocell output blocks for increased versatility. Another second-generation bipolar product soon to be available is an expanded PLA structure from Signetics which is to feature logic macrocells.

The most significant changes represented by second-generation PAL products is in the domain of CMOS fabricated devices. Devices in this category range from CMOS clones of first-generation MMI PALs (Sprague, Cypress, and Harris) to more versatile devices featuring output macrocell architectures. A very significant distinction of the second-generation CMOS PAL products is that almost all of them are erasable and reprogrammable. The pattern erasure is accomplished via exposure to ultraviolet light. Two manufacturers (Harris and National) have kept with programming via fusible links even though fabricating the device with a CMOS process. Other manufacturers of CMOS PAL devices have recently released devices with macrocell outputs (Panatech, VLSI Technology, and soon Atmel). One manufacturer (Lattice Semiconductor) has recently released PAL products which might be considered as being generation 2.5 since they are fabricated in CMOS, have an expanded architecture, and are electrically erasable

Third-generation PLDs represent even more significant advances in the state-of-the-art. In late 1985, Xilinx released an SRAM-based, reconfigurable logic cell array device. (LCA is a registered trademark of Xilinx.) This device features 64 user configurable logic blocks which provide a usable gate equivalency of 2000 NAND gates, and it includes 58 individually configurable I/O pins which allow any mixture of inputs, outputs or bi-directional signals. Moreover, input threshold levels are user selectable for either TTL or HCMOS compatibility. The logic circuit configuration is programmed via SRAM cells, and the desired pattern can

be load by any one of four configuration modes. Another distinction of this product is that the configuration pattern can be changed "on-the-fly" which opens up a host of possible applications.

Altera Corporation was the first manufacturer to release an erasable CMOS macrocell based programmable logic device. Intel serves as the foundry facility for Altera products and will also serve as a second source for Altera products; moreover, Intel plans to develop enhanced EPLD versions of the Altera designs. The Altera EP300, 600, 900, 1200, and 1800 devices can serve to implement logic circuit designs with 300 to 1800 equivalent gates, respectively. Exel Microelectronics recently released a PLD which is called an ERASIC (Electrically Reprogrammable Application Specific IC). A prime distinction of this device is that it employs a new array architecture called folding. This technique combines the AND and OR arrays into a single array wherein feedback lines from the output are attached to the inputs thus permitting implementation of multilevel logic. Inputs to the array can form product terms that can connect to the feedback lines thereby making the product terms inputs to the array. Any term can be assigned to a feedback line and product term sharing can be implemented. Nested logic can be implemented more efficiently with the use of this device.

Bipolar, fusible-link PLDs have a few limitations which are noted in the following list.

- o High power consumption, low tolerance to supply voltage variations, and low noise immunity. However, reduced power versions of bipolar PLDs are available from some manufacturers.

- o Relatively low level of circuit integration due to the fact that a large portion of the die area is taken up by the fuse structures.

- o One-Time-Programmable (OTP). This feature does not accommodate rework of programmed PLD inventory.

- o Bipolar fuses can only be destructively tested. Testing is usually done via sampling techniques on auxilliary test circuitry on the chip. One hundred percent testability and maximum silicon utilization cannot be achieved.

CMOS erasable programmable logic devices use EPROM cell technology to accommodate reprogramming. Additional CMOS EPLD benefits are listed below:

- o Low power consumption, wider tolerance to supply voltage variations and a high level of noise immunity.

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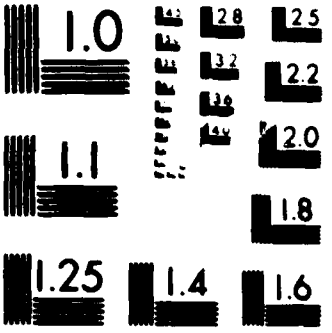

- o Higher logic circuit density since EPROM cells are significantly smaller than fuse elements.

- o Complete testability of product due to the erasability feature. Devices can be fully tested independent of specific applications. Bipolar PLDs require application-specific testing.

- o Architectural enhancements are feasible due to the possibility of one hundred percent testability. Many new circuit features can be added since full test coverage is possible.

- o Improved design security. Even though many bipolar PLDs provide a programmable security fuse, they can often be reverse-engineered via optical viewing of a programmed array; whereas, optical observation of a programmed EPLD does not reveal pattern specifics.

Advanced CMOS processes produce devices that can begin to compete with speeds of many bipolar products. Some CMOS PLDs have propagation delays of 35 nanoseconds or less. Reprogrammability results in no waste of devices with "blown" fuse patterns in the circuit development phase. The power consumption attribute of CMOS PLDs may not be lower than their bipolar architectural counterparts depending upon the frequency of operation. Published CMOS device power consumption data may not relate to device application switching rates. Some CMOS PLDs have a power-down mode to reduce power consumption when the device is not required to be accessed in a system application; however, the power-down mode may or may not be feasible depending upon the timing of the data path in which the PLD is placed. Another CMOS PLD which is due to be released towards the end of 1986 is a 5 volt only EEPLD.

Advances in PLD architectures and new logic cell types are significantly improving device flexibility. The most distinguishing feature of any PLD is the extent to which its architecture expands upon or deviates from the basic AND-OR programmable array structure. Deviations from established PLD architectures range from barely noticeable to dramatic. Some second-generation PLDs are merely a CMOS replacement of first-generation bipolar PALs; whereas, other new PLD architectures have versatile output macrocell structures. Besides distinctive output structures, some manufacturers are expanding the customization options for inputs and outputs as well as programmability of internal cells. The GAL (generic array logic) EEPLD from Lattice Semiconductor can replace any of eight earlier PAL versions. The registers in the output macrocells of Altera EPLDs can be configured as various types of flip-flops, and buried flip-flops can be implemented without losing the I/O association of a given flip-flop. Other manufacturers are also planning to release PLD products which can optionally implement buried flip-flops. Several new or planned PLDs are targeted at state machine applications for optimal state machine application performance.

Signetics is developing a bipolar PLD with folded-logic-plane architecture which will accommodate buried registers and flexible interconnects; in addition, this product is proposed to operate at 80 to 100 MHz.

5.2 PLD DESIGN AND PROGRAMMING SYSTEM OPTIONS

Programmable logic devices are programmed by using PROM programmers with PLD adapter modules or by using programming equipment which has been specifically designed to program PLDs. Perhaps the most widely used PLD programming equipment is that which is manufactured by Data I/O Corporation. Data I/O offers a dedicated PLD programmer as well as a selection of PROM programmers which accommodate PLD design and programming modules. The Data I/O PLD design system can be linked to a video terminal or to a host computer system such as an IBM-PC or DEC VAX system (IBM-PC and VAX are registered trademarks of International Business Machines and Digital Equipment Corporation, respectively).

PLD programmering equipment is divided into two major categories namely, hardware-based and software-based. The hardware-based equipment operates under self-contained firmware which contains device programming algorithms which are tailored to meet various manufacturer and device process and architectural requirements. Device programming patterns are downloaded to the programmer from a terminal or generated directly in an edit mode via programmer firmware utility control. Software-based device programmers operate via a link to a host computer system and the device-unique programming algorithms are retrieved from a database on the host computer and communicated to universal hardware pin drivers in a slave programming unit. The software-based device programming systems are inherently universal since a wide assortment of programmable device (PROM, PLA, and PAL inclusive) manufacturer-specific programming algorithms may be stored in the host computer system and be readily called upon to drive the universal pin electronics modules in the programming hardware unit. An additional advantage of the software-based, universal device programming systems is that they can be easily updated for a host of devices merely via transfer of new programming algorithms on portable data storage media.

A given logic circuit design is implemented in a PLD via a straightforward method. After selecting an appropriate PLD, the transfer functions are expressed in a sum-of-products set of Boolean equations. Next a design data file is created via a PLD development system. This file may be generated on a computer or directly on a development system in edit mode. The design specification data file is then processed by an assembler program such as PALASM to produce a fuse map data file in a format which is compatible with the selected device programming equipment. The fuse map file is then downloaded to the programming unit RAM and then, in turn, downloaded to the PLD.

Several versions of PLD assembler programs are available from various manufacturers of PLDs. Representative of these programs are: PALASM (registered trademark) by MMI, AMPALASM20 by AMD, PLAN (registered trademark) by National Semiconductor, and AMAZE by Signetics. AMAZE is a very flexible, user-friendly FPLA development software package and includes utilities to implement several standard PAL device architectures into Signetics FPLA devices. Third-party, more comprehensive PLD software packages are represented by ABEL (Advanced Boolean Expression Language, a registered trademark of Data I/O Corporation) and CUPL (Universal Compiler for Programmable Logic, a registered trademark of Assisted Technology Division of Personal CAD Systems). These software products include higher level entry modes such as state diagrams and function tables in addition to accepting Boolean equations. Some development software packages include logic minimization and even schematic-level data entry.

Various other manufacturers also offer an array of PLD programming equipment and PLD development systems and software. The current trend is for manufacturers of standard PLDs to either make their designs compatible with existing PLD development software or to generate software to accommodate the implementation of their devices and make it available to the device users under various arrangements. Manufacturers of PLDs with radically new architectures, such as Altera and Xilinx offer development and programming systems which are uniquely tailored to their PLD products. Xilinx has gone one step further in making available the first PLD in-circuit emulator system on the market. In some cases, fuse map assembly software may be available to device customers via a very economical arrangement. Comprehensive PLD development software packages are also available from some device manufacturers, device programmer manufacturers, and from third-party software developers. Comprehensive development software packages, with multiple design utilities, will of course cost more than edit/assemble PLD software.

5.3 SUMMARY OF PLD REVIEW

The preceding programmable logic device overview has presented a review of PLD history, process technology, and architecture. PLD fabrication process technology and architectural enhancements are yielding devices with speed enhancements, lower power consumption, higher circuit densities, erasability, reprogrammability, virtual 100 percent testability, and much greater circuit flexibility. First-generation PLDs are predominated by MMI bipolar SSI/MSI PALs, and many alternate sources are available. Second-generation PLDs are primarily UV erasable CMOS products some of which merely copy first-generation MMI bipolar PALs and others which have significant architectural enhancements. Other second-generation PLDs are speed enhanced bipolar versions of first-generation standard PALs. Yet other second-generation PLDs are significantly

larger sized versions of first-generation architectures. Third-generation PLDs are still very new on the scene but consist of products with radical architectural improvements which are primarily implemented via logic macrocell structures. The most distinctive of the third-generation PLDs is the SRAM-based reconfigurable logic cell array product from Xilinx.

An increasing selection of device architectures and manufacturers is available to the user of programmable logic devices. The PLD product market is in a growth mode with a wide selection of device processes and architectural options. Multiple sourcing of PLD products should not be a problem except for perhaps the most radical designs until their viability is established. The increased circuit density and architectural complexity of PLDs should serve to move them towards more use in filling the gap between standard SSI and MSI logic and gate arrays. In some cases, PLDs could be used to replace smaller sized gate arrays.

The low development, rapid design cycle, and rapid design revision cycle continue to be main advantages of using PLD products. Programmable logic device design, development, and programming systems are also in a growth mode. More systems are becoming available with improved features and at moderate cost. Many of these systems are offered as subsystems to be used in conjunction with small computer systems (such as the IBM-PC) which are already available to many current and potential PLD users.

At the time of this report, military version PLD products were available from the following manufacturers: Advanced Micro Devices Incorporated, Cypress Semiconductor Corporation, Fairchild Semiconductor Corporation, Harris Corporation, Lattice Semiconductor Corporation, Monolithic Memories Incorporated, National Semiconductor Corporation, Signetics Corporation, Texas Instruments Incorporated, and Xilinx.

6. CONCLUSIONS

This report has summarized the programmable logic project work done under the RADC contract and has additionally presented an overview of application-specific integrated circuit devices with a primary emphasis upon programmable logic devices. In regard to the contract activity, the MMI PAL32R16 "MegaPAL" was selected for evaluation under the contract following two manufacturer and literature surveys for a high-density, state-of-the-art PLD. Due to continued delays in the availability of military-grade samples of the PAL32R16, and due to the interest expressed by RADC to incorporate an evaluation of a 512K UVEPROM into the contract activity, the PAL32R16 project was terminated and replaced by an evaluation of the 27512 EPROM. In retrospect, the AMD PAL22V10 may have been a better selection for the PLD evaluation project. This device is still on the market, is available in military-grade version, is alternately sourced, and other manufacturers are planning to produce the PAL22V10. The FPLA products identified in the early selection process were not considered to have potentially as wide an acceptance as did the PAL products and were, therefore, not selected.

Programmable logic device products are very much in a growth mode at the present time, and market projections indicate that they will take an increasing portion of the total ASIC market in the next few years. Programmable logic devices have been on the market for several years with the first such devices being structured as FPLAs. In the past two years, PLD products, primarily of PAL basic structure, have multiplied very significantly. Many new PLD manufacturers have emerged and their products range from drop-in replacements for first-generation bipolar MMI PALs to architecturally complex erasable and reconfigurable third-generation PLD components. Advances in the quality and availability of programmable logic device programming and development systems and software have also recently taken place. The user of programmable logic devices now has a wide selection of device processes and architectures from which to choose as well as a selection of programming and development system components. The implementation of PLDs in logic circuit applications can serve to reduce overall product development time and cost while increasing the efficiency of final product size and cost.

Further details on programmable logic devices and their associated design and programming systems may be found by reviewing the publications listed in the bibliography of this report.

7. GLOSSARY

Glossary of Acronyms and Trademarks

ABEL	Advanced Boolean Expression Language (Registered trademark of Data I/O Corporation)
AMAZE	Automatic Map and Zap Equations (Registered trademark of Signetics Corporation)
AMD	Advanced Micro Devices Incorporated
ASIC	Application Specific Integrated Circuit
ATE	Automatic Test Equipment
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CUPL	Universal Compiler for Programmable Logic (Registered trademark of Assisted Technology Division of Personal CAD Systems)
Data I/O	Data I/O Corporation
DEC	Digital Equipment Corporation (Registered trademark)
ECL	Emitter Coupled Logic
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory
ERASIC	Electrically Reprogrammable Application Specific Integrated Circuit (Registered trademark of Exel Microelectronics)
FPLA	Field Programmable Logic Array
FPLS	Field Programmable Logic Sequencer
FSC	Fairchild Semiconductor Corporation
GaAs	Gallium Arsenide

GAL	Generic Array Logic (Registered trademark of Lattice Semiconductor Corporation)
GTE	GTE Corporation
HCMOS	High-speed Complementary Metal Oxide Semiconductor
IBM	International Business Machines Corporation (Registered trademark)
IBM-PC	International Business Machines Personal Computer (Registered trademark)
IC	Integrated Circuit
I/O	Input/Output
JEDEC	Joint Electron Device Engineering Council
LCA	Logic Cell Array (Registered trademark of Xilinx)
LogicPak	PLD interface unit for Data I/O universal device programmer (Registered trademark of Data I/O Corporation)
LSI	Large Scale Integration
MegaPAL	Second-generation bipolar PAL series from MMI (Registered trademark of Monolithic Memories Incorporated)
MMI	Monolithic Memories Incorporated
MSI	Medium Scale Integration
NRE	Non-Recurring Engineering (cost)
NSC	National Semiconductor Corporation
PAL	Programmable Array Logic (Registered trademark of MMI)
PALASM	Programmable Array Logic ASseMbler (Registered trademark of Monolithic Memories Incorporated)
PLA	Programmable Logic Array
PLAN	Programmable Logic Analysis by National (Registered trademark of National Semiconductor Corporation)

PLD	Programmable Logic Device
PLDS	Programmable Logic Development System
PLE	Programmable Logic Element (Registered trademark of Monolithic Memories Incorporated)
PROM	Programmable Read Only Memory
RADC	Rome Air Development Center
RAM	Random Access Memory
Signetics	Signetics Corporation
SRAM	Static Random Access Memory
SSI	Small Scale Integration
TI	Texas Instruments Incorporated
TTL	Transistor Transistor Logic
UVEPROM	Ultraviolet Erasable Programmable Read Only Memory
VAX	Virtual Address Extension (Registered trademark of Digital Equipment Corporation)
VLSI	Very Large Scale Integration

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