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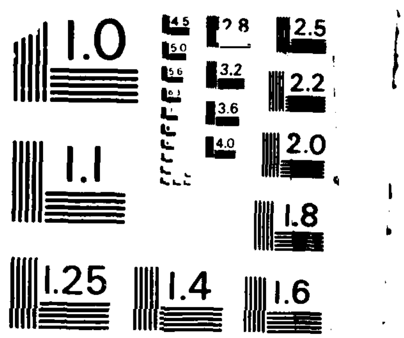

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AD-A176 857

Single Event Upset Rate Estimates for a 16-K CMOS SRAM

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30 September 1986

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This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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A radiation-hardened 16K CMOS SRAM has been developed for satellite and deep space applications. The RAM memory cell was modeled to predict the critical charge, necessary for single-particle upset, as a function of temperature, total dose, and hardening feedback resistance. Laboratory measurements of the single event cross section and effective funnel length were made using the Lawrence Berkeley Laboratory's 88-inch cyclotron to generate high energy krypton ions. The combination of modeled and measured parameters permitted estimation of the upset rate for the RAM cell, and the mean-time-to-failure for a 512-K word, 22-bit memory system employing error detection and correction circuits while functioning in the Adam's "90% worst case" cosmic ray environment. This report is presented in the form of a worst tutorial review, summarizing the results of substantial research efforts within the single event community.

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PREFACE

The authors gratefully acknowledge the contributions of R. V. Jones and R. K. Treece of Sandia National Laboratories, Albuquerque, New Mexico.

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I. INTRODUCTION

At the present time, it is generally accepted that single-particle upset is a potential threat to the reliable operation of memory systems.[1] The resistive decoupling in RAM cells, while ultimately limited to applications where the current pulse corresponding to a legitimate RAM cell state change is longer than current pulse widths from cosmic ray interactions, remains a useful hardening technique at current levels of integration for memory circuits used in satellite and deep space applications. The work described here is a combination of experimental and analytical techniques used to evaluate the reliability of an idealized 512-K word memory system composed of 16 K by 1-bit static radiation hardened RAMs, functioning in the Adam's "90% worst case" cosmic ray environment.

II. INTEGRATED CIRCUIT DESCRIPTION

The single event upset (SEU) data presented in this report was measured for the SA3240 complementary metal oxide semiconductor (CMOS) integrated circuit. The SA3240 is a 16-K static random access memory (RAM) organized as 16 K by 1 bit. The memory is fabricated in hardened, bulk on epitaxial substrate, silicon gate technology, 2-micron 5-V process. The standard six transistor RAM cell is utilized. The resistive decoupling method is used to achieve SEU hardness. The SA3240 has demonstrated latch-up immunity, total-dose hardness to a level of 10^6 rad(Si), and dose rate hardness to a level in excess of 5×10^8 rad(Si)/s.

III. RAM CELL CRITICAL CHARGE ESTIMATE

Transient circuit analysis was performed to determine the critical charge required to upset the RAM cell as a function of feedback resistance.* The devices and RAM cell circuit were simulated using the SPICE computer program. The cosmic ray interaction was simulated by applying a current pulse from generators placed in parallel with the sensitive device junctions. The current pulse amplitude was varied to find the threshold for memory changes. The critical charge was then determined by calculating the time integral of the minimum current pulse that caused upset. A plot of critical charge (Q_C) versus feedback resistance (R_F) under normal and worse-case operating conditions is shown in Fig. 1. The percent change in critical charge due to biasing (V ~ 16%), temperature (T ~ 7%) and radiation (R ~ 3%) is also shown. The critical charge is assumed equal for either p-channel or n-channel transistor drain hits. The critical charge estimates are provided courtesy of the Center for Radiation Hardened Microelectronics, Sandia National Laboratories.

*T. M. Mnich, B. D. Shafer, and S. E. Diehl, "Comparison of Analytical Models and Experimental Results for Single Event Upset in CMOS SRAMS," unpublished manuscript, 1984.

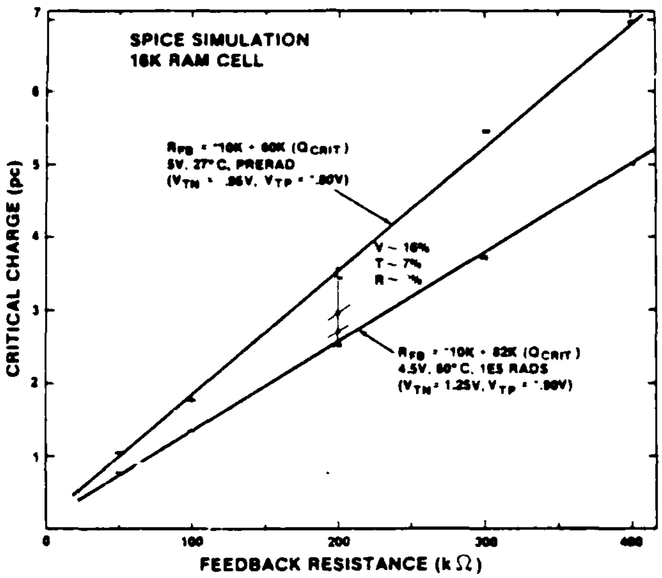

Fig. 1. Critical Charge, SA3240 RAM Cell

IV. FUNNELING CONSIDERATIONS

Seven de-lidded SA3240 SRAMS were tested for latch-up and SEU in a 140-MeV krypton beam, at the Lawrence Berkeley Laboratory's 88-inch cyclotron facility. The test hardware is documented in Reference 2. These tests were designed to simulate a worse-case cosmic ray environment encountered by memory system on space vehicles. All seven devices were found to be immune to heavy ion induced latch-up. The test data and the SEU cross section are shown in Table I. The cross section was calculated using the expression

$$\sigma = AE/[N \cos(\theta)] \tag{1}$$

where A is the area of the beam monitor, E is the number of errors detected, N is the number of monitor counts, and θ is the angle between the beam direction and the normal to the integrated circuit die. The monitor area was 1.8 cm^2. The cross section increased sharply with beam angle, reaching a peak value around 60°. The peak value is in fair agreement with the sum of the p-channel drain areas, shown in Fig. 2.

An estimate for the effective funnel length was obtained by interpreting the experimental results. It was assumed that the krypton ion penetrated the p-channel drain junction at the angle θ with respect to the normal to the surface, resulting in a path length through the p-channel depletion region of 1.27 μm/cos θ. The linear energy transfer (LET) of the ion was assumed to be constant over the region of interest. The deposited charge is then

$$Q_D = \frac{(1.27 \times 10^{-4}\,\mathrm{cm})(\mathrm{LET})(\rho)}{(22.5)(\cos\theta)} \tag{2}$$

Table I. SA3240 Single Event Upset Test, 140-MeV Krypton, 9/18/84

Serial No.	Bias V	Beam Angle (°)	Counts (per 1.8 cm^2)	Errors 1-0	Errors 0-1	Cross Section (cm^2)
200	5	70	1,010,674	145	121	1.39×10^{-3}
(83 kΩ)		70	493,793	180	171	2.56×10^{-3}
		45	502,782	102	111	1.08×10^{-3}
		30	1,002,256	35	31	1.37×10^{-4}
		0	569,997	1	0	3.16×10^{-6}
		0	2,997,563	1	1	1.20×10^{-6}
197	5	70	672,122	117	134	1.97×10^{-3}
(83 kΩ)		60	503,024	182	200	2.73×10^{-3}
		45	499,309	157	153	1.58×10^{-3}
		30	1,002,428	44	71	2.38×10^{-4}
		30	500,977	28	42	2.90×10^{-4}
		0	1,000,831	0	0	$<1.80 \times 10^{-6}$
155	5	60	1,000,638	4	4	4.21×10^{-5}
(160 kΩ)		60	501,594	6	10	1.15×10^{-4}
		45	501,843	0	0	$<5.07 \times 10^{-6}$
4.5	4.5	70	502,459	56	46	1.07×10^{-3}
		60	503,054	112	103	1.54×10^{-3}
		45	501,156	121	134	1.40×10^{-3}
		30	501,649	25	33	2.40×10^{-4}
		0	501,626	1	1	7.18×10^{-6}
157	5	70	1,002,918	18	16	1.78×10^{-4}
(160 kΩ)						
126	5	70	3,000,727	0	0	$<1.05 \times 10^{-6}$
(250 kΩ)	4.5	70	4,999,323	0	0	$<1.05 \times 10^{-6}$
127	5	70	5,030,437	0	0	$<1.05 \times 10^{-6}$
(250 kΩ)	4.5	70	5,002,373	1	2	3.16×10^{-6}
128	4.5	70	1,009,036	0	0	$<5.22 \times 10^{-6}$
(220 kΩ)						

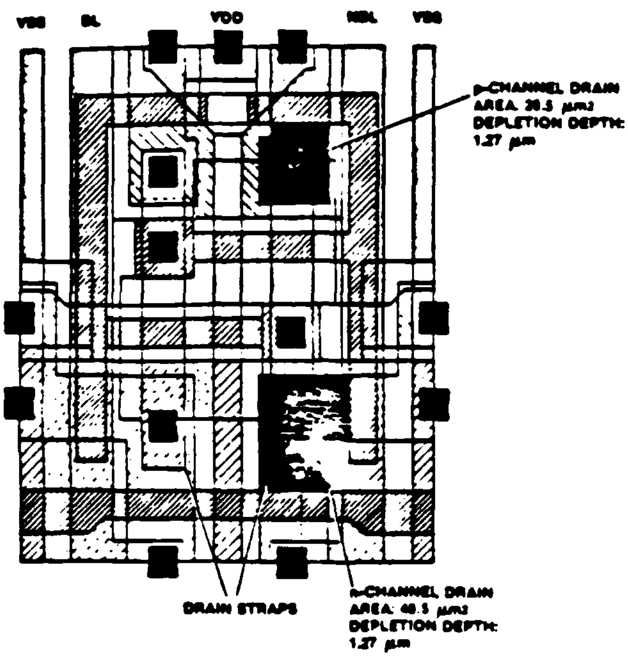

Fig. 2. Sensitive Volumes for 16 K by 1 bit CMOS SRAM Memory Cell

where Q_D is in pC, LET - 4×10^4 is in MeV-cm^2/g, and ρ is the density of silicon in g/cm^3. The cross section versus charge deposited in the p-channel transistor drain is shown in Fig. 3. To take into consideration the observed variation in sensitivity to SEU of the RAM cells, a conservative estimate of 0.56 pC for the upset threshold was selected. At this value, 90% of the RAM cells do not upset.

The charge collected due to the funneling mechanism was obtained by subtracting 0.56 pC from the critical charge required to upset the RAM cell with a decoupling resistance of 83 KΩ. From the charge collected due to funneling, an effective funnel length of 1.46 μm was obtained. This estimate for the funnel length depends upon the experimentation cross section and the validity of the SPICE simulation of the critical charge.

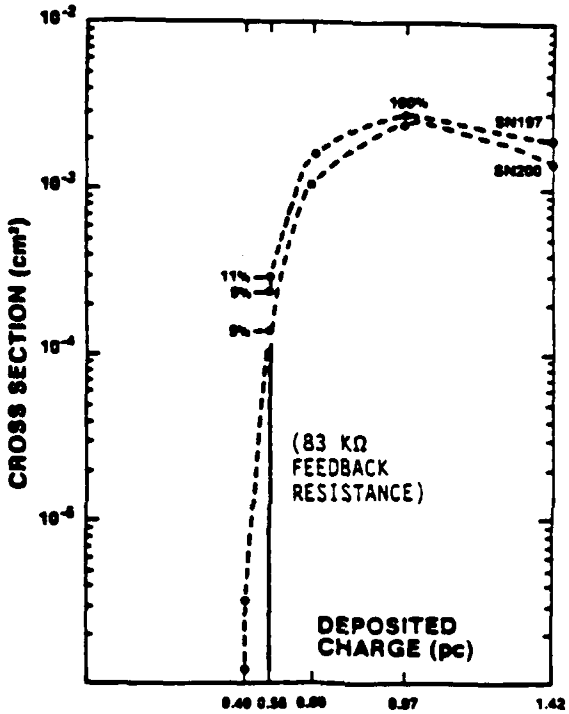

Fig. 3. Cross Section, SA3240 RAM Cell

V. COSMIC RAY INDUCED ERROR RATE CALCULATION

The error rates used in the cosmic ray interaction analysis described in the remainder of this report were calculated using the CRUP computer code[3] modified for funneling. The CRUP code requires, as inputs, the size of a depletion region specified as a retangular parallel piped with dimensions $a \leq b \leq c$, the effective funnel length, the critical charge, and the cosmic ray environment specified as a different LET spectra. The Adam's 90% "worst case" spectra were used for the calculations.[4]

In the CRUP code, the error rate is calculated as

$$\lambda = \frac{A}{4} \int_{LET_{min}}^{LET_{max}} \phi(LET) C(S_{min}) d(LET) \tag{3}$$

where $A = 2\ (ab + ac + bc)$ is the total surface area of the depletion region, ϕ (LET) is the differential LET spectrum with a maximum LET of LET_{max}, $C(S_{min})$ is the probability of a particle traversing the sensitive volume with a chord length greater than S_{min}, and S_{min} is derived from the critical charge as

$$S_{min} = \frac{22.5_{Qc}}{\rho LET} \tag{4}$$

The minimum value of LET that will produce an upset, LET_{min}, is given by

$$LET_{min} = \frac{22.5_{Qc}}{\rho S_{max}} \tag{5}$$

where $S_{max} = (a^2 + b^2 + c^2)^{1/2}$.

To accommodate funneling the chord length distribution, $C(S_{min})$, is shifted by the funnel length where appropriate. A constant funnel length is assumed. Based upon the analytical model of McLean and Oldham,[5] which predicts that the funnel length continuously increases with LET, the use of the effective funnel length for krypton ions should overestimate the charge collected for lower LET ions. Therefore, the error rate calculations presented below are conservative.

Table II shows the p- and n-channel error rates calculated for several values of decoupling resistance. The overall error rate is obtained by summing the error rates for all sensitive devices in the RAM cell. The error rate versus feedback resistance is shown in Fig. 4.

Table II. Crup Simulation, Adam's 90% Worst Case, 16 K RAM Cell

FEEDBACK RESISTANCE (kΩ)	Q_{CRIT} (pC)	P-CHANNEL ERRORS/BIT-DAY	N-CHANNEL ERRORS/BIT-DAY
50	0.73** 1.00*	4.25×10^{-8} 1.19×10^{-8}	8.72×10^{-9} 3.03×10^{-9}
100	1.34 1.83	3.26×10^{-9} 4.9×10^{-10}	1.6×10^{-9} 3.34×10^{-10}
200	2.56 3.50	2.66×10^{-13} -0-	8.44×10^{-11} 1.39×10^{-12}
300	3.78 5.17	-0- -0-	-0- -0-
350	4.39 6.00	-0- -0-	-0- -0-
400	5.00 6.83	-0- -0-	-0- -0-

*5 V, 27°, PRERAD.
**4.5 V, 60°, 1E5 RADS.

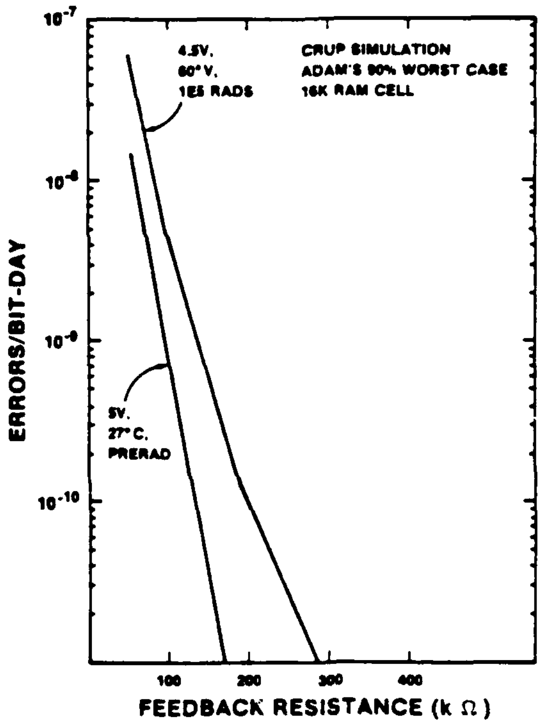

Fig. 4. Error Rate, SA3240 RAM Cell

VI. ERROR DETECTION AND CORRECTION LOGIC CONSIDERATIONS

In order to guard against errors caused by single event upsets, one may attempt to use an information code that facilitates error detection and correction by special logic circuits.[6] The general approach is to append parity bits to each word which are used to locate errors in the word. Figure 5 shows the structure of a general EDAC scheme.

If an information code possesses the property that the occurrence of 1, 2, 3, ..., or d errors transforms a valid code word into an invalid code word, it is said to be a d-error-detecting code. The minimum distance, M, of a code is the smallest number of bits in which any two code words, $A = \{a_k | k = 1, \ldots, n\}$ and $B = \{b_k | k = 1, \ldots, n\}$, differ:

$$M = \sum_{i=o}^{n} (a_i \oplus b_i) \; A,B \tag{6}$$

where the symbol $\oplus$ represents sum mod 2, and the summation is an arithmetic sum. A code is a d-error-correcting code if and only if $M - 1 = d$.

The d-error-detecting code is a special case of the d-error-detecting and c-error-correcting code which obeys the general relation

$$M - 1 = c + d \qquad c \leq d \tag{7}$$

where c is the number of errors which can always be corrected, and d is the number of errors which can always be detected. The condition $c \leq d$ is imposed because it is not possible to correct more errors than can be detected. Note that for a specified M, various combinations of c and d will satisfy the general relation. Note also that if more errors occur than the code is capable of detecting, an invalid code word may result if correction is performed.

Either error-detection or error-correction may be used for protection against soft errors. Error detection requires retransmission of information or redundant information storage, while error correction permits restoration of invalid code words.

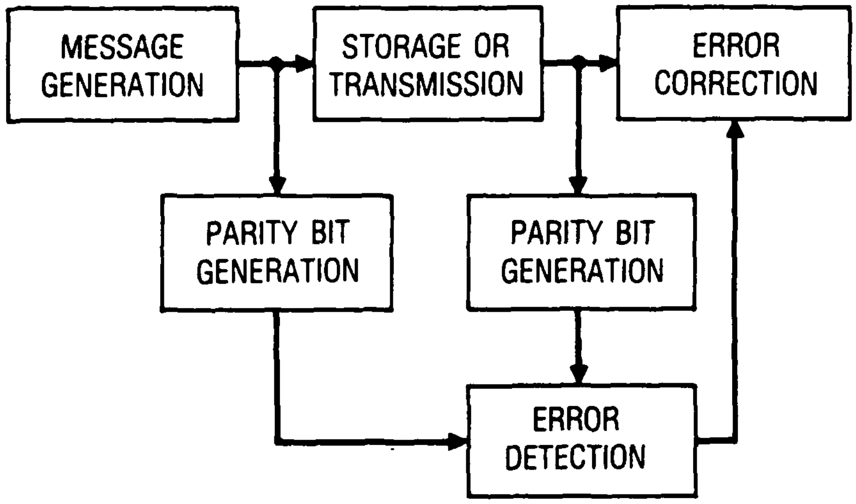

Fig. 5. General Error Detection and Correction Time

Any desired level of protection against soft errors can be obtained by satisfying two separate conditions: the code must have the minimum distance specified by inequality, and sufficient parity bits must be appended to encode all error conditions and the error-free condition. An error can occur in any of the $n = i + p$ bits (information plus parity bits). The parity bits must then either specify that no error has occurred or locate the 1,2,3,..., or d errors. The p parity bits can represent 2^p different conditions. Therefore, a necessary condition for EDAC to succeed is that the following inequality be satisfied.

$$2^p \geq \sum_{k=o}^{d} \binom{n}{k} \tag{8}$$

where $\binom{n}{k}$ denotes the number of combinations of k errors in bits.

VII. DEVELOPMENT OF STATISTICAL RELIABILITY MODEL

From the upset rate described above, a probability of upset of a single bit may be obtained, and can then be used to estimate the reliability of a digital memory system[7] with error detection and correction (EDAC) circuits. If λ is a constant error rate, then the probability of upset after time Δt is

$$P_{1,1} = 1 - e^{-\lambda \Delta t} \tag{9}$$

Assuming that the probability $P_{1,1}$ is the same for each bit, and the occurrence of an error in a bit is independent of the occurrence of errors in any of the other bits, the probability of r errors in n bits is given by the binomial distribution

$$P_{r,n} = \binom{n}{r} P_{1,1}{}^{r} (1 - P_{1,1})^{n-r} \tag{10}$$

Initially, the code word is error free. After time Δt, the probability that the code word is correct is approximately

$$R_1(\Delta t) = 1 - P_{r,n} \qquad r = d + 1 \tag{11}$$

In this approximation higher order terms, which are usually insignificant, have been neglected. After N intervals of Δt, the probability that the code word is correct is

$$R_1(N\Delta t) = [1 - P_{r,n}]^N \tag{12}$$

Assuming independence of code words, the reliability of a system of W code words after time $N\Delta t$ is

$$R_W(N\Delta t) = [1 - P_{r,n}]^{NW} \tag{13}$$

The expected life of a system is referred to as a mean time before failure (MTBF), defined by the equation

$$\text{MTBF} = \int_{0}^{\infty} - t\,dR \tag{14}$$

where R is the reliability of the system. Noting that t = NΔt, then

$$R_W(N\Delta t) = \{[1 - P_{r,n}]^{\frac{W}{\Delta t}}\}^t \tag{15}$$

which when substituted into equation 14 yields the solution

$$\text{MTBF} = \frac{-\Delta t}{W \ln[1 - P_{r,n}]} \tag{16}$$

VIII. MEAN TIME BEFORE FAILURE ESTIMATES

Using the statistical mode developed above, a set of MTBF calculations was performed for an idealized memory system of 524288 words of 16 information bits with and without error detection or correction, and up to protection against 3 errors per word. The worst-case operating conditions were assumed. The results of these calculations are shown in Table III.

If a system lifetime of 15 years is desired, then it is probably reasonable to require a MTBF of 150 years, or 5.5×10^4 days. For each assumed error rate, the table entries that satisfy the 150-year requirement are separated from those that do not by a line drawn between the table entries.

As can be seen from Table III, the 300-k Ω decoupling resistance without error detection and correction will probably provide adequate SEU hardness for the memory system. However, 100-k Ω decoupling resistance with either single-error-detection or single-error detection and single error-correction will satisfy the 150-year MTBF requirement.

Table III. MTBF (Day) for a 52488 Work Memory System, Adam's 90% "Worst Case" Cosmic Ray Environment

λ (Errors/Bit-day)	n (Bits)	d/c (Errors)	Δt (Day) 2.6 × 10^3	3.7 × 10^2	30.0	1.00	0.42	6.9 × 10^-3
10^{-4}	16	0/0	0.12	0.12	0.12	0.12	0.12	0.12
(~0 Ω)	17	1/0	5.7	39.0	4.7×10^{2}	1.4×10^{4}	3.4×10^{5}	1.9×10^{7}
	21	1/1	3.7	25.0	3.0×10^{2}	9.1×10^{2}	2.2×10^{5}	1.4×10^{7}
	21	2/0	2.3×10^{2}	1.1×10^{4}	1.6×10^{6}	1.4×10^{9}	---	---
	22	2/1	2.0×10^{2}	9.4×10^{3}	1.4×10^{6}	1.2×10^{9}	---	---
	22	3/0	1.6×10^{4}	5.4×10^{7}	9.7×10^{9}	---	---	---
10^{-7}	16	0/0	1.2	1.2	1.2	1.2	1.2	1.2
(~50 kΩ)	17	1/0	5.5×10^{2}	3.8×10	4.7×10^{6}	1.4×10^{6}	3.4×10^{7}	---
	21	1/1	3.6×10^{2}	2.5×10^{3}	3.0×10^{4}	9.1×10^{5}	2.2×10^{7}	---
	21	2/0	2.2×10^{5}	1.1×10^{7}	1.6×10^{9}	---	---	---
	22	2/1	1.9×10^{5}	9.3×10^{7}	1.4×10^{9}	---	---	---
	22	3/0	1.6×10^{9}	5.4×10^{11}	---	---	---	---
10^{-8}	16	0/0	12.0	12.0	12.0	12.0	12.0	12.0
(~100 kΩ)	17	1/0	5.5×10^{4}	3.8×10^{5}	4.7×10^{6}	1.4×10^{8}	2.9×10^{9}	---
	21	1/1	3.6×10^{4}	2.5×10^{5}	3.0×10^{6}	9.1×10^{7}	1.9×10^{9}	---
	21	2/0	2.2×10^{8}	1.1×10^{10}	1.4×10^{12}	---	---	---
	22	2/1	1.9×10^{8}	9.3×10^{9}	1.4×10^{12}	---	---	---
	22	3/0	1.6×10^{12}	---	---	---	---	---
10^{-9}	16	0/0	1.2×10^{2}	1.2×10^{2}	1.2×10^{2}	1.2×10^{2}	1.2×10^{2}	1.2×10^{2}
(~150 kΩ)	17	1/0	5.5×10^{6}	3.8×10^{7}	4.7×10^{8}	1.4×10^{10}	---	---
	21	1/1	3.6×10^{6}	2.5×10^{7}	3.0×10^{8}	9.2×10^{9}	---	---
	21	2/0	2.2×10^{11}	1.0×10^{13}	---	---	---	---
	22	2/1	1.9×10^{11}	1.0×10^{13}	---	---	---	---
10^{-10}	16	0/0	1.2×10^{3}	1.2×10^{3}	1.2×10^{3}	1.2×10^{3}	1.2×10^{3}	1.2×10^{3}
(~200 kΩ)	17	1/0	5.5×10^{8}	3.8×10^{9}	4.7×10^{10}	---	---	---
	21	1/1	3.6×10^{8}	2.5×10^{9}	3.0×10^{10}	---	---	---
	21	2/0	1.8×10^{14}	---	---	---	---	---
	22	2/1	1.8×10^{14}	---	---	---	---	---
10^{-11}	16	0/0	1.2×10^{4}	1.2×10^{4}	1.2×10^{4}	1.2×10^{4}	1.2×10^{4}	1.2×10^{4}
(< 300 kΩ)	17	1/0	5.5×10^{10}	3.8×10^{11}	---	---	---	---
	21	1/1	3.6×10^{10}	2.5×10^{11}	4.1×10^{12}	---	---	---

IX. CONCLUSIONS

In this report, a combination of experimental and analytical techniques was used to estimate the upset rate for a 16-K by 1-bit CMOS SRAM memory cell, and the MTBF for a 512-K word, 16-information bit memory system functioning in the Adam's "90% worst case" cosmic ray environment. Although the MTBF was estimated for an idealized memory system, the engineer will recognize the trade-off between employing the resistive decoupling technique in the ramcells or EDAC logic circuits to achieve the required MTBF.

The SEU susceptibility of the unhardened 16-K SRAM may be such that EDAC alone cannot provide an adequate MTBF. The required MTBF can be obtained by combining EDAC with the resistive decoupling technique, or by selecting a sufficiently large feedback resistance.

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