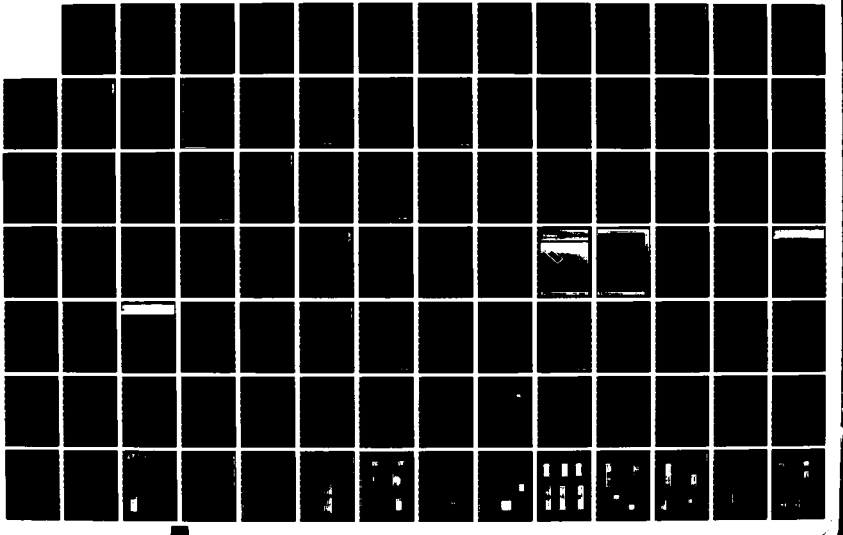
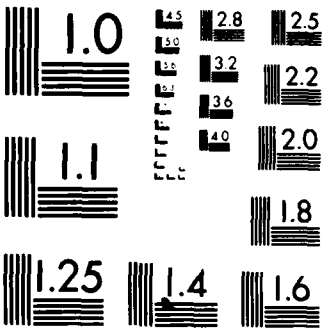
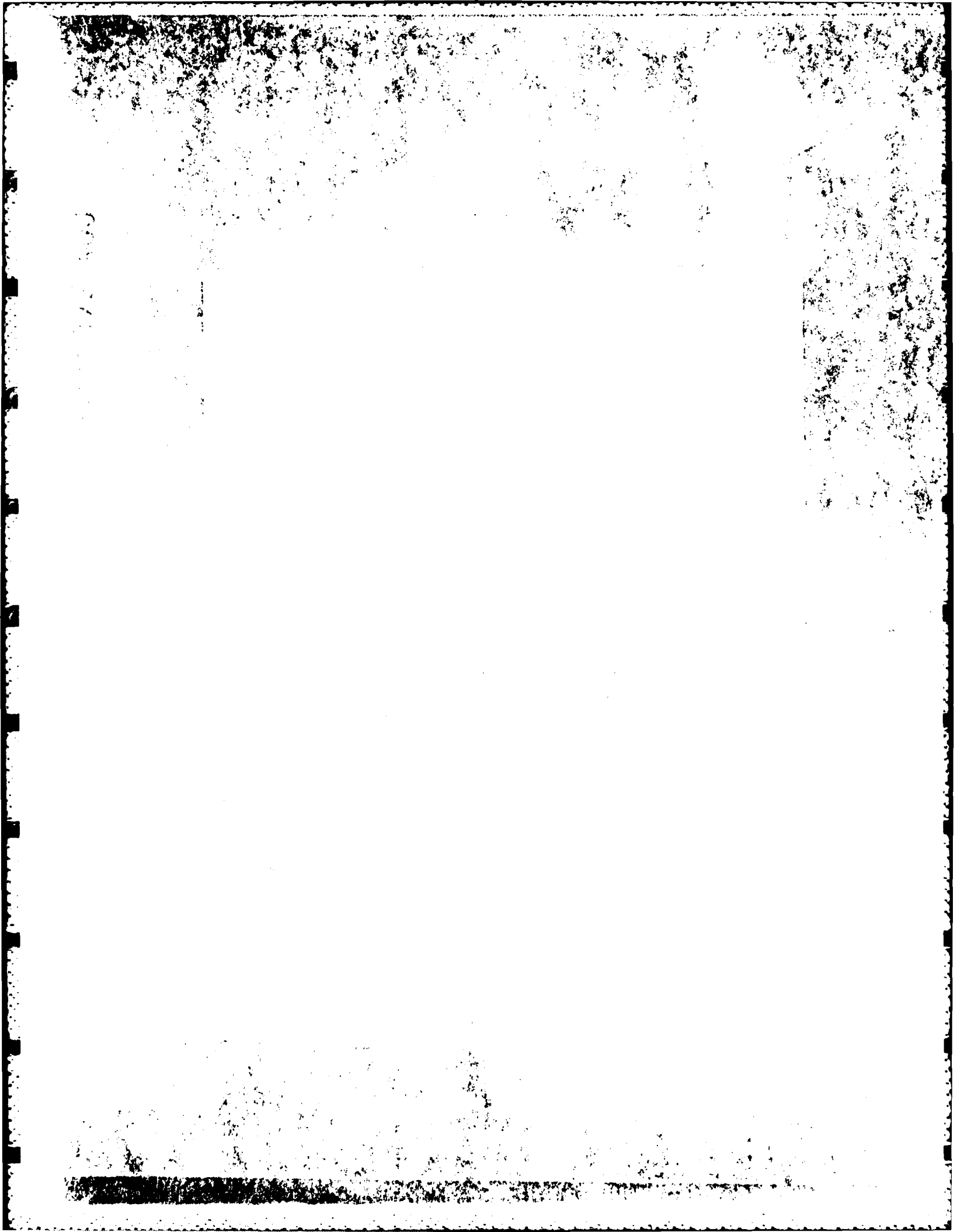
AD-A172 400 SMALL SELF-CONTAINED AIRCRAFT FATIGUE DATA RECORDER(U) 1/2
ESPIRT TECHNOLOGY INC WALNUT CREEK CA P FLANNER AUG 86
N62269-85-C-0716
UNCLASSIFIED F/G 20/11 NL







FINAL REPORT

"Small, Self-Contained Aircraft Fatique Data Recorder"

Contract No.: N62269-85-C-0716

10/85 - 08/86

DEFENSE SMALL BUSINESS INNOVATION RESEARCH (SBIR) PROGRAM FINAL REPORT

Title: **Aircraft Fatigue Recorder**
Phase I Effort – FY 1985 SBIR, Topic #127

Sponsor: Naval Air Development Center, Warminster, PA

Contract No: N62269-85-C-0716

Contractor: **ESPRIT Technology Inc.**
144-A Mayhew Way
Walnut Creek, CA 94596

Principal Investigator: Philip Flanner, Engineering Manager

August, 1986

Reporting Period: 10/85-8/86
Contract Type: Competitive
Contract Amount: $49,884
Sponsor: A. Negri
Naval Air Development Center
Code 6042, Warminster, PA 18974-5000

DEFENSE SMALL BUSINESS INNOVATION RESEARCH (SBIR) PROGRAM
FINAL REPORT

Title: **Aircraft Fatigue Recorder**
Phase I Effort – FY 1985 SBIR, Topic #127

Sponsor: Naval Air Development Center, Warminster, PA

Contract No: N62269-85-C-0716

Contractor: **ESPRIT Technology Inc.**
144-A Mayhew Way
Walnut Creek, CA 94596

Principal Investigator: Philip Flanner, Engineering Manager

Summary – Because of aging airframes and more severe mission requirements, the need to monitor structural fatigue damage on military aircraft has become critical. It is particularly important to be able to study the dynamic loads in remote locations such as the vertical tail, wing spar, landing gear, etc. However, there is presently no small, battery-operated data recorder available to investigate fatigue characteristics at these localized stress "hot spots." Having available a miniature data-logger that could be easily attached to any desired location on an aircraft will enable engineers to quickly examine, and correct, the cause of fatigue cracks and similar structural problems.

The purpose of this program was to investigate the feasibility of utilizing the latest technology in low-power circuitry, transducers and packaging to produce a small, rugged, self-contained fatigue recorder, requiring no tie-in to aircraft wiring for installation.

The project stages included: feasibility study, design evaluation, submittal of an interim report, and culminated in the design layout and construction of a brassboard demonstration unit. This feasibility demonstrator is a single channel device connected to an internal accelerometer and includes a means for automatically activating the micro-processor circuitry by sensing the vibration associated with the start-up and operation of the aircraft's engines. Size of the ultimate unit is targeted at 8 cubic inches, and the demonstrator is approximately three times this volume because of using discrete devices rather than hybrids or SMD's.

The design objectives, as achieved on the brassboard unit, and as projected for the Phase II design, may be summarized as follows:

OBJECTIVE	BRASSBOARD PERFORMANCE	PROJECTED FOR FINAL UNIT
Size	22 cu. in.	8 cu. in.
No. of channels	one	two
Bandwidth	16 Hz	50 Hz
Duration of self-power	5 days (est.)	30 days
Auto. turn-on circuit	demonstrated	achievable
programmable range	demonstrated	achievable
programmable offset	demonstrated	achievable
programmable bandwidth	demonstrated	achievable
programmable Algorithms	demonstrated (one)	achievable
Real-time clock	not included	achievable

It is concluded that the success of this feasibility study justifies a follow-on effort to develop a final design featuring hybrid or SMD packaging, and the delivery of 3 units for lab evaluation and flight test by the Navy.

A miniature, easily-installed, battery-operated structural recorder will also be extremely valuable for use on commercial aircraft, buildings, bridges, earthquake monitors and oil platforms.

TABLE OF CONTENTS

1.0 INTRODUCTION

1.1 Identification and Significance of Phase I Effort

There is a steadily increasing need to monitor and record the fatigue life consumption of aircraft structural members. With the adoption of Service Life Extension Programs to extend the life of older airframes and with changes in mission and loading from the original design criteria, aircraft are being subjected to fatigue environments far greater than were originally planned. Additionally, for newer aircraft, the advent of special-purpose alloys, the incorporation of sophisticated but stressful automatic flight control systems, and the narrowing of structural design margins, all serve to heighten concerns over the accumulation of fatigue damage.

Accordingly, there is a requirement for a fatigue data recorder readily installed on various structural locations in military aircraft to measure and store data on the number of times that various flight dynamic loads have been exceeded. In the past these measurements were accomplished either by a specially-instrumented test aircraft using a large on-board tape recorder, or by the existing Counting Accelerometer system installed at the C.G. and totalizing four levels of vertical acceleration data. In the former case, the instrumentation task is bulky, expensive and time consuming; and in the latter case, the data is very limited in scope and has no flexibility as regards location on the aircraft.

Technology now exists for the mechanization of microprocessor based data recorders featuring solid-state memory and electronic data retrieval.

The results of the Phase I effort have confirmed that a fatigue data recorder can be developed which is small, self-contained, easily installed, self-powered to store up to one month of flight data, and designed for mounting in a variety of critical locations on an aircraft.

The basic concept behind the device demonstrated in Phase I is to solve structural problems and these problems could be anywhere on the aircraft -- wing, empennage, tail, landing gear, etc. The resultant production instrument will be able to be readily attached to any structural member, either internally or on the skin, and flown operationally for up to one month to assess the type of loads that the structural member normally experiences. The recorder would then be removed and the accumulated fatigue data read-out on a simple desk-top computer. The entire procedure will feature simplicity, ease of installation, and versatility of investigative parameters. It will be a major advancement to help structural engineers solve critical fatigue problems, not only on military aircraft, but on commercial airlines, buildings, bridges, and all safety-conscious structures.

1.2 Technical Objectives - Phase I

The ultimate goal of this three-phase program is the production of a small (1" x 2" x 4" typical) self-powered data recording system comprising transducers and electronics to monitor physical parameters (acceleration, strain, pressure, temperature) of interest to fatigue monitoring programs. The recorder combines transducers, CMOS circuitry and software for low power operation. The measurement ranges, data compression schemes, and data variation exclusion levels will be under software control and can be set by the user. The data will be recorded in solid state memory and retrieved by removing the recorder from the aircraft and mating it with a data Transcriber, thereby transferring the data from the recorder to a suitable medium (e.g. disk) in the Transcriber. The Transcriber will also be used to reprogram the Recorder and could be used for preliminary data reduction.

The feasibility study of Phase I was an investigation of the application of existing technology to a miniaturized data recording system. In particular we have investigated development of a minimum battery-drain device through such techniques as strobed power-control, as well as an automatic power-up and power-down circuit based on sensing of the vibration associated with the aircraft engine's operations. We also sought to achieve maximum user flexibility by investigating low power usage algorithms for internal data compression and processing, as well as the feasibility of configuring the unit with different bandwidths, to be able to handle low frequency-low bandwidth parameters such as Nz, as well as higher (50Hz) bandwidths to monitor buffet loads.

Additionally, we have endeavored to provide installation flexibility by configuring the recorder for use with a variety of external signals such as temperature sensors, pressure transducers, cat/arrest sensors, etc.

The Phase I effort, in providing a conceptual design, design performance analysis and brassboard model represents the normal first step in a phased engineering development program. Phase I sets the stage for moving into a Phase II engineering development program intended to result in a finished, documented, tested recording system.

The technical objectives of Phase I were:

1) To determine the feasibility of melding transducers, electronics and software in a compact device which will accurately measure and internally classify the parameters of interest while:

   a) Achieving very low power operation; and
   b) Packaging the resultant configuration in a small volume.

2) To provide a hardware design concept and design performance analysis for the projected recording system.

The major question to be answered was: Can a power control methodology based on an interplay between transducers, low-power circuitry and smart algorithms be devised and packed in a small volume?

2.0 SYSTEM DESCRIPTION

The system provided under the SBIR contract is a version of Esprit's ELAPS I battery-operated flight data recorder which had been developed for a variety of remote monitoring uses. For their application the Navy has adopted the nickname "Slap-Track" unit, to reflect its easy installation and ability to track the fatigue loads on a particular structure.

2.1 The Slap-Track System

The Slap-Track system has two major components: the airborne system and the ground support system, each of which can be considered to be made up of two or more subcomponents.

The airborne system includes the recorder and the transducer set. The recorder is completely self-contained and self-powered; it includes a power source, a microcomputer, program memory, data memory, a digitizer, analog signal conditioners, a power control transducer and associated circuitry and at least one optional accelerometer. The transducer set includes any strain-based transducer of reasonable input impedance and bridge-like circuitry. Pressure, acceleration and strain transducers are presumed to be of the greatest interest. Current source temperature sensors or medium to high impedance resistance thermometers could also be handled.

A desktop computer, computer interface and master program disk comprise the ground based system. Virtually any small desktop computer would suffice to handle the recorder programming, data retrieval and data transcription tasks assigned to the computer. An IBM compatible unit appears to offer the greatest flexibility. The computer interface assures that the handshake protocol and logic voltage levels between the computer and the recorder serial interface are compatible. The system master disk contains the algorithm menus and user interactive software.

Block diagrams of the Recorder System and the Recorder are given in Figures 2.1 and 5.1 respectively.

2.2 The Recorder

The Recorder is a battery powered, four channel data monitoring, compression and storage system. Three major subsystems make up the Recorder, namely the power supply, analog signal conditioning and digital sections. (See Figure 5.1, the Recorder Block Diagram.)

The power supply includes a set of lithium batteries, a step down switch mode power supply, a transducer, a rectifier/comparator circuit and transducer drive circuitry. The switch mode supply derives the nominal 5 volt operating power from a 7 to 11 volt battery supply and provides for use of battery chemistries to match the expected temperature range. The transducer and rectifier/comparator act to conserve the system power by

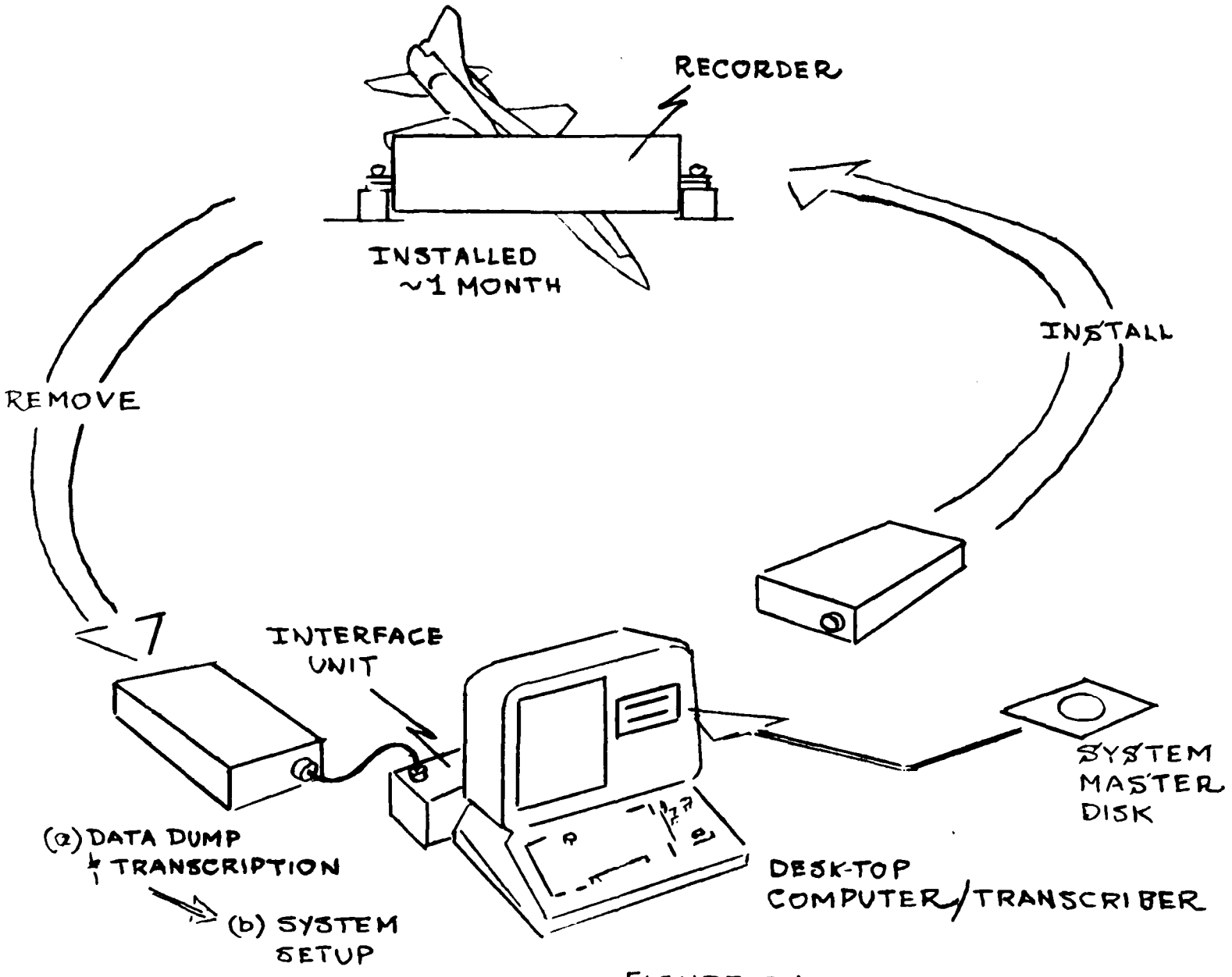


FIGURE 2.1
BLOCK DIAGRAM-RECORDER SYSTEM

keeping the system in a low power mode when valid data signals are not present. A self-generating velocity transducer will be built into the system. (Other types of transducers could provide this function.) The data transducers are driven by switched, low duty cycle sources to reduce their power consumption.

The analog signal conditioning section includes two main and two auxiliary data channels. The main channels have high impedance inputs and feature software controllable gains, offsets and bandwidths. The available bandwidths range from 2.5 to 50 Hz and are set by clocking of the 4th order, low pass, butterworth, switched capacitor filter. The auxiliary channels are included to provide for event monitoring (e.g., catapults and arrests) and simple two wire transducer temperature monitoring).

The digital section contains an A/D converter, four D/A converters, a CMOS microcontroller and CMOS memory. The A/D converter is an 8 bit successive approximation converter with a built-in 8 channel multiplexer. The D/A converters are 8 bit, latched multiplying converters, included to provide software control of offset and bandwidth. The microcontroller is the 80C31 Intel 8 bit, low power CMOS device. The memory includes U.V.EPROM containing the operating system and counting algorithms and static RAM for data storage. Each of the two memories has a 64 K bit capacity arranged in 8 kilobyte format. The software includes provisions for adjusting the analog gains, bandwidths and offsets, as well as selection of the counting algorithms. The algorithms include load level, peak valley and rain flow data compression of the physical parameter being monitored.

3.0 DESIGN GOAL SPECIFICATION

General:	The equipment shall be a self-contained, self-powered data recorder capable of monitoring a variety of environmental transducers. The recorder shall perform preliminary data reduction/compression and store the results in non-volatile memory for later retrieval.
Size:	1" x 2" x 4" maximum volume (See Figure 3.1).
Mounting:	To mounting pads. Mounting pads bonded or bolted to the aircraft. (See Figure 3.1)
Power:	Supplied by internal batteries. Up to 1 month supply per battery set. Projected - 3AA lithium cells to support up to 100 hours of data gathering and one month or more of untended installation.
Power Control:	a) CMOS static RAM, continuously supported. b) Other circuitry activated and de-activated by turn-on circuit sensitive to engine vibrations. c) In flight algorithms designed to utilize CMOS processor standby and wait states.
Data Channels:	Two channels max plus 2 event counts (e.g., count of catapults and arrests.)
Channel Bandwidth:	Up to 50 Hz (one channel system) Up to 20 Hz (two channel system) 2.5 Hz minimum bandwidth
Bandwidth Control:	By software.
Conversion Resolution:	8 bits.
Conversion Type:	Absolute.
Data Compression:	Choice of: a) level classification (exceedance count). b) peak valley pairs. c) simple rainflow.
Compression Control:	By software.

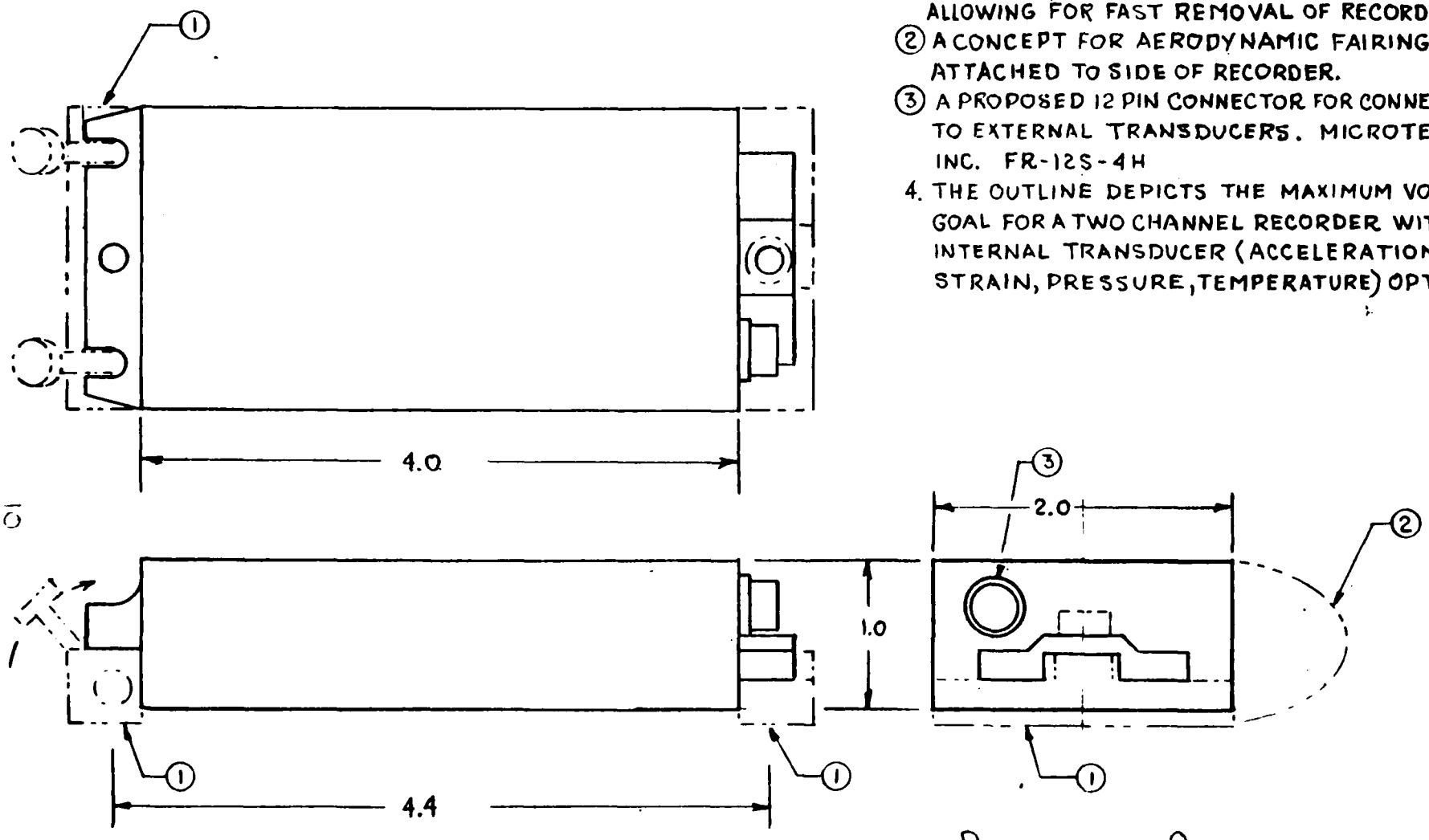
Data Format:	a) Level classes - up to 32 (over 16 x 10^6 counts per level). b) Peak valley pairs - up to 32 x 32 peak-valley matrix (496 cells, up to 2 bytes per cell, 65 x 10^3 counts per cell). c) Rainflow - up to 32 vector magnitudes and starting values. 65 x 10^3 counts per magnitude.

(cell sizes for (b) & (c) can be doubled for data bandwidths above 20 Hz.)

Data Memory:	2K x 8 CMOS Static RAM
Data Retrieval:	Module removed from aircraft and transported to Transcriber (commercial microcomputer, e.g., an IBM PC plus associated interface hardware). Data transfer through a serial port and software UART.
Transducer Location:	Options for internal or external mounting.
Transducer Power:	Internal - Powered by system. External - Powered by system if low power device capable of pulsed power operation. Supplementary battery pack or ships' power required for high-drain servo type transducers.
Operation Options:	The mode of operation is controlled by software. The transcriber is used to program the recorder. The following features are under software control: Channel Bandwidth Channel Ranges Channel Sample Rate Data Compression Method Data Format
System Accuracy:	5% max; 3% design goal.
Design:	To meet the intent of MIL-E-5400T Class 3 equipment.

NOTES:

1. PHANTOM LINES DEPICT A MOUNTING CONCEPT ALLOWING FOR FAST REMOVAL OF RECORDER.
2. A CONCEPT FOR AERODYNAMIC FAIRING ATTACHED TO SIDE OF RECORDER.
3. A PROPOSED 12 PIN CONNECTOR FOR CONNECTION TO EXTERNAL TRANSDUCERS. MICROTECH INC. FR-12S-4H
4. THE OUTLINE DEPICTS THE MAXIMUM VOLUME GOAL FOR A TWO CHANNEL RECORDER WITH INTERNAL TRANSDUCER (ACCELERATION, STRAIN, PRESSURE, TEMPERATURE) OPTIONS.



PRELIMINARY OUTLINE
SELF CONTAINED FATIGUE DATA RECORDER
FIGURE 3.1

4.0 PACKAGING

The packaging approach is described in paragraph 4.0 of Appendix A (The Interim Report).

Since the report was submitted, further study of the volume requirements has led us to select and propose a mix of surface mount and hybrid modules for use in the final design. The latter has been selected for the analog circuitry to minimize volume.

5.0 CIRCUITS (Also see paragraph 5.0 of Appendix A.)

A recorder system block diagram is given in Figure 5.1. The major system components are:

(5.1) Data Source
- (a) Transducer
- (b) Transducer driver/timer

(5.2) Power Supply
- (a) Batteries
- (b) Power Control
  - (i) reset control
  - (ii) vibration detector
  - (iii) ram and clock save
  - (iv) switched supply

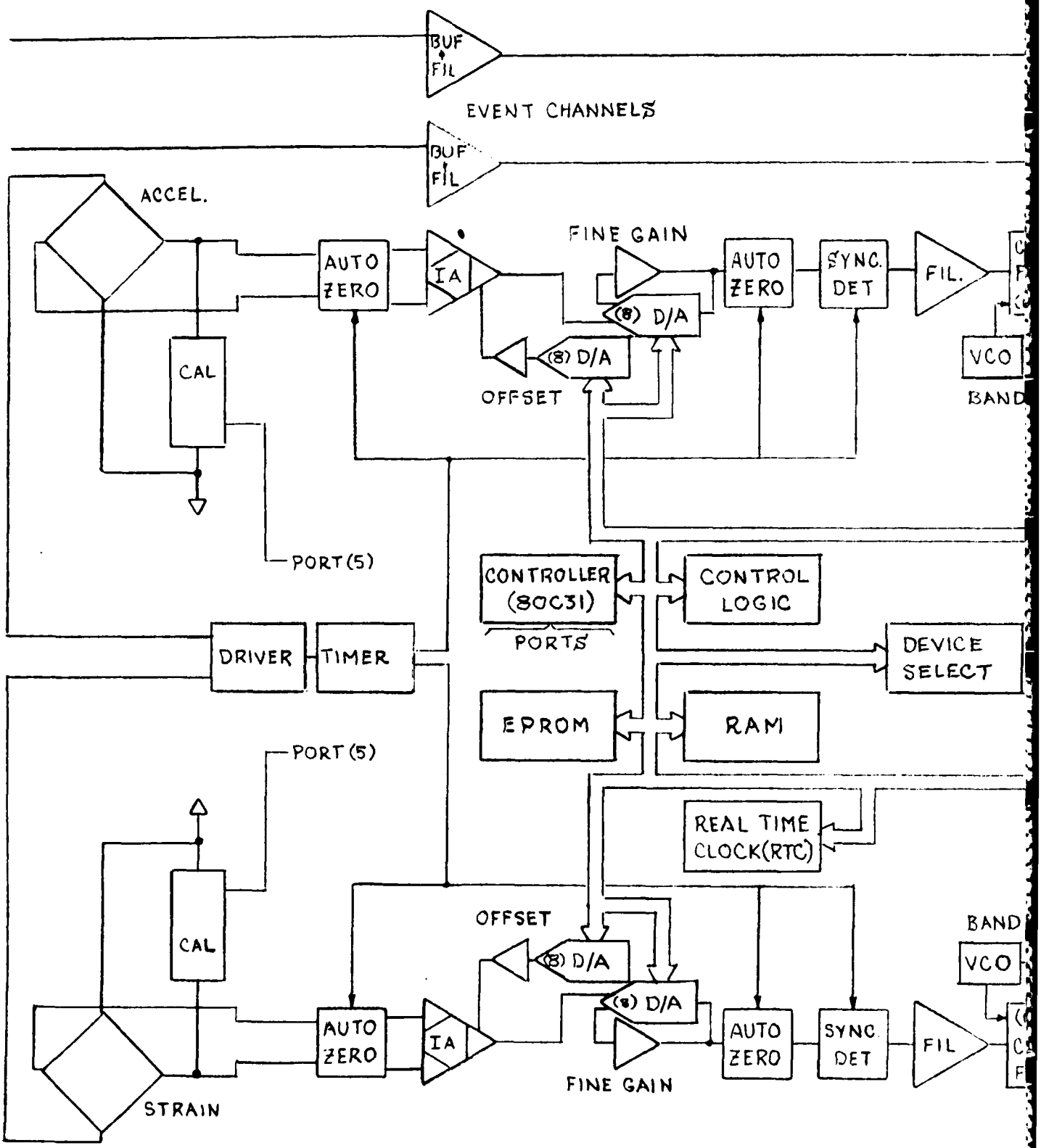
(5.3) Analog Chain
- (a) Input amplifier
- (b) Fine gain
- (c) Auto zero
- (d) Sample & hold
- (e) Filters
- (f) A/D converter

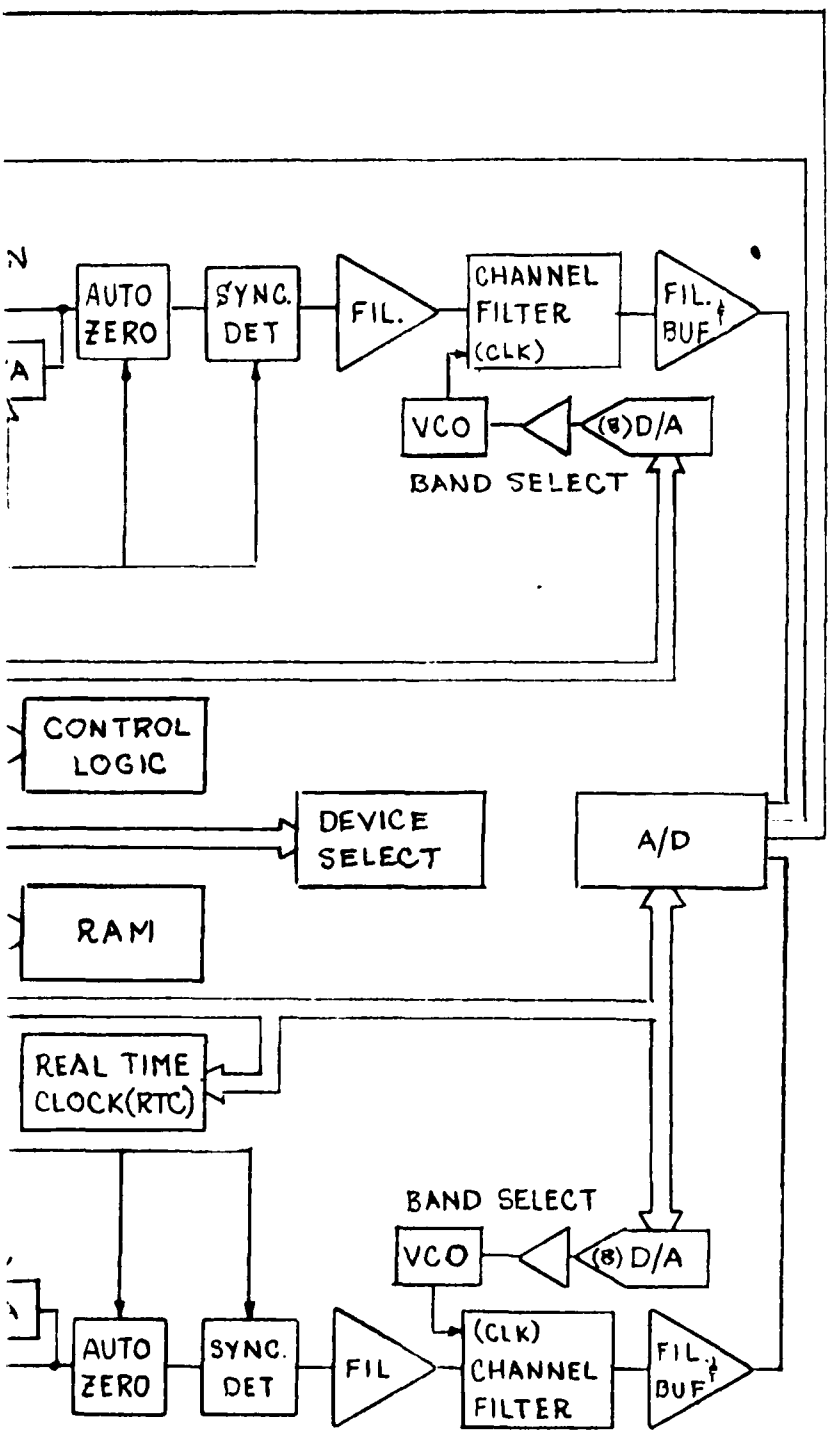
(5.4) Digital Section
- (a) Controller
- (b) Program memory
- (c) Data memory

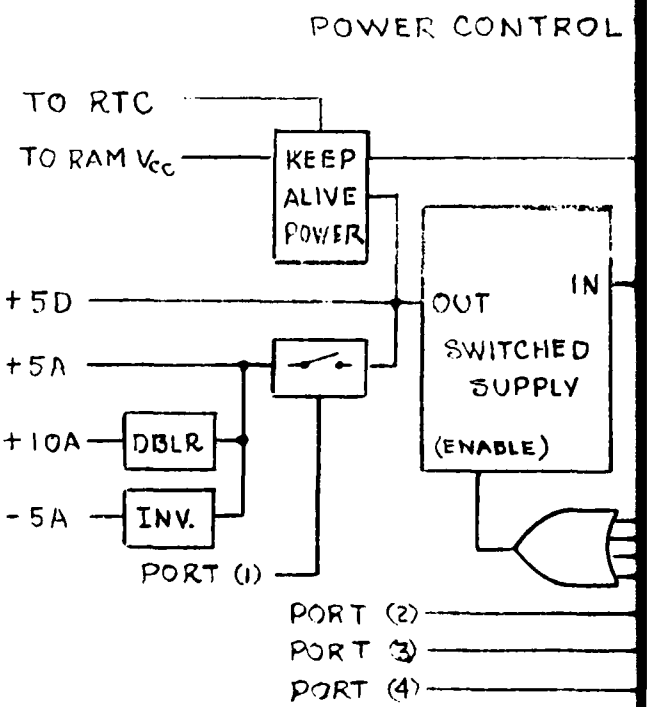
5.1 DATA SOURCE

(a) Transducers

The transducers are discussed in paragraph 7.0 of Appendix A. The analog channels are intended to drive and accept signals from strain based transducers. The channels also can accept and process signals from other types of transducers so long as adequate grounding is maintained between the transducer and the recorder.


BUF
FIL
EVENT CHANNELS
BUF
FIL
ACCEL.
AUTO
ZERO
IA
FINE GAIN
(8) D/A
AUTO
ZERO
SYNC.
DET
FIL.
VCO
BAND
(8) D/A
OFFSET
CAL
PORT(5)
CONTROLLER
(80C31)
PORTS
CONTROL
LOGIC
DRIVER
TIMER
DEVICE
SELECT
EPROM
RAM
PORT(5)
REAL TIME
CLOCK(RTC)
CAL
OFFSET
BAND
VCO
(8) D/A
(8) D/A
AUTO
ZERO
IA
AUTO
ZERO
SYNC.
DET
FIL
FINE GAIN
STRAIN


AUTO ZERO
SYNC. DET
FIL.
CHANNEL FILTER (CLK)
FIL. BUF
VCO
(8) D/A
BAND SELECT
CONTROL LOGIC
DEVICE SELECT
A/D
RAM
REAL TIME CLOCK(RTC)
BAND SELECT
VCO
(8) D/A
AUTO ZERO
SYNC. DET
FIL
(CLK) CHANNEL FILTER
FIL. BUF


POWER CONTROL
TO RTC
TO RAM Vcc
KEEP ALIVE POWER
+5D
+5A
+10A
DBLR
-5A
INV.
PORT (1)
OUT
IN
SWITCHED SUPPLY
(ENABLE)
PORT (2)
PORT (3)
PORT (4)

POWER CONTROL SYSTEM

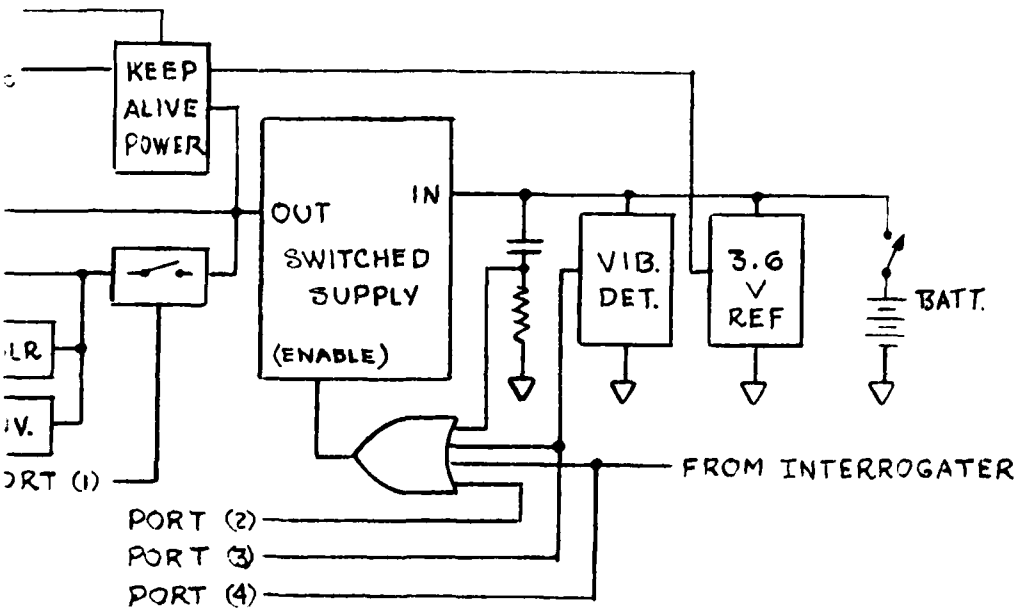


FIGURE 5.1

RECORDER
BLOCK DIAGRAM

ESPRIT TECHNOLOGY ASSOCIATES

Also included are two event channels that will accept either digital ("0" and "1") or simple analog signals from various transducers such as parameter driven switches (e.g., acceleration) or high level analog devices.

(b) Transducer Driver/Timer

A number of different transducer drive schemes were studied in Phase I. They are described in paragraph 5.0 of Appendix A.

The transducers will be driven by a switched D.C. voltage operating at a 10% to 20% duty cycle in order to minimize transducer power and yet attain as high a level signal as possible from the transducer. A conceptual drive system is shown in Figure 5.5 (Analog Channel Conceptual Schematic). Figure 5.2 shows a simple breadboard circuit and the input/output waveforms obtained in a bench test.

The circuit is intended to drive the transducer with a fixed amplitude voltage pulse. Fixed amplitude voltage drive leading to absolute value conversion in the A/D converter has been selected for two reasons:

1. If the recorder is to be easily adapted to monitor a variety of transducers, especially signal sources not powered by the recorder, it is virtually imperative that the recorder be designed for absolute rather than ratiometric voltage measurements.

2. Most commercially available temperature compensated strain transducers are designed for voltage rather than current drive.

The transducer driver is controlled by a timer circuit that acts to synchronize the transducer drive, synchronous detection and auto zero functions. A timer scheme is shown in Figure 5.3. The two analog channels are timed on and off by one shot circuits triggered by the basic square wave timer oscillator. Channel one is triggered by the rising edge and channel two by the falling edge of the square wave in order to minimize the current pulses drawn by the transducers. As shown in the diagram, the signal sampling (synchronous detection) is coincident with the transducer drive pulse while the auto zero occurs when the transducer drive is off. In the final configuration, time delays may be introduced between signals to assure both settling of the analog chain before sampling and entry to the hold mode before auto zeroing. In addition, the offset D/A converter may be removed from the circuit during auto zero.

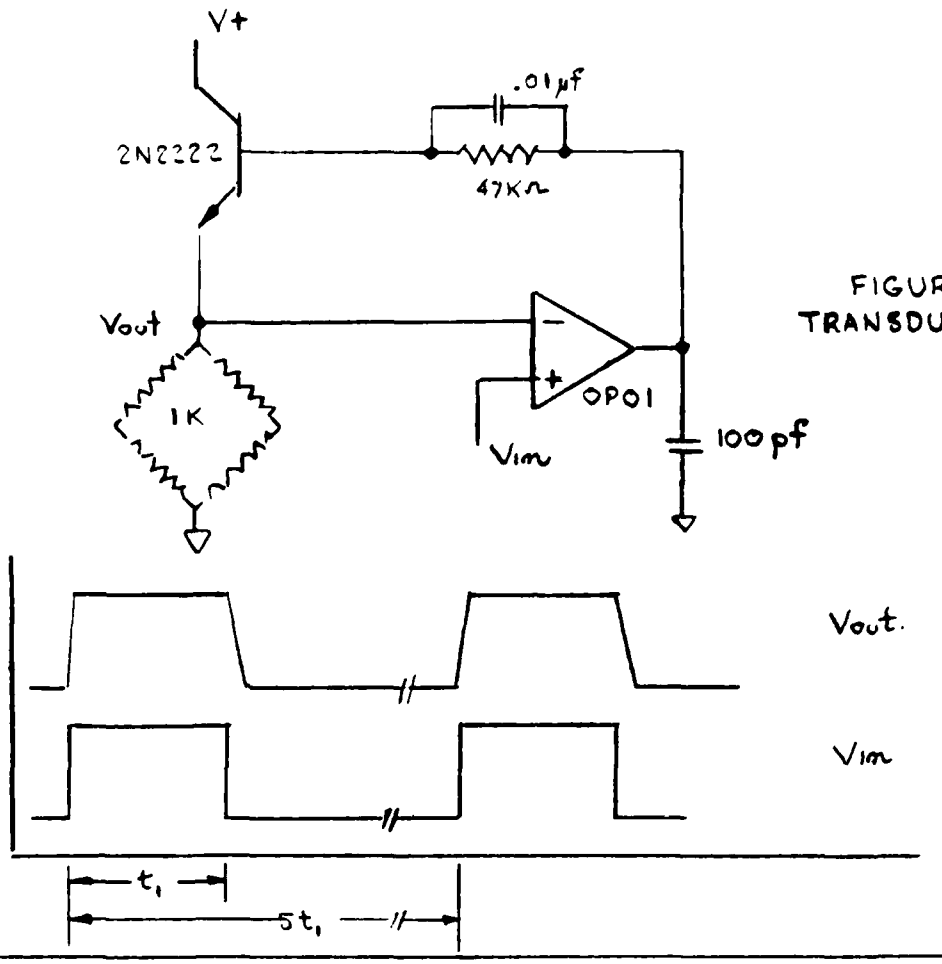
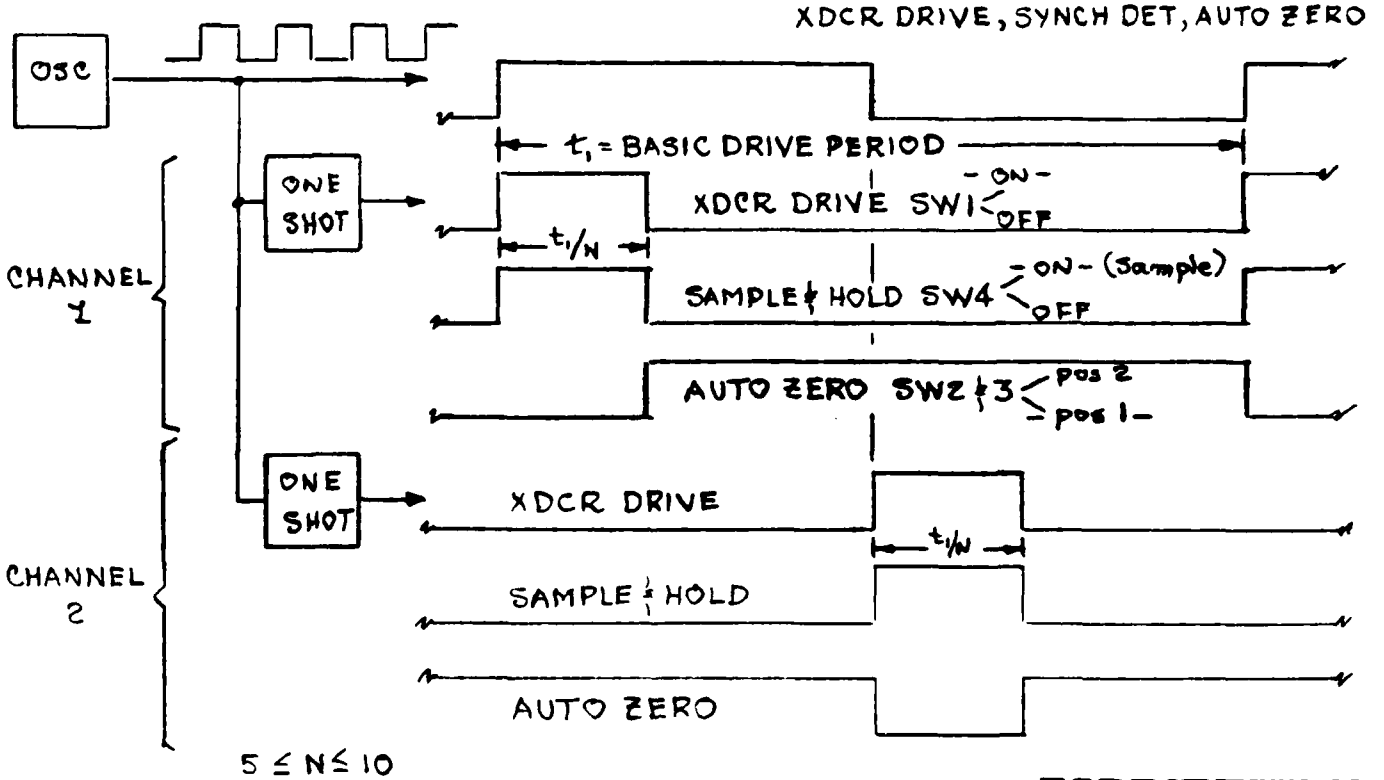


FIGURE 5.2
TRANSDUCER DRIVE

FIGURE 5.3
TIMER-
XDCR DRIVE, SYNCH DET, AUTO ZERO



5.2 POWER SUPPLY

(a) Batteries

The system is designed to use lithium batteries and presently calls for a series pack of 3 AA size cells. AA size has been chosen to ease procurement as it is a standard size supplied by a number of manufacturers.

Different battery chemistries will probably be required to cover different temperature ranges of operation. For instance, Lithium Thionyl Chloride can be used over the range -40 C to +71 C (source 1) or -40 C to +125 C (source 2), Lithium Poly-carbon Monofluoride over the range -73 C to +93 C (source 2) and Lithium Copper Oxyphosphate over the range 0 C to +175 C (source 3). In the preceding, "source" refers to various battery suppliers.

We note that a part of the Phase II effort is to study the application safety of these batteries.

Paragraph 8.0 of Appendix A describes the battery selection effort carried out in Phase I and presents various papers and data items pertaining to the batteries.

(b) Power Control

The power control system is shown on the block diagram of Figure 5.1. Included in the power control system is a vibration detector, an initial battery on detector (RC circuit), an OR gate power enable driver, a reference supply to keep the data RAM and RTC (real time clock) alive, and a switched-buck converter followed by inverters and doublers required to supply the system voltages.

The power control system keeps the recorder in a low power mode until the buck converter is enabled by any of three events, namely: (1) battery switched on, (2) interrogator plugged in, or (3) vibration is detected. This subsystem is best described by relating the sequence of events as the recorder is set up and used.

Assume the operator has completed the initial recorder set up with the transcriber; i.e., the counting algorithm, bandwidth and initial gains and offsets have been programmed in. After completing the programming, the operator leaves the battery switch open as the recorder is transported to the installation site. The recorder is then mounted and connected to the previously installed transducer(s). The battery switch is closed. The signal from the RC timer enables the switched supply and, as the +5D power comes on, the processor is reset. The first reset of the processor causes it to initialize and ready itself for the measurement task. During initialization

the processor holds port 2 high to keep the switched supply on until initialization is complete at which time port 2 goes low, the power goes off, and the system is in a low power mode. The operator then plugs in the interrogator to complete the system check out and trim the gains and offsets to match the installed transducer(s). (Note that the "interrogator" and "transcriber interface" are the same device - see Figure 2.1) When the interrogator is plugged in, the switched supply is enabled and the processor is reset. As the processor comes on, it detects (through port 4) the interrogator presence and goes to that portion of the internal software allowing the operator to make adjustments as required. When the interrogator is removed, the power supply goes off and the system enters the low power mode.

The recorder is now set up, installed, trimmed and ready to perform the data monitoring, compression and storage task. Data monitoring is initiated by a signal from the vibration detector. When the vibration detector senses aircraft vibration, it enables the switched supply through the OR gate. The processor applies power to the analog system by signaling through port 1 and x minutes later starts the monitoring task.

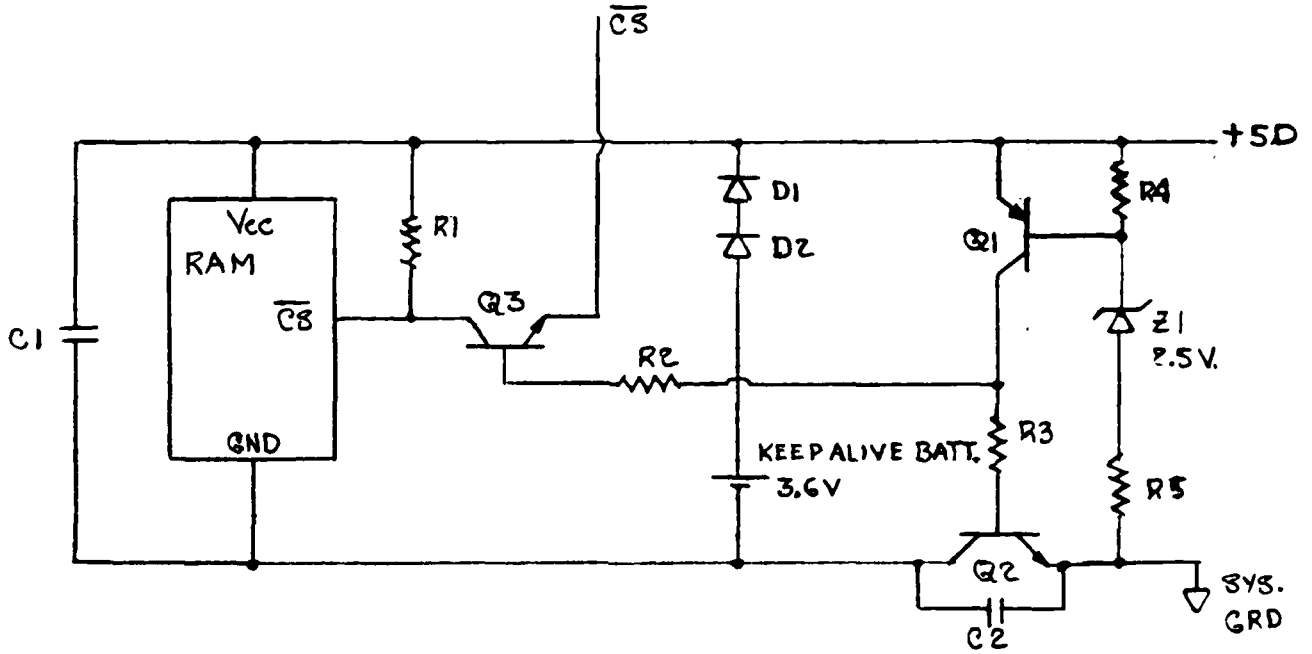
During the data monitoring mode the processor holds the power on through port 2 and watches port 3 for loss of the vibration signal. If the vibration signal disappears, the processor waits y minutes, completes its data storage and shut down steps and goes to the low power mode to wait for the next indication the aircraft is operating.

A vibration detection scheme using an acceleration switch was demonstrated in the brassboard system. The results showed that a vibration transducer with no D.C. term; i.e., that gives no output for constant acceleration or velocity inputs, is required. If the transducer does have a D.C. term, its sensitivity is dependent on its orientation in the installation. Phase II thus includes incorporation of vibration transducer(s) with no D.C. term - namely a dynamic velocity sensor. The sensor is described in paragraph 5.0 of Appendix A under the Power Supply heading. We note that the sensor described in that paragraph and in Exhibit 3 to that paragraph does not exhibit stick-slip ("stiction") - it is based on a leafspring supported mass.

The RAM and clock save reference power supply keeps the real time clock and RAM alive when the switched supply is not running; i.e., when the recorder is in the low power mode. This supply is driven directly from the battery and its output is enabled when the 5D voltage from the switched supply goes low. A RAM keep alive supply scheme is shown in Figure 5.4. The circuit applies a 2.2 to 2.4 volt Vcc to the RAM when 5D is turned off. Coincidentally, the RAM CS is pulled high to prevent an inadvertent write to the

FIGURE 5.4

RAM KEEP ALIVE CIRCUIT



+5D	D1, D2	Q1, Q2	$\overline{CS}$	Vcc
ON	REVERSE BIASED	ON	ENABLED	+5 V.
OFF	FORWARD BIASED	OFF	DISABLED	+2.2 to +2.4 V

DIODES D1 & D2 PREVENT CURRENT FLOW INTO THE BATTERY WHEN 5D IS ON.

A $\overline{CS}$ LOW IS PASSED THROUGH Q3 TO THE RAM $\overline{CS}$ PIN WHEN 5D IS ON & $\overline{CS}$ IS ENABLED.

Q2 ISOLATES THE BATTERY AND RAM FROM THE SYSTEM GROUND WHEN 5D IS OFF. CARE IS TAKEN TO ASSURE NO "HIDDEN" PATHS EXIST FROM +5D THROUGH OTHER CHIPS & BACK THROUGH THE RAM SIGNAL LINES.

memory when the 5D power is off. A similar circuit is applicable to the real time clock.

The keep alive system shown in Figure 5.4 requires a separate battery in the keep alive circuit. This feature is worth consideration. A keep alive battery separate from the power supply batteries can offer an increase in the data retention reliability for if, in the middle of an installation/removal cycle, the main battery goes bad, the separate battery will retain the previously collected data. This design feature will be considered in Phase II.

The Phase II effort includes development of the switched supply. The supply will be a switch mode D.C. to D.C. converter developing 5 volts from a 7-11 volt battery input. The goal is to attain a 75% to 80% efficiency in the conversion to give 2.6 to 2.8 ampere hour capacity from the battery/converter system.

The converter will be optimized both for the 10 to 10.5 volt input operating voltage provided by three Thionyl Chloride AA cells and for the system operating current required when driving two transducers and using a peak/valley data compression scheme.

Our preliminary approach is to use one of the CMOS micro-power switching regulators as the kernel of the supply. A step down mode has been selected to avoid the approximate 8% loss of power in protection diodes used for parallel battery systems. We note that either the battery safety or the supply efficiency investigation may point the design towards a step up configuration. (batteries in parallel).

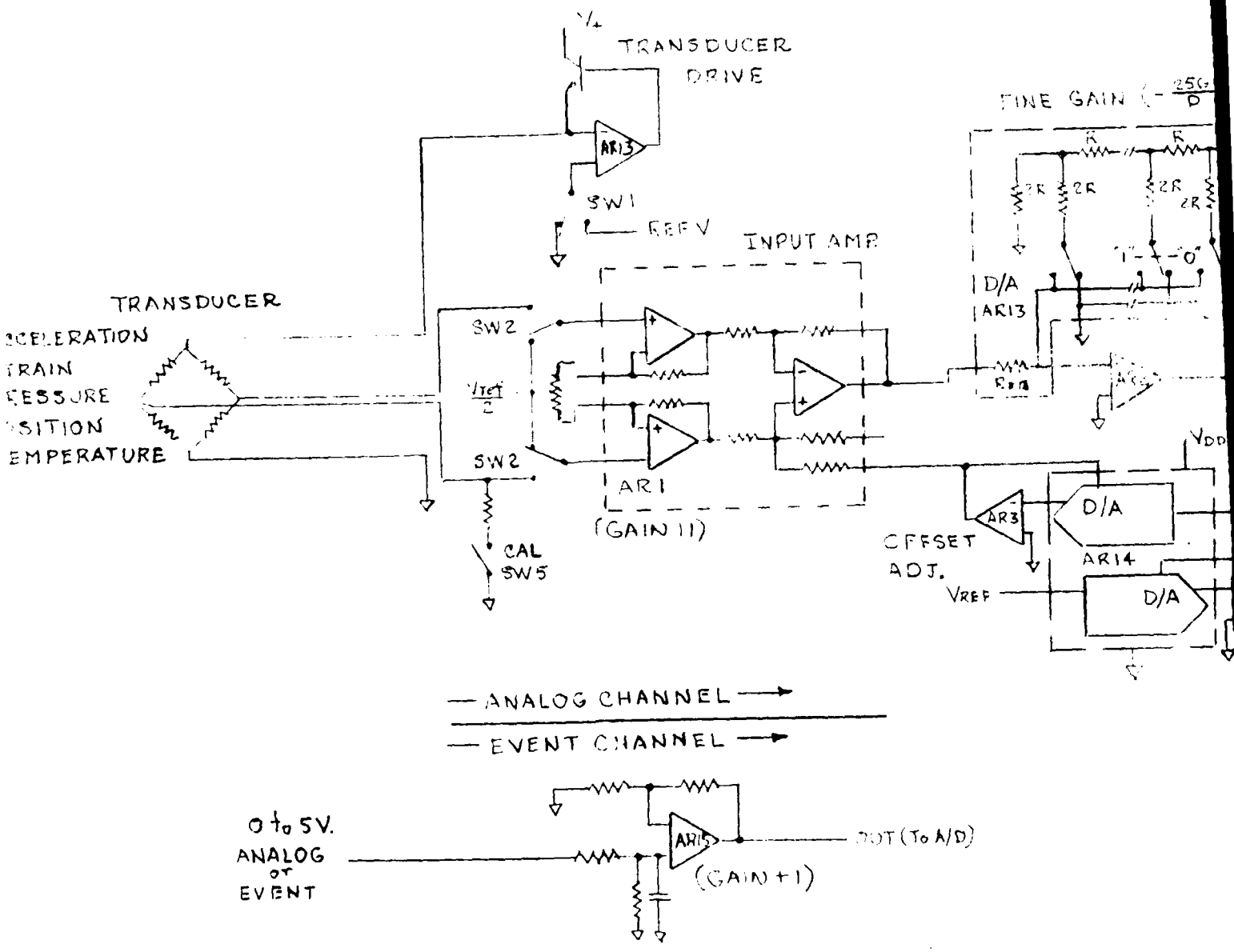
5.3 THE ANALOG CHAIN

The recorder has four analog channels; two intended as event channels and two for general analog data handling. The latter two channels feature software control of gain, offset and bandwidth.

The proposed packaging scheme is to include two identical analog hybrids each of which contains one general analog and one event channel. A conceptual schematic of the circuitry in one hybrid is given in Figure 5.5.

The signal flow in the analog channel is from left to right in the figure - the channel contains the following elements:

(a) Input Amplifier -- The input amplifier is a standard three op amp instrumentation amplifier with fixed gain. The amplifier presents a high impedance to the source and can accept signals from either differential or single-ended output devices. The high impedence input ensures no degradation of the signal source due


TRANSDUCER DRIVE
AR13
SW1
REF V
INPUT AMP
TRANSDUCER
SW2
SW2
AR1
(GAIN 11)
CAL
SW5
FINE GAIN
D/A
AR13
AR3
D/A
AR14
D/A
OFFSET
ADJ.
VREF
VDD
— ANALOG CHANNEL →
— EVENT CHANNEL →
0 to 5V.
ANALOG
or
EVENT
AR15
(GAIN +1)
OUT (To A/D)

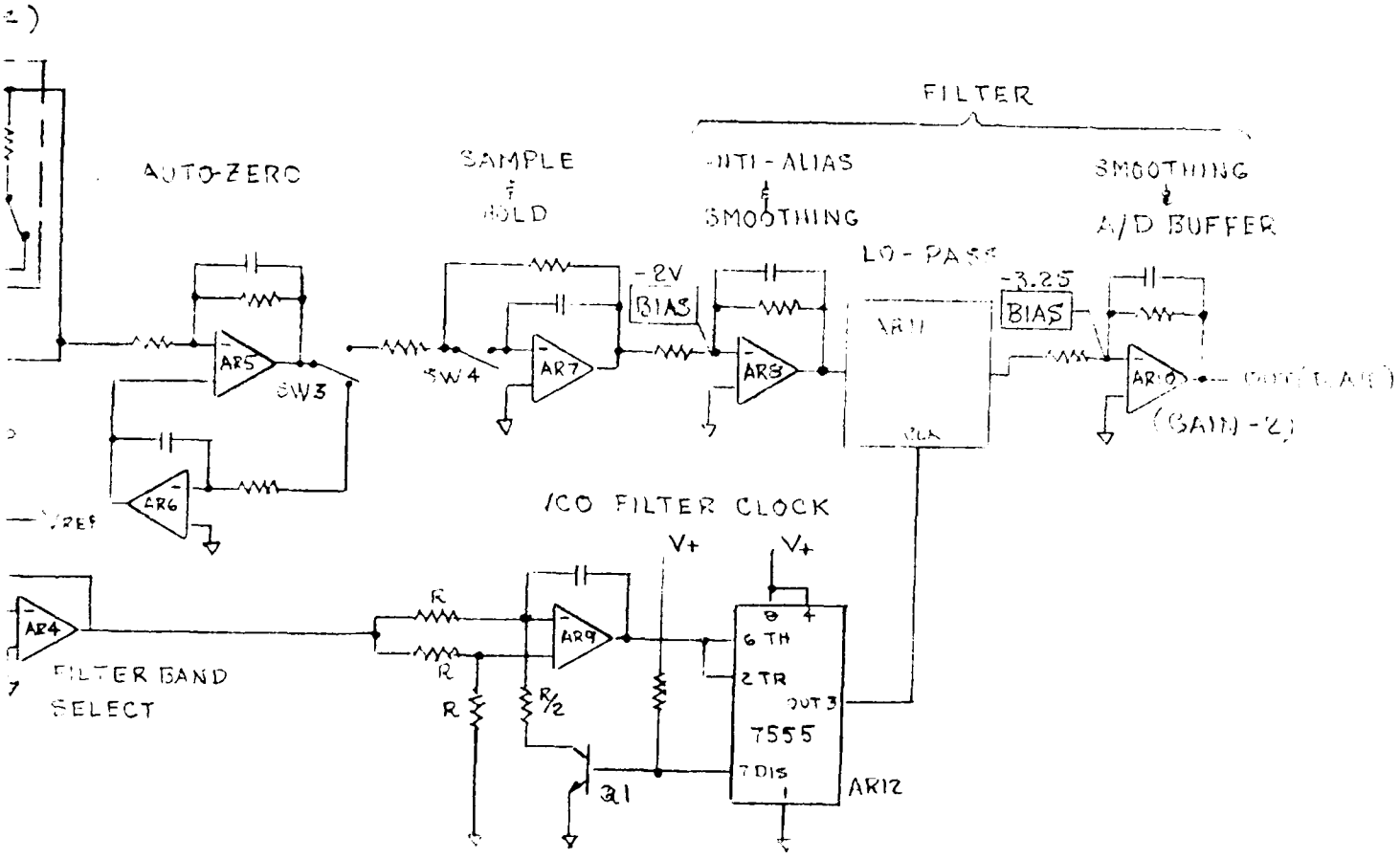


FIGURE 5.5
CONCEPTUAL SCHEMATIC
ANALOG CHANNEL

to loading by the recorder. A software controlled offset voltage is added to the signal at the amplifier's output stage. The offset can be used for either or both of counteracting transducer bias and shifting the channel range to cover asymmetrical inputs. The offset level is determined by a digital word to the offset D/A converter and its value is:

$$-V_{ref} \frac{(\text{Digital Word})_{10}}{256}$$

where the digital word ranges from 0 to 255.

(b) Fine Gain -- The fine gain stage provides for software control of the channel gain. The D/A converter (AR13) presents a variable (digitally controlled) feedback to the inverting amplifier AR2. The gain is:

$$G = \frac{-256}{(\text{Digital Word})_{10}}$$

and thus ranges from -256/255 to -256. In use, this gain adjust would normally be restricted to gains of 25 or less to preserve a 10% or finer step adjust of gain. (The percentage change in gain for a ΔD of 1 is given by:

$$100 \left|\frac{G}{G}\right| = \left|\frac{100}{D}\right| \Delta D$$

and for 100/D to be 10 or less, $D \geq 10$ which gives a gain of 25.6 or less).

(c) Auto Zero -- The auto zero acts to zero out the bias drifts associated with the amplifiers and circuits preceding it in the analog chain. The basic auto zero is an inverting amplifier (AR5) with a wash out integrator feedback (AR6). With the switches in the positions shown, no power is applied to the transducer, the differential input signals are shorted together and tied to the transducer common mode voltage, the offset voltage D/A (AR14) is set for zero out, the previous signal is held on the capacitor in the feedback of AR7 and the integrating capacitor in the feedback of AR6 is charging to whatever value is required to drive the output of AR5 to zero. The washout integrator thus sums into AR5 the voltage required to counteract any common mode signal not attenuated by AR1 as well as offset voltages associated with the AR1, AR2, AR3, and AR5 circuits. When the switches are thrown to their other position, the auto zero integrator adds the above voltage to the signal and thus negates the error voltages. The switching functions are synchronized to assure auto

zero, sample and hold and transducer drive are all operating together in the correct temporal relationship. A timing diagram is given in Figure 5.3.

(d) Sample & Hold -- The sample and hold circuit (AR7) has a dual function; it, (1) is a synchronous detector operating in conjunction with the transducer drive circuit and (2) it "holds" the analog signal during the auto zero. The functions are performed simultaneously as shown in the timing diagram of Figure 5.3.

(e) Filter -- The filter includes an anti-aliasing and sample and hold output smoothing filter (AR8), a switched capacitor - 4 pole - low pass butterworth filter (AR11), an output smoothing filter and A/D buffer (AR10) and voltage controlled clock for the switched capacitor filter (AR14, AR4, AR9 & AR12).

The corner (-3db point) of the switched capacitor filter is 0.01 times the clocking frequency. This filter is the main channel filter and its corner is controlled by software through the VCO and D/A converter. The band selection is intended to extend from 2.5 Hz (250 Hz clock) to 50 Hz (5000 Hz clock).

The switched capacitor filter is a sampled data system and as such requires the signal input to have little or no energy content above 1/2 the sampling rate if aliasing errors are to be avoided. The active filter section AR8 supplies this prefilter function. This filter is shown as a simple low pass in the conceptual schematic. The final design may require a higher order or a degree of tuneability in this filter to reduce aliasing errors - especially if low bandwidth signals are to be abstracted from signals with large high frequency content.

The output of the switched capacitor filter appears as small steps following the input signal (below the filter bandwidth). These steps are "smoothed" out by the output smoothing filter so as to present a clean signal to the A/D converter.

The supply voltages to the switched capacitor filter will be V+ = +5 volts and V- = ground in order to minimize the filter power usage. (11.5 milliwatts versus 35 milliwatts for a $\pm$ 5 volt supply). In addition, the A/D converter will be unipolar; i.e., it wll accept signals in the zero to +5 volt range. The bias networks indicated at AR8 and AR10 shift the signal zero level as needed for operation over the requisite voltage ranges.

(f) A/D Converter -- The A/D converter we plan to use is an 8-channel, 8-bit data acquisition device with a built-in multiplexer and sample and hold. It is a low power CMOS device consuming 2.5 milliwatts or less power and yet performing a successive approximation conversion in 25 microsec.

Figure 5.6 outlines an example of the set up and scaling of an analog channel for a particular application. The example illustrates how the offset is applied to the output stage of the input amplifier to handle an asymmetric signal source. The calculations performed to select the gain and offset digital word values would be carried out with interactive software menus on the desktop computer in the final system.

5.4 DIGITAL SECTION

The digital section is described in 5.0 of Appendix A.

The only change made in the digital section since the interim report was written is the addition of the real time clock.

The EDH687C31 microPak described in Exhibit 6 to paragraph 5 of Appendix A includes the microcontroller, the program memory and the data memory. Phase II includes a task to isolate the data RAM power and ground so the RAM can be kept alive to serve as the nonvolatile data memory. A keep alive circuit scheme is sown in Figure 5.4.

6.0 COMPONENTS

The major digital component, the EDH687C31 microPak, is described in Exhibit 6 to paragraph 5 of Appendix A.

Table 6 gives a listing of components that fit the scheme of the conceptual schematic of Figure 5.5.

The system A/D converter is not shown on the schematic. The converter used in the brassboard unit was the Siliconix 8 channel, 8 bit, CMOS data acquisition system and is currently the converter of choice for the final unit. The converter has a total unadjusted error of $\pm$ 0.75 LSB over the full temperature range. The converter is powered by +5 volts for both Vcc and Vref with a total current draw of 1ma maximum over the full temperature range.

7.0 TRANSDUCERS

The transducers are described in paragraph 7.0 of Appendix A.

EXPECTED RANGE - 0 to 4000 με

TRANSDUCER - STRAIN BRIDGE
1.025 MV/V/1000 με SENS.
0.5 MV/V OFF SET

TRANSDUCER EXCITATION - 4 VOLT PULSES

TRANSDUCER OUTPUT	AT 0 IN .002 Volts	AT 4000 με .0184 Volts
AR1 GAIN = 11 ∴ WITH 0 OFFSET OUT = WITH D/A REF V. = 2.5 V SET D_{10} = 11 OFFSET = -.1074 Volts	.022	+.2024
∴ OUTPUT FROM AR1 =	-0.0854	+.095
AR2 SET D_{10} = 20 ∴ GAIN = - 256/20 = -12.8		
∴ OUTPUT FROM AR2 =	+1.0931	-1.216
AR5 GAIN = -1 ∴ OUTPUT =	-1.0931	+1.216
AR7 GAIN = -1 ∴ OUTPUT =	+1.0931	-1.216
AR8 GAIN = -1, ADD -2V BIAS TO SUMMING JUNCTION.		
∴ OUTPUT FROM AR8 =	+.9069	+3.216
AR11 GAIN = 1 ∴ OUTPUT =	+.9069	+3.216
AR10 GAIN = -2, ADD -3.25V BIAS TO SUMMING JUNCT.		
∴ OUTPUT FROM AR10 =	+4.686	+0.068

THUS - GIVEN A 5 VOLT REF TO THE A/D CONVERTER THE INPUT SPAN OF 4000 με RESULTS IN AN OUTPUT BIT SPAN OF

$$\frac{4.686 - .068}{5} \times 256 = 236.4 \text{ BITS}$$

GIVING A SENSITIVITY OF

$$\frac{4000 \mu\varepsilon}{236.4 \text{ BITS}} \cong 16.9 \mu\varepsilon/\text{BIT}$$

FIGURE 5.6

AN EXAMPLE OF ANALOG CHANNEL SCALING

MFR	PART NO	SCHEMATIC DESIG.	I_s	V_{io} V_{io} T.C.	i_{io} i_{io} Tc	i_b i_b TC	BAND WIDTH	DESCRIPTION
NATIONAL	LH0036	AR1	60 μa (±5V)	INP. 1 MV 10μv/°C OUT 5 MV 15μv/°C	40na –	100na	~9KHz	3 OP AMP INST. AMPLIFIER.
SILICONIX	L144A	(AR3,4 & 15) (AR2,5 & 6) (AR7,8 & 9)	100μa (±5V)	5 MV 3.3 μv/°C	50na –	200na	~400KHz	3 OP AMP MONOLITHIC CHIP
HARRIS	HA5144A-2	AR10	75μa	2MV 3μv/°C	10na 15na	75na 100na	~100KHz	μ POWER OP AMP. OUT SWINGS TO RAIL

MFR	PART NO	SCHEMATIC DESIG.	I_s	GAIN SET	GAIN DRIFT	
PMI	PM7524A	AR13	100μa (25°C) 500μa (O.T.)	±1%	±.004%/°C	8 BIT D/A CONV.
PMI	PM7528A	AR14	100μa 600μa (REF)	±1LSB	±.007%/°C	DUAL 8 BIT D/A CONV.
SILICONIX	DG307A	SW1,2,3	100μa	N/A	N/A	SPDT CMOS SW - DUAL
SILICONIX	DG304A	SW4	100μa	N/A	N/A	SPST CMOS SW - DUAL

MFR	PART NO	SCHEMATIC DESIG	I_s	GAIN	OUT OFFSET	OUT OFFSET T.C.	DESCRIPTION
NATIONAL	MF4-100	AR11	2.3ma (+5V)	±.15dB	-300mv	~163μv/°C	4 POLE, LOW PASS BUTTERWORTH, SWITCHED CAP. FILTER

SEE FIG. 5.5

TABLE 6.
COMPONENTS

8.0 POWER

A discussion of batteries is included in Paragraph 8.0 of Appendix A. A preliminary power budget was presented in that paragraph. An updated estimate of the power requirement for the system (exclusive of the processor and memory) is presented in Table 8.

Combining the updated estimate with the earlier figures for the processor and memory we get:

Operating	(15.24 + 9.5)	x 100 hours	=	2474 mah
Standby	0.5 ma	x 650 hours	=	325 mah
				2799 mah

Considering that our battery and switched supply estimate lies in the range of 2600 to 2800 milliampere hour capacity, the goal appears realistic.

9.0 DATA CHANNELS

The recorder has four data channels. Two channels will have software control of gain, offset and bandwidth. They will handle differential or single ended signals and will present a high impedance to the signal source. The other two channels are called event channels and will have a fixed gain of +1 with no bandwidth or offset adjustments internal to the recorder.

The event channels would normally be used to monitor the occurrrence of isolated events such as landings, catapults etc. They are analog rather than digital however, and can be used to monitor analog signals in much the same way as the two main analog channels.

The data channels are also disussed in Paragraph 9.0 of Appendix A.

10.0 DATA SYSTEM

The counting algorithms are described in Paragraph 10 of Appendix A.

11.0 SYSTEM ACCURACY

The specification of Paragraph 3.0 calls for a system accuracy of 5% with a design goal of 3%.

An accuracy assessment of the analog chain presented in Figure 5.5 was performed using the manufacturer's published data. The result is tabulated in Figure 11.1.

In Figure 11.1, accuracies are noted as percent of value figures and are given for half scale and full scale signals

COMPONENT	DRIVE CURRENT MA	SIGNAL CURRENT MA
TRANSDUCERS		2.0 (10% Duty Cycle)
DRIVERS	0.2	
TIMERS	0.2	
AR1	0.12	0.4
AR2	0.066	0.3
AR13	1.0	
AR5	0.066	0.05
AR6	0.066	
AR7	0.066	0.05
AR8	0.066	0.05
AR8 BIAS	0.2	
AR11	4.6	
AR10	0.15	0.07
AR10 BIAS	0.2	
AR9	0.066	0.2
AR12	0.2	
AR4	0.066	0.2
AR3	0.066	0.25
AR14	1.4	
AR15	0.066	0.2
SW1,3	0.2	
SW2	0.2	
SW4	0.2	
A/D	1.0	
	10.464	3.77
VIB DET	0.3	
REF SUPPLY	3.3	
RAM/RTC SUPPLY	0.3	
RTC	0.1	
	11.47	

CURRENT DRAIN EXCLUSIVE OF PROCESSOR & MEMORY = 15.24 ma.

TABLE 8
POWER ESTIMATE

item	component	error source	basic error - % Val. @ 25°C ½ Scale	basic error - % Val. @ 25°C Full Scale	basic error - % Val. @ 95°C ½ Scale	basic error - % Val. @ 95°C Full Scale	residual error - % val @ 25°C ½ Scale	residual error - % val @ 25°C Full Scale	residual error - % val @ 95°C ½ Scale	residual error - % val @ 95°C Full Scale	reduction by Cal.	reduction by O. Zero
1	AR1	inp. offset V @ 25°C	12.2	6.1	12.2	6.1					X	X
2	AR1	" drift	—	—	8.6	4.3						X
3	AR1	input offset i	1.0	0.5	1.0	0.5					X	
4	AR1	CMRR	7.6	3.8	7.6	3.8						X
5	AR1	Output offset V.	5.6	2.8	5.6	2.8					X	X
6	AR1	" drift	—	—	1.2	0.6						X
7	AR1	gain nonlinearity	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03		
8	AR1, AR13, AR14	offset adjust drift	—	—	1.6	0.8	—	—	1.6	0.8		
9	AR2, AR13	gain set	1.2	1.2	1.2	1.2	0.1	0.1	0.1	0.1	X	
10	AR2, AR13	gain drift	—	—	0.3	0.3	—	—	0.3	0.3		
11	AR2	inp. offset V @ 25°C	5.6	2.8	5.6	2.8					X	X
12	AR2	" drift	—	—	0.1	0.1						X
13	AR2	input bias i	4.4	2.2	4.4	2.2					X	X
14	AR5	gain drift	—	—	0.25	0.25			0.25	0.25		
15	AR5	input offset V @ 25C	0.44	0.22	0.44	0.22					X	X
16	AR5	" drift	—	—	0.02	0.01						X
17	AR6	Auto zero droop	0.18	0.09	0.18	0.09	0.18	0.09	0.18	0.09		
18	AR7	gain drift	—	—	0.25	0.25	—	—	0.25	0.25		
19	AR7	input offset V @ 25C	0.44	0.22	0.44	0.22					X	
20	AR7	" drift	—	—	0.02	0.01	—	—	0.02	0.01		
21	AR7	Sample & Hold droop	0.05	0.03	0.05	0.03	0.05	0.03	0.05	0.03		
22	AR8	gain drift	—	—	0.25	0.25	—	—	0.25	0.25		
23	AR8	input offset V @ 25°C	0.44	0.22	0.44	0.22					X	
24	AR8	" drift	—	—	0.02	0.01	—	—	0.01	0.02		
25	AR8	input bias i	0.15	0.08	0.15	0.08					X	
26	AR8	" drift	—	—	0.15	0.08			0.15	0.08		

19

25	ARS	Input bias i	0.15	0.08	0.15	0.08					X			
26	ARS	drift	–	–	0.15	0.08			–	–	0.15	0.08		
27	ARII	Bias	1.7	1.7	1.7	1.7							X	
28	ARII	Output offset	34.6	17.3	34.6	17.3							X	
29	ARII	drift	–	–	1.0	0.5					1.0	0.5		
30	ARIO	gain drift	–	–	0.25	0.25			–	–	0.25	0.25		
31	ARIO	Input offset voltage	0.18	0.09	0.18	0.09							X	
32	ARIO	Drift	–	–	0.04	0.02			–	–	0.02	0.04		
33	ARIO	Input offset i	0.04	0.02	0.04	0.02							X	
34	ARIO	drift			0.02	0.01					0.02	0.01		
35	Bias@ARS	Bias drift	–	–	0.30	0.15					0.30	0.15		
36	Bias@ARIO	Bias drift	–	–	0.50	0.25					0.50	0.25		
37	A/D Conv.	Ref. V. drift		–	0.18	0.18					0.18	0.18		
38	A/D Conv.	Unadjusted error	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3				
39	Xder drive	level error	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25				
		% of Val. Absolute error					0.9	0.8	0.9	4.1				
		% of Val RSS error					0.4	0.4	2.1	1.2				

Note: 1. See figure 5.5 (Conceptual schematic.)
2. Calculations based on signal levels presented in figure 5.6

FIGURE II.1
RECORDER ERROR ANALYSIS

at 25 C and 95 C. The calculations were made in relation to the sample system set up of Figure 5.6 in which a strain bridge is used to measure strains in the range 0 to 4000$\mu\epsilon$.

Both absolute and RSS errors are given - the former would be a worst case while the latter should be closer to the actual error in any measurement situation.

Perusal of the table shows that bias drifts are the major error source and further, that the intentionally added bias voltages (at AR1, AR8 and AR10) as well as the output drift of the switched capacitor filter make up the bulk of the irreducible errors. The latter error might be reduced by providing a temperature sensitive bias at either AR8 or AR10 while the other three sources are strictly dependent on the excellence of the bias source.

This accuracy assessment does not cover errors associated with signal frequency content - the main one being aliasing at the switched capacitor filter. As noted previously, the prefilter (AR8) may require more poles or a degree of tuneability. Aliasing will be covered in Phase II.

The results of the accuracy assessment are promising. The final system should meet the specification requirement.

12.0 COST ESTIMATE

Our preliminary cost estimate for the recorder is $3000 to $3500 each in quantities of 99 and up. The final price will have a strong dependence on the packaging, with the cost of the surface mount and hybrid modules being the major cost drivers.

13.0 CONCLUSION

The study to date leads us to conclude the project goals are realistic. An engineering program in Phase II will result in the recorder system described in the initial solicitation and proposal.

A summary of the program to date, the work completed, and the results obtained is given on the summary page and in the introduction of Paragraph 1.0 of this report.

APPENDIX A: Interim Report
Small-Self-Contained
Aircraft Fatigue Data Recorder

ESPRIT TECHNOLOGY INC.
144-A Mayhew Way, Walnut Creek, California 94596, USA • (415) 947-0400

ESPRIT TECHNOLOGY INC.
N62269-85-C-0716
$49,654.00
COMPETITIVE
A. NEGRI
NAVAL AIR DEVELOPMENT CENTER
CODE 6042, WARMINSTER, PA. 18974-5000

ESPRIT TECHNOLOGY INC.

INTERIM REPORT
SMALL-SELF-CONTAINED AIRCRAFT FATIGUE DATA RECORDER

Cont. No. N02269-85-C-0716
Oct. - Dec. 1985

Submittal Date: January 21, 1986

LIMITED RIGHTS LEGEND
CONTRACT No. N02269-85-C-0716
CONTRACTOR: ESPRIT TECHNOLOGY INC.

This technical data shall not, without the written permission of the above contractor, be either (A) used, released or disclosed in whole or in part outside the Government, (B) used in whole or in part by the Government for manufacture, or (C) used by a party other than the Government. This legend shall be included on any reproduction of this data, in whole or in part.

The design information contained herein is the sole property of ESPRIT Technology Inc. and the disclosure of this information does not constitute the release of the proprietary rights thereof.

TABLE OF CONTENTS

1.0 Introduction/Summary

This interim report describes the work carried out on contract N62269-85-C-0716 from October, 1985 through early January, 1986. The intent of the report is to apprise the sponsor of the progress to date and to solicit comments from the sponsor on the report content and the direction the design is taking.

The initial design study has turned up no technical problems precluding attainment of the design goal. We have no reason to believe a Phase II effort will not culminate in creation of a small, battery powered data recorder configured to support operational surveys of military aircraft.

Each paragraph of the report covers a specific segment of either a design task or program element. Although some tasks and elements remain to be completed, short paragraphs have been included to illustrate the form planned for the final report.

The early stages of the design effort have been particularly directed at circuits (paragraph 5), component selection (paragraph 6), power sources (paragraph 8) and the data system (paragraph 10). A brief summary of the design approach follows.

The recorder is powered by lithium batteries. The final design includes a small DC-DC converter to provide for use of various battery chemistries to cover different temperature ranges of operation. The power supply system contains a vibration transducer and associated circuitry to activate and deactivate the recorder according to whether the aircraft is in use or not. Two main and two auxiliary data channels are included. The main channels interface with most transducers of interest since their input circuits are classic high impedance, high CMR instrumentation amplifiers. The system is designed to drive strain based transducers with switched current sources run at a low duty cycle to limit power consumption. The analog chains of the two main channels consist of an input amplifier, a synchronous demodulator, a post demodulation pre-sampling filter combination, a switched capacitor low pass filter, a smoothing filter and an output amplifier. The channel gain, offset and bandwidth are under software control. The available bandwidths range from 2.5 Hz to 50 Hz and are set by the clocking of the 4th order, low pass, butterworth switched capacitor filter. The auxiliary channels are included to provide for event monitoring (e.g. catapults and arrests) and simple two wire transducer temperature monitoring. The conditioned analog signals are digitized by an 8-bit, successive approximation converter that has a built-in four channel analog multiplexer. The digital portion of the recorder has a CMOS microcontroller and CMOS memory - the latter being UV EPROM to contain the operating system and counting algorithms and static RAM for data storage. The software includes provisions for controlling the aforementioned gains, offsets and bandwidths as well as for selection of the desired counting algorithms. The counting

algorithms provide for load level, peak-valley or rainflow counting of the physical parameter being monitored.

Expanded descriptions of the design approach are given in the body of the report with the main content lying in paragraphs 5, 8 and 10.

2.0 System Description

The system being designed has two major components, the airborne system and the ground support system, each of which can be considered to be made up of two or more subcomponents.

The airborne system includes the recorder and the transducer set. The recorder is completely self-contained and self-powered; it includes a power source, a microcomputer, program memory, data memory, a digitizer, analog signal conditioners, a power control transducer and associated circuitry and at least one accelerometer. The transducer set includes any strain based transducer of reasonable input impedance and bridge-like circuitry. Pressure, acceleration and strain transducers are presumed to be of the greatest interest. Current source temperature sensors or medium to high impedance resistance thermometers could also be handled.

A desktop computer, computer interface and master program disk comprise the ground based system. Virtually any small desktop computer would suffice to handle the recorder programming, data retrieval and data transcription tasks assigned to the computer. An IBM compatible unit appears to offer the greatest flexibility. The computer interface assures that the handshake protocol and logic voltage levels between the computer and the recorder serial interface are compatible. The system master disk contains the algorithim menus and user interactive software.

Although not strictly a system component, an operation manual is also required for user support.

3.0: Specification

The initial design studies lead us to make some minor adjustments to the original design goal specification. The updated specification is included below with changes or additions indicated by an asterisk.

Design Goal Specification

General: The equipment shall be a self-contained, self-powered data recorder capable of monitoring a variety of environmental transducers. The recorder shall perform preliminary data reduction/compression and store the results in non-volatile memory for later retrieval.

Size: 1" x 2" x 4" maximum volume (See Figure 3.1)

Mounting: To mounting pads. Mounting pads bonded or bolted to the aircraft. (See Figure 3.1)

*Power: Supplied by internal batteries. Minimum 1 month supply per battery set.
Projected - 3000 mah batteries to support up to 100 hours of data gathering and one month or more of untended installation.

Power Control:
a) CMOS static RAM, continuously supported.
b) Other circuitry activated and de-activated by turn-on circuit sensitive to engine vibrations.
c) In flight-algorithms designed to utilize CMOS processor standby and wait states.

Data Channels: Two channels max plus 2 event counts (e.g. count of catapults and arrests.)

*Channel Bandwidths: Up to 50 Hz (one channel system)
Up to 20 Hz (two channel system)
2.5 Hz minimum bandwidth

Bandwidth Control: By software.

Conversion Resolution: 8 bits

Conversion Type: Absolute or ratiometric

Data Compression: Choice of a) level classification (exceedance count).

b) peak valley pairs.
c) simple rainflow.

Compression Control: By software.

*Data Format:
a) level classes - up to 32 (over 16 x 10^6 counts per level.)
b) Peak valley pairs - up to 32 x 32 peak-valley matrix (496 cells, up to 2 bytes per cell, 65 x 10^3 counts per cell).
c) Rainflow - up to 32 vector magnitudes and starting values. 65 x 10^3 counts per magnitude)

(cell sizes for (b) & (c) can be doubled for data bandwidths above 20 Hz.)

Data Memory: 2K x 8 CMOS static RAM.

Data Retrieval: Module removed from aircraft and transported to Transcriber (commercial microcomputer, e.g. an IBM PC plus associated interface hardware). Data transfer through a serial port and software UART.

Transducer Location: Options for internal or external mounting.

Transducer Types:
Internal - Acceleration, strain or pressure; all strain type devices.
Temperature; two-terminal IC device.
External - General environmental transducers.

Transducer Power:
Internal - Powered by system.
External - Powered by system if low power device capable of pulsed power operation. Supplementary battery pack or ships power required for high power servo type transducers.

Operation Options: The mode of operation is controlled by software. The transcriber is used to program the recorder. The following features are under software control:

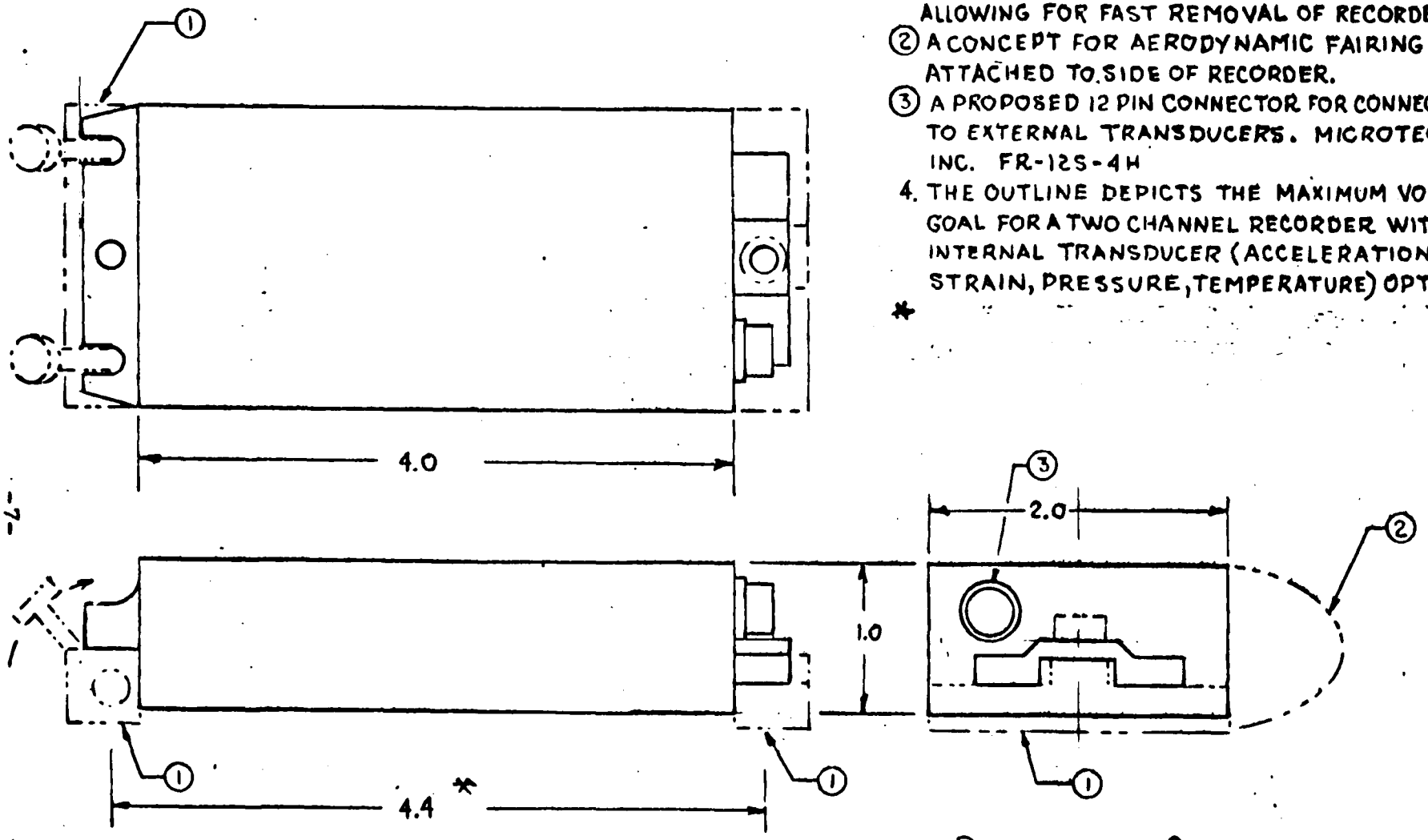
Channel Bandwidth
Channel Ranges
Channel Sample Rate
Data Compression Method
Data Format

System Accuracy: 5% max; 3% design goal.

Design: To meet the intent of MIL-E-5400T Class 3 equipment.

NOTES:

1. PHANTOM LINES DEPICT A MOUNTING CONCEPT ALLOWING FOR FAST REMOVAL OF RECORDER.
2. A CONCEPT FOR AERODYNAMIC FAIRING ATTACHED TO SIDE OF RECORDER.
3. A PROPOSED 12 PIN CONNECTOR FOR CONNECTION TO EXTERNAL TRANSDUCERS. MICROTECH INC. FR-12S-4H
4. THE OUTLINE DEPICTS THE MAXIMUM VOLUME GOAL FOR A TWO CHANNEL RECORDER WITH INTERNAL TRANSDUCER (ACCELERATION, STRAIN, PRESSURE, TEMPERATURE) OPTIONS.



PRELIMINARY OUTLINE
SELF CONTAINED FATIGUE DATA RECORDER
FIGURE 3.1

4.0 Packaging

Conventional discrete component/printed circuit board packaging does not provide the volumetric efficiency required to meet the package volume goal.

We plan to use a combination of hybrid and surface mount technology. The Electronic Designs EDH6687C31 μPAK shown in exhibit 6 to paragraph 5 is an example of a practical approach to packaging. The device is essentially a surface mount module with the major I.C's in chip carriers being mounted to a ceramic substrate (i.e. surface mount) with the subassembly then being finished as a "standard" 40 pin DIP for mounting in conventional P.C. boards.

The EDH6687C31 meets some of the criteria we have set for packaging. First, it provides a major system component (the digital subassembly) as a module and second it illustrates the availability of external vendors to perform this type of assembly. The latter is important - we do not propose to emphasize high volume, capital intensive manufacturing within our company but rather prefer to concentrate on system assembly and engineering design.

In addition to the modular surface mount technique described above, we are also considering true hybrids. Exhibit 1 to this paragraph is an example of a microcomputer built as a true hybrid. This device, the White Technology Inc. DHC8-P85 is very attractive - note the -55 C to +200 C operating temperature range - but may require too much power for the present application. It does, however, exhibit the availability of hybrid technology for our application - in fact White Technology Inc. will do custom designs.

Hybridizing is more costly, both for the initial design and for the production, than is modular surface mount. As we move into the conceptual package design, modular surface mount will be considered as first choice.

Our packaging approach will thus be to design a system made up of major subassemblies, each of which is a surface mount module.

Package Mounting

We plan to mount the package as described in the original proposal. (See also paragraph 3.0)

The package will mount to blocks that are attached to the airframe. The mounting will be with self-locking quick disconnects to provide for simple exchange of recorder modules. In addition, the recorder package will be designed with an expansion joint to prevent build-up of shear stress at the interface of the mounting blocks and the airframe.

The blocks will be bolted or cemented to the airframe. A precedent exists for cementing in the mounting of the Leigh Instruments MSR strain recorder currently in use in a number of military aircraft. An example of an adhesive used for this purpose is included as exhibit 2 to this paragraph.

Detailed instructions for cementing the blocks to the airframe must be developed and included in the recorder operating instructions.

EXHIBIT 1

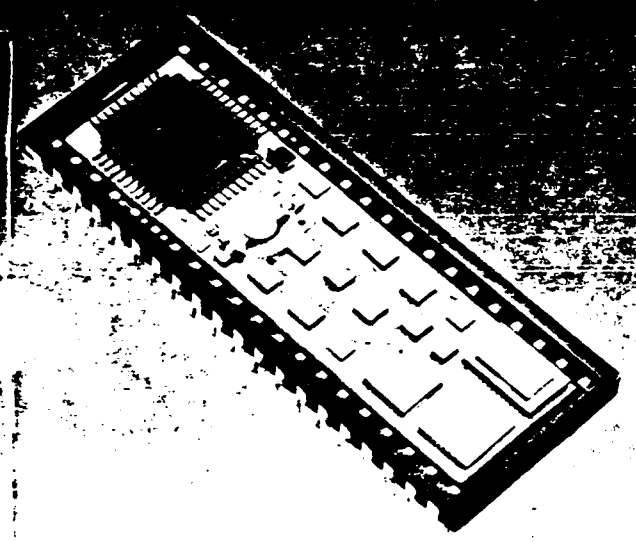
The White Technology Inc.

DHC6-P65

White Technology, Inc.

8-BIT MICROCOMPUTER SYSTEM

DHC8-P85



- Oscillator & Crystal in Package
- Full 8085 Instruction Set
- 2K Byte Static RAM
- 2K Byte CMOS ROM
- Hardware UART (50 to 9600 Baud)
- Built-In Power-On Reset
- Direct Operation of Terminal With Built-In Monitor—RS232 at 9600 Baud
- Low Power Hibernate Mode

DESCRIPTION

The White Technology DHC8-P85 is a high performance 8 bit microcomputer arranged around a CMOS 8085 microprocessor. Also contained in the 40 pin ceramic package is a 14.74559 MHz crystal clock oscillator with the crystal contained within the package. Communication with virtually any RS-232 compatible terminal is provided for using a Programmable Asynchronous Communication Interface (PACI). Initial program storage is accommodated with an internal 2K byte CMOS ROM and program data is stored in the internal 2K byte CMOS static RAM. All output lines and many input lines are buffered with high speed, high current drive CMOS 3-state buffers.

White Technology has sought to satisfy a wide range of high performance microcomputer needs for Oil Logging, Engine Instrumentation and other Hostile Environments. The dense thick film multilayer substrate interconnects over 17 IC's in a standard 40 pin ceramic package.

White Technology has enhanced the quality and reliability by manufacturing and processing the units with the HE-1 Hostile Environment quality and reliability specification. Included are rigorous inspections, tests and reliability evaluations to assure the users that the finished assemblies are suitable for operation in some of the more severe applications.

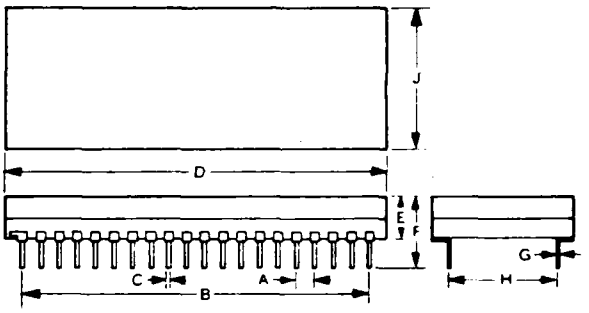
The DHC8-P85 is the core module of the DHC8 family. Other members include RAM, ROM, I/O and DATA ACQUISITION modules. The members of the family are intended to be interconnected readily with little design effort to realize a wide variety of data acquisition and process control functions. The widely used 8085 series microprocessor bus was chosen as the main communication link between the various modules. Most modules feature address/data demultiplexing and address decoding to reduce the system device count.

White Technology, Inc.
4246 EAST WOOD STREET • PHOENIX, ARIZONA 85040
TEL: 602-437-1520 • TWX: 910-951-4203

Printed in U.S.A.

Specifications (-55°C to +200°C)					
Symbol	Parameter	Min.	Max.	Typ.	Unit
$V_{CC(OP)}$	Supply Voltage (Operating)	4.75	5.0	5.25	Vdc
$V_{CC(SB)}$	Supply Voltage (Stand-By)	3.5	—	7.0	Vdc
$I_{CC(OP)}$	Supply Current (Operating)	—	35	—	mA
$I_{CC(SB)}$	Supply Current (Stand-By)	—	4.0	—	mA
V_{IH}	Input High Voltage	2.0	—	—	Vdc
V_{IL}	Input Low Voltage	—	—	0.8	Vdc
V_{OH}	Output High Voltage	3.0	—	—	Vdc
V_{OL}	Output Low Voltage	—	—	0.4	Vdc
F_{CLK}	CPU Clock Frequency	1.8432			MHz
T_{access}	Memory Access Time from Address Change	—	—	500	nsec
I_{IL}	Input Low Leakage	—	—	100	μA
I_{IH}	Input High Leakage	—	—	100	μA
I_{OL}	Output Low Leakage	—	—	1000	μA
I_{OH}	Output High Leakage	—	—	1000	μA

CASE OUTLINE



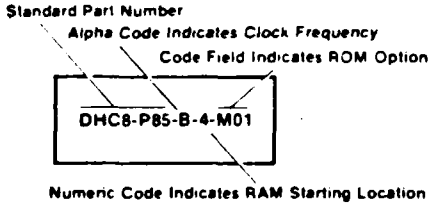
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.095	.105	2 4	2 7
B	1.802	1.908	45 8	48 5
C	.016	.020	0 4	0 5
D	2 074	2 116	52 7	53 7
E	.226	.284	5 7	7 2
F	.395	480	10	12 2
G	008	012	.2	3
H	590	610	15	15.5
J	780	805	19 8	20 4

ORDERING INFORMATION

The variety of options is accommodated during ordering by using the following codes to indicate the user's requirements. If you have any questions or need additional information, please do not hesitate to contact the factory for assistance.

Shown below is the part number for the standard version of the DHC8-P85. The codes following the primary part number are varied to specify various options. The options and their codes are explained in the following paragraphs.

Example:



The DHC8 is the product series designator for the 8 bit modular microcomputer based system.

The P85 designates the core Microcomputer module that executes 8085 code.

The alpha designator ("B" in the example) indicates the optional CPU clock frequency. The options are listed below.

Code	Frequency
A	.92160 MHz
B	1.8432 MHz
C	3.6864 MHz
D	7.3728 MHz

The numeric field ("4" in the example) designates the RAM starting location. Optional starting locations are listed below.

Code	Starting Location
1	800 Hex
2	1000 Hex
3	1800 Hex
4	2000 Hex
5	2800 Hex
6	3000 Hex
7	3800 Hex

The final option field ("M01" in the example) indicates the ROM program. The ROM may be supplied with a standard program developed by White Technology or with one developed by the user. When a user program is installed, a special designator will be assigned to identify the parts. As an option, units may be purchased without ROM for applications where the user wishes to use external RAM and ROM.

Code	Description
Blank	No ROM included, externally connected RAM or ROM
M01	The White Technology Terminal Monitor Program
—	Other codes will be assigned for user developed ROMs, custom and other standard programs.

White Technology, Inc.
4246 EAST WOOD STREET • PHOENIX, ARIZONA 85040
TEL: 602-437-1520 • TWX: 910-951-4203

EXHIBIT 2

Hysol EA9320 Adhesive

HYSOL
AEROSPACE & INDUSTRIAL PRODUCTS DIVISION
P O BOX 312 PITTSBURG CALIFORNIA 94565
415-687-4201

01 November 1985

Mr. Jack Reichel
ESPRIT TECHNOLOGY, INC.
144-A Mayhew Way
Walnut Creek, CA. 94596

Dear Mr. Reichel:

Enclosed is a data sheet for our EA 9320 which you requested. This product is qualified to the following United States Government Specifications:

SM-A-949481
MIS-35827
A3020636
MMM-A-132, Type 1, Class 2

If you have any questions, please do not hesitate to contact me.

Very truly yours,

Jon A. Buffo
Customer Service Supervisor

JAB/mjn

Enclosure

EA 9320
Room Temperature Cure Adhesive With High Shear and Peel Strength

DESCRIPTION

EA 9320 is a two-part, modified epoxy adhesive that is qualified to Federal Specification MMM-A-132, Type I, Class 2 when cured at ambient temperature. Bonds prepared with EA 9320 have high shear and peel strength from —67°F to +200°F. These properties are retained after exposure to salt spray, water and most organic fluids. EA 9320 does contain asbestos.

PROPERTIES

Viscosity at 77°F (Brookfield, HBT for Part A and LVF for Part B, per ASTM D-1824):

Part A — 3,000-6,000 poise, (Spindle #7, 20 rpm).
Part B — 14-16 centipoise, (Spindle #1, 60 rpm).

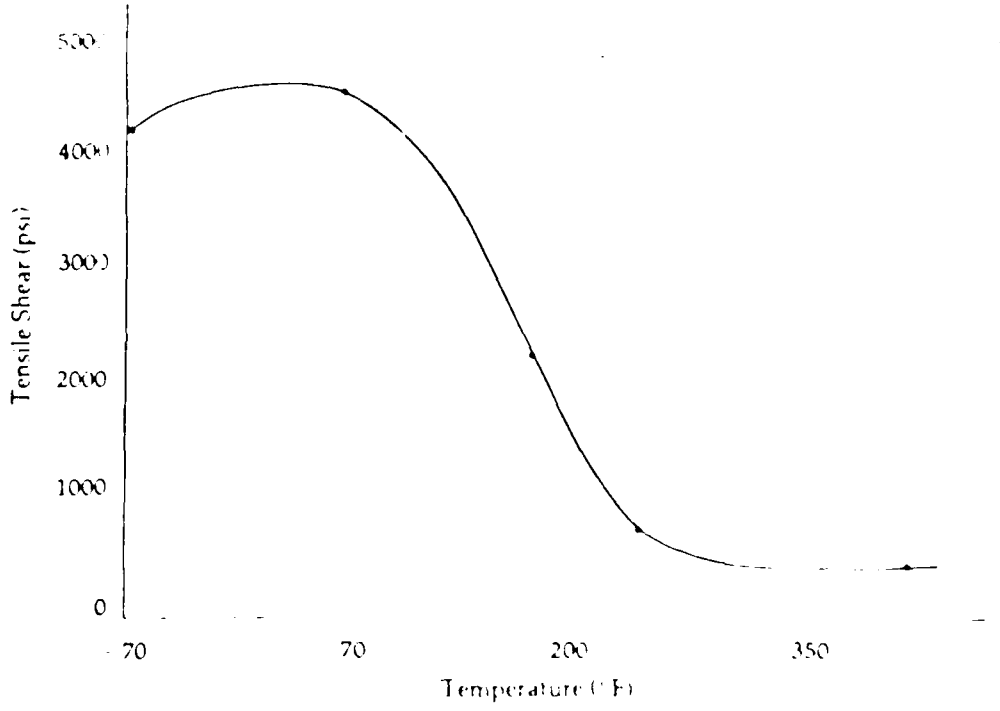
Density, gm/ml:

Part A — 1.5
Part B — 0.98
Cured — 1.10

Shelf Life: Greater than 1 year at 77°F for separate components.

TYPICAL CURED PROPERTIES

Effects of Temperature on Tensile Shear Strength. Chromic acid etched 2024-T3 Alclad, .063 inch, 0.05 inch overlap, one inch wide. Cured for 7 days at 77°F, 10 psi pressure:



Effects of Temperature on Floating Drum Peel Strength: Chromic acid etched 2024-T3 Bare, .025 inch/.063 inch, 0.05 inch wide. Cured for 7 days at 77°F, 10 psi pressure.

Test Temperature:	—67°F	77°F	200°F
Peel Strength, lb/in:	6	55	21

Strength Properties of EA 9320 when tested per MMM-A-132, Type I, Class 2.
Cured for 7 days at 77°F:
Average Test Data is based on 3 lots of EA 9320.

Test Description		Requirement	Test Data
Tensile Shear at	77°F (psi)	2500	4680
	180°F (psi)	1250	2330
	—67°F (psi)	2500	4040
Blister Detection	TS/77°F (psi)	2250	3550
Creep Deflection	77°F (in)	<.015	.0004
	180°F (in)	<.015	.0018
T-Peel	77°F (lb/in)	15	29

Environmental Resistance

7 days Anti-icing Fluid at 77°F		
TS/77°F (psi)	2250	4980
TS/180°F (psi)	——	2400
30 day Distilled Water at 77°F		
TS/77°F (psi)	2250	4440
TS/180°F (psi)	——	1750
7 days Hydraulic Fluid at 77°F		
TS/77°F (psi)	2250	4610
TS/180°F (psi)	——	2300
7 days Hydrocarbon at 77°F		
TS/77°F (psi)	2250	4510
TS/180°F (psi)	——	1430
7 days JP-4 at 77°F		
TS/77°F (psi)	2250	4980
TS/180°F (psi)	——	2400
30 day Salt Spray at 95°F		
TS/77°F (psi)	2250	4510
TS/180°F (psi)	——	1880
30 day 95% RH at 120°F		
TS/77°F (psi)	2250	4650
TS/180°F (psi)	——	1890

Service Temperature: 225°F for 1,000 psi Tensile Shear Strength on etched aluminum.

MIXING

Combine 100 parts A with 19 parts B by weight and mix thoroughly until adhesive is an even blue color.

Pot Life: 25-30 minutes for a 250 gram mass at 77°F.

APPLYING

Surface Preparation: Surfaces to be bonded should be thoroughly cleaned, dried and properly prepared as described in Bulletin G1-100, *Preparing the Surface for Adhesive Bonding*. The use of clean, cotton gloves is recommended to protect the hands from staining and the parts to be bonded from contamination.

A spatula, knife-spreader or roller coater may be used to spread a thin layer of EA 9320 on each surface to be bonded. Assemble parts and hold them together with low pressure (10-30 psi), clamps or weights until the adhesive is cured.

CURING

The cure of EA 9320 may be accomplished at any temperature between 77°F and 250°F. At room temperature, 24 hours is sufficient for quick service although 5 days is recommended for near optimum properties. Cures as short as 15 minutes at 250°F have been effective although longer periods at lower temperatures are recommended.

CLEAN-UP

Excess adhesive must be cleaned up before it hardens. A cloth, or industrial wiper, saturated with alcohol in well ventilated areas works well. Apply just enough to do the job. The part B portion can be cleaned with hot water. Consult solvent container labels for skin and flame warnings.

CAUTION

This product contains asbestos fibers . It may cause skin sensitization or other allergic responses. Avoid inhalation of vapor. Use good ventilation particularly if heated or sprayed. Prevent all contact with skin. If contact occurs, wash immediately with soap and water. This product carries ANSI Classification 2, classified according to *Guides for Classifying and Labeling Epoxy Products According to Their Hazardous Pontentialities*, prepared and published by the American Standards Institute, Inc., 1430 Broadway, New York, New York 10018. See also Bulletin G1-100 *Suggested Precautions for Handling HYSOL Products* and Bulletin G1-100.1 *Suggested Precautions of the Use of Asbestos-Containing Adhesives.*

AVAILABILITY

EA 9320 is available from HYSOL Division, The Dexter Corporation, 2850 Willow Pass Road, Pittsburg, California 94565. Phone: (415) 687-4201. TWX: 910-387-0363.

BULLETIN G1-100

Suggested Precautions for Handling HYSOL Products

HYSOL products are being used successfully as adhesives, sealants and coatings. Since some of these materials may cause dermatitis or eye irritation, a basic understanding of handling techniques is important for their safe use. The major consideration in the control and prevention of this problem is to use the materials with care. Generally speaking, PROPER VENTILATION AND GOOD HOUSEKEEPING ARE ESSENTIAL and prevention rather than cure is the successful approach to handling any chemical products. Always refer to individual product bulletins and container labels for specific handling instructions. The following procedures should also be followed:

VENTILATION

Adequate ventilation should be provided at the point of work to prevent the inhalation of fumes. Fumes should be drawn across the work, away from the operator and vented outside the building. For lighter than air fumes, a hood should be placed in front of the operator rather than overhead. Fumes which are heavier than air will settle to the surface of the work area of floor and should be drawn off at this level. When ventilating hoods are not practical, face masks and other safety divices should be considered.

CLEANLINESS

Care in preventing the unnecessary contact of the materials to skin, clothing and the areas on tools and equipment that require handling cannot be over emphasized. Spillage should be removed as soon as possible and the area washed with alcohol or a recommended cleaner, followed by soap and water. Disposable paper towels and covering for bench tops and work area are suggested as means of preventing accidental spreading of material.

CLOTHING

Employees should wear protective clothing such as coveralls, shop coats or plastic aprons. Contaminated clothing should be removed and laundered before reuse.

PERSONAL CONTACT

Wash hands thoroughly before and after work, before rest periods, lunch and other interruptions, before applying skin creams and putting on gloves and immediately after any material has touched the skin. Use a mild soap without abrasive scrubbers or use a waterless cleaner which is low alkaline or neutral and contains minimum quantities of petroleum solvent or defatting agents.

Do not use irritating solvents to wash skin as they tend to remove the skin's natural oils and can alone cause severe irritation. Over a period of years, however, it has been found that isopropyl alcohol is very effective in the removal of the material from the skin, provided its use is followed by washing with soap and water and then applying lanolin type hand cream. Keep fingernails short and clean. Wear only clean clothing and gloves.

Use protective gloves. Polyethylene bags may also be used to cover parts of the arms. Care should be used in removing either gloves or bags so that the arms and wrists are not contacted. Contaminated articles should be discarded. Special precautions are suggested to prevent contact with the eyes.

The most common cause of rash is careless handling. Determine where and how it was caused and correct it. Occasionally, it is caused by various allergies not connected at all with handling of the materials. If dermatitis does occur, the affected area should not be bandaged as the rash will generally disappear if the person is removed from the work area. If irritation becomes worse, a doctor should be consulted.

In case of eye contact, irrigate eyes immediately with large amounts of water and obtain prompt medical attention.

Excessive concentrations of fumes may cause irritation in the respiratory tract. Should this occur, get the exposed person to an uncontaminated area at once. Call a physician.

PROTECTIVE CREAMS

Barrier creams should be applied to arms, hands, face and neck.

REFERENCES

Guides for Classifying and Labeling Epoxy Products According to Their Hazardous Potentialities published by the American National Standards Institute, Inc., 1430 Broadway, New York, New York 10018.

For urethanes only, see recommendations of *Chemical Safety Data Sheet SD-73, Properties and Essential Information for Safe Handling and Use of Tolylene Diisocyanate* (Revised 1971) published by the Manufacturing Chemists Association, 1825 Connecticut Avenue N.W., Washington, D.C. 20009.

See HYSOL bulletin G1-108, *Handling HYSOL Urethane Products.*

See HYSOL bulletin G1-100.1, *Suggested Precautions for Handling Asbestos-Containing Adhesives.*

HYSOL DIVISION • THE DEXTER CORPORATION

2850 WILLOW PASS ROAD, PITTSBURG, CALIFORNIA 94565 PHONE: 415-687-4201 TWX: 910-387-0363
OTHER U S PLANTS INDIANAPOLIS INDIANA • INDUSTRY CALIFORNIA • SEABROOK NEW HAMPSHIRE • OLEAN NEW YORK
FOREIGN PLANTS HONG KONG LONDON MEXICO CITY MUNICH PARIS TORONTO YOKOHAMA

5.0 Circuits

A preliminary recorder system block diagram is given in figure 5.1. The major system components are:

1. Data Source
   - .(a) Transducer
   - .(b) Transducer drive

2. Power Supply
   - .(a) batteries
   - (b) Power Regulator
   - .(c) Power Control
     - (i) Vibration Transducer
     - (ii) Amplifier/comparator

3. Analog Chain
   - (a) Input Amplifier
     - (i) Gain
     - (ii) Bias
   - .(b) Filters
   - (c) Output Amplifier
   - (d) Auxiliary Channel(s)
   - .(e) A/D Converter

4. Digital Section
   - .(a) Controller
   - .(b) Program Memory
   - .(c) Data Memory

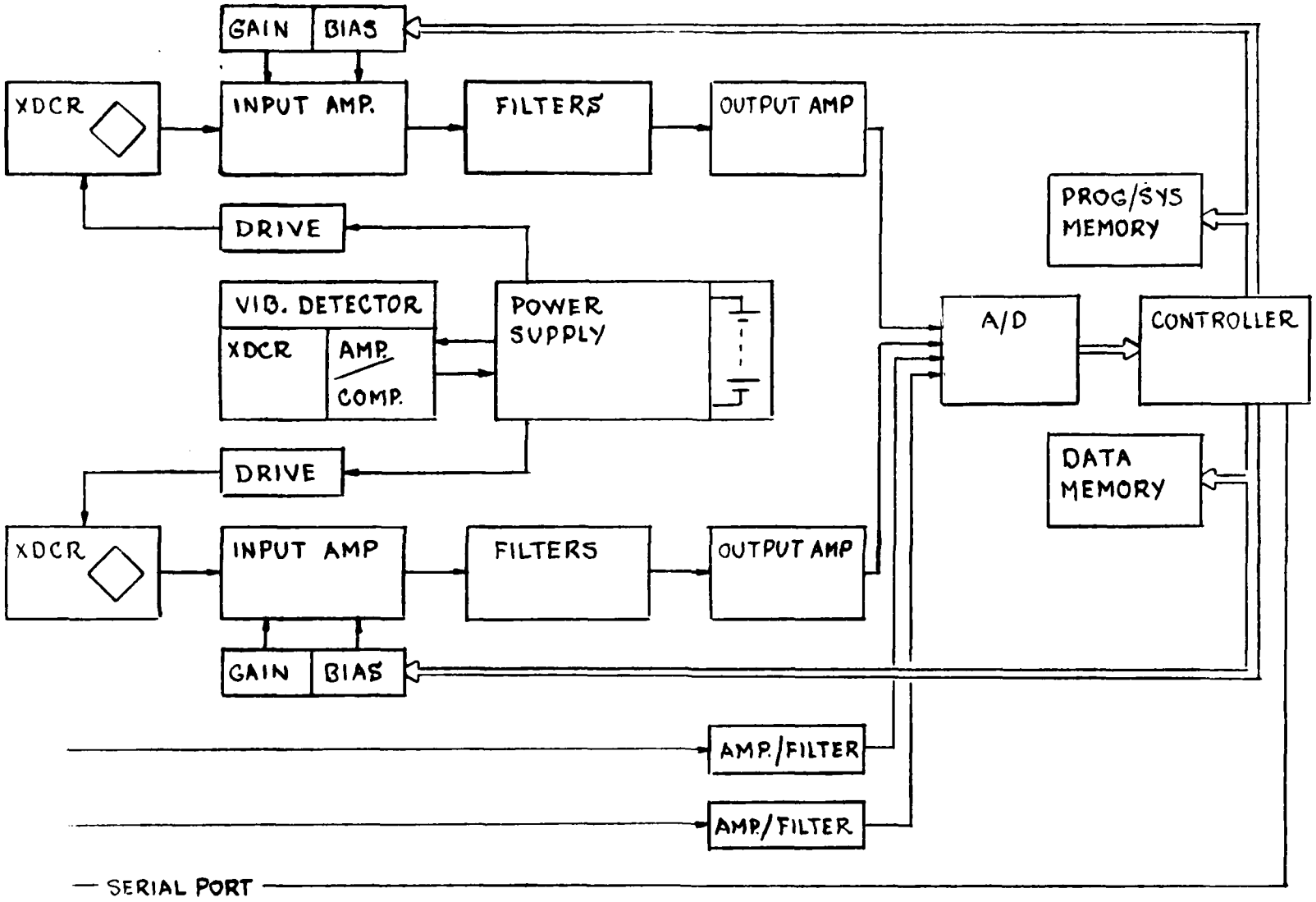
The system components highlighted by . are those that are particularly vital for attaining the design goal. They have received the most attention during the initial design phase.

Data Source

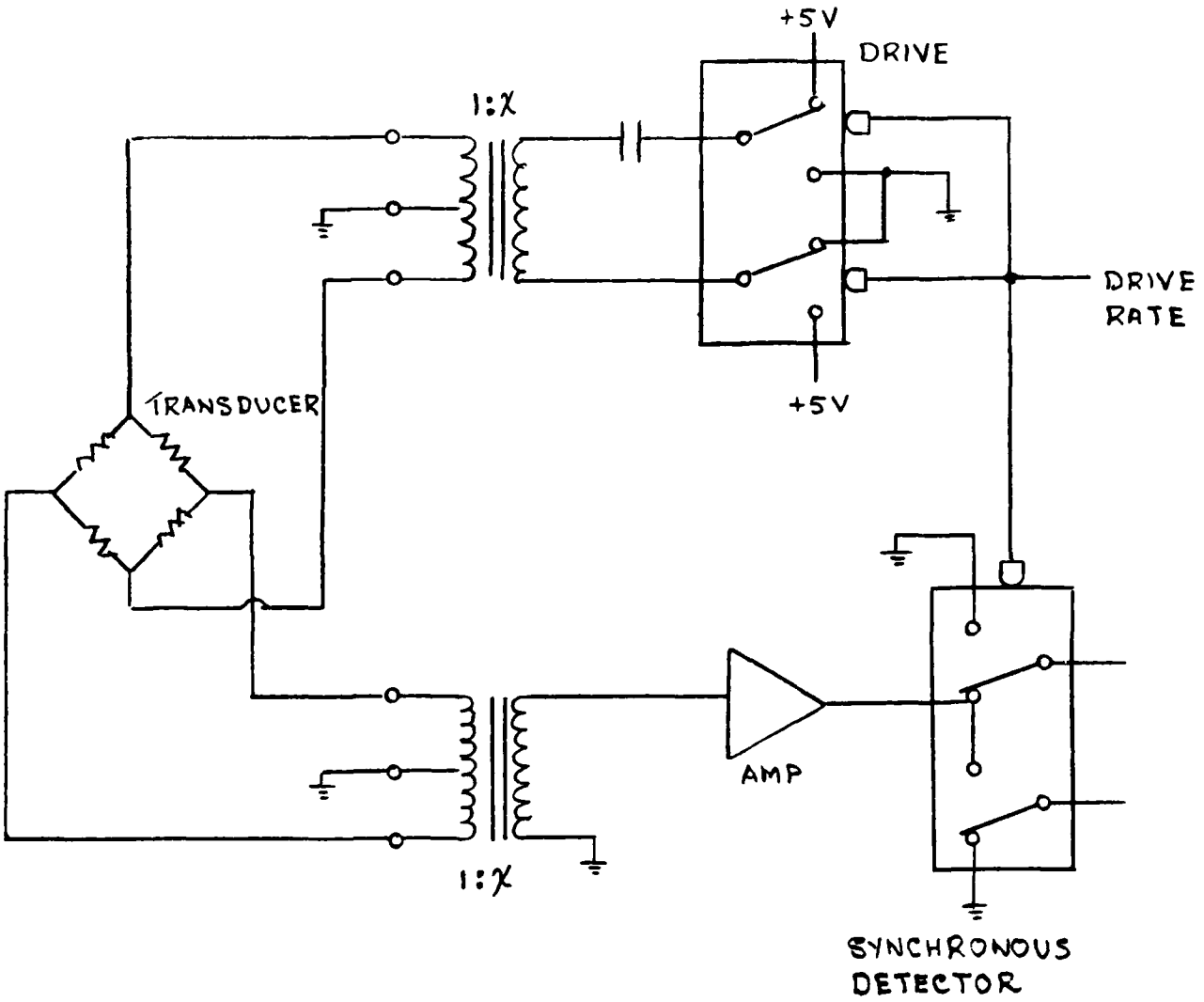
(a) Transducers - The transducers are discussed in paragraph 7.0. In general, the system is designed to utilize virtually any reasonable transducer signal. However, if the system is to provide power to the transducer, the design is currently limited to low power strain based devices - strain gauges or strain gauge pressure and acceleration transducers. Signals from other transducers, deriving their power from some external source, can be used. The auxiliary channels are intended for event counts and two wire temperature measurements.

(b) Design of low power transducer drive systems is one key to attaining low power operation. Two systems, both of which provide pulsed or alternating drive to the transducers, have been studied.

Figure 5.2 shows one scheme being considered; it is an A.C. carrier drive using transformers for an impedance transformation.



PRELIMINARY
SYSTEM BLOCK DIAGRAM
FIGURE 5.1



TRANSDUCER DRIVE

AC WITH SYNCHRONOUS DETECTION

FIGURE 5.2

The system is low power - for example, a turns ratio of 1 to 10 results in a 1 volt peak to peak signal applied to the bridge - roughly a 25 to 1 reduction in power used in the bridge.

The transformer, in addition to performing the impedance transformation (square of the turns ratio), allows a single ended primary side drive and a balanced drive to the transducer which minimizes radiation and stray pickup.

An AC carrier system (1kHz to 10kHz) allows the use of syncronous detection, which has the following benefits:

1. AC amplification of low level signals (no DC offsets).
2. Superior signal to noise performance at low frequencies by avoiding the 1/F noise region (100Hz and below). This is a problem with low power op amps that use low bias current input stages.
3. High degree of quadrature rejection.
4. Operation at higher carrier frequency (e.g. 10kHz) places the signal above most noise sources.

The use of a transformer for the bridge ouput has the following major advantages:

1. The equivalent noise input resistance of a low power op amp is greater than 10k ohms. This is a very poor match to the low impedance of a strain gauge. For example, if the bridge resistance were 100 ohms there would be a 20db reduction in signal to noise ratio due to thermally generated noise.
2. The transformer does the differential to single ended transformation with no power consumption and considerable gain.
3. The transformer provides excellent rejection of common mode noise that is picked up on the leads from the strain gauge.

The switches shown are dual SPDT CMOS switches consuming very little power. Examples are the Siliconix DG307A or the Harris HI-5043.

Some disadvantages associated with this approach are:

1. Extra components such as transformers and switches are required. (Pico F or W series plug in transformers with volumes .013 in and .03 in respectively).
2. A single set of transformers will probably not suffice to drive every type of transducer. Transformers and transducers might have to be matched sets.

The scheme described above provides for low power operation by increasing the apparent impedance of the transducer as seen by the source. The second scheme being considered attains low power average drive through duty cycle control of the transducer excitation. The objective of the second scheme is to obtain a

higher useable signal at the transducer output with no additional power cost.

Figure 5.3A shows a voltage doubler circuit using capacitors and diodes. The doubler is described in exhibit 1 of this paragraph. As an example of the operation, suppose the drive were 5 volts peak into a 350 ohm bridge. The current draw during the "on" drive pulse is $\sim$14 ma and if the pulse widths were 20 μsec on with a basic half cycle time of 100 μsec (20% duty cycle and basic drive frequency of 5kHz) the average drive current is 14/5 $\cong$ 2.8 ma. The output $e_a - e_b$ however (neglecting leakages) is that to be expected from a bridge with 10 volt excitation and 28 ma drive. Since the diode forward voltage enters the picture, the diodes have to be matched over temperature to minimize errors. Figure 5.3B shows the same circuit with the diodes replaced by a synchronous switch set.

The advantage of the circuit is of course the "high" signal from the bridge - it meets the objective in that respect. Also - as opposed to the first circuit - no transformers are required. The diode doubler has been breadboarded and tested with a strain gauge accelerometer and 100% duty cycle drive.

A major disadvantage of this approach is the bipolar drive which will require extra circuit components. Also note that the input amplifier may not be "best" for all transducer types as it is not configured as a true instrumentation amplifier.

The drive circuit of figure 5.3C is the simplest of those discussed so far. The basic transducer input interface is ordinary - a straight run into a standard instrumentation amplifier. The interface will work with virtually any transducer. The drive system is unipolar and thus not as complex as the drive for the doubler circuits.

We will use a drive circuit similar to that shown in figure 5.3C in the prototype hardware unless further analysis and testing dictates otherwise. The continuing design effort will center on this circuit with the drive being a switched current source and the demodulator a synchronous sample and hold system with a post sample filter.

Power Supply

(a) Batteries - The batteries are discussed in paragraph 8.0 of this report.

(b) Power Regulator - As noted in paragraph 8.0 we propose to use series regulators in the prototype hardware. The final unit will have a DC-DC converter configured to cover various input voltages (e.g. 1.5 to 4 volts) to allow for use of various battery chemistries.

(c) Power Control - Power control is the key to attaining the one month installation/100 hour operation goal. The basic

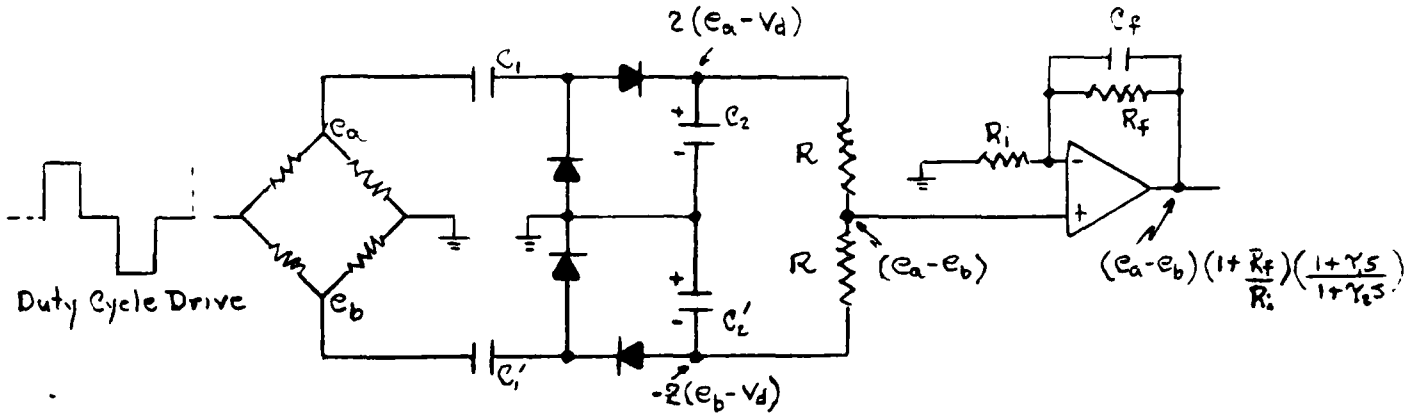
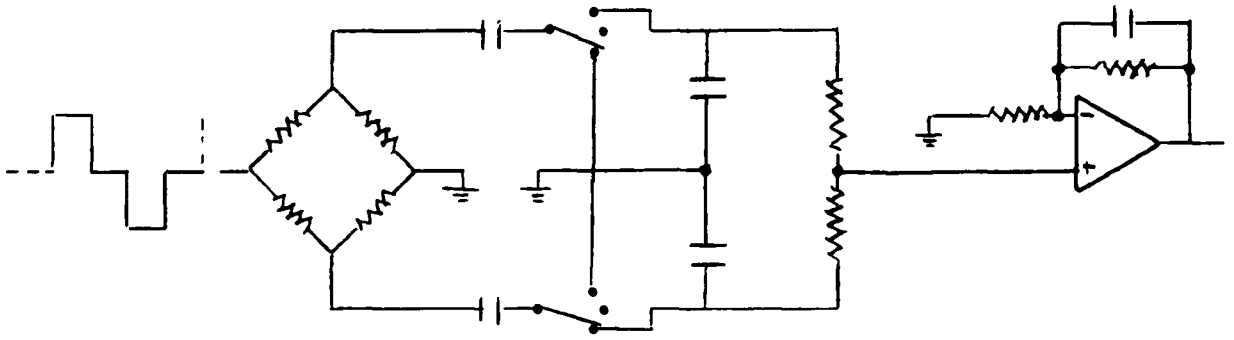


FIG. 5.3A
VOLTAGE DOUBLER



Same as 5.3a with diodes replaced by Synchronous switch.

FIG. 5.3B
VOLTAGE DOUBLER

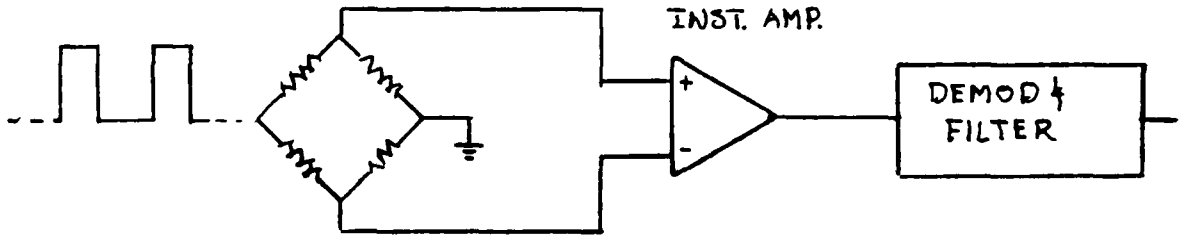


FIG. 5.3C
DIFFERENTIAL INPUT

approach is to sense aircraft ambient vibration when the engines are on and use that sense to switch on the main power to the system.

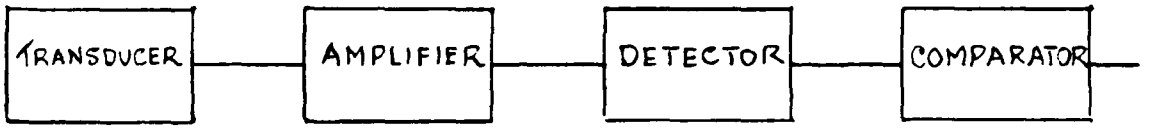
Our plan is to provide a vibration sensor driving an amplifier/comparator combination whose output, 1 or 0, controls the main power supply. We expect to exhibit the basic system in the prototype and fine tune the design in Phase 2 of the program.

At present we have only cursory knowledge of the vibration amplitude and spectrum to be expected. Our queries to one manufacturer of transducers who has run engine vibration studies were only partially successful. General information such as 50 to 250 Hz basic rotating frequencies was all they could offer as they had no experience monitoring engine vibrations at spots not in the immediate vicinity of the engines.

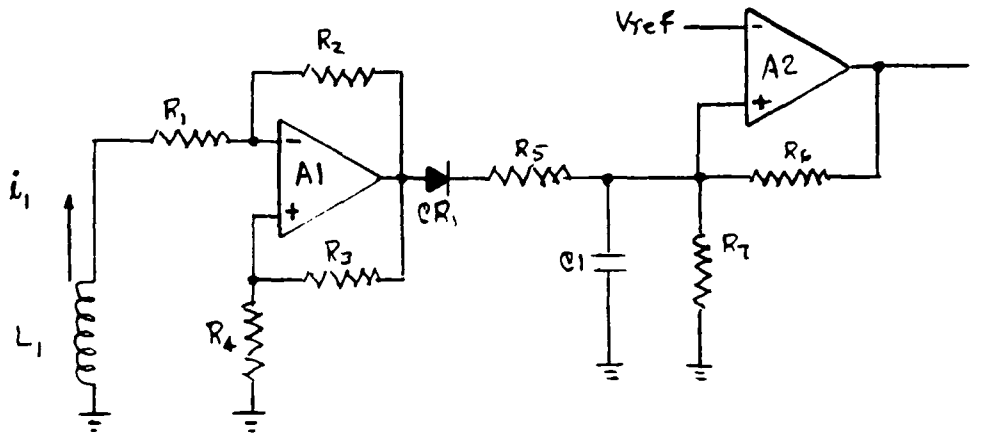
We believe some field testing will probably be required in Phase 2 to garner further information on vibration amplitude and spectral content. There may, however, be other viable sources of this information that remain to be traced. A look at table 514.2-11A of MIL-STD-810B or table 514.3-111 of MIL-STD-810C leads one to believe the formulae and criteria for calculating expected vibration levels could not have been developed without some detailed knowledge of actual aircraft vibrations. There must be a government agency with the requisite information. Another source would be the air frame manufacturers albeit each would presumably only have information on a particular aircraft.

The design approach is shown in figure 5.4. A transducer, amplifier, detector and comparator comprise the subsystem. (see figure 5.4a) The amplifier provides an amplified A.C. transducer signal to the detector. The detector rectifies the signal and provides the initial system time delays (see below). When the rectified signal reaches a preselected level the comparator output switches from 0 to 1 which signal is then used to apply full power to the system. The comparator has a built in hysteresis to prevent "chatter" in the logic output.

The power control system has four time delays associated with applying and removing system power. Two are built into the detector circuit and two are handled by the system software. The objective is to use time and signal level as criteria for power and signal monitoring control. The voltage level at the detector output is delayed by an RC time constant at the onset of vibration. When a 1 from the comparator turns on the system power the controller senses power on, resets and runs through a power on routine. This latter routine contains a time delay that prevents signal monitoring for x seconds after the comparator 1. One time delay at turn on delays power application while the other



VIBRATION DETECTOR
SUBSYSTEM
FIG. 5.4A



L_1 is the velocity sensor coil

$R_1 - R_4$ Set the gain and damping (damping is prop. to i_1 - Lenz's Law)

CR_1 Provides half wave rectification of the Transducer signal.

$R_5 - R_7$ Set the detector time delays and the system hysteresis.

C1 is the detector filter capacitor

SUBSYSTEM SCHEMATIC

FIG. 5.4B

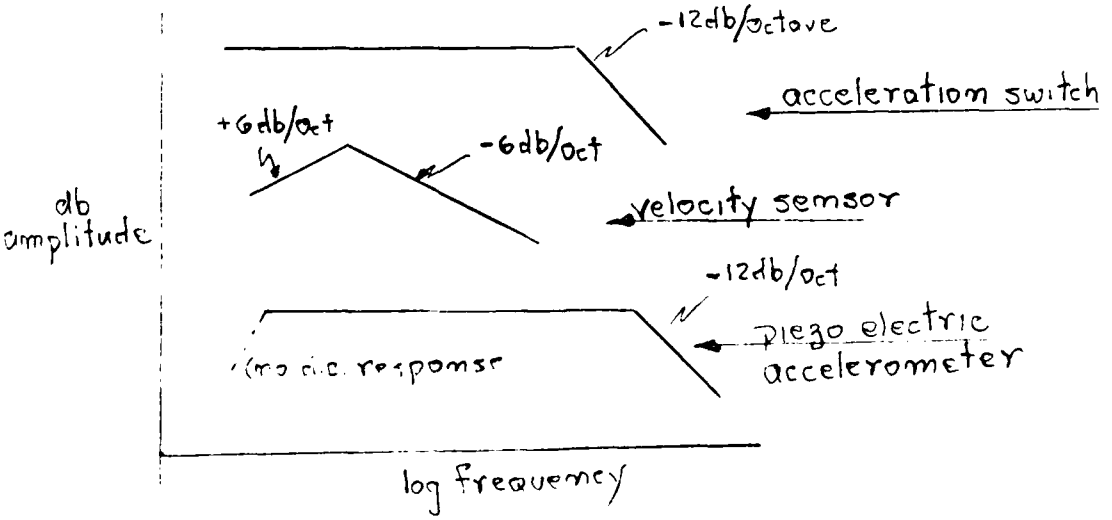
holds off signal monitoring. The idea is to prevent false starts. When the vibration disappears, a time constant in the detector delays the switch to 0 from the comparator while the software adds another delay before going to the power off routine. Here the idea is to prevent false power downs and subsequent possible data loss.

Figure 5.4B illustrates a subsystem using a simple inertial velocity sensor (see below for sensor description). The sensor and A1 provide an AC signal to the detector. Resistors R1 through R4 are sized to provide signal gain and sensor damping. The latter is due to Lenz's law. The current through the coil is caused by the motion (velocity) of the magnet with respect to the coil. The current - by Lenz's law - creates a coil field that opposes the relative motion of the coil and magnet. The opposing force is proportional to the relative velocity; i.e. a velocity dependent damping force.

The detector is a simple half wave diode rectifier with filter capacitor. The resistors are used to set circuit time constants and comparator hysteresis.

Three different transducers for vibration monitoring have been investigated: (1) a vibration switch, (2) piezo-electric accelerometers, and (3) a velocity sensor. The first two are commercially available while the last is an ESPRIT design.

Any of the three types of transducers should suffice to detect airframe vibrations and thus control the power application. Viewing them as black boxes, they differ only in their transfer functions and signal characteristics. The vibration switch and piezo-electric device are accelerometers while the ESPRIT design is classified as a velocity sensor. The classification relates to transfer function behavior. Given a constant acceleration amplitude versus frequency the three transducers will respond as shown below (amplitude response).



The acceleration switch will respond to steady state accelerations and then behaves as a simple spring mass system with a response out to some natural frequency with a response roll off of -12 db/octave thereafter. Exhibit 2 to this section shows the response of an Aerodyne normally closed acceleration switch. The response is relatively flat out to 3000 Hz - a frequency well above any expected vibrational accelerations in the airframe. To use this switch, the schematic in figure 5.4B would be modified to replace the coil with series resistors and the switch contacts driven by the battery. An alternating signal would result when the switch contact "chattered" due to vibration. Note that Aerodyne ran their test with about 32 μa driving the switch so the steady state, 650 hour power usage would be negligible.

The velocity sensor and piezo-electric accelerometer are self-powered. A system with a velocity sensor is shown in figure 5.4b and the velocity sensor is described more fully in exhibit 3 to this section. The accelerometer has an amplitude response similar to the acceleration switch except that it does not respond to steady state accelerations.

The breadboard hardware will include either the acceleration switch or the velocity transducer. The piezo-electric accelerometer, being the most expensive and largest of the three, will be held in reserve.

Analog Chain

(a) Input Amplifier

Our preference is to provide a true instrumentation amplifier for the input. This approach provides for interface with virtually any transducer. The basic input circuit is shown in figure 5.3C.

Three instrumentation amplifier configurations have been looked at. The amplifier could be: (a) an I.C. low power three operational amplifier classic instrumentation amplifier, (b) an implementation of (a) using three low power op amps and precision resistors, or (c) a switched capacitor input amplifier.

Keeping in mind that channel gain and offset are to be under software control the last implementation offers the simplest solution. Two D/A converters - one for offset and one for gain - will suffice. Linear Technology's technical literature is included as exhibit 4 to this section to illustrate the many applications of their switched capacitor building block.

A switched capacitor building block instrumentation amplifier has two disadvantages that lead us to hold this

approach in reserve. First, the implementation will take up more volume and use more power than the method selected (see below) and second, the capacitive input may preclude the future use of some types of transducers.

The input amplifier we have selected for the breadboard is the National LH0036 micropower instrumentation amplifier. It is a classic three op amp I.C. device requiring 0.4 ma drive over a full -55 C to +125 C temperature range. This is the minimum volume approach.

Channel offset will be provided by feeding the output from a D/A converter to the plus input of the I.C's output amplifier. The offset will be under software control and will provide an offset resolution equal to the channel resolution (as determined by the A/D converter). Channel gain will be provided by switching in gain resistors between the negative inputs of the two input amplifiers. Gain of the LH0036 is determined by: Gain = 1 + 50K/R where R is the gain resistor. A 16 level (2^4) gain resolution is proposed as suitable. This will require four switches and four resistors for each input amplifier. Switches such as the Siliconix DG307A or DG515 will be used.

(b) Filters

The National MF-4 fourth order, low pass Butterworth filter will be used in the breadboard model. This filter has been selected because it offers the simplest software control of bandwidth of any type filter and uses the least volume to accomplish the filtering function.

Both analog and digital filtering have been considered. Although digital filtering is conceptually the least volume approach, it is by no means the simplest. The digital controller can handle the entire system operation and counting algorithm task without floating point multiplication. A general digital filter approach would require the floating point capability - a sophistication overkill for the intended use of the recorder. We therefore looked at a simplified digital filter to emulate a third order Butterworth transfer function. Exhibit 5 to this section shows how the third order Butterworth function is implemented as a state variable filter. Comparing that implementation to the basic Butterworth transfer function one sees the coefficients b_3, b_2, b_1 and b_0 as being 1, 2, 2 and 1 respectively. These coefficients can be handled by simple left and right data shifts in the controller and thus the state variable filter could be emulated without floating point calculations. However, since synthesis of the filter bandwidth is intimately tied in with the data rate (the sampling rate) we do not yet see a simple software control of bandwidth in the digital filter implementation and therefore are planning to use an analog filter.. The study of digital filtering will continue but will not lie in the mainstream of the design effort.

The analog filter could of course be implemented with discrete parts - amplifiers, resistors and capacitors. This approach requires too many components and too much volume if the filter bandwidth is to be under software control. The discrete analog filter is being held in reserve as an alternate to the selected switched capacitor device.

The switched capacitor device is a sampled data system requiring prefiltering to preclude aliasing errors. The system bandwidth will be selectable between 2.5 Hz and 50 Hz upper limits and the corresponding clock rate of the MF4 will be from 250 hz to 5 Khz. The prefilter will be a 2 pole filter tuned to about 62 Hz for signal bandwidths from 2.5 to 25 Hz and to twice that value for signal bandwidths from 25 to 50 hz. Such tuning is a compromise between limiting aliasing errors in the MF4 and attenuation of the signal of interest - in the latter case the aim is to keep the valid data well below the prefilter corner. The prefilter will also act as the post sample filter for the synchronous sampler at the output of the channel 1st stage.

A similar filter will be included at the output of the MF4 to act as a smoothing filter.

(c) Output Amplifiers

A low power amplifier with sufficient bandwidth to drive the A/D converter will be used at the end of the analog chain.

(d) Auxiliary Channels

Our initial design includes the auxiliary channels to provide options for monitoring temperature (two wire transducer) and events such as catapults and arrests. These will be simple unfiltered channels.

(e) A/D Converter

We have provisionally selected the National ADC0844 A/D Converter for the 8-bit conversion. The selection was based on power usage and ease of interface with the controller. This converter has a built in analog multiplexer - another point in its favor since that function then need not be supplied by other components.

Serial converters, such as the TI TLC549, could also be used. These converters use more controller time since the words are read one bit at a time unless additional registers are used. This type of converter is being held in reserve.

Digital Section

The digital section contains the controller, program memory and data memory.

(a) Controller

The Intel MD80C31BH controller has been selected for this system. This CMOS device has a number of features making it attractive for use in small, battery powered systems. As shown in the energy budget, we expect to draw an average of 4.5 ma operating at 3.5 MHz - a very low power device for its features. The controller contains a timer and serial (UART) port - devices that then do not have to be provided with additional discrete parts.

There are a number of CMOS microcontrollers appearing on the market that have been considered for this design. An example is the Motorola 68HC11. This device, an 8-bit machine, has an on chip timer, UART and 8-channel A/D converter. It also contains 512 bytes of EEPROM and has fractional divide and multiply in its instruction set. Some other candidates were the Motorola 68HC805, the Motorola 146805 and the Harris 80C88. The factors leading to selection of the 80C31 were power consumption, design maturity, on chip functions, direct memory addressing capability, military temperature range availability, instruction set features and availability of software support.

Exhibit 6 to this paragraph contains the data sheets for the Electronic Designs Inc. EDH887C31 μPAK device. This microcomputer will be used in the breadboard hardware. It is built around the Intel M80C31BH microcontroller we have selected for the recorder design and includes ample memory to handle program and data storage. The design typifies the packaging approach we plan to follow (see paragraph 4.0).

(b)(c) Memory

The breadboard unit will utilize the memory included in the EDH8087C31 described above. The operating system and counting algorithms will be stored in the 8K x 8 UV EPROM and the data will be stored in the 8K x 8 static RAM.

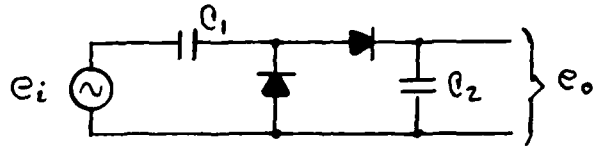
Interestingly enough, we had selected the Intel 80C31 and planned to use UV EPROM and static RAM memory before we discovered the Electronic Designs package. The memory choice was based on power and timing requirements. Although EEPROM would appear as a better choice (simpler to program and absolute data retention) for the recorder design, we know of no available low power devices. In addition, using EEPROM for data storage in real time requires additional software to handle the 2 to 10 msec write time per byte. We note, as indicated in the discussion of battery systems, that one approach to bypassing the write time and power problems would be to store the data in static RAM during the data collection period (the flight) and after the flight (before power shut down) transfer the data to an EEPROM in the recorder. At present this scheme appears to restrict the battery selection and preclude some useful chemistries.

Recognizing that nonvolatile data retention is vital, we plan to continue the memory design study. One concept is to use static RAM and provide a separate data retention battery. The idea is to retain the data even if the system battery runs down. Another possibility is the future appearance on the market of low power, CMOS EEPROM devices. At least one company, XICOR, is planning on introducing CMOS versions of their standard memory chips in the next year or so. These chips would also have reduced guaranteed write times. As these chips become available, the approach described at the end of the preceding paragraph might be followed by placing an energy storage device (a capacitor) between the battery supply and the EEPROM to limit the battery current. This would apply only to the data memory as the program memory obviously operates continuously in real time.

EXHIBIT 1

Voltage Doubler

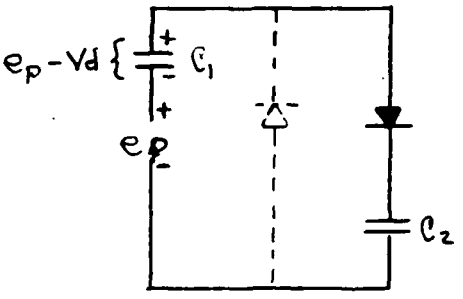
A Simple Voltage Doubler



$e_i = e_p \sin \omega t$; $C_1/C_2 = k$
V_d = diode voltage

During each negative half cycle, C_1 will charge to $e_p - V_d$

1. 1st Cycle - with C_1 charged to $e_p - V_d$, as we reach the positive peak we have - as charge is transferred -



(i) $e_p + (e_p - V_d) - \frac{\Delta Q}{C_1} = \frac{\Delta Q}{C_2} + V_d$

(ii) $2(e_p - V_d) = \frac{\Delta Q}{C_1} + \frac{\Delta Q}{C_2} = \frac{\Delta Q}{C_1}(1+k)$

(iii) $\Delta Q = \frac{C_1}{1+k}[2(e_p - V_d)]$

(iv) $e_{o1} = \frac{\Delta Q}{C_2} = \frac{k}{1+k}[2(e_p - V_d)]$

let $\epsilon = (e_p - V_d)$, $u = \frac{k}{1+k}$

$e_{o1} = 2\epsilon u$

2. 2nd Cycle

(i) $e_p + (e_p - V_d) - \frac{\Delta Q}{C_1} = e_{o1} + \frac{\Delta Q}{C_2} + V_d$

(ii) $2\epsilon - e_{o1} = \frac{\Delta Q}{C_1}(1+k)$; $\Delta Q = \frac{C_1}{1+k}[2\epsilon - e_{o1}]$

(iii) $e_{o2} = \frac{\Delta Q}{C_2} + e_{o1} = \frac{k}{1+k}[2\epsilon - e_{o1}] + e_{o1}$

$= e_{o1} + (1-u)e_{o1}$

3. 3rd Cycle The same as the 2nd Cycle except

(ii) $2\epsilon - e_{o2} = \frac{\Delta Q}{C_1}(1+k)$; $\Delta Q = \frac{C_1}{1+k}[2\epsilon - e_{o2}]$

(iii) $e_{o3} = \frac{\Delta Q}{C_2} + e_{o2} = 2\epsilon u + (1-u)e_{o2}$

$= e_{o1} + (1-u)[e_{o1} + (1-u)e_{o1}]$

$= e_{o1} + (1-u)e_{o1} + (1-u)^2 e_{o1}$

4. The progression is thus of the form

$$e_{om} = e_{o1}\left(1 + (1-u) + (1-u)^2 + \cdots + (1-u)^{n-1}\right)$$

$$= 2\epsilon u \sum_{p=0}^{n-1} (1-u)^p = 2\epsilon \frac{k}{1+k} \sum_{p=0}^{n-1} \left(\frac{1}{1+k}\right)^p$$

This has the form of a geometric progression with common ratio $r = 1/1+k$ which is less than 1

$$\lim_{n\to\infty} e_{om} = 2\epsilon \frac{k}{1+k} \cdot \frac{1}{1-\frac{1}{1+k}} = 2\epsilon$$ thus we have a voltage doubler.

5. What value of k is required if we wish to reach the final value of 2ϵ within 5 parts/1000 (i.e. ½%) within 4 cycles?

$$\text{or } \frac{k}{1+k} \sum_{p=0}^{3} \left(\frac{1}{1+k}\right)^p \geq .995$$

note if $S_4 = 1 + r + r^2 + r^3$

then $rS_4 = r + r^2 + r^3 + r^4$

and $(1-r)S_4 = 1 - r^4$

$$S_4 = \frac{1-r^4}{1-r}$$

with $r = \frac{1}{1-k}$ we have $\frac{k}{1+k} \cdot \frac{1 - \frac{1}{(1+k)^4}}{1 - \frac{1}{(1+k)}} \geq .995$

or $1 - \frac{1}{(1+k)^4} \geq .995$; $\frac{1}{(1+k)^4} \leq .005$; $(1+k)^4 \geq 200$

$1 + k \geq (200)^{1/4} \geq 3.76$

Thus if $k > 2.76$ we reach 2ϵ within ½% in 4 cycles.

Conversely if $k = 2$ how many cycles are required to attain the same result?

$$(1+k)^n \geq 200 \text{ or } 3^n \geq 200$$

$n = 5$ $(3^5 = 243)$

5 cycles are required.

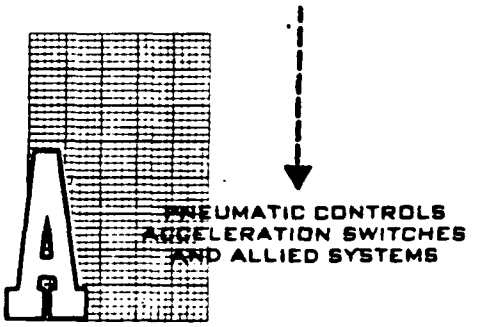
EXHIBIT 2

An Acceleration Switch

Aerodyne Controls Corporation

30 Haynes Court • Ronkonkoma, N.Y. 11779

516-737-1900
TWX 510-220-1137



November 27, 1985

Esprite Technology, Inc.
144-A Mayhew Way
Walnut Creek, CA 94596

Attention: Mr. Phil Flanner
Vice President, Engineering

Subject: Acceleration Switch
Frequency Response Data

Dear Phil,

It was a pleasure meeting with you on October 24, 1985. Thank you for the time you spent with Neil Cooper and me.

Enclosed are two copies of our Document TIS-4675-1, which provides frequency response information on our acceleration switch and two copies of our switch drawing, 4675-1-000 in accordance with your request.

We would like very much to be your supplier for this program and look forward to further discussing your requirements after you have reviewed our report.

Thanks again for meeting with us.

Very truly yours,

AERODYNE CONTROLS CORPORATION

Richard B. Graeb
Director of Sales and Marketing

cp
Enclosures: TIS-4675-1 (2 copies)
Dwg. #4675-1-000

cc: Main Engineering and Marketing Associates

REVISIONS

REV.	DESCRIPTION	CHANGE BY	DATE	APPROVAL BY	DATE

DOCUMENT NO. TIS-4675-1

PROJECT NO. 4675

TECHNICAL INFORMATION SHEET

FREQUENCY RESPONSE TEST

P/N 4675-1-000

N.C., ACCELERATION SWITCH

APPROVAL DATE	PROJECT NO.
PROGRAM APPROVAL 9/27/85	R.F.Q. NO.
RELIABILITY APPROVAL	CONTRACT NO.
Q.C. APPROVAL	CUSTOMER
PROJECT ENG. CR 11/26/85	
CHECKED	
PREPARATION CR 11/26/85	

AERODYNE CONTROLS CORPORATION

30 HAYNES COURT • RONKONKOMA, NY 11779

TITLE: Technical Information Sheet
Frequency Response Test

SIZE	CODE IDENT. NO.	DOCUMENT NO.	REV.
A	14923	TIS-4675-1	
SCALE	WEIGHT	SHEET 1 OF 3	

1.0 PURPOSE

The purpose of the testing was to determine the frequency response of a low g threshold normally closed acceleration switch similar to or 4048/3356 series type acceleration switches. A single development test sample switch, P/N 4675-1-000, acceleration switch, normally closed, was built and tested in the cross-axis direction on 11/18/85 and in the in-line direction on 11/25/85.

2.0 REFERENCES

AERODYNE CONTROLS CORPORATION

Drawing No. 4675-1-000	Acceleration Switch, Normally Closed

3.0 TEST EQUIPMENT AND PROCEDURES

The 4675-1-000 switch was mounted in a test fixture affixed to the vibrator, Ling Dynamic Systems LTD, model V411, Vibrator, S/N 377. The vibrator was driven by sine wave signals from a Hewlett Packard model 3311A Function Generator, amplified by a David Hafler Company, Stereo Power Amplifier, Model DH-220.

An Entran Devices Inc. Accelerometer Model EGC-240-1000D was used to measure vibration amplitude. Both the vibration acceleration and the switch contact state were monitored on a Tektronix T912 Dual Beam Storage Oscilloscope. During vibration scans, the switch contacts were loaded with a 47,000 ohm resistor in series with a 1.5 VDC battery.

4.0 TEST RESULTS

Tabulated below are the results of the vibration scans. Note that during in-line vibration the header end of the test sample switch was up. The "g" values tabulated denote the vibration amplitude at which the switch contacts began to open.

TABLE 1
FREQUENCY RESPONSE
P/N 4675-1-000

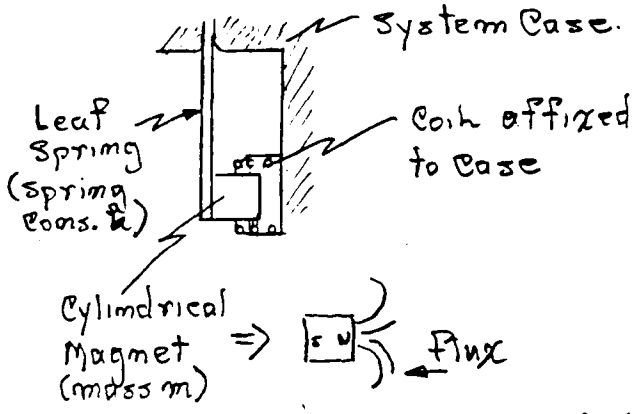
HZ	IN-LINE "g"	CROSS AXIS "g"	HZ	IN-LINE "g"	CROSS AXIS "g"	HZ	IN-LINE "g"	CROSS AXIS "g"	HZ	IN-LINE "g"	CROSS AXIS "g"	HZ	IN-LINE "g"	CROSS AXIS "g"
5	1.2	4.0	80	1.2	2.5	600	1.0	25	1800	1.4	13	5000	1.0	40
8	1.2	4.2	85	1.4	3.0	650	1.0	-	1900	1.2	19	5500	2.4	40
10	1.2	6.0	90	1.4	3.6	700	1.0	25	2000	1.2	21	6000	4.8	40
15	1.2	7.0	95	1.4	3.8	750	1.2	-	2100	1.2	17	6500	2.8	39
20	1.2	4.2	100	1.4	4.0	800	1.2	31	2200	1.2	16	7000	2.6	12
25	1.2	4.0	125	1.4	5.2	850	1.2	-	2300	1.2	12.5	7500	2.6	10
30	1.0	3.8	150	1.4	5.3	900	1.2	25	2400	1.4	7.5	8000	3.4	9
35	1.0	3.8	175	1.2	4.5	950	1.2	-	2500	1.4	10	8500	4.8	34
40	.8	3.5	200	1.0	7.5	1000	1.2	20.5	2600	1.2	38	9000	7.6	40
45	1.0	3.3	250	1.0	9.0	1100	1.2	22	2700	1.2	25	9500	4.8	40
50	1.0	2.6	300	1.0	11.5	1200	1.2	22	2800	1.2	5.5	10,000	4.8	40
55	1.2	2.3	350	1.2	14.0	1300	1.4	28	2900	1.2	18	11,000	3.0	-
60	1.2	2.0	400	1.2	17.0	1400	1.4	16	3000	1.6	22	12,000	2.8	-
65	1.2	2.0	450	1.2	18.0	1500	1.4	8	3500	2.0	30	13,000	7.2	-
70	1.2	2.0	500	1.2	18.0	1600	1.4	16	4000	.8	39	14,000	6.0	-
75	1.2	2.4	550	1.0	24.0	1700	1.4	10	4500	.8	40	15,000	4.4	-

CODE IDENT. NO. 14923
SIZE A
DOCUMENT NO. TIS-4675-1
SHEET 3 OF 3
REV

EXHIBIT 3

Velocity Sensor

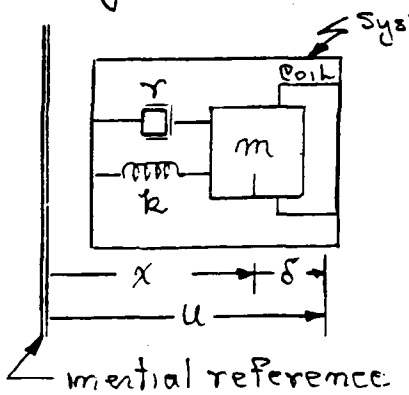
A Simple Velocity Sensor.



A cylindrical magnet mounted on a leaf spring. The magnet lies in a cylindrical coil affixed to the case.

As the system case (mounted on the aircraft) moves or vibrates with respect to inertial space the magnet moves with respect to the coil and a voltage, proportional to the magnets velocity with respect to the coil, is induced in the coil.

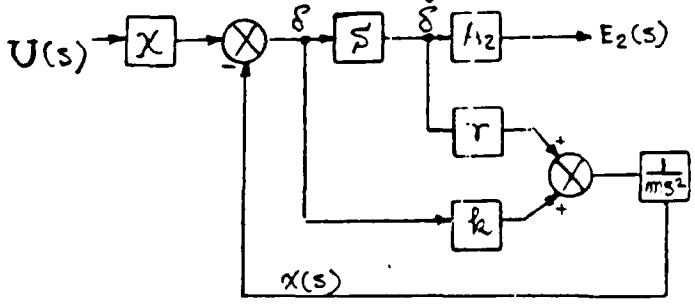
The system can be modeled as below:



r is the damping. (dynes/cm/sec.)
k is the spring constant (dynes/cm)
m is the mass (grams)

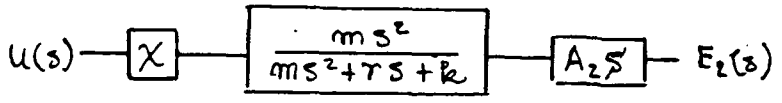
u is the case position with respect to inertial space.
x is the mass position with respect to inertial space.
δ is the relative displacement of the mass and case.

A block diagram transfer function appears as



where s is the Laplace variable

This block diagram can be reduced to



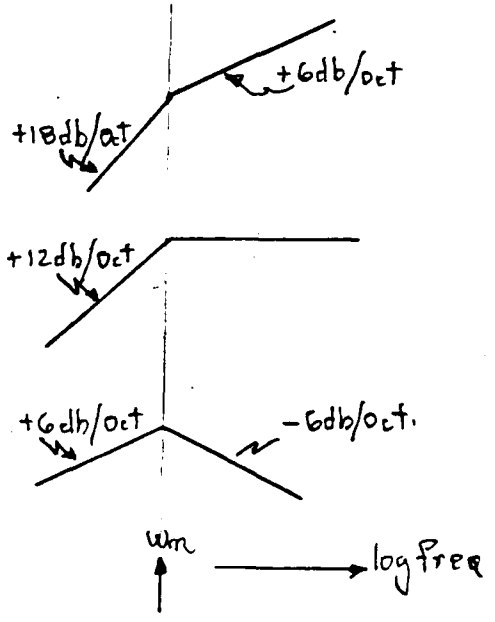
which gives the general transfer function

$$\frac{E_2(s)}{U(s)} = \frac{X \cdot A_2 s^3}{s^2 + \frac{r}{m} s + \frac{k}{m}} = \frac{X \cdot A_2 s^3}{s^2 + 2\zeta\omega_n + \omega_n^2}$$

For constant amplitude position vs freq. in $U(s) = u(s)$ $X = 1$ } Freq. resp

For constant amplitude velocity vs freq. in $U(s) = \dot{u}(s)$ $X = 1/s$ } Freq. resp.

For constant amplitude acceleration vs freq. in $U(s) = \ddot{u}(s)$ $X = 1/s^2$ } Freq resp.



In this system

1. $\omega_n = \sqrt{k/m}$ i.e. $2\pi f = \sqrt{k/m}$ where k is the spring constant (dynes/cm), m is the magnet mass (grams) f is the natural frequency (Hz)
2. r is the damping. It is proportional to the current allowed to flow in the coil. r is (dyne/cm/sec.)
3. $r/m = 2\zeta\omega_n$ where ζ is the damping ratio
4. A_2 is the output section (Volt/cm/sec.). A_2 is dependent on the magnetic field flux density and the number of turns in the coil.

EXHIBIT 4

The Linear Technology LTC1043

Switched Capacitor Building Block

LTC1043

Dual Precision Instrumentation Switched-Capacitor Building Block

FEATURES

- Instrumentation Front End with 120dB CMRR
- Precise, Charge-Balanced Switching
- Operates from 3V to 18V
- Internal or External Clock
- Operates up to 5MHz Clock Rate
- Low Power
- Two Independent Sections with One Clock

APPLICATIONS

- Precision Instrumentation Amplifiers
- Ultra Precision Voltage Inverters, Multipliers and Dividers
- V–F and F–V Converters
- Sample and Hold
- Switched-Capacitor Filters

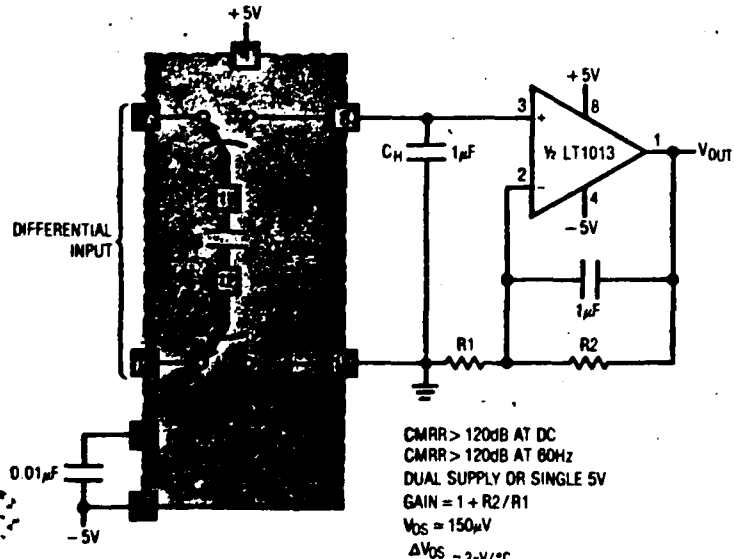
DESCRIPTION

The LTC1043 is a monolithic, charge-balanced, dual switched-capacitor instrumentation building block. A pair of switches alternately connects an external capacitor to an input voltage and then connects the charged capacitor across an output port. The internal switches have a break-before-make action. An internal clock is provided and its frequency can be adjusted with an external capacitor. The LTC1043 can also be driven with an external CMOS clock.

The LTC1043, when used with low clock frequencies, provides ultra precision DC functions without requiring precise external components. Such functions are differential voltage to single-ended conversion, voltage inversion, voltage multiplication and division by 2, 3, 4, 5, etc. The LTC1043 can also be used for precise V–F and F–V circuits without trimming, and it is also a building block for switched-capacitor filters, oscillators and modulators.

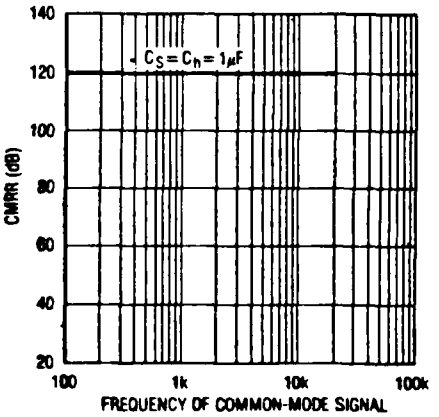
The LTC1043 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

Instrumentation Amplifier



CMRR > 120dB AT DC
CMRR > 120dB AT 60Hz
DUAL SUPPLY OR SINGLE 5V
GAIN = 1 + R2/R1
V_{OS} = 150μV
$\frac{\Delta V_{OS}}{\Delta T}$ = 2μV/°C
COMMON-MODE INPUT VOLTAGE INCLUDES THE SUPPLIES

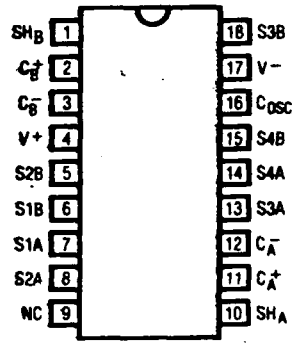
CMRR vs Frequency



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Input Voltage
at Any Pin ..... $-0.3V \leq V_{IN} \leq V^+ + 0.3V$
Operating Temperature Range
LTC1043C ..... $-40°C \leq T_A \leq 85°C$
LTC1043M ..... $-55°C \leq T_A \leq 125°C$
Storage Temperature Range ..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1043CN LTC1043MD

ELECTRICAL CHARACTERISTICS

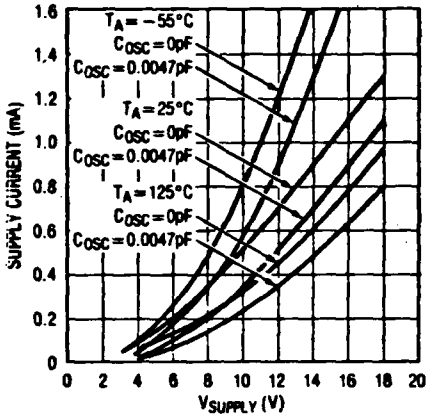
$V^+ = 10V$, $V^- = 0V$, $T_A = 25°C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1043M MIN	LTC1043M TYP	LTC1043M MAX	LTC1043C MIN	LTC1043C TYP	LTC1043C MAX	UNITS
I_S	Power Supply Current	Pin (16) Connected High or Low			0.25	0.4		0.25	0.4	mA
			●			0.7			0.7	mA
		C_{OSC} (Pin 16 to V^-) = 100pF			0.4	0.65		0.4	0.65	mA
			●			1			1	mA
I_I	OFF Leakage Current	Any Switch, Test Circuit 1			6			6		pA
			●		6	500		6		nA
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 7V$, $I = \pm 0.5mA$ $V^+ = 10V$, $V^- = 0V$			240	400		240	400	Ω
			●			700			700	Ω
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 3.1V$, $I = \pm 0.5mA$ $V^+ = 5V$, $V^- = 0V$	●		400	700 1		400	700 1	Ω kΩ
f_{OSC}	Internal Oscillator Frequency	C_{OSC} (Pin 16 to V^-) = 0pF			185			185		kHz
		C_{OSC} (Pin 16 to V^-) = 100pF Test Circuit 3		20	34	50	20	34	50	kHz
			●	15		75	15		75	kHz
I_{OSC}	Pin Source or Sink Current	Pin 16 at V^+ or V^-			40	70		40	70	μA
			●			100			100	μA
	Break-Before-Make Time				25			25		ns
	Clock to Switching Delay	C_{OSC} Pin Externally Driven			75			75		ns
f_M	Maximum External CLK Frequency	C_{OSC} Pin Externally Driven with CMOS Levels			5			5		MHz
CMRR	Common-Mode Rejection Ratio	$V^+ = 5V$, $V^- = -5V$, $-5V < V_{CM} < 5V$, DC to 400Hz			120			120		dB

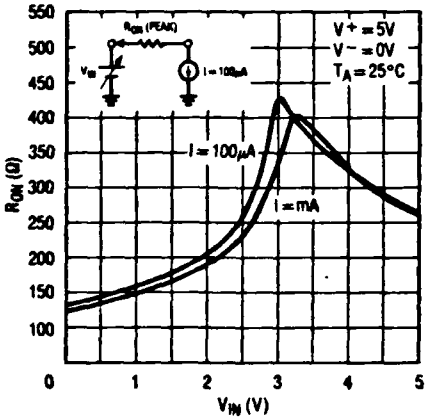
The ● denotes the specifications which apply over the full operating temperature range: LTC1043M operates from $-55°C \leq T_A \leq 125°C$, LTC1043C operates from $-40°C \leq T_A \leq 85°C$.

TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

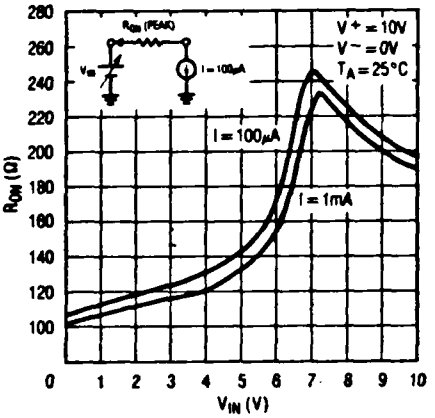
Power Supply Current vs Power Supply Voltage



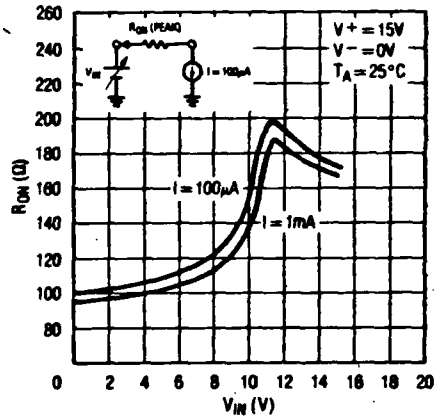
RON vs VIN



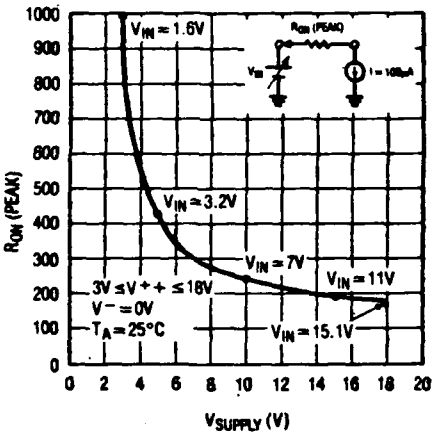
RON vs VIN



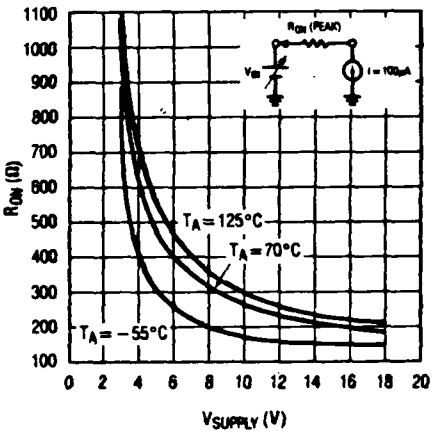
RON vs VIN



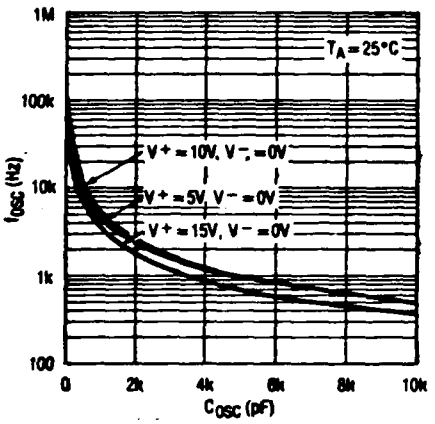
RON (Peak) vs Power Supply Voltage



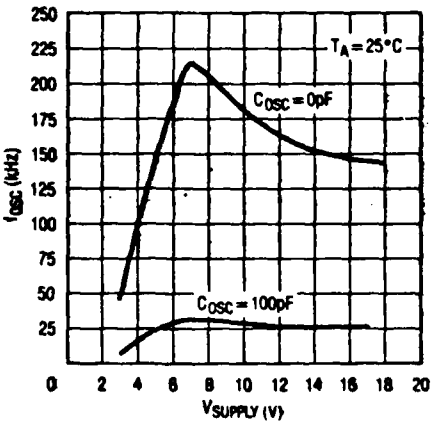
RON (Peak) vs Power Supply Voltage and Temperature



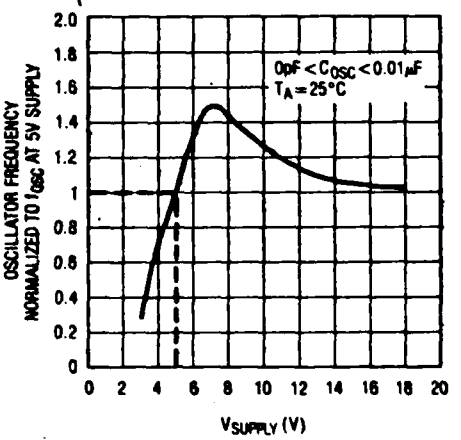
Oscillator Frequency, fOSC, vs COSC



Oscillator Frequency, fOSC, vs Supply Voltage

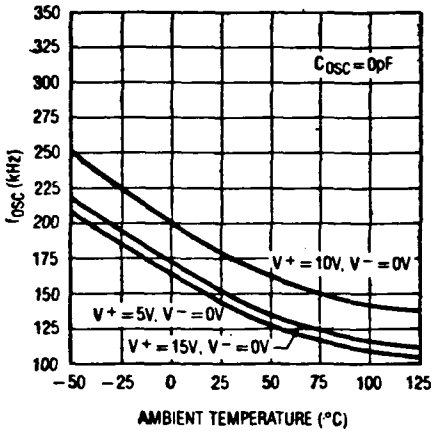


Normalized Oscillator Frequency, fOSC, vs Supply Voltage

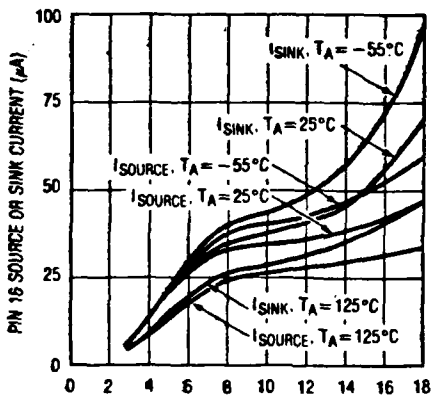


TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

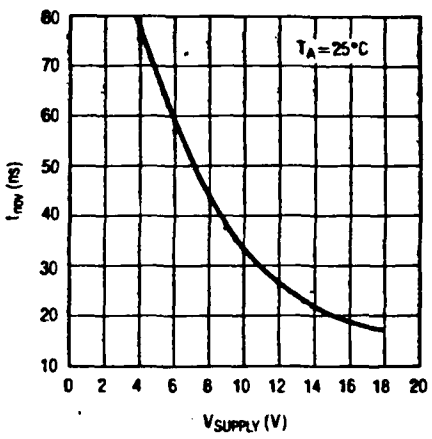
Oscillator Frequency, f_{OSC}, vs Ambient Temperature, T_A



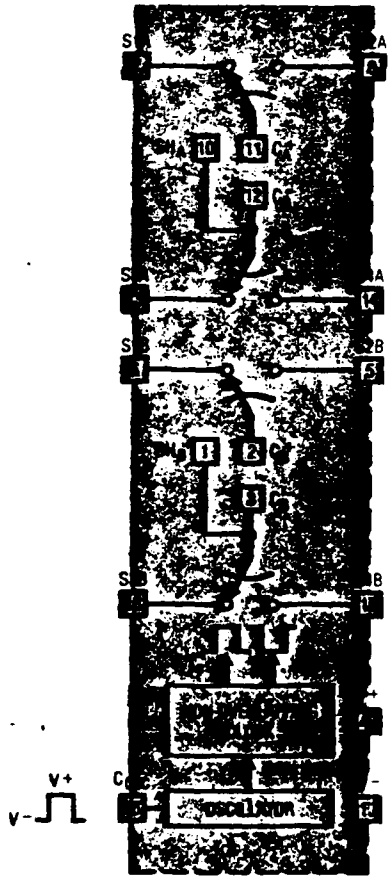
C_{OSC} Pin I_{SINK}, I_{SOURCE} vs Supply Voltage



Break-Before-Make Time, t_{nov}, vs Supply Voltage

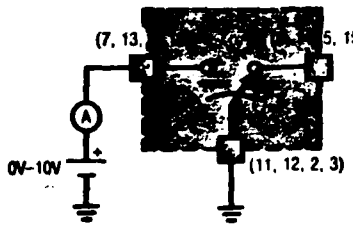


BLOCK DIAGRAM



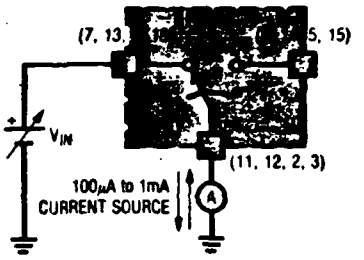
THE SWITCHES ARE TIMED AS SHOWN WITH PIN 16 HIGH

TEST CIRCUITS

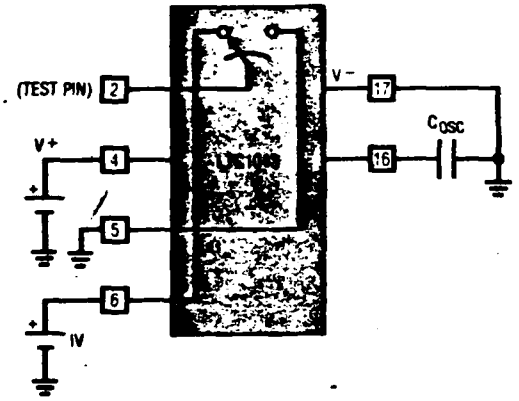


NOTE: TO OPEN SWITCHES S1 AND S3 SHOULD BE CONNECTED to V⁻. TO OPEN S2, S4, C_{OSC} PIN SHOULD BE TO V⁺. C_{OSC}

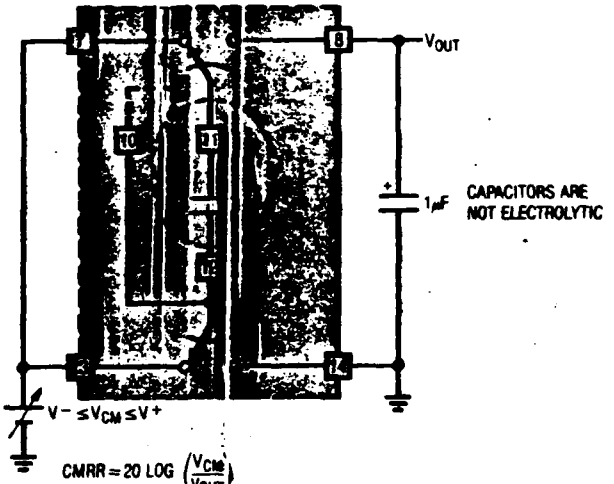
Test Circuit 1. Leakage Current Test



Test Circuit 2. R_{ON} Test



Test Circuit 3. Oscillator Frequency, f_{OSC}



$$CMRR = 20 \log \left(\frac{V_{CM}}{V_{OUT}}\right)$$

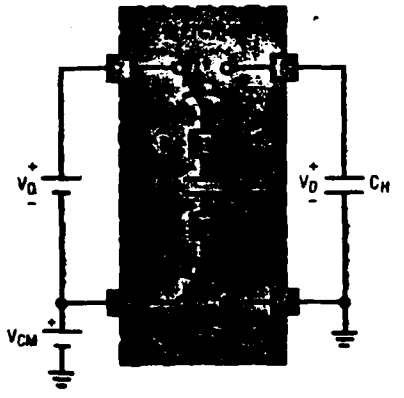
NOTE: FOR OPTIMUM CMRR, THE C_{OSC} SHOULD BE LARGER THAN 0.0047μF, AND THE SAMPLING CAPACITOR ACROSS PINS 11 AND 12 SHOULD BE PLACED OVER A SHIELD TIED TO PIN 10.

Test Circuit 4. CMRR Test

APPLICATIONS INFORMATION

Common-Mode Rejection Ratio (CMRR)

The LTC1043, when used as a differential to single-ended converter (Figure 1) rejects common-mode signals and preserves differential voltages. Unlike other techniques, the LTC1043's CMRR does not degrade with increasing common-mode voltage frequency. During the sampling mode, the impedance of pins 2, 3 (and 11, 12) should be reasonably balanced, otherwise, common-mode signals will appear differentially. The value of the CMRR depends on the value of the sampling and holding capacitors (C_S, C_H) and on the sampling frequency. Since the common-mode voltages are not sampled, the common-mode signal frequency can well exceed the sampling frequency without experiencing aliasing phenomena. The CMRR of Figure 1



C_S, C_H ARE MYLAR OR POLYSTYRENE

Figure 1. Differential to Single-Ended Converter

APPLICATIONS INFORMATION

is measured by shorting pins 7 and 3 and by observing, with a precision DVM, the change of the voltage across C_H with respect to an input CM voltage variation. During the sampling and holding mode, charges are being transferred and minute voltage transients will appear across the holding capacitor. Although the R_{ON} on the switches is low enough to allow fast settling, as the sampling frequency increases, the rate of charge transfer increases and the average voltage measured with a DVM across it will increase proportionally; this causes the CMRR of the sampled data system, as seen by a "continuous" instrument (DVM), to decrease, Figure 2.

Switch Charge Injection

Figure 3 shows one out of the eight switches of the LTC1043, configured as a basic sample and hold circuit. When the switch opens, a "hold step" is observed and its magnitude depends on the value of the input voltage. Figure 4 shows charge injected into the hold capacitor. For instance, a 2pCb of charge injected into a 0.01μF capacitor causes a 200μV hold step. As shown in Figure 4, there is a predictable and repeatable charge injection cancellation when the input voltage is close to half the supply voltage of the LTC1043. This is a unique feature of this product, containing charge-balanced switches fabricated with a self-aligning gate CMOS process. Any switch of the LTC1043, when powered with symmetrical dual supplies, will sample and hold small signals around ground without any significant error.

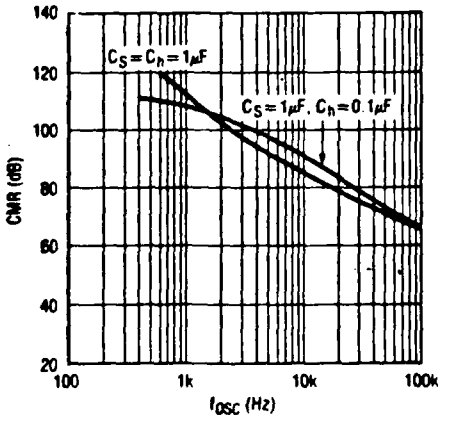


Figure 2. CMRR vs Sampling Frequency

Shielding the Sampling Capacitor for Very High CMRR

Internal or external parasitic capacitors from the C^+ pin(s) to ground affect the CMRR of the LTC1043, (Figure 1). The common-mode error due to the internal junction capacitances of the C^+ pin(s) 2 and 11 is cancelled through internal circuitry. The C^+ pin, therefore, should be used as the top plate of the sampling capacitor. The interpin capacitance between pin 2 and dummy pin 1 (11 and 10) appears in parallel with the sampling capacitor so it does not degrade the CMRR. A shield placed underneath the sampling capacitor (Figure 5) and connected to either pin 1 or 3 helps to boost the CMRR in excess of 120dB.

Excessive external parasitic capacitance between the C^- pins and ground indirectly degrades CMRR; this becomes visible especially when the LTC1043 is used with clock frequencies above 2kHz. Because of this, if a shield is used, the parasitic capacitance between the shield and circuit ground should be minimized.

It is recommended that the outer plate of the sampling capacitor be connected to the C^- pin(s).

Input Pins, SCR Sensitivity

An internal 60Ω resistor is connected in series with the input of the switches (pins 5, 6, 7, 8, 13, 14, 15, 18) and it is included in the R_{ON} specification. When the input voltage exceeds the power supply by a diode drop, current will flow into the input pin(s). The LTC1043 will not

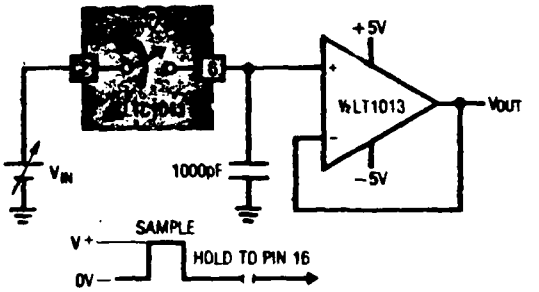


Figure 3

APPLICATIONS INFORMATION

latch until the input current reaches 2mA–3mA. The device will recover from the latch mode when the input drops 3V–4V below the voltage value which caused the latch. For instance, if an external resistor of 200Ω is connected in series with an input pin, the input can be taken 1.3V above the supply without latching the IC. The same applies for the C^+ and C^- pins.

Cosc Pin (16), Figure 6

The Cosc pin can be used with an external capacitor, Cosc, connected from pin 16 to pin 17, to modify the internal oscillator frequency. If pin 16 is floating, the internal 24pF capacitor plus any external interpin capacitance set the oscillator frequency around 190kHz with ±5V supply. The typical performance characteristics curves provide the necessary information to set the oscillator frequency for various power supply ranges. Pin 16 can also be driven with an external clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of pin 16, they will in reality drive the Cosc pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1043 Cosc pins. The typical trip levels of the Schmitt trigger, Figure 6, are given below.

SUPPLY	TRIP LEVELS	
$V^+ = 5V$, $V^- = 0V$	$V_H = 3.4V$	$V_L = 1.35V$
$V^+ = 10V$, $V^- = 0V$	$V_H = 6.5V$	$V_L = 2.8V$
$V^+ = 15V$, $V^- = 0V$	$V_H = 9.5V$	$V_L = 4.1V$

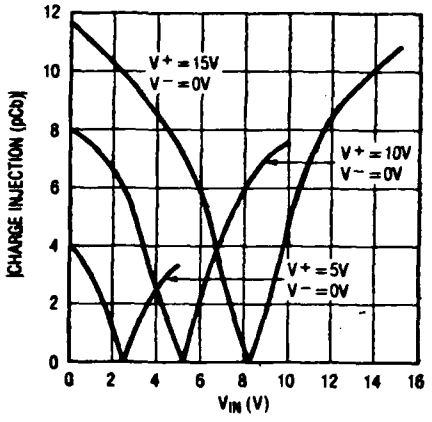


Figure 4. Individual Switch Charge Injection vs Input Voltage

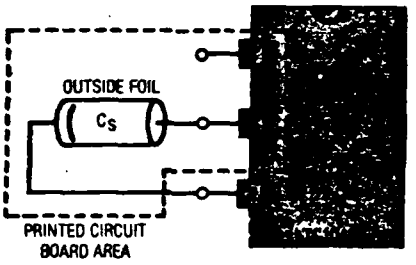
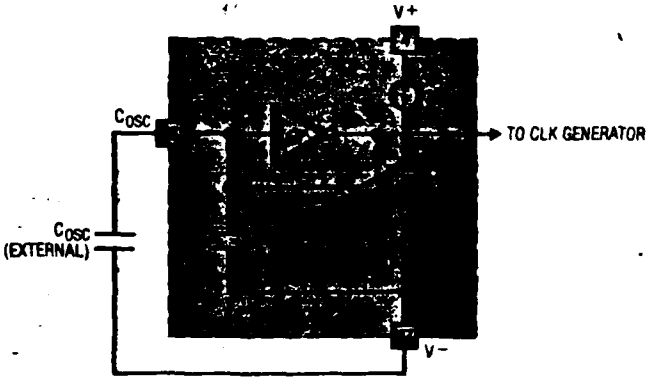


Figure 5. Printed Circuit Board Layout Showing Shielding the Sampling Capacitor

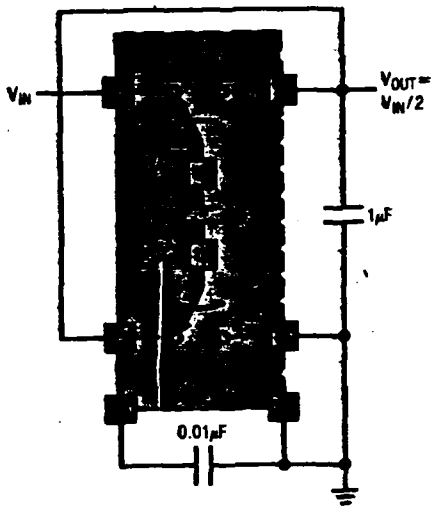


$$f_{OSC} = 190kHz \times \frac{(24pF)}{(24pF + C_{OSC})}$$

Figure 6. Internal Oscillator

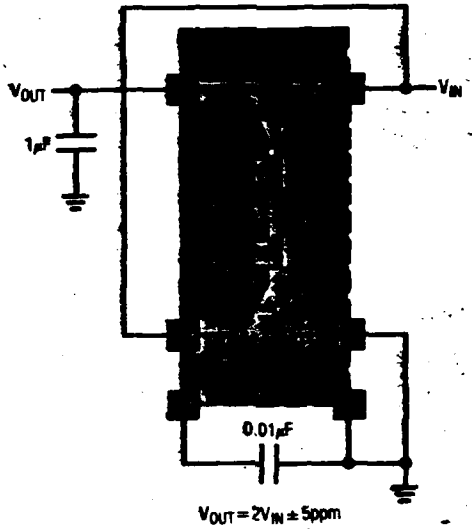
APPLICATIONS

Divide by 2



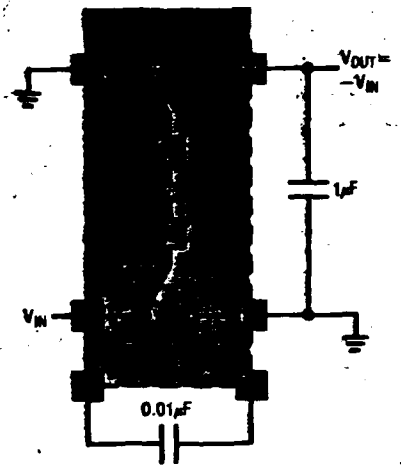
$V_{OUT} = V_{IN}/2 \pm 1ppm$
$0 \le V_{IN} \le V^+$
$3 \le V^+ \le 18V$

Multiply by 2



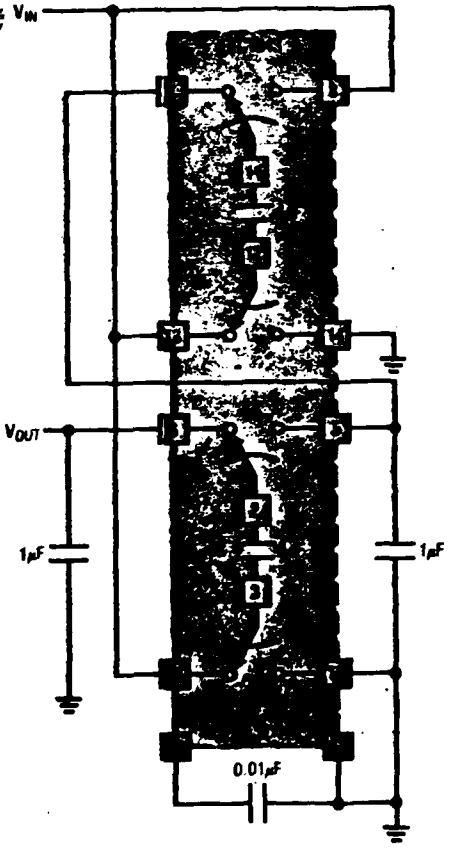
$V_{OUT} = 2V_{IN} \pm 5ppm$
$0 \le V_{IN} < V^+/2$
$3 \le V^+ \le 18V$

Ultra Precision Voltage Inverter



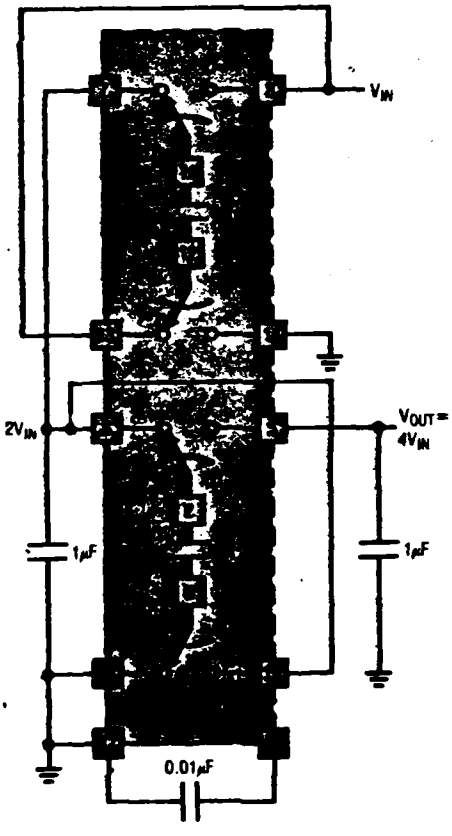
$V_{OUT} = -V_{IN} \pm 2ppm$
$V^- < V_{IN} < V^+$
$V^+ = +5V, V^- = -5V$

Precision Multiply by 3



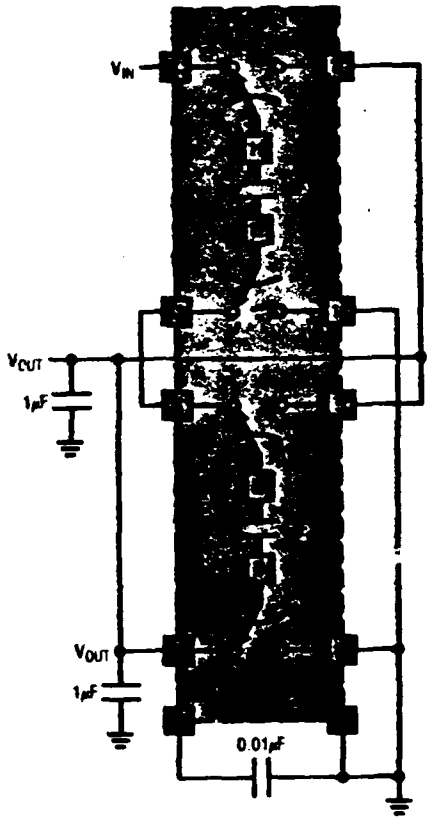
$V_{OUT} = 3V_{IN} \pm 10ppm$
$0 < V_{IN} < V^+/3$
$3V < V^+ < 18V$

Precision Multiply by 4



$V_{OUT} = 4V_{IN} \pm 40ppm$
$0 \le V_{IN} \le V^+/4$
$3V < V^+ < 18V$

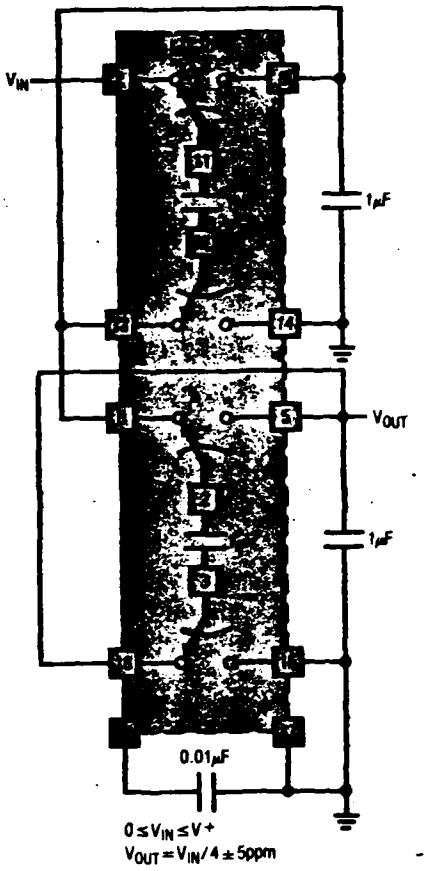
Divide by 3



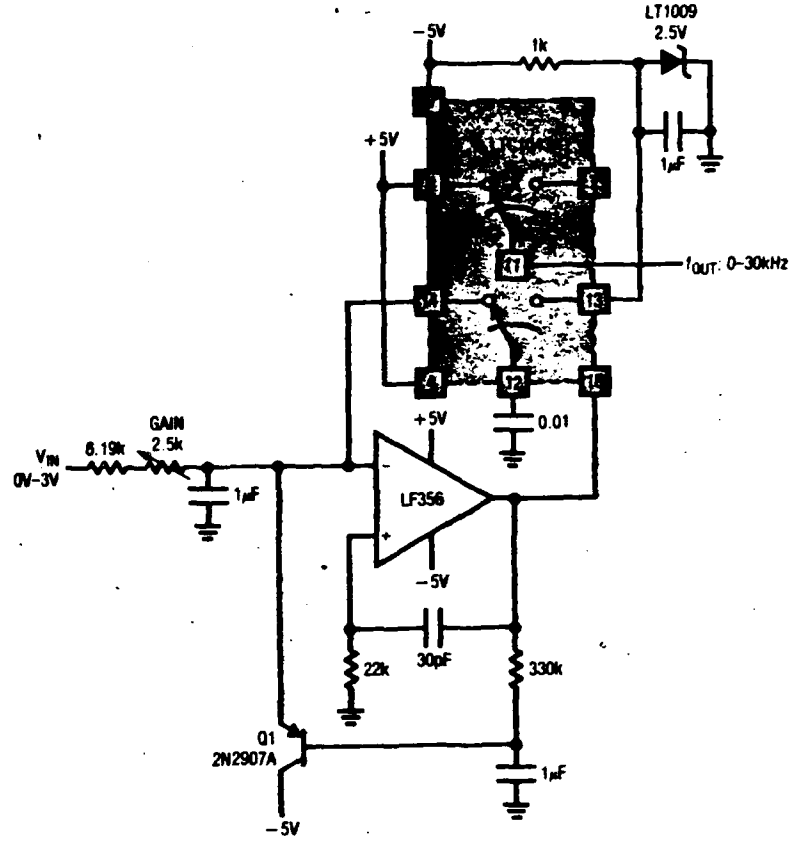
$V_{OUT} = V_{IN}/3 \pm 3ppm$
$0 \le V_{IN} \le V^+$

APPLICATIONS

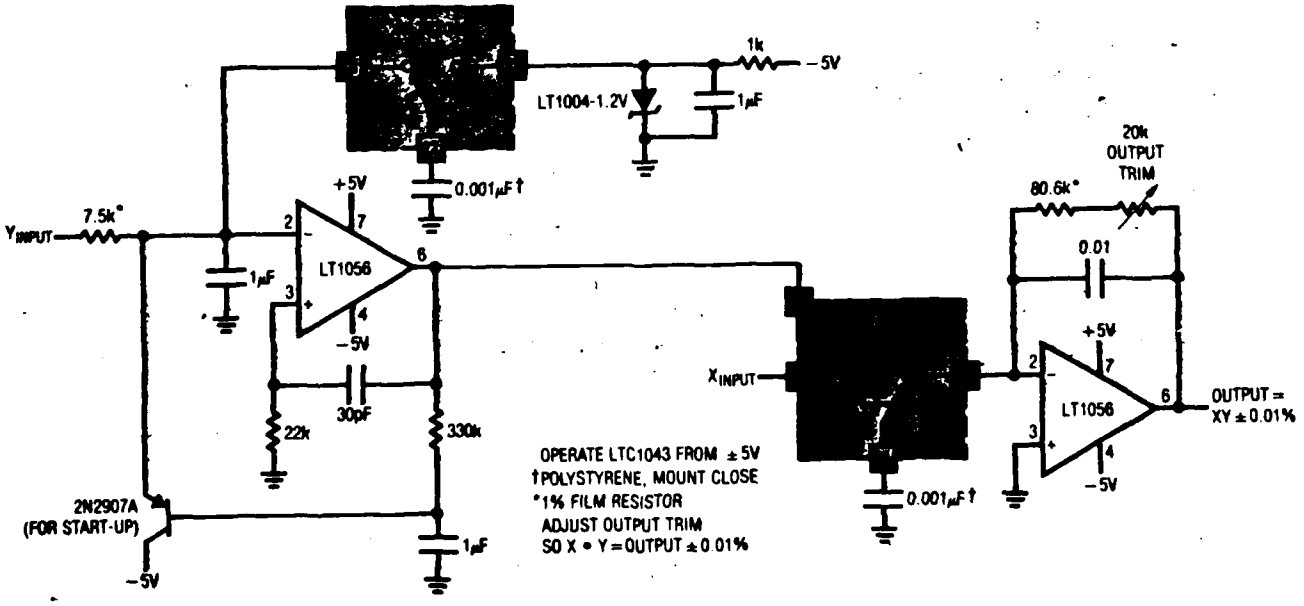
Divide by 4



0.005% V → F Converter

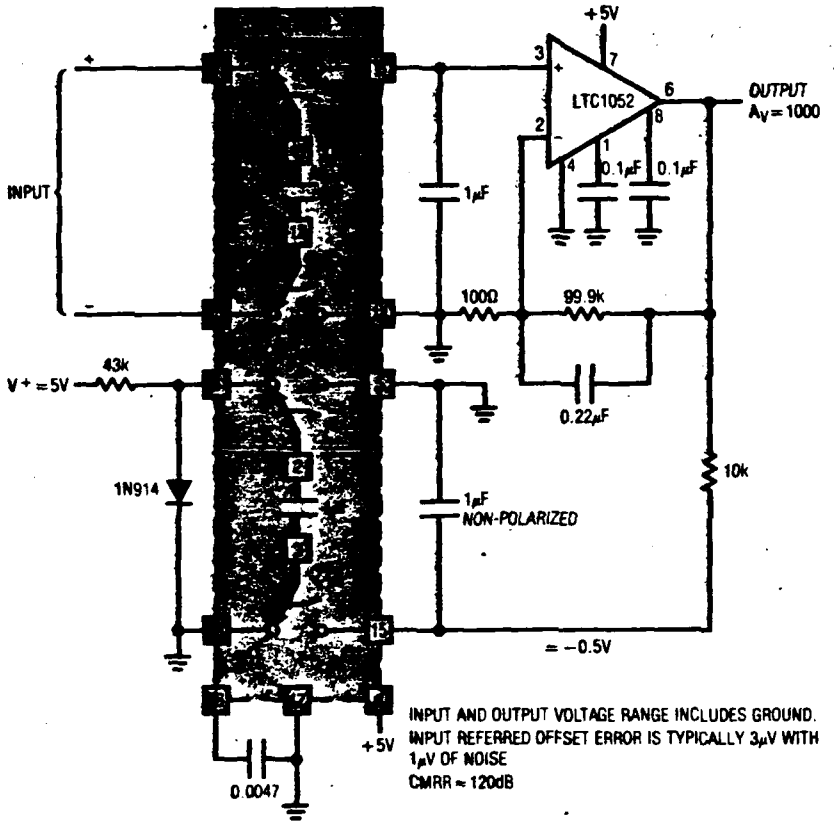


0.01% Analog Multiplier



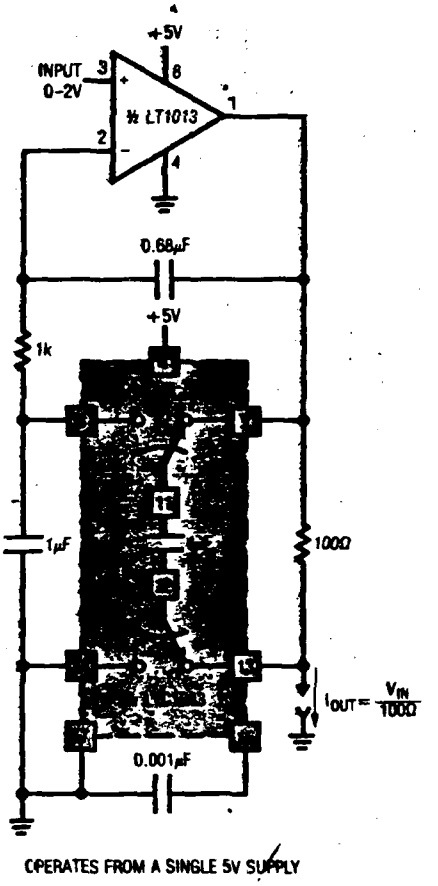
APPLICATIONS

Single 5V Supply, Ultra Precision Instrumentation Amplifier



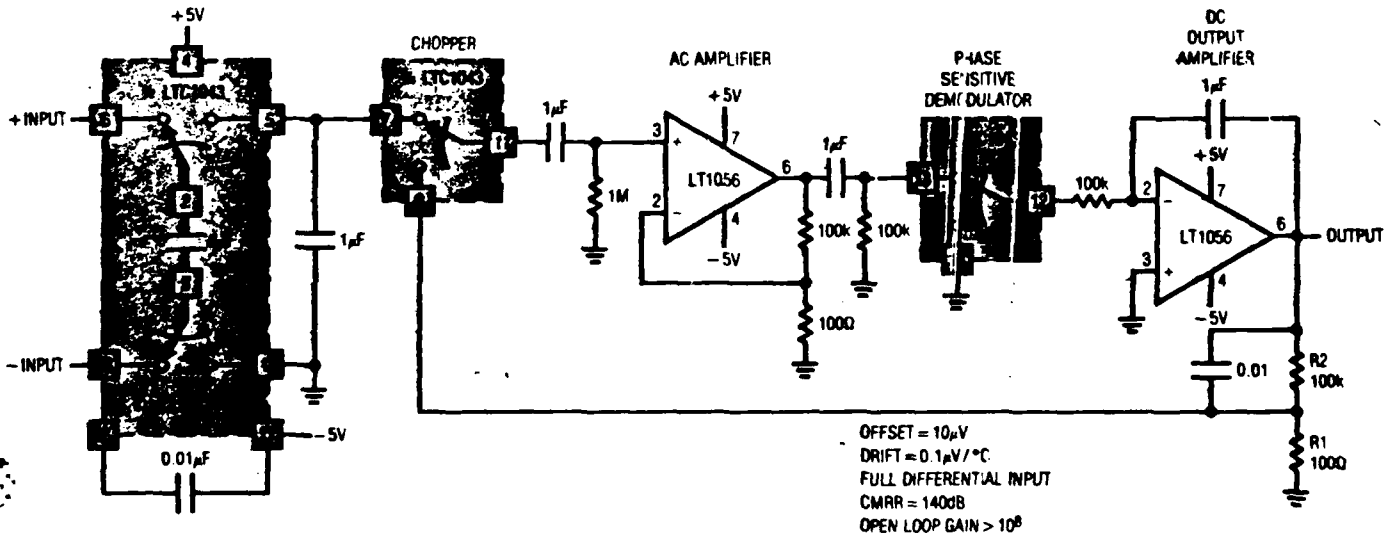
INPUT AND OUTPUT VOLTAGE RANGE INCLUDES GROUND.
INPUT REFERRED OFFSET ERROR IS TYPICALLY 3μV WITH 1μV OF NOISE
CMRR ≈ 120dB

Voltage Controlled Current Source with Ground Referred Input and Output



OPERATES FROM A SINGLE 5V SUPPLY

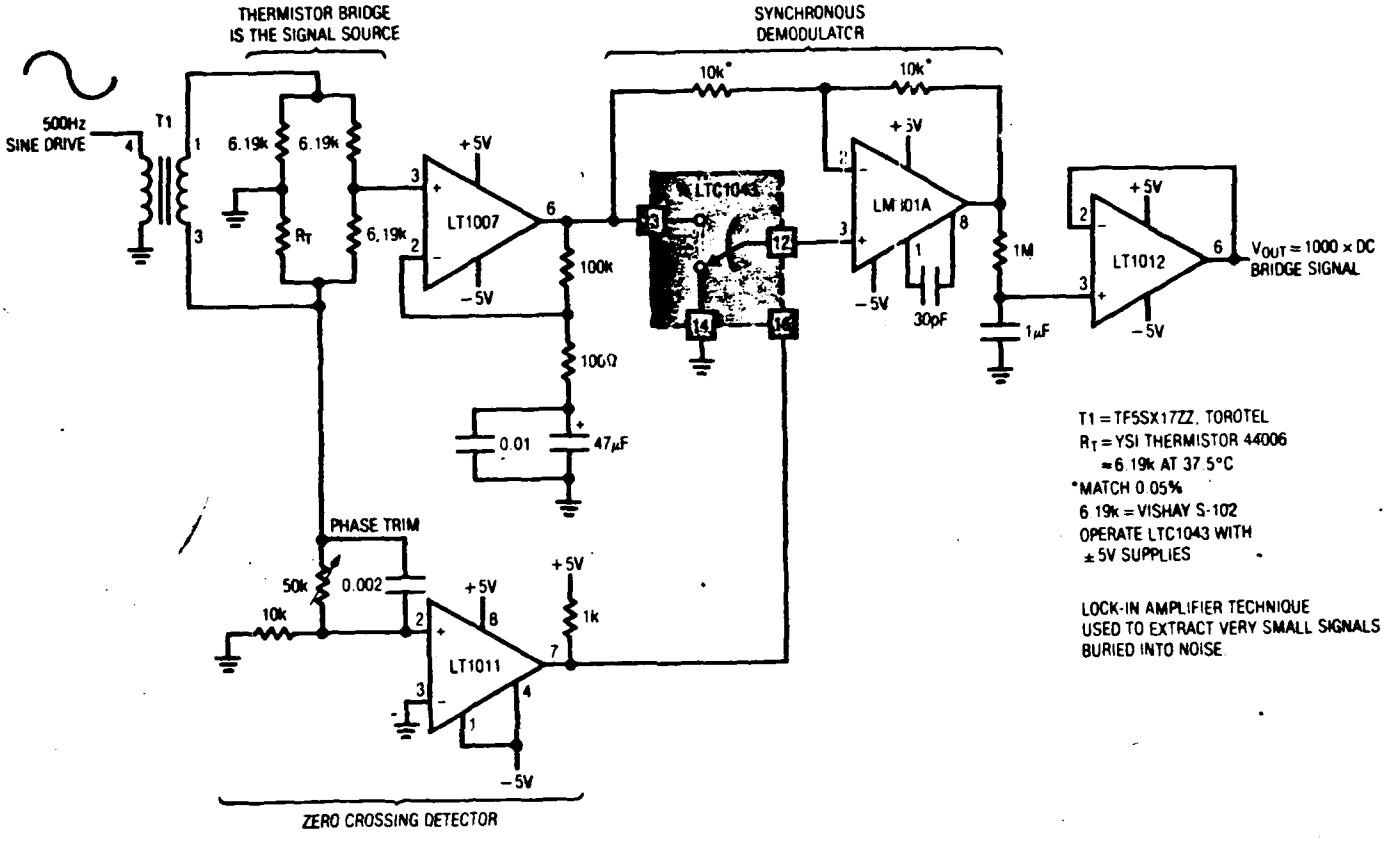
Precision Instrumentation Amplifier



OFFSET = 10μV
DRIFT = 0.1μV/°C
FULL DIFFERENTIAL INPUT
CMRR = 140dB
OPEN LOOP GAIN > 10^8
GAIN = R2/R1 + 1
I_{BIAS} = 1nA

APPLICATIONS

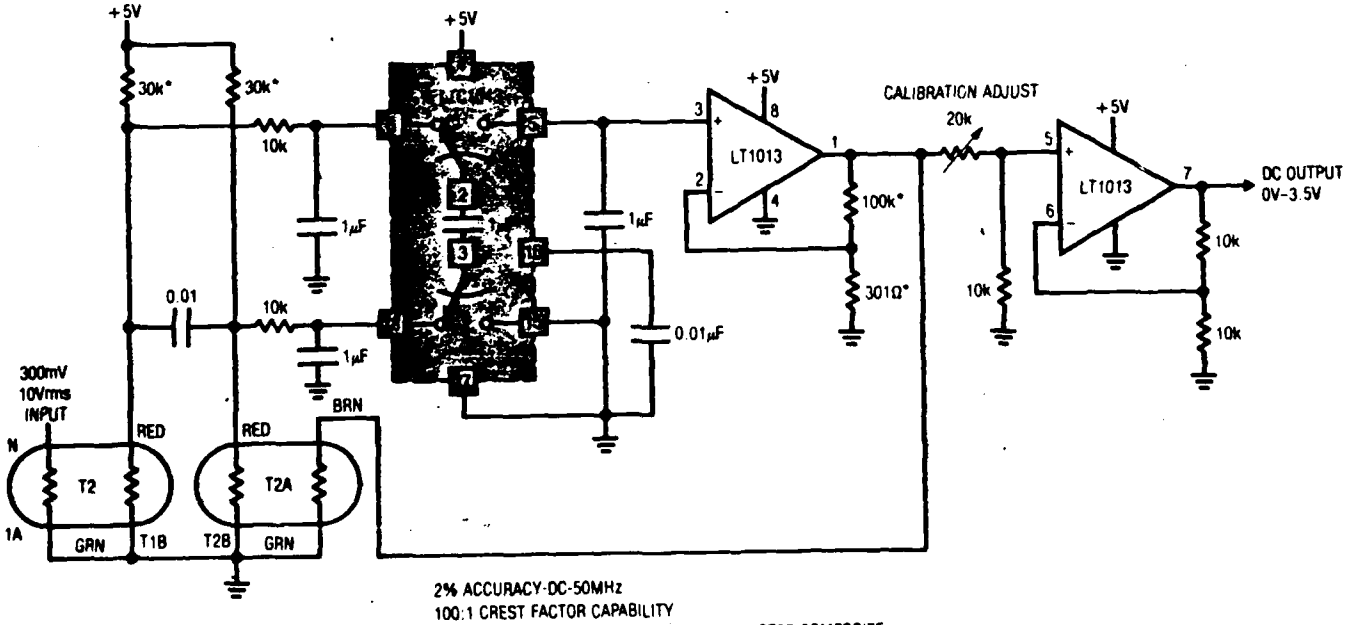
Lock-In Amplifier (=Extremely Narrow-Band Amplifier)



T1 = TF5SX17ZZ, TOROTEL
R_T = YSI THERMISTOR 44006
≈6.19k AT 37.5°C
*MATCH 0.05%
6.19k = VISHAY S-102
OPERATE LTC1043 WITH
±5V SUPPLIES

LOCK-IN AMPLIFIER TECHNIQUE USED TO EXTRACT VERY SMALL SIGNALS BURIED INTO NOISE.

50MHz Thermal rms → DC Converter

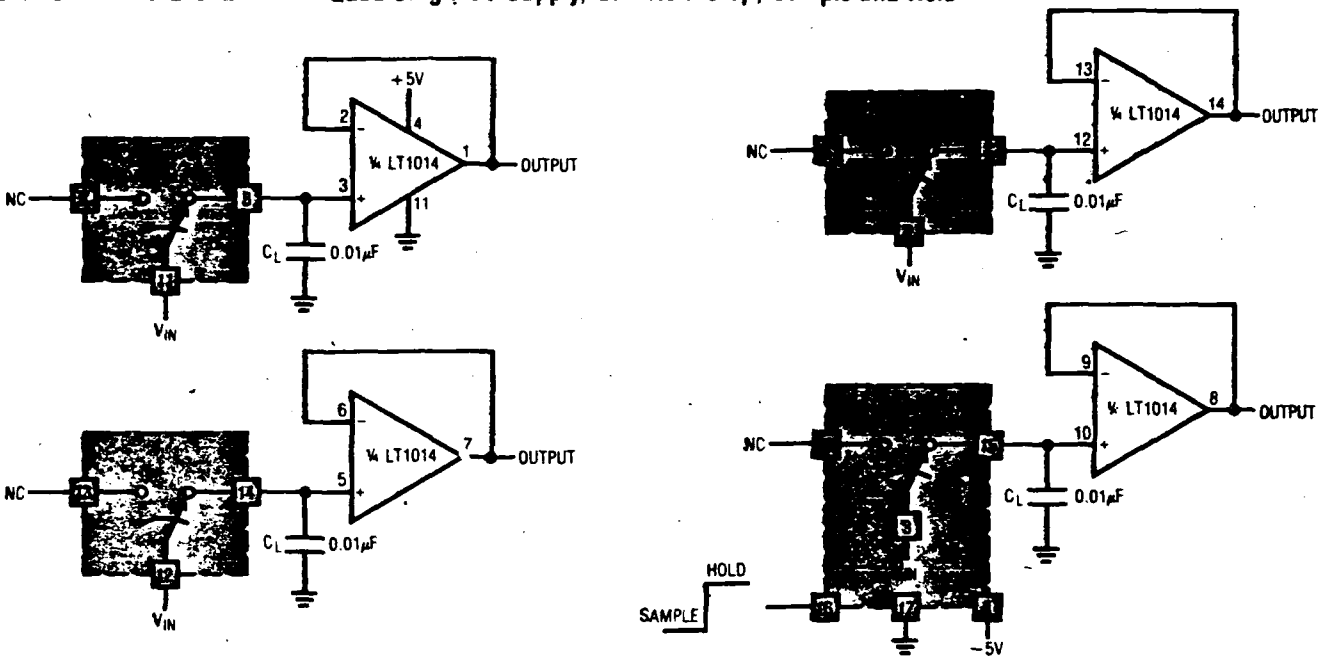


*1% RESISTOR

2% ACCURACY-DC-50MHz
100:1 CREST FACTOR CAPABILITY
T1-T2 = YELLOW SPRINGS INST. CO. THERMISTOR COMPOSITE
ENCLOSE T1 AND T2 IN STYROFOAM
SINGLE 5V SUPPLY

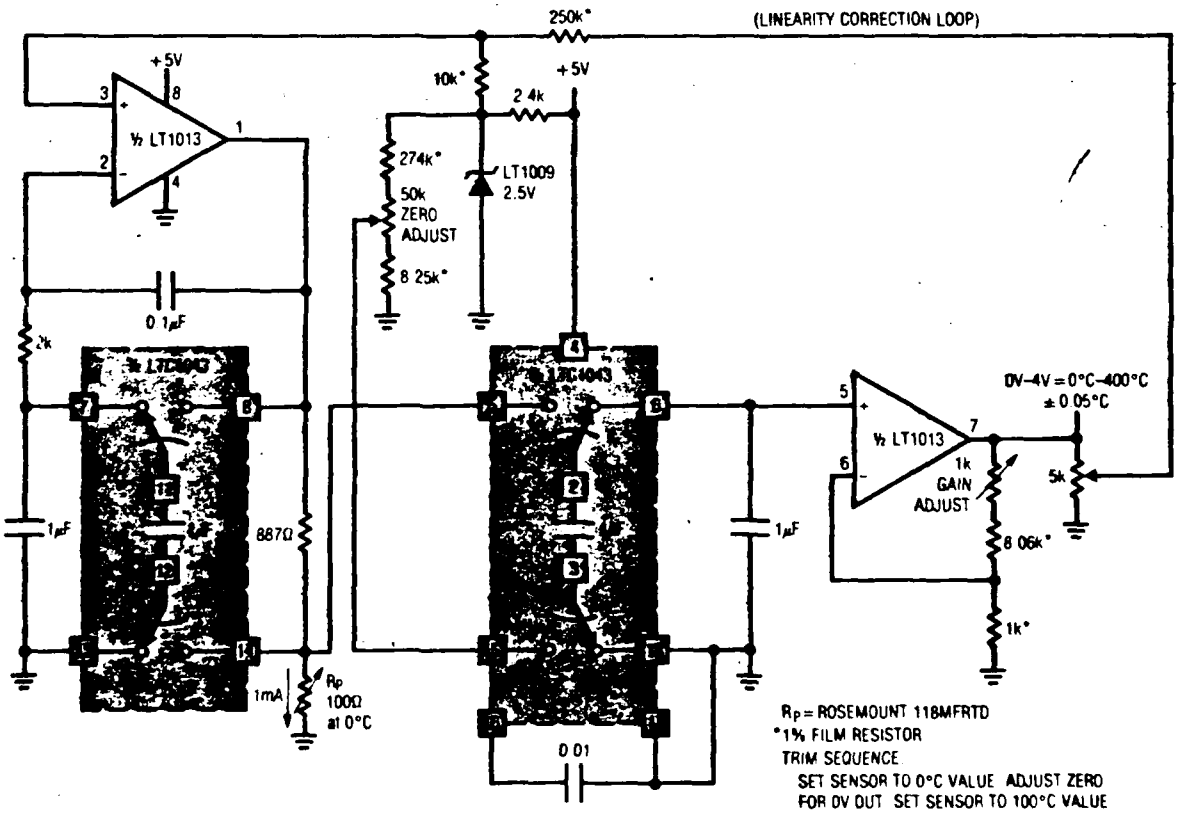
APPLICATIONS

Quad Single 5V Supply, Low Hold Step, Sample and Hold



FOR $1V \leq V_{IN} \leq 4V$, THE HOLD STEP IS ≤300μV.
ACQUISITION TIME = $8 \times R_{ON} C_H$ FOR 10-BIT ACCURACY.

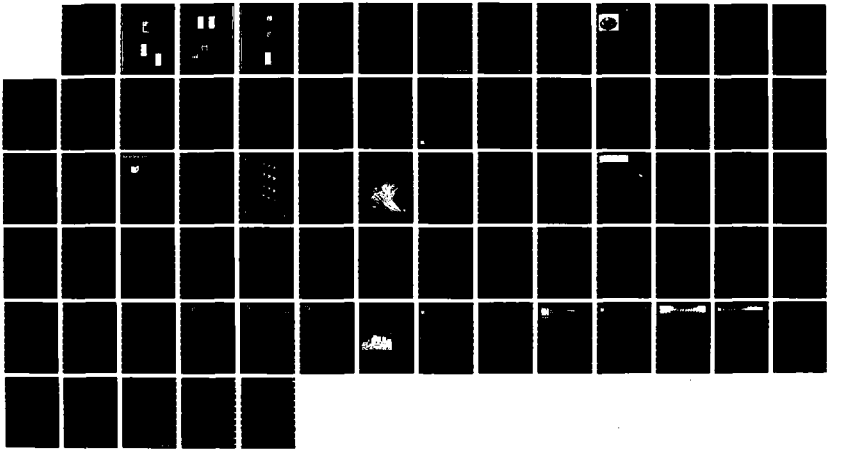
Single Supply Precision Linearized Platinum RTD Signal Conditioner

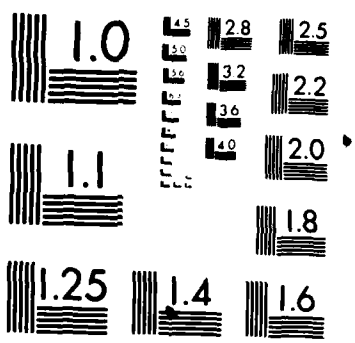


R_P = ROSEMOUNT 118MFRTD
*1% FILM RESISTOR
TRIM SEQUENCE
SET SENSOR TO 0°C VALUE ADJUST ZERO
FOR 0V OUT SET SENSOR TO 100°C VALUE
ADJUST GAIN FOR 1.000V OUT SET SENSOR
TO 400°C VALUE ADJUST LINEARITY FOR 4.000V OUT
REPEAT AS REQUIRED

AD-A172 400 SMALL SELF-CONTAINED AIRCRAFT FATIGUE DATA RECORDER(U) 2/2
ESPIRT TECHNOLOGY INC WALNUT CREEK CA P FLANNER AUG 86
N62269-85-C-0716

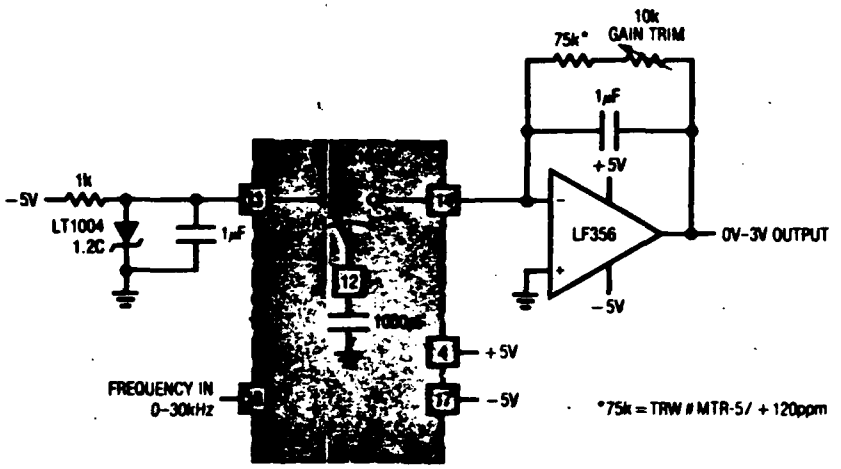
UNCLASSIFIED F/G 20/11 NL



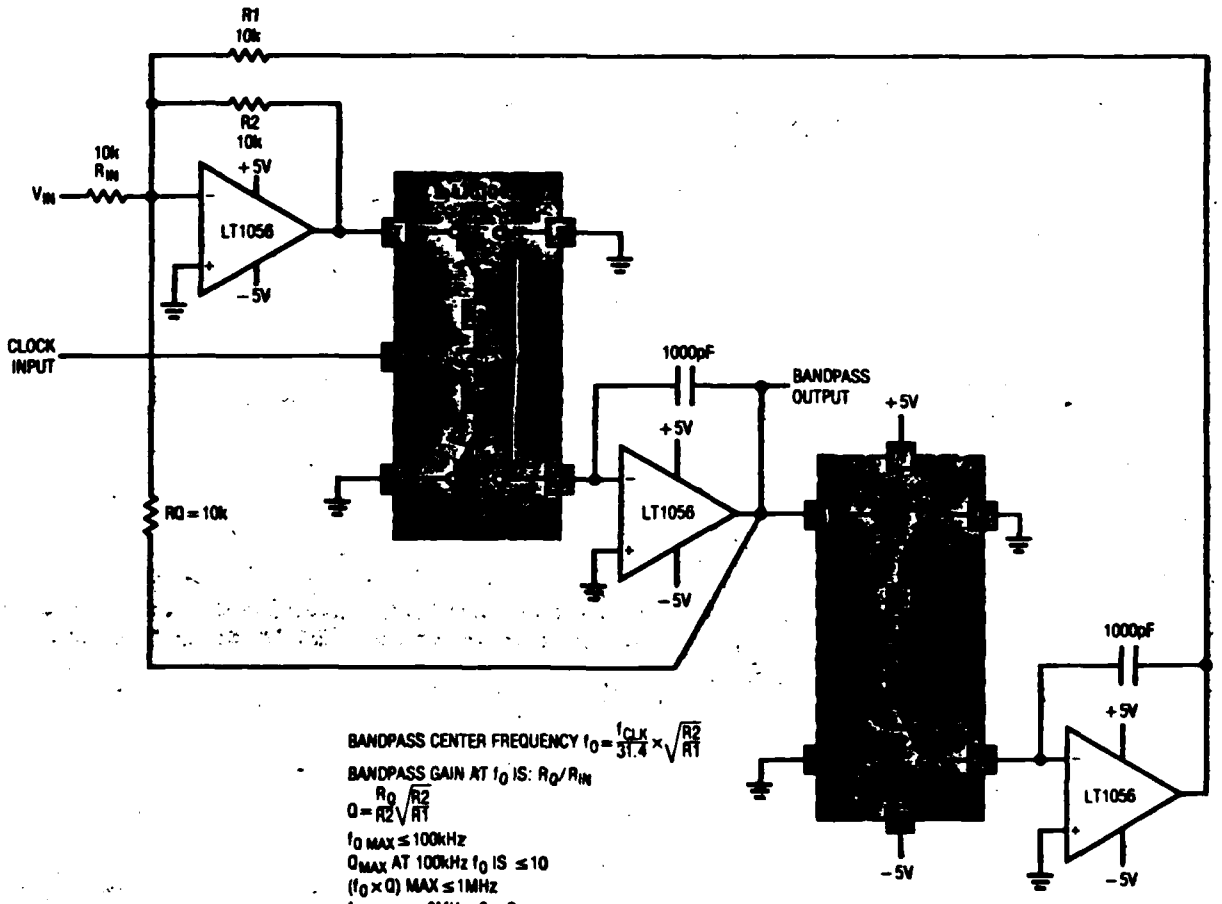


APPLICATIONS

0.005%F → V Converter



High Frequency Clock Tunable Bandpass Filter



BANDPASS CENTER FREQUENCY $f_0 = \frac{f_{CLK}}{31.4} \times \sqrt{\frac{R2}{R1}}$

BANDPASS GAIN AT f_0 IS: R_Q/R_{IN}

$Q = \frac{R_Q}{R2}\sqrt{\frac{R2}{R1}}$

$f_{0\,MAX} \leq 100kHz$

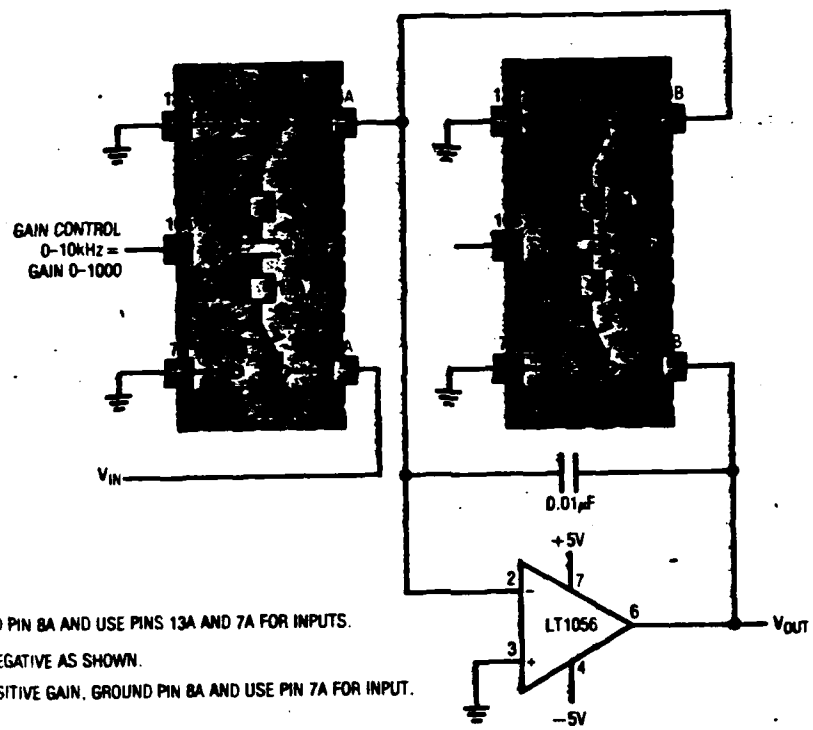
Q_{MAX} AT 100kHz f_0 IS ≤ 10

$(f_0 \times Q)$ MAX $\leq 1MHz$

$f_{CLK\,MAX} \leq 3MHz$, $Q < 2$

APPLICATIONS

Frequency-Controlled Gain Amplifier



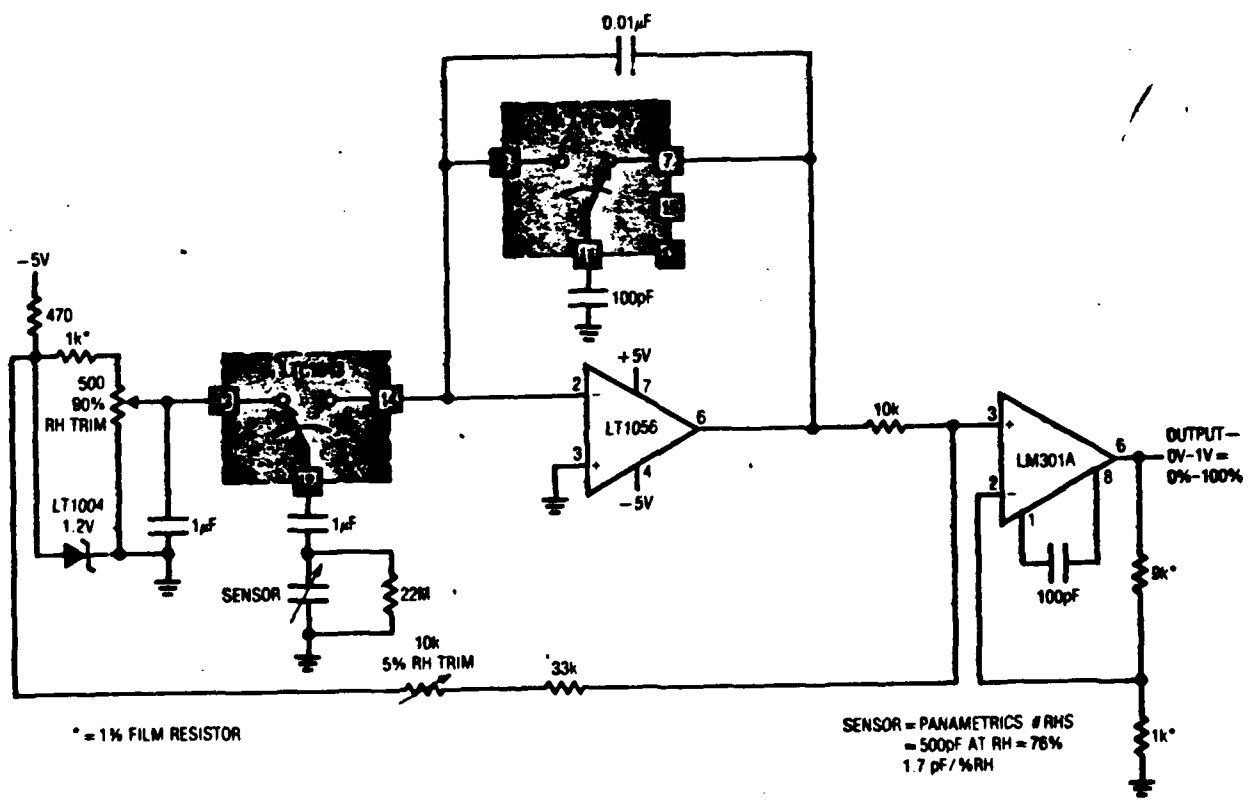
FOR DIFFERENTIAL INPUT, GROUND PIN 8A AND USE PINS 13A AND 7A FOR INPUTS.

GAIN = $\frac{f_{IN} \times 0.01\mu F}{1kHz \times 100pF}$; GAIN IS NEGATIVE AS SHOWN.

FOR SINGLE-ENDED INPUT AND POSITIVE GAIN, GROUND PIN 8A AND USE PIN 7A FOR INPUT.

USE ±5V SUPPLIES FOR LTC1043.

Relative Humidity Sensor Signal Conditioner

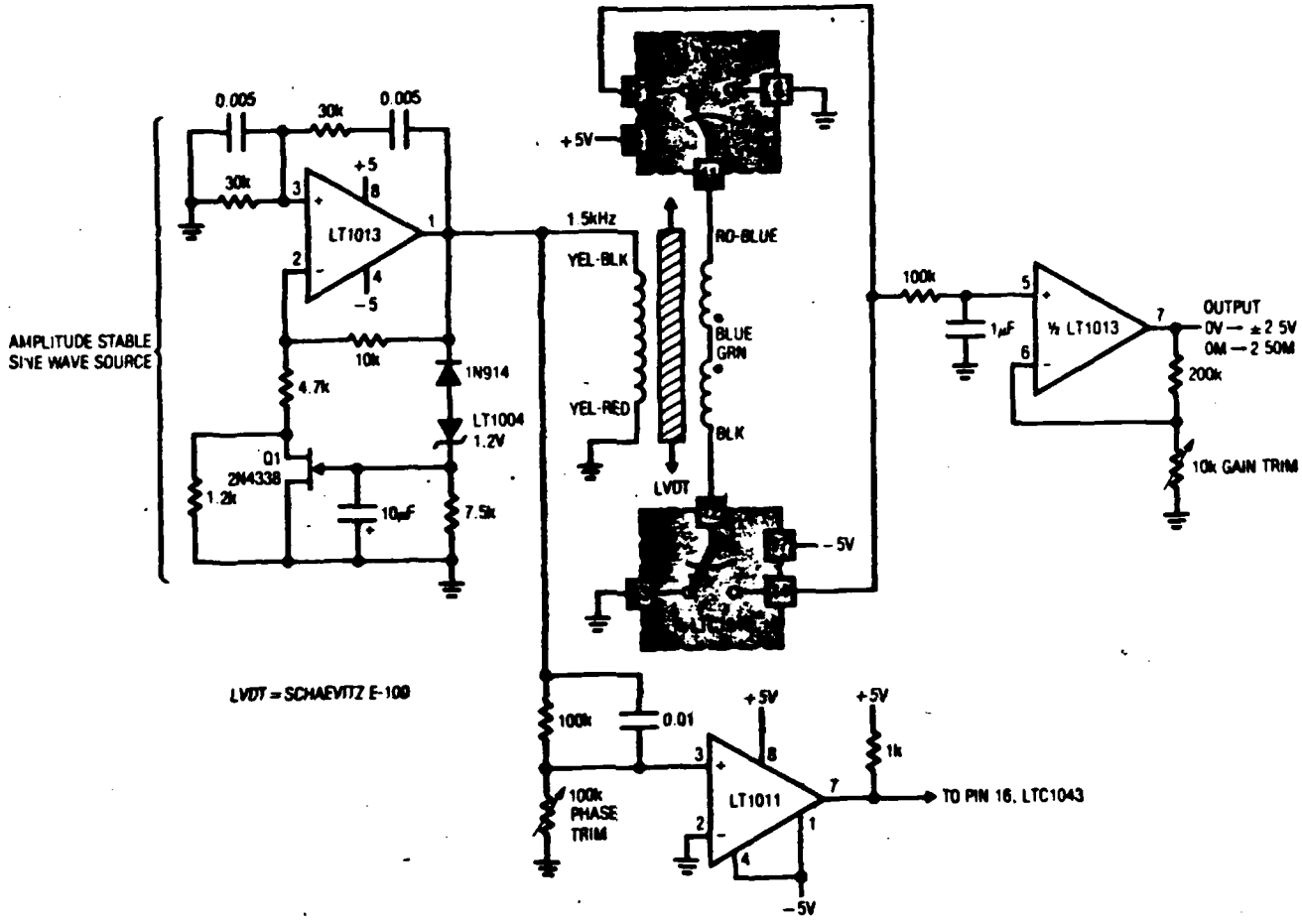


* = 1% FILM RESISTOR

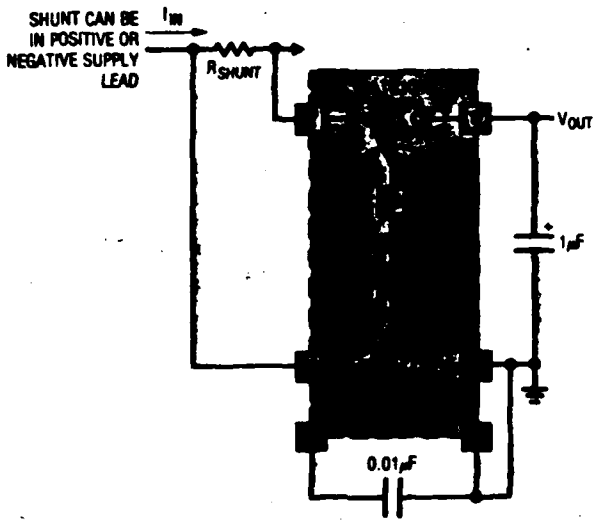
SENSOR = PANAMETRICS #RHS
= 500pF AT RH = 76%
1.7 pF/%RH

APPLICATIONS

Linear Variable Differential Transformer (LVDT), Signal Conditioner

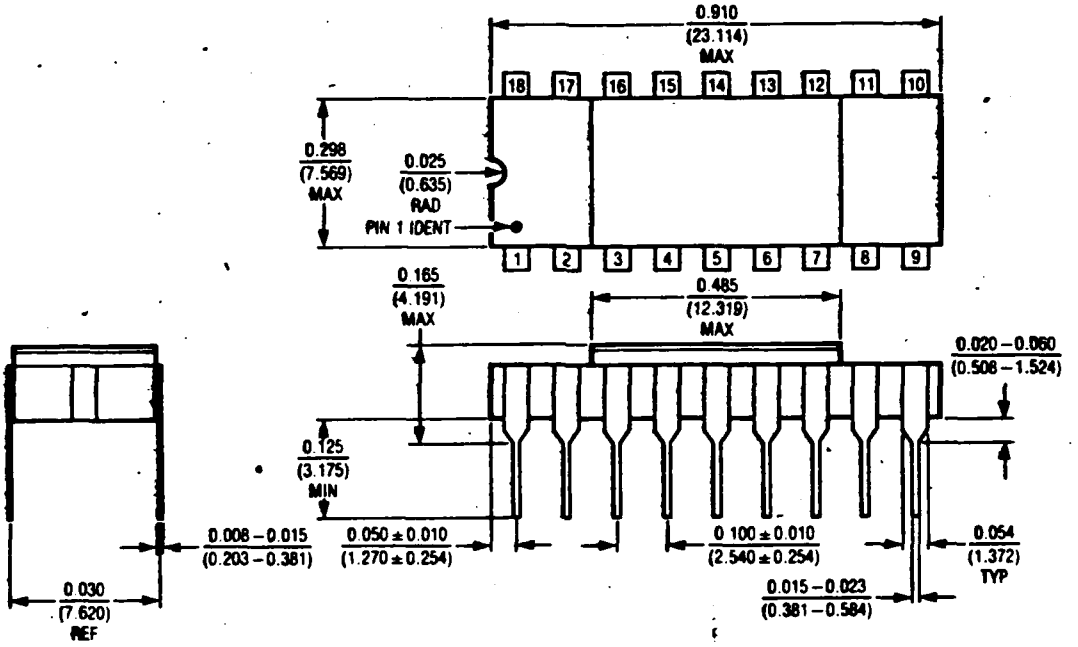


Precision Current Sensing in Supply Rails



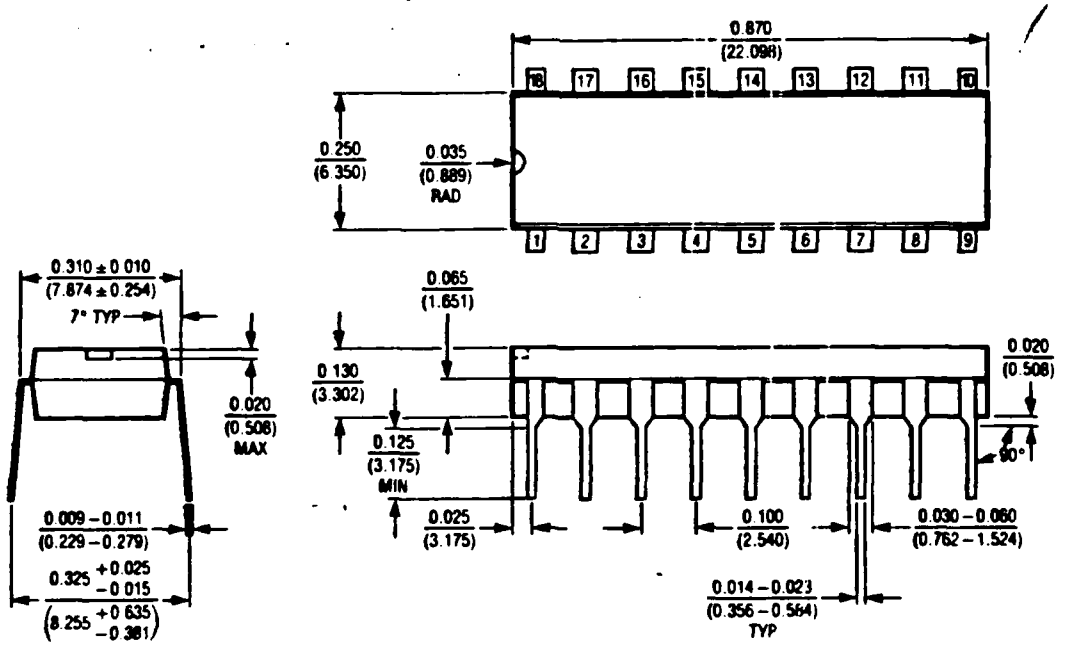
PACKAGE DESCRIPTION

D Package
18 Lead Side Brazed



	T_{jmax}	Θ_{ja}
LTC1043MD	150°C	100°C/W
LTC1043CD	150°C	100°C/W

N Package
18 Lead Plastic DIP



	T_{jmax}	Θ_{ja}
LTC1043CN	100°C	100°C/W

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487 • (408) 942-0810

GP/IM 984 20K

EXHIBIT 5

A 3rd Order Butterworth Filter

3 Pole Butterworth

A 2ND order section of $Q = 1$ preceded with a simple pole at ω_0.

The form

$$\frac{e_o}{e_i} = \frac{\omega_0^2}{s^2 + Q\omega_0 s + \omega_0^2} \times \frac{\omega_0}{s + \omega_0}$$

which, with $Q = 1$ gives

$$\frac{e_o(s)}{e_i(s)} = \frac{\omega_0^3}{s^3 + 2\omega_0 s^2 + 2\omega_0^2 s + \omega_0^3}$$

The magnitude function -

1ST substitute $s = j\omega$ to get

$$\frac{e_o(j\omega)}{e_i(j\omega)} = \frac{\omega_0^3}{(\omega_0^3 - 2\omega_0\omega^2) + (2\omega_0^2\omega - \omega^3)j}$$

$$\left|\frac{e_o(j\omega)}{e_i(j\omega)}\right| = \frac{\omega_0^3}{\sqrt{(\omega_0^3 - 2\omega_0\omega^2)^2 + (2\omega_0^2\omega - \omega^3)^2}} = |M| \quad \left(\text{from mag } \frac{1}{a+bj} = \frac{1}{\sqrt{a^2+b^2}}\right)$$

$$= \frac{1}{\sqrt{\left(1 - 2\frac{\omega^2}{\omega_1^2}\right)^2 + \left(2\frac{\omega}{\omega_0} - \frac{\omega^3}{\omega_0^3}\right)^2}} = |M|$$

note: $|M| = \dfrac{1}{\sqrt{1 + \left(\left(\frac{\omega}{\omega_0}\right)^2\right)^3}}$

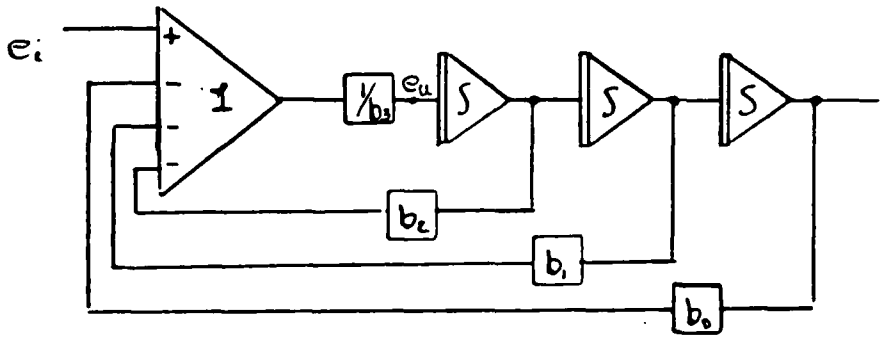
at $\omega = \omega_0$

$$20 \log |M| = 20 \log \frac{1}{\sqrt{2}} = -10 \log 2 = -3.01 \text{ db.}$$

at $\omega = \omega_0/2$

$$20 \log |M| = 20 \log \frac{1}{\sqrt{\left(\frac{1}{2}\right)^2 + \left(\frac{7}{8}\right)^2}} = 20 \log \frac{1}{\sqrt{65/64}} = -.067 \text{ db} \quad (\approx -.8\%)$$

State Variable Filter.



where $\boxed{S} = \frac{w_o}{s}$

Then

$$e_u = \left\{ e_i - e_u \left(\frac{w_o b_2}{s} + \frac{w_o^2 b_1}{s^2} + \frac{w_o^3 b_0}{s^3} \right) \right\} \frac{1}{b_3}$$

or $$e_u = \frac{e_i}{b_3 + \frac{b_2 w_o}{s} + \frac{b_1 w_o^2}{s^2} + \frac{b_0 w_o^3}{s^3}}$$

but $$e_o = e_u \frac{w_o^3}{s^3}$$

thus $$\frac{e_o}{e_i} = \frac{w_o^3}{b_3 s^3 + b_2 w_o s^2 + b_1 w_o^2 s + b_0 w_o^3}$$

and, comparing to the 3 pole butterworth, we see that if $b_3 = 1$, $b_2 = 2$, $b_1 = 2$, $b_0 = 1$ then we have created the 3 pole butterworth configuration.

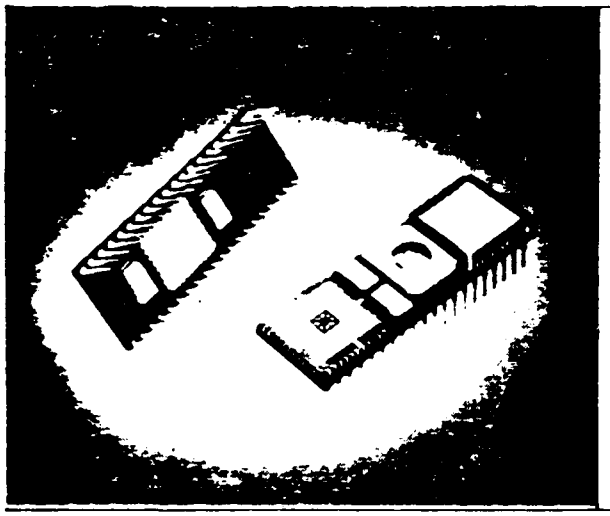
The state variable function could be emulated with a digital computer.

EXHIBIT 6

The Electronic Designs Inc.

EDH0067C31 PAK

Electronic Designs Inc.



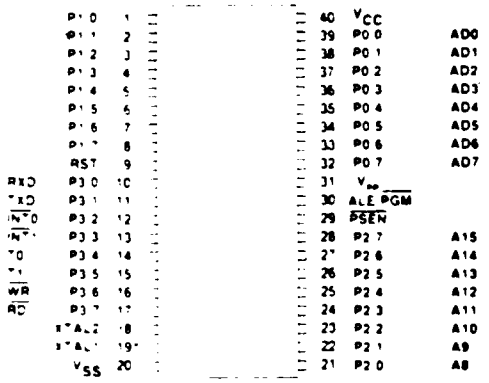
EDH687C31 μPak
MILITARY
Micro Computer CMOS, 80C31 Based 8Kx8 EPROM, 8Kx8 SRAM

PRELIMINARY

The EDH687C31 μPak from EDI is the first in a series of High Density Microcomputer Modules based on the Intel 80C31. The all CMOS 687C31 μPak Module is functionally compatible with the 80C31 device. The module incorporates an 80C31, 8Kx8 of EPROM, 8Kx8 of RAM and a Logic Control Unit, all packaged in leadless chip carriers and mounted onto a 40 pin ceramic substrate with 600 mil pin spacing.

The open architecture allows memory to be added externally with a total address range of 64K Bytes for both Program and Data storage giving 128K Bytes of accessible memory.

PINOUTS



FEATURES

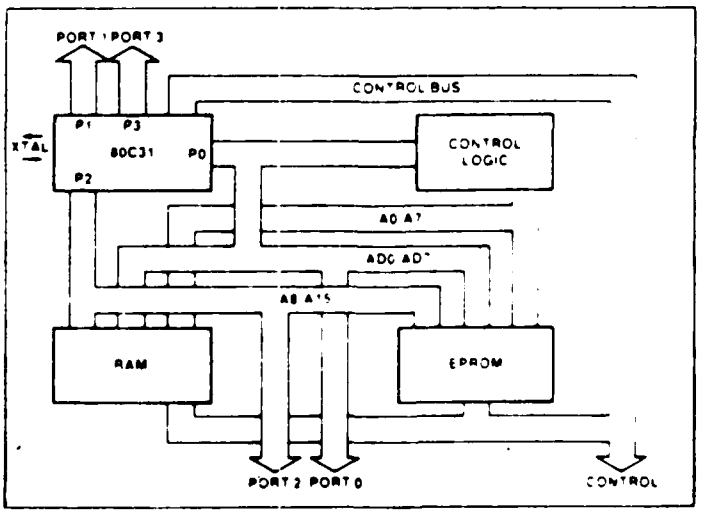
High Density CMOS Micro Computer Module
80C31 80C31 Compatible with 8192x8 bit EPROM and 8192x8 bit SRAM

Memory
- 8Kx8 EPROM onboard programmable
- 8Kx8 SRAM
- Open system architecture
- 128K Byte Dual Map

Full CMOS low power
- 3.5 - 8 MHz Operation
- Power Down Consumption = 150μA typ.

40 Pin Double Sided Dual-in-line Package
- Pins on 600 mil centers
- L-2.05" x W-0.700" x H-0.325"

Single +5V (±10%) Supply Operation
Mil-STD 883 Equivalent Processing



DESCRIPTION

The EDH687C31's open system architecture allows it to operate like an 80C31. Consequently, PORT 0 and PORT 2 are dedicated address/data-lines and address-lines respectively, both when considered "on substrate" and from the interfacing logic.

The 687C31 is configured with dual 64K byte memory maps. The Program Memory Area is occupied from address 0000H with 8Kx8 of EPROM on the substrate.

Programming of the EPROM is accomplished on-board with the aid of a Programming Adaptor, and any programmer that supports 2764 - type EPROMs.

The Data Memory Area has 8Kx8 of Static RAM configured from address 8000H. The addresses of F800H and above are reserved for the POWER DOWN REGISTER (see section on POWER DOWN REGISTER) and cannot be utilized by external memory. All remaining areas unused internally may be configured externally.

In addition to on-board memory, the 687C31 features its own logic control unit (LCU). This gate array decodes and selects the control lines to and from the on-board memory and allows programming to take place. The LCU ensures that the lower current conditions prevail while the device is in power down mode.

The EDH687C31 supports both IDLE and POWER DOWN modes of the 80C31 and is processed to meet full MIL-STD 883B requirements.

The only pinout variations from the 80C31 are pins 30 and 31.

	EDH687C31	80C31
PIN 30	ALE/$\overline{PGM}$	ALE
PIN 31	V_{PP}	$\overline{EA}$

Pin 30 on the EDH687C31 is a bi-directional pin, whereas on the 80C31 it is an output only. On the EDH687C31, the pin has a double function, due to the need for a PGM pin during the programming of the EPROM. (Described later). This applies to the 687C31's pin 31 as well. When operating the EDH687C31, V_{CC} must be applied to pin 31. On the 80C31, pin 31 has to be held at GND level during operation.

CONTROL LINES

Control lines from the CPU are used when interacting with the on-substrate environment as well as with the system in which the EDH687C31 is operating.

ALE, $\overline{PSEN}$, $\overline{WR}$ and $\overline{RD}$ are used for controlling external memories, latches and other I/F - circuits. $\overline{INT0}$, $\overline{INT1}$, T0 and T1 are used when external circuitry wants to interrupt the 687C31, start or stop one of the CPU timers, or do event counting. The serial lines, RXD and TXD and XTAL lines, 1 and 2, are as specified for the 80C31. This is also true for the RST line, the reset line which is directly connected to the CPU.

BUS LINES

The EDH687C31, like the 80C31, needs to access external memory in order to fetch its program. This is why ports P0 and P2 are dedicated as address and data busses. There is one dedicated I/O port. This is directly connected to the 687C31 PORT 1 for direct control of I/O functions.

SPECIAL LINES

Special lines are needed on the EDH687C31 in order to program the on-substrate EPROM. The V_{PP} pin (31) is needed in order to provide the EPROM with its programming voltage. The control signal normally found on an 80C31's pin 31 ($\overline{EA}$) controls access to external memory. As the 80C31 used on the 687C31 always accesses external memory, this pin is connected to ground within the substrate. The other special line is the combined input/output pin ALE/$\overline{PGM}$ (30). In operational mode the pin acts as the ALE-output from the EDH687C31. In the EDH687C31 programming mode, the pin is considered as an input for the EPROM programming signal - PGM. Programming and control of this operation is described later.

CPU

The CPU used on the EDH687C31 μPak is the Intel M80C31BH.

CONTROL LOGIC

The control logic consists of a High Speed CMOS Gate Array. The control logic operates in one of two possible ways; one when the μPak is operating and one when the μPak is being programmed. Under normal operations, the logic decodes the addresses in order to select the EPROM or the SRAM. The selection is controlled by either signals ALE, $\overline{PSEN}$,

$\overline{RD}$ or a combination. The control logic dictates the direction of the ALE/$\overline{PGM}$-pin (output or input).

In programming mode, the logic performs several functions. It controls the selection to the EPROM. It reverses the direction of the ALE/$\overline{PGM}$ pin, such that ALE/$\overline{PGM}$ becomes the programming input pulse for the EPROM. It also ensures that programming only takes place within the specified EPROM address area.

The control logic also incorporates the address separating latch needed in 80C31 systems.

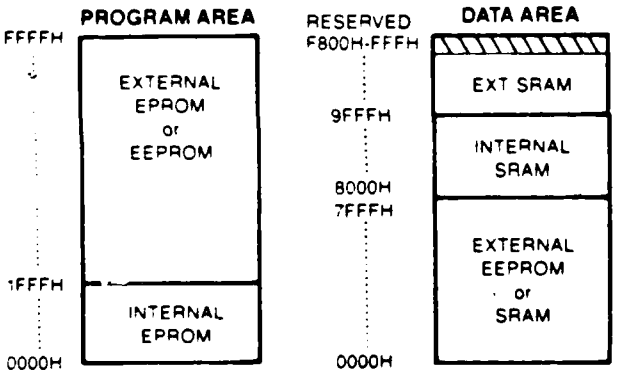
MEMORY

The static CMOS RAM and CMOS EPROM are industry standard products organized as 8Kx8.

MEMORY MAP

The basic memory map is as follows:

DUAL MAP MODE



The PROGRAM AREA is controlled exclusively by $\overline{PSEN}$ (Program Storage Enable) which is only asserted during an instruction fetch cycle. Addresses 0000H to 1FFFH are allocated to the internal on-substrate EPROM. During normal program execution, memory in the PROGRAM AREA cannot be altered as there is no $\overline{WR}$ (WRITE) control line connected to it and all write cycles are routed to the DATA AREA. However, when the 87C31 is placed in the programming mode, by raising V_{PP} to the required programming voltage, the internal EPROM may be programmed on substrate by use of the Programming Adaptor.

The Data Area is controlled by the $\overline{RD}$ and $\overline{WR}$ lines and is accessed under program control to obtain or store data. The internal on-substrate RAM is allocated to addresses 8000H to 9FFFH with all other remaining addresses, except F800H and above, available for external memory. Addresses F800H to FFFFH are used for the POWER DOWN register and are not for general use. (See section on POWER DOWN REGISTER)

POWER DOWN REGISTER

In order for the 87C31 to consume as little power as possible during POWER DOWN, it is necessary to ensure that both the on-board EPROM and RAM are deselected. Because the 80C31 maintains its port data and brings both ALE and $\overline{PSEN}$ low when in POWER DOWN Mode, it is possible that a valid on-board memory address can be decoded resulting in the RAM or EPROM remaining selected.

To prevent this from taking place, a "POWER DOWN" register has been positioned at address F800H to FFFFH. This address is used internally on the LCU and is effectively a RAM location used to flag POWER DOWN mode entry. From the users standpoint only two points need consideration:

1. No external memory may be configured in the Data Area above address F7FFH.
2. The register address F800H must be written to (the data written is not important) immediately preceeding the instruction for entry into Power Down mode. A typical program flow is below:

"1" INTO ALL PORTS	Set All Ports To 1
M S B OF 8 REG. = CARRY BIT	Ensure That The M S B Of B Reg Equals The Carry Bit (80C31 Requirements)
WRITE TO ADDRESS F800H	Write To Power Down Register (Dat Not Crucial)
02H→ PCON	Enter Power Down Mode
	Power Down
RESET	Reset And Restart Execution
FIRST INS.	

After access to address F800H, and upon completion of the Power Down instruction, the LCU disables and takes high all "chip select" lines on the on-board EPROM and RAM irrespective of the address output on the 80C31 ports. In this way minimum current consumption is ensured.

PROGRAMMING

The "on-substrate" EPROM, used for program memory, may be programmed easily using a special programming adaptor between the EDH687C31 and standard EPROM programming equipment. The EDH60C31 Family Programming Adaptor, together with the on-substrate control logic, controls the programming sequence. It sets up the conditions needed; activates the necessary control lines and routes the data and address lines between the μPak and the programming equipment. (See the EDH60C31 FPA Reference Manual for further information.)

The actual programming of the EDH687C31's EPROM is similar to programming an ordinary EPROM. Programming time is the same and the programming voltage, V_{PP}, is the same. A brief description of the EDH60C31 FPA operation, for programming an EDH687C31 follows:

When the programming voltage V_{PP} is raised to the correct level, the EDH60C31 FPA will enter the programming mode. A reset is issued to the EDH687C31, causing the 80C31BH CPU to go into reset (high impedance port input lines) and the on-substrate control logic to enter programming mode as well. The on-substrate control needs both the active reset line and V_{PP}, at programming level, before entering the mode. Programming will now take place as for any EPROM. After programming, the programming equipment verifies the content of EPROM and this is done with $V_{PP}=V_{CC}$.
This change in V_{PP} causes the on-substrate control logic to enter verify mode (reset still active), and verification can take place.

Programming of the EDH687C31 μPak, with the EDH60C31 FPA can be performed on all commonly available EPROM programmers.

		DUAL MAP MODE	
TOTAL MEMORY		128K BYTES	
DATA AREA		64K BYTES (2K BYTES RESERVED)	
PROGRAM AREA		64K BYTES	
INTERNAL MEMORY	EPROM	DATA AREA	PROGRAM AREA
			8K BYTES ADDRESS 0-1FFFH
	SRAM	8K BYTES ADDR 8000H-9FFFH	
EXTERNAL MEMORY	EPROM/ SRAM/ EEPROM	54K BYTES ADDR 0-7FFFH & A000H-F7FFH	56K BYTES ADDR 2000H-FFFFH

EMULATION

Two methods are available for emulation of the 687C31 for software design purposes. In one method, a full Intel development system can be used. Instructions are then executed from the Intel development system's internal memory.

For the second method, EDI has developed an emulation board containing all necessary logic and memory. This emulation board allows for utilization of either a DIP 80C31 or a smaller PDS (personal development system). These PDSs are capable of emulating adequate amounts of memory.

ABSOLUTE MAXIMUM RATINGS*

Case Temp under bias	−55 to +125°C
Storage Temp	−65 to +150°C
Voltage on V_{PP} to V_{SS}	−2.0 V to 13.5 V
Voltage on any other Pin to V_{SS}	−0.1 V_{SS} to V_{CC} +0.3 V
Voltage on V_{CC} to V_{SS}	−0.3 V to +6.5 V
Power Dissipation	0.8 W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Maximum Operating Current (Note 1)

I_{CCOP} (mA)

	V_{CC}		
Freq.	4.5V	5V	5.5V
3.5 MHz	9.5	10.5	11.5
8.0 MHz	15	16	17

Maximum Idle Current (Note 2)

I_{DC} (mA)

	V_{CC}		
Freq.	4.5V	5V	5.5V
3.5 MHz	5.5	6	7
8.0 MHz	6	7.5	8

NOTES

(1) I_{CC} is measured with all output pins disconnected. XTAL1 is driven with TCLCH, TCHCL = 5 NS, V_{IL} = .5 V, $V_{IH} = V_{CC} - .5$V, XTAL2 N.C. RST = Port 0 = V_{CC}. I_{CC} would be slightly higher if a crystal oscillator is used.

(2) Idle I_{CC} is measured with all output pins disconnected, XTAL1 is driven with TCLCH, TCHCL = 5 NS, V_{IL} = .5 V, $V_{IH} = V_{CC} - .5$ V, XTAL2 N.C., Port 0 = V_{CC}, RST = V_{SS}.

(3) Case temperatures are instant on.

(4) Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE, and Ports 1 and 3. The noise is due to the external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1 to 0 transition during bus operations. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such case it may be desirable to qualify ALE with a Schmitt Trigger for exeternal use.

(5) Power Down I_{CC} is measured with all outputs disconnected, Port 0 = V_{CC}, XTAL2 N.C., RST = V_{SS}.

D.C. CHARACTERISTICS (Note 3)

(T_C = −55°C to +125°C, V_{SS} = 0V, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
Input Low Voltage	V_{IL}	−0.1	0.65	V		
Input High Voltage (Except XTAL1, RST)	V_{IH}	2.2	V_{CC} +0.5	V		
Input High Voltage XTAL1 and RST	V_{IH1}	3.5	V_{CC} +0.5	V		
Output Low Voltage (Port 1,2,3)	V_{OL}		0.45	V	I_{OL}=1.6 mA	
Output Low Voltage (P0, ALE / $\overline{PGM}$, $\overline{PSEN}$)	V_{OL1}*		0.45	V	I_{OL}=3.2 mA	4
Output High Voltage (Ports 1,2,3)	V_{OH}*	2.4		V	I_{OL}=75 μA	*
Output High Voltage (P0 in Ext Bus Mode, ALE / $\overline{PGM}$, $\overline{PSEN}$)	V_{OH1}*	2.4		V	I_{OL}=375 μA	*
"0" Input Current (Ports 1,2,3)	I_{IL}		−85	μA	V_{IN} = 45V	
Logical 1 to 0 Transition Current (Ports 1,2,3)	I_{TL}		−775	μA		
Input Leakage Current (Port 0)	I_{LI}	+25	−25	μA	45 V < V_{IN} < V_{CC}	
RST Pulldown Resist	R_{RST}	50	150	KΩ		
Pin Capacitance (Port 0,2)	C_{IO1}		35	pF	Test Freq.=1 MHz, T_A=25°C	
Pin Capacitance (All Other Pins)	C_{IO2}		15	pF		
Average Operating Current	I_{CCAVE}		45	mA	V_{CC}=5.5 V, F = 8 MHz	
Power Down Current	I_{PD}		490	μA	V_{CC} = 4 to 5.5V	5
V_{PP} Supply Current	I_{PP}		100	μA	V_{PP} = V_{CC}	

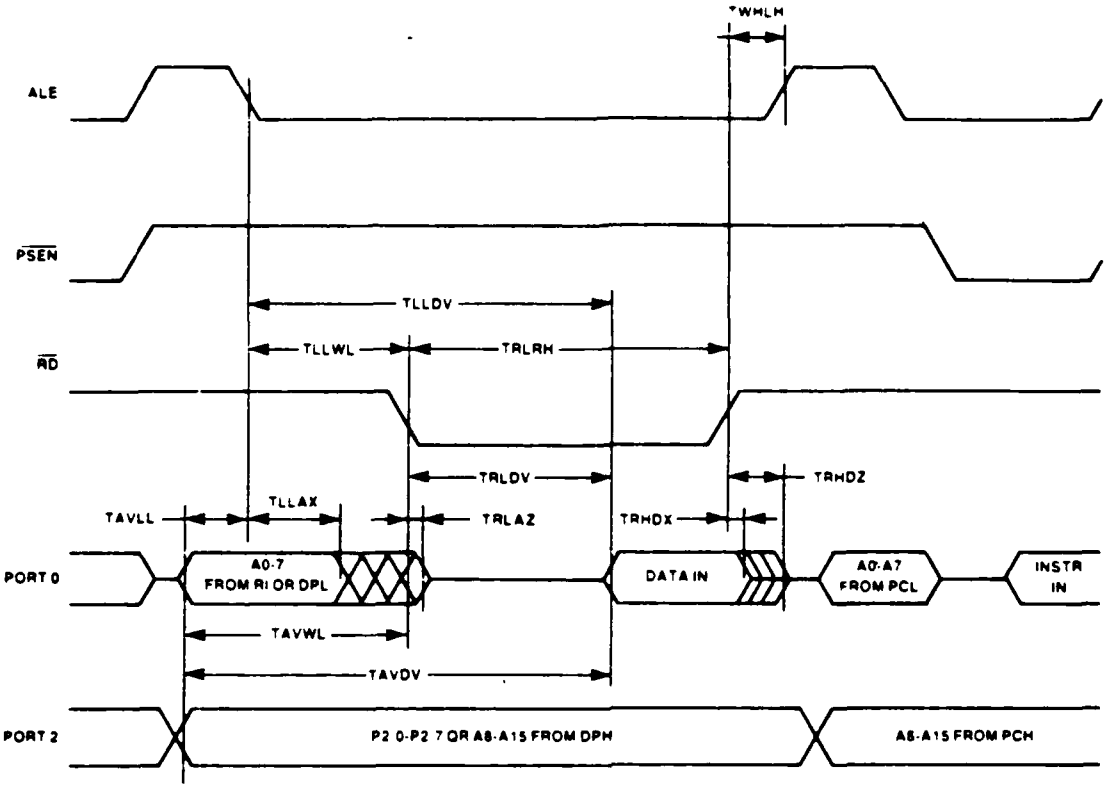
*Guaranteed, but not tested.

A.C. CHARACTERISTICS (Note 3)

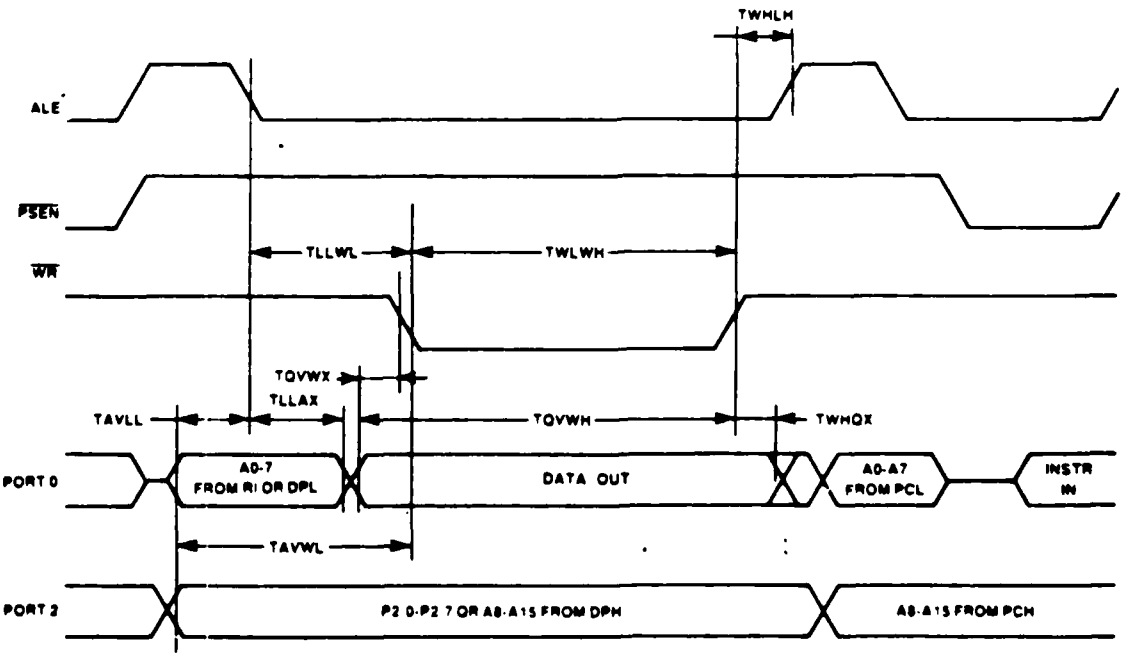
(T_C = −55°C to +125°C, V_{CC} = 5V ±10%, V_{SS} = 0 V).
Load capacitance for Port 0, ALE and $\overline{PSEN}$ = 80 pF.
Load capacitance for all other outputs = 70 pF.

PARAMETER	SYMBOL	8 MHz		VARIABLE OSCILLATOR		UNIT
		MIN	MAX	MIN	MAX	
ALE Pulse Width	TLHLL	195		2TCLCL-55		ns
Address Valid to ALE Low	TAVLL	65		TCLCL-70		ns
Address Hold After ALE Low	TLLAX	75		TCLCL-50		ns
ALE Low to Valid Instruction In	TLLIV		385		4TCLCL-115	ns
ALE to $\overline{PSEN}$ Low	TLLPL	70		TCLCL-55		ns
$\overline{PSEN}$ Pulse Width	TPLPH	315		3TCLCL-60		ns
$\overline{PSEN}$ Low to Valid Instruction In	TPLIV		255		3TCLCL-120	ns
Input Instruction Hold After $\overline{PSEN}$	TPXIX	0		0		ns
Input Instruction Float After $\overline{PSEN}$	TPXIZ		85		TCLCL-40	ns
Address to Valid Instruction In	TAVIV		505		5TCLCL-120	ns
$\overline{PSEN}$ Low to Address Float	TPLAZ		25		25	ns
$\overline{RD}$ Pulse Width	TRLRH	650		6TCLCL-100		ns
$\overline{WR}$ Pulse Width	TWLWH	650		6TCLCL-100		ns
$\overline{RD}$ Low to Valid Data In	TRLDV		440		5TCLCL-185	ns
Data Hold After $\overline{RD}$	TRHDX	0		0		ns
Data Float After $\overline{RD}$	TPHDZ		165		2TCLCL-85	ns
ALE Low to Valid Data In	TLLDV		830		8TCLCL-170	ns
Address to Valid Data In	TAVDV		940		9TCLCL−185	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	TLLWL	310	440	3TCLCL-65	3TCLCL+65	ns
Address to $\overline{RD}$ or $\overline{WR}$ Low	TAVWL	355		4TCLCL-145		ns
Data Valid to $\overline{WR}$ Transition	TQVWX	50		TCLCL-75		ns
Data Hold After $\overline{WR}$	TWHQX	60		TCLCL−65		ns
$\overline{RD}$ Low to Address Float	TRLAZ		0		0	ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High	TWHLH	60	190	TCLCL-65	TCLCL+65	ns
Oscillator Frequency	1/TCLCL			3.5	8.0	MHz

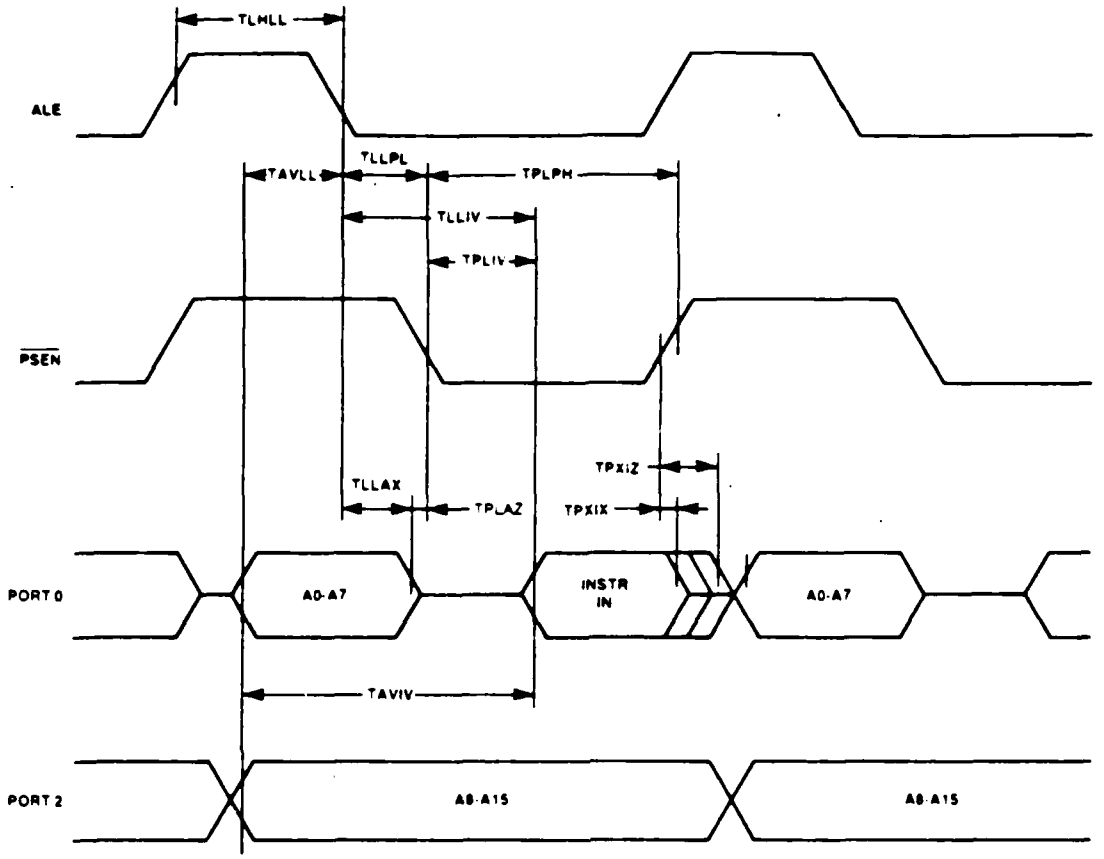
EXTERNAL DATA MEMORY READ CYCLE



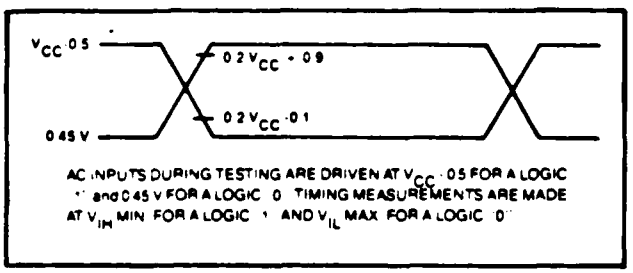
EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL PROGRAM MEMORY READ CYCLE

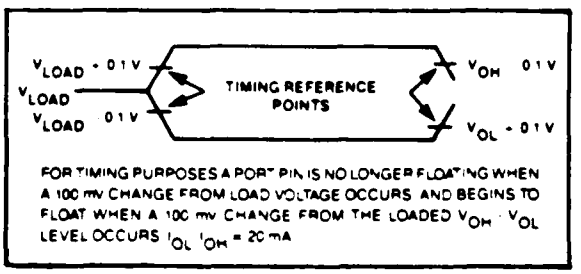


AC TESTING: INPUT, OUTPUT WAVEFORMS



AC INPUTS DURING TESTING ARE DRIVEN AT V_{CC} - 0.5 FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT V_{IH} MIN. FOR A LOGIC "1" AND V_{IL} MAX. FOR A LOGIC "0".

FLOAT WAVEFORM



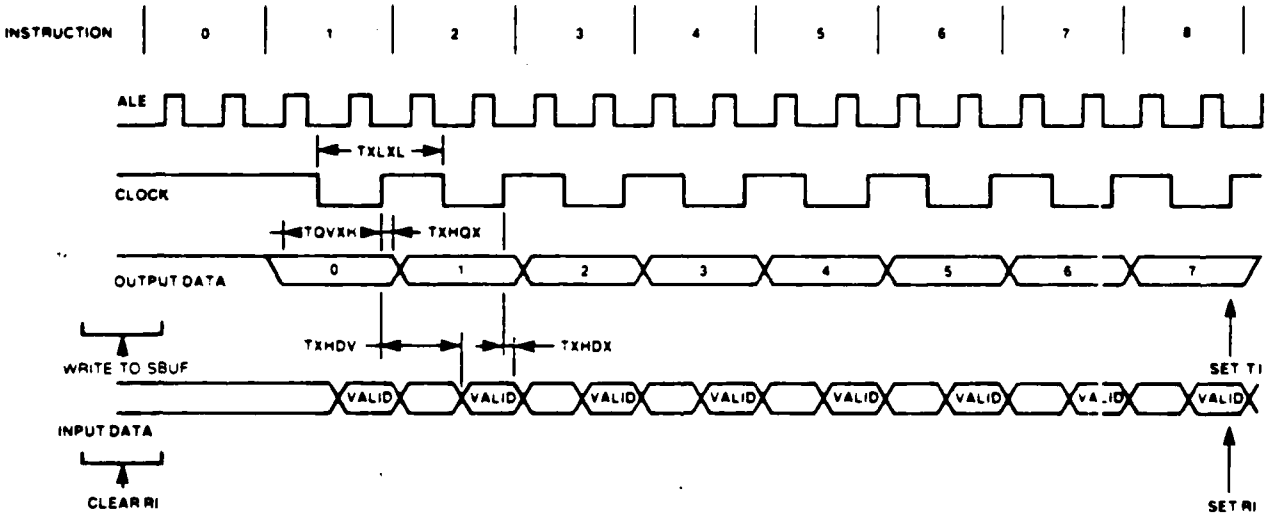
FOR TIMING PURPOSES A PORT PIN IS NO LONGER FLOATING WHEN A 100 mV CHANGE FROM LOAD VOLTAGE OCCURS AND BEGINS TO FLOAT WHEN A 100 mV CHANGE FROM THE LOADED V_{OH}/V_{OL} LEVEL OCCURS. I_{OL}/I_{OH} = 20 mA.

SERIAL PORT TIMING — SHIFT REGISTER MODE (Note 3)

Test Conditions: T_C = −55°C to +125°C; V_{CC} = 5 V ±10%; V_{SS} = 0 V; Load Capacitance = 70 pF

PARAMETER	SYMBOL	8 MHz OSC		VARIABLE OSCILLATOR		UNITS
		MIN	MAX	MIN	MAX	
Serial Port Clock Cycle Time	TXLXL	1.5		12TCLCL		μs
Output Data Setup to Clock Rising Edge	TQVXH	1 12		10TCLCL-133		μs
Output Data Hold After Clock Rising Edge	TXHQX	133		2TCLCL-117		ns
Input Data Hold After Clock Rising Edge	TXHDX			0		ns
Clock Rising Edge to Input Data Valid	TXHDV		1 12		10TCLCL-133	μs

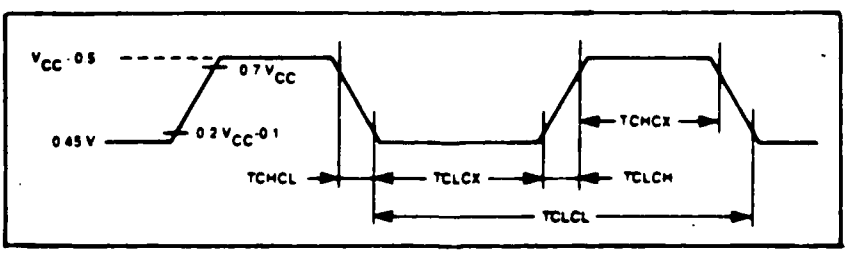
SHIFT REGISTER TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

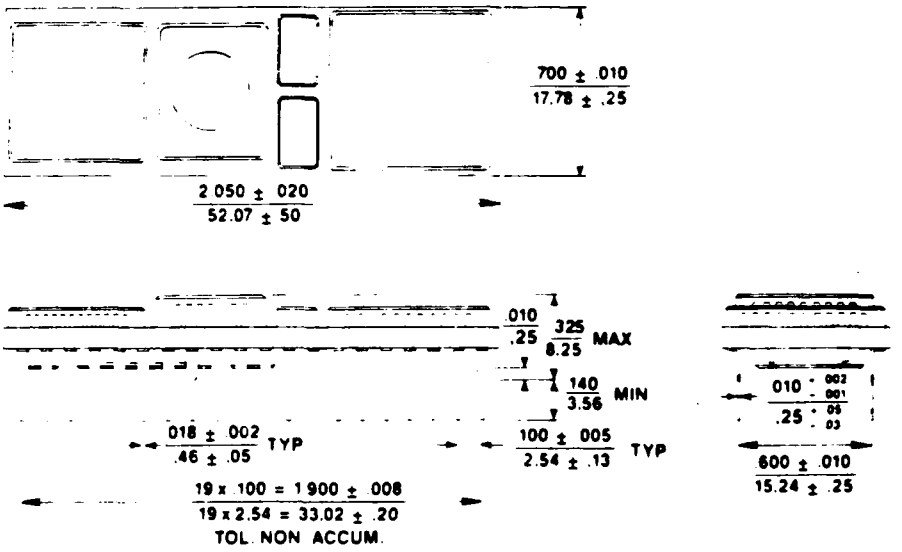
PARAMETER	SYMBOL	MIN	MAX	UNITS
Oscillator Frequency	1/TCLCL	3.5	8	MHz
High Time	TCHCX	42.5		ns
Low Time	TCLCX	42.5		ns
Rise Time	TCLCH		20	ns
Fall Time	TCLCH		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



DIMENSIONS

INCHES
MILLIMETERS



ELECTRONIC DESIGNS INC
35 South Street
Hopkinton MA 01748 USA
Phone (617) 435-9077 TELEX 948004

ELECTRONIC DESIGNS EUROPE
Shelley House
The Avenue Lightwater
Surrey GU18 5RF United Kingdom
Phone—(0) 276 726 37 TELEX—858325

6.0 Components

At present this section exhibits lists of representative components. The final report will have expanded data on the components used in the brassboard model.

Representative Circuit Components

Memory

Mfr.	Desig.	Type	Icc			Cycle Time	Volume	
			OP.	Std. By	P-t.		DIP	LCC
Harris	6516	Static RAM 2K×8	10ma @ 1MHz	.05ma.	.025ma @ V_{cc}=2V.	~200 n. Sec.	1.27×.62×.18 ~.14 in³	.46×.56×.20 ~.03 in³
Hitachi/ Fujitsu	27C64	UVEPROM 8K×8	8ma @ 1MHz	.1 ma	—	~300 n. Sec.	1.37×.4×.21 ~.12 in³	.46×.56×.13 ~.04 in³
National	27C16	UVEPROM 2K×8	5ma @ 1MHz	.1 ma	—	~500 n. Sec.	1.29×.53×.23 ~.16 in³	—
National	27C32	UVEPROM 4K×8	5ma @ 1MHz	.1ma	—	~500 n. Sec.	~.16 in³	—

Controller

Mfr.	Desig.	Icc		Features
		OP	Idle	
Intel	80C31 (8 bit)	1.2f + 1.6ma (f in MHz)	1.6ma (50μa Power down)	128K mem. Address (64K prog., 64K data), 128×8 RAM, 2 Timers, UART Serial port, Ports, on chip clock, Software multiply & divide. Volume: DIP 2.1×.62×.23 = ~.3in³ LCC .66×.66×.11 = ~.05in³

Representative Circuit Components

A/D Converter

Mfr.	Desig.	Icc	IREF	Features
National	ADC0844	2.5ma ($\overline{CS}$ hi)	2ma	3 bit parallel out with tri state latch, 4 channel input multiplexer, single +5V operation. 40μs/channel conv. Volume: DIP .985 × .32 × .2 = ~.07 in³ LCC .65 × .65 × .08 = ~.04 in³
Texas I.	TLC549	2ma ($\overline{CS}$ Lo)	1ma	8 bit serial out. Single +5 V. operation. 10 μs. conv. time. Volume: DIP .4 × .31 × .2 = ~ .03 in³

D/A Converter

		Features
National DAC083X	2ma	8 bit double buffered. Single +5V operation Volume: DIP 1.01 × .3 × .165 = ~.05 in³
MicroPower Systems MP7628	.5ma (inc. REF current)	8 bit buffered. 4 converters. Single +5V operation. Volume: DIP 1.46 × .6 × .22 = ~ 0.2 in³

Representative Circuit Components

Operational Amplifier

Mfr.	Desig.	I_s	Gain-Bandwidth	Slew rate	Features
Harris	HA5114XA	75μa/amp.	400KHz	1V./μsec	Single Dual or Quad Op Amp. Single or dual supply Op. 5mv offset. (3μv/°c) 20nv/$\sqrt{Hz}$ to 1KHz Volume: Quad. .79×.31×.17 = .04 in³ Dip
PMI	OP220	170μa.	100KHz	.05V/μsec	Dual Op Amp. Single or dual supply. 0.3mv offset. 40nv/$\sqrt{Hz}$ at 1KHz Volume: DIP
PMI	OP221	550μa	~500KHz	.2V/μsec.	Dual Op Amp. Single or dual supply. 0.3mv offset. (1.5μv/°c) 20nv/$\sqrt{Hz}$ at 1KHz Volume as for OP220.

Comparator

Mfr.	Desig.	I_s	Features
Linear Technology	LTC1040	~30μa	A dual, differential micropower comparator. Single or dual supply Operation. Sampling rate ext. driven or by int. osc. Volume: DIP .92×.32×.2 = .06 in³

Representative Circuit Components

Filters

Mfr.	Design	I_s	Offset (max)	
Linear Technology	LTC1060	4ma (5V. Supply)	60m.V.	A Switched Capacitor, Universal, 2 two pole filter. Configure to 4 poles. 100 to 1 Clock to f_c. Volume: DIP $1.06 \times .33 \times .2 = \sim .07 in^3$
"	LTC1062	10ma	0	A Switched Capacitor, 5th order Low Pass filter. 100 to 1 Clock to f_c. Volume: DIP $.41 \times .32 \times .2 = \sim .03 in^3$
National	MF-4	3.5ma. (10V. Supply) 2.25ma (5V. Supply)	-400mV.	A 4th order, Butterworth, low pass filter. 100 to 1 Clock to f_c. Volume: DIP $.4 \times .28 \times .2 = \sim .03 in^3$

Representative Circuit Components

Switches/Multiplexers

Mfr.	Desig.	Type	Supply	Switch Res.	
Harris	HI-5043	CMOS Dual SPDT	1.5 ma ±	75Ω	Volume: DIP .79 × .31 × .2"
Siliconix	DG307A	CMOS Dual SPDT	0.1 ma ±	75Ω	Volume: DIP .79 × .31 × .2"

Instrumentation Amplifier

Mfr.	Desig.	Type	Supply	
National	LH0036	Classic 3 OP Amp	0.4ma ± 5V	Currently packaged in a TO8 can .56dia, .18 high

7.0 Transducers

Standard instrumentation amplifiers will comprise the input sections of the two data channels. These amplifiers can accept signals from virtually any type of transducer of interest to the end user.

The transducer set comprises two categories, namely those powered by the system and those powered by some external source.

The recorder is designed to drive strain based transducers. The projected drive system is described in paragraph 5. Some representative transducers are shown in exhibit 1. In that exhibit, the Entran accelerometer, I.C. pressure sensors and Columbia strain gages are examples of the strain based transducers under consideration. The Aerodyne acceleration switch represents a device that would be used for detecting such events as catapults and arrests.

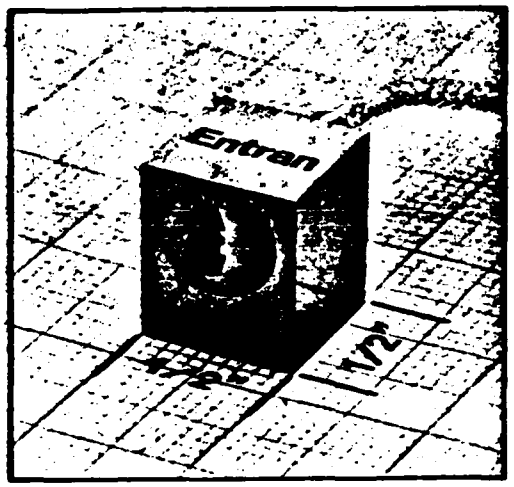
If the recorder is to be used with a transducer that is not powered by the system, care must be taken to avoid overdriving the input amplifiers. The user must also provide a ground return between the external device and the recorder to prevent saturation of the recorder's input instrumentation amplifiers.

EXHIBIT 1

Representative Transducers

Entran Devices, Inc.

EGC-500DS-20



EGC-500DS Series
Miniature Heavy Duty Accelerometers

- **5g TO 5000g RANGES**
- **200mV FULL SCALE**
- **DAMPING & OVERRANGE STOPS**
- **STEADY STATE AND DYNAMIC RESPONSE**

The EGC-500DS is a heavy duty miniature accelerometer. Created for on-site testing where rugged construction and overload protection is of paramount importance. The EGC-500DS is ideal for acceleration, vibration and shock measurements and has become the work-horse of testing engineers.

The EGC-500DS is a true miniature accelerometer, weighing only as little as 10 grams, but built to withstand high overloads in operation and installation. Entran's EGC-500DS is both damped, eliminating resonance, and fitted with mechanical stops to impede overload response. The standard unit has an overrange rating of 1000% Full Scale and higher ranges are available on request.

The EGC-500DS operates in both static (steady state) and dynamic measurement of acceleration, vibration and shock. Its high full scale output can be used without amplification and can directly interface with most readout instrumentation. This can eliminate costly and intricate signal conditioning.

The EGC-500DS accelerometer has a fully active semiconductor strain gage bridge and is fully compensated for temperature variations in the environment. The EGC-500DS is available in full scale "g" ranges from 5g to 5000g in single and multiaxial configurations, and comes with damping and overrange stops as standard equipment. Typical applications range from Automotive Crash and Barrier Testing, to Industrial Vibration Monitoring, to Ballistic Missile Flight Test.

Entran Devices, Inc.
10 Washington Avenue
Fairfield, N.J 07006, USA
(201) 227-1002, Telex 130361

Entran Bulletin **EGC500DS-183**

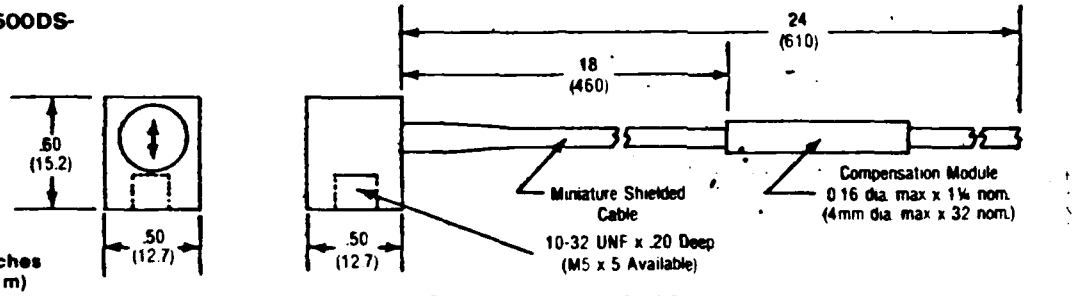
SPECIFICATIONS

MODEL	EGC-500DS -5	EGC-500DS -10	EGC-500DS -20	EGC-500DS -50	EGC-500DS -100	EGC-500DS -200	EGC-500DS -500	EGC-500DS -1000	EGC-500DS -2000	EGC-500DS -5000
RANGE	±5g	±10g	±20g	±50g	±100g	±200g	±500g	±1000g	±2000g	±5000g
[1] OVERRANGE	±50g	±100g	±200g	±500g	±1000g	±2000g	±5000g	±10000g	±20000g	±50000g
SENS. mV/g nom.	25	20	10	4	2	1	0.4	0.2	0.1	0.04
[2] RES. FREQ. nom.	370 Hz	500 Hz	800 Hz	1500 Hz	2300 Hz	2800 Hz	3500 Hz	4000 Hz	5000 Hz	7000 Hz

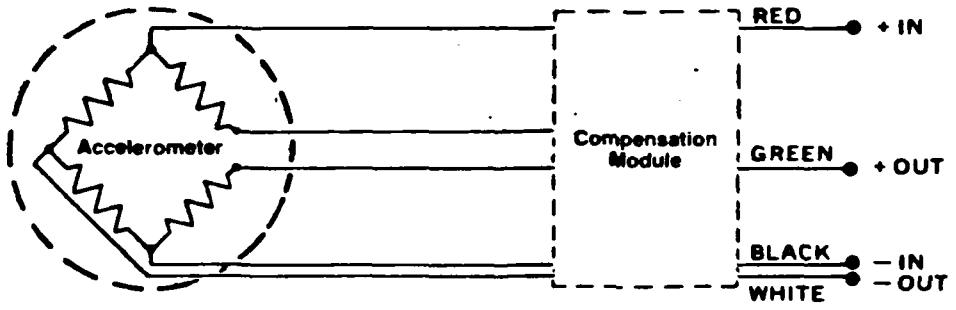
[1] Overrange valid at all frequencies. [2] Useful frequency range is 30% of Resonant Frequency minimum, but may be as high as 50%. [3] Damping is nominally 0.7cr at 80°F but can range from 0.3 to 1 cr. [4] Zero offset of ±15mV max at 80°F after warm-up. Lower values available on request. [5] ±2½%/100°F for 5g Model. [6] Other Excitations and Temperature Ranges available on request.

NON-LINEARITY	±1%	INPUT IMPEDANCE nom.	1000Ω: 2000Ω optional
TRANS. SENS.	3% max.	OUTPUT IMPED. nom.	450Ω: 900Ω optional
THERMAL ZERO	[4,5] ±1%F.S./100°F	EXCITATION	[6] 15VDC
THERMAL SENS.	±2½%/100°F	COMPENSATED TEMP.	[6] 70°F to 170°F (21°C to 77°C)
DAMPING	[3] 0.7cr nom.	OPERATING TEMP.	[6] -40°F to 250°F (-40°C to 121°C)
USEFUL FREQ. RANGE	[2] 30% to 50% Res. Freq.	WEIGHT (without cable)	Steel: 20gms Al: 10gms

EGC-500DS-

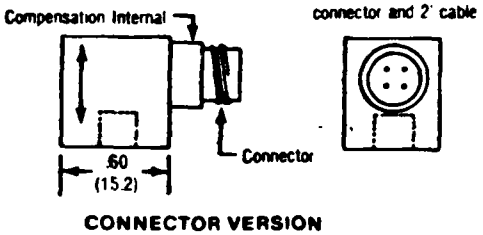


DAMPING AND OVERRANGE STOPS ARE STANDARD



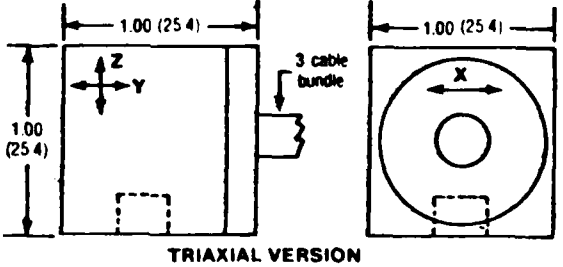
Entran

EGC-500DSC-



CONNECTOR VERSION

EGC3-500DS-



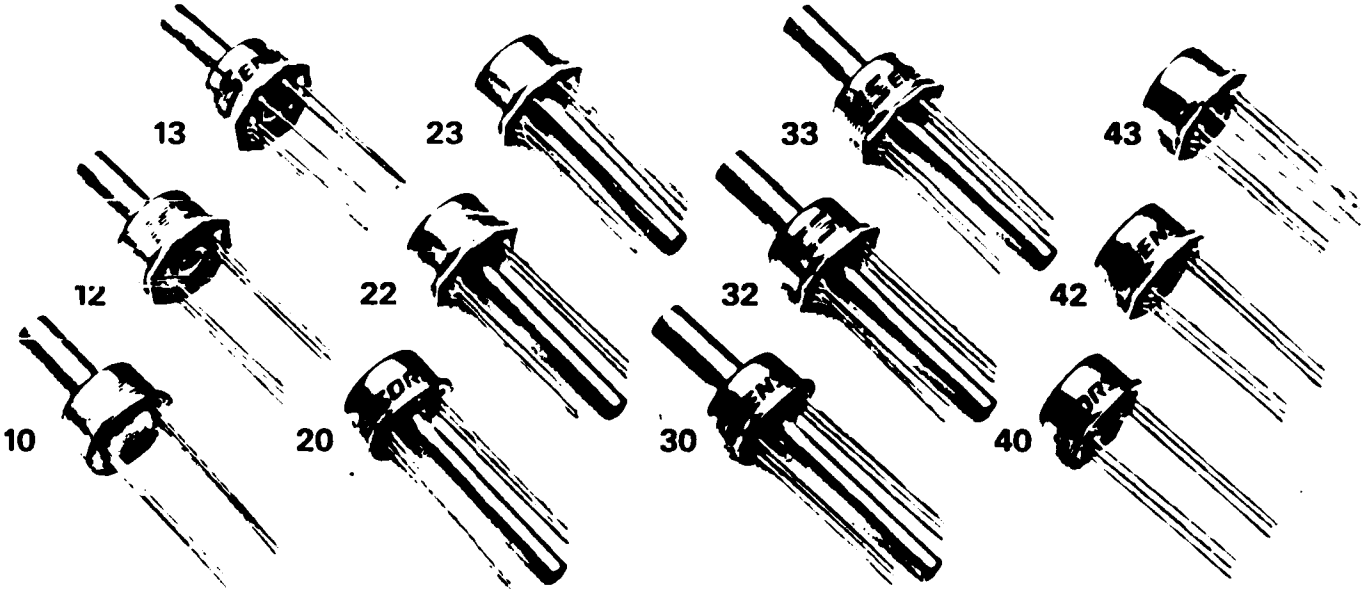
TRIAXIAL VERSION

Entran Devices, Inc.
10 Washington Avenue
Fairfield, N.J. 07006, USA
(201) 227-1002, Telex 130361

Specifications subject to change without notice.

Pressure Sensors
Selection Guide
PC Board Mountable

	Gage & Absolute Non-Corrosive Gases General Purpose	Gage Corrosive Liquids Media Compatible	Differential Gases/Liquids Bi-Directional	Gage & Absolute Non-Corrosive Gases Compact Size
Interchangeable	13	23	33	43
Integral Temperature Compensation	12	22	32	42
External Resistor Values Supplied	10	20	30	40



Models 10 thru 43—Selected Features

- Piezoresistive
- Constant Current
- Performance Graded
- 0-5 to 0-250 PSI
- 3X Overpressure
- 0.1% Accuracy
- 100 mV Output
- Ratiometric
- Low Power
- 0-50°C Compensation
- .02%/°C Span TC
- .02%/°C Zero TC
- 0.2% LTS
- Serialized
- Low Cost

Pressure Sensors Selection Guide PC Board Mountable

Silicon Sensing Element

The sensing element in each device is an integrated circuit silicon chip with a micromachined diaphragm. Four piezoresistive strain gage resistors are diffused into the diaphragm to form a fully active Wheatstone Bridge.

The silicon diaphragm deflects upon the application of pressure which results in an electrical output that is proportional to the input pressure. The single crystal nature of the diaphragm assures a pressure hysteresis that is essentially unmeasurable.

Package Configurations

The four package types used are modifications of the basic TO-8 metal can structure. Pressure can be applied to either the top (top entry) of the package, the bottom (bottom entry) or a combination of both.

In the top entry design the pressure media is applied to the circuit side of the chip which is covered with a protective silicone gel that offers moderate protection to the media. This design is intended for non-corrosive gases and is not recommended for liquids. Models 10-12-13-40-42-43 utilize this structure to measure absolute and gage pressures.

In the bottom entry design the pressure media is applied to the non-circuit or back side of the chip. The attachment scheme or construction is such that the only wetted materials are silicon, gold and glass, which makes this design ideal for most corrosive liquids and gases. Models 20-22-23 are bottom entry and measure gage pressures.

Models 30-32-33 measure differential pressure in a dual port design that utilizes a combination of both the top and bottom entry structures. The reference (top port) media must, of course, be compatible with the silicone gel material.

Temperature Compensation & Calibration

In each package series there are several options with differing performance parameters.

Models 10-20-30-40 are supplied with a computer printout that specifies the necessary external compensation resistors.

Models 12-22-32-42 are provided with integral temperature compensation and zero balancing over 0-50°C with laser trimmed resistors. No external resistors are required.

Models 13-23-33-43 contain integral temperature compensation, zero balance and an additional laser trimmed resistor to normalize pressure sensitivity variations by programming the gain of an external amplifier, thus providing ± 1% interchangeability along with high level output.

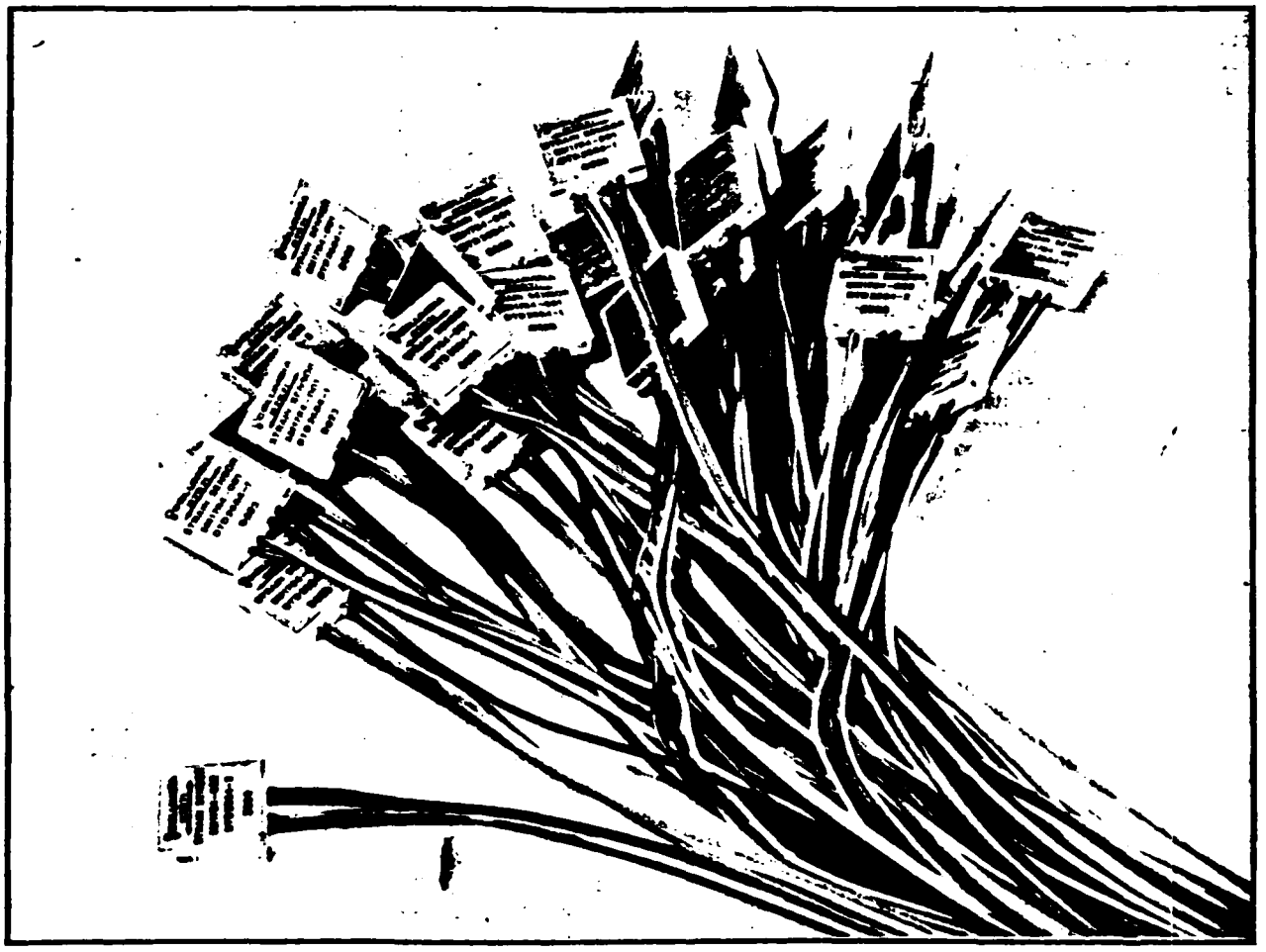
Quality Assurance

Each sensor is both pressure and temperature tested and marked with a unique serial number prior to shipment. Complete traceability is possible back to the wafer. Type testing is performed on every lot and internal quality control reports are generated on all devices.

Applications Assistance

IC Sensors has the experience to assist you with your applications requirements. Products are available at all levels, from the basic chip to a fully compensated transducer. Both standard and custom.

COLUMBIA
RESEARCH LABORATORIES, INC.
WOODLYN, PA 19094



STRAIN SENSORS FOR FATIGUE LOAD MONITORING

BULLETIN 106

- HIGH ACCURACY
- SELF TEMPERATURE COMPENSATING
- ENVIRONMENTAL RESISTANT
- EASE OF INSTALLATION
- HIGH OUTPUT - TWO ACTIVE ARMS
- RUGGED CONSTRUCTION

PREDICTING FATIGUE FAILURE OF AIRCRAFT STRUCTURES

The COLUMBIA 2680 Series of strain sensors are integral, full-bridge, temperature compensated, strain gage transducers designed specifically for fatigue-life monitoring of structural elements of high performance aircraft. The 2680 Sensors are self-temperature compensating, with models available for all materials commonly used in aircraft structural fabrication. They are designed for ease of installation by instrument technicians in the field or by manufacturing personnel in the airframe assembly plant, achieving the highest installed accuracy possible for this critical application. The replacement of counting accelerometer systems with direct strain measurement or strain exceedance counting systems can provide the optimum solution for fleet damage monitoring programs.

WHY FATIGUE LOAD MONITORING?

In 1970, the North Atlantic Treaty Organization's Advisory Group for Aerospace Research and Development (AGARD) presented its Advisory Report #28 on fatigue load monitoring of military aircraft. This report resulted from a study conducted by AGARD on fatigue level control of tactical aircraft. The conclusion of this report recommended the development of a strain recording system for monitoring fatigue loads experienced by tactical aircraft in service. The purpose of this monitoring system is to facilitate the prediction of potential fatigue induced failures of aircraft structural components and allow the scheduling of timely maintenance and replacement operations. The result of such an orderly and timely servicing routine would result in a higher level of flight safety, and maximize the number of tactical aircraft available for service.

STRAIN MEASUREMENT

A major impediment to the implementation of an effective fatigue-load monitoring program has been the strain gage technology itself. The bonding and inter-wiring of strain elements and the awkward schemes employed to obtain temperature stable operation, have effectively limited their use to test laboratory personnel and short term usage due to their fragility when exposed to the rigors of operational environments. The uncertainty of data accuracy obtained under such conditions tends to compromise the confidence placed in conclusions or predictions based upon these measurements. The development of the integral strain sensor, in cooperation with the U.S. Naval Air Development Center, was a direct response to the inaccuracies and high cost of the measurement techniques then available.

COLUMBIA, with its 2680 Series of integral strain sensors, now makes available to the civilian and military aircraft industries the ideal device for obtaining accurate, reliable strain measurements on critical airframe components. The cost in time and labor for installation of these gages is reduced to a level which permits their use in many areas that were previously impractical or impossible.

APPLICATIONS

The COLUMBIA Fatigue-Monitor Strain Sensor may be bonded to critical airframe surfaces using conventional strain-gage bonding techniques. The unique construction and small size of the 2680 Series permits easy application with a new and higher level of accuracy and mechanical integrity. The four, #26 AWG, Teflon-insulated lead wires eliminate the tedious and difficult termination methods required with conventional strain gage installations. A final coating of flexible, waterproofing material provides additional environmental and mechanical protection.

In aircraft applications, the use of direct strain measurement in place of the counting accelerometer methods commonly in use for fatigue load monitoring provides a more accurate representation of the fatigue loading experienced by tactical aircraft under various conditions of speed, weight, and mission configuration. Critical areas, such as undercarriage structures and control surfaces may be more accurately monitored for potential fatigue damage induced by high stress maneuvers and high-g landings.

These rugged, easily installed sensors open up new areas of opportunity for monitoring critical structures in commercial aircraft as well as high-performance military tactical aircraft. By combining the strain sensors with level sensing and recording systems, a stress-related history can be maintained for structures or assemblies which may be subject to damage or abuse during maintenance and overhaul operations, as well as monitoring the stress loading encountered in normal flight operations. The use of stress histories in conjunction with established S-N (fatigue life) curves for commonly used materials will allow the development of safer, more cost-effective maintenance and overhaul programs thru the application of end-of useful life predictions.

ADDITIONAL USES FOR INTEGRAL STRAIN SENSORS

Although the COLUMBIA 2680 Series of strain sensors have been developed for the demanding requirements associated with tactical military aircraft, they are equally useful for performing many of the more common strain measurements encountered in the materials testing laboratory. It is, in fact, the outstanding simplicity, reliability, and ruggedness of these sensors that makes them suitable for routine laboratory use. The higher output levels associated with the two-active-arm configuration provide a more sensitive device yielding higher installed accuracy. The built-in dummy gages provide optimum temperature compensation for zero shift stability. The complete, full bridge strain sensor needs only the most basic signal conditioning equipment to provide accurate, reliable data for any temperature-compensated strain measurement requirement.

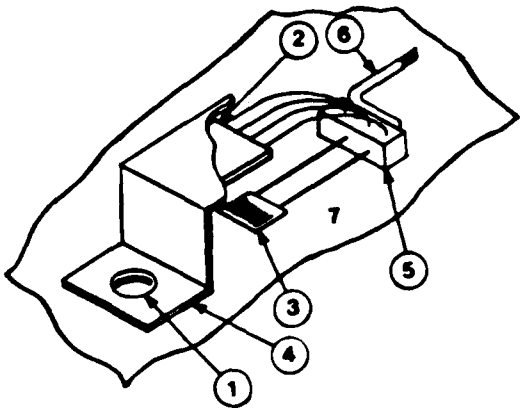


FIG. 1. TYPICAL INSTALLATION OF OLD-STYLE STRAIN GAGES

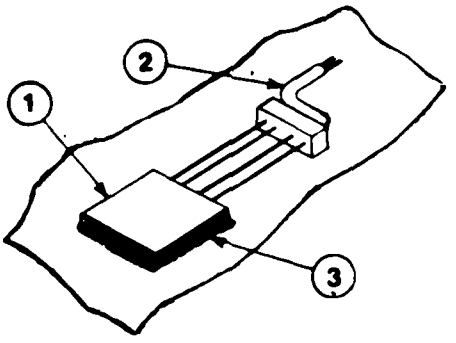


FIG. 2. INSTALLATION OF 2680 SERIES STRAIN SENSOR

1. Bolt or rivet removed from assembly.
2. Dummy gage(s) bonded to "Z Tab" of same material as structure.
3. Active gage bonded to structure under test.
4. "Z Tab" mounted to structure with bolt or rivet.
5. Strain gage leads interwired and soldered to junction block.
6. Lead wires routed to signal conditioning.
7. Entire unit covered with protective material.

1. Strain sensor bonded to surface under test.
2. Leads connected to wire harness.
3. Coat sensor and wires with waterproofing material.

ADVANTAGES

- Higher level of accuracy
- Twice the output
- Less installation time
- No loss of structural integrity
- Optimum temperature compensation

TYPICAL SPECIFICATIONS[1]

PERFORMANCE

Input Resistance: 1000 ohms, ±1%
Sensitivity: (±1%); 1.025 mV/V/1000 $\mu\epsilon$
Linearity: ±0.5% maximum
Zero Offset: ±0.5 mV/V typical
±1.5 mV/V maximum
Operating Range: -3500 to +5000 $\mu\epsilon$

Output Resistance: 1000 ohms, ±1%
Sensitivity Shift: ±.005%/° F
Hysteresis, Repeatability: ±0.5% max.
Zero Shift: ±.00025 mV/V/° F Typical
±.0005 mV/V° F maximum
Creep: <0.5%, 5 min., @5000 $\mu\epsilon$

ENVIRONMENTAL[2]

Temp. Range: -54° to +125° C
Vibration: 30 g, 10 to 2000 Hz
Humidity: MIL-STD-202, Method 106
Sand & Dust: MIL-STD-202, Method 110A
Salt Spray: MIL-STD-202, Method 101D
(168 hours)
Insulation Res: 100 meg. min @500 VDC

Dielectric Strength: 500 VRMS, 60 Hz, 1 min.
Altitude: Sea level to 70,000 ft.
Shock: 100 g, 11 msec.
Thermal Shock: MIL-STD-202, Method 107D
Flammability: MIL-STD-202, Method 111A
Fluids: Resistant to short term exposure to fuel, lubricating oils, and hydraulic fluids.

PHYSICAL

Size: .56 x .56 x .15 (inches)
(14,3 x 14,3 x 3,8 mm)
Leads: #26 AWG, Teflon ins, SPC, 12" min.

Encapsulant: Silicone rubber per MIL-S-23586A type 1, Class 2, Grade A
Weight: 10 grams
Matrix: .001" polyimide

[1]at +25° C [2]Installed Gage

Mac Dade Blvd. & Bullens Lane Woodlyn, Pa. (215) 872-3900

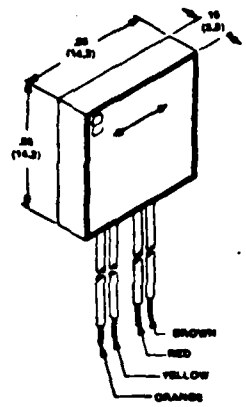


FIG. 3. DIMENSIONAL OUTLINE 2680 SERIES STRAIN SENSOR

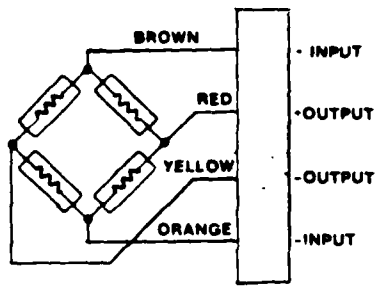


FIG. 4. CIRCUIT SCHEMATIC 2680 SERIES STRAIN SENSOR

PRICE LIST

TEMPERATURE COMPENSATION-ALUMINUM*

Model	1 Unit	2-5 Units	6-24 Units	25-99 Units	100-249 Units
2681	$283.00	$274.50	$268.50	$264.25	$256.25

TEMPERATURE COMPENSATION-STEEL*

Model	1 Unit	2-5 Units	6-24 Units	25-99 Units	100-249 Units
2682	$283.00	$274.50	$268.50	$264.25	$256.25

TEMPERATURE COMPENSATION-TITANIUM*

Model	1 Unit	2-5 Units	6-24 Units	25-99 Units	100-249 Units
2683	$283.00	$274.50	$268.50	$264.25	$256.25

TEMPERATURE COMPENSATION-GRAPHITE EPOXY*

Model	1 Unit	2-5 Units	6-24 Units	25-99 Units	100-249 Units
2684	$320.00	$310.50	$304.00	$295.00	$286.00

TEMPERATURE COMPENSATION-MAGNESIUM*

Model	1 Unit	2-5 Units	6-24 Units	25-99 Units	100-249 Units
2685	$295.00	$286.00	$281.00	$272.50	$264.00

*OTHER TEMPERATURE COMPENSATION MATERIALS AND RESISTANCE VALUES AVAILABLE — CONSULT FACTORY

PRICES AND SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

TYPICAL SPECIFICATIONS

The specifications as given are typical. Normal deviations and yield factors for the typical specifications may be obtained from the manufacturer upon request. Compliance to specific tolerances and implementation of MIL specifications are available upon special order. This is not to imply that all COLUMBIA units do not receive and meet final inspection and test in accordance with our procedures.

COLUMBIA RESEARCH LABORATORIES, INC.
Mac Dade Blvd & Bullens Lane Woodlyn, Pa. 19094

PHONE: (215) 872-3900
TWX: 510-669-3625

RICHARD B. GRAEB
Director of Sales and Marketing

Aerodyne Controls

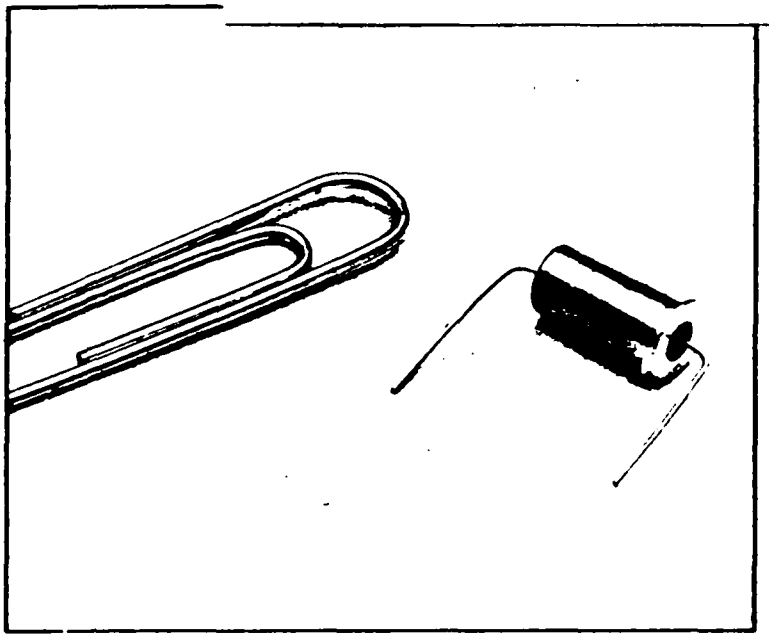
PNEUMATIC CONTROLS, ACCELERATION SWITCH

AERODYNE CONTROLS CORPORATION
PNEUMATIC CONTROLS - ACCELERATION SWITCHES

30 HAYNES COURT
RONKONKOMA, N.Y. 11779

516 737-1900
TWX 510-220-1137

MODEL 1990 ACCELERATION SWITCH



FEATURES

- Very Lightweight—Less Than 1.25 Grams
- Wide Set Point Range—1.25 to 1000 g; Accurate to ± 5%
- Wide Range of Applications
- Normally Open or Normally Closed Versions Available
- Can Turn Aircraft Emergency Transmitters and Flight Recorders On/Off
- Can Sense Launch, Spin, or Impact in Missiles
- Fully Flight Qualified
- Designed for Circuit Board Mounting

DESCRIPTION

The Aerodyne Model 1990 Acceleration Switch weighs only 1.25 grams, making it an ideal device in applications where weight is a critical factor. For example, in aircraft, helicopters, or missiles, it can be used to turn on the emergency transmitter or turn off the flight recorder after a specified time. In missile applications, it can be set to sense launch, spin, or impact.

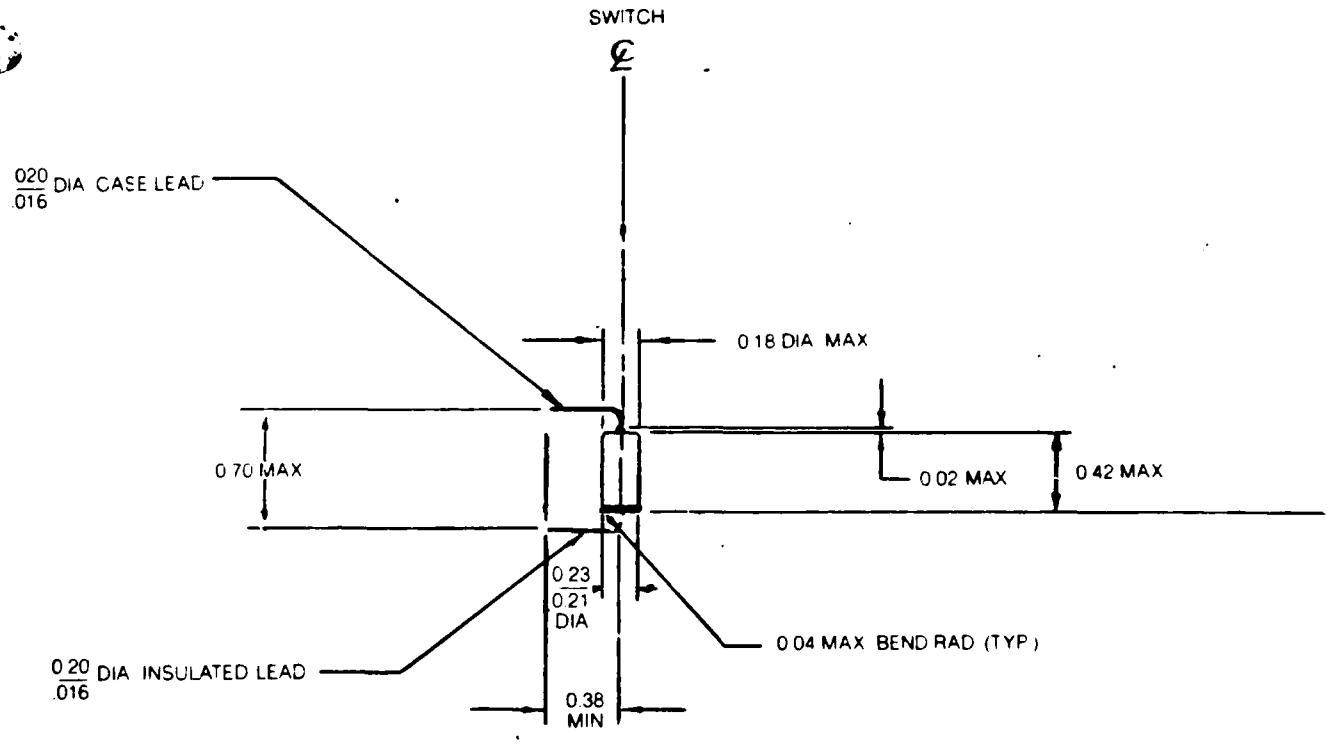
Available in a choice of normally open or normally closed switch configurations, the Model 1990 senses acceleration by the opening or closing of electrical contacts and is designed for circuit board mounting. The switch can be set for accelerations from 1.25 to 1000 g, typically with a ± 10% tolerance. A closer tolerance on set point is available. Fully tested and flight qualified, the Model 1990 has an operational temperature range from − 65°F to + 185°F.

Normally Closed
"Disturbance" Switch

MODEL 1990 ACCELERATION SWITCH

TYPICAL SPECIFICATIONS–Used as a Spin Switch

Weight:	1.25 grams
Contacts:	Single pole, single throw, normally open
Open Circuit Resistance:	10 megohms minimum at zero rps
Closed Circuit Contact Resistance:	a. Greater than 20,000 ohms at spin rates between 0 and 20 rps b. 0.25 ohm maximum at spin rates betwen 0 and 20 rps
Contact Rating at 35 VDC, Resistive Loads:	a. 200 ma continuous (2 minutes) b. 1.5 amperes, 10 cycles, 10 seconds on, 20 seconds off at 35 rps c. 10 amperes, 20 cycles, 0.050 second on, 0.450 second off at 35 rps
Spin Radius:	1.5 inch
Operating Temperature Range:	– 65 °F to + 185 °F
Launch Acceleration Environment:	a. 0 to 280 rps spin about spin axis in 2 milliseconds b. 20,000 g maximum for 10 milliseconds perpendicular to spin axis
Hermetic Seal:	Switch helium leak rate does not exceed 1×10^{-6} SCCS He at 1 atmosphere



ALL DIMENSIONS ARE IN INCHES

6.0 Power

The airborne recorder is self-contained - it will be battery powered.

The battery system selection centers on five attributes; they are energy density, cell voltage, current drive capability, wide temperature performance and medium operating life.

Fortunately, the lithium systems currently available fit the selection criteria. (It is interesting to note that a great deal of research effort is being expended in industry on these types of systems.) The commercially available lithium chemistries have:

1. Energy Density: range 2100 to 3400 joules/cm^3
2. Cell Voltage: range 2.8 to 3.5 volts (loaded)
3. Current: range to 500 ma
4. Temperature: -73 C to +175 C (not covered by the same cell type)
5. Operating Life: Well above the one month goal

Exhibit 1 is a good general paper (circa 1982) with a comparative discussion of battery types. Note figure 2 which compares energy densities and figure 5 showing cell voltages and discharge characteristics.

Exhibit 2 is a quick comparison of commercially available lithium cells - it is representative not exhaustive. This survey leads us to believe a plethora of choices for various applications are available.

In further pursuit of information on lithium batteries we have opened discussions with four battery suppliers - SAFT America, Electrochem Industries, Catalyst Research Corporation and Eagle Picher Industries. Thus far we have received a written response from SAFT America and Electrochem Industries.

A copy of our letter and the response from SAFT America is included in Exhibit 3. The letter reveals our current thinking on the system power requirements and the possibility of including EEPROMs to provide absolute data retention. (We had provisionally selected the thionyl chloride system before talking with the battery manufacturers.) Also included is a recent advertisement by SAFT. Exhibit 3 also contains the response from Electrochem Industries. Their response highlights two interesting points, namely the availability of high current pulse batteries and the use of different battery chemistries for different temperature range of operation.

Energy Budget

A preliminary energy budget allocating energy usage to system elements has been created. Figure 6.1 shows the allocation.

We are assuming a 750 hour installation (~1 month) split into 650 hours of standby and 100 hours of operation. With this assumption, the current values of figure 6.1 result in the following:

Operating	-	20.7 ma x 100 hours	=	2070 mah
Standby	-	0.5 ma x 650 hours	=	325 mah
				2995 mah

with 5 volt operation, this translates to

$$2.995 \times 5 \times 3600 = 53,901 \text{ Joules}$$

as the energy required to meet the specification goal.

The power requirements for the controller and memory are estimated as follows:

Controller - Intel 80C31. Power requirements (see par. 6.0) are (i) operating current 1.2f + 1.6 ma, (ii) idle current 1.6 ma, and (iii) power down current 0.05 ma. If we assume 3.5 MHz operation and 50% duty cycle we get an average of 3.7 ma and adding 20% for low temperature operation gives 4.5 ma.

Program Memory - 27C64 UV EPROM. Power requirements (see par. 6.0) are 6 ma at 1 MHz (40 milliwatt per MHz). With the processor clock running at 3.5 MHz and each instruction taking 12, 24 or 48 clock cycles, an assumption of one read from memory per 12 clock cycles gives a basic memory frequency of 3.5/12 = 292 KHz or .292 x 6 = 2.3 ma. That figure has been rounded up to 4 ma to allow for temperature and provide a conservative number.

Data Memory - Harris 6516. Power requirements (see par. 6.0) are (i) operating 10 ma/MHz, (ii) idle 0.05 ma, and (iii) data retention 0.025 ma. Considering that the fastest data will be 50 points per second with three bytes per point, we have an operating frequency of 150 Hz. The memory is essentially always in the idle mode. A 1 ma allocation provides a conservative figure.

Summary

Our present approach to the power supply design is:

Battery System - Thionyl Chloride
- Energy ~ 65 x 10^3 joules
- Volume ~ 2 in^3

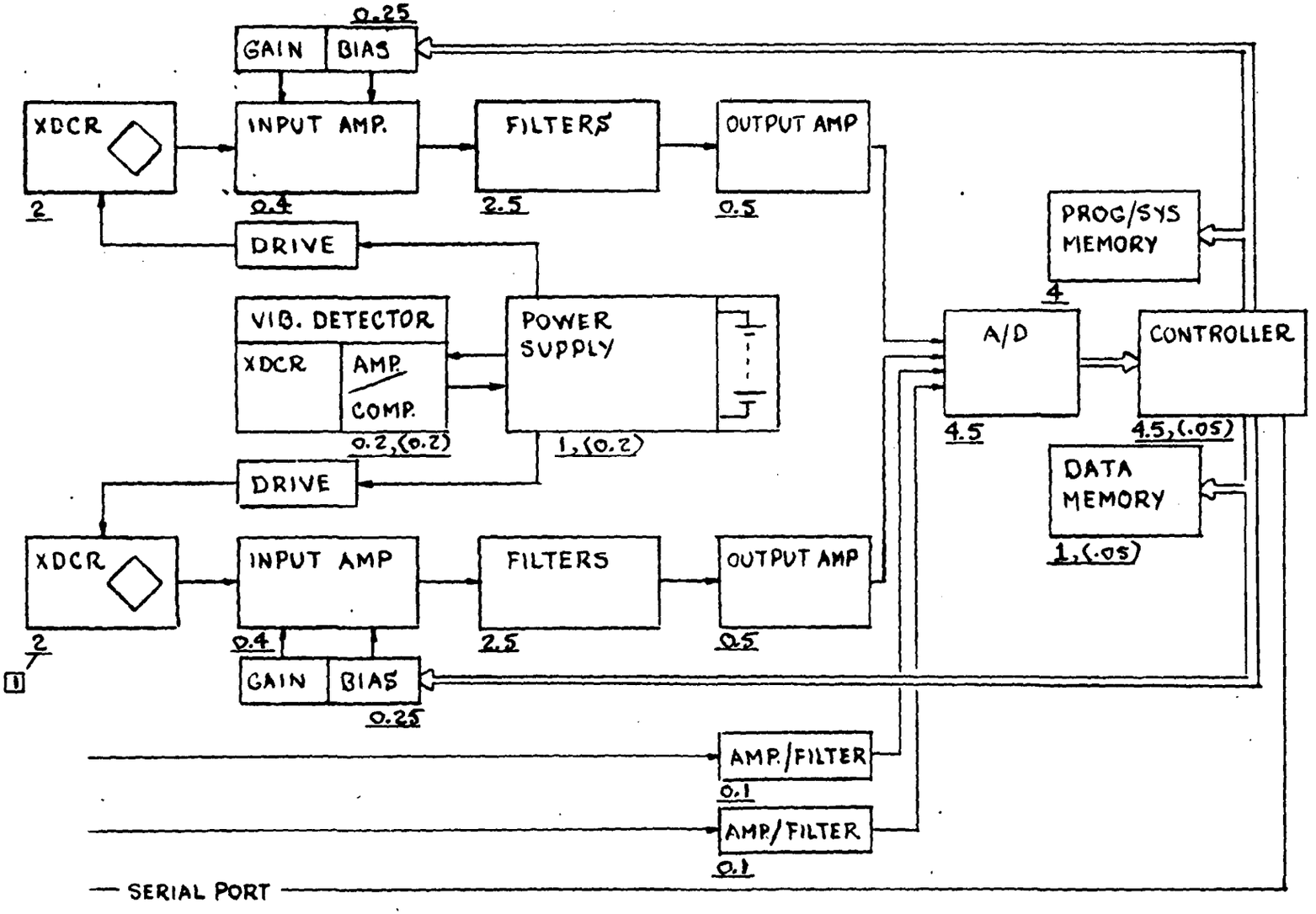
* Voltage ~ 5.6 to 7 volts
* (Capacity ~ 3 Ah)
Regulation - Series regulator in brassboard.
DC-DC converter in final unit.

We expect to design for AA cells to allow for wider selection in the end use. (For instance - a different chemistry to meet a special temperature range requirement.) Note AA lithium cells contain more than 0.5 grams of lithium and are not to be transported on commercial passenger aircraft.

The final unit will contain a miniature, high efficiency wide range input DC-DC converter to provide for use of various cell voltages and to eliminate power loss associated with series regulators.

* 1. Capacity (amp. hrs) of a given battery is dependent on the load current and the temperature of operation.

° 2. Total energy content in terms of Joules (one Joule equals 1 watt sec thus Op Volt x Amp Hrs x 3600 is the energy available from the battery or the energy used in the system) is used for determining battery capacity and system energy requirement. This approach simplifies the comparison of batteries and systems, especially if voltage converters are used.



PRELIMINARY
SYSTEM BLOCK DIAGRAM

FIG. 8.1

PRELIMINARY POWER BUDGET

[1] CURRENT VALUES IN MILLIAMPS, X = 100 HOUR VALUE, (Y) = 650 HOUR STANDBY VALUE

ESPRIT TECHNOLOGY ASSOCIATES

EXHIBIT 1

"Long Life Primary and Secondary Batteries"

LONG LIFE PRIMARY AND SECONDARY BATTERIES

Thomas Irwin
Application Engineer
RAYOVAC Corporation
101 East Washington Avenue
Madison, WI 53703

INTRODUCTION

Since the development of the electrochemical storage battery almost a century ago, a growing number of applications have employed batteries both as their only power source and as a back up supply during commercial power outages. In the last 100 years, a variety of battery chemistries have evolved both in primary and secondary batteries.

Today we are entering a microcomputer age where the demand for standby power to preserve volatile memories and to insure uninterrupted clock operation is increasing rapidly. Applications for standby power are in computers or process control equipment using real time clocks, computer printers where the customer initializes his printing format in volatile memories, portable data terminals used in inventory control, telecommunications, portable test equipment, and a growing list of other applications.

Miniature batteries are becoming an important tool to the microcomputer system designer. When complimented with power line sensing and write inhibit semiconductor devices, it enables the designer to use standard NMOS and CMOS RAMs without risking program or data loss. The designer can then continue using high speed low cost memories without sacrificing write speeds or having to resort to EPROMs or high priced low speed multi-voltage EEPROMs. Nor, is the number of write operations limited to some number X due to wear-out phenomena.

The purpose of the battery is to protect the microcomputer, its volatile memory, its clock circuitry, or any combination of these from AC line disturbances. To design a battery backup system, an engineer needs an understanding of power line disturbances. The types of abnormal power line conditions to be reckoned with are 1) Transients: a short term voltage or current disturbance having a duration between 1 nanosecond and 5 milliseconds. 2) Voltage Sags: a drop in voltage lasting more than 5 milliseconds but less than 5 seconds. The voltage value must be below the lower specification limit for nominal voltage. 3) Power Interruption: a complete loss of voltage for any period greater than 5 milliseconds, but less than 500 milliseconds. 4) Power Outage: a complete loss of voltage for any period exceeding 500 milliseconds. 5) Brownout: a deliberate reduction in nominal voltage supplied by the utility company. The value may fall at or below the lower limit specified for nominal voltage.

To quantify the problem, IBM did a study[1] of AC power sources for typical data processing equipment. The study involved 49 locations and 125,000 hours of monitoring. The study was made from July 1969 to July 1972. The information is broken down into duration of disturbance and percent of voltage lost.

During the 125,000 hours of monitoring 1,790 voltage sages, power interruptions, and power outages occurred; that is, one disturbance every 69 hours of operation.

Assuming the power supply can operate down to 80% of nominal line voltage, Figure 1 shows line disturbances that will cause memory problems. In 125,000 hours of operation there would be 1,040 disturbances, or one problem every 120 hours of operation. With the addition of a battery backup system, errors due to line disturbance can be controlled.

Additional considerations to be aware of are the electronic cash registers which may be shut off at night or on weekends and without battery backup could encounter loss of sales totals and/or inventory sold. Computerized office equipment involved in office moves and rearrangements can be subjected to power outages of several minutes, hours, or days. Without battery backup initialized data, accumulated data, and clock functions can be lost.

DURATION IN CYCLES	PERCENT OF LINE VOLTAGE SAG				
	20-60	60-70	70-80	80-90	TOTAL
.5 to 1	0	3	16	673	692
1 2	1	7	11	35	54
2 3	1	3	13	33	50
3 4	0	3	8	49	60
4 5	1	9	26	46	82
5 6	5	13	14	39	71
6 7	1	12	6	23	42
7 8	1	2	6	7	16
8 9	3	2	3	9	17
9 10	0	3	5	4	12
10 15	1	6	9	17	33
15 30	1	4	13	18	36
30 120	1	4	8	43	56
120 900	0	0	0	97	97
over 900	0	0	1	465	466
TOTALS	16	71	139	1588	1784

FIGURE 1 VOLTAGE SAGS FOR 125,000 HOURS

One additional problem is worth mentioning. Some computer products are manufactured and shipped with pre-programmed information. Batteries must be used for memory retention in the interim between shipment and installation by the end user.

The purpose of this paper is two-fold: 1) to review the history of primary and secondary batteries used for memory backup applications; and 2) to present the most recent developments in lithium batteries as they relate to the microcomputer/microelectronics environment.

Before I get into the different battery systems, I'd like to establish some general characteristics of an "Ideal Power Cell" and use it as the yardstick to which all batteries are compared and measured. The "Ideal Power Cell" would have:

1. Maximum Energy Density - offer a maximum amount of energy stored in a minimum amount of space.
2. Unlimited Shelf Life - no self-discharge irregardless of storage period.
3. Rechargeable - fully rechargeable at any charging rate.
4. Light Weight - combine maximum energy density with a minimum amount of weight in the materials used.
5. Safe - the ideal cell would be completely safe - no leakage or gassing. The contents would be harmless to people and the environment.
6. Good Performance - deliver the required current and voltage under a wide range of temperature and load conditions.
7. Cost - the materials used to make the cell would be in plentiful supply, multisourced, and manufacturing costs would be minimal.

SECONDARY BATTERIES

Nickel-Cadmium Batteries

Nickel-cadmium rechargeable batteries are secondary batteries. They were first developed in the 1940's. Figure 2 is an overview of several battery systems and their respective energy densities. Although the nickel-cadmium battery has a low energy density, the fact that it can be recharged compensates for this characteristic.

Advantages of nickel-cadmium batteries are: they offer excellent rate capabilities, have a stable discharge voltage, perform very well at low temperatures (-20°C and below), and have an operational life of 3 to 5 years, or 500 to 1000 charges, whichever comes first.

Disadvantages are: it has a low energy density, an individual cell voltage of 1.2 volts requiring a stack of several cells to form a usable battery for memory backup/clock applications, a high self-discharge rate of 1% per day at room temperature and several percent per day at temperatures above 40°C, and if subjected to many shallow discharge/charge cycles can develop a "memory effect" where it can fail to deliver its full capacity when called upon to do so.

Figure 3 compares the nickel-cadmium to the ideal power cell.

Most applications employ batteries consisting of a 3 or more cell stack. Typical applications are for memory backup/clocks, calculators (LED), test equipment, toys, etc.

Sealed Lead Acid

Sealed lead acid rechargeable batteries are members of the secondary battery family. Conventional lead acid batteries with the liquid electrolyte have been available for over seventy years. Sealed lead acid batteries have been available for about 7 years. Figure 2 compares its energy density to

other battery systems. Although sealed lead acid batteries have a low energy density, the fact that they can be recharged compensates for this characteristic.

PRACTICAL ENERGY DENSITY FOR CELL SYSTEMS

ALKALINE SYSTEMS	MID-LIFE VOLTAGE V	ENERGY DENSITY WH/L	LITHIUM SYSTEMS	MID-LIFE VOLTAGE V	ENERGY DENSITY WH/L
AIR/Zn	1.3	970	$SOCl_2/Li$	3.5	760
AgO/Zn	1.55	650	Ag_2CrO_4/Li	3.0	670
HgO/Zn	1.35	550	CF_x/Li	2.8	570
Ag_2O/Zn	1.55	460	MnO_2/Li	2.9	520
MnO_2/Zn	1.3	230	SO_2/Li	2.8	450
CARBON/Zn	1.3	140	SOLID STATE	2.8-2.0	500-530
NICAD	1.2	75			
SEALED LEAD ACID	2.0	70			

CELL SIZE: 11.6 x 4.2 mm

DRAIN: 5 MICROAMPERES

FIGURE 2

Advantages of sealed lead acid batteries are: they have a nominal cell voltage of 2 volts, can deliver high currents, have a flat discharge, can operate over a temperature range of -40°C to +60°C, operational life of 3 to 5 years or 100 to 250 charges, and an ability to tolerate cell reversal without damage.

Disadvantages are: its low energy density, a self-discharge rate of 6% to 8% per month at room temperature, limited number of recharges, the smallest size available is comparable to a "D" size, and it is physically heavy.

Figure 3 compares the Sealed Lead Acid battery to the ideal power cell.

Sealed Lead Acid batteries are available in sizes from 2.5 AH to over 25 AH and in 2 volt increments from 2 volts to 48 volts. Typical uses are standby power for powering large blocks of memory at a 2 volt data retention level, uninterruptable power supplies for small to medium size computers, alarms, emergency lighting, and as cyclic power for tools, instruments, engine starting, televisions, and video tape recorders.

Mercury Batteries

Mercury primary batteries were first mass produced during World War II. Figure 2 shows mercury's energy density relative to other battery systems. As you can see, mercury is very high in the table and at the time of development was the highest energy density battery available. This characteristic also facilitated development of miniature button cell batteries having capacities in the hundreds of milliampere-hours.

Advantages of mercury batteries are their high energy density, flat discharge characteristic, good rate capability at currents from microamperes to hundreds of milliamperes, and an operating temperature range of -20°C to 60°C.

Disadvantages of the battery are: a cell voltage of 1.35 volts, a shelf life at room temperature of 1-2 years, problems of mercury migration during discharge which can internally short out the cell, the environmental concern of mercury disposal, and relatively high cost.

In some of the first computerized cash registers, 1 AH mercury batteries were used for memory backup. However, it was found that the batteries did not stand up well under the daily temperature cycling. Too often the cells would leak or go dead after one-half of their capacity had been expended. Coupled with the 1-2 year shelf life, the mercury battery bowed out of the memory backup market.

Figure 3 compares the mercury battery to the ideal power cell.

Present day applications for the mercury battery are in hearing aids, cameras, instruments, and smoke detectors, which benefit from its high energy density characteristics.

Alkaline Batteries

The alkaline manganese, or simply alkaline battery as it is commonly called, was developed about 25 years ago. While most of the alkaline batteries available today are primary

COMPARISON TO IDEAL POWER CELL

CHARACTERISTICS

CHARACTERISTIC	IDEAL POWER CELL	SEALED LEAD ACID	NICAD	MERCURY	ALKALINE	SILVER	LITHIUM
MAX ENERGY DENSITY	High	Low	Low	High	Med	High	High
SHELF LIFE	Excellent	Low/Med	Low	Low	Good	Good	High
RECHARGEABLE	Yes	Yes	Yes	No	No	No	No
LIGHT WEIGHT	Yes	No	No	No	No	Yes	Yes
SAFE	Yes	Good	Good	Low	Good	Good	Good*
GOOD PERFORMANCE	Yes	Yes	Yes	Yes	Yes	Yes	Yes
COST	Low	Med	Med	High	Med	Med	High

*Depends upon particular system

FIGURE 3

batteries, there is a rechargeable version. Figure 2 is an overview of several energy density chemistries. As you can see, Alkaline Manganese is an improvement over the zinc carbon and nickel-cadmium, but has only 40% of the energy density of mercury.

Alkaline batteries are available in sizes from 40 MAH button cells to multiampere hours "D" cells and battery voltages from 1½ volts to 9 volts.

Advantages of the alkaline battery are its high rate efficiency, improved shelf life of 3-5 years, good to excellent low temperature performance, cell voltage of 1.55 to 1.6 volts, and low cost.

Disadvantages are its low to moderate energy density. Alkaline button cell batteries have insufficient energy to meet memory backup power requirements for several years of operation. Elevated temperatures accelerate the self-discharge rate, limiting its overall service life.

Figure 3 compares the alkaline manganese battery to the ideal power cell.

Present day applications for this battery are LCD calculators, cameras (exposure control system and strobes), and toys.

Silver Oxide

Silver oxide batteries were commercially developed about 10-15 years ago. There are two similar chemistries used in commerical silver oxide button cell batteries, monovalent and divalent silver oxide.

Figure 2 lists the energy density of both silver oxide chemistries. Monovalent silver oxide has the formula Ag_2O and falls between alkaline and mercury. Divalent has the formula AgO and offers the highest energy density outside of the Zinc-Air system. (The mechanics of activating/deactivating a Zinc-Air battery prevents its use in battery backup applications.) The high energy densities lend themselves to miniature button cells. Almost all commercially available silver oxide batteries are button cells. The development of larger cylindrical size silver oxide batteries is possible but is restricted by the price of silver.

Characteristics of the monovalent and divalent cells are their high energy densities - about 2 - 2½ times that of alkaline, an operating voltage of 1.55 volts, light weight, good low and high rate current capacities, a shelf life at room temperature of 3 to 5 years in high rate cells, and 4 to 6 years in low rate cells, good low temperature operation, and low leakage rates.

Disadvantages of both types are the increased self-discharge rates which occur when cells are subjected to high temperatures for extended periods of time. The fluctuating market price for silver in the past couple of years has increased silver oxide button cell prices significantly. Currently, silver is below $10/Troy Oz. and it is again a viable cost product.

Differences between mono and divalent cells occur in two areas. First, divalent has a higher energy density, about 30% more, than monovalent. In the same size cell, divalent can offer significantly more energy. Second, divalent chemistry produces a higher cell voltage of 1.8 volts compared to 1.55 volts for monovalent. In commercial divalent silver oxide cells, special techniques are used to reduce the voltage to 1.55 volts without sacrificing the higher energy density.

In terms of low temperature operation, a divalent silver oxide watch cell measuring 11.56 mm diameter by 5.36 mm high and rated at 1.5V, 220 MAH, has delivered 113 microamperes at -70°F at a closed circuit voltage of 1.44 volts.

Silver oxide button cell batteries range in size from 2.10 mm high by 6.80 mm diameter to 5.36 mm high by 11.56 mm diameter and capacities of 17 MAH to 220 MAH.

Figure 3 compares both silver oxide battery systems to the ideal power cell.

Lithium Batteries

The most exciting new battery system entering the marketplace today is lithium. Actually, it should be referred to as lithium systems since there are in excess of 10 different systems that use lithium.

Figure 4 is a partial listing of companies and the lithium technologies they are or have investigated.

The primary incentive for the development of lithium batteries is their potential for very high energy densities which in small batteries can realistically be expected to be 450 to 760 Watt-Hours/Liter delivered. Another incentive is the higher cell voltage of 2.6 to 3.6 volts. Lithium batteries also exhibit shelf lives of 5 to 20 years depending upon the particular lithium system. They can also operate at low temperatures to which conventional batteries would be inoperative.

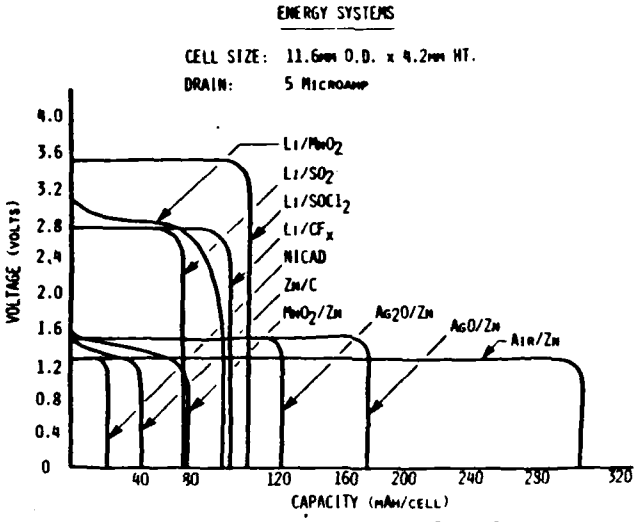
PARTIAL LISTING OF COMPANIES INVOLVED IN LITHIUM CELL DEVELOPMENT/MANUFACTURE

COMPANY	LITHIUM SYSTEMS
RAYOVAC CORP.	MnO_2, CuS, Cu_2S, $SOCl_2$, Ag_2CrO_4, FeS, CF_x, SOLID STATE
TOSHIBA RAYOVAC	MnO_2
SANYO	MnO_2
MATSUSHITA	CF_x, CuO, MnO_2
UNION CARBIDE	MnO_2, FeS_2, $SOCl_2$
MALLORY	MnO_2, SO_2
HITACHI-MAXELL	FeS
GENERAL ELECTRIC	MnO_2
HONEYWELL	$SOCl_2$, V_2O_5
GTE	$SOCl_2$
EAGLE-PITCHER	CF_x
VARTA	MnO_2, Bi_2O_3
BEREC	MnO_2
ALTUS	$SOCl_2$
ULTRA ENERGY	SO_2
CATALYST RESEARCH	SOLID STATE
WILSON GREATBACH	Br_2 COMPLEX, SOLID STATE, Ag COMPLEX
SAFT	CuO, $Bi_2Pb_2O_5$, MnO_2, $SOCl_2$, Ag_2CrO_4
PCI	SO_2
TADIRAN	$SOCl_2$

FIGURE 4

Lithium is the lightest metallic element known to man and is very reactive. It is a far more reactive material than zinc and even surpasses potassium and sodium. The extreme reactivity of lithium metal, which theoretically makes it such an attractive anode material, also makes it very difficult to work with. In the presence of water vapor or water it can ignite spontaneously. Hence, assembly must take place in dry rooms and the seals on the cells must be of a very high quality.

In terms of lithium chemistries which are at a production or prototype level, the major ones are solid state, sulfur dioxide (SO_2), carbon monofluoride (CF_x), manganese dioxide (MnO_2), and thionyl chloride ($SOCl_2$). Figure 2 compares the energy densities for these lithium systems. Figure 5 is a graph of their discharge characteristics.



CHARACTERISTIC DISCHARGE VOLTAGE OF ENERGY SYSTEMS
FIGURE 5

Solid State

Lithium solid state batteries are as their name implies, composed of a solid anode, solid electrolyte, and solid cathode. Combined with hermetic sealing, they may achieve shelf lives of 10 to 20 years or longer.

Solid state batteries were initially used in cardiac pacemakers where high reliability, low drains, and long operational life were extremely important. As power requirements for CMOS memories were reduced to the low microampere range, a new application for solid state batteries developed.

Solid state batteries offer a high energy density, approximately twice that of the alkaline battery, a long shelf life of 10 to 20 years, a wide temperature operating range of -55°C to +125°C, no leakage, a cell voltage of 2.8 volts, and a flat discharge characteristic.

In button cell sizes the principal limitation is a typical current drain of 20-25 microamperes, 50 microamperes maximum. They also have a moderate to high cost.

As the standby power requirements for CMOS RAMs continue to fall into the low and sub-microampere range, more applications will develop for solid state lithium batteries.

Lithium/Manganese Dioxide

Lithium manganese dioxide cells consist of a lithium anode, separator, manganese dioxide cathode, and an organic electrolyte. They have a nominal cell voltage of 3 volts and deliver approximately 2.9 volts under load. Its energy density is better than twice that of an alkaline battery. They usually employ crimp seals but can use a hermetic seal if the application so requires. The shelf life is estimated at 5 to 10 years. Lithium manganese dioxide cells are available in button cell and cylindrical sizes ranging in capacity from 30 MAH to 1000 MAH.

Advantages are its high energy density, 3 volt cell voltage, good rate capability, low self-discharge rate, has a temperature operating range of -20°C to +50°C, and a sloping discharge which lends itself to end of battery life sensors.

Lithium/Carbon Monofluoride

Lithium carbon monofluoride cells consist of a lithium anode, separator, carbon monofluoride cathode, and an organic electrolyte. The nominal cell voltage is 3 volts and 2.8 volts under load. It has an energy density slightly higher than that of lithium manganese dioxide. Lithium carbon monofluoride cells are available in sizes from button cells to "C" size cylindrical cells. Crimp seals are used in both the button and cylindrical cells. Shelf life is estimated at 5 to 10 years. Capacities range from 40 MAH to 5 AH. The button cells can deliver continuous currents up to 250 uA with pulsing up to 10 milliamperes. The larger cylindrical cells can deliver currents from microamperes to hundreds of milliamperes.

Advantages are its high energy density, cell voltage of 3 volts, good rate capability, low self-discharge rate, and an operating temperature range of -20° to +60°C.

Lithium Thionyl Chloride

Lithium thionyl chloride cells are a high voltage, high energy density lithium system. Figure 2 shows lithium thionyl chloride at the top of the list.

If lithium systems were classified as low, medium, or high rate, thionyl chloride would fall in the high rate category. It has a nominal voltage of 3.6 volts and is commercially available in sizes from .85 AH to 10.8 AH.

They are available both in low profile prismatic and conventional cylindrical shapes. The basic construction consists of a lithium anode, a separator, a carbon cathode, and a thionyl chloride electrolyte/depolarizer.

Advantages are: a very high energy density, a high cell voltage, excellent rate capability, with hermetic seals - a shelf life of up to 10 years, a very low self-discharge rate, and a temperature operating range of -55°C to +70°C.

Disadvantages of the system are its susceptibility to a voltage delay problem. If initially unused for some period of time, a passive layer develops on the anode. If the cell is subjected to a light current drain, the voltage drop will be very small to non-existant. It is only on a heavy drain that the cell voltage drop is pronounced. The delay time during heavy drains can be several seconds in length. Under both light and heavy drains the layer is dissipated.

Lithium Sulfur Dioxide

Lithium sulfur dioxide cells have been in production for several years, primarily for military markets. They are available in sizes of .43 AH up to 30 AH. The nominal cell voltage is 3 volts and 2.8 volts under load. The basic cell is spiral wound consisting of a lithium anode, a separator, a carbon cathode, and a sulfur dioxide rich electrolyte. The cells are usually hermetically sealed. The sulfur dioxide cells are operated at a positive internal pressure which can reach 100-200 PSI (pounds per square inch) at elevated temperatures. The operating temperature range is -65°F to +165°F. At temperatures between 230°F to 250°F and pressures of 450 to 500 PSI, a safety vent is activated rendering the cell inoperative. The sulfur dioxide system can sustain currents from microamperes to amperes in its "D" cell size. Shelf life is estimated to be about 10 years.

Lithium sulfur dioxide cells are also susceptible to the same type voltage delay seen with lithium thionyl chloride. Here too, good progress is being made to eliminate the problem.

Lithium as a composite battery system has the advantage of a high energy density, a cell voltage of 2.6 to 3.6 volts, a wide temperature operating range, greatly improved shelf life, low leakage rates, light weight, good rate capabilities and long term reliability.

Lithium is not a high current drain battery system. On an equivalent size basis to an alkaline battery, it cannot supply the same high currents to a load. Lithium is high priced primarily because it is not yet in mass production. There is a lack of universal availability and there are government restrictions on shipment of lithium cells having over one-half gram of lithium.

Today's applications for lithium button cells are strongest in the watch and calculator markets. However, a growing number of applications for button cells as small as the 40 MAH to as large as multiampere hour thionyl chloride cells, are appearing in industrial controls, test equipment, telephones, memory backup, and computer clock/timing functions.

Figure 3 compares the lithium systems with the ideal power cell.

CONCLUSION

The microelectronic system designer now has a broad portfolio of battery systems with which to meet his backup power requirements. Secondary batteries like the Nickel-Cadmium and Sealed Lead Acid should be considered where the application could require frequent replacement of primary batteries, where high current drains are required, where primary batteries may not be replaced, and if rechargeability makes the device more desirable to the user. Primary batteries like the silver oxide and lithium systems can offer many years of reliable protection for volatile memories and clocks, can reduce maintenance, and in some cases may be good for the life of the equipment, can eliminate the need of charging circuitry, can operate over broad temperature ranges, and can be directly mounted on the printed circuit board.

While this paper presents some design guidelines for selecting and applying primary and secondary batteries, it is by no means complete. It is intended as a guide to you, the systems designer, for determining your battery requirements.

In the process of making your battery selection, it is very important to solicit more detailed information and assistance from the battery manufacturers. Generally, manufacturers have a group of trained application engineers to provide technical assistance and specification guidelines. By working with the battery manufacturer, you can minimize risk in product design, optimize product performance and continue the successful alliance of batteries with microelectronics.

REFERENCES

1. Memory Support for Data Processing Equipment; Mr. David Kuykendall, 1979 Wescon Professional Program, Session #12.

2. Power Sources for Volatile Memories; Joseph Carone, 1980 Wescon Professional Program, Session #24.

EXHIBIT 2

Commercially Available Lithium Cells

Comparison

Lithium Battery Systems

The basic types of lithium cells are:

(i) Lithium - inorganic electrolyte
(ii) Lithium - organic electrolyte
(iii) Lithium - solid electrolyte

Type (i) - Lithium - Thionyl Chloride (Li-$SOCl_2$)
Highest energy density 64 10 Joules/in
wide temperature operation
cell voltage 3.5 volts
current - 1 to 1000 ma (design dependent)

possible unpredictable self discharge.
$SOCl_2$ is highly reactive.

Examples:

Eagle Picher	7PMP
Electrochem	BCX72
Electrochem	CSC93 (Sulfuryl Chloride)
Altus	AL2AA
SAFT	LS6

Type (ii) - (a) Lithium - Manganese Dioxide (Li-MnO_2)
(b) Lithium - Carbon Fluoride (Li-CFx)
(c) Lithium - Sulfur Dioxide (Li-SO_2)
Medium energy density 35 10 Joules/in
wide (advertised) temperature operation
Cell voltage 2.8 to 3.0 volts
Current - to 10 ma

predictable self discharge.

Examples:
(a) Duracell DL2N
(b) Eagle Picher - LDFS type
(c) Ray-O-Vac BR2/3A

The Lithium Sulfur Dioxide batteries are not being considered for use as they can vent into the electronic cavity albeit the venting occurs at high temperature (115 C).

Other system chemistries appearing on the market for very high temperature operation are lithium copper oxide (Li-CuO) and lithium copper oxyphosphate (Li-$Cu_4(PO_4)_2$) cells with voltages ranging from 1.5 to 2.4 volts. These cells can be operated to +175 C but normally are limited to operation above 0 C. Examples are the Saft LCP series and the Electrochem CuO and CH1 series.

Type (iii) - Lithium - Iodine
Medium to high energy density 53 10 Joules/in
cell voltage 2.4 to 2.8 volts
Current - to 2 ma

The low load capability of this battery precludes its use in the present system.

EXHIBIT 3

Battery System Correspondence

We are under government contract to develop a small, self contained, processor based, solid state data recorder for application in military aircraft. The recorder must be battery powered and generally meet the requirements of MIL-E-5400T Class 2 (-54°C to + 71°C, intermittent to + 95°C) or class 3 (-54° to 95°C, intermittent to +125C).

The recorder will be installed on aircraft for periods up to one month (750 hours) and are designed to stay in a semi quiescent state (low current $\leq$ .2ma) except for certain sub periods of that 750 hours (sub periods that could add up to 100 hours) in which the batteries must provide 10 to 15 milliamperes to the system. Our current estimation of the power requirements are:

Battery voltage: 5.4 to 6.1 volts

System Load:

(i) Quiescent State (650 hours)	$\leq$ 0.2 milliamperes.
(ii) Operational State (N 2 to 6 hour periods totaling 100 hours)	15 milliamperes
(iii) Storage Pulse (1 or 2 minute periods at the end of each operational period)	120 milliamperes

The major focus of this development project is to minimize the size of the recorder with a goal of 8 to 10 cubic inches for total volume. Allocating about 25% of that volume to the power source we get - say - a 2 in^3 goal for the battery pack. Ignoring temperature variations, straight forward calculations give us an 1830 mah capacity figure. (Based on 650 hours at 0.2 ma, 100 hours at 15 ma, and .033 hours at 120 ma for 50 occurrences). Using a nominal 6 volt figure this gives (6)(1.83) (3600) = 39,528 Joules (watt. sec.) of energy expended and combining this value with the volume goal we get an energy-volume storage capacity of at least 20,000 Joules/in^3 (1200 Joules/cm^3) for the battery.

ESPRIT TECHNOLOGY INC.

We believe energy density values of this magnitude dictate the use of lithuim chemistry batteries and are seeking your aid in defining a suitable battery system. At present we have no statistical estimations of the temperature/time spectrum and can only state that the batteries must not present a hazard when subjected to the temperatures noted. The system could conceivably be configured to operate over restricted temperature ranges, e.g. -20°C to + 71°C, depending upon its final usage.

Another thing to note is that the 120 ma pulse is required to drive an EEPROM included to provide absolute non volatility in the memory. This might possibly be taken care of by using a second, low capacity, 2.5 volts battery system to back up a static RAM.

We would like to thank you in advance for any help you can give us in defining a battery system for this application.

Sincerely,

Philip Flanner
Engineering Manager

SAFT AMERICA INC.
Advanced Battery Systems Division

December 27, 1985

Philip Flanner
Esprit Technology, Inc.
144-A Mayhew Way
Walnut Creek, CA 94596

Dear Mr. Flanner,

Thank you for your interest in SAFT batteries. After reviewing your specifications, I have the following recommendations.

1. System load (iii) 1 to 2 minute pulse at 120 ma for loading an EEPROM cannot be handled by a lithium battery based on wide temperature range. Therefore, we suggest use of a RAM instead of EEPROM in both of the following.

2. For use using Class 2 temperature of MIL-E-5400T we recommend the use of four lithium thionyl/chloride "AA" size cells SAFT Type LS6. They would be connected two in series and two in parallel to yield 7 volts and 3.4 AH. The use of a voltage regulator would be needed (with a low voltage drop) to maintain a constant voltage since over the temperature range the voltage would fluctuate under load from 7.1 volts to 5.5 volts. Cells in stock.

3. For Class 3 temperature of MIL-E-5400T our lithium copper oxide "AA" size would be needed, Type LCH6GTM. Five cells would be needed to yield 7 volts and 3.4 AH. Again a voltage regulator would be needed since the voltage range would be 5.0 volts to 9.0 volts. This cell has been designed but not developed. Therefore some commitment on your part or your customer's part would be needed.

If you have any questions, please call our sales engineer, Mr. Ted Williams (818-884-6151) or myself.

Sincerely,

Michael Line
Lithium Systems Product Manager

ML:Bjm.

cc: T. Williams

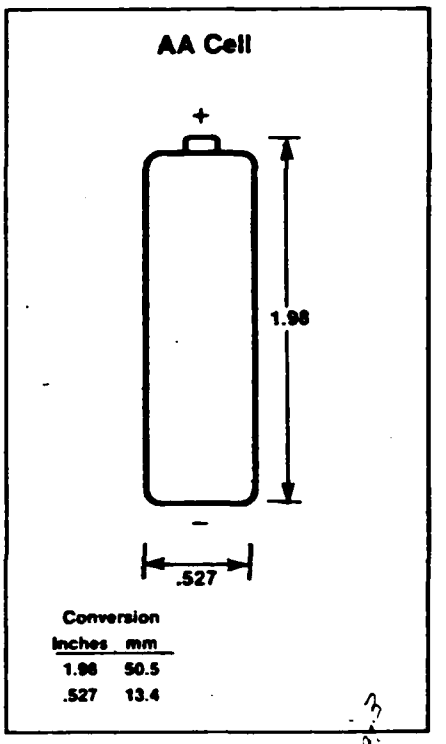
107 Beaver Court Cockeysville, Maryland 21030 Tel (301) 666-3200 TWX 710-862-2637

LITHIUM THIONYL CHLORIDE

LS 6

Nominal Voltage **3.5 V**

The LS 6 is a liquid cathode cell of bobbin type construction exhibiting one of the highest energy densities available. Cells are available as shown, with pin mounts suitable for PC board insertion or in battery assemblies.

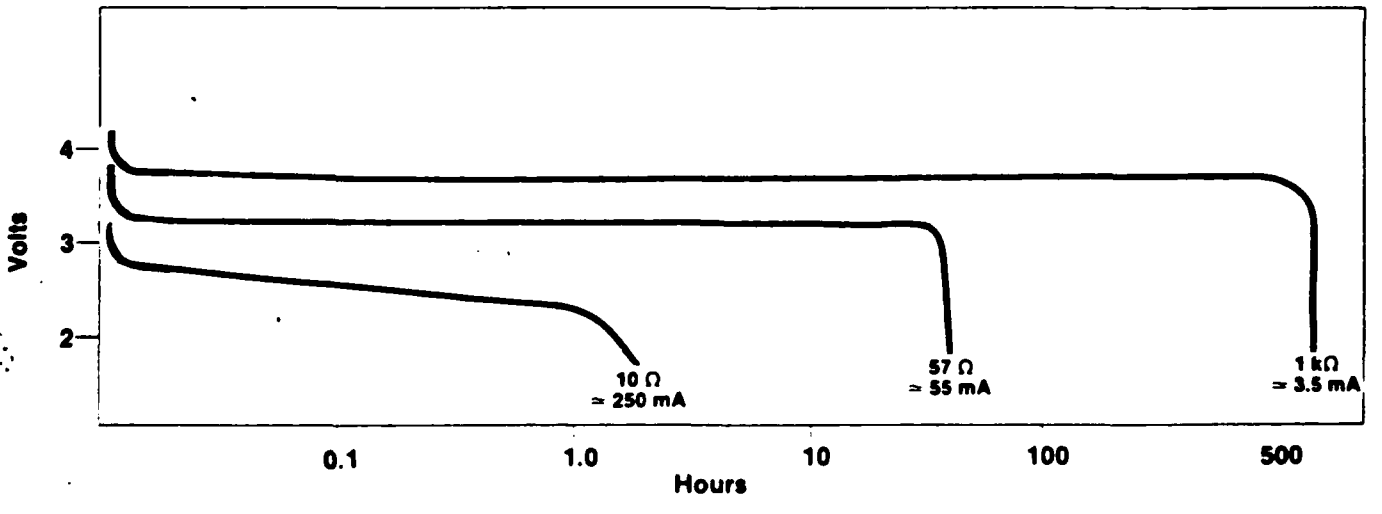


Specifications

OCV, volts	3.67
Nominal Voltage, volts	3.5
Nominal Capacity, Ah	1.7
Weight	
ounce	.54
grams	15.4
Case Material	*Stainless steel*
Sealing	Glass to Metal
Hermeticity	10×10^{-8} Std/CC per sec. Helium
Temperature Range*	-40 to + 160° F -40 to + 71° C

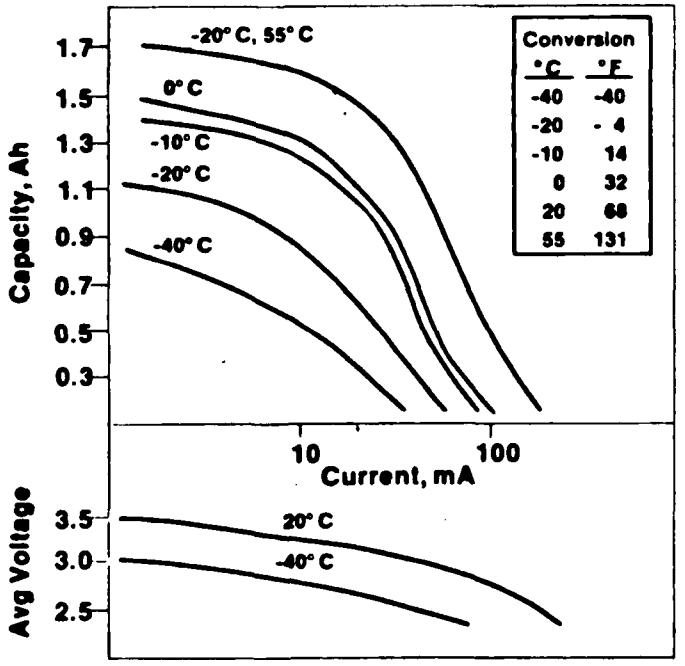
*Operation at temperatures up to 265° F (+130° C) is possible with certain precautions.

Typical Discharge Curves At 68° F (20° C)

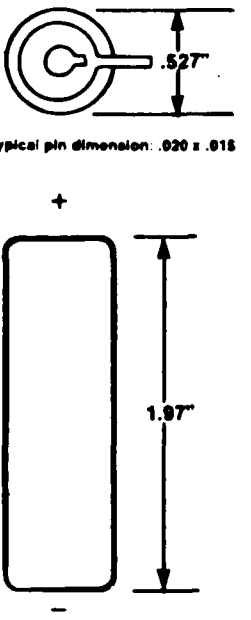


LS 6

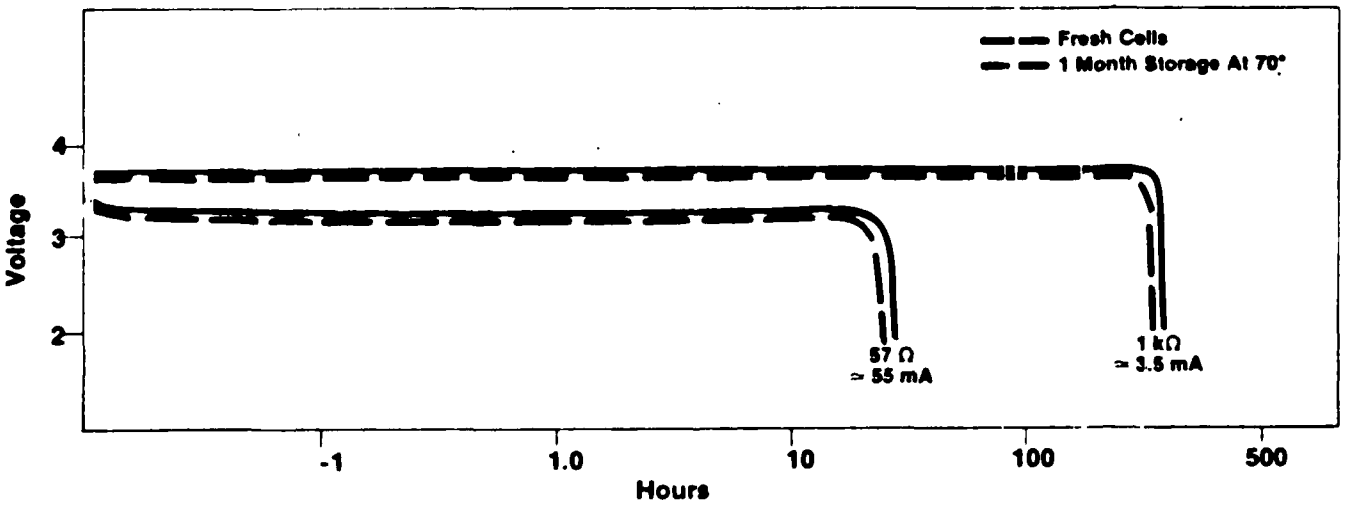
Typical Performance of LS 6 After One Year Storage At 20° C



LS 6 with pin mounts for direct mounting on printed circuit boards



Effect of High Temperature Storage on LS 6



CAUTION: *Do not recharge or dispose of in fire; do not short cells or attempt to solder directly to them; do not dismantle cells. For further handling information, please contact SAFT Engineering. Disregard of these precautions may lead to explosions and/or the release of toxic gases.*

SAFT Advanced Battery Systems Division
107 Beaver Court
Cockeysville, Maryland 21030
Telephone 301/666-3200
TWX. 710-862-2637

array. This requires 710 ns, leaving time for refresh and also clocking the address counter to other rows.

"We're expecting a large market in both TV sets and video recorders," says NEC Marketing Manager Allen Hu. "In digital TVs, the 41221 is going to upgrade performance with better color reproduction, still pictures, windows, zoom, noise reduction, and non-interlaced scan. In VCRs, it provides superior still pictures, jitter corrections, and other features."

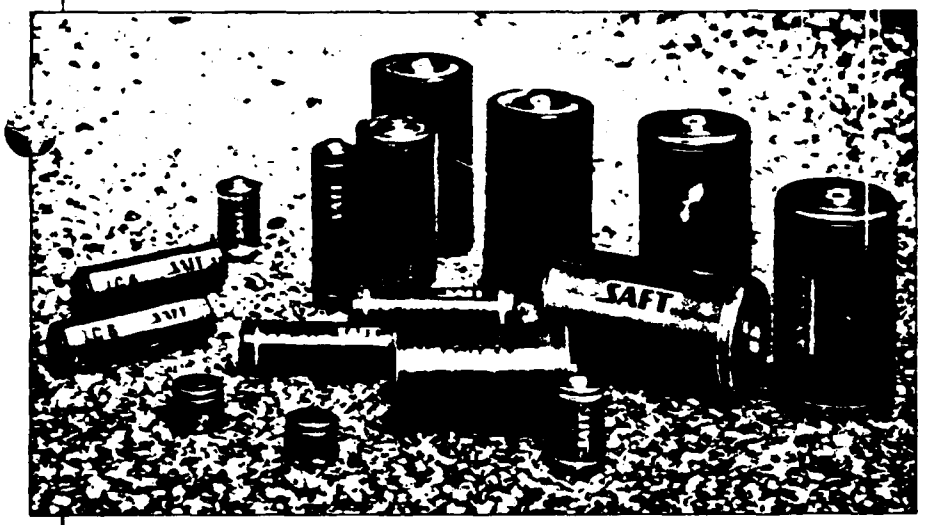
For large-volume orders, the 320 x 700 layout can be changed. In production quantities, the price is expected to drop to approximately that of standard 256-Kbit DRAMs. The μPD41221 comes in a 14-pin, 400-mil-wide plastic DIP for operation from 0° to 70°C. ($15 ea/100—stock.)

NEC Electronics Inc.
Mountain View, CA
Mike Conant 415-960-6141

IC Master Memory

CIRCLE 346

Lithium battery operates to 175° C, defying long-standing temperature limit



Based on a new lithium battery chemistry—lithium copper oxyphosphate [$Li/Cu_4O(PO_4)_2$] developed by Saft America Inc., LCP series batteries operate safely up to 175°C, the highest operating temperature specified for a lithium battery. A few lithium batteries of other chemistries are rated to 150°C max; most are rated well below that temperature.

The reason for the 150°C limit on lithium batteries is that this material melts at 180°C, and the liquid lithium and liquid electrolyte form a volatile, and dangerous, mixture. So manufacturers have set the maximum temperature to 150° to provide a safety margin.

LCP batteries, however, use an electrolyte that is chemically stable towards lithium. There's no reaction between the lithium and the electrolyte, even when the lithium is in liquid form above 180°C. The firm says LCP batteries have operated safely at 200°C—20° above the melting point of lithium. To provide a safety margin, however, Saft specifies a maximum operating temperature of 175°C.

High-temperature operation is not the only attribute of the new batteries. Because of lithium-electrolyte stability, LCP batteries exhibit an extremely long storage life—98% capacity retention after being stored for 10 years. Unlike other lithium batteries, they exhibit no voltage delay at turn-on after long storage.

LCP high-temperature lithium batteries provide a nominal 2.4 V. Two versions are available, the LCP-6HT AA battery and the LCP-14HT C battery. The LCP-6HT battery is rated at 1.9 Ah and measures 0.55 (dia) x 2.0 (L) in. The LCP-14HT battery has a 5.0-Ah rating and is 1.0 (dia) x 2.0 (L) in.

Lower-temperature versions, the LCP-6 and LCP-14, are also available. Both operate to 70°C and cost much less than their high-temperature counterparts. (LCP-6HT, $20 ea/1,000; LCP-14HT, $46 ea/1,000; LCP-6, $5 ea/1,000; LCP-14, $10 ea/1,000—stock.)

Saft America Inc.
Cockeysville, MD
Michael Brookman 301-666-3200

eem file 3900

CIRCLE 347

2-μm HCMOS arrays hit 10,000 gates, offer second sourcing

It doesn't happen often that engineers doing gate-array designs have a new family at their disposal that's supplied by two sources. But this is just about the case with the GB series of 2-μm, double-level metal HCMOS arrays whose seven sizes range from the equivalent of 1,120 to 9,776 two-input NAND gates.

Mostek Corp., Carrollton, TX, is already taking orders for the parts, while Gould-AMI, Santa Clara, CA, is likely to be doing so by the end of the month. The two companies have extended for five years their past agreement to offer uniform design and fabrication techniques for the GA series of gate arrays, a 3-μm family that offers densities up to 4,000 equivalent gates.

The new agreement guarantees

ELECTROCHEM INDUSTRIES
Div. of Wilson Greatbatch Ltd.
10,000 Wehrle Drive
Clarence, NY 14031
716-759-6901

TLX 91-386

06 January 1986

ESPIRIT Technology Inc.
144 A Mayhew Way
Walnut Creek, CA 94596
Attn: Mr. Philip Flanner
Engineering Manager

Dear Mr. Flanner:

Thank you for your interest in our lithium oxyhalide battery system.

After reviewing your application we've narrowed down the possibilties to 2 specific types of cells, the PWR .45 C and the HRT .45 C. Each cell will fit your needs, each in its own particular way.

HRT .45 C

Open Circuit Voltage (per cell)	3.9 Volts
In a 2 Cell Series Pack Configuration	7.8 Volts
Rated Average Load Voltage (per cell)	3.3 Volts
In a Pack Configuration	6.6 Volts
Rated Discharge Current	75 Milliamps
Maximum Continuous Discharge Current	500 Milliamps
Operating Temperature Range	-40°C to +72°C
Dimensions	1.015" $\pm$ .015" Length 1.009" $\pm$ .012" Diam.

PWR .45 C

Open Circuit Voltage (per cell)	3.95 Volts
In a 2 Cell Series Pack Configuration	7.90 Volts
Rated Average Load Voltage (per cell)	3.3 Volts
In a Pack Configuration	6.6 Volts
Rated Discharge Current	175 Milliamps
Maximum Continuous Discharge Current	500 Milliamps
Operating Temperature Range	-32°C to +93°C
Dimesnsions	Same as the HRT .45 C

As you can see we believe that either of these 2 types of cells will do the job for you, depending on the exact temperature requirements you select.

They are of our standard product line and delivery is in the 1 to 2 week range.

We look forward to your return call.

Best Regards,

Robert A. Altieri
Sales Coordinator

RAA:st
Enclosures

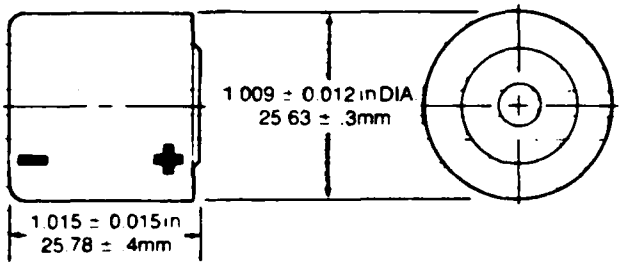
Electrochem Lithium Batteries Technical Data

PWR

Series PWR93

3B682

.45C Size



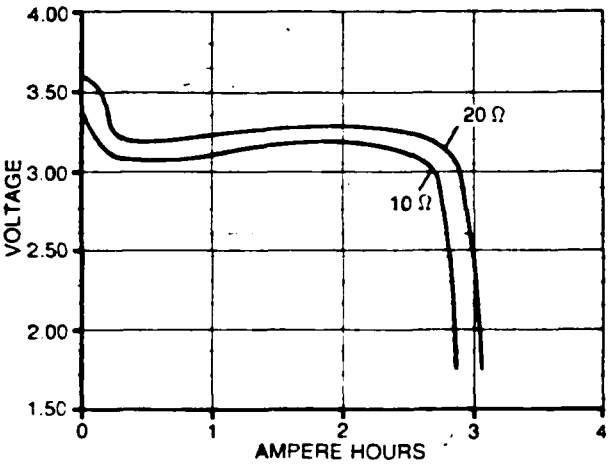
Applications:

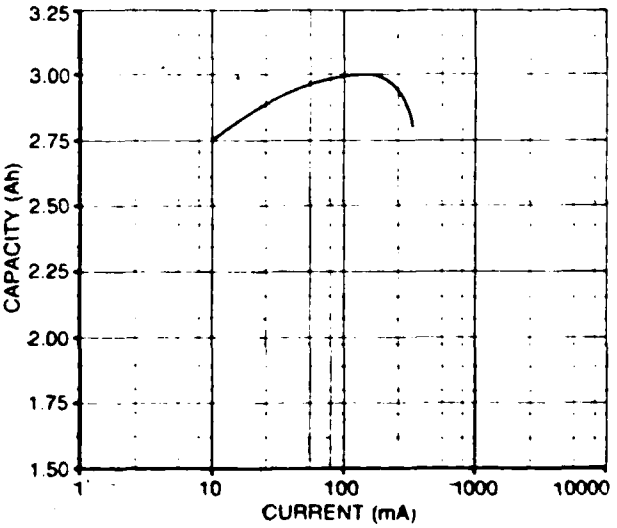
- **Communications Equipment**
- **Avionics Power Sources**
- **Remote Sensing Devices**
- **Guidance Control Systems**

Specifications:

Open Circuit Voltage (Nominal)	**3.95V**
At Room Temperature:	
Rated Average Load Voltage	**3.3V**
Rated Discharge Current	**175mA**
Rated Capacity	**3Ah**
Maximum Continuous Discharge Current	**500mA**
Operating Temperature Range	**-32 to 93°C (-26 to 199°F)**
Weight	**30g**
Safety Fuse	**4 Amp**
Energy Density	**330 $^{Wh}/_{kg}$, .74 $^{Wh}/_{cc}$**

WARNING Excessive heating of the battery may cause a runaway reaction causing the cell to open mildly (venting) or violently (explosion). Do not incinerate, short circuit, use or store outside specified temperature range, puncture, crush, disassemble, recharge or force over discharge (reversal).





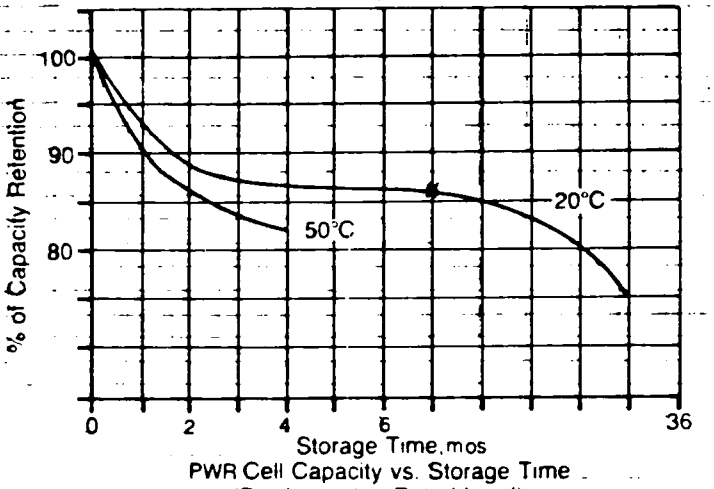
The performance curves above are based on tests on fresh cells. These charts are to be used as an application guide only.

Electrochem Lithium Batteries

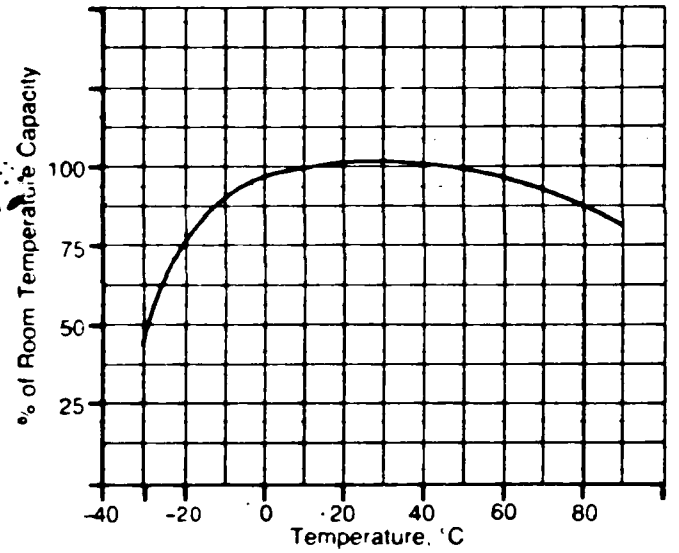
PWR Lithium Oxyhalide Primary Cells

The PWR line of high quality lithium oxyhalide primary cells is the high rate specialist of the Electrochem family. For qualified applications, the PWR can deliver up to 4 amps from the D size or 500 milliamps from the tiny .45 and ½C sizes. With an OCV of 3.95 volts and high energy density, the PWR is one of the highest performing primary cells available.

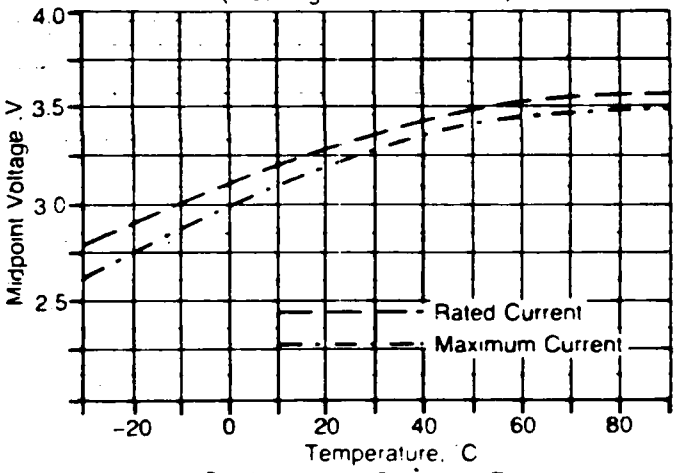
The wound construction, in a hermetic, glass-to-metal sealed 304L stainless steel case means the PWR supply power in the toughest environments, in temperatures ranging from –32°C (–26°F) up to 93°C (199°F) Available in custom packs.



PWR Cell Capacity vs. Storage Time
(Discharged at Rated Load)



PWR Cell Capacity vs Discharge Temperature
(100% Capacity Delivered at Room Temp.)



PWR Cell Voltage vs Discharge Temperature

Your best source for Quality Lithium Batteries

You can have just the right amount of power you need, when you need it, simply, reliably — with Electrochem lithium batteries. One "D" size Electrochem 9CX cell yields about as much energy as 16 carbon-zinc cells — light and compact power that may last for a decade on the shelf or standing by. With an open circuit voltage of 3.9 volts, the tiny PC cell requires very little real estate on your circuit board, yet can deliver an Amp-hour of usable current.

Whether your requirements are microamps or amps, 100°C or –40°, Electrochem has the cell that you can rely on. Quality that means predictable high performance in a wide range of cells and packs, for applications from outer space to the ocean depths.

Electrochem cells have a long pedigree of quality. The technology that made long lasting and reliable pacemakers possible is ours, and we've harnessed it for industry.

No technology will provide volatile memory backup so compactly, simply, and reliably as lithium cells. No other cells have such a high energy density.

The Electrochem line has a quality cell for almost any use. The workhorse, BCX, provides long life for low drain rate applications at –40° to 72°C. The CSC is the higher rate, higher temperature performer, and the HRT has some of the best of both worlds — higher rate, long life *and* –40°C to 72° operation. For specialized very high drain rates, there's the PWR, while high temperatures — up to 150°C, demand the RMM. The new QTC thionyl chloride is the first to offer economy and E-I quality.

For even higher voltage and capacity, use an Electrochem lithium battery pack, designed and built to be the uncompromising best.

Your first step to quality and high performance is Electrochem, the source for predictable power. The best source.

We'll help you get the right power source for your application. The best source.

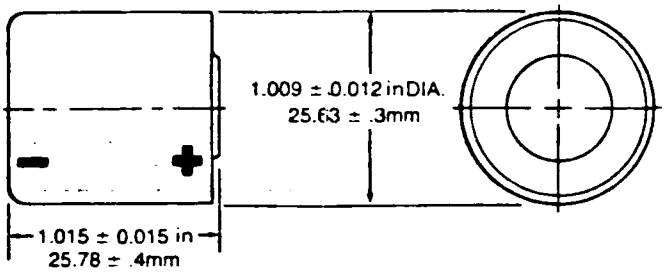
Electrochem Industries A division of Wilson Greatbatch, Ltd. 10,000 Wehrle Drive Clarence, New York 14031
Telephone (716) 759-2828 Telex 91-386

Electrochem Lithium Batteries
Technical Data

Series HRT72

3B752

.45C Size



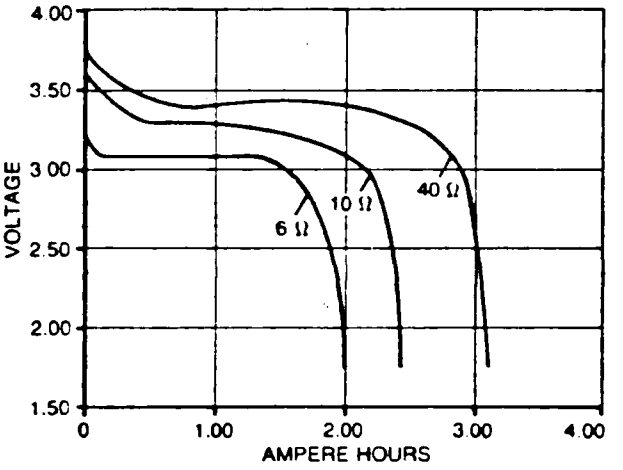
Applications:

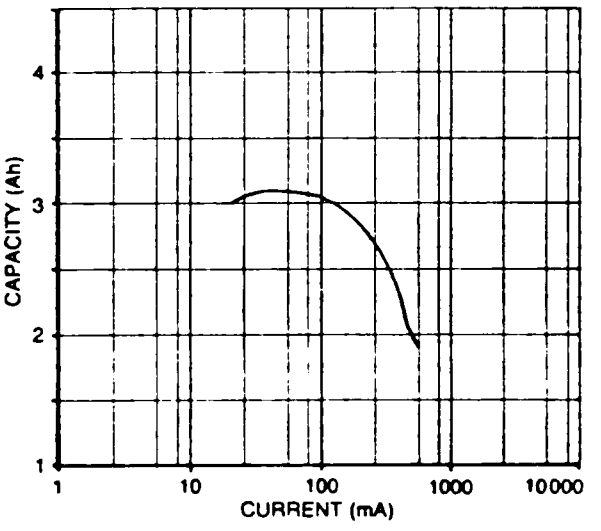
- **Transceivers**
- **Surveillance Devices**
- **Remote Sensing Devices**
- **Electronic Instrumentation**

Specifications:

Open Circuit Voltage (Nominal)	**3.9V**
At Room Temperature:	
Rated Average Load Voltage	**3.4 V**
Rated Discharge Current	**75mA**
Rated Capacity	**3Ah**
Maximum Continuous Discharge Current	**500mA**
Operating Temperature Range	**-40 to 72°C (-40 to 162°F)**
Weight	**.30g**
Safety Fuse	**4 Amp**
Energy Density	**340 $^{Wh}/_{kg}$, .77 $^{Wh}/_{cc}$**

WARNING Excessive heating of the battery may cause a runaway reaction causing the cell to open mildly (venting) or violently (explosion). Do not incinerate, short circuit, use or store outside specified temperature range, puncture, crush, disassemble, recharge or force over discharge (reversal).





The performance curves above are based on tests on fresh cells. These charts are to be used as an application guide only.

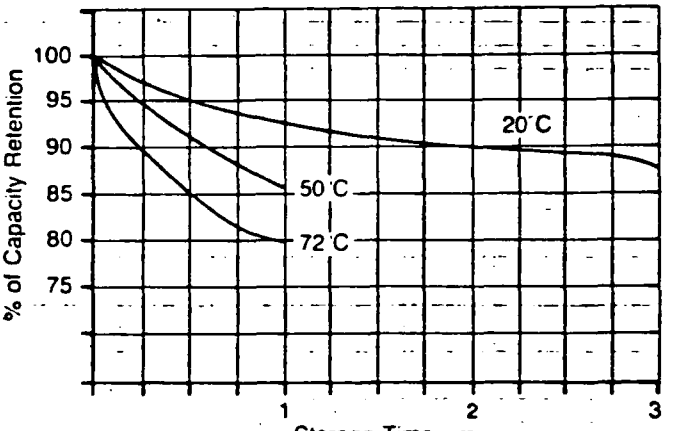
Electrochem Industries A division of Wilson Greatbatch, Ltd. 10,000 Wehrle Drive Clarence, New York 14031

Electrochem Lithium Batteries

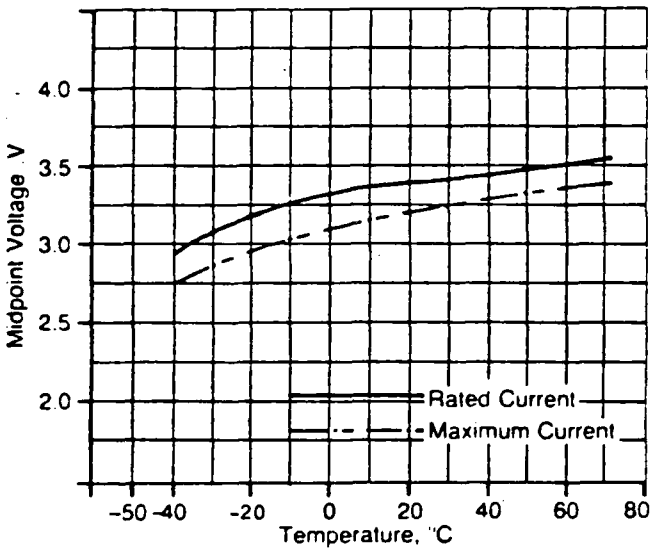
HRT Lithium Oxyhalide Primary Cells

The HRT line of high quality lithium oxyhalide primary cells is the powerhouse of the Electrochem BCX family. The HRT chemistry yields high performance in high-rate applications — an OCV of 3.9 volts, high energy density and long shelf life.

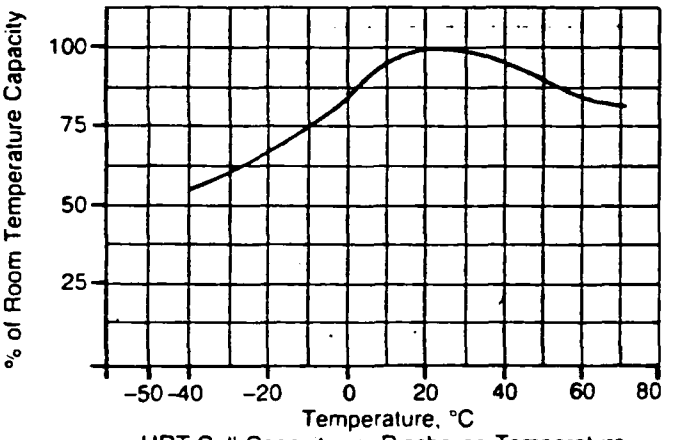
The wound construction, in a hermetic, glass-to-metal sealed 304L stainless steel case, means predictable performance, even in tough environments. From 72°C (162°F) all the way down to –40°C (–40°F), the HRT is the reliable performer, in packs or single cells in .45C, ½C & D sizes.



HRT Cell Capacity vs. Storage Time
(Discharged at Rated Load)



HRT Cell Voltage vs. Discharge Temperature



HRT Cell Capacity vs. Discharge Temperature
(100% Capacity Delivered at Room Temp.)

Your best source for Quality Lithium Batteries

You can have just the right amount of power you need, when you need it, simply, reliably — with Electrochem lithium batteries. One "D" size Electrochem BCX cell yields about as much energy as 16 carbon-zinc cells — light and compact power that may last for a decade on the shelf or standing by. With an open circuit voltage of 3.9 volts, the tiny PC cell requires very little real estate on your circuit board, yet can deliver an Amp-hour of usable current.

Whether your requirements are microamps or amps, 100°C or –40°, Electrochem has the cell that you can rely on. Quality that means predictable high performance in a wide range of cells and packs, for applications from outer space to the ocean depths.

Electrochem cells have a long pedigree of quality. The technology that made long lasting and reliable pacemakers possible is ours, and we've harnessed it for industry.

No technology will provide volatile memory backup so compactly, simply and reliably as lithium cells. No other cells have such a high energy density.

The Electrochem line has a quality cell for almost any use. The workhorse, BCX, provides long life for low drain rate applications at –40° to 72°C. The CSC is the higher rate, higher temperature performer, and the HRT has some of the best of both worlds — higher rate, long life *and* –40°C to 72° operation. For specialized very high drain rates, there's the PWR, while high temperatures — up to 150°C, demand the RMM. The new QTC thionyl chloride is the first to offer economy and E-I quality.

For even higher voltage and capacity, use an Electrochem lithium battery pack, designed and built to be the uncompromising best.

Your first step to quality and high performance = Electrochem, the source for predictable power. The best source.

We'll help you get the right power source for your application. The best source.

Electrochem Industries A division of Wilson Greatbatch, Ltd. 10,000 Wehrle Drive Clarence, New York 14031
Telephone (716) 759-2828 Telex 91-386

9.0 Data Channels

The current approach is to provide four data channels. Two of the channels will be full-up analog channels with software control of gain, offset and bandwidth while the other two are intended for event counting and simple (e.g. two wire temperature transducer) monitoring. The event channels do not contain bandwidth or sampling filters.

The main data channel bandwidths range from 2.5 to 50 Hz. The channel bandwidth is selected by setting the clocking rate of the switched capacitor filter described in paragraph 5.

As noted in the specification of paragraph 5, data monitoring at the higher bandwidths (above 20 Hz) is limited to one channel. This limitation occurs because of the sample rate required to preserve the stated system accuracy goals and the necessity to limit the processor full-up operating time to attain low power operation. In the final analysis, the user may be offered the option of high data rate in both channels, albeit with degraded accuracy.

10.0 Data System

The data algorithms are selectable. The end user can select one of three basic data compression and storage schemes to fit the needs of a particular survey program.

We still must decide if the totality of algorithms will reside permanently in the recorder or whether they will be cycled in and out through the system desktop computer using the system master disk. The decision is tied in with the algorithm design, the power budget and the size of the system memory. At present, all algorithms will be included within the brassboard model.

We note that the counting algorithms that will be provided with the system are not the only ones an end user must use if the end user elects to write some of his own using the instruction set of the selected microcomputer. (The Intel 80C31)

Our basic approach is being directed to providing a menu of counting and storage schemes from which the end user can select those applicable to a projected survey. To do this we are separating the data task into four distinct categories:

(i) Preliminary compression
(ii) Counting method
(iii) Storage configuration
(iv) Data transcription

There are two compression schemes, three counting methods and two storage configurations being designed. Data transcription, i.e. transcription of data from the recorder into a form the engineer can use, will be defined when the algorithms and storage schemes are selected. In conjunction with these, we are designing algorithms for load level counting, peak valley counting and rainflow counting.

Preliminary Compression

Two preliminary compression schemes are being designed, one to handle load level counting and one to serve as a basis for both peak-valley and rainflow counting. The two schemes are similar.

Figure 10.1 is the latest algorithm that sets the stage for either peak-valley or rainflow counting. This algorithm forms vector magnitudes (valley to peak excursions) and also denotes the low point (valley) associated with the vector.

A load level compression scheme placing the level detection within the "loops" of the depicted algorithm is currently being configured.

The data gathered in the compression schemes is then used as a basis for the ensuing count.

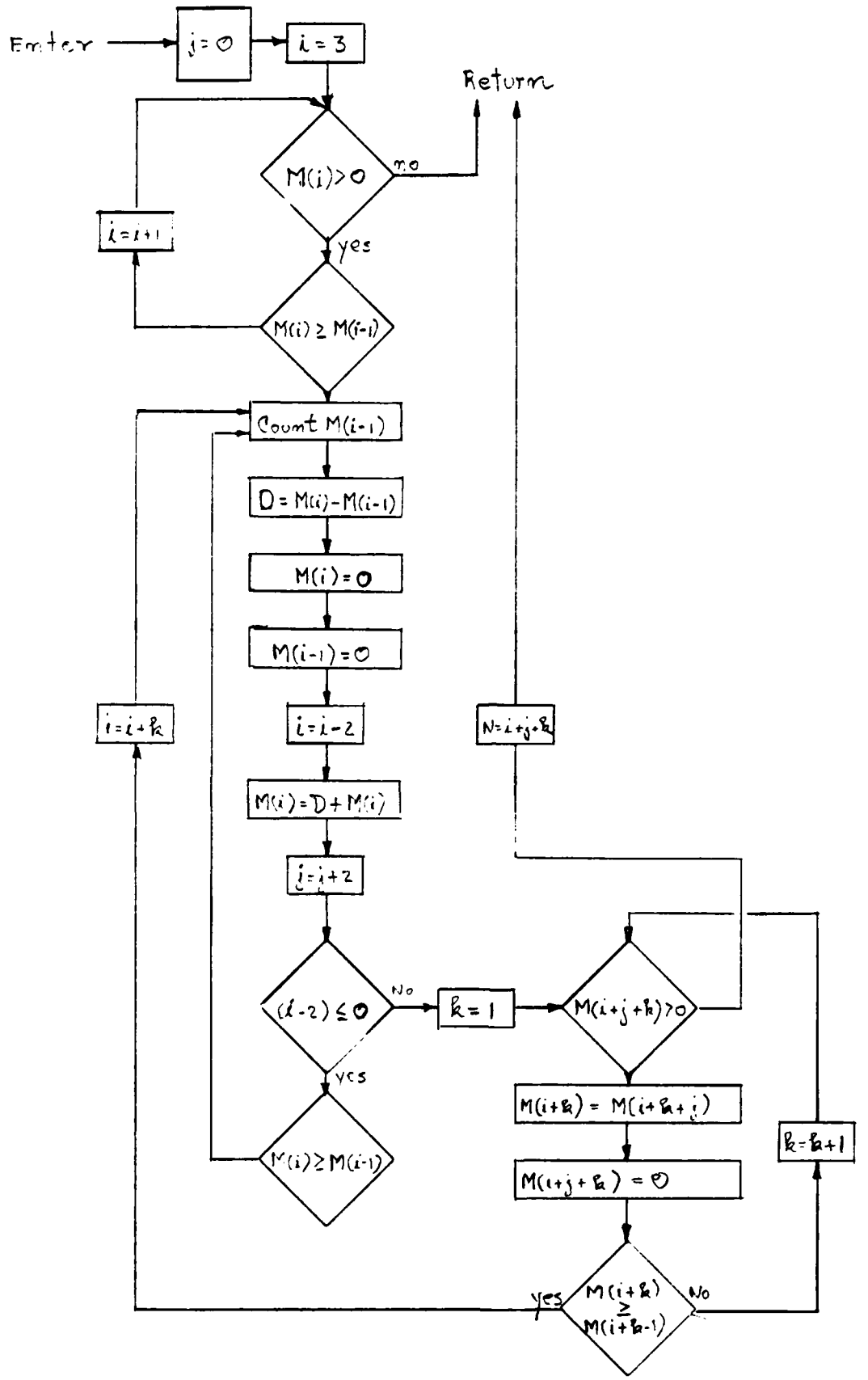
Counting Method and Storage Configuration

The three counting methods are load level, peak-valley and rainflow counting.

Load level counting is exceedance counting as in the counting accelerometer with one exception - load levels below a given level exceedance will not be counted in the recorder but rather will be summed up in the transcription of the data. The storage configuration will be a simple table with three bytes ($>16 \times 10^6$ counts) provided for each level. We are planning on providing up to 32 levels with the number of levels and their value rating (in measured parameter values) selectable by the end user.

Peak valley counting is self descriptive. Successive cycles of the input measurand are classified by their peak to valley excursion. Scrutiny of the algorithm of figure 10.1 reveals the necessary data at hand in terms of vector magnitude and valley values. The data will be stored in a 32 x 32 half matrix as starting point (valley value) and magnitude. In addition, the value of E (1 or 0 - see figure 10.1) denotes whether the first vector was a rising or falling vector. The matrix will have 496 bins with two bytes of storage provided in each bin. There is thus a memory requirement of 2 x 496 = 992 bytes for each channel. Note that limiting the space to two bytes ($\sim$65K counts per bin) results in a 1984 byte requirement. A standard 2K x 8 memory will suffice for data. A peak-valley sequence and the resultant vector set is shown in figure 10.2.

Rain flow counting will enumerate the size and position of closed hysteresis cycles. Of the three methods, rainflow places the severest strain on processor speed and system power. Figure 10.2 shows a stress-strain hysteresis loop family with the resultant vector set. The counting method we have designed is given in figure 10.3. Storage of the data will be as described for peak-valley counting. Here the low point will denote the left most extent of a given closed loop while magnitude will represent its extension along the abcissa (strain width if associated with a strain measurement). This counting scheme is based on the premise the measured parameter behaves as shown in figure 10.2. Figure 10.4 shows how the peliminary compression and counting scheme of figures 10.1 and 10.3 will compress, count and report the hysteresis loops and resulting vector set of figure 10.2.



Reimflow Count
Figure 10.3

11.0 System Accuracy

The design must be carried further before an analytical accuracy assessment can be accomplished. The aim for 5% max and 3% design goal appears realistic.

12.0 Cost Estimate

A cost estimate will be made for the final report and the Phase II proposal.

13.0 Conclusion

At this interim stage, we conclude that the project goals are realistic. Our initial studies are encouraging and we expect a full scale design effort in Phase II will result in creation of the recorder described in the initial solicitation and proposal.

END

10-86

DTIC