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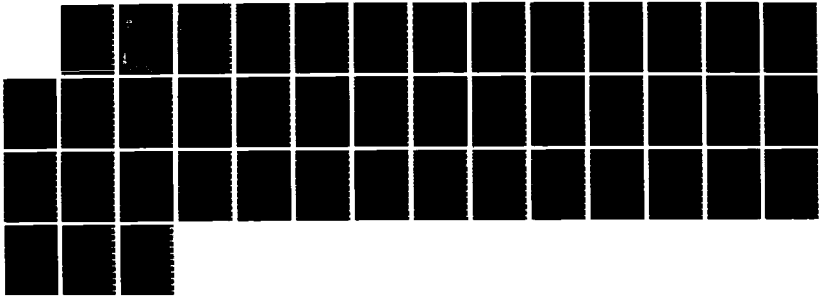

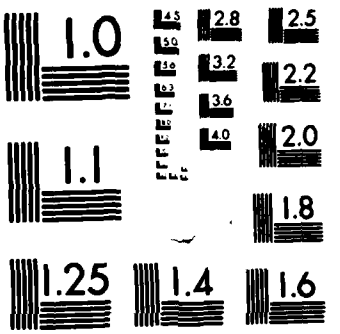

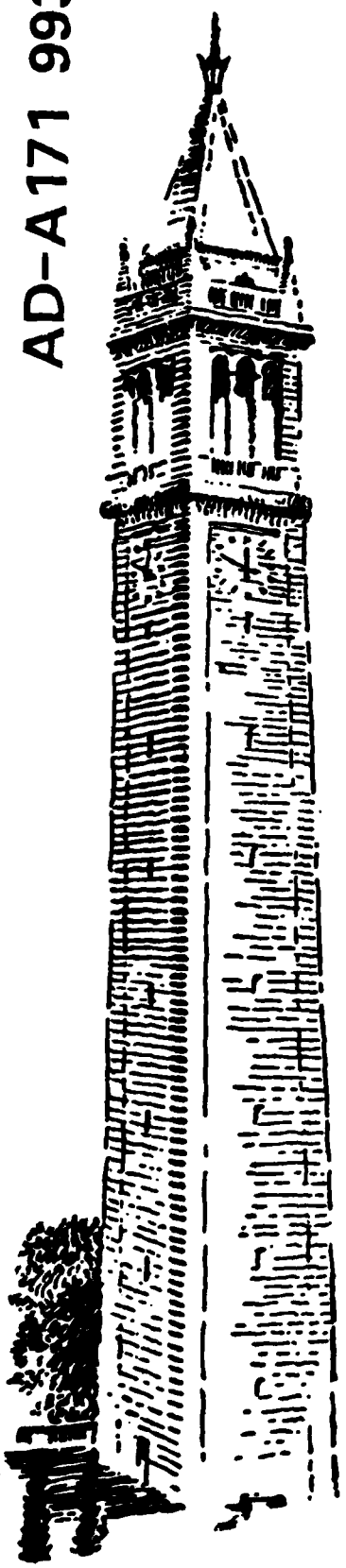

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Report No. UCB/ERL 86/1

JOINT SERVICES ELECTRONICS PROGRAM

Annual Progress Report
(Contract F49620-84-C-0057)
1 May 1985 → 30 April 1986

W.G.Oldham

April 1986

Prepared for:

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ELECTRONICS RESEARCH LABORATORY
College of Engineering
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An annual report of the JSEP (Joint Services Electronics Program) in Electromagnetics, Quantum Electronics, Solid State Electronics, Materials and Devices and Information Systems is presented. In addition, results of the research to date are summarized and significant accomplishments are indicated.

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JOINT SERVICES ELECTRONICS PROGRAM

ANNUAL PROGRESS REPORT (CONTRACT F49620-84-C-0057)
(1 May 1985 - 30 April 1986)

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PART A: DIRECTORS OVERVIEW

The research sponsored by JSEP is presently divided into efforts in Quantum Electronics, Electromagnetics, Solid-State Electronics, and Information Systems. Some of the work crosses these boundaries. A large number of Research Assistants (presently under the title of "Postgraduate Researcher") and projects are supported, in fact more than can be continued into the second year. In general the work sponsored by JSEP is supported to completion, punctuated by a thesis, publications, and graduation of the Research Assistant. The JSEP program is complemented by related programs under separate sponsorship. Complementary projects are common, but overlap of sponsorship is not permitted. (In some publications joint sponsorship is cited; generally this refers to sponsorship of the different individuals. In a few cases an individual is moved from one sponsor to another as one phase of a project ends and another begins.)

JSEP continues to be a significant factor in the ability of the laboratory to respond to important new research opportunities. The research results reported here are significant and gratifying. The list of accomplishments are given in Part B. Part C contains a list of 31 articles published during the reporting period.

Management Issues

A review of the JSEP projects was held April 10, 1985. Each research assistant presented a talk summarizing the results to date and the directions of the research. Based on these presentations it was clear that there were several areas of particular strength in the JSEP program at Berkeley. We propose to emphasize projects which leverage this strength to achieve even more significant research results.

As stated above, in the Berkeley JSEP proposal the projects are grouped according to the categories of Electromagnetics, Quantum Electronics, Solid-State Electronics, and Information Systems. It is interesting to consider another way of grouping the research projects... according to areas of potential application. We find two major areas of eventual application: 1) communication hardware, and 2) complex systems. We may further sub-divide the areas; a possible outline follows.

Potential Research Applications Areas

1) Very Wide-Bandwidth Communication Devices
   (Potential applicatons in all forms of future communication systems.)

   a) Lightwave technology...Integrated optical structures
   b) Millimeter-wave Devices
   c) Electromagnetic propagation
   d) Quantum effects and quantum-well structures
   e) Superconductive Devices
   f) Reliability and basic device limitations

g) Basic research on support technologies:

MBE/LPE growth of III-V compound devices

Patterning to sub-micron dimensions

Materials problems in films and interfaces

2) General Systems Organization, Optimization, Automation, and Simulation Issues

(Potential applications in architecture, design, and operation of complex systems)

a) Control of non-linear systems and Adaptive Control

b) Simulation-based optimization of complex systems.

Grouped in this fashion it is possible to see several advantages to emphasizing certain projects, and to see gaps that must be filled. We have tried to reevaluate the priorities within the JSEP program at Berkeley. Beyond this, we have begun looking at the relative importance of various projects in the Electronics Research Laboratory. With the change of administration of ERL we have undertaken an evaluation of the roles that key projects play in the success of the Laboratory. JSEP is traditionally the most important program, and we intend to keep it the key focus of high-caliber research which cuts across the broad field of electronics. The in-depth review recently undertaken most strongly supports our general positive attitude toward the JSEP program. Counting students and faculty, some 30 plus top notch individuals are engaged in a large number of exciting basic studies which have the potential of continuing the important JSEP contributions to the nation's electronics capability. We would like to further strengthen the program. We appreciate your comments and support.

PART B: ACCOMPLISHMENTS

Three significant accomplishments for this year are as follows:

Materials Issues in VLSI Interconnections –N. W. Cheung, C. M. Hu, and W. G. Oldham (Related to Project SSM-85-1)

The physical mechanisms responsible for oxide breakdown and wearout have been studied in order to explore several possibilities for process improvement and modeling. The oxide charge has been correlated to breakdown, hole generation and trapping rate. It has demonstrated that radiation-hard process produces oxides with longer lifetimes. Further, a mathematical model has been developed that characterizes oxide "defect" density and predicts oxide failure rate and screen yield.

Topological Criteria for Nonlinear Resistive Circuits Containing Controlled Sources to Have a Unique Solution –N. W. Chang, C. M. Hu, and W. G. Oldham (Related to Project ISS-85-1)

A definite solution has been obtained to the following fundamental problem: When does a network containing nonlinear monotone resistors, dc sources and linear controlled sources possess a unique solution? The uniqueness criteria is couched in strictly topological terms. In particular, the uniqueness of a large class of practical nonlinear circuits can be determined, often by inspection, by checking for the presence of a new and fundamental topological structure called a cactus graph. The paper with the above title was published in the *IEEE Trans. on Circuits and Systems*, Vol. CAS-31, No. 8, August 1984, pp. 722-741 and was honored as the *1985 IEEE Guillemin-Cauer Prize Paper* (the most prestigeous award from The IEEE Society on Circuits and Systems).

Protocol Workroom Facility--P. P. Varaiya and J. Walrand (Related to ISS-85-2)

A Protocol Workroom Facility has been completed which will provide a unique environment for experimental research in Communications Network and Distributed Systems. The channel emulator can emulate a large variety of network topologies including bus, rings, point-to-point, and radio.

PART C: DESCRIPTION OF INDIVIDUAL WORK UNITS

RESEARCH PROJECTS

Project No. **Title and Faculty Investigator**

I. **ELECTROMAGNETIC**

EM-85-1 Conformal Time Domain Finite Difference Methods of Solving Scattering Problems—K. K. Mei and D. J. Angelakos

EM-85-2 Millimeter Wavelength Electromagnetic Structures—S. E. Schwarz, K. K. Mei, and D. J. Angelakos

EM-85-S(a) Specialized Equipment for EM-85-2

II. **QUANTUM ELECTRONICS** J. R. Whinnery (Coordinator)

QE-85-1 Analysis of Integrated-Optics Networks Applied to Semiconductor Lasers—J. R. Whinnery and S. Wang

QE-85-2 Electro-Optical Interactions in Quantum-Well Structures: Applications to Detection and Millimeter Mixing— T. K. Gustafson, S. E. Schwarz, and R. M. White

III. **SOLID STATE ELECTRONICS**

A. **Materials** S. Wang (Coordinator)

SSM-85-1 Materials Issues in VLSI Interconnections—N. W. Cheung, C. M. Hu, and W. G. Oldham

SSM-85-2 Studies of MBE Growth Kinetics and High-Energy Ion Implantation in Compound Semiconductors--N. W. Cheung and S. Wang

Project No.	Title and Faculty Investigator

B. **Devices** T. Van Duzer (Coordinator)

SSD-85-1	Problems in E-Beam and Optical Lithography--A. R. Neureuther and W. G. Oldham
SSD-85-2	Study of the Effects Limiting Realization of Far-Submicron Superconductive Electronic Structures--T. Van Duzer
SSD-85-5	Wide-Dynamic-Range Signal Processing Using Monolithic Integrated Circuit Technology--R. G. Meyer, R. W. Brodersen, and P. R. Gray
SSD-85-6	High-Field Transport in MOS Devices--C. Hu and P. Ko

IV. **INFORMATION SYSTEMS** C. A. Deoser (Coordinator)

ISS-85-1	Large-Scale and Nonlinear Circuits Study--L. O. Chua and E. S. Kuh
ISS-85-2	Control in Distributed Systems--P. P. Varaiya and J. Walrand
ISS-85-3	Robust, Adaptive Control and Computer-Aided Design--C. A. Desoer, S. S. Sastry, and E. Polak
ISS-85-4	Optimization Based Computer-Aided Design of Integrated Circuits--A. Sangiovanni-Vincentelli and R. G. Meyer

I. ELECTROMAGNETICS

EM-85-1 Conformal Time Domain Finite Difference Methods of Solving Scattering Problems--K. K. Mei and D. J. Angelakos

Progress

Two dimensional time domain scattering was completed under the support of JSEP. It was demonstrated that a focus beam was obtained when it passed through a Maxwell's fish-eye lens. This work resulted in a thesis (A. C. Cangellaris) in which an abstract follows:

> The method of conforming boundary elements is developed and applied for the numerical comptuation of transient electromagnetic wave scattering from composite two and three-dimensional structures in free space illuminated by an impulsive wave.
>
> The transient scattering problem is formulated as an initial-boundary-value problem governed by Maxwell's differential equations and is numerically solved by means of a finite-element time-domain method. Boundary elements are introduced to conform the desirable conducting geometries and dielectric interfaces. Additional numerical conditions are implemented for satisfying the radiation condition for a the scattered field on an artificial boundary that is used for the truncation of the finite-element region. The convergence and the stability of the numerical method as well as the various types of errors introduced by the numerical discretization, are investigated. Stable numerical models for treating the field singularities at the vicinity of edges and corners are also discussed.
>
> Computations are carried out for scattering by two-dimensional, perfectly conducting cylinders of arbitrary cross-section illuminated by a plane-wave Gaussian pulse at normal incidence. The results are in good agreement with those obtained from a time-domain integral equation approach. Scattering by dielectric cylinders is also computed and the focusing effect of the dielectrics is illustrated. Finally, the method is applied for the numerical computation of scattering by finite conducting cylindrical structures with constant cross-section. The structure can be more complex by adding conducting fins or wires to it. Available experimental results provide us with a further check of the validity of the method. Because of its demonstrated accuracy, efficiency and versatility, the method will be a powerful tool in the study of electromagnetic scattering and penetration of large

The measurement of scattering by object at air-ground interface was also accomplished under the support of JSEP. The abstract of a thesis by T. M. Kvam summarizes the research as follows:

> K. K. Mei's unimoment method has been applied to compute the field scattered by twio types of objects. One is an infinitesimally thin metal disk lying on an air-ground interface. It has a diameter of 10.8 cm. The other

object is a flush buried dielectric cylinder. The cylinder has diameter of 10.8 cm, a height of 4.76 cm and a dielectric constant of 2.61. The incident field is a monochromatic plane wave which propagates normally towards the interface. The component of the scattered electric field parallel to the incident field has been directly measured and compared to the computed results. The measurements were made at several points along a line one inch (2.54 cm) above the ground, passing over the center of the object, and oriented perpendicularly to the incident electric field. The comparison is made for frequencies ranging from 500 MHz to 1000 MHz in 100 MHz increments. The comparison is made for frequencies is presented in terms of plots of the magnitude and phase referenced with respect to the electric field of the incident plane wave. The measurements agree quite well with the calculations, and the degree of agreement establishes the credibility of both. Also presented here is an *in situ* method for determining the dielectric constant of the soil. This method does not require the recompacting or redistributing of the soil, and thus should prove interesting to those wishing to determine, on site, the electromagnetic properties of the undisturbed surface of the earth.

Publications

T. M. Kvam, K. K. Mei, and D. J. Angelakos, "Measurement of Scattering By Targets on Air-Ground Interface," Proceedings of ISAP '85, Kyoto, Japan.

K. K. Mei, "Electromagnetic Wave Snapshots," IEEE ElectroTechnology Review, 1984.

Theses Completed

"Measurements and Computation of Scattering by Buried and Flush Buried Targets," Ph.D. Thesis, Terry M. Kvam, May 1985.

"Time-Domain Computation of Electromagnetic Wave Scattering By the Method of Conforming Boundary Elements," Ph.D. Thesis, A. C. Cangellaris, September 1985.

"2-Dimensional Time Domain Scattering by Buried Objects," Ph.D. Thesis, C. C. Lin, May 1985.

EM-85-2 Millimeter Wavelength Electromagnetic Structures--S. E. Schwarz, K. K. Mei, and D. J. Angelakos

Progress

The past period was spent in determining how to incorporate the powerful techniques of CAD in developing accurate models of passive elements such as transmission lines, sections of lines, bends, inductive and capacitive elements. Conventional modeling of such components relies on the TEM wave assumption and ignores radiation, coupling and end effects. Such low fidelity approaches become unsatisfactory when the frequency increases. For mm-wave devices, it is vital that circuit components be modeled accurately. In a matching network, for example, the end effect of an open circuit or the geometrical discontinuity of the junction of two different lines must be accurately considered. Many similar questions must be answered before a CAD program for mm-wave integrated circuit design can be really effective. We suggest a time-domain approach for modeling of transmission lines, bends, tees, and other components. The proposed technique has the potential to be a breakthrough in CAD of planar circuits. It promises to be more accurate than conventional approaches while still requiring reasonable amounts of computer time.

Existing CAD programs model microstrip as a lossless parallel-strip transmission line. End effects such as open circuits, shorts, and bends are estimated using one or more of the following approximations: (1) use TEM mode; (2) use equivalent dielectric constants to model air-substrate interfaces; (3) use magnetic wall for the vertical sides to obtain wave guide modes. Although radiation effect can be considered using (2), its accuracy cannot be independently confirmed [1]. The wave guide mode method using magnetic walls [2] does not consider radiation or interfaces. Recently, full wave solutions have been obtained using the method of moments [3], but the computations, requiring Sommerfeld's integrals with both the source and field points on the air-substrate interfaces, are very expensive. Because of this, the current distributions across the lines are either assumed apriori or taken to be a constant. Such assumptions become more unsatisfactory when the line takes a bend. Furthermore, because the computations are done in the frequency domain, each frequency requires a completely different computation, which is indeed a very costly procedure. We can show that in the time-domain approach we can obtain results for a wide range of frequencies from a single computation [4,5].

References

[1] Abouzahra, M. D., "On the radiation from microstrip discontinuities," *IEEE Trans. MTT, Vol. MTT-29, No. 7, July 1971*, pp. 666-675.

[2] Chu, T. S. and T. Itoh, "Modified residue calculus technique for microstrip step discontinuities," *Electron. Lett., Vol. 21, No. 7, March 1985, pp. 257-8.*

[3] Katehi, P. B. and N. G. Alexopoulos, "Frequency dependent characteristics of microstrip discontinuities in mm-wave integrated circuits," *IEEE Trans. MTT, Vol. MTT-23, No. 10, October 1985, pp.* 1029-1035.

[4] Cangellaris, A. C., "Time domain computation of electromagnetic wave scattering by the method of conforming boundary elements," Ph.D. dissertation, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, 1985.

[5] Lin, C. C., "Numerical modeling of two dimensional time domain electromagnetic scattering by underground inhomogeneities," Ph.D. dissertation, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, 1985.

EM-85-S(a) Specialized Equipment for EM-85-2

Progress

The following equipment has been ordered from Honeywell Corp.: Model 1412 frequency extender, 65-85 GHz Model CAW-8 plug-in sweep generator, 85-100 GHz Carrying case, model CA-100X.

The equipment, which is being made on special order, is expected to arrive on April 25, 1986. The purpose of this equipment is to extend the range of our present network analyzers to 100 GHz. It will be used to make direct measurements on high-frequency passive and active components. In particular it will be used to test mathematical models of passive planar circuit elements, and to measure the performance of high-frequency active devices.

II. QUANTUM ELECTRONICS J. R. Whinnery (Coordinator)

QE-85-1 Analysis of Integrated-Optics Networks Applied to Semiconductor Lasers--J. R. Whinnery and S. Wang

Progress

The main objective of this research is to apply the concepts developed for integrated optics to semiconductor lasers to extend into nonlinear and short-pulse range of applications. The primary requirement for nonlinear optics applications is to have a coherent source capable of delivering high power. Since the power from a single semiconductor laser is limited by facet damage, integrated-optics approaches must be taken to phase-lock and combine constructively the output power from many individual lasers. There are two basic approaches to accomplish this objective: (1) combining coherent sources in passive waveguides such as Y junctions and (2) forming a coupled laser array. In our present investigation, we take the latter approach and choose evanescent coupled lasers to form an array because of simplicity in the fabrication of the lasers. The three components of this research are: (1) control of array-mode behavior; (2) study of the effect of laser-field carrier interaction; and (3) study of waveguide formation and wavelength control. Here we present a summary of the results reported in publications (items 1-5).

A first-order theory of evanescently-coupled semiconductor-laser arrays is based on the coupled-mode theory developed for integrated optics primarily for passive coupled waveguides. An extension of the first-order theory to N-coupled waveguides establishes the existence of array modes with distinct far-field radiation patterns. The most desirable array mode is one for which the fields in the array elements are all in phase so that practically all the power from the array is radiated into a single lobe of diffraction-limited beam. The in-phase mode requires, however, a substantial gain in the mid-region between laser waveguides to sustain the laser field there. We accomplished this by pumping the mid region as well as the waveguide region of the array. For the first time, single-lobe radiation patterns were reproducibly obtained [1] even at an output-power level of 250 mW. The radiation pattern remained stable at the highest power level even though it became somewhat broadened. The broadening is caused by spatial hole burning in the gain profile. In subsequent studies, arrays with gain profile tailored to the in-phase mode-intensity distribution [2] and arrays with varying spacing [4] were fabricated and investigated. Indeed, the power-dependent broadening was eliminated.

An integral part of our array research is to gain an understanding of the effects of carrier optical-field interaction, which are neglected in the first-order theory of laser arrays. Optical fields affect the carrier distribution through stimulated emission. The phenomenon is known as spatial hole burning. Carriers affect the modal property of a waveguide not only through gain but also through refractive index dependence on carrier. We have incorporated both effects in our computer simulation study of evanescently coupled semiconductor-laser arrays. For the first time, we can follow the evolution [3,4] of the array modes as the injection current is raised. There are important

differences between the results based on the first-order array theory (based on coupled passive waveguides) and those on the active array theory. First, the field distribution in an array is significantly altered. This results in a certain degree of beam broadening. Second, the modal gain for different array modes is very sensitive to the inter-guide spacing, owing to the carrier-induced refractive index change. This means that the physical dimensions governing the guiding property of an array should be properly chosen to ensure the excitation of the in-phase array mode. Finally, a certain radiation mode of a passive array can gradually evolve into a genuine mode of an active array. This is the combined result of the increased gain and the carrier-induced index change. Our simulation results clearly indicate that the passive coupled-mode theory is no longer adequate to fully describe the behavior of evanescently coupled laser arrays. The effects of carrier optical-field interaction must be taken into account in any accurate prediction of array behavior. Because of its importance, the research on active array is being continued and computer simulation studies are being extended to power levels where two or more array modes are lasing. The importance of such studies cannot be overemphasized if we are to use laser arrays in a predictable manner.

The third component of this research program concerns waveguide formation and frequency stabilization. We have grown by MBE super lattices [5] of alternate N-$Ga_{0.7}Al_{0.3}As$ layers of 90 Å thickness and P-GaAs of 100 Å, and subsequently performed zinc diffusion. The samples are then annealing at 750, 800, and 850°C for one hour. Photoluminescence spectra were measured at 2.05°K to detect any significant intermixing of Ga and Al across the superlattice interface. Our original aim was to study the effect of disordering caused by zinc diffusion as a means to produce index guiding in our effort to make multiple-quantum-well (MQW) laser arrays. The multiple quantum wells were intended to force the array to oscillate at a single wavelength defined by the energy levels of the quantum wells. To our surprise the photoluminescence spectra indicate little Al-Ga interdiffusion across the superlattice interface. Our results indicate the important effects of doping on disordering, and are in agreement with previous work by Kawabe et al. (*Appl. Phys. Lett.*, Vol. 46, 1985, p. 849) and the work by Chang and Koma (*Appl. Phys. Lett.*, Vol. 29, 1976). The former paper shows remarkable suppression of disordering when Be doping exceeds Si doping. The latter paper indicates the necessity of T > 900°C for Al-Ga interdiffusion result of our study is that superlattices can be preserved even held at T =850°C for one hour. This work will be extended to modulation-doped 2-D electron-gas devices to determine the limit of processing temperature that can be tolerated by these devices without performance degradation.

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[3] Y. J. Twu, K. L. Chen, S. Wang, J. R. Whinnery, and A. Dienes, "Eigen Mode Analysis of Phase Locked Semiconductor Laser Arrays," *Appl. Phys. Lett.*, Vol. 48, 1986, p. 16.

[4] Y. J. Twu, "Studies of Phase-Locked Semiconductor Laser Arrays," Ph.D. thesis, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley 1985.

[5] Y.-H. Wu, M. Werner, S. Wang, J. Flood, and J. L. Merz, "Effects of Dopants on Disordering of AlGaAs-GaAs Superlattice by Zinc Diffusion," *Electron. Lett.*, Vol. 22, 1986, p. 115.

QE-85-2 Electro-Optical Interactions in Quantum-Well Structures: Applications to Detection and Millimeter Mixing--T. K. Gustafson, S. E. Schwarz, and R. M. White

Accomplishments:

Small area (10^{-14} m^2) devices have been fabricated using an active vertical length of 20 nm of an etched metallic film 2 μm in width. These devices are located above an angled edge of a silicon substrate to facilitate coupling laser radiation up through the angled substrate. The junctions are embedded in a coplanar microwave guide to efficiently couple out microwave difference frequencies resulting from infra-red mixing experiments.

The stationary state model for tunnel junction phenomena has been extended [1,2] to include multi-photon processes. Quantum mixer matrix elements have been derived, as well as general expressions for the response of junction devices to multi-frequency excitations.

The detection process must compete with phonon losses in the metals. This loss of optical power to heating the metals explains the $\omega^{3/4}$ roll off in the signal to noise ratio as a function of i.f. frequency observed in visible frequency point contact mixing experiments [3]. A junction quantum efficiency, defined as the ratio of power contributing to tunneling to the total power coupled into the junction, of approximately 1% at 10 μm for current devices is predicted. This quantum efficiency limits direct detection and the heterodyne response in MBM's and Schottky diodes in the infra-red. Methods of improving this response are suggested by the theory.

CO_2 radiation at 9.3 μm has been detected in the antenna coupled MBM's. The response and coupling characteristics are being compared with theory to aid in the understanding of the diodes.

[1] David Robert Haas, "Infra-red Detection and Mixing in Metal-Barrier-Metal Tunnel Junctions," Ph.D. Dissertation, University of California, 1985.

[2] S. R. Whiteley, D. Haas, and T. K. Gustafson, "Relationship between the Stationary State and First Order Transfer Hamiltonian Tunneling Models," *J. of Appl. Phys.*, July 1985.

[3] D. Haas, T. Yu, and T. K. Gustafson, "On The High Frequency Rolloff in the Response of Junction Detectors," *J. O. S. A-B, Vol. 2, No. 12*, December, 1985

III. SOLID STATE ELECTRONICS

A. Materials S. Wang (Coordinator)

SSM-85-1 Materials Issues in VLSI Interconnections--N. W. Cheung, C. M. Hu, and W. G. Oldham

Summary of Efforts

We have studied the physical mechanisms responsible for oxide breakdown and wearout. Based on this basic understanding, we have explored several possibilities of process improvement and modeling of the oxide defect density, failure rate and screen yield.

Accomplishments

1. We correlated the oxide charge to breakdown and hole generation and trapping rate (deduced from flatband voltage shift). The two are inversely proportional to each other, supporting the model that hole trapping is responsible for breakdown.
2. We have demonstrated that radiation-hard process (low-temperature process) produces oxides with longer lifetime, due to reduced hole trapping rate.
3. A mathematical model that characterizes oxide "defect" density from simple measurements and predicts oxide failure rate and screen yield as functions of device area and electric field has been developed.

Publications

[1] I. C. Chen, S. Holland, C. Hu, "Hole trapping and breakdown in thin SiO_2," to appear in *IEEE Electron Device Lett.*, March 1986.

[2] J. Lee, I. C. Chen, S. Holland, Y. Fong, C. Hu, "Oxide defect density, failure rate and screen yield," to appear in Proceedings of the 1986 VLSI Technology Symposium, May 1986.

[3] S. Holland and C. Hu,"Correlation between breakdown and process-induced positive change trapping in thin thermal SiO_2," to appear in *J. Electrochemical Society.*

SSM-85-2 Studies of MBE Growth Kinetics and High-Energy Ion Implantation in Compound Semiconductors--N. W. Cheung and S. Wang

We have systematically studied the feasibility of using megavolt (MeV) ion implantation for device fabrication. The residual damage distribution created by MeV implants in Si implies in-situ annealing is important to minimize defect formation. Device-quality Si can be obtained at the top few microns of the Si substrate after a post-implant annealing step. We have demonstrated the compatibility of MeV implantation with conventional IC processing procedures. A family of majority-carrier devices (NMOS, CMOS, buried interconnects) and minority-carrier devices (PN diodes, NPN bipolar transistors) have been successfully fabricated. The CMOS latchup susceptibility of the MeV implanted devices is superior to those made by epitaxial buried layers.

We have also investigated ion implantation through MOS structures. The objective of this work is to study the nature of damage introduced by through-oxide implants and to predict long-term reliability of these MOS structures. We have used the constant-voltage stressing method to study the charge trapping in the polysilicon SiO_2 Si system as a function of dose for boron implantation. We have shown that electrical stressing is an effective technique to assess implantation-induced oxide damage and to monitor charge trapping in oxide. For boron, we found that even after high temperature annealing at $950^{\circ}C$, damage still exists which enhances both hole and electron trapping. Both the flatband shifts and the oxide tunneling current can be explained by the competing generation rates of electron traps versus hole traps. Ion-induced electron traps can overcompete hole traps for doses higher than $5x\,10^{13}cm^{-2}$.

Another objective of this research is to explore the feasibility of three-dimensional packing of compound-semiconductor devices. One basic requirement in a multi-level device architecture is the electrical isolation between adjacent layers of device structures. One approach to accomplish this is the MBE growth of cr-doped semi-insulating GaAs films and the subsequent selected-area ion implantation. An attractive alternative is to grow GaAs films by MBE on different underlying materials, for example stripes of GaAs separated by stripes of SiO_2. Our objective is to have the film grown on GaAs to be of device-quality and the film grown in SiO_2 to be of high resistivity. We are happy to report that we have accomplished this. In addition, we also have fabricated devices by MBE to test the quality of our MBE-grown films. The following report is, therefore, divided into two groups: (1) studies of selective epitaxy by MBE of GaAs films on SiO_2 and through windows in SiO_2 and (2) studies of dual-gate FETs and interferometric lasers fabricated by MBE. Here we give a brief summary of the results reported in a series of publications [3-7].

On selective epitaxy, windows in the form of stripes were opened through SiO_2 masks and then GaAs films were grown by MBE. The GaAs films grown through the windows were of single crystal while the films grown on top of the oxides were polycrystalline. The optical and crystalline property [3] of the single crystal region and the electrical property [4] of the polycrysrtalline region were examined.

The photoluminescence spectra taken at 2.2°K from the single crystal region consisting of several exciton peaks near 820 nm and broader acceptor-

related peaks centered at approximately 830 nm are comparable to those observed in high-quality planar MBE-grown GaAs films reported in the literature. Further, the luminescent intensity from the single crystal region is determined by cathodoluminescence to be much higher than that from the polycrystalline region. Transmission electron microscopy (TEM) and x-ray diffractometry were also used. It is found that the GaAs grains on the SiO_2 grow with their (111) planes preferentially parallel to the SiO_2 surface. Therefore, the polycrystalline region consists mostly of small angle grain boundaries.

The high optical quality of the single-crystal GaAs films grown in the window areas makes the selective-area epitaxy very useful for future integration of opto-electronic devices. The polycrystalline GaAs can then be used for electrical isolation. Therefore the electrical properties of the polycrystalline region were studied. It is found that in the low voltage region, the polycrystalline GaAs has a very high resistivity comparable to semi-insulating GaAs. Due to surface charges at a grain boundary, a potential barrier exists, limiting the current flow. As the voltage is increased, the space-charge region extends. When the voltage for punch-through is reached, the current increases rapidly. This is again similar to the behavior of the current-voltage relation observed in semi-insulating GaAs stripes of comparable dimensions.

Based on the measured optical and electrical properties of the MBE grown single-crystal and polycrystalline films, we believe that selective-area growth can be very useful not only for integration of opto-electronic devices but also for integration of electronic devices.

Besides selective-area epitaxy which is mainly a material study, we have also initiated device studies [5-7] and fabricated by MBE a novel four-terminal FET consisting of a MESFET and a MISFET sharing a common channel [5,6]. The transconductance and the current level of the device can be varied and adjusted by applying a negative bias to either the top gate of the MESFET or the back gate of the MISFET. The threshold voltages of the top and back gates can be independently designed without influencing each other. Because of the high g_m / C_{gs} ratio, the device is expected to have a high frequency response. The very high breakdown voltage (> 13 V) achieved should raise the maximum output power per unit width in microwave applications. We also have made interferometric lases by MBE, which showed single-wavelength operation and stable far-field pattern [7]. The excellent performance of the FET and the laser indicates the high quality of the MBE-grown films. Currently we are growing and characterizing films for devices based on two-dimensional electron gas. We are also making preparations for growing GaAs films on Si substrates.

References

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Phys. Lett., Vol. 48, 1986, p. 142.

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B. **Devices** T. Van Duzer (Coordinator)

SSD-86-1 Problems in E-Beam and Optical Lithography--A. R. Neureuther and W. G. Oldham

Progress

Electron-beam lithography offers higher resolution, better linewidth control, and alignment superior to that of photolithography. Compared with organic polymers, inorganic resists offer superb contrast, excellent aspect ratio, and increased compatibility with the pattern transfer process. Both experiment and simulation have been used to study the basic mechanisms of $Ge_{0.1}Se_{0.9}$ inorganic resist under the electron-beam exposure and to explore application of the resist in sub-half-micrometer device fabrication. A first-order model as to how the electron energy drives the vertical silver diffusion were simulated with the Monte Carlo technique. These simulations showed nonlinear sensitivity dependence on beam voltage and silver-sentized layer thickness. Experiments with different accelerating voltages and sensitized layer thicknesses were used to gain insight into the physical mechanisms of exposure. Experimental results agreed with simulations, and demonstrated a sensitivity within a factor of two of that of PMMA at 20 kev. Direct alignment through the inorganic resist layer is feasible at high beam voltage and optimum sensitized layer thickness.

Special test geometries including multiscanning patterns are designed to explore lateral diffusion of silver in the sensitizer as well as proximity effects induced by the backscattered electrons. The short-term goal is to achieve sub-half-micrometer workable lithography with the developed inorganic resist layer served as the mask for reactive ion-etching of the underlying polymer resist. Experimental work on polymers including multilevel resist and metal lift-off schemes are also being undertaken. Feasible applications in microfabrications under current study include superconducting Schottky diode with thin barrier, ultrahigh speed MESFET devices with narrow gate definition, distributed feedback injection lasers with corrugated interface of submicrometer periodicity, and normal- and shear-sensitive tactile array sensors using the quasi-conformal coating capability. An exploratory assessment of the resolution and sensitivity of other novel inorganic resist systems will also be made.

Publications

[1] A. R. Neureuther, "Topography Simulation Tools," *Solid State Technol.*, 29, no. 3 (1986).

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[3] A. R. Neureuther and W. G. Oldham, "Chapter 3: Simulation of Lithography," in *Process and Device Modeling*, edited by W. L. Engl (North-Holland, 1986), pp. 71-106.

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SSD-85-2 Study of the Effects Limiting Realization of Far-Submicron Superconductive Electronic Structures—T. Van Duzer

New Fabrication Technique

One of the goals of efforts to improve circuit fabrication techniques for superconductive electronics is to reduce the spread of tunneling currents in the Josephson junctions. We have developed a method for the formation of junctions in which the formation of the tunneling barrier is done on freshly deposited metal and the counter electrode is deposited without opening the vacuum system. A base layer of niobium is covered with a layer of SiO. A square hole is formed by exposing crossed lines in two superimposed layers of photoresist; this gives accurate control of the size of the hole, which is especially important for junctions of 2x2 μm^2 or smaller. Reactive ion etching is used with the resist mask to etch a vertical walled hole in the SiO. A very thin layer of a lead alloy is deposited; it is thin enough that the side walls of the SiO are not covered. The oxide barrier is then formed and a thick layer of a lead alloy is deposited as the counter electrode. With this procedure we have made series strings of junctions with spreads of Josephson currents as small as $\sigma = 2\%$ for 2x2 μm^2 junctions. It appears possible to extend the technique to make Nb-Al_2O_3-Nb junctions, which have been shown in another fabrication technique to be robust and of good electrical character. This work has been presented at the Workshop on Superconductive Devices, Circuits, and Systems, Waterville Valley, NH, August 1985 and at the West Coast Superconductive Electronics Meeting, Berkeley, CA, March 7, 1986.

Picosecond Testing of a New Logic Gate

We have designed a logic gate with three times higher output voltage in order to achieve some increase of speed of logic chips. The higher output voltage leads to smaller transmission lines with significant space saving on the chip. This increases the circuit density, which increases the gate count and also reduces the intergate delays. This gate will be tested on a chip containing also a sampling circuit that will allow determination of rise times less than 5 ps. Gate delays will be measured and related to the scaling rules developed as a part of this research. Fabrication is now underway.

Publications

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[2] T. Van Duzer and H. Ko, "Miniaturization of Josephson Logic Circuits," *IEEE Trans. Magn.*, Vol. MAG-21, March 1985, pp. 725-728.

[3] T. Van Duzer and N. F. Raley, "Simple, Nondestructive Silicon Membrane Thickness Measurement Using a Scanning Electron Microscope," *Jour. Appl. Phys.*, Vol. 58, July 1985, pp. 280-286.

We intend to submit the new fabrication technique soon for publication.

SSD-85-5 Wide-Dynamic-Range Signal Processing Using Monolithic Integrated Circuit Technology—R. G. Meyer, R. W. Brodersen, and P. R. Gray

This work resulted in a thesis (K.-L. Lee); the abstract follows:

Distortion mechanisms in switched-capacitor circuits have been investigated by theoretical analysis and closed form expression relating harmonic distortion to circuit parameters derived. The relative importance of each distortion source has been determined from the theoretical results.

Design techniques for low distortion applications have been devised and applied to several monolithic test circuits, which include a 6^{th} order experimental filter, a switched-capacitor integrator, test operational amplifiers and test capacitors. The filter design uses a fully differential, class A/B op amp with a continuous-time common-mode feedback circuit, and a node voltage scaling technique. A novel four-phase clock is also implemented in these test circuits to test the relative importance of the effect of clock related noise.

Distortion measurements on the test circuits show good agreement with the theoretical results, and for the 6^{th} order switched-capacitor filter the THD is 0.02% within the whole 4 kHz bandwidth for 82 dB dynamic range (relative to the noise floor).

SSD-85-6 High-Field Transport in MOS Devices--C. Hu and P. Ko

Accomplishment

We have studied the dependence of channel electric field and hot-electron effects on MOSFET channel length, width, junction depth, oxide thickness, drain voltage and gate voltage. The results help us understand the effects of device scaling on hot-electron effects.

Summary of Efforts

We have found the substrate and gate currents to be proportional to channel width in several NMOS and CMOS processes. This means that the electric field does not peak at the field oxide edges.

The maximum channel electric field, E_m, has been shown to determine the rate of all hot-electron activities including device degradation and

$$E_m = (V_{ds} - V_{dsat}) / 0.22\, T_{ox}^{1/3} x_j^{1/2}$$

The channel length and gate voltage affect E_m through the saturation voltage V_{dsat} term. The oxide thickness and junction depth are perhaps even more influential over hot-electron effects than channel length. This E_m model has been verified with substrate current measurements and 2-D device simulations.

Publications

[1] T. C. Ong, S. Tam, P. K. Ko, and C. Hu, "Width Dependence of Substrate and Gate Currents in MOSFET's," *IEEE Trans. on Elect. Devices*, Vol. ED-32, September 1985, p. 1737.

[2] T. Y. Chan, P. K. Ko, and C. Hu, "Dependence of Channel Electric Field on Device Scaling," *IEEE Elect. Device Letters*, Vol. EDL-6, October 1985, p. 551.

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IV. INFORMATION SYSTEMS C. A. Desoer (Coordinator)

ISS-85-1 Large-Scale and Nonlinear Circuits Study—L. O. Chua and E. S. Kuh

Progress

A. A Dynamic Model for the MOS Structure

Frequency-dependency is a phenomenon that is observed in many different materials and devices. One of the most familiar examples is the frequency-dependent C-V characteristics observed in MOS (Metal-Oxide-Semiconductor) structure (also known as MOS capacitor or MOS diode. The MOS structure is the most useful device in the study of semiconductor surfaces and an understanding of its surface physics is of great importance to device operations. Furthermore, the MOS structure plays a major role in the development and the characterization of MOS processing which has become the workhorse of today's IC industry. I particular, the MOS structure is placed in the test pattern of nearly all MOS wafers to evaluate important process and device parameters.

Our objective here is to introduce a complete circuit model of the MOS structure which is derived entirely from device physics and which yields correctly predicted MOS device behavior at *all* frequencies and for *large-signal excitations*. Some preliminary efforts have been made in the study of the physics of MOS structure and we have recently derived a nonlinear *higher-order dynamic* model which yields satisfactory results. The model consists of three elements, namely, a linear oxide capacitor C_o, a nonlinear depletion capacitor $C_d(v_s)$ (where v_s is the semiconductor surface potential) and a *C-dynamic element* which accounts for the nonequilibrium minority carrier transport in the semiconductor.

Our new dynamic model agrees qualitatively and quantitatively with the experimental results, not only at low and high frequencies, but at *all intermediate frequencies*. Moreover, since this model is described by a nonlinear differential equation it can be used for large-signal transient analysis. The parameters used in this model are the basic device parameters and can be easily measured.

Further investigation will be made of the large-signal behaviors of the MOS structure which should provide important insight into the dynamic nature of the charge redistribution of the structure. Continued efforts will also be made in the study of the basic device physics equations and thus modification can be made to improve the accuracy and efficiency of the new model.

B. Building-Block Layout Design

A new method of placement for building-block layout design of IC chips has been developed. This combines bottom-up clustering with top-down partitioning, and yields excellent results for a number of examples tested. The method has been implemented in the software program BBL.2 (the Berkeley Building-Block

Layout System).

Publications

[1] T. Nishi and L. O. Chua, "Topological Criteria for Nonlinear Resistive Circuits Containing Controlled Sources to Have a Unique Solution," *IEEE Transactions on Circuits and Systems* Vol. CAS-31, August 1984, pp. 722-741.*

[2] L. O. Chua and A. C. Deng, "Negative Resistance Devices: Part II," *International Journal of Circuit Theory and Applications*, Vol. 12, 1984, pp. 337-373.

[3] L. O. Chua and A. C. Deng, "Canonical Piecewise-Linear Analysis: Part II," *IEEE Transaction on Circuits and Systems*, Vol. CAS-32, May 1985, pp. 417-444.

*This paper [1] was awarded the Guillemin-Cauer Prize Paper.

ISS-85-2 Control in Distributed Systems—P. P. Varaiya and J. Walrand

Progress

We have completed the hardware design of the Protocol Workroom Facility which will provide a unique environment for experimental research in Communications Networks and Distributed Systems. The overall facility is described in [1]. The channel emulator can emulate a large variety of network topologies including bus, rings, point-to-point, and radio. A 4-node channel emulator has been built. It is described in [2]. The node emulator design is completed, and a prototype will be built by June 1986.

Our earlier work on distributed estimation is summarized in [3]. We show that if different estimators have the same model, then they can arrive at a consensus. If they have different models, they may reach an impasse which serves to indicate that their models are different.

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[2] A. Kao and L. Ludwig, "Channel Emulator for U.C. Berkley Protocol Workroom Facility," Electronics Research Laboratory Memorandum No. UCB/ERL M85/83, University of California, Berkeley, February 1986.

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ISS-85-3 Robust, Adaptive Control and Computer-Aided Design-- C. A. Desoer, S. S. Sastry, and E. Polak

The following students have been supported on the grant:

Niklas Nordstrom
Li-Chen Fu (Fall 85-)
Saman Behtash (Spring 86-)

The area of research has been adaptive identification and control. Nordstrom and Sastry have worked on problems of identification by least squared or gradient style techniques for possibly unstable linear systems. They have given frequency domain conditions for adaptive identification [1,2]. Fu and Sastry have been involved in adaptive tracking, i.e., using techniques of adaptive control to devise servo-control laws for tracking of slowly varying reference signals as would be encountered in tracking of aircraft, missile-guidance as well as the adaptive control of robots. (Reports to appear)

In perhaps the most exciting work to date Behtash and Sastry have been studying fundamental convergence properties of a new class of networks that has been proposed by Hopfield and others as a candidate for Computer-Associative Memories, and models for distributed computation. At this point their work has been to fill in some important analytic gaps in the literature. This work will be continued in several directions:

i) An analytical investigation of the properties of the proposed networks: such as their convergence and "fail-softness". An investigation into the "self-organizing" properties of randomly or probabilistically interconnected networks, such as their reconfigurability or their probabilistic convergence properties. Further, on an on-going basis to suggest new topologies of interconnection of various memory/processor primitives along with their performance analysis.

ii) Research on algorithms of data processing, data fusion, intelligent control (knowledge based), decentralized decision making which could use the massively parallel and flexibly reconfigurable processors and memories.

References

[1] N. Nordstrom, "Adaptive Identification of Possibly Unstable-Linear Systems," Electronics Research Laboratory Memorandum No. UCB/ERL M86/30, April 1986. University of California, Berkeley, submitted to the *IEEE Trans. on Automatic Control.*

[2] N. Nordstrom and S. Sastry, "Persistency of Excitation in Possibly Unstable Continuous Time Systems an Parameter Convergence in Adaptive Identification," to appear in the Proc. of the IFAC Workshop on Adaptive Identification, Lund, Sweden, July 1986.

ERL-85-4 Optimization Based Computer-Aided Design of Integrated Circuits—A. Sangiovanni-Vincentelli and R. G. Meyer

Timing Analysis Algorithm

Most timing analysis algorithms use backward Euler integration and one sweep of relaxation techniques to decompose and solve the system of nonlinear algebraic equations describing the circuit equations. However, these algorithms cannot produce accurate solutions when floating capacitors are present in the circuit under analysis. The Implicit-Implicit-Explicit (IIE) method has been proven to be consistent, stable and convergent when applied to circuits containing floating capacitors. In addition, we have proved that for a special class of circuits, the IIE method is A-stable.

This IIE method has been implemented in the circuit simulation program RELAX. It is used as a pre-processor to the waveform relaxation based circuit simulator RELAX, since the speed of convergence of the waveform relaxation methods used in RELAX can be greatly improved if a fairly accurate initial guess for the waveforms is provided. The result of the simulation will be available soon.

Aggregation Methods for Large-Scale Circuit Simulation

Relaxation-based circuit simulation has proved very effective for accurately simulating large-scale digital circuits, but, if tight feedback loops are present, the convergence of relaxation algorithms can be slow. Aggregation methods have been proposed to speed up relaxation algorithms used in the solution of large systems of algebraic equations.

A survey of aggregation methods was compiled by F. Chatelin and W.L. Miranker [1], who also showed that all the existing aggregation methods are nothing else but different implementations of the same mathematical idea; more precisely, aggregating a system corresponds to performing a projection on a suitable linear subspace: different aggregation methods correspond to different choices of subspaces.

We have developed a new algorithm that uses information obtained from the relaxation process to build the aggregated system; theoretical analysis and numerical experiments performed on several matrices show that this algorithm is more effective than the other aggregation methods proposed so far. In particular, when applied to solve a linear system arising from a placement problem, it yielded an approximation to the real solution that was several orders of magnitude more accurate than the one computed by "standard" aggregation after the same number of iterations. Our results have been published in the following paper:

G. Casinovi and A. Sangiovanni-Vincentelli: Aggregation Methods for the Solution of Large Scale Systems of Linear Algebraic Equations. *Proceedings of the 1985 International Conference on Circuits and Systems*, Kyoto, Japan, June 1985, pp. 1055-1058.

Statistical Circuit Design

Our work on statistical circuit design has had a major breakthrough this year. We have developed a model and a methodology that is revolutionary in several aspects. The model is based on the profit to be expected from the production of an IC as a function of its parametric design. The model is to serve as the criterion function in an optimization-based design methodology.

The profit model has two components--a cost model and a revenue model. Important improvements in the cost model include: the development and documentation of a procedure for the construction of an appropriate flow structure for the processing and testing of circuits after wafer separation; incorporation of a more sophisticated treatment of defect yield and its dependence on components of die area.

The heart of the revenue model is a stochastic model for quantity of circuits demanded by customers as a function of the specs and price of the product. The estimation of demand is based on a relatively complex market research methodology, important detailed characteristics of which have been fixed recently. The methodology yields a demand model for each customer who supplies the required information. The most significant new improvement is the removal of the assumption that the specification types (e.g., voltage offset, supply current, bandwidth) of greatest importance to each customer are the same for all customers.

An application outside the one originally planned has been found for the mechanism provided in the methodology for capturing the price, multi-performance tradeoff judgements of a single customer. For the direct benefit of customers who purchase by contract, it can replace the rigid lowest-bidder-meeting-specs approach currently in widespread use.

The profit model contains considerable structure and detail, and requires ambitious documentation. This property has been addressed with the recent publication of an extensive paper [RIL86].

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Publications

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APPENDICES

LIST OF PUBLICATIONS

L.O. Chua A-C Deng	5/85	"Canonical Piecewise-Linear Analysis: Part II—Tracing Driving-Point and Transfer Characteristics," *IEEE Trans. on Circuits and Systems*, vol. CAS-32, no. 5, May 1985, pp. 417-444.
A.R. Neureuther W.G. Oldham	5/85	"Resist Modeling and Profile Simulation," *Solid State Technology*, May 1985, pp. 139-144.
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D. Giandomenico D-S Kuo C. Hu	8/85	"Oscillations in Multichip Power MOSFETs," *PCIM*, August 1985, pp. 74-78.
T-C Ong S. Tam P-K Ko C. Hu	9/85	"Width Dependence of Substrate and Gate Currents in MOSFET's," *IEEE Trans. on Electron Devices*, vol. ED-32, no. 9, September 1985, pp. 1737-1740.
T.Y. Chan P-K Ko C. Hu	10/85	"Dependence of Channel Electric Field on Device Scaling," *IEEE Electron Device Letters*, vol. EDL-6, no. 10, October 1985, pp. 551-553.
P.B. Katehi N.G. Alexopoulos	10/85	"Frequency Dependent Characteristics of Microstrip Discontinuities in mm-Wave Integrated Circuits," *IEEE Trans. MTT*, vol. MTT-23, no. 10, October 1985, pp. 1029-1035.
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J.M. Hong S. Wang T. Sands J. Washburn J.D. Flood J.L. Merz T. Low	1/86	"Selective-Area Epitaxy of GaAs Through Silicon Dioxide Windows by Molecular Beam Epitaxy," *Appl. Phys. Lett.*, vol. 48, no. 2, January 13, 1986, pp. 142-144.
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LIST OF MEMORANDUMS

E. Polak D.Q. Mayne	M85/33 4/26/85	Algorithms for Optimization Problems with Exclusion Constraints
D.Q. Mayne E. Polak	M85/52 6/21/85	An Exact Penalty Function Algorithm for Control Problems with State and Control Constraints
D. Riley	M85/58 5/27/85	A New, Profit Maximization Methodology for Statistical Design of Integrated Circuits, Part I: Problem Formulation
N. Nordstrom	M85/72 8/30/85	Order Reducing Approximation of Two-Time-Scale Stochastic Discrete Linear Time-Varying Systems
W.Y. Leung	M85/76 9/26/85	Characterization of Inorganic Resist for VLSI Fabrication
A. Fawaz D. Giralt L. Ludwig	M85/82 11/85	The PROTOCOL WORKROOM: An Experimental Protocol and Distributed Systems Research Facility for UC Berkeley
A. Kao L. Ludwig	M85/83 11/85	A Flexible 10 Mbps Channel Emulation System for Communications Research
A. Fawaz L. Ludwig M. Peck	M85/84 11/85	Node Emulator Architecture for the UC Berkeley Protocol Workroom Facility
L.O. Chua T. Matsumoto M. Komuro	M85/102 10/20/85	Double Scroll Family: Part I Rigorous Proof of Chaos, Part II Rigorous Analysis of Bifurcation Phenomena
R. Cieslak A. Fawaz	M85/103 12/12/85	A General Architecture for Data Link Layer Controllers
C.A. Desoer S.M. Shahruz	M86/9 1/9/86	Stability of Nonlinear Systems with Three Time Scales

L.O. Chua C-C Chang	M86/14 2/7/86	A Simple Dynamic Circuit Model for MOS Structure
A-C Deng L.O. Chua	M86/22 3/13/86	Nonlinear Electronics (NOEL) Package 0: General Description
A-C Deng L.O. Chua	M86/23 3/13/86	Nonlinear Electronics (NOEL) Package 1: Linear Circuit Formulations, N-Port Representations, and State Equations
A-C Deng L.O. Chua	M86/24 3/21/86	Nonlinear Electronics (NOEL) Package 2: Computer Generation of Symbolic Transfer Function
A-C Deng L.O. Chua	M86/26 3/21/86	Nonlinear Electronics (NOEL) Package 3: Nonlinear DC Analysis

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