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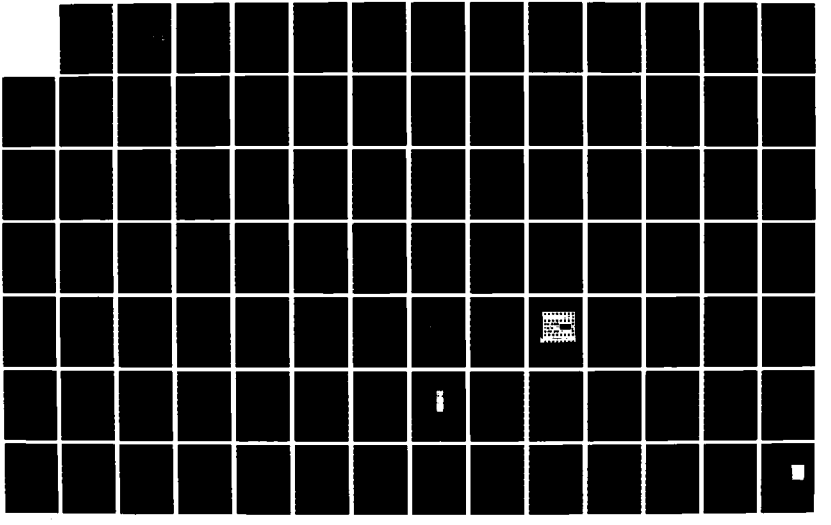

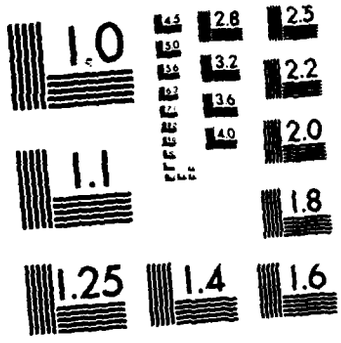

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ABSTRACT

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The hydrogenated amorphous silicon (a-Si:H) thin film transistor (TFT) has been studied extensively for several years. Its application as a switching element in large area liquid crystal display arrays has been demonstrated. Modeling studies have been performed to quantify and explain the performance of the a-Si:H TFT. However, throughout these investigations little has been reported concerning the ambipolar nature of the a-Si:H TFT; that is, the ability of the device to operate alternatively as an n-channel or a p-channel device.

The work described in this thesis extends the previous work by specifically addressing the ambipolar behavior of the a-Si:H TFT. In particular, a process sequence has been developed to fabricate high quality ambipolar a-Si:H TFTs with emphasis on ohmic source/drain contacts. Using experimental data from these devices and TFT theory, a model has been developed for obtaining the output drain current vs. drain voltage of ambipolar a-Si:H TFTs. The model involves the numerical integration of an interpolated sheet conductance function. By using the appropriate flat-band voltage, the model accurately predicts the experimental output drain current characteristics for both n- and p-type operation over many orders of magnitude.

FABRICATION AND MODELING OF AMBIPOLAR HYDROGENATED AMORPHOUS SILICON THIN FILM TRANSISTORS

A Thesis

Submitted to the Faculty

of

Purdue University

by

Harold F. Bare, Jr.

In Partial Fulfillment of the

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of

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ABSTRACT

Bare, Harold F., Jr. Ph.D., Purdue University. August 1986. Fabrication and Modeling of Ambipolar Hydrogenated Amorphous Silicon Thin Film Transistors. Major Professor: Gerold W. Neudeck.

The hydrogenated amorphous silicon (a-Si:H) thin film transistor (TFT) has been studied extensively for several years. Its application as a switching element in large area liquid crystal display arrays has been demonstrated. Modeling studies have been performed to quantify and explain the performance of the a-Si:H TFT. However, throughout these investigations little has been reported concerning the ambipolar nature of the a-Si:H TFT; that is, the ability of the device to operate alternatively as an n-channel or a p-channel device.

The work described in this thesis extends the previous work by specifically addressing the ambipolar behavior of the a-Si:H TFT. In particular, a process sequence has been developed to fabricate high quality ambipolar a-Si:H TFTs with emphasis on ohmic source/drain contacts. Using experimental data from these devices and TFT theory, a model has been developed for obtaining the output drain current vs. drain voltage of ambipolar a-Si:H TFTs. The model involves the numerical integration of an interpolated sheet conductance function. By using the appropriate flat-band voltage, the model accurately predicts the experimental output drain current characteristics for both n- and p-type operation over many orders of magnitude.

CHAPTER 1
INTRODUCTION

1.1 Background

Since the early 1970's amorphous silicon has attracted considerable attention as a material for potential semiconductor device applications. With the realization that amorphous silicon could be prepared with characteristics somewhat similar to those of single-crystal silicon, much effort has been expended in developing amorphous silicon into a very viable semiconductor technology. In particular, with the realization that hydrogenated amorphous silicon (a-Si:H) could be prepared with a low density of localized states in the mobility gap [1] and could be doped n- or p-type to control its electronic properties[2], the foundation was laid for much of the device developmental work.

The development of the a-Si:H technology has been further enhanced by its compatibility with existing single-crystal Si integrated circuit processing technology[3]. For example, even though processing temperatures must be kept low enough to prevent crystallization of the amorphous material, the same (or similar) photoresist processes, gate dielectrics, metals for interconnect layers and materials for passivation layers can be used for processing both single-crystal and amorphous silicon devices.

Another factor encouraging the development of a-Si:H device technology is that a-Si:H can be deposited over large areas while maintaining its attractive electrical and optical properties[4]. Such a feature makes a-Si:H ideally suited for those applications requiring similarly processed active devices over large areas.

An example which demonstrates the large area capability of a-Si:H is seen in the use of a-Si:H thin film transistors (TFTs) as switching elements in liquid crystal display arrays[5]. Much work has been done to characterize and optimize the performance of these devices. In particular, several device schemes have been demonstrated[6,7,8] and several theoretical models have been developed to predict the performance[9,10,11,12]. However, throughout these many investigations very little has been said or observed concerning the ambipolar

nature of the a-Si:H TFT; that is, the ability of this device to operate alternatively as an n-channel or a p-channel device.

Since the primary application of the a-Si:H TFT has been as a simple switching element, this apparent lack of interest in the ambipolar behavior is not surprising. However, as the device quality of a-Si:H continues to improve, the ambipolar nature of these devices could lead to important novel circuit applications, thereby increasing the overall usefulness of a-Si:H TFTs.

1.2 Thesis Overview

With the aforementioned lack of research into the ambipolar nature of a-Si:H TFTs, the investigation described in this thesis was conducted to better understand this phenomena. In particular, an ambipolar a-Si:H TFT fabrication sequence was developed with emphasis on device quality a-Si:H films, ohmic source/drain contact regions, and a high quality gate insulator. Devices fabricated with this process were shown to demonstrate the desired ambipolar behavior. A model was then developed from elementary TFT theory to predict the output drain current vs. drain voltage characteristics of these ambipolar devices.

Chapter 2 contains a review of the relevant literature on the development of a-Si as a viable semiconductor material with emphasis on a-Si:H TFTs. A review of the previous work done to investigate the ambipolar behavior of a-Si:H TFTs is also included. Chapter 3 describes the development of the ambipolar a-Si:H TFT processing sequence used to fabricate devices for use in the subsequent modeling effort. Chapter 4 describes the modeling effort performed to predict the output drain characteristics of the ambipolar a-Si:H TFT. Finally, Chapter 5 contains a summary of this investigation and recommendations for future work.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

Since its attractive semiconducting properties were first recognized in the early 1970's, much has been written on amorphous silicon and its use in semiconductor devices. Some of the more recent reviews covering the important aspects of this subject have been edited by Brodsky[13], Kazmerski[14], Willardson and Beer[15], and Joannaopoulos and Carlson[16,17]. Each review covers the basic properties and theoretical models of a-Si along with discussions of device applications. It should be emphasized that most work done to date has been of an experimental rather than of a theoretical nature. Thus most of the work presented in these reviews is an explanation of experimental observations and, like the field of amorphous semiconductors, is rather limited in available theory.

The purpose of this review is to discuss the present level of understanding of a-Si as it is used in thin film transistors as well as other applications. This review will be conducted by first describing some of the basic properties and theoretical models of amorphous silicon which demonstrate the use of a-Si as a viable semiconductor material. Next, an account will be given of the experimental and theoretical development of the a-Si TFT including previous work on its ambipolar behavior. Finally, a summary will be given of the many uses of a-Si demonstrated to date.

2.2 Basic Properties of Amorphous Silicon

2.2.1 Structure and Localized States

The basic properties of amorphous silicon relate directly to its continuous random atomic network. As shown in Figures 2.1a and 2.1b, this network is characterized by short-range rather than long-range order. In contrast, as shown in Figure 2.1c, single-crystal Si is composed of a highly ordered atomic network with long-range, as well as short-range, order. The short-range amorphous order is characterized by a well-defined first-neighbor separation,

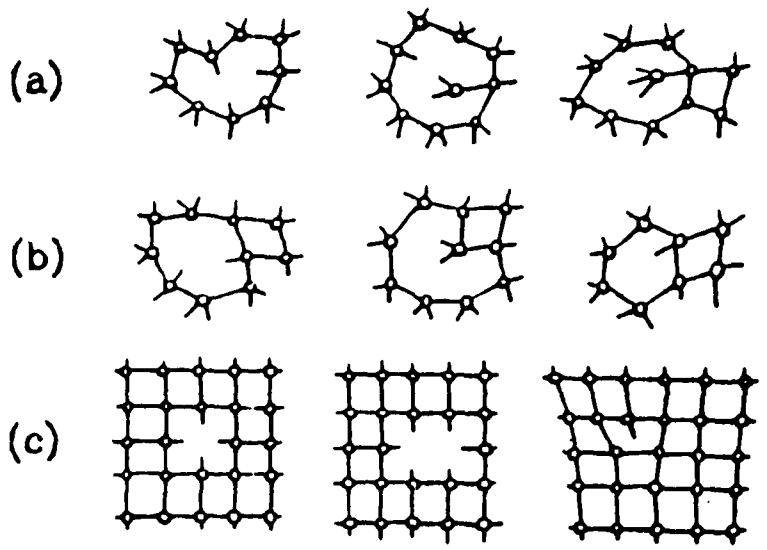


Figure 2.1 Schematic representation of possible defects in (a), (b) a-Si, and (c) single-crystal Si. The three defects in (a) and (b) correspond to three dangling bonds in various configurations in a continuous random network. The three defects in (c) correspond to a monovacancy, a divacancy and a dislocation. From Ref. 18.

the same bond length in single-crystal Si, and a broadened distribution of second-neighbor separations due to ±5% variation in bond angle[19].

The gross features of the atomic and electronic structures of both single-crystal and amorphous Si are dominated by their covalent bonding requirements[20]. Thus the short-range order in a-Si is expected to be similar to that found in single-crystal Si leading to conduction and valence bands such as shown in Figure 2.2. The existence of such band-like behavior in a-Si has been verified by the activated temperature dependence of the electrical conductivity described by the relation[21]:

$$\sigma = \sigma_o \, e^{-\Delta E/kT} \tag{1}$$

where σ_o is a pre-exponential factor in $(\text{mho-cm})^{-1}$, ΔE is the activation energy in eV, k is $8.62X10^{-5}$ eV/K and T is the temperature in Kelvin.

Although the activated conductivity temperature dependence seems to indicate a sharply defined energy bandgap, such is not actually the case because of localized states at the band edges. The lack of long-range order in the material gives rise to localized states within and at the edges of the bandgap. See Figure 2.2b. These states are termed "localized" because a quantum mechanical description of them indicates that they can only be found in restricted regions of the material[20]. Those quantum states that can be found anywhere within a region of the material are termed "extended" and refer to those states in the conduction and valence bands. Conduction mechanisms in single-crystal Si take place through extended states alone, while such mechanisms in a-Si take place through both extended and localized states.

Localized states deep in the gap of a-Si are due to defects in the amorphous network and impurities[22]. The simplest defect is a broken or dangling bond in which one of the two shared atoms in a covalent bond is not available to complete the bonding arrangement shown in Figures 2.1a and 2.1b. Such defects produce states within the gap.

Since the distribution of localized states in a-Si at the band edges tapers off into the bandgap, there does not appear to be a sharp cutoff in the conduction mechanism. However, such a sharp cutoff is observed as indicated by equation (1). The reason that such a cutoff, or distinct ΔE, is observed is due to the difference in mobility of carriers in the localized and extended states. Localized state mobility is much lower than extended state mobility. Thus the observed ΔE actually relates to a mobility gap rather than an energy gap in the density of states.

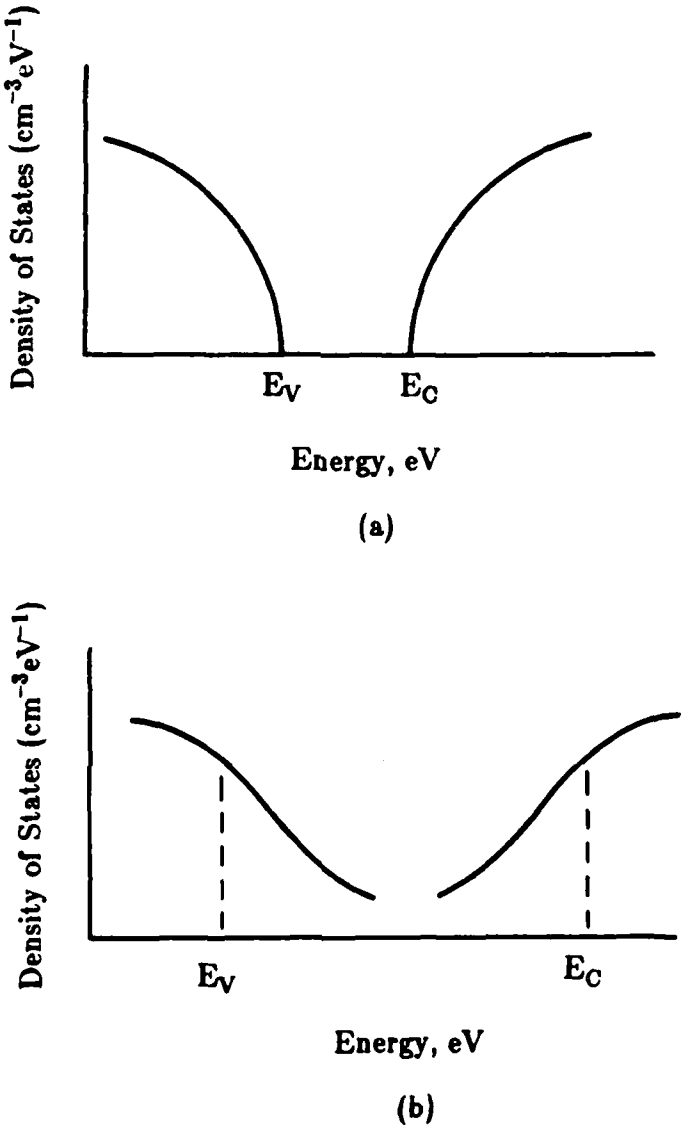


Figure 2.2 General band diagram for (a) single-crystal Si and (b) a-Si.

Various experimental techniques have been used to measure the density of localized states in the mobility gap of amorphous silicon. The earliest pictures of the density of states were obtained by Spear and LeComber[1]. Using the field effect technique, their results indicated a surprisingly low density of states close to midgap and two defect bands - one 0.4 eV below the conduction band and one 0.6eV above the valence band. These two defect bands have become somewhat controversial[23]. Since a transverse electric field is applied to the a-Si through an insulator in this technique, the effect of the insulator/a-Si interface on the measurements is of some concern. In fact, field effect measurements are undoubtedly the most surface sensitive of density of states measurements and hence the least reliable for obtaining a bulk density of states measurement. More details of this technique are given in Section 2.3.1.

Other techniques used to measure the density of states include capacitance-voltage, capacitance-frequency, capacitance-temperature, and deep level transient spectroscopy techniques. Since the results of these techniques do not necessarily support each other, it is indeed difficult to know which technique is the best. Recent reviews of all these techniques and the differences in their results have been given by Cohen[23] and Street and Biegelsen[24].

2.2.2 Density of States and Conduction

In order to develop a good understanding of the basic properties of amorphous silicon, it is essential to have a good theoretical basis on which to build. For this reason, several density of states models have been proposed for use in explaining conduction in a-Si. In these models the extended states exist beyond the mobility gap, while localized states are distributed in band tails within the mobility gap. Differences in the models arise in the expected shape of the band tailing. Not all known models and variations will be presented here, but only those relevant to this research. Others can be found in the literature[25,26].

Much of our understanding of the band structure in amorphous materials is based on the original work by Anderson[27] with refinements by Mott[28]. As indicated by these authors, strong structural disorder within noncrystalline material can lead to spatial fluctuations in potential resulting in the formation of localized states[24]. These localized states, in turn, form band tails above the valence band and below the conduction band penetrating into the mobility gap. The Cohen-Fritzsche-Ovshinsky (CFO) model [29] and Davis-Mott model [30] are further refinements of the models developed by Anderson and Mott.

The CFO model[29] is shown is Figure 2.3a. Notice that the band tail states extend across the gap with little fluctuation in the state distribution. Such a distribution results from conduction and valence band tails overlapping. With such overlap occurring, there will be electrons in the valence band tail states having higher energies than electrons in conduction band tail states. To maintain charge neutrality, these valence band tail state electrons will fall into the lower energy conduction band tail states. When this electron redistribution occurs, the filled states in the conduction band tail will be negatively charged, assuming they are acceptor-type states, while the empty states in the valence band tails will be positively charged, assuming they are donor-type states. Hence, this redistribution insures self-compensation and pins the Fermi level close to the middle of the gap where the density of states is at a minimum[25]. This model has been shown to agree with experimental data for a-Si[9].

The Davis-Mott model[30] is shown in Figure 2.3b. Notice that the band tail states exist only at the very edges of the mobility gap and that another band exists at the middle of the gap arising from material defects. This middle band may be split into donor and acceptor bands which pin the Fermi level at or near mid-gap. Experimental evidence has indicated that this model is a somewhat simplistic view of the state distribution. Instead of a single band of states existing at the gap center due to defects, there can be several localized gap states at well-defined energies in the gap. The position of the Fermi level is then determined by the charge distribution in the gap states. Such a variation to the Davis-Mott model showing bands of donors and acceptors in the upper and lower halves of the mobility gap was introduced by Marshall and Owen[31]. This model seems to be best suited for chalcogenide glasses rather than amorphous semiconductors.

Using the CFO model to explain conduction in a-Si, carrier transport through the material occurs via two channels - extended states and localized states. At elevated temperatures, charge carriers can be excited beyond the mobility edge into the extended states. Current transport in the extended states of a-Si is similar to that occurring in the valence band or in the conduction in single-crystal Si. However, the carrier mobility in the extended states is much lower than in single-crystal Si due to the random amorphous network. For example, recent studies have estimated the extended state electron mobility to be 10 to $20cm^2/V\text{-}sec$[32] or well over $100cm^2/V\text{-}sec$[33] depending on what is chosen for the thermalization depth of electrons within the mobility gap. Both of these are well below that of $1500cm^2/V\text{-}sec$ for electrons in single-crystal Si.

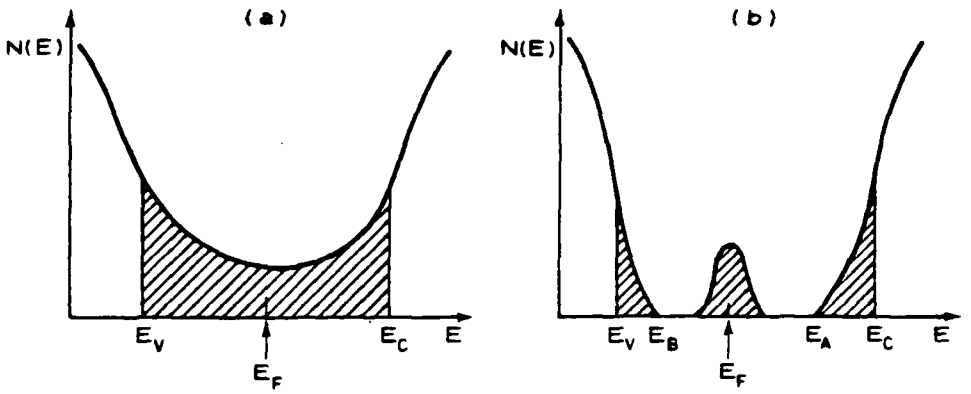


Figure 2.3 Schematic density of states diagrams for amorphous semiconductors: (a) CFO model and (b) Davis-Mott model. From Ref. 25.

At low but finite temperatures, the conduction mechanism is dominated by the low mobility conduction in localized states near the Fermi level. It is generally agreed that electrons in these states have a mobility near $1cm^2/V\text{-}sec$[32,33]. Obviously, the energy distribution of the density of states significantly affects conduction. In this conduction mechanism, carriers jump from localized states to other sites through a phonon assisted tunneling process known as "variable range hopping." This process is similar to impurity band conduction in heavily doped semiconductors at low temperatures. This hopping conduction has been described by Mott[34] and is characterized by the relation

$$\sigma = [\frac{e^2}{2(8\pi)^{1/2}}]\nu_{ph}\left[\frac{N(E_F)}{\alpha kT}\right]^{1/2} e^{-(A/T^{1/4})} \qquad (2)$$

where

$$A = 2.1\left[\frac{\alpha^3}{kN(E_F)}\right]^{1/4}, \qquad (3)$$

ν_{ph} is the phonon frequency in Hz, α is the rate of wave function fall-off at a site, $N(E_F)$ is the density of states at the Fermi level in $\#/cm^3\text{-}eV$ and "e" is the charge on an electron in Coulombs. This relation has been verified experimentally[34].

Conductivity in hydrogenated a-Si is affected by light. Staebler and Wronski[35] first reported that long exposure to light decreases the photoconductivity and dark conductivity of a-Si:H. They found that annealing above 150 ° C reverses the process. This effect, which now bears their names, is attributed to changes in the density or occupation of low mobility gap states. Such conductivity changes are not observed in unhydrogenated a-Si prepared by evaporation or sputtering techniques.

2.2.3 Hydrogen in a-Si

Hydrogen plays a very significant role in the observed properties of amorphous silicon[36]. It primarily acts as a dangling bond terminator to reduce material defects, thereby decreasing the number of localized states in the mobility gap. With fewer states in the gap, a-Si more closely approaches the band structure of single-crystal Si enabling greater application of this material in semiconductor-type devices. However, care must be taken in the processing

of device quality hydrogenated a-Si not to allow the temperature to exceed 300 ° C where the hydrogen tends to effuse out of a-Si[37]. The proper designation for the hydrogenated a-Si alloy is "a-Si:H" and is the form of a-Si used in this research.

Initially, the role of hydrogen in a-Si was not recognized[38]. The first study on glow discharge a-Si, which is now known to contain a significant amount of hydrogen, made in 1969 made no mention of hydrogen[39]. Instead, mention was made only of the drastically different properties of this material as compared to evaporated and sputtered a-Si. The existence of hydrogen in a-Si did not become apparent until 1975 when glow discharge a-Si was shown to contain hydrogen[40]. However, the presence of hydrogen and its ability to eliminate dangling bonds in glow discharge a-Ge was recognized in 1974[41]. Today glow discharge produced a-Si is known to have a hydrogen content of 10 to 50at.% and most of the hydrogen is bonded to Si atoms[42].

Direct evidence that hydrogen neutralizes dangling bonds is seen by the disappearance of the electron spin resonance (ESR) signal in hydrogenated a-Si as compared to pure a-Si. The ESR signal originates from unpaired electron spins which are produced by dangling bonds. Thus, those materials with weaker ESR signals have fewer unpaired spins, or dangling bonds, than those with stronger signals. Luminescence studies have also been conducted to demonstrate the role of hydrogen as a defect-reducer[43].

The way that hydrogen is incorporated into a-Si:H also affects the observed properties[44,45]. Several studies have been conducted to identify the bonding configurations[46,47,48,49]. Much of this work is based on infrared absorption and Raman scattering of a-Si containing substantial amounts of bonded hydrogen. The material is described as a Si-H alloy where there are multiple, as well as single, H-atom attachment. Figure 2.4 shows the atomic motions of the vibrational modes used to investigate the a-Si:H structure.

Flourine has also been found to be an effective dangling bond terminator in amorphous silicon. In fact, it has been shown that glow discharge a-Si:F:H has characteristics superior to a-Si:H (i.e., better doping efficiency and lower density of states in the mobility gap)[50,51,52]. In addition, a-Si:F is more heat resistant than a-Si:H. In particular, the flourine content and temperature dependence of the conductivity are left unchanged when a-Si:F is annealed to 600 ° C[53].

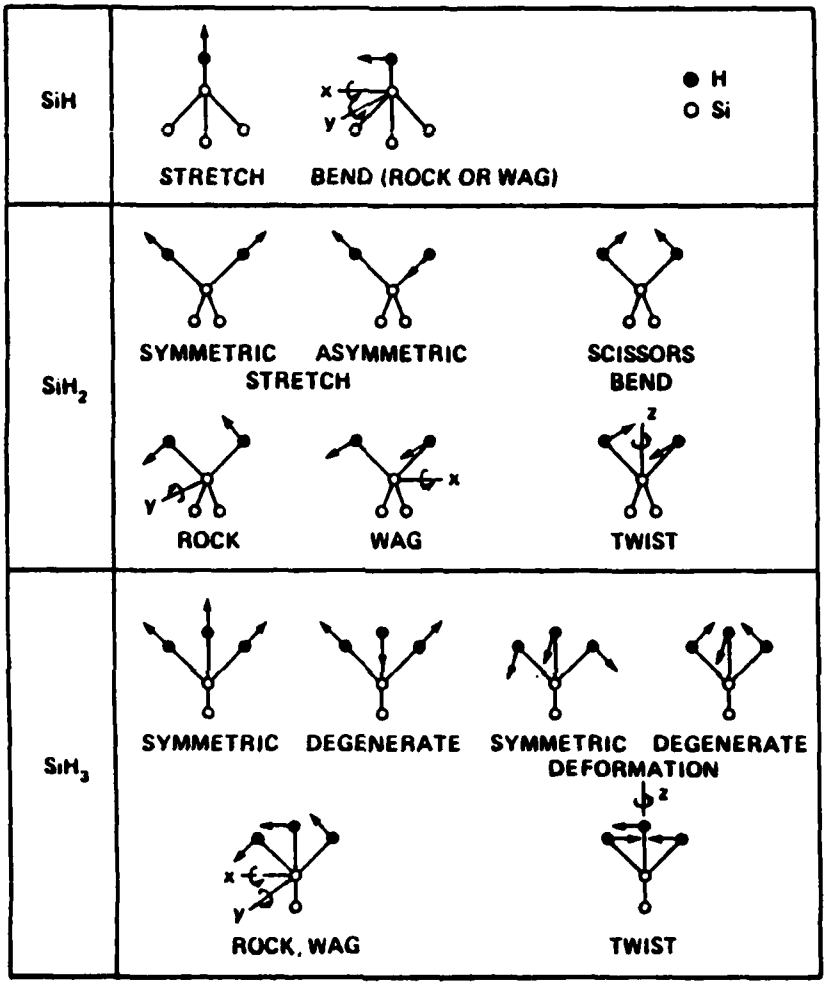


Figure 2.4 Atomic displacement of H atoms in local and resonance mode vibrations in (a) SiH groups, (b) SiH_2 groups, and (c) SiH_3 groups. From Ref. 44.

2.2.4 Preparation of a-Si:H Films

Amorphous silicon films have been prepared by a number of techniques. In particular, films have been prepared by vacuum evaporation[54,55], ion implanting into single-crystal Si[56], sputtering[57,58], chemical vapor deposition (CVD)[59,60] and glow discharge techniques[39,61]. With the realization that hydrogen incorporation in a-Si results in a higher quality semiconducting film, the emphasis in material preparation has shifted to those techniques which make the film more hydrogen-rich. The three most practiced preparation techniques being used today are glow discharge, sputtering, and thermally-enhanced CVD. While the glow discharge technique is inherently hydrogen-rich because of the dissociated silane gas containing hydrogen ions, the sputtering and CVD techniques are not as hydrogen rich. To incorporate hydrogen, sputtering can be accomplished in a hydrogen-rich environment or the sputtered a-Si can be post-hydrogenated. Similarly, the CVD material must be post-hydrogenated because of its inherently high temperature processing ($\simeq$600 $^{\circ}$ C) which tends to evolve any hydrogen incorporated during this thermal decomposition process. However, work is underway to delete this need for post-hydrogenation process in CVD films[60,62,63,64]. Post-hydrogenation of the sputtered and CVD materials can be accomplished with a hydrogen glow discharge plasma[65] or by hydrogen ion implantation[66]. Since the research described in this thesis is concerned with a-Si:H prepared by the glow discharge technique, the rest of this section will address only the glow discharge material. Several recent reviews describe the details of the sputtering and CVD techniques, as well as the glow discharge technique[15,16].

Glow Discharge a-Si

The glow discharge process is actually a plasma-enhanced CVD technique. The first recorded use of this technique to deposit a-Si was in 1969[39]. Since then much work has been done to investigate and optimize the deposition-dependent semiconducting properties of glow discharge a-Si. The electrical glow discharge for this process is generated by flowing silane gas into a low power RF field under a low pressure (0.1 - 1.0T)[67]. As the gas passes into the RF field, energy from the field accelerates only the few free electrons present in the gas. Any ions present are relatively unaffected due to their much heavier mass. After acquiring sufficient energy, the free electrons collide with the gas species producing excitations and ionizations. Electrons resulting from these ionizations are in turn accelerated by the RF field quickly avalanching into a glow discharge. The discharge is maintained by a loss of electrons and ions to

electrodes and other surfaces within the chamber and a gain of an equal number of electrons from ionizations and other electron-producing processes. The inelastic collisions occurring within the discharge between electrons and gas molecules give rise to reactive species, such as excited neutrals and free radicals, as well as the ions and electrons. Through these collisions then, the energy of the electrons acquired from the RF field is used to create the reactive species needed to deposit the a-Si:H.

Deposition conditions significantly influence the quality of a-Si:H films deposited using the glow discharge process[68]. In particular, RF power level and coupling technique, substrate temperature, pressure, silane concentration and flow rate, and electrode spacing all have some bearing on the quality of the deposited films. Depending on the particular desired a-S:H film application, deposition conditions must be carefully characterized and optimized for each type of reaction chamber used[69]. In addition, deposition conditions are known to affect insulator/a-Si:H interface states[70]. In general, those films deposited at slower deposition rates, and hence lower RF power levels, have preferable qualities for semiconductor applications, i.e., low density of states in the mobility gap. However, such is not always the case as alternate RF source excitations[71] and gases other than SiH_4[72,73] have been used to speed up the deposition process. Table 2.1 shows a typical range of deposition parameters. As indicated previously, care must be taken not to allow the substrate temperature to exceed 300 ° C during deposition as hydrogen effuses from a-Si:H at these temperatures. Also, undoped a-Si:H crystallizes near 620 ° C[74]. Thus high temperatures must be avoided on all a-Si:H processing if the film is to remain amorphous and hydrogen-rich. More will be said on selecting the optimum deposition conditions in Section 3.4.5 when the optimization of the deposition conditions used in this research is discussed.

2.2.5 Substitutional Doping of a-Si

During the early stages of amorphous silicon development, it was generally believed that this material could not be doped by the introduction of impurities[75]. It was argued that all bonds of a trivalent or pentavalent impurity atom introduced into a random a-Si network would be satisfied. Thus, no donor or acceptor action would be possible. Fortunately, Spear and LeComber[75] and Carlson and Wronski[76] did not accept this premise. Both groups independently demonstrated n- and p-type doping of a-Si:H using gaseous dopants during film deposition.

Table 2.1 Range of discharge parameters for a-Si:H deposition. From Ref. 69.

Parameter	Range
SiH_4 concentration	10-100% in H_2 or Ar
Total gas flow rate	20-200 sccm
Total pressure	0.05-2.0 Torr
RF power	1-100 W
Substrate temperature	200-300 °C

The success of the doping was attributed to the very low overall density of gap states in a-Si:H compared to the higher number of states found in evaporated or sputtered films[2]. In particular, in evaporated or sputtered a-Si with a large density of states, 10^{19} to $10^{20}cm^3$–eV, the introduction of impurities could not move the Fermi level more than a few kT (1kT = 0.026eV). However in a-Si:H with a considerably lower density of states, $10^{17}cm^3$–eV, the introduction of impurities could move the Fermi level several tenths of an eV. For example, Spear and LeComber[2] found that with the introduction of phosphine gas into the glow discharge, the Fermi level shifted from 0.6eV to 0.19eV below the conduction band. Similar results were obtained with the addition of diborane gas to the discharge. The result of these Fermi level shifts was a ten orders of magnitude change in the room temperature conductivity, i.e., from 10^{-12} mhos/cm to 10^{-2} mhos/cm. In addition, other studies have shown that the Fermi level cannot be moved into the conduction band at high doping levels, so that the doping saturates and degenerate conduction does not occur[77].

With the success of doping a-Si:H from a gaseous source, the possibility existed of doping it by ion implantation, a technique used widely in the semiconductor industry. Muller et al[78] demonstrated that n- and p-type doping could be accomplished with ion implantation, but more dopant was required to achieve the same relative conductivity as in gaseous doping. In other words, gaseous doping was more efficient. It was also found that the most effective implants were those done at substrate temperatures approaching the a-Si:H substrate deposition temperature. By heating the substrate during implantation, the inherent damage of the implant was annealed out as the implant progressed. The heated implant then resulted in less overall damage to the a-Si:H than implanting at room temperature and annealing afterwards to activate the implant.

2.2.6 Contacts to a-Si:H

In order to obtain good experimental data from structures fabricated with a-Si films, consideration must be given to the scheme used for making electrical connection to the film. Should this scheme be too resistive, misleading information about the film properties and/or device performance can be obtained. In particular, if the contact resistance is too high, the film and/or device performance can be obscured or masked entirely by the contact resistance.

Since all metals form reasonable Schottky barriers on a-Si:H[79], a special challenge exists in making ohmic, or even quasi-ohmic, contacts to a-Si:H. It has long been recognized that ohmic contacts to a-Si:H cannot be achieved by simply evaporating a low work function metal onto the a-Si:H surface[80] or vice versa[5]. Techniques similar to those used in crystalline semiconductors are needed to form ohmic contacts on a-Si:H. Two such techniques include annealing and doping the a-Si:H film in the vicinity of the metal/a-Si:H interface.

Several investigations have been performed to investigate the effects of annealing and doping on the metal/a-Si:H contact performance[81,82,83,84]. These investigations have shown that Al and Au readily interdiffuse with undoped and doped a-Si:H at temperatures below 200 °C, while Cr, Ni, NiCr, Pd, and Pt do not. This interdiffusion has the tendency to degrade the contact performance by the formation of single-crystal Si islands which apparently do not become part of the current path[85]. However, the contact performance can be improved by annealing if a metal silicide happens to form along with the interdiffusion. When the interdiffusion does not accompany the annealing operation, the contact performance is not usually degraded and can even be improved[81].

The effect of contact performance on device operation has been shown in several a-Si:H TFT investigations[86,87]. Devices were fabricated with and without doped source/drain contact regions. Those devices with the doped contact regions yielded significantly higher current levels than those without the doped contact regions. In fact, the highest current levels achieved to date in a-Si:H TFTs have been with doped source/drain contact regions[3].

2.3 Amorphous Silicon Thin Film Transistors

2.3.1 Introduction

During the early investigations into the electrical properties of a-Si:H, Spear and LeComber[1] used the field effect technique to measure the energy dependence of the density of localized states in the mobility gap. Since then many others have used the basic concepts of this technique to profile the density of states[54,88,89].

In the field effect technique, a structure similar to that shown in Figure 2.5 is used. Notice that the semiconducting film is essentially one electrode of a parallel-plate capacitor[90]. When a potential is applied to the gate, the capacitor becomes charged and an accumulation layer of electrons or holes is

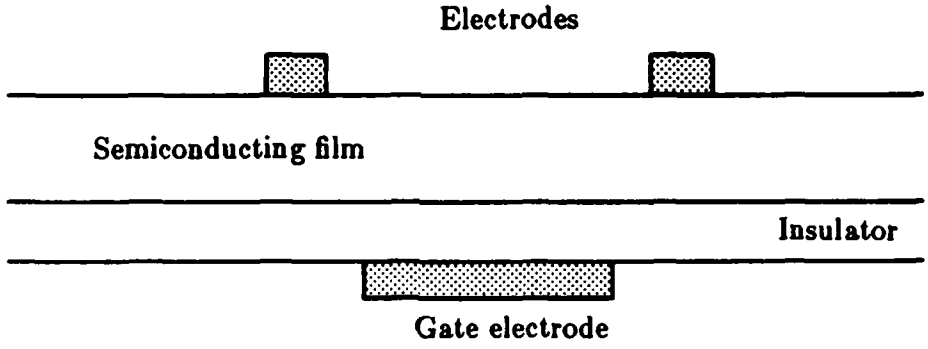


Figure 2.5 Field effect measurement test structure or thin film transistor.

formed in the film adjacent to the capacitor insulator. A potential distribution then exists in the accumulation layer causing a shift in the occupancy of the electronic states at the insulator/film interface. It is this distribution in the potential that determines the conductance in the film between the two electrodes attached to the film. As the gate potential is changed, the conductance is modulated according to the change in potential distribution. An analysis of the conductance as a function of the applied potential using Poisson's equation then yields the density of states distribution.

In examining the structure shown in Figure 2.5, it is essentially that of a thin film transistor (TFT) described widely in the literature[91,92,93]. Although the TFT can be made with various semiconducting films (e.g., CdSe or CdS), its general output performance characteristics remain similar. It seems reasonable then that after the field effect structure was used to demonstrate the semiconducting properties of a-Si, that its TFT characteristics should also be examined. This subsequent TFT investigation is in fact what happened at several laboratories[1,10,54,88,94,95].

The basic operation of an n-channel a-Si TFTs is shown in Figure 2.6. With no gate (V_G) or drain voltage (V_D) applied, no conduction occurs through the device (Figure 2.6a). Upon application of a positive V_G to the ideal device, an accumulation layer of electrons forms at the insulator/a-Si interface underneath the gate electrode (Figure 2.6b). When V_G is large enough, the accumulation layer serves as a low resistance channel for current flow between the source and drain. Hence, when a drain voltage is applied, current flows from source to drain through a low resistance channel region and through a high resistance bulk region.

As V_D is increased, current through the device increases until the change in potential across the drain end of the device reduces the number of enhanced electrons at the drain end to a negligible amount or zero (Figure 2.6c). This point is called the "pinch-off" point, beyond which only small changes in current result from additional increases in drain voltage.

As V_D is increased beyond the voltage at which pinch-off occurs (V_P), the electron current in the enhanced channel increases slightly because V_P is mildly dependent on V_D. While this electron current is increasing, the drain end of the enhanced channel is being depleted of electrons causing the enhanced electron channel to shrink towards the source (Figure 2.6d). Since the increase in V_D beyond V_P is applied between the drain and the end of the enhanced channel, the potential across the shrinking enhanced channel stays about the same, permitting the current to rise only slightly as V_D increases. In addition,

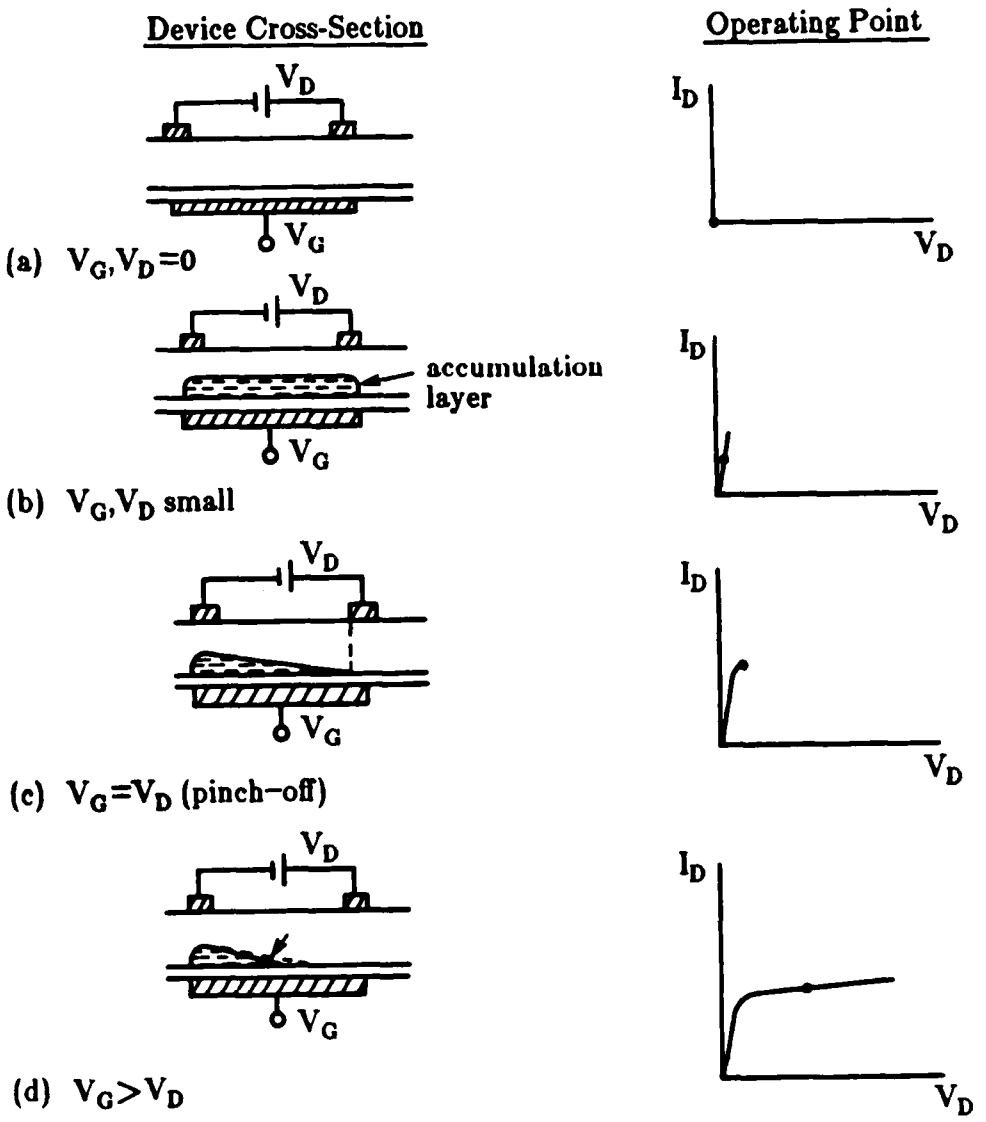


Figure 2.6 a-Si TFT operation: (a) no applied bias, (b) below pinch-off, (c) pinch-off, and (d) beyond pinch-off. (V_G is the effective gate voltage, V_D is the applied bias).

the parallel current component through the bulk region of the device continues to increase slightly as V_D is increased.

The greater the number of interface states at the insulator/a-Si interface and/or the density of states in the mobility gap, the higher the gate voltage required to form a channel in the TFT. Ideally with a small V_D applied, a channel should be formed for small values of V_G. However if significant charge exists at the interface, a greater amount of V_G will be necessary to enhance conduction. Thus, during the fabrication of a-Si TFTs, consideration must be given to reducing interface states and localized states in the mobility gap to enhance device performance.

2.3.2 Modeling of a-Si TFTs

After demonstrating the TFT properties of the field effect structure, it was desirable to theoretically analyze the device so that it could be better understood and improved. Because of the large density of localized states in the mobility gap, an analytical expression for the output drain current vs drain voltage characteristics is not easily obtained. Neudeck and Malhotra[95] published one of the first analyses with experimental verification of a-Si TFT output drain characteristics. They derived a simple expression that agreed with their more detailed theory based on calculating the energy band bending and the resulting source-drain conductance. Suzuki et al[10] analyzed the influence of localized state distribution on the basic characteristics of a-Si:H TFTs. Their results showed that the slope of the density of states distribution near and above the Fermi level is a key factor in determining the on/off current ratio in a-Si:H TFTs. They concluded that in order to get higher on/off current ratios for switching, the Fermi level should be positioned in the middle of the mobility gap, the density of states near the conduction band edge should be small, the gate insulator should be thin and the dielectric constant of the insulator should be large. The analysis performed by Shur and Hack[12] demonstrated the importance of the density and distribution of deep and tail localized states on device performance. Their theory predicted how device characteristics scale with gate length, insulator thickness, channel doping, temperature and material properties. Lee and Chen[11] calculated the field effect conductance of a-Si:H TFTs taking into account the space charge due to excess free carriers and the charge in the surface states. The effect of the surface state charge was found to be additive to that of the bulk localized state charge, and thus it was difficult to distinguish between the two.

All of the above modeling efforts obtained useful results, but in different respects. In particular, either a suitable analytical formula to calculate the drain characteristics in all regions of operation was not obtained or computer simulation techniques were necessary to obtain a solution. Recently however, Neudeck et al[96] developed a simplified model based on the experimental function for the channel conductance vs gate voltage. Four constants obtained from the experimental data of drain current (I_D) vs gate voltage (V_G) at a small drain voltage (V_D) completely specify the model. In addition, these constants can be derived from basic theory taking into account the surface state charge, fixed charge at the insulator/a-Si interface, and device geometry. Such a model is useful in circuit calculations and in computer aided design programs.

The experimental function, or transfer curve, is shown in Figure 2.7. To obtain an expression for I_D for this function, the relation developed by Tickle[93] was used:

$$I_D = \frac{W}{L} \int_{V_G - V_D}^{V_D} G_s(V)\, dV \tag{4}$$

where V is the potential across the insulator, $G_s(V)$ is the channel sheet conductance, W is the device width, and L is the device length. If V_D is small, $G_s(V)$ can be approximated by:

$$G_s(V) = b\,[e^{aV} + c] \tag{5}$$

where "a" is a function of the slope of the straight-line portion of the ln I_d vs V_G curve, "b" is an arbitrary constant that depends on carrier mobility, temperature and device geometry, and "c" is related to the density of states in the mobility gap and device geometry. As the localized states near the Fermi level decrease, "a" becomes larger and "c" becomes smaller. Including flat-band voltage (V_{FB}) in the above expression for $G_s(V)$ in equation (4), I_D becomes

$$I_D = \frac{Wb}{L} \int_{V_G - V_{FB} - V_D}^{V_G - V_{FB}} \left(e^{aV} + c \right) dV \tag{6}$$

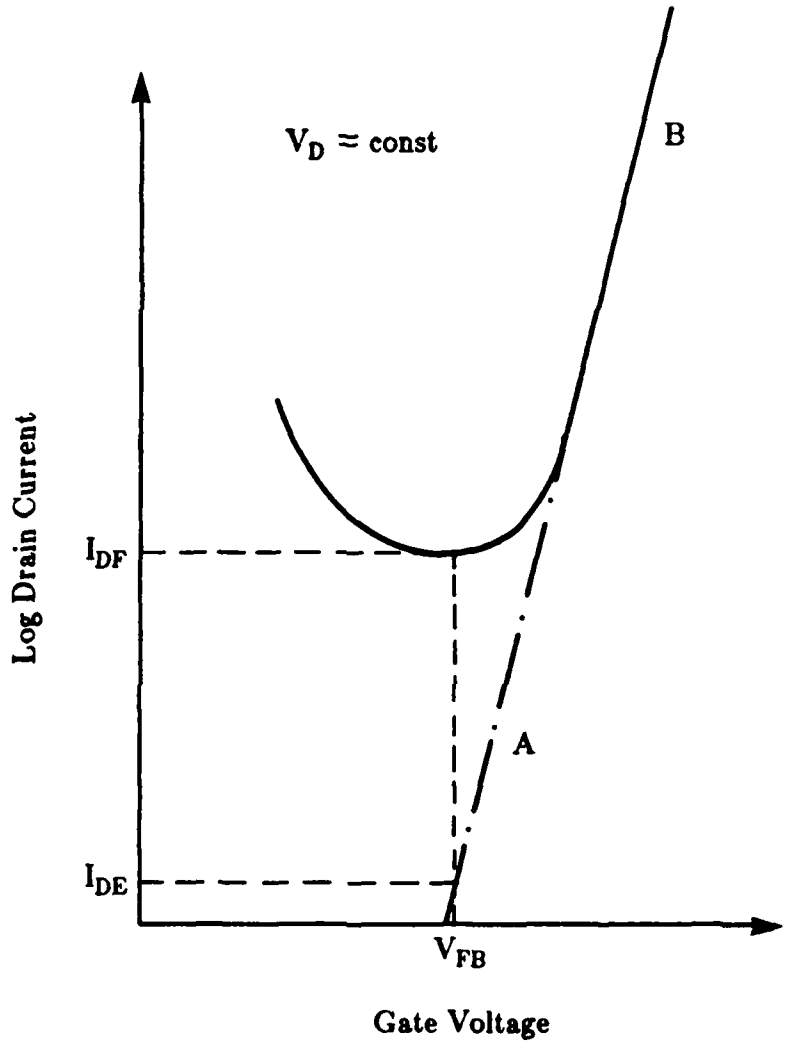


Figure 2.7 Typical experimental transfer curve for a small fixed V_D.

Equation (6) can be used to describe device performance in all regions of operation. For example, when $V_G > V_{FB}$ and $V_G - V_{FB} > V_D$, equation (6) becomes

$$I_D = B\left\{acV_D + e^{a(V_G-V_{FB})}\left[1-e^{-aV_D}\right]\right\} \tag{7}$$

The constants "a," "B," "c" and V_{FB} can be determined from the experimental transfer curve as illustrated in Figure 2.7 where V_D is a small constant value. In particular, "a" is determined from the slope of the AB portion of the curve. "B" is determined from the relation

$$B = \frac{I_{DE}}{aV_D} \tag{8}$$

and "c" from the relation

$$c = \frac{I_{DF}}{BaV_D} = \frac{I_{DF}}{I_{DE}} \tag{9}$$

V_{FB} is obtained by finding the gate voltage corresponding to the minimum I_D.

The drain current expression derived from basic theory in Reference 96 demonstrates the theoretical basis for the "a," "B" and "c" constants. Figure 2.8 illustrates the basic definitions for the a-Si TFT channel configuration used in the derivation. This derivation proceeds from the expression of the potential drop, V_o,across the channel element, dy, for:

$$dV_o(y) = I_D dR \tag{10}$$

where x is the direction perpendicular to current flow y. The expression developed for the differential resistance, dR, which is composed of both the flat-band and enhanced channel resistance resulting from band bending, assumes extended state conduction, Maxwell-Boltzman statistics and that the mobilities are independent of electric field. Using this expression for dR, the resulting current expression is

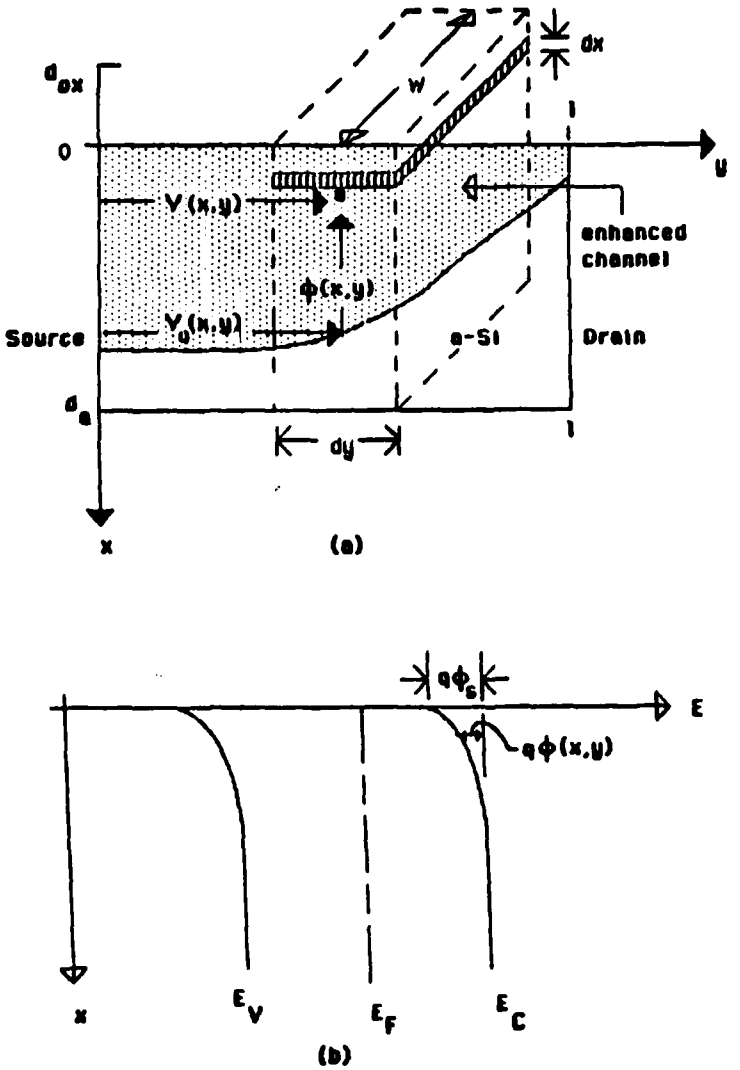


Figure 2.8 Diagrams for a-Si TFT analysis: (a) geometric definition diagram and (b) energy band diagram.

$$I_D = \frac{W}{L}\left[\sigma_T d_a V_D - \sigma_{no}\int_0^{V_D\phi_s}\int_0^{} \frac{e^{q\phi/kT}-1}{\partial\phi/\partial x}\, d\phi dV_o\right.$$

$$\left. - \sigma_{po}\int_0^{V_D\phi_s}\int_0^{} \frac{e^{q\phi/kT}-1}{\partial\phi/\partial x}\, d\phi dV_o\right] \qquad (11)$$

where the total extended state conductance, σ_T, equals the sum of the electron, σ_{no}, and hole, σ_{po}, extended state conductances, respectively. Also, d_a is the a-Si film thickness and $\phi(x,y)$ represents the amount of band bending in the channel.

To find an expression for $\phi(x,y)$, Poisson's equation is used:

$$I_D = \nabla^2\phi(x,y) = \frac{\partial^2\phi(x,y)}{\partial x^2} = -\frac{\rho(x,y)}{\epsilon_o K_s} \qquad (12)$$

where ϵ_o is the permittivity of free space and K_s is the dielectric constant of a-Si.

To obtain closed form solutions for the desired constants, certain assumptions must be made at the this point. For example, localized state density is much greater than the enhanced free carrier density in vacuum evaporated and hydrogen implanted a-Si so that the free carrier term in $\rho(x,y)$ is ignored. Also, for uniform localized state density distribution and a symmetric Fermi function, $\rho(x,y)$ is related to the localized state density distribution, N_t, by

$$\rho(x,y) = -q^2 N_t \phi(x,y) \qquad (13)$$

Solving Poisson's equation yields

$$\frac{\partial\phi}{\partial x} = -M\phi \qquad (14)$$

where

$$M = \left\{ \frac{N_t q^2}{\epsilon_o K_s} \right\}^{1/2} \tag{15}$$

Equation (14) can now be solved for $\phi(x,y)$ and the result substituted into equation (11) yielding

$$I_D = \frac{W}{L} \left[\sigma_T d_s V_D + \sigma_{no} \int_0^{V_D \phi_s} \int_0^{} \frac{e^{q\phi/kT} - 1}{M\phi} \, d\phi dV_o \right.$$

$$\left. + \sigma_{po} \int_0^{V_D \phi_s} \int_0^{} \frac{e^{q\phi/kT} - 1}{M\phi} \, d\phi dV_o \right] \tag{16}$$

where ϕ_s is the surface band bending.

If this surface band bending varies linearly in y, it is related to the applied gate voltage by

$$V_G = V_{FB} + V_i(y) + \phi_s(y) + V_o(y) \tag{17}$$

where $V_i(y)$ is the voltage drop across the insulator. To obtain a solution, it is necessary to solve for $\phi_s(y)$ in terms of gate voltage by eliminating $V_i(y)$. When this is done, $\phi_s(y)$ can be expressed as

$$\phi_s(y) = [K_{ox}/K_n][\, V_G - V_{FB} - V_o(y) \,] \tag{18}$$

where

$$K_n = K_{ox} + K_s d_{ox} \left[M + \frac{q^2 N_s}{\epsilon_o K_s} \right] \tag{19}$$

and K_{ox} is the dielectric constant of the insulator, d_{ox} is the insulator thickness and N_s is the density of surface states. Note that M increases with N_t while K_n increases with N_s.

In order to obtain a closed form solution, the integrals of equation (16) must be simplified. When this is done the drain current can be expressed as

$$I_D = \frac{W}{L}\left[\left(\sigma_{no} d_a + \frac{\sigma_{no} kTS_1}{M}\right) V_D\right.$$

$$\left. + \frac{\sigma_{no} k^2 T^2 K_n S_1}{MqK_{ox}} e^{\frac{qK_{ox}(V_G - V_{FB})}{kTK_n}} \left(1 - e^{\frac{qK_{ox} V_D}{kTK_n}}\right)\right] \tag{20}$$

where $\sigma_T \simeq \sigma_{no}$ and $\sigma_{no} >> \sigma_{po}$.

Comparing equation (7) with equation (20) allows the coefficients "a," "B" and "c" to be determined as follows:

$$a = \frac{qK_{ox}}{kTK_n} \tag{21}$$

$$B = \frac{W\sigma_T}{L} \frac{kTS_1}{Ma} \tag{22}$$

$$c = \frac{Md_a}{kTS_1} - 1 \tag{23}$$

where

$$S_1 = \frac{1}{kT} \frac{\sum_{n=1}^{\infty} \frac{(q\phi_s/kT)^n}{nn!}}{e^{q\phi_s/kT} - 1} \tag{24}$$

By referring to equations (15) and (19), equation (21) shows that the slope of the experimentally determined transfer curve decreases when N_t and/or N_s increases, as expected. They also show how the G_s function is related to localized states, surface states, and device geometries.

2.3.3 Ambipolar a-Si TFTs

Ambipolar TFTs are capable of both n- and p-channel device operation. Essential to the fabrication of ambipolar a-Si TFTs is the formation of ohmic source and drain contact regions and the use of a high quality gate insulator. Without the formation of ohmic contacts, the flow of electrons and/or holes through these regions can be severly diminished and even blocked. Thus, such devices will be incapable of both n- and p-channel operation.

In addition, the use of a high-quality gate insulator is required in a-Si TFTs in order to observe the ambipolar behavior at reasonable voltage levels. To date the ambipolar behavior has been observed only in devices containing thermally grown[97] SiO_2 and quartz[89] insulators. Both n- and p-channel operation for the same device using a silicon nitride insulator has not been reported. This is due to the inherent fixed positive charge in the SiN_x insulator which hinders the formation of a p-channel device as the gate voltage is biased negatively. At large enough negative gate voltages the p-channel device might be observed.

Evidence of the ambipolar behavior of a-Si TFTs was observed by Neudeck and Malhotra in 1975[54]. However, a formal investigation of this property was not done until 1985 when Pfleiderer et al applied a general ambipolar field-effect transistor (FET) theory to a-Si:H TFTs[98]. This widely publicized theory[99,100,101], based on a modification to the Pao-Sah description of a unipolar FET, is quite thorough and seems to explain the transition between electron and hole regimes very well. However, some limitations appear to exist in its ability to consistently predict output drain characteristics over many decades of drain current.

2.3.4 a-Si TFT Applications

As indicated previously, much work has been done to investigate and demonstrate the applicability of a-Si TFTs as viable electronic devices. To better describe this applicability, the role of this device in large area display arrays, integrated circuits, image sensors and radiation hardened circuits will be presented.

Perhaps the most widely used application of the a-Si:H TFT is in large area display arrays. This application has been successfully demonstrated in many laboratories[5,102,103] and is used to manufacture a commercial product[104]. The a-Si:H material is well-suited for these arrays because it can be easily deposited over large areas, has a high resistivity (a requirement for

low leakage current) and has a low mobility (a disadvantage for high frequency operation, but desired for high resolution displays)[5]. The desired low mobility for high resolution displays stems from the minimum device size causing a lower off-resistance with lower mobility materials than it does with higher mobility materials, thereby permitting the required low off-currents needed for successful display operation.

As a specific example of a-Si TFTs being used in large area arrays, consider the example shown in Figure 2.9 where the TFTs are used to drive a liquid crystal display (LCD) array[105]. Such arrays typically require a 3 - 6V ac drive signal without any dc component which tends to degrade the material. The TFT responds to the rms value of the ac signal having a threshold of 1 - 2V.

One TFT is needed to control each LCD element in the array. The TFTs are interconnected by X and Y drive buses, (i.e., G_1, G_2, ... gate lines and S_1, S_2, ... source lines). The drain contact for each TFT is connected to the indium-tin-oxide (ITO) electrodes, D. The transient behavior of the TFT in the matrix is determined by the capacitive loading of the liquid crystal element. Panels containing 20 X 25 elements have been built and successfully run at 80Hz for 15 months, (i.e., $6X10^{19}$ operations) with no evidence of deterioration in the device transfer characteristics.

Another application for a-Si:H TFTs is in integrated circuits, especially those used to drive the TFTs of an LCD array. Although their inverter circuits were somewhat leaky and had slow turn-on, Matsumura and Hayama[4] were the first to demonstrate the use of a-Si:H TFTs in integrated form. Their initial work was followed by demonstrations of other inverter circuits and other logic functions using a-Si:H TFTs which operated at 500Hz[106]. It is especially attractive that all of these circuits could be operated below 15V making them compatible with modern integrated circuit voltage levels. Figure 2.10 shows examples of the early inverter circuits.

a-Si:H TFTs have also been integrated in three-dimensional form. Nara et al[107] have demonstrated inverters and nine-stage ring oscillators. The basic inverter circuit consists of an n-channel driver and a p-channel load as found in many single-crystal Si integrated circuit applications. The inverters have step-like transfer characteristics and a small-signal gain of about 10, while the ring oscillators have a 60μsec propagation delay per gate or 16.7MHz operation.

Another application of a-Si:H TFTs is in addressable image sensors which use the high photoconductivity and high dark resistivity of a-Si:H. This application has been demonstrated by both Matsumura et al[108] and Snell et

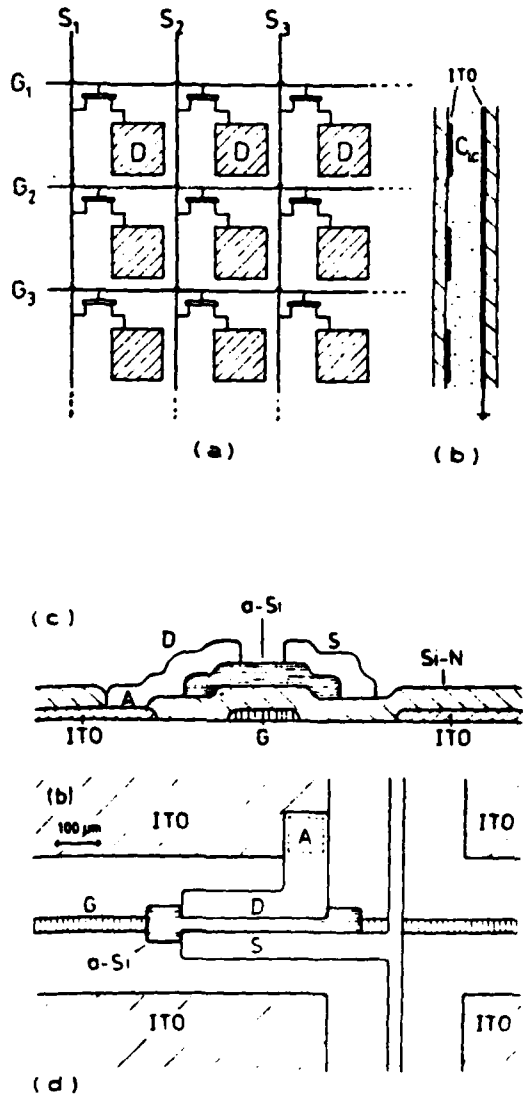


Figure 2.9 Example of a-Si:H TFTs in LCD array: (a) schematic layout of an addressable TFT array, (b) cross-section of liquid crystal elements with capacitance C_{LC}, (c) cross-section of the a-Si:H TFT, and (d) layout of the a-Si:H TFT. From Ref. 105.

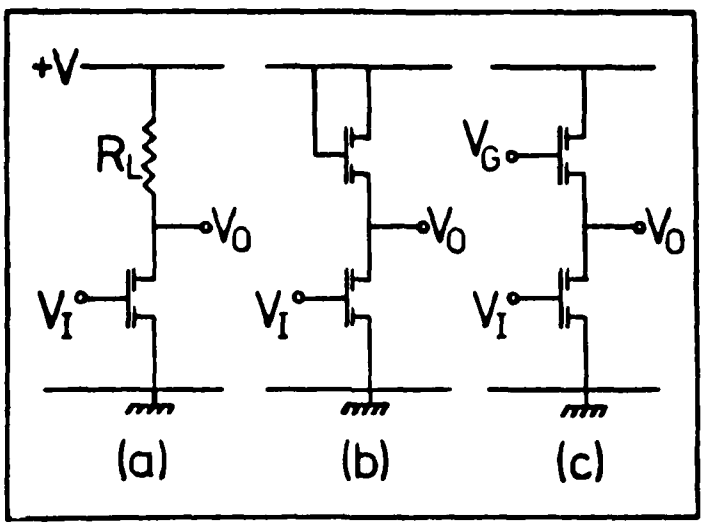


Figure 2.10 Three examples of a-Si:H TFT inverter circuits: (a) and (b) from Ref. 106, and (c) from Ref. 4.

al[106]. A schematic circuit diagram and unit cell structure from Matsumara et al's work are shown in Figure 2.11. Notice that the device consists of a photoconductor, capacitor and field effect transistor (or TFT). When light is incident on the photoconductor, the capacitor is charged up. Upon application of a clock pulse, the TFT output current which is proportional to the incident photon flux on the photoconductor can be read. Recently, Snell et al[109] have dispensed with the capacitor and developed a new vertically integrated image sensing element consisting of the TFT fabricated on top of the a-Si photoconductor. Evaluation of these devices have indicated that less than 25ms would be required to read information from 1000 of these elements. Such performance corresponds to 40Hz operation.

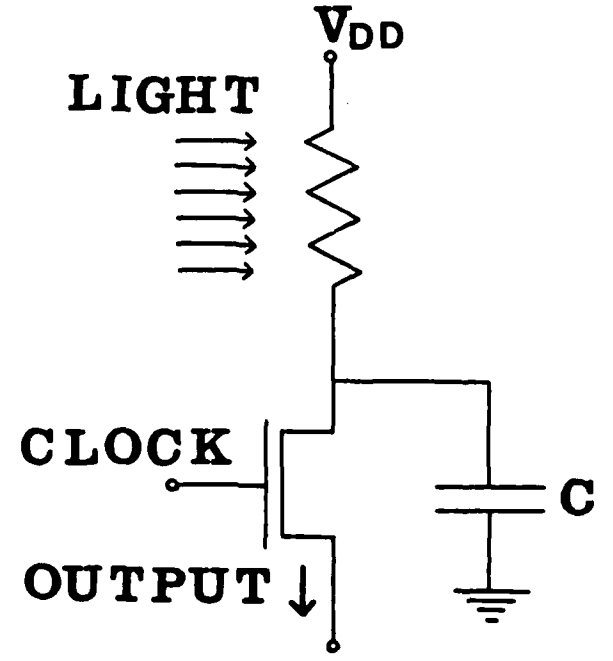
A proposed application of a-Si:H TFTs is in radiation hardened circuits. French et al[110] investigated the susceptibility of unpassivated a-Si:H TFTs with a 3000Å silicon nitride insulator. This investigation showed that the threshold voltage of these devices changed less than 3V while the transconductance changed less than 10% when irradiated with Co^{60} γ-ray doses of up to 5Mrad(Si). The changes were observed to be reversible by annealing the devices at 130 °C. Such shifts are indeed comparable to single-crystal Si field effect devices made with much thinner silicon dioxide insulator[111]. Thus, it seems that a-Si:H TFTs are remarkably resistant to γ-radiation and should be considered for radiation hardened applications.

From the applications described above, a-Si:H TFTs are indeed feasible devices in a number of practical circuits. Their use as switching devices in LCD arrays has been well demonstrated. However, their use in logic circuits and other applications appears to be somewhat limited by frequency response[87]. This response is limited by the time required for the device on-current to charge up circuit capacitances. The charging time can be improved by optimizing device geometry (i.e., reducing the source to drain spacing) and/or optimizing device on-conductance by reducing the density of interface states at the insulator/a-Si interface and the density of localized states in the mobility gap.

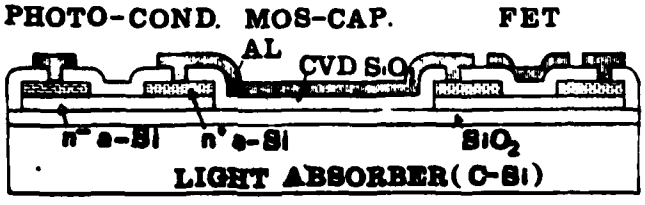
In general, the high frequency performance of a TFT can be characterized by the gain-bandwidth product or "figure of merit," f_m, given by[93,112]

$$f_m = \frac{g_m}{2\pi CWL} \tag{25}$$

In this relation, g_m is the transconductance, C is the gate capacitance, W is the



(a)



(b)

Figure 2.11 a-Si image sensor: (a) circuit diagram and (b) unit cell cross-section. From Ref. 108.

gate width and L is gate length. Since g_m can be expressed as

$$g_m = \frac{CW\mu}{L}(V_G) \tag{26}$$

where μ is the effective field-effect mobility and V_G is the effective gate voltage, f_m becomes

$$f_m = \frac{\mu V_G}{2\pi L^2} \tag{27}$$

If $\mu = 0.3cm^2/V\text{-sec}$, $V_G = 15V$ and $L = 4\mu m$, a value of $f_m = 5Mz$ is obtained. Since there are many applications where this maximum operating frequency can be well tolerated, it is highly probable that a-Si:H TFT development will continue and demonstrate MHz range applications.

2.4 Other Applications of Amorphous Silicon

2.4.1 Introduction

Aside from the TFT, a-Si has also been proposed and demonstrated in many other applications. For example, a-Si has been used in solar cells, image pickup tubes, passivation of single-crystal Si devices and emitters of single-crystal Si bipolar transistors. Each of these applications will be briefly reviewed in this section.

2.4.2 Solar Cells

The first a-Si:H solar cell was fabricated by Carlson[113] in 1977. Due to poor contacts, the conversion efficiency of this device was less than 1%. Since then solar cells have been fabricated with efficiencies over 10% and are expected to improve further as material properties and design techniques are improved. Commercialization of amorphous silicon alloy solar cells began in 1980 with Sanyo's introduction of a solar-powered calculator. Since then solar cell powered photodetectors, power supplies for watches and NiCd battery chargers have also been commercialized[114]. Examples of a-Si solar cell structures are shown in Figure 2.12. Notice that both cells consist of a p-i-n structure.

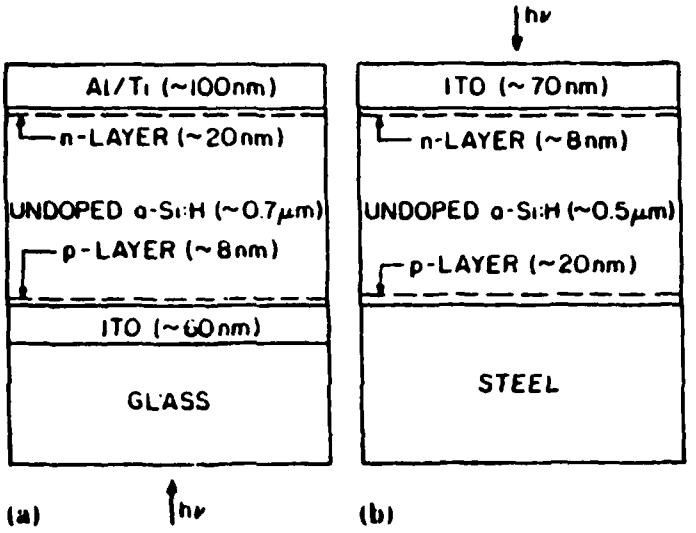


Figure 2.12 p-i-n solar cell structure: (a) on a glass substrate and (b) on a steel substrate. From Ref. 114.

Sunlight incident upon the cell generates electron-hole pairs in the junction. These carriers are then separated by the built-in electric field and collected at electrodes on either side of the semiconducting film. Since the device under load is subjected to a forward bias, it operates in the fourth quadrant of the device I-V characteristics, thereby delivering power to the external load. For efficient conversion action, the device must have good optical absorption, efficient collection of photogenerated carriers on both sides of the semiconducting film, a large built-in potential to maximize the voltage output of the cell and a small series resistance to minimize the voltage drop across the cell.

Amorphous silicon has been shown to be an excellent semiconducting film for solar cell applications because it meets many of the above requirements[114, 115]. For example, the absorption coefficient of a-Si:H is greater than $10^4 cm^{-1}$ over most of the visible range, thus requiring only a $1\mu m$ thickness to absorb most of the solar energy. Such performance is about 100 times better than that of single-crystal Si, the original solar cell material[116]. Also since the carrier collection length is sufficiently long in a-Si:H, carriers can move through the device and be collected before recombining. In particular, the collection length is equal to the product of carrier mobility, carrier lifetime and built-in electric field. Since the three latter quantities are sufficiently high, the photogenerated carriers can be efficiently collected. In addition, carrier diffusion lengths are maximized in a-Si:H by the inherently low density of localized states in the mobility gap so that more carriers can be collected.

Although a-Si:H contains many desirable properties for solar cell applications, it does have some disadvantages[114]. For example, the doping efficiency of a-Si:H could be higher to increase the built-in potential and hence the device conversion efficiency. However, doping introduces defects into the mobility gap which adversely affects the carrier diffusion length.

Device schemes other than those shown in Figure 2.12 have been developed for more optimum device operation. For example, stacked (Figure 2.13) and heterojunction devices have been developed for more efficient operation over most of the solar spectrum. In these techniques, the overall conversion efficiency is increased by stacking junctions in decreasing order of bandgap widths in the direction of radiation flow through the device[117]. Since each junction has a different bandgap width, the overall spectral response of the device will be determined by the responses of the individual junctions. The bandgaps and thicknesses of the junctions are tailored to permit the same photocurrent in each junction. Since the junctions are in series, the built-in

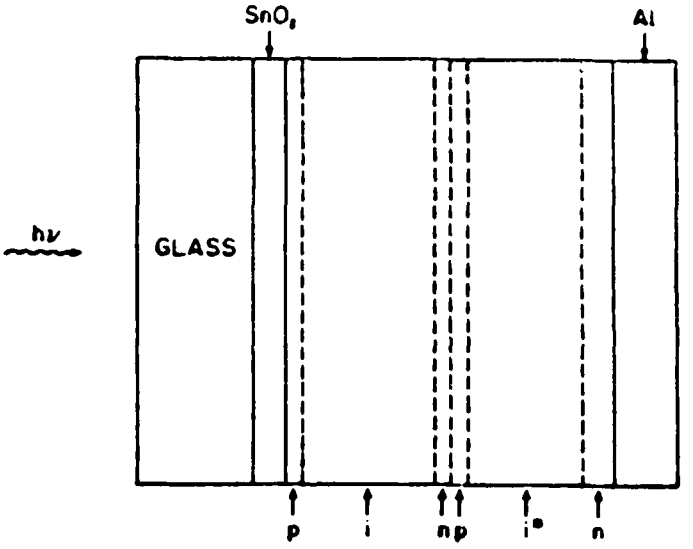


Figure 2.13 Stacked or multijunction solar cell structure. From Ref. 114.

voltages and currents are also in series permitting greater collection efficiency.

2.4.3 Image Pickup Tubes

The use of a-Si:H has also been demonstrated in image pickup tubes. Such vidicon-type imaging devices were first demonstrated by Imamura et al[118] in 1979. Since then other applications have been demonstrated, such as in a television camera for an x-ray image intensifier system and in a single tube color-imaging system[119]. Further applications of this device in high-performance imagers are expected in the field of color television cameras and high definition television systems[120].

Figure 2.14 shows the fundamental structure and operation mechanism for the image pickup tube. The resistivity of the photoconductor must be high enough to be subdivided into an array of picture elements with resistance r_p and capacitance c_p. See the equivalent circuit diagram in Figure 2.14b. The transparent electrode is biased positively with respect to the cathode. When the scanning electron beam strikes the photoconductor, the photoconductor surface becomes negatively charged and brought to the cathode potential. Since the resistance of the photoconductor is much greater than the electron beam resistance R_b, the surface potential of the photoconductor is nearly the same as the cathode. As the photoconductor is illuminated, the resistance r_p is decreased and the surface potential increased. This potential change is stored during the scanning period in the capacitor c_p. During the next scanning period, the surface is recharged to the cathode potential. The additional beam current striking the photoconductor corresponds to the light intensity at each picture element and is detected through the load resistance R as a signal current. Such type of storage operation can produce signals at low light levels approximately 10^5 times larger than would nonstorage operation.

a-Si:H has several material properties conducive to image pickup tube applications[119]. For example, the photosensitivity of a-Si:H covers the whole visible range, shows a high quantum efficiency and extends into the infrared range making it an ideal material for color television cameras. Also, a-Si:H conductivity can be changed many orders of magnitude through impurity doping making it possible to form blocking-type contacts. Such n-i-p diode like contacts suppress carrier injection into the photoconductor during the scanning operation enabling only photogenerated carriers in a-Si:H to contribute to the signal current. This reduces dark currents and supports a rapid photoresponse. However if n- and p-resistivity become too low, high resolution is difficult to

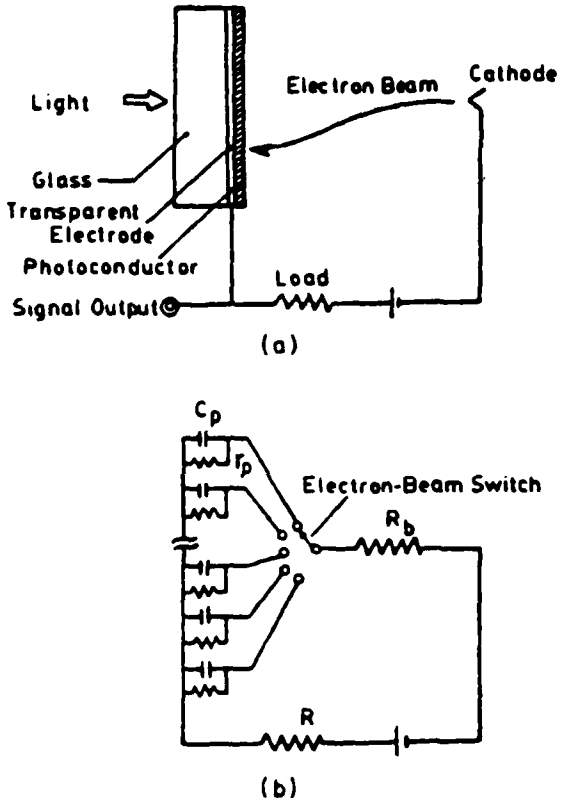


Figure 2.14 Schematic diagrams for the structure and operation of image pickup tubes: (a) fundamental structure and (b) equivalent circuit. From Ref. 119.

obtain. In addition, a-Si:H films are stable up to over 100 ° C making outdoor camera applications possible.

2.4.4 Hybrid Structures

The use of a-Si:H has also been demonstrated in improving the performance of certain single-crystal Si devices. The specific properties that have been exploited include the abundance of hydrogen in the material, the wide energy bandgap and the high dielectric constant. Two examples demonstrating this exploitation include a-Si:H as a passivant of single-crystal Si devices and as a material for heterojunction formation with single-crystal Si[121].

The surface of single-crystal Si terminates in dangling bonds. Some of these dangling bonds can be terminated by oxygen absorption forming thin oxide layers. However, not all bonds are passivated in this way. Those dangling bonds still present lead to interface states which serve as generation-recombination centers. These centers are responsible for generating unwanted noise and leakage currents in devices when a field is applied[121].

Pankove and Tarng[122] demonstrated the use of a-Si:H as a dangling bond terminator on single-crystal Si p-n junctions. They found that the reverse leakage current of such devices could be significantly reduced if a-Si:H was deposited over the p-n junction at the device surface. This improvement was found to be over two orders of magnitude greater than when a thermal silicon dioxide passivation was used.

A heterojunction is a p-n junction in which two regions have different energy bandgaps. Such structures are of particular interest because they allow efficient injection of minority carriers into narrower gap material. A forward biased a-Si/single-crystal Si heterojunction is shown is Figure 2.15.

Electrons from the wider bandgap n-type a-Si are readily injected into the lower bandgap p-type single-crystal Si, but holes are blocked by a potential barrier. The characteristics of such junctions are greatly affected by interface states that can pin the Fermi level or act as generation-recombination centers. However, the abundance of hydrogen in a-Si:H should help to eliminate these interface states[121].

Several investigators have demonstrated the use of heterojunctions in the emitter-base junction of bipolar transistors to improve the device current gain[123,124,125]. Recently, Ghannam et al[126] demonstrated the use of a-Si/single-crystal Si heterojunctions in such an application. A cross-section of their device is shown in Figure 2.16. The lower than expected current gain of

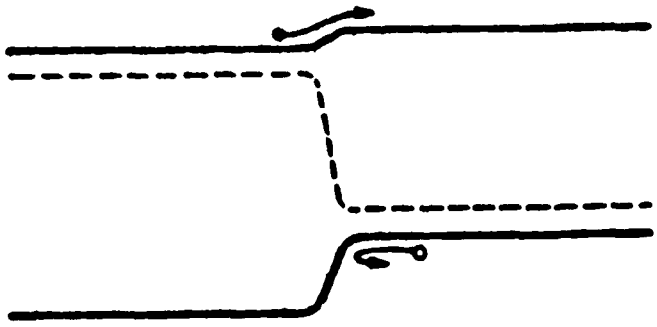


Figure 2.15 Forward-biased heterojunction. From Ref. 121.

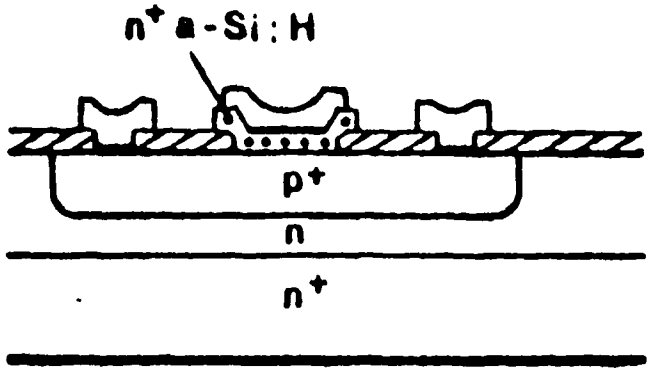


Figure 2.16 Cross-section of a bipolar transistor with a doped a-Si:H emitter. From Ref. 126.

this device was attributed to a large recombination base current component at the a-Si:H emitter/single-crystal Si base interface. Hence, a suitable passivation procedure is currently being sought to improve the current gain.

2.4.5 Closing Remarks

In this section, only a few applications of amorphous silicon have been described. Many others exist including tunnel rectifiers[127], phototransistors[128], charge-coupled devices[129], electron-beam-induced information storage[130], ambient sensors[131], photodetectors[132], electrophotography[133], switching devices[134], xerography[22] and more. With such demonstrated potential, the future of a-Si is indeed bright. As the material properties become better understood and additional models are developed, the performance of existing applications will improve and many new applications will be identified. Hence, much remains to be done before this technology is fully exploited.

CHAPTER 3
a-Si:H THIN FILM TRANSISTOR PROCESS DEVELOPMENT

3.1 Introduction

In order to investigate the ambipolar behavior of a-Si:H TFTs, it was first necessary to develop a fabrication process and make devices for testing. Basic to this process development effort was the selection of an appropriate device structure along with its associated masking levels. Once the device structure was determined, a parametric test pattern was designed which contained those structures needed in the process development and in the subsequent modeling effort. Next, the process steps peculiar to a-Si:H TFTs (i.e., depositing high quality a-Si:H films, defining patterns in a-Si:H and forming ohmic contacts to a-Si:H) were developed. Finally, devices fabricated with this newly developed process were tested and shown to exhibit state-of-the-art performance characteristics as well as ambipolar behavior. This chapter details the steps involved in this a-Si:H TFT process development effort.

3.2 Device Structure

The inverted, staggered a-Si:H TFT structure used in this investigation is shown in Figure 3.1. This structure was selected because it has superior performance to a non-inverted structure[79] and utilizes an extremely high quality, low fixed charge insulator - thermally grown silicon dioxide. This insulator is highly desirable for ambipolar a-Si:H TFT research because it permits the formation of both n- and p-channel devices at low $|V_D|$. In addition, SiO_2 is desirable for basic a-Si:H TFT research investigations because it permits small leakage currents and minimizes the effects of the insulator/a-Si:H interface trap density on device performance. Hence, the TFT performance can be observed with a minimum of parasitic effects.

The fabrication of the selected structure requires a minimum of two masking levels, but three others are included to allow maximum flexibility and ease of testing during process development. Minimally, the two masking levels required are for patterning the a-Si:H film and the metallization layer. To

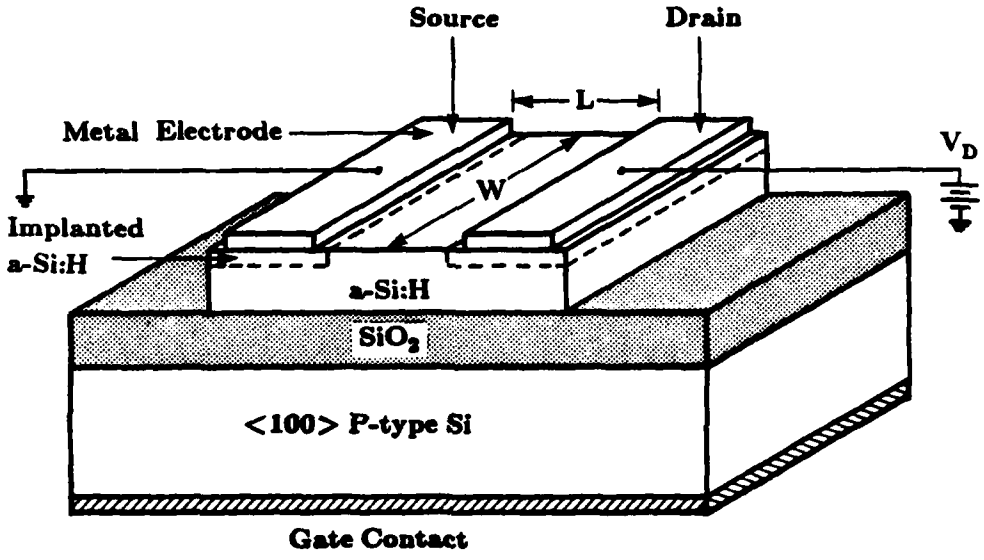


Figure 3.1 Cross-section of inverted, staggered electrode a-Si:H thin film transistor structure.

pattern the SiO_2 layer for gate contacts to the top of the Si substrate and for scribe lanes between die, a third masking level was added. To include provisions for doping the source/drain contact regions via ion implantation, a fourth masking level was added. Finally, to define passivation layer openings at the probe pads, a fifth masking level was added.

To complete this discussion of the device structure, the rationale for doping the source/drain contacts regions via ion implantation rather than via gas phase doping should be addressed. Nearly all doping done in published a-Si:H TFT studies is via gas phase doping. In fact, only laboratories at the University of Groningen[135] and Purdue[136] use ion implantation to dope the source/drain contact regions. This apparent lack of interest is not surprising considering the desirability to fabricate a-Si:H TFTs over large areas and the relative ease of doping in the gas phase using existing a-Si:H deposition systems. However, ion implantation is a widely used doping technique within the semiconductor industry that can be accomplished under much safer conditions than gas phase doping and it offers the same range of control of the electrical properties as gas phase doping[78]. Further, for basic research purposes, knowing the amount of impurity and its placement is very important in understanding device performance.

3.3 Test Pattern

With the selection of a device structure and its five masking levels, the *GLO*w *D*ischarge *A*morphous *S*ilicon (*GLODAS*) test pattern shown in Figure 3.2 was designed. The purpose of this test pattern was to facilitate the process development and permit characterization of a wide variety of a-Si:H TFTs. As shown in Figure 3.3, the GLODAS pattern was composed of three major areas; A, B and C. Area A contains 14 variously dimensioned TFTs utilizing interdigitated and non-interdigitated source/drain electrodes with undoped source/drain regions. Area B contains structures for measuring process parameters (i.e., oxide capacitance, doped and undoped a-Si:H resistivities, and a-Si:H and metallization thicknesses). Area C is similar to Area A except that the 14 TFTs contain doped source/drain regions. A common gate (or substrate) connection runs throughout the pattern, while a common source connection exists in each of the TFT areas. Appendix A contains a list of the GLODAS test structures and pen plots of Areas A, B and C.

The overall dimensions of the GLODAS pattern are 130 X 130$mils^2$ so that over 150 die can be fabricated on a single 2in Si wafer. Individual die are

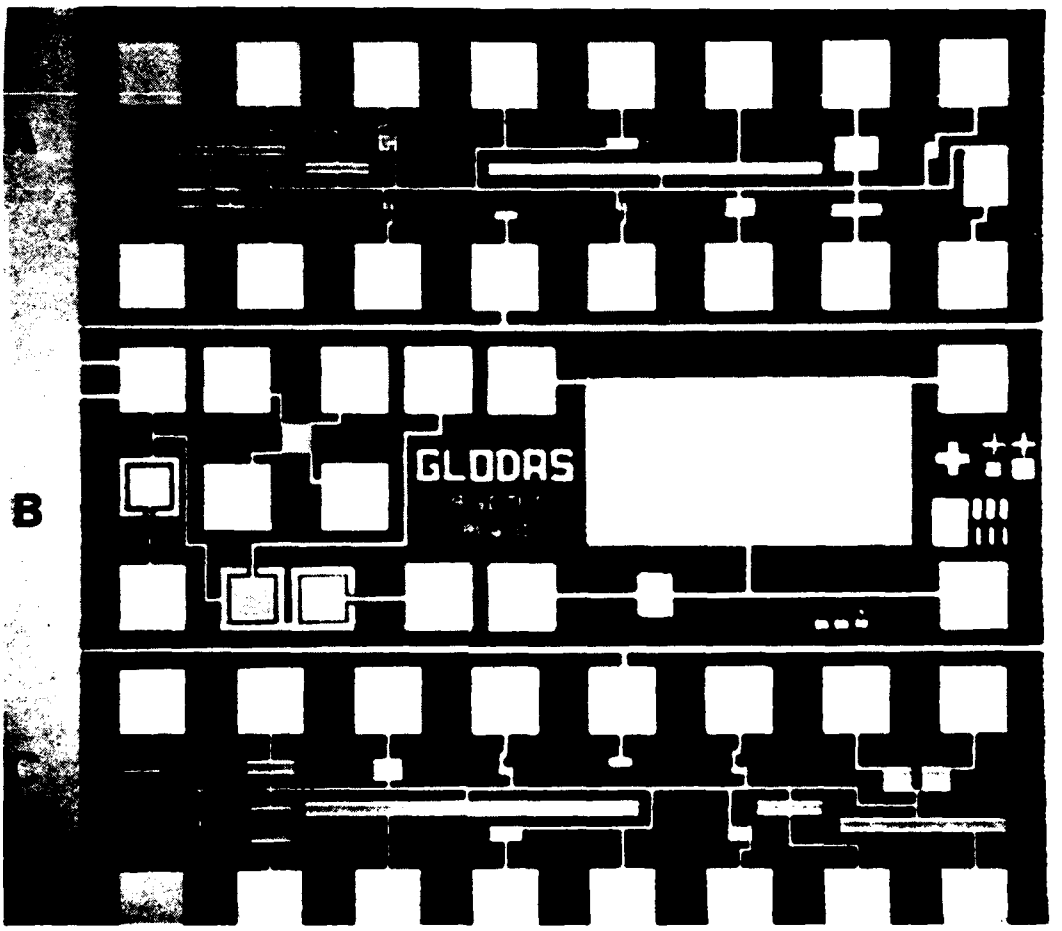


Figure 3.2 50X photograph of the GLODAS test pattern fabricated during the a-Si:H TFT process development. Area A - TFTs with undoped source/drain regions, Area B - process parameter test structures, and Area C - TFTs with doped source/drain regions.

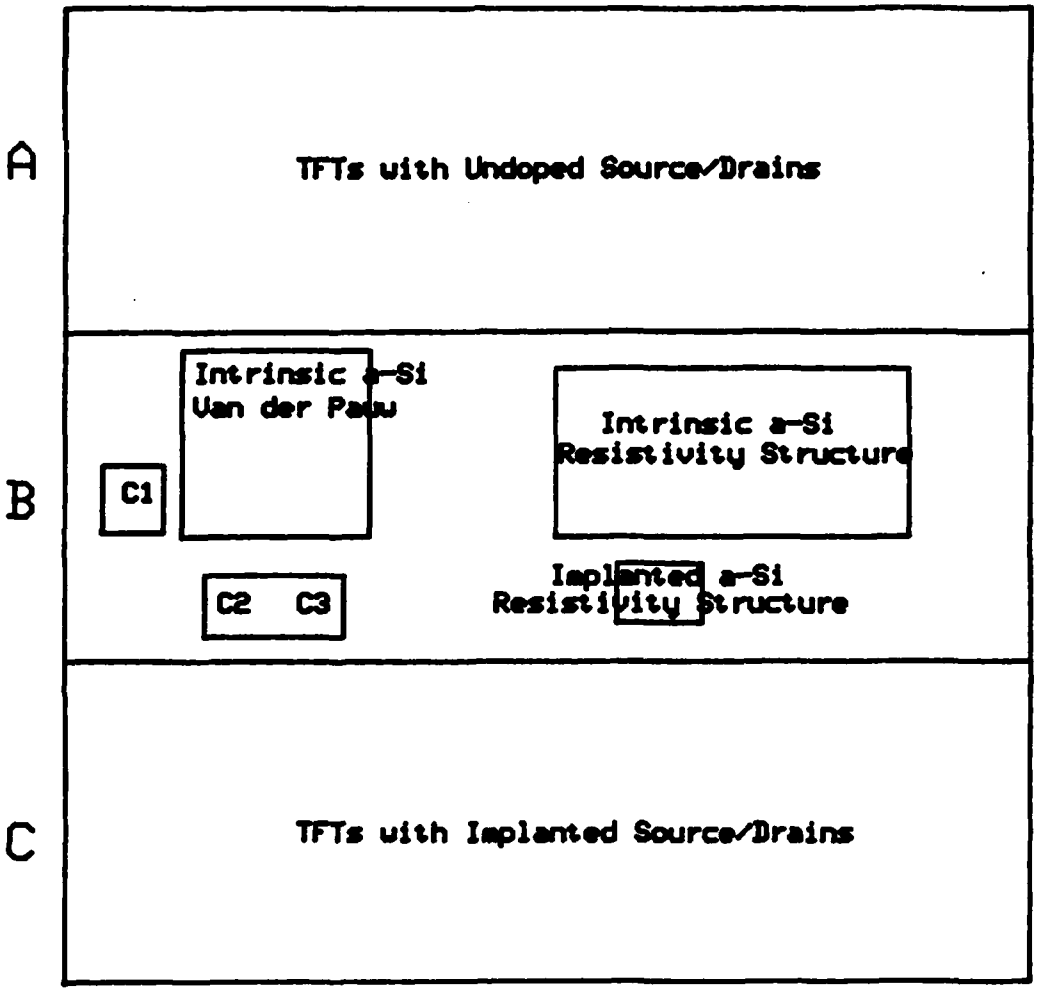


Figure 3.3 GLODAS structure locator diagram (C1 - metal/substrate capacitor, C2 - intrinsic a-Si/substrate capacitor, C3 - implanted a-Si/substrate capacitor).

identified on a patterned substrate using an x,y coordinate system. As shown in Figure 3.4, the origin, or 0,0 die, is located along the pattern's left border at the first fully patterned die to the left of the substrate flat.

3.4 Deposition of High Quality a-Si:H Films

3.4.1 Approach

As indicated in the literature review, each type of plasma deposition system has an optimum set of deposition parameters that will yield low localized state density films suitable for device fabrication. While it is possible to obtain a general set of parameters from the literature that will yield good device quality films, a systematic optimizing process of the variable deposition parameters is recommended to obtain the best film qualities from a given system. Hence, the first step in developing the a-Si:H TFT process was to determine a set of optimized plasma deposition parameters.

The approach for optimizing the deposition parameters was based on obtaining high resistivity films which inherently have a low number of defects. Such films would undoubtedly be device quality material. An optimum deposition parameter was determined by varying this parameter over a few deposition runs, while holding the other deposition parameters constant, and then noting the highest resistivity obtained in these runs. The parameter corresponding to the highest resistivity in these runs was then selected as the optimized parameter. Obviously, more runs could have been done for each parameter optimized. However, for the purposes of this research, the optimization process conducted was determined to be quite sufficient as demonstrated by the initial TFT performance presented in Section 3.4.6.

3.4.2 Plasma Deposition System

Deposition of the a-Si:H films was performed in the vacuum chamber of a TECHNICS PlanarEtch II-A System with PD II-B Deposition Module shown in Figure 3.5. This capacitively-coupled plasma-enhanced CVD system contains a vacuum chamber with radial gas input and axial exhaust, a 30KHz,500W solid state power supply, and 11in diameter electrodes separated by 1in. The lower electrode contains a substrate heater controllable up to 350 °C and hence serves as the deposition platen.

The supporting equipment for the plasma system is shown in Figure 3.6. The vacuum chamber (contained in a) is evacuated with a 400l/min two-stage,

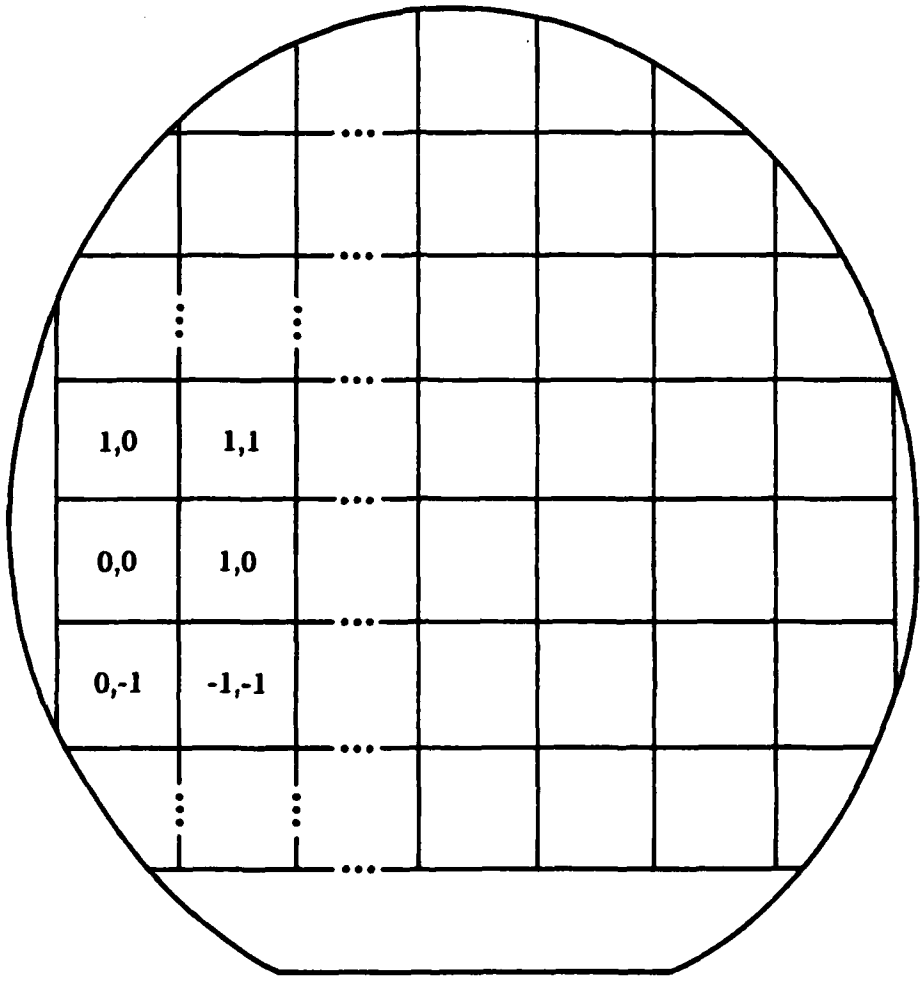


Figure 3.4 Examples of GLODAS die locations on a patterned substrate.

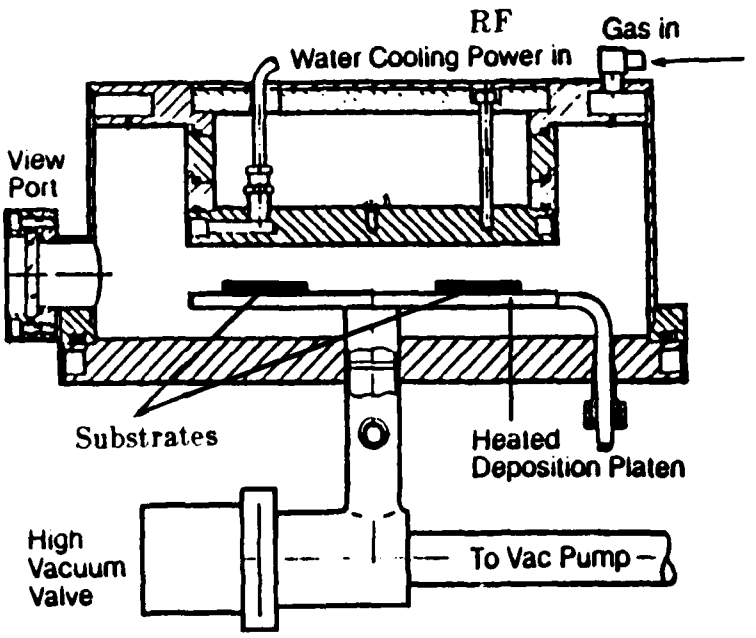


Figure 3.5 Cross-section of TECHNICS PD II-B plasma deposition vacuum chamber.

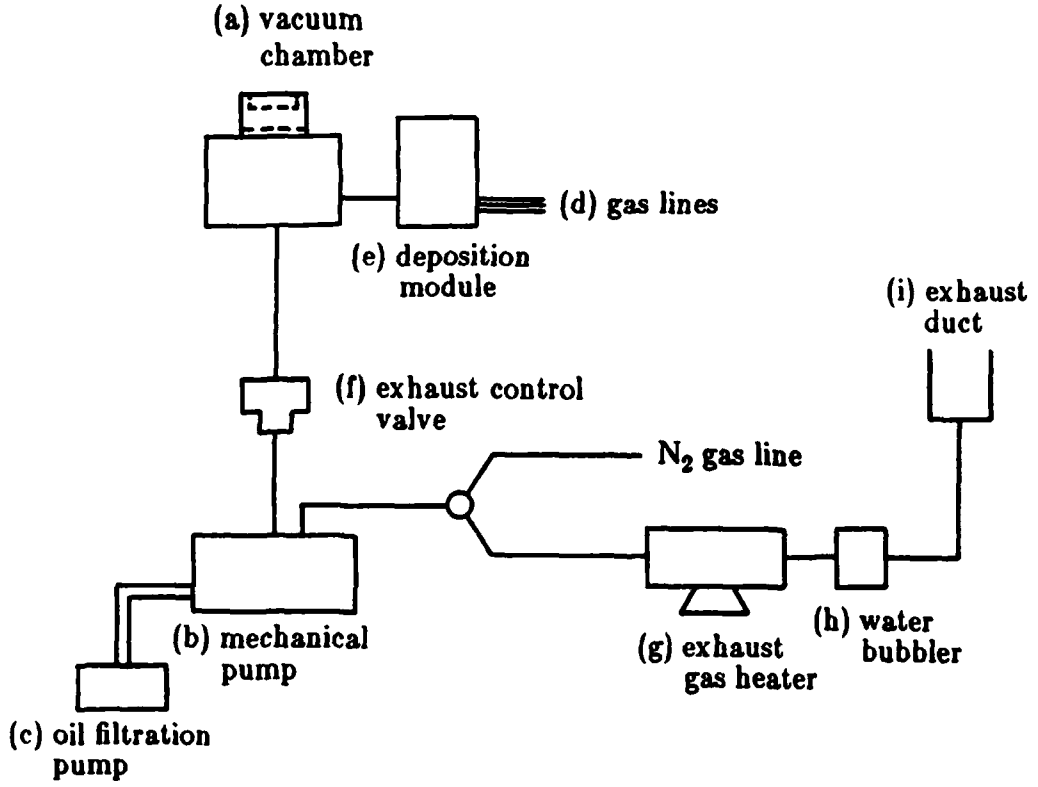


Figure 3.6 Simplified block diagram of plasma deposition system and supporting equipment.

direct-drive Alcatel model 2012A mechanical pump (b). To reduce wear on mechanical pump parts subjected to Si particulates during deposition, the pump is equipped with a Motor Guard model 111300 oil purification system (c). The deposition process gases (d) are metered into the vacuum chamber under the control of MKS model 2295B-00100 mass flow controllers located in the PD II-B module (e). These gases enter the chamber via a gas ring located underneath the deposition platen. An MKS type 253A-1-40-2 control valve (f) controlled by an MKS type 252A exhaust valve controller (EVC) is used to maintain the desired chamber pressure during deposition. The gases exhausted from the chamber are passed through an exhaust gas heater (g) at 800 ° C for thermal decomposition and a water bubbler (h) for Si dust removal prior to being vented into the laboratory exhaust duct (i). Such a decomposition is needed to insure the removal of all toxic and flammable gas products and particulates prior to exhausting them into the surrounding environment.

Depositions are performed by loading substrates into the vacuum chamber and evacuating the chamber to less than 90mT. Argon gas is then fed into the chamber at 45sccm, while the deposition platen is allowed to stabilize at the desired deposition temperature. (However, if a vacuum thermal etch (VTE) of the substrate is desired prior to the deposition, the platen is allowed to stabilize at the VTE temperature for the required etch time before the deposition temperature is set). After the desired deposition temperature is reached, the Ar is switched off and the appropriate deposition gases are metered into the chamber at preset flow rates. The EVC is set for the desired deposition pressure and the plasma ignited by turning on the RF generator to a preset value. The deposition proceeds until the desired thickness of deposited material is obtained. At the completion of the deposition, the RF generator, substrate heater and deposition gas switches are turned off and the EVC opened. Ar is then allowed to flow through the chamber for approximately 10min before venting and removing the substrates.

After each deposition run, the chamber is cleaned with a plasma containing a CF_4/8.5% O_2 gas mixture. This plasma is maintained at 400W and 550mT. To remove any CF_4 derivative contaminants left on the chamber walls after the cleaning etch, an Ar etch is performed at the same power and pressure levels for 5-10min.

3.4.3 Electrical Test Facilities

All electrical measurements taken during the process development and subsequent modeling effort were performed on the Hewlett-Packard (HP) probe-level data acquisition test station shown in Figure 3.7. In using this test station, the device under test, which is located on a Si wafer substrate, is placed on a 2in diameter vacuum chuck to prevent movement during the measurement operation. The chuck itself is located inside a light-tight, RF shielded aluminum box which measures 12in X 24in X 10in. An N_2 gas feed-through is available inside the box for blowing N_2 over unpassivated devices during measurements. Three probe-arm assemblies are contained within the box to provide direct electrical connection through coaxial and triaxial cables from the device under test to the HP4140B pA meter/DC voltage source.

The pA meter of the HP4140B has a basic accuracy of 0.5% over a wide measurement range ($\pm 0.001X10^{-12}$A to $\pm 1.999X10^{-2}$A) enabling stable pA current measurement at 10^{-15}A. The maximum voltage drop across the pA meter is less than 10μV at full scale (10mA) which corresponds to a resistance of less than 1mΩ.

The DC voltage source of the HP4140B is comprised of two separate programmable voltage supplies, one variable or constant (V_A) and one constant (V_B). The variable supply includes both a ramp and staircase generator. Each supply of the DC voltage source has an output range of $\pm$100V in 100mV steps or $\pm$10V in 10mV steps and the ramp range for the variable supply can be set from 0.001mV/sec to 1V/sec at 0.001V/sec resolution. Each supply has a current limiter to avoid damaging the device under test.

The HP4140B can be either manually or computer controlled. Computer control is provided by the HP9845B desktop computer via the HP-IB interface bus. Measured data can be automatically stored as well as graphically displayed on the HP9845B CRT during a measurement sequence.

To facilitate the measurement of a-Si:H TFT output drain current (I_D) vs drain voltage (V_D) characteristics at a fixed gate voltage (V_G), the TFTIVB software program was developed. This program permits output drain measurements under a variety of test conditions. In particular, the V_D start and stop voltages, the V_D voltage step increment, the hold time at each applied V_D voltage before the I_D measurement is recorded (10min maximum), and the number (up to 10) and value of the fixed V_G voltages to be applied. Also, to examine device hysteresis, a retracing of the V_D sweep from the stop voltage back to the start voltage can be requested. The circuit diagram for measuring the output drain characteristics using this program is shown in Figure 3.8a.

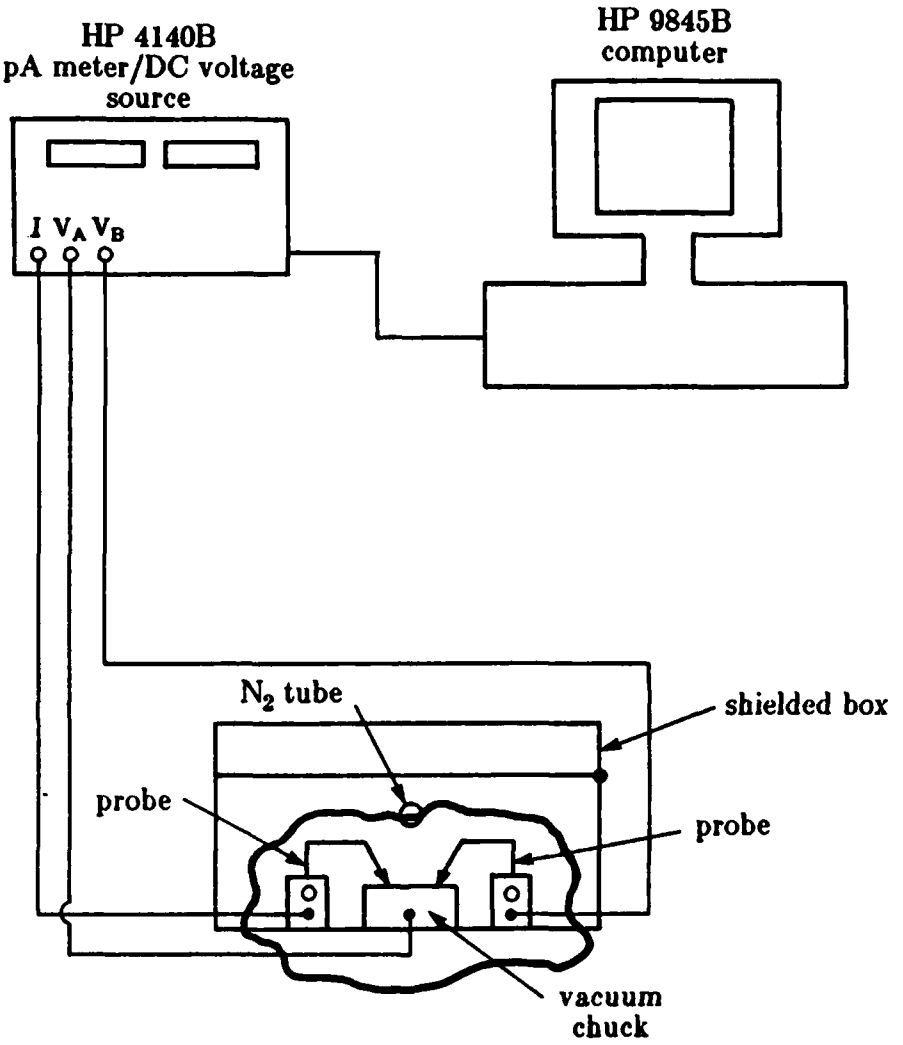
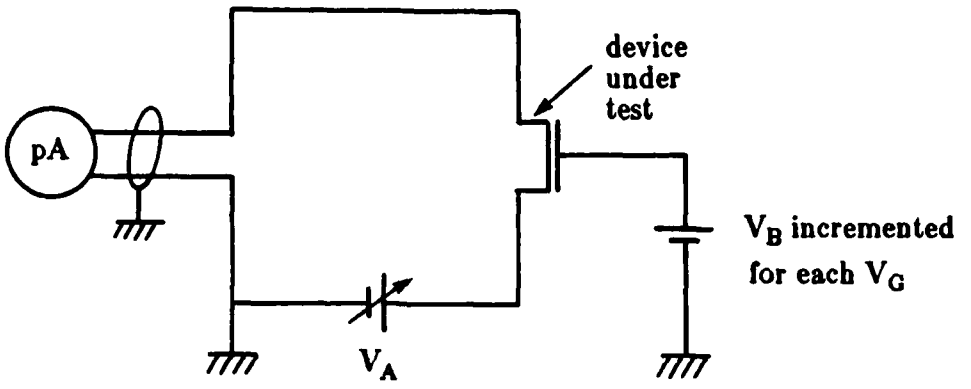
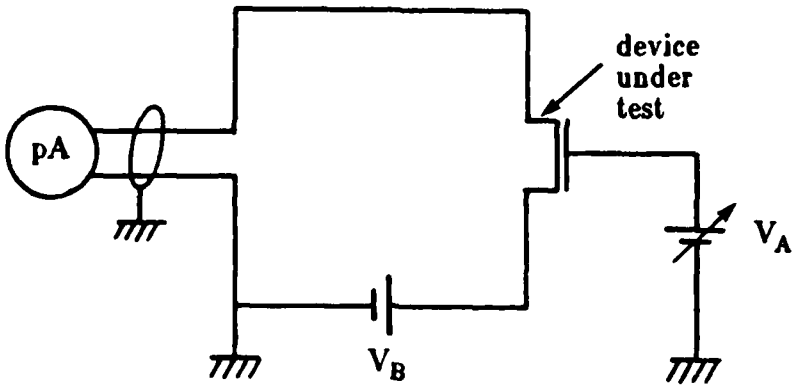


Figure 3.7 Block diagram of the HP test station.



(a)



(b)

Figure 3.8 Circuit diagrams for TFT characteristics taken with the HP4140B pA meter/DC voltage source: (a) output drain and (b) transfer characteristics.

In addition to the output drain characteristics, the TFTIVB program can also be used to obtain the transfer characteristics (I_D vs V_G at a fixed V_D) by simply reconnecting the device as shown in Figure 3.8b and noting the appropriate voltage changes in the program, i.e. V_D becomes V_G and vice versa.

3.4.4 Resistivity Test Structure Design, Fabrication and Test

The test structure shown in Figure 3.9 was used to measure the resistivity of the deposited films. This structure consists of interdigitated electrodes patterned onto the a-Si:H film surface as shown in Figure 3.10. The interdigitated electrode pattern is made up of 50 interdigitated finger pairs approximately 0.98mil wide and 95.3mils long with 1.68mils spacing between fingers. Considering the current flowing between a pair of fingers, the effective width (W) to length (L) ratio of the device is 5616. Such a wide device structure is needed in order to obtain measurable currents through the inherently high resistivity material ($\simeq 10^9 \Omega$-cm). Upon application of a voltage between the two electrodes, a current can be measured. Knowing the film thickness, the resistivity, ρ, can then be calculated using the relation

$$\rho = (V/I) t (W/L) \tag{28}$$

where V is the applied voltage, I is the measured current, t is the film thickness, and W/L = 5616.

Fabrication of the a-Si:H resistivity test structures was straightforward. The a-Si:H films were deposited onto the silicon dioxide layer of 2in diameter SiO_2/Si wafer substrates. The <100> oriented wafers were either n- or p-type with a resistivity of 0.1 to 3.5Ω-cm. Oxidations were done at either 1000 ° C for 150min or 1100 ° C for 70min resulting in 1500Å SiO_2 layers, as determined from a color chart.

Immediately after oxidation, the wafers were placed in the vacuum chamber of the plasma deposition system as described in Section 3.4.2 and a-Si:H was deposited on them. After the deposition was complete, the substrates were removed from the vacuum chamber and immediately placed in an NRC vacuum evaporation system where approximately 2000Å of aluminum was evaporated on top of the a-Si:H film at a pressure of less than $5X10^{-7}$T. Eight sets of electrodes comprising the resistivity test structures were then patterned

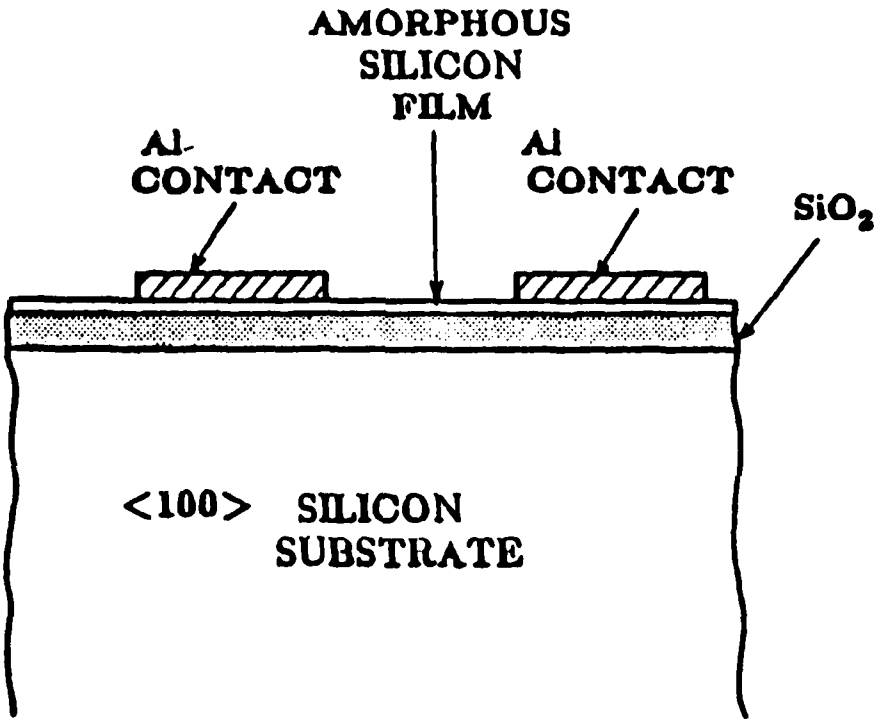


Figure 3.9 Cross-section of the resistivity test structure.

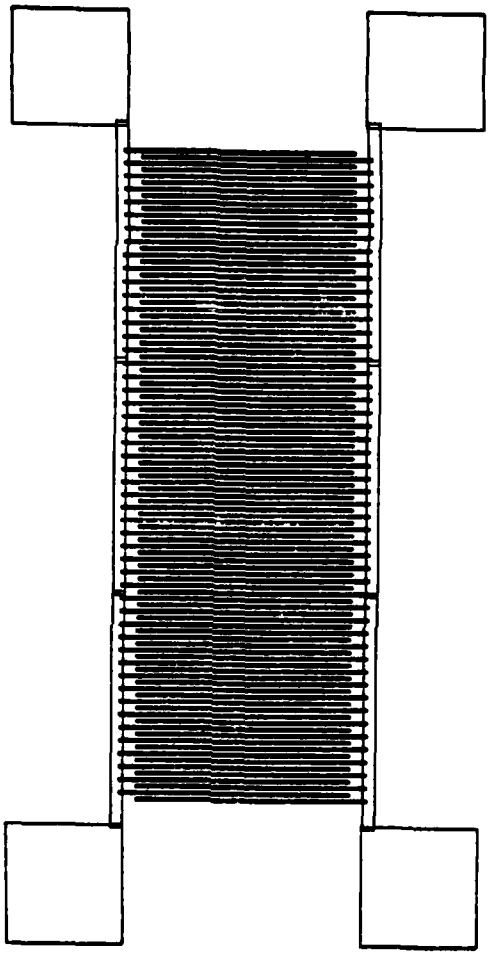


Figure 3.10 Resistivity test structure interdigitated electrode pattern.

as shown in Figure 3.11 onto the a-Si:H surface using the positive photoresist procedure in Appendix B. The unwanted Al was etched off using a mixture of H_3PO_4:CH_3COOH:$HN0_3$:H_2O = 76:15:3:5 by volume. No sintering or annealing of the Al was performed.

The individual devices were identified for testing by their oxidation run number and location on the substrate. In general, each device was given a designation of the form AA-B#C. AA refers to the oxidation run number, while B refers to a specific wafer within a given oxidation run. C refers to the location of the device as shown in Figure 3.11. Thus, the designation 17-3#4 refers to the device located in position 4 of Figure 3.11 on the third wafer from oxidation run 17.

Finally, the structures were examined under a high-powered microscope to identify any structures containing obvious defects, i.e., open, shorted or scratched lines. Those structures containing these obvious defects were not used for the subsequent resistivity measurements.

In order to measure the resistivity of these test structures, the substrates were placed on the vacuum chuck of the test station described in Section 3.4.3. Dry N_2 gas was then blown over the substrate surface. Probes connected to the current input and constant voltage supply of the HP4140B pA meter were placed on the probable electrodes of the structures. A constant voltage of 1.5V was placed between the electrodes and the resulting current monitored. Due to the metastable nature of the a-Si:H, it took several minutes for the current to drop to a level value suitable for resistivity calculations. Once the level was achieved, the polarity of the applied voltage was reversed and the measurement repeated. When a similar current value was obtained for both voltage polarities on a given structure, this value was used to calculate the resistivity using equation (28). In this way, any questionable test structures were eliminated from the resistivity measurements.

In using equation (28) to calculate the resistivity, it was also necessary to know the depositied film thickness, t, for a particular resistivity structure. This value was determined by etching a-Si:H patterns in either a piece of the substrate containing the given structure or a substrate deposited at the same time as the substrate of the given structure. These patterns were defined using the a-Si:H pattern definition procedure to be described in Section 3.5. After the patterns were defined, the a-Si:H thickness was measured on a Sloan DEKTAK model 138-000.

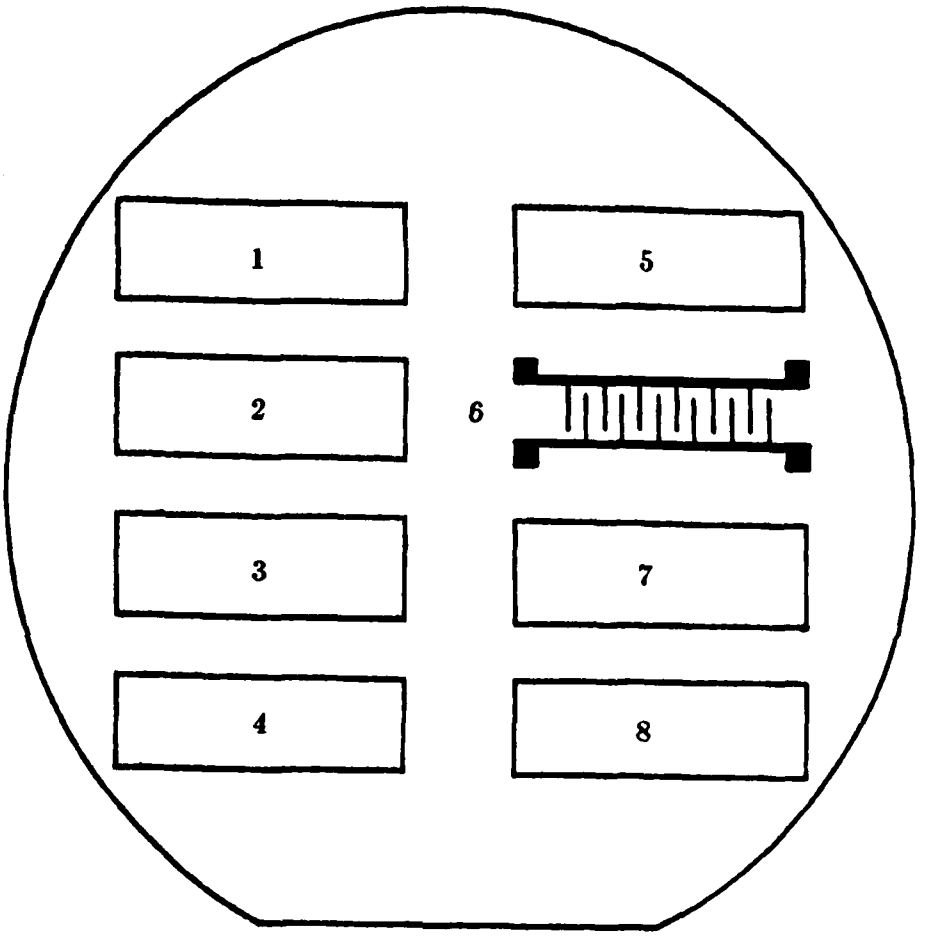


Figure 3.11 Location of resistivity test structures on substrate surface.

3.4.5 Selection of Optimum Deposition Parameters

After establishing the technique to measure the resistivity of the deposited films, many depositions were performed with varied deposition parameters. Starting from a baseline set of four deposition parameters (i.e., RF power = 15W, pressure = 300mT, substrate temperature = 275 ° C and SiH_4 = 10% in argon), one such parameter was varied for a group of deposition runs and the optimum parameter selected from resulting resistivity measurements. Since a high flow rate is needed to avoid particulates in the deposited film, only one high flow rate of 50sccm was used for all deposition runs.

Table 3.1 contains a summary of all the optimization deposition runs. In addition, the results of the highest resistivity measurements obtained for a given deposition parameter variation are shown in Figures 3.12 to 3.15. These results clearly indicate the importance of examining each deposition parameter of a given plasma system to identify the individual and total parameter effects on film quality. For example, in Figure 3.12 notice that the highest resistivity film ($1.1X10^{11}\Omega$-cm) resulted from the lowest power level (5W). Since the lowest power level also corresponds to the lowest deposition rate (0.57Å/sec), it might seem that the effect of the deposition conditions on film quality can be understood in terms of the deposition rate. However, in examining Figure 3.13, it seems that the pressure range examined has little affect on the film quality, but the corresponding deposition rates increase dramatically with pressure (from 0.67Å/sec at 300mT to 1.24Å/sec at 900mT). Similar results are seen for the substrate temperature variation in Figure 3.14 and the SiH_4 concentration variation in Figure 3.15. Hence, it is indeed necessary to examine each deposition parameter in a systematic way to determine the optimum deposition parameters.

Based on the results of the resistivity measurements from the deposition parameter variation runs, a set of optimized parameters was selected. These parameters are shown in Table 3.2. Since it was sometimes difficult to achieve a 300mT pressure in the vacuum chamber during a-Si:H film deposition, a 350-400mT pressure range was selected. According to Figure 3.13, such a range should not significantly affect the film quality.

After the optimum deposition conditions were established, a deposition run was made to examine the quality of the optimized film. As seen in Figure 3.16, the resistivity of the optimized film ($7 X 10^{10}\Omega$-cm) was certainly comparable to the highest resistivity film observed during the optimization process ($1 X 10^{11}\Omega$-cm). The only difference in the deposition parameters of these two films is the pressure (300mT vs 400mT) which was shown to have little effect on the

Table 3.1 Summary of deposition parameter variations (* indicates optimized film deposition parameters).

Device	RF Power (W)	Pressure (mT)	Substrate Temp. (°C)	Silane Conc. in Ar (%)	Dep. Rate (Å/sec)	Resistivity (Ω-cm)
8-5#6	5	300	275	10	0.57	1.1×10^{11}
8-2#7	15	300	275	10	0.80	3.4×10^{10}
8-3#1	30	300	275	10	1.15	2.9×10^{10}
12-1#7	10	300	250	10	0.69	2.1×10^{9}
11-4#2	10	300	275	10	0.67	2.5×10^{9}
11-3#3	10	300	300	10	0.67	1.6×10^{9}
13-5#3	10	600	275	10	0.73	2.2×10^{9}
15-2#3	10	900	275	10	1.24	2.3×10^{9}
14-1#6	10	300	275	5	0.44	2.1×10^{9}
14-4#7	10	300	275	100	2.52	1.4×10^{9}
*17-2#4	5	400	275	10	0.69	7.1×10^{10}

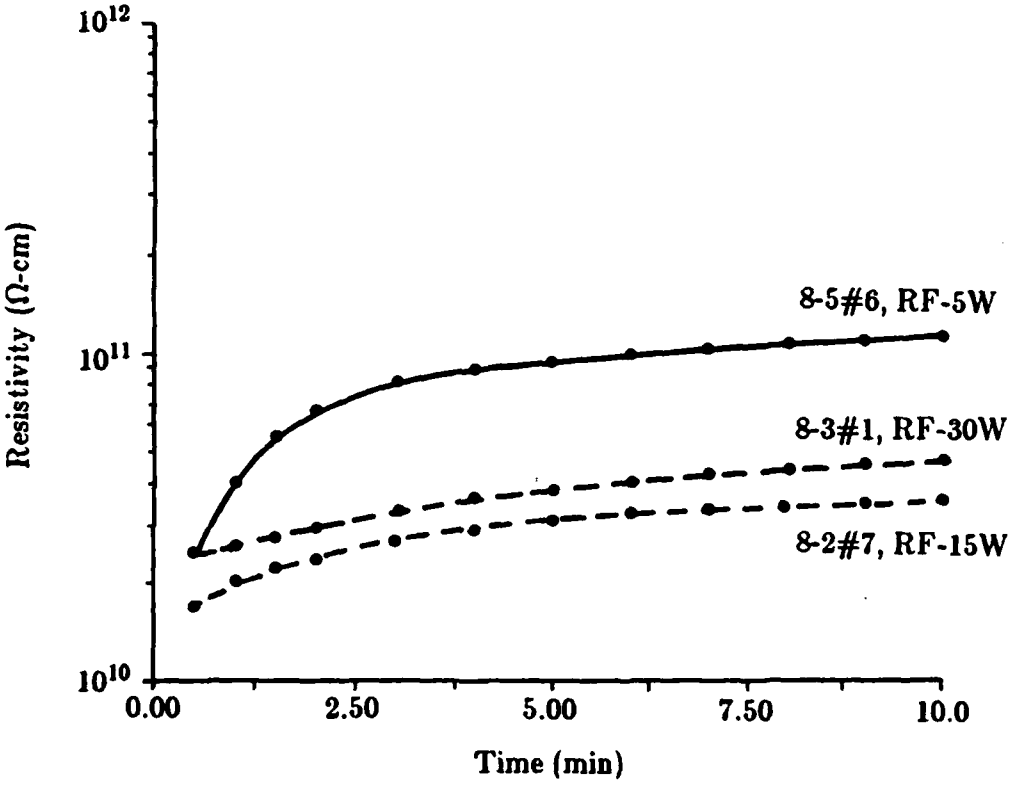


Figure 3.12 Power level variation resistivity measurements (pressure = 300mT, substrate temperature = 275 ° C, SiH_4 = 10% in Ar).

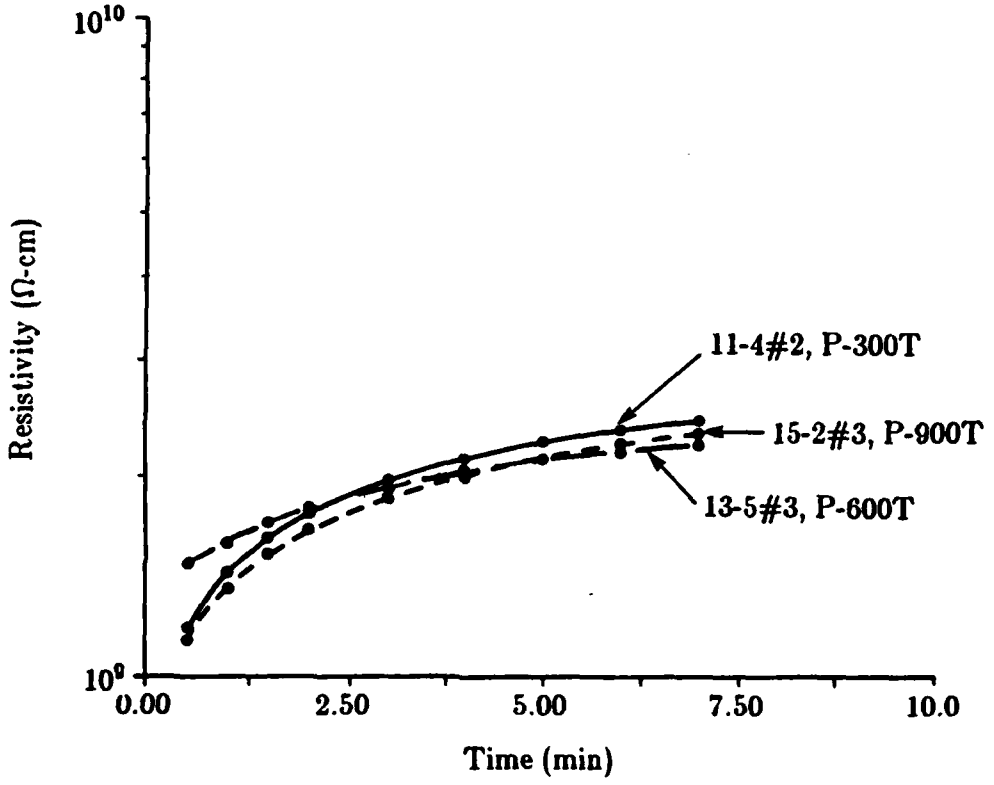


Figure 3.13 Pressure variation resistivity measurements (RF power = 10W, substrate temperature = 275 ° C, SiH_4 = 10% in Ar).

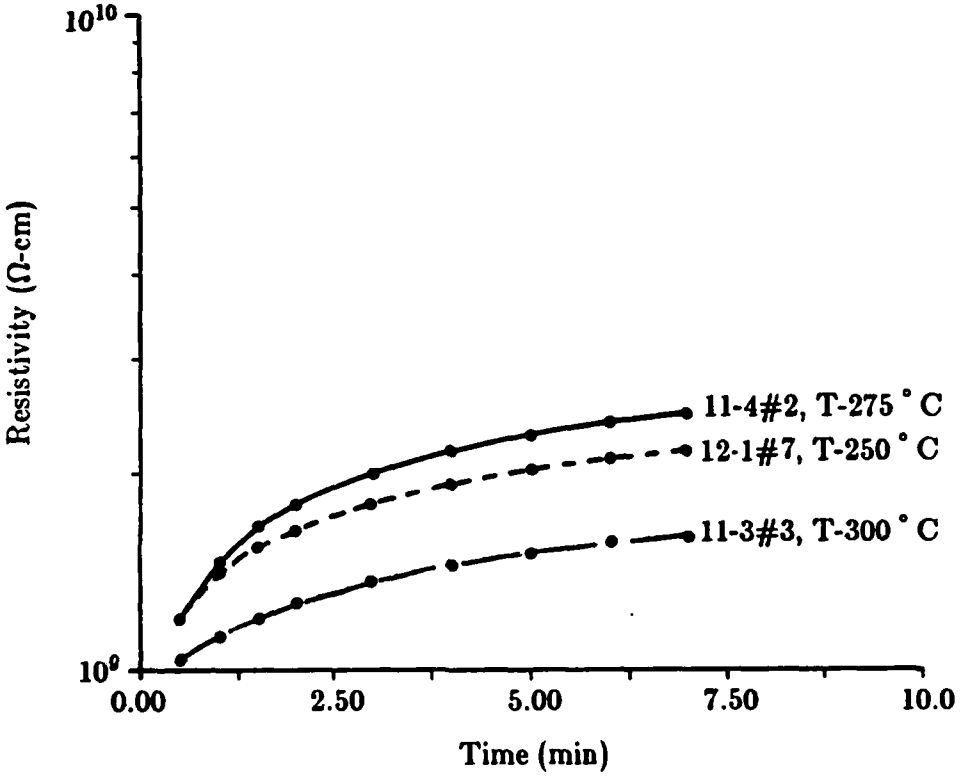


Figure 3.14 Substrate temperature variation resistivity measurements (RF power = 10W, pressure = 300mT, SiH_4 = 10% in Ar).

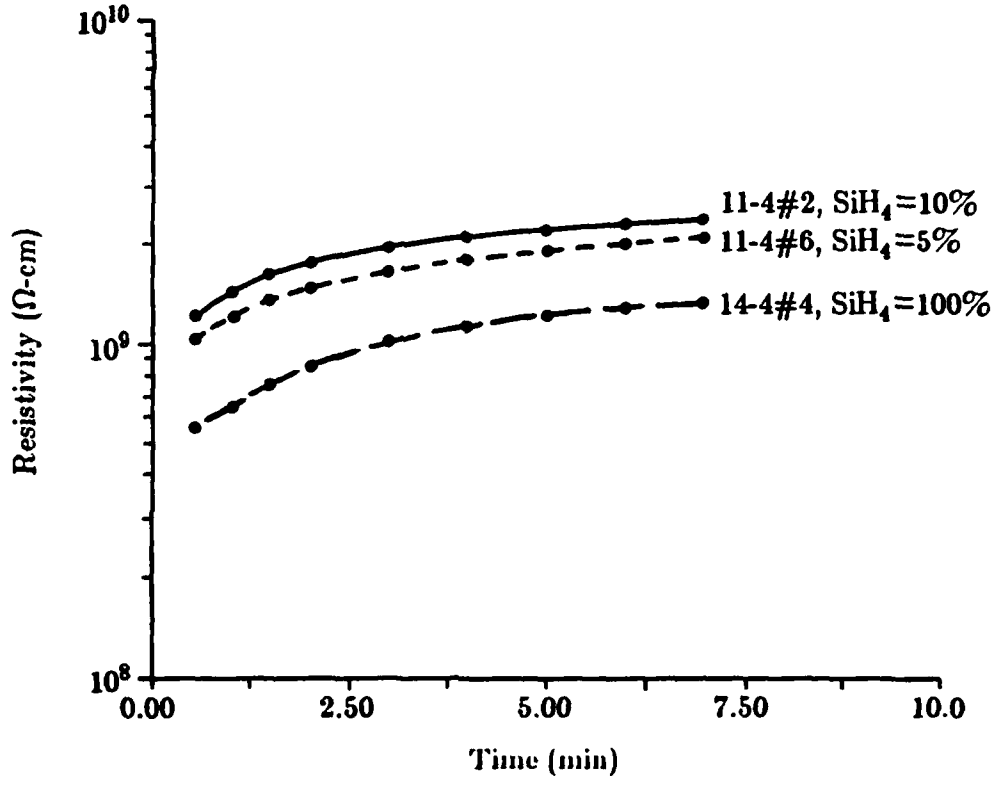


Figure 3.15 SiH_4 concentration variation resistivity measurements (RF power = 10W, substrate temperature = 275 ° C, pressure = 300mT).

Table 3.2 Optimized a-Si:H film deposition parameters.

Parameter	Value
RF power level	5W
Pressure	400mT
Substrate temperature	275 °C
SiH_4 concentration in Ar	10%

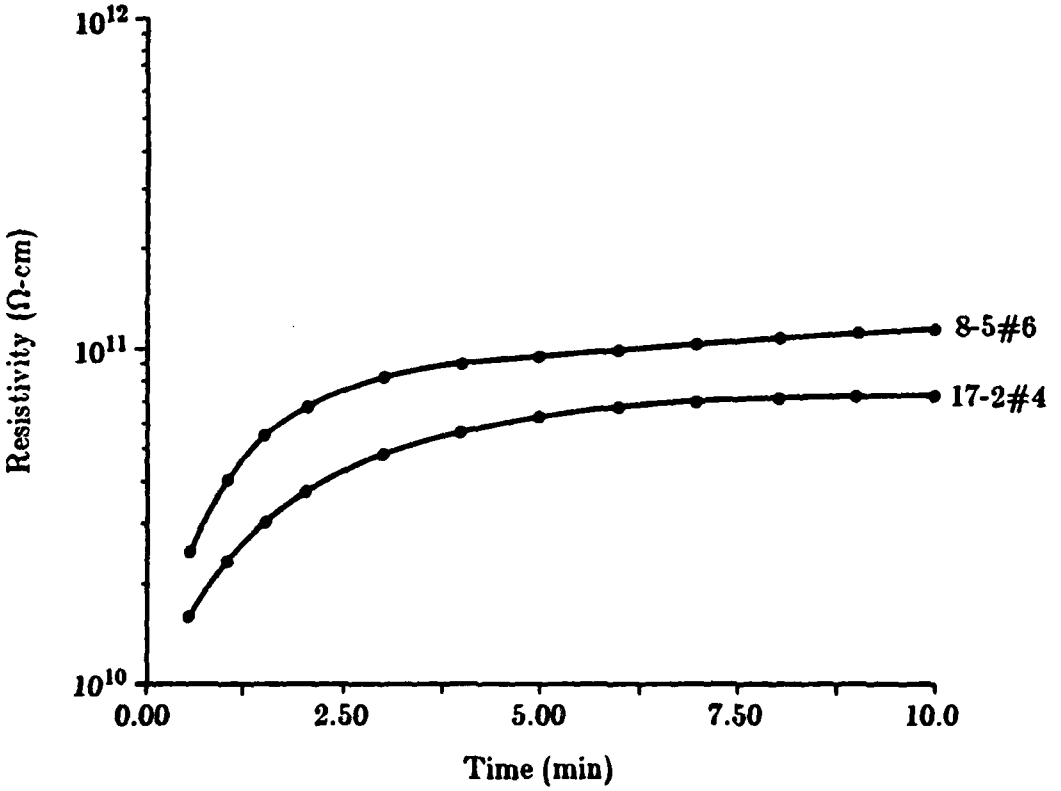


Figure 3.16 Comparison of highest resistivity film to optimized film (device 8-5#6 on highest resistivity film deposited at RF power = 5W, pressure = 300mT, temperature = 275 °C, SiH_4 = 10% in Ar; device 17-2#4 on optimized film deposited at RF power = 5W, pressure = 400mT, temperature = 275 °C, SiH_4 = 10% in Ar).

film quality (Figure 3.13). Thus, rather than continuing to adjust the deposition parameters or use the sometimes difficult to achieve lower pressure level of the higher resistivity film, the original set of optimized parameters was used to fabricate the initial a-Si:H TFTs in the process development effort.

3.4.6 Performance of Initial a-Si:H TFTs

To examine the performance of TFTs fabricated with the optimized a-Si:H films, TFTs with a relatively simple structure were fabricated and tested. In particular, these a-Si:H TFTs were fabricated as were the resistivity test structures described in Section 3.4.4 except that an Al contact was made to the back-side of the substrate for gate control. This contact was made after the oxide on the back-side was etched off. The two electrodes on the a-Si:H surface then became the source and drain terminals of the device. In addition, to improve the SiO_2/a-Si:H interface, a 4hr, 340 ° C vacuum thermal etch just prior to a-Si:H film deposition was included. Characterization measurements were then made on the TFTs to verify the test measurement techniques and device performance.

The a-Si:H TFT characterization measurements, consisting of transfer and output drain characteristics, were performed with the HP test station described in Section 3.4.3. Transfer curve measurements included both forward and reverse gate voltage sweeps to examine the hysteresis of a given device, while the output drain characteristics included only a forward drain voltage sweep. Appropriate hold times (e.g., 3 or 7min) were used to insure adequate settling of the device current at each applied voltage.

To establish a performance baseline from which to compare the performance of the TFTs made with the optimized a-Si:H films, probe-level measurements were first made on hydrogen implanted (dose = 1.5 X $10^{17}cm^{-2}$) vacuum evaporated a-Si TFTs[137]. The device characteristics for an unpassivated, evaporated a-Si TFT are shown in Figures 3.17 and 3.18. In Figure 3.17, notice that the device exhibits 6 orders of magnitude increase in current when the applied gate voltage is increased from 0 to 100V, but requires approximately 12V of gate voltage before conduction occurs between source and drain.

Recalling from Section 2.3.2 that the slope of the linear portion of the transfer curve is inversely related to the density of localized states in the mobility gap, Figure 3.17 can be used to get a relative indication of film quality. For example, the smaller slope of Figure 3.17 (0.2) compared to the

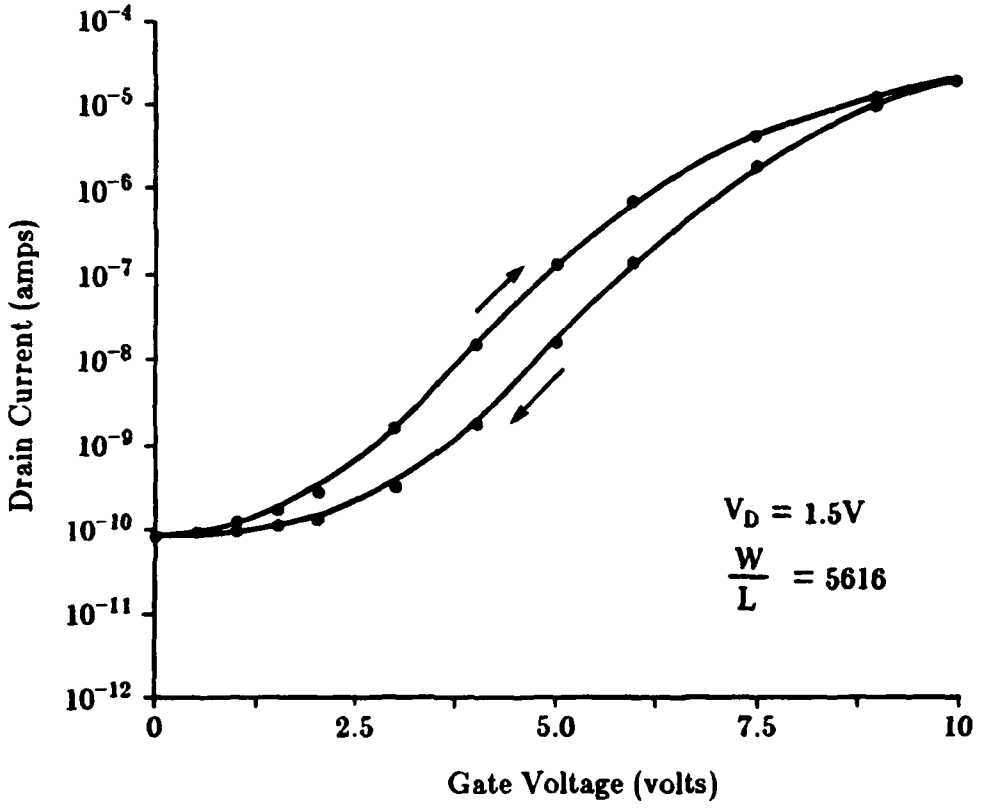


Figure 3.17 Vacuum evaporated a-Si TFT transfer characteristics for device 37*-[1]-(3).

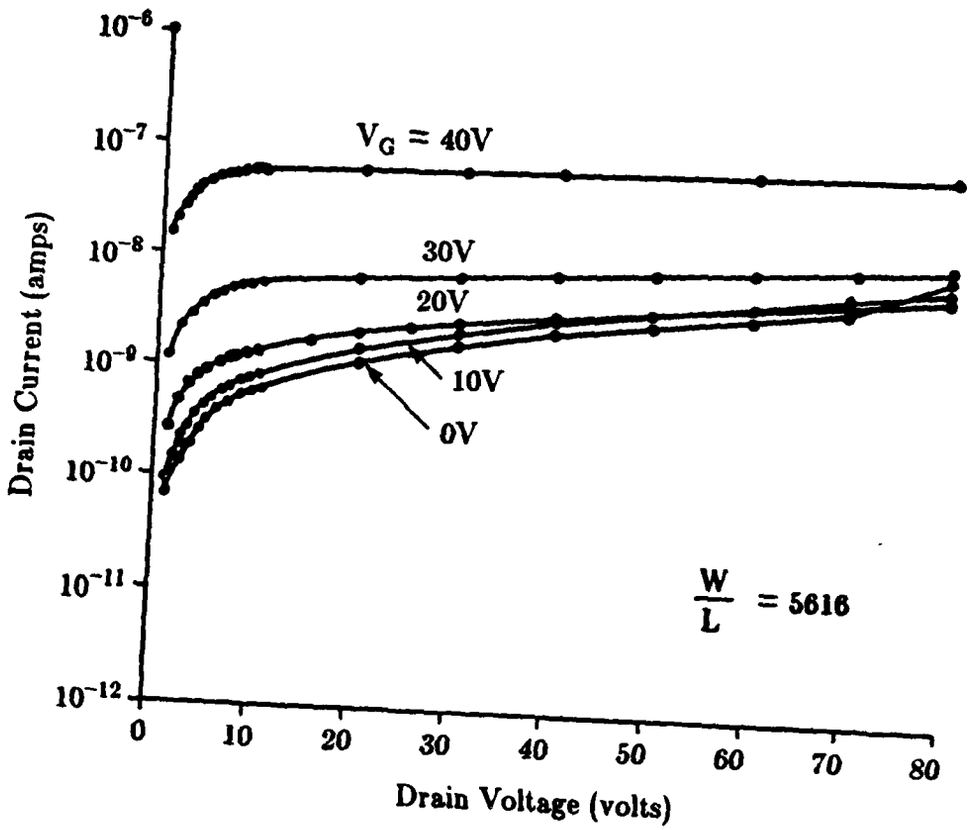


Figure 3.18 Vacuum evaporated a-Si TFT output drain characteristics for device 37*-[1]-(3).

slope of Figure 3.19 (0.6) indicates that the vacuum evaporated material has a higher density of states than the optimized a-Si:H films as expected. This higher density of states explains the need for a gate voltage of 12V to permit enhanced conduction between source and drain.

Figure 3.18 shows the vacuum evaporated a-Si TFT output drain characteristics. As expected for a given gate voltage, the source-drain current increases as the drain voltage is increased up to the pinch-off voltage. Beyond pinch-off, the source-drain current increases very little.

One of the first probe-level transfer curves for a TFT made with an optimized a-Si:H film is shown in Figure 3.19. This device exhibits a 7 orders of magnitude increase in current when the applied gate voltage is increased from 0 to 100V with less than 1V of gate voltage needed before enhanced conduction occurs between source and drain. As indicated previously, the linear portion of the slope of this curve compared to that of a vacuum evaporated a-Si TFT imply a lower density of states in the a-Si:H films. This lower density of states explains the lower gate voltage needed for enhanced conduction in the a-Si:H TFTs than in the vacuum evaporated a-Si TFT.

Figure 3.20 shows an output drain characteristic for a TFT made with an optimized a-Si:H film. Compared to the vacuum evaporated a-Si TFT output curves of Figure 3.18, the curves of Figure 3.20 contain initially steeper characteristics as a result of the lower density of states in the plasma deposited material. Notice also the abrupt current rise in the V_G = 0, 10, and 20V curves of Figure 3.20. The steeper rise is due to the ambipolar behavior of the device and will be discussed more fully in Chapter 4.

As the above measurements indicate, the optimized a-Si:H films definitely contain a lower density of states than the vacuum evaporated films and so should make for better TFTs. Hence, the a-Si:H TFT process development effort proceeded using the optimized film deposition parameters of Table 3.2.

3.5 a-Si:H Pattern Definition

In order to fabricate a-Si:H TFTs isolated from one another on the same insulating substrate, it was necessary to develop a technique to pattern a layer of a-Si:H into individual regions. Such a technique would also be useful for a-Si:H thickness measurements. Since the Cu-Be shadow mask patterning technique used in previous a-Si research at Purdue would not provide the desired dimensional tolerance control and edge acuity, an alternate patterning technique had to be developed[138].

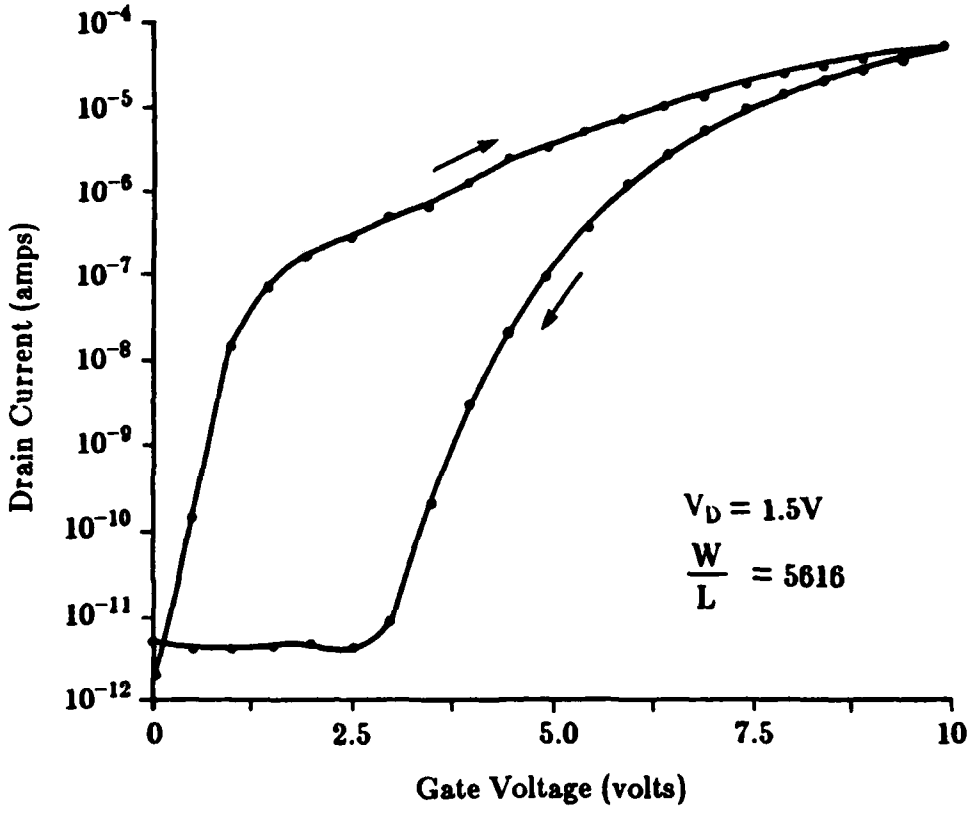


Figure 3.19 a-Si:H TFT transfer characteristics for device 17-2#4.

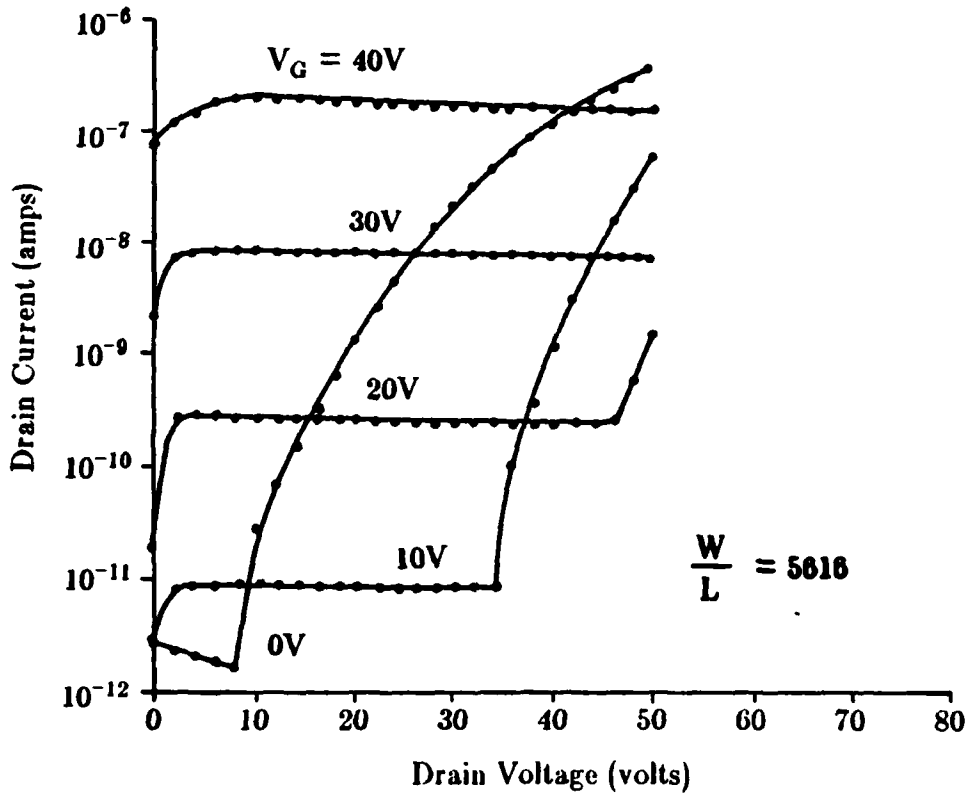


Figure 3.20 a-Si:H TFT output drain characteristic for device 17-2#4.

The a-Si:H film to be patterned is located on an insulating SiO_2 layer as shown in Figure 3.1. The film thickness is approximately 4000Å. A simple patterning technique was desired which avoids any damage to the SiO_2 insulator/a-Si:H interface, leaves the SiO_2 layer intact, and minimizes the number of additional processing steps. To avoid the possible occurrence of interface damage that would affect the TFT performance, a wet chemical etchant was pursued rather than ion milling or plasma etching. To minimize the number of processing steps, a single photoresist layer containing the desired pattern was preferred over an intermediate masking layer such as a deposited layer of SiO_2.

Published details describing the desired patterning technique were not readily available. Most papers dealing with TFT fabrication indicate that "standard" of "conventional" photolighographic techniques can be used to pattern a-Si:H[86,106,139,140], while only a few are somewhat more specific. For example, Ast[5] has indicated the used of a "modified poly-Si etch" along with a "well-baked photoresist, applied with an adhesion improver," to pattern a-Si:H. Uchida et al[8] have indicated using CF_4 along with a photoresist patterned aluminum mask for controlling a-Si geometry. Thus, the details of an a-Si:H patterning technique for the final process had to be pursued in the laboratory.

Many well-known silicon and polysilicon wet etches[141] were investigated as possible candidates for an appropriate amorphous silicon etchant. Unfortunately, most were not sufficiently compatible with a photoresist mask, even when an adhesion promoter such as hexamethyldisilazane (HMDS) and extended hard-bake cycle were used. Undercutting of the photoresist mask usually occurred resulting in a-Si:H patterns with unacceptably distorted edges. However, one etchant was found to successfully etch a-Si:H films being compatible with a photoresist mask.

The etchant found to successfully define patterns in a-Si:H, compatible with a photoresist mask, contains H_3PO_4, HNO_3 and HF in the proportions shown in Table 3.3. This etchant was originally specified to etch Cr-Si films[142].

In defining patterns with this etchant, the layer of a-Si:H on a SiO_2 substrate is first exposed to a vapor phase deposition of HMDS for 10min. A 1.76 μm AZ1350J-SF photoresist mask is then defined on the a-Si:H surface using the manufacturer's recommendations[143]. Next, the etchant is mixed being careful not to add the final etchant reagent, HF acid, until the desired etching time is relatively close at hand. For example, etching patterns in 1000Å intrinsic a-Si:H films is normally done 5 to 20min after the HF acid is

Table 3.3 Amorphous silicon etchant reagents.

Reagent	Weight(%)	Parts by Volume
H_3PO_4	85	60
HNO_3	70	5
HF	49	1

added to the etchant. This delay results in well-defined patterns. Finally, after the etching step is completed, the substrate is rinsed in deionized water to quench the etching operation and blown dry in N_2. A scanning electron micrograph of the a-Si:H pattern definition achieved with this process in a 1000Å film is shown in Figure 3.21. Note the fairly even and well-defined edges.

It should be emphasized that if the time delay is too short after mixing and before beginning to etch, the etch rate can be much too fast for controllable etching. See Table 3.4 for an example of the varying etch times (hence etch rate) as a function of the time when the HF reagent was added. Very fast etch rates cause the photoresist mask to be lifted off the film.

Alternatively, if the delay after mixing and before beginning to etch is too long, the nonuniform etching is very noticeable. The nonuniform etching is caused by the etchant first removing a-Si:H at the photoresist mask edges and at structurally less dense regions in the film. The result is a thinning of the SiO_2 around the pattern edges, at random locations across the unpatterned portions of the substrate surface, and around the periphery of the substrate. Should the etch rate be allowed to become too slow, the SiO_2 underneath the pattern edges and the less dense regions can be etched through to the Si surface before all of the unwanted a-Si:H is removed. However, this etching through to the Si surface is not a significant problem as long as careful attention is given to the required time delay between mixing and using the etchant.

Determining the a-Si:H etch rate in the etchant is very difficult. Scanning electron micrographs taken of patterned samples etched for only 1sec show that the a-Si:H is removed in chunks along the photoresist pattern edges and at seemingly less dense locations across the film down to the underlying insulator surface. The thickness of the chunks appears to be that of the original film. No layered removal was observed. In addition, etching was noticed for several seconds after a freshly etched sample was placed in deionized water to quench the etching operation. So instead of relying on a given set of etch rates, some experimentation with the a-Si:H etchant is necessary to establish a suitable set of etching parameters.

The selectivity of the a-Si:H etchant for defining patterns on both SiO_2 and SiN_x surfaces was found to be excellent (SiN_x was investigated because it is the most widely used insulator in a-Si:H TFT fabrication). Figure 3.22 shows typical etch rate variations with time after mixing and before beginning to etch, when etching SiO_2 and SiN_x films. Notice that the etch rates are

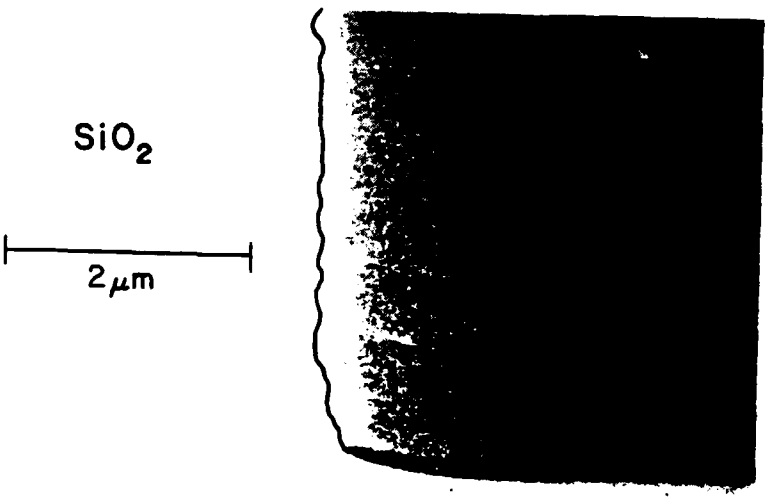


Figure 3.21 a-Si:H pattern definition on SiO_2 surface using photoresist mask and a-Si:H etchant. Etching time began 5min after HF reagent added to a-Si:H etchant. a-Si:H film thickness is 1000Å.

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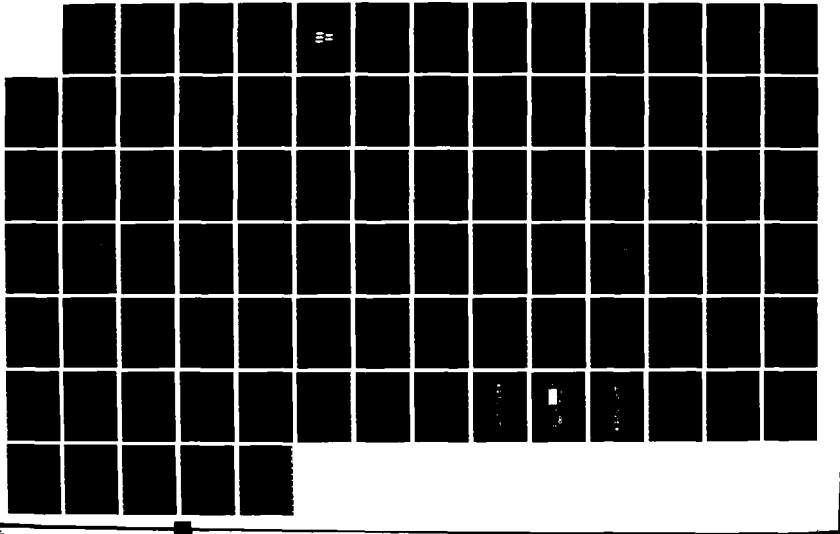

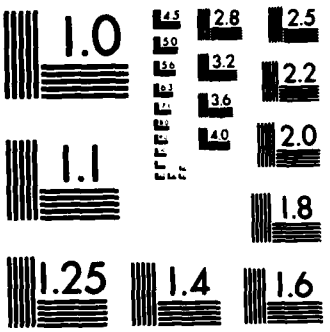

MICROCOPY RESOLUTION TEST CHART
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Table 3.4 Example of etch time variation for 900Å a-Si:H film as a function of when the last etchant reagent (HF acid) is added.

Approximate time etching cycle began after adding HF acid to etchant	Approximate etching time for a-Si:H patterns to be defined
1.5min	9sec
5.0min	20sec
60.0min	200sec

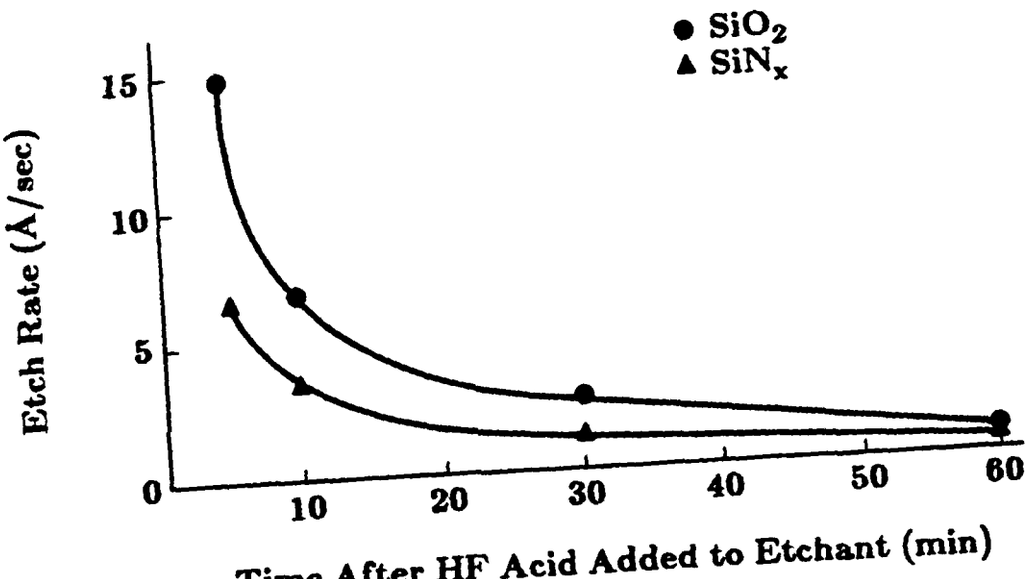

Figure 3.22 Typical SiO_2 and SiN_x etch rates as a function of time after HF reagent added to a-Si:H etchant.

sufficiently slow. This provides good selectivity when etching a-Si:H films without degradation of the underlying SiO_2 or SiN_x insulator. Also note that the etch rate for SiO_2 is greater than that for SiN_x.

Since the purpose of this work was only to identify a suitable a-Si:H etchant, a detailed study to isolate and explain the etching mechanism was not performed. However, a review of the well-known HNO_3:HF:H_2O single-crystal Si etchant reveals that excessive amounts of diluent (H_2O) cause this etchant to become "erratic and extremely critical with respect to small changes in composition."[144] Since an excessive amount of diluent (H_3PO_4) is used in the a-Si:H etchant, which is compositionally very similar to the HNO_3:HF:H_2O etchant, it seems reasonable that similar mechanisms are responsible for the etching behavior observed in both etchants. Specifically, in the HNO_3:HF:H_2O etchant, the H_2O diluent is known to limit the supply and consistency of reagents to the silicon surface through the kinetic interaction of etching components[145]. Thus, the apparently erratic behavior observed in the a-Si:H etchant could also be caused by the excessive amount of H_3PO_4 diluent affecting the HNO_3:HF etching kinetics at the a-Si:H surface.

The geometries achieved with this pattern definition process are very compatible with the desired a-Si:H TFT process. As shown in the scanning electron micrograph of Figure 3.23, five micrometer lines and spaces have been achieved with this process. However, since a micron can be lost on some edges of a pattern, this patterning process is best suited for non-critical dimensions over large areas where a strict dimensional tolerance is not required. Such dimensional tolerance is clearly acceptable for the a-Si:H patterning done in this investigation.

3.6 Contacts to Source/Drain Regions

In the fabrication of a-Si:H TFTs, it is necessary to provide direct electrical contact to the source and drain regions of the device. To insure the best ambipolar device performance possible, these contacts must be as nearly ohmic as possible. In particular, they must have as small of a built-in potential barrier as possible to allow for high-level electron and hole injection between the metal electrode and a-Si:H film. As in single-crystal Si devices, the contact performance in a-Si:H devices can be improved by doping the semiconductor region adjacent to the metal contact. Such a technique results in a large number of carriers and low barrier potential yielding high carrier injection contacts.

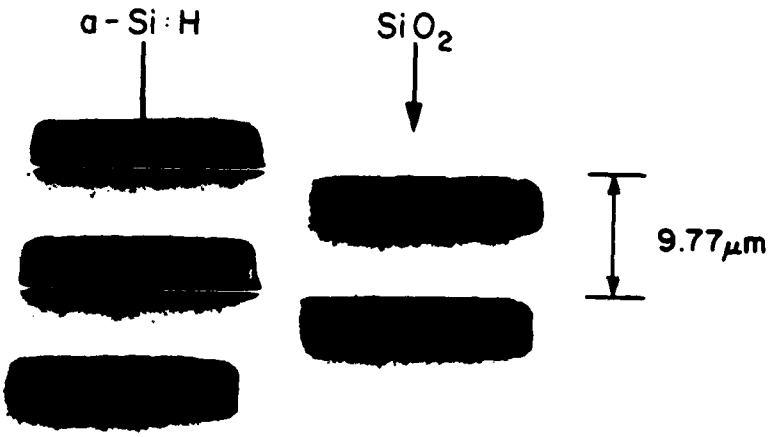

Figure 3.23 Five micrometer lines and spaces achieved with a-Si:H etchant on SiO_2 surface. Etching began 5min after HF reagent added to a-Si:H etchant. The a-Si:H film thickness is 1000Å.

Initially in the process development, it was desired to avoid doping the a-Si:H source/drain contact regions as this would add a masking level to the TFT fabrication sequence. However, when the performance of TFTs fabricated using the GLODAS test pattern without doped source/drain regions was examined, it became obvious that improvements to the source/drain contact scheme were needed. Hence, a series of experiments were performed to determine the best method of contacting the source/drain regions[136].

The source/drain contact experiments consisted of fabricating a-Si:H TFTs using the GLODAS test pattern with variations in the source/drain contact scheme. The substrates used in these experiments were <100> single-crystal Si wafers (ρ = 4-6Ω-cm). Silicon dioxide was thermally grown on these substrates in a dry O_2 environment at 1100 °C. The resulting oxide thickness was either 1200Å of 2000Å as determined from a color chart.

The a-Si:H film was deposited in the plasma deposition system described in Section 3.4.2 using the optimum deposition conditions listed in Table 3.2 for 145min. The resulting film thickness was between 4500Å and 5000Å as measured on a Tencor Instruments Alpha-Step surface profiler. The films were patterned using the technique described in Section 3.5.

Ion implantation was used to dope the source/drain regions in an Accelerators, Inc. AIM 210 implanter. The ion implants were performed on either an unheated or heated (260 °C-270 °C) substrate stage using an Al or Al-Si-Cu mask, respectively. Both single and double-level phosphorous (P^+) implants were performed. The single-level implants were at 30KeV with a total dose of 10^{16}ions/cm^2, while the double-level implants were at 30KeV and 60KeV, each with a total dose of 10^{16}ions/cm^2. The beam currents of the implanter ranged from 50 to 100μA.

Both Al and Al-Si-Cu metallization schemes were investigated. The Al was vacuum-evaporated in an NRC evaporation system, while the Al-Si-Cu was sputter deposited in a Millatron ion beam miller. Post metallization anneals were done at 200 °C in a dry nitrogen ambient for either 30min or 1hr, or both.

Individual devices were identified for testing by their oxidation run number, die location on the substrate surface and device type. In particular, a designation of the form AA-B(X,Y){I}LxW was given to each device. AA refers to the oxidation run, while B refers to a specific wafer within a given oxidation run. X,Y refer to the die location as shown in Figure 3.4. "I" indicates implanted source/drain regions, while the absence of "I" indicates these regions are undoped. L and W are the device length and width,

respectively. Thus, the designation 35-1(7,-1)10x500 refers to the unimplanted 10x500 device located in die 7,-1 fabricated on wafer 1 from oxidation run 35.

The experiments began by measuring the transfer curve of several like-dimensioned TFTs (channel width, W, = 500μm and channel length, L, = 10μm) fabricated with Al/intrinsic a-Si:H source/drain contacts. This curve then served as the baseline for all subsequent performance comparisons for devices incorporating various contact improvement schemes. Since the only difference in the various devices was in the contact schemes, any change in the transfer curves was attributed to a change in contact performance.

The first set of results of the contact experiments is shown in Figure 3.24. Notice that the baseline transfer curve for Al/intrinsic a-Si:H contacts, curve (a), shows very little conductivity change as the gate voltage was increased (less than one order of magnitude). Since no attempt had been made to remove the native oxide layer on the a-Si:H surface prior to Al deposition, this small conductivity change is not surprising. Leaving the oxide layer in this contact scheme is expected to cause a significant energy barrier for carriers moving through the contact region. However, since this contact scheme did provide a repeatable and convenient basis of comparison for the subsequent improvements to the contact scheme, it proved to be a good starting point.

As expected, the contact performance improved significantly when a buffered HF acid (BHF) dip was used to clean off the native oxide layer from the a-Si:H surface immediately preceding the Al deposition. This improvement is clearly demonstrated by curve (b) of Figure 3.24 where the drain current changed over five orders of magnitude as the gate voltage was increased. This oxide removal effectively reduced the potential energy barrier injected carriers encounter as they move through the contact region.

The contact performance was further improved by doping the source/drain contact region. By implanting phosphorous ions at a single level into the contact regions, the conductivity was further increased as is evidenced by curve (c) of Figure 3.24. Improvements were also observed for heating the substrate during the implant, curve (d), and using a BHF dip along with the heated implant, curve (e). The improvement due to the heated implant was in agreement with Kalbitzer et al[146] who found that implanting at approximately the a-Si:H film deposition temperature resulted in more efficient implants for a given amount of dopant. Heated implants have the general effect of removing defects as they are formed before clustering to larger and more stable microvoid structures occurs[78]. The improvement due to the BHF dip was again the result of a cleaner a-Si:H surface onto which the Al metallization is deposited.

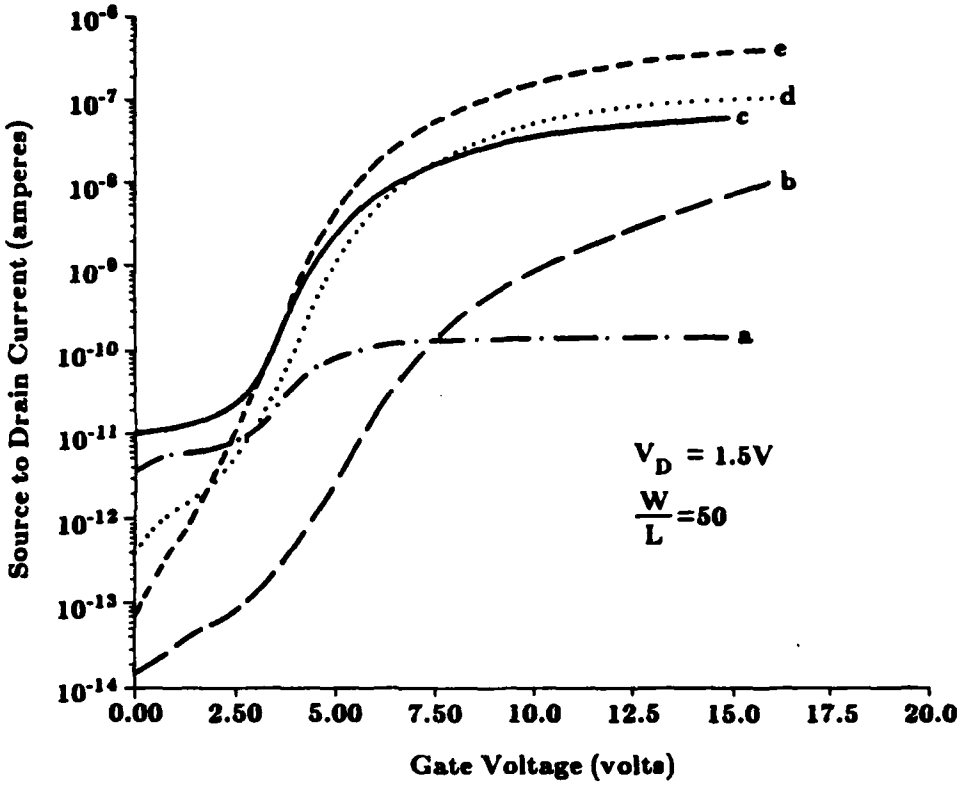

Figure 3.24 Transfer curves showing improvement to a-Si:H TFT performance as a result of changes to the source/drain contact fabrication scheme: (a) device 26-4(6,4) - Al/intrinsic a-Si:H contacts, (b) device 31-5(5,5) - Al/intrinsic a-Si:H contacts with BHF dip, (c) device 26-4(7,4)I - Al/implanted n+ a-Si:H contacts, (d) device 34-3(5,4)I - Al/heated implant n+ a-Si:H contacts, and (e) device 34-1(8,2)I - Al/heated implant n+ a-Si:H contacts with BHF dip. All device are 10x500.

The implant dosage was also found to affect the contact performance for the single-level implants. As expected, higher implant doses yielded higher current levels for both off-currents (recorded near zero gate voltage) and saturated on-currents (recorded at large gate voltages). In particular, for device 25-2(4,4)I10x500 a single-level 30KeV unheated implant with a dose of 10^{15}ions/cm^2, the off-current was $1.5X10^{-12}$A, while the saturated on-current was $1.1X10^{-8}$A. In device 26-4(7,4)I10x500 when the dosage was increased to 10^{16}ions/cm^2 while maintaining the same energy level, the off-current increased to $1.1X10^{-11}$A and saturated on-current to $6.0X10^{-8}$A. Hence, increasing the dosage from 10^{15} to 10^{16}ions/cm^2 essentially increased the current levels one order of magnitude. Increased dosages beyond 10^{16}ions/cm^2 for single-level implants would have undoubtedly increased the current levels still more, but to minimize the device off-current and avoid lengthy implant times, the 10^{16}ions/cm^2 dose was considered adequate. The increase in off-current was attributed to an increased amount of dopant getting through the Al implant mask at the higher dosage, thereby permitting an increase in back-channel leakage on the a-Si:H surface.

For completeness, implanting at two energy levels into the contact region was also investigated. Such a technique yields a thicker, more uniformly doped contact region. Since the fabrication of the double-level implant devices required a thicker silicon dioxide layer (and hence gate insulator) to mask the additional implant, the transfer curve of Figure 3.24 could not be used for comparing devices with different insulator thicknesses. Instead, a normalized transfer curve where the sheet conductance, G_s, is plotted as a function of the total surface space charge density induced by the gate field, Q, was used. G_s and Q are determined from the relations[79]

$$G_s = \frac{I_D}{\frac{W}{L} V_D} \tag{29}$$

$$Q = \frac{K_{ox} V_G}{q d_{ox}} \tag{30}$$

K_{ox} is the dielectric constant of the insulator, q is the electron charge and d_{ox} is the insulator thickness.

Figure 3.25 contains such a curve for both the single-level, curve (a), and double-level, curve (b), implants. This figure demonstrates the additional improvement in contact performance when a second implant was performed at 60KeV after the initial 30KeV implant. The dose for each implant was 10^{15}ions/cm^2. As indicated by Schropp[147], this result is due to the contact region extending deeper into the a-Si:H film nearer to the conducting channel. Such a doping depth reduces the resistance that the injected carriers encounter as they move through the enhanced channel region.

Two metallization schemes were also investigated. When Al metallization was used, the post metallization anneal temperature and time were found to affect contact performance. It is well-known that Al interdiffuses with a-Si:H above 170 ° C, thereby increasing the contact resistance[81]. Early in this investigation, a suitable annealing temperature yielding optimum contact performance was established. TFTs with unheated implants and without a BHF dip were annealed for 1hr at 250 ° C beyond an anneal of 200 ° C for 1hr in dry N_2. It was found that the 250 ° C anneal saturated on-current level was reduced to one-third the 200 ° C anneal value, while the off-current was reduced to one-fourth its 200 ° C anneal value. Thus 200 ° C was selected as the annealing temperature. Further, it was observed that devices annealed at 200 ° C for 30min in dry N_2 sometimes had slightly higher saturated current levels than those annealed for 1hr in the same environment. Therefore 30min was selected as the annealing time.

In order to obtain further improvement in contact performance, a non-interdiffusing metallization scheme was pursued. Since Al-Si-Cu is known for its non-diffusing properties in single-crystal Si, it was investigated as a possible replacement for the Al metallization. As expected when Al-Si-Cu was deposited over an a-Si:H surface, heated to 250 ° C for 2hrs and then stripped off the surface, no interdiffusion pits were observed on the a-Si:H surface. When a similar experiment was performed using pure Al, interdiffusion pits were observed. With the results of these experiments, devices were fabricated with Al-Si-Cu metallization and annealed at 200 ° C for 30min and 1hr in dry N_2. Unfortunately, no improvement in the off or saturated on-currents of the devices fabricated with Al-Si-Cu was observed when compared to similar devices fabricated with Al. Evidently the 30min annealing time used for the Al metallization was not sufficient to degrade contact performance below that observed when the Al-Si-Cu metallization was used.

Based on the result of the above experiments, the final process sequence includes implanting the source/drain contact regions with a double-level P^+

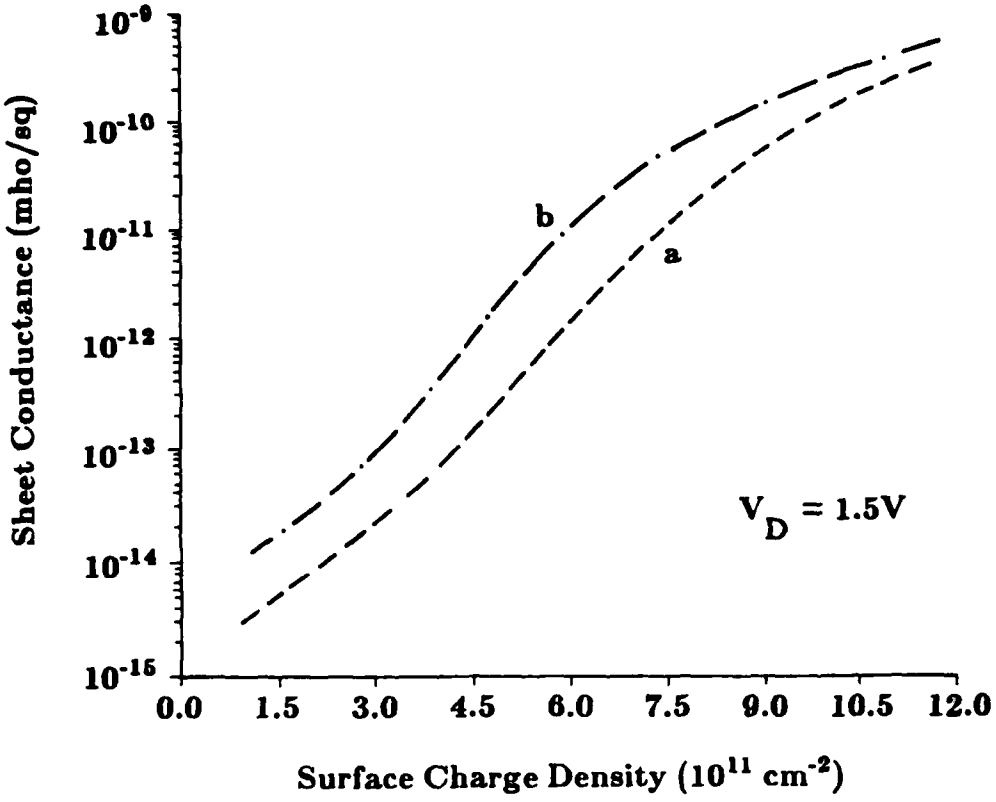

Figure 3.25 Normalized transfer curves for a-Si:H TFTs fabricated with (a) device 34-1(8,2)I - one implant at 30KeV and (b) device 36-2(8,1)I - two implants, one at 30KeV and one at 60KeV. All implant doses were 10^{16}ions/cm^2 of P+ ions done at approximately 270 ° C. All devices are 10x500.

ion implant at 30 and 60KeV. Each implant dose is 10^{16}ions/cm^2 and is performed while heating the substrate to the approximate a-Si:H film deposition temperature. Al-Si-Cu is used to mask areas not being implanted.

3.7 Device Passivation

In order to protect the a-Si:H TFTs from harmful environmental effects, such as humidity and handling, the placement of a protective layer over the fabricated devices was desired. Such a scheme should not only protect the devices, but lead to more reproducible performance characteristics by providing a more consistent back-surface environment between the source and drain electrodes. The passivation layer materials investigated were plasma deposited silicon nitride and a commercially available polyimide organic film. Both passivants can be applied to the a-Si:H TFT structure at temperatures below 300 ° C to prevent hydrogen effusion which would degrade device performance.

Application of the SiN_x film was performed in the plasma deposition system described in Section 3.4.2. After stabilizing the deposition platen to 220 ° C, the appropriate substrate was placed on the platen and the plasma chamber was evacuated to 70mT. NH_3 at a flow rate of 40sccm and SiH_4 at a flow rate of 26sccm were introduced into the chamber while controlling the pressure to 410mT. SiN_x was deposited for 15min at an RF power level of 70W. This resulted in approximately 3000Å of SiN_x. After pumping out the deposition gases from the plasma chamber, the substrate was removed. The total time the substrate was exposed to the 220 ° C deposition environment was approximately 20min.

Patterns were defined in the SiN_x films as necessary using the positive photoresist procedure described in Appendix B. The patterned SiN_x films were etched in the same plasma vacuum chamber as the deposition. Etching was performed at 70W and 200mT for 3min. The etch gas was CF_4 with an 8.5% O_2 concentration.

Application of the DuPont Pyralin PI-2555 polyimide film was performed after the surface of the appropriate substrate had been treated with an adhesion promoter. This treatment consisted of baking the substrate at 250 ° C for 30min to remove moisture, spinning on DuPont VI-651 adhesion promoter at 5Krpm for 30sec and then baking at 90 ° C for 5min. The polyimide film was spun on the substrate at 3Krpm for 30sec and cured at 90 ° C for 5min and 135 ° C for 30min.

Patterns were then defined in the polyimide film as necessary using a modified photoresist procedure to that described in Appendix B. The modifications consisted of using a different developer (AZ-351) and a longer exposure time (24.0 on the Kasper 17A aligner). Finally, the polyimide film was cured at 200 ° C for 1hr regardless of whether or not a patterning step was performed.

The investigation proceeded by fabricating simple test structures to measure the fixed charge and leakage currents associated with each passivant. The fixed charge test structure was essentially that of a capacitor. The passivation layer, which served as the dielectric, was applied to a freshly cleaned single-crystal Si wafer. The top electrode was formed by evaporating 40mil diameter Al dots onto the passivation layer surface through a shadow mask. The bottom electrode was then formed by evaporating Al onto the bottom side of the Si wafer.

Capacitance-Voltage (C-V) curves measured at 10^5Hz were attempted on the fixed charge structures with both SiN_x and polyimide dielectrics. These curves were desired to see if any obvious fixed charge, which would adversely effect TFT performance, was associated with these dielectrics. As seen in Figure 3.26, there is some fixed charge associated with the SiN_x layer, but it is not considered significant enough to markedly degrade TFT performance. Unfortunately, a C-V curve could not be obtained for similar structures fabricated with a polyimide film dielectric. Evidently the polyimide/Si interface states were sufficient enough to mask any fixed charge associated with the polyimide film.

Next, the leakage current test structures were fabricated. These structures consisted of passivating a GLODAS metallization pattern on an a-Si:H film surface. The a-Si:H film, deposited with the optimized deposition parameters listed in Table 3.2, was located on a SiO_2/Si wafer substrate. Such a structure permits Al/intrinsic a-Si:H contact I-V measurements before and after passivation. If these measurements show that the current levels increase significantly after passivation, then the passivation layer obviously provides an undesirable leakage current path and should not be used. If the measurements show little or no increase in the current levels after passivation, then the passivation layer should be a sufficient device passivant.

I-V curves were measured on the leakage current test structures before and after SiN_x and polyimide passivation. As shown in Figure 3.27, the current decreased many orders of magnitude when the SiN_x passivant was used. This decrease in current was attributed to the interdiffusion of Al and a-Si:H during

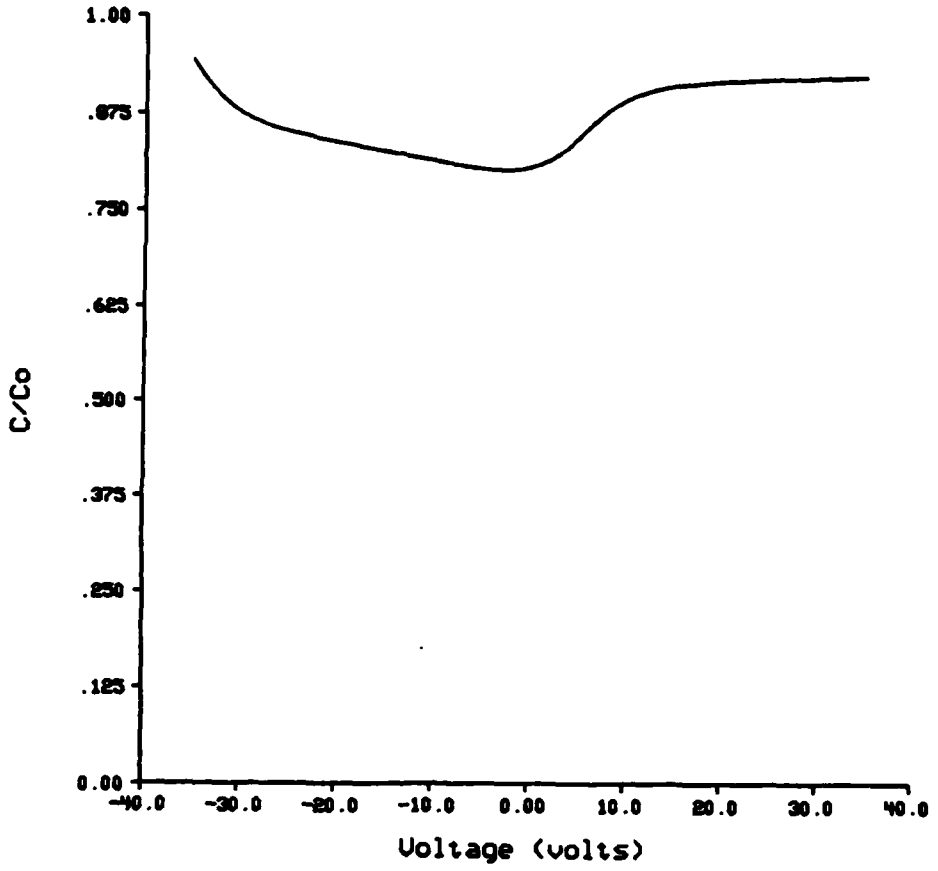

Figure 3.26 C-V curve of fixed charge test structure with SiN_x dielectric (C_o = 68.4pF, C_i = 63.4pF, frequency = 10^5Hz).

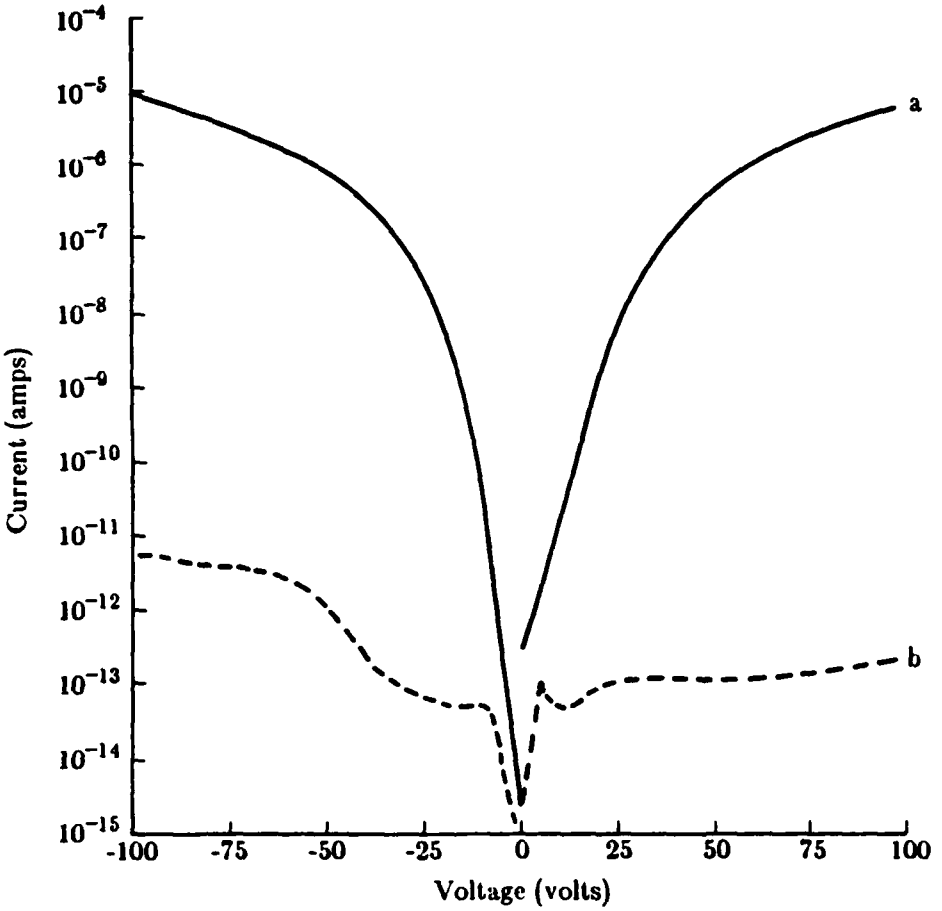

Figure 3.27 I-V measurement of leakage current test structure (a) without and (b) with SiN_x passivant.

the 220 ° C, 20min SiN_x deposition cycle which increased the contact resistance. Although such a high contact resistance may not be desirable from a device standpoint, the low measured currents indicate that the SiN_x does not provide a leakage current path between electrodes. Hence, if a non-interdiffusing metallization scheme were used, SiN_x deposited with the above deposition conditions would be an excellent passivant.

As shown in Figure 3.28, the leakage current increased noticeably when the polyimide passivant was used. Recall that the polyimide test structures were annealed at 200 ° C for 1hr so that the Al and a-Si:H must have interdiffused thereby increasing the contact resistance. However, since the current was noticeably higher after the passivation process, it appears as though the polyimide provided a leakage current path between the electrodes. Thus, the polyimide material used here does not appear to be an acceptable passivation material even if a non-interdiffusing metallization scheme were used.

Although from an environmental standpoint it was desirous to pursue a passivation scheme, from a performance standpoint it was not essential. As shown in Section 3.4, sufficient device performance could be obtained from unpassivated devices with N_2 blowing over the surface. Thus, rather than developing a non-interdiffusing metallization scheme compatible with the SiN_x passivation material, the process development proceeded without the passivation of devices.

3.8 a-Si:H Film Quality Verification

Since the a-Si:H film deposition parameters of Table 3.2 had been developed by measuring the highest resistivity films using the simple, unimproved Al/intrinsic a-Si:H contacts and demonstrated in TFTs with a simple structure using these same type contacts, it seemed prudent to verify that these films actually yielded devices of sufficient quality for this investigation. To examine the film quality, the GLODAS devices described in Section 3.6 that yielded the best source/drain contact performance (i.e., curve (b) of Figure 3.25) were used as a baseline. Recall that the a-Si:H films used in these devices were deposited at the optimum deposition conditions; RF power level = 5W, pressure = 350mT, substrate temperature = 275 ° C and SiH_4 = 10% in argon. To hopefully improve the film quality, adjustments were made to these deposition parameters that would tend to incorporate more hydrogen into the film. In particular, a lower deposition temperature was attempted to

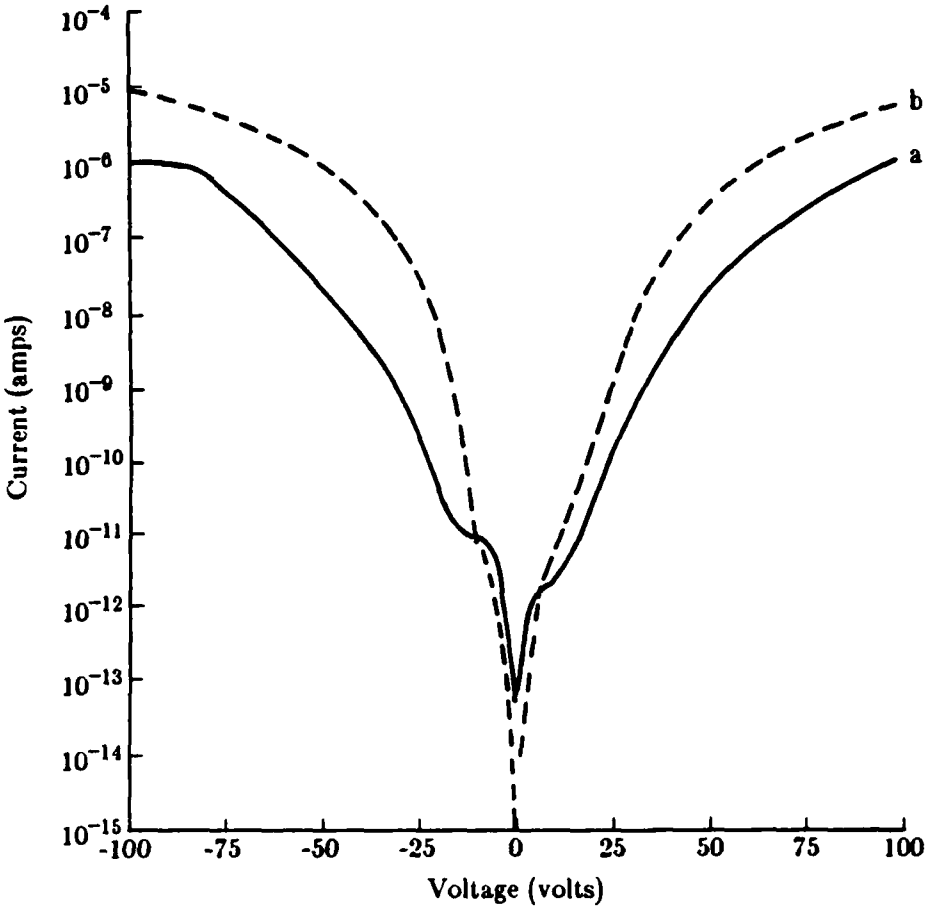

Figure 3.28 I-V measurement of leakage current test structure (a) without and (b) with polyimide passivant.

reduce any hydrogen effusion and a richer SiH_4 environment was utilized to increase the hydrogen available for incorporation into the film.

Figure 3.29 shows the results of the a-Si:H deposition parameter verification experiments. For convenience, curve (a) is the same as curve (b) in Figure 3.25 and serves as the baseline for any performance improvement comparison. Curve (b) of Figure 3.29 is for devices containing films deposited at 250 ° C and shows a slightly higher saturated current level than the baseline. Curve (c) of Figure 3.29 is for devices containing films deposited at 250 ° C and 100% SiH_4 and shows much better performance than the baseline. As a result of these experiments, an improved set of deposition parameters was selected and is shown in Table 3.5. The resistivity of a-Si:H films deposited with these improved parameters is 7.5 X $10^{10}\Omega$-cm which, as expected, is larger than that obtained for the initially optimized films of 7.1 X $10^{10}\Omega$-cm (see Table 3.1).

3.9 Final a-Si:H TFT Process Sequence and Performance Demonstration

3.9.1 Introduction

With the process development work completed, a suitable a-Si:H TFT process sequence could now be specified. This section outlines this process sequence showing several cross-sectional views of the device structure during fabrication. In addition, evidence is presented to show that devices fabricated with this final process sequence have performance comparable to those fabricated by other a-Si:H TFT researchers and display the desired ambipolar behavior.

3.9.2 Final Process Sequence Outline

The following outline highlights the fabrication steps in the final process sequence. Details for performing these steps have been presented in the previous sections of this chapter. Appendices B and C contain details of the positive and negative photoresist procedures used in this process, respectively, while Appendix D contains a final process runsheet.

1. Ultraclean substrate (2in diameter <100>, 4-6Ω-cm p-type single-crystal Si wafer) in H_2O_2:H_2SO_4 = 1:1 and buffered HF:H_2O = 20:1 solution by volume. Rinse substrate thoroughly in deionized (DI) water after each etch bath.

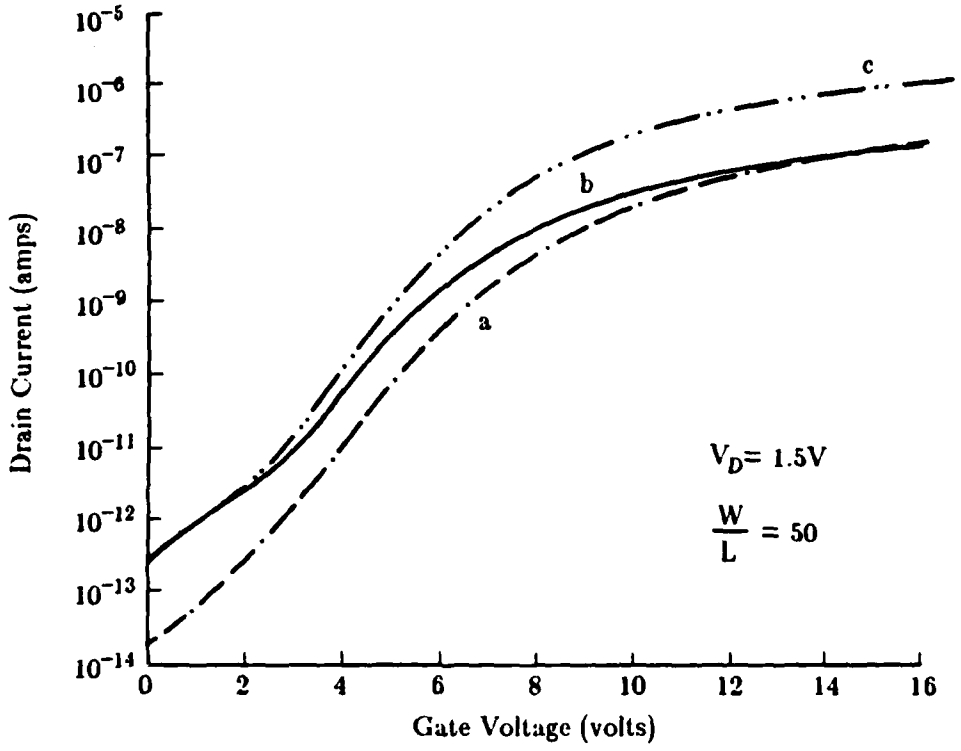

Figure 3.29 Transfer curves from a-Si:H deposition parameter verification experiments: (a) device 36-2(8,1)I - substrate temperature = 275 ° C, SiH_4 = 10% in Ar, (b) device 37-2(8,3)I - substrate temperature = 250 ° C, SiH_4 = 10% in Ar, and (c) device 38-1(4,4)I - substrate temperature = 250 ° C, SiH_4 = 100%. RF power = 5W and pressure = 350mT for all depositions. All devices are 10x500.

Table 3.5 Improved a-Si:H film deposition parameters.

Parameter	Value
RF power level	5W
Pressure	350mT
Substrate temperature	250 ° C
SiH_4 concentration	100%

2. Thermally oxidize substrate in dry oxygen at 1100 ° C for 2.5hr. Use a 3min push and pull to load and unload wafers from the oxidation furnace, respectively. This oxidation yields 2000Å of SiO_2 which is yellow-gold in color.
3. Place SiO_2/Si substrate in vacuum chamber of Technics plasma system and perform vacuum thermal etch of SiO_2/Si substrate for 2hr at 300 ° C to drive out impurities and improve the subsequent SiO_2/a-Si:H interface.
4. Deposit a-Si:H at RF power = 5W, pressure = 350mT, substrate temperature = 250 ° C, 100% SiH_4 and total gas flow rate = 50sccm. This yields approximately 4000Å of a-Si:H (deposition rate = 1.7Å/sec).
5. (MASK 1) - Define a-Si:H island pattern using positive photoresist procedures in Appendix B including a 10min HMDS precoat (See Figure 3.30).
6. Etch a-Si:H using H_3PO_4:HNO_3:HF = 60:5:1 solution by volume. Begin etching 7.5min after HF added to etchant. Strip photoresist.
7. Place substrate in Millatron ion beam miller and coat surface with >2000Å of Al-Si-Cu (Deposition rate is approximately 6Å/mA-min of beam current).
8. (MASK 2) - Define regions of a-Si:H islands to be implanted using negative photoresist procedures in Appendix C.
9. Etch openings in Al-Si-Cu using H_3PO_4:CH_3COOH:HNO_3:H_2O = 18:1:1:2 by volume by volume at 45 ° C. Strip photoresist.
10. Load substrate into AIM 200 ion implanter with the 3in matrix installed. Heat substrate to 250 ° C. Implant two $10^{16}cm^{-2}$ doses of phosphorous; one at 30KeV and one at 60KeV. Use a beam current of 50-100μA. Remove Al-Si-Cu masking layer with etchant described in step 9 (See Figure 3.31).
11. (MASK 3) - Define gate contact regions using negative photoresist procedures in Appendix C.
12. Etch oxide openings through to substrate using 6:1 premix buffered HF (BHF) solution. Strip photoresist.
13. Clean substrate in acetone, trichloroethane, acetone (3min each) and in H_2O_2:H_2SO_4 = 1:1 solution by volume (10min). Rinse substrate thoroughly in DI water before and after acid bath.
14. Immediately prior to Al evaporation, perform BHF dip for 10sec in 6:1 premix BHF. Rinse thoroughly in DI water.

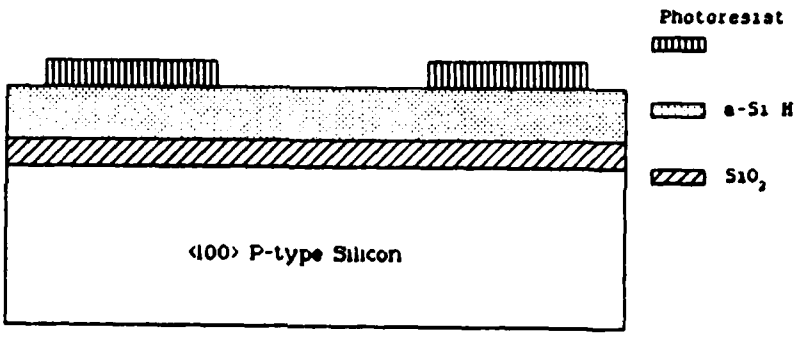

Figure 3.30 Cross-section of a-Si:H TFT during fabrication before island definition (step 5 of final process sequence).

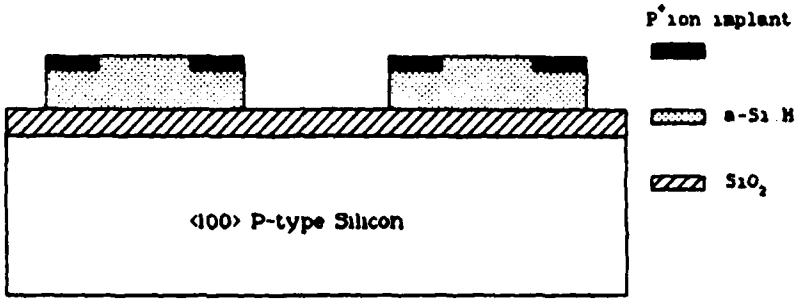

Figure 3.31 Cross-section of a-Si:H TFT during fabrication after ion implantation (step 10 of final process sequence).

15. Place substrate in NRC evaporation system and deposit between 1500Å and 2000Å of Al in the low 10^{-7}T range.
16. (MASK 4) - Define metal electrode pattern using positive photoresist procedures in Appendix B.
17. Etch Al using H_3PO_4:CH_3COOH:HNO_3:H_2O = 76:15:3:5 solution by volume. Strip photoresist (See Figure 3.32).
18. Inspect substrate under high power microscope and identify good devices for electrical probing.
19. Electrically probe devices to verify proper operation.

3.9.3 State-of-the-Art Performance Demonstration

To verify that TFTs fabricated with the above final process sequence are comparable to those fabricated in other laboratories (i.e., state-of-the-art devices) a performance comparison was made. This comparison consisted of plotting a series of normalized transfer curves for a-Si:H TFTs made in the various laboratories. As shown in Figure 3.33, devices fabricated with the final process sequence, curve (a), compare favorably to those fabricated elsewhere using an SiO_2 insulator, curves (b_1),(b_2),(b_3) and (c). Thus, the final process sequence yields state-of-the-art devices.

In addition, as shown in the transfer curve Figure 3.34, devices fabricated with the final process exhibit both n- and p-channel operation, or ambipolar behavior, while traversing over 7 orders of magnitude in drain current. In particular, when V_G is greater than the flat-band voltage (V_{FB}), electron conduction, or n-channel device operation, occurs and when V_G is less than V_{FB}, hole conduction, or p-channel device operation occurs. Hence, the final process sequence yields devices with the desired ambipolar behavior at reasonable $|V_G|$ levels.

With the successful demonstration of state-of-the-art devices exhibiting ambipolar behavior, the process development effort was completed. The research continued with the test and analysis of devices to develop a model for the ambipolar output drain characteristics.

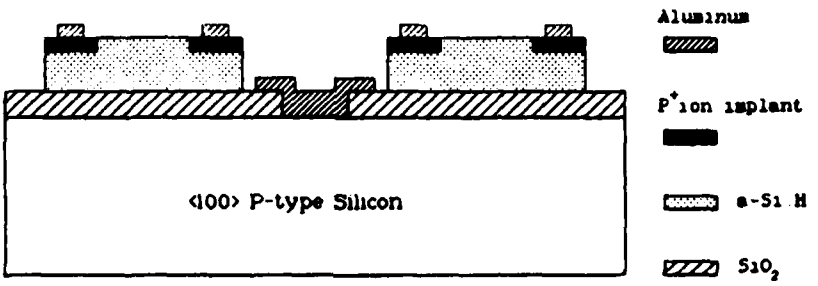

Figure 3.32 Cross-section of a-Si:H TFT fabricated with the final process sequence.

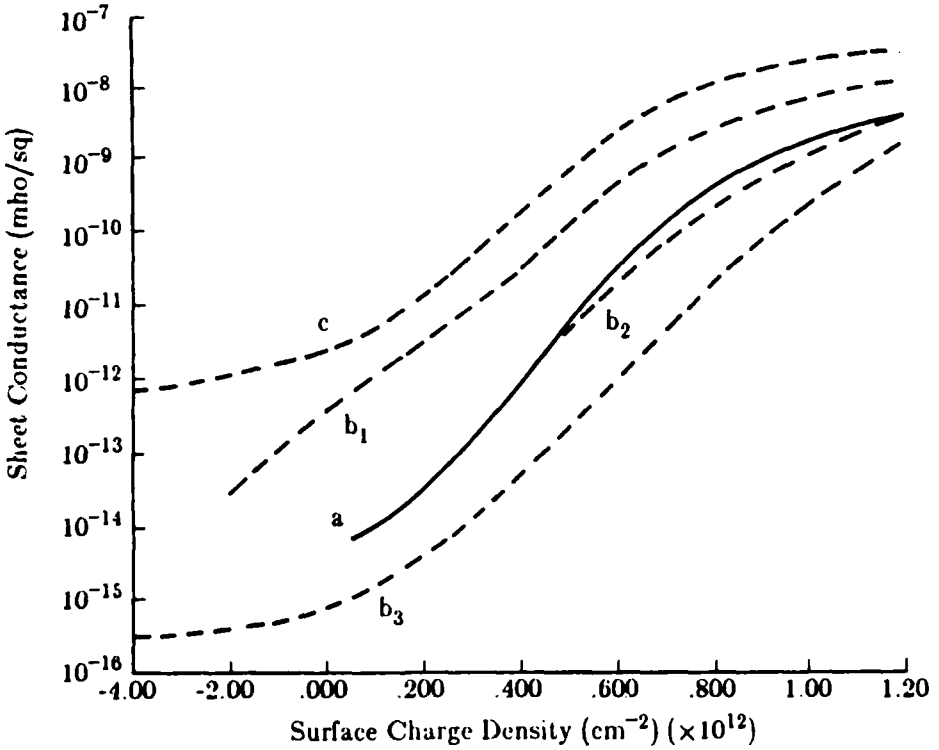

Figure 3.33 Normalized transfer curves for devices (a) fabricated with the final process sequence, (b) from Ref. 3 where 3 normalized transfer curves from 3 different laboratories are reported, and (c) from Ref 135.

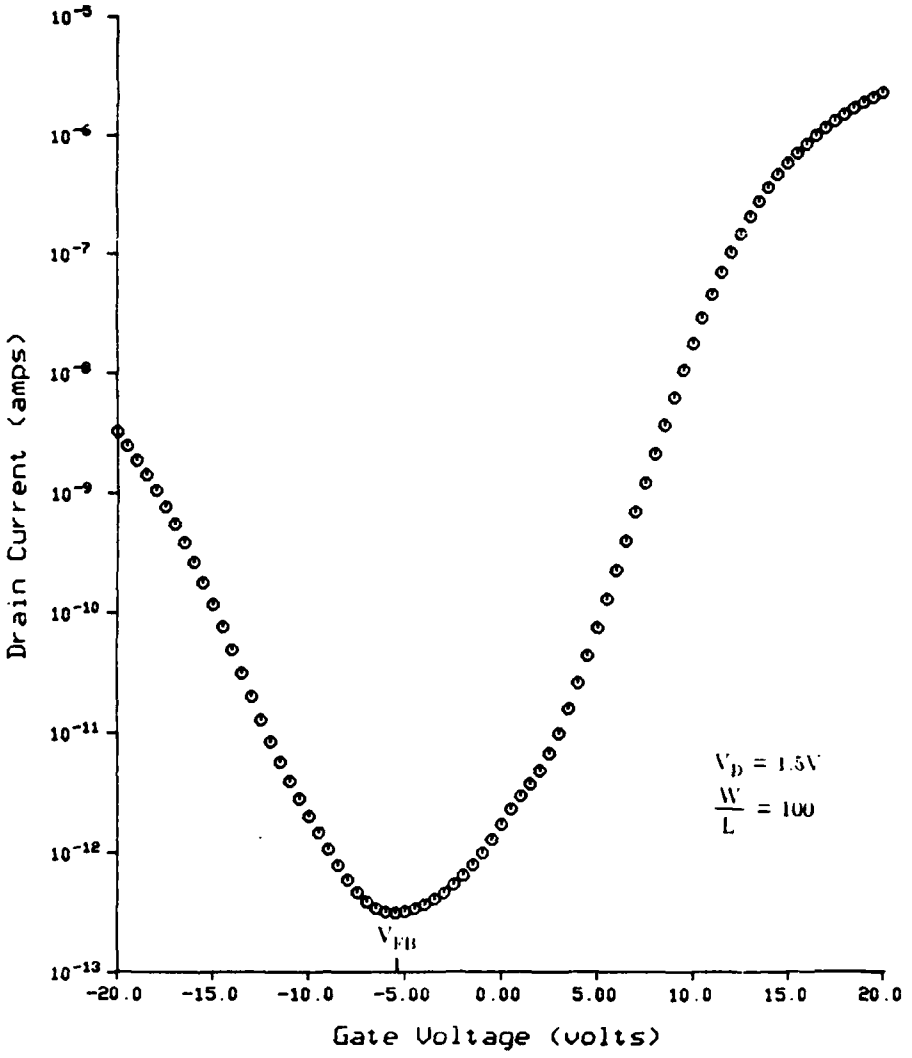

Figure 3.34 Transfer curve for device 38-1(5,2)I10x500 fabricated with the final process sequence.

CHAPTER 4
MODELING OF AMBIPOLAR a-Si:H THIN FILM TRANSISTORS

4.1 Introduction

This chapter describes the ambipolar a-Si:H thin film transistor modeling research. [148] The effort proceeded by first characterizing the performance of devices fabricated with the process sequence of Section 3.9.2. Simple TFT theory was then used to explain the device operation and to develop a basic model which predicts the output drain current vs drain voltage characteristics of these ambipolar devices. Finally, the basic model was improved to more accurately predict the output characteristics for both n- and p-type operation.

4.2 Device Characterization

After fabricating the devices, both drain current vs gate voltage transfer characteristics and output drain vs drain voltage characteristics were measured using the HP test station and TFTIVB program described in Section 3.4.3. For each device, a set of transfer curves was measured at four equally spaced values of V_D, (V_D = -3V, -1V, 1V and 3V). At each V_D, I_D was measured in 0.5V increments as V_G was swept from -20V to 20V and back to -20V. Each I_D measurement was made 10sec after a new V_G was applied. Prior to measuring a transfer curve, V_G was held at -20V for 3min to reduce the number of filled traps in the a-Si:H. As shown in the solid-line curve of Figure 4.1, each transfer curve contained a noticeable amount of hysteresis caused by charge trapping and detrapping in the a-Si:H and SiO_2 insulator. This trapping and detrapping effectively caused the flat-band voltage (V_{FB}) to shift up and down the channel as the gate voltage was increased and decreased. In an attempt to reduce the effects of this shifting V_{FB} on the subsequent modeling effort, the forward and reverse values of I_D were averaged at each measured V_G. The dashed-line curve in Figure 4.1 shows an averaged transfer curve.

Each averaged transfer curve was converted to a sheet conductance, G_s, curve using equation (29). With a set of four sheet conductance curves measured at four equally spaced values of V_D, a two-dimensional spline

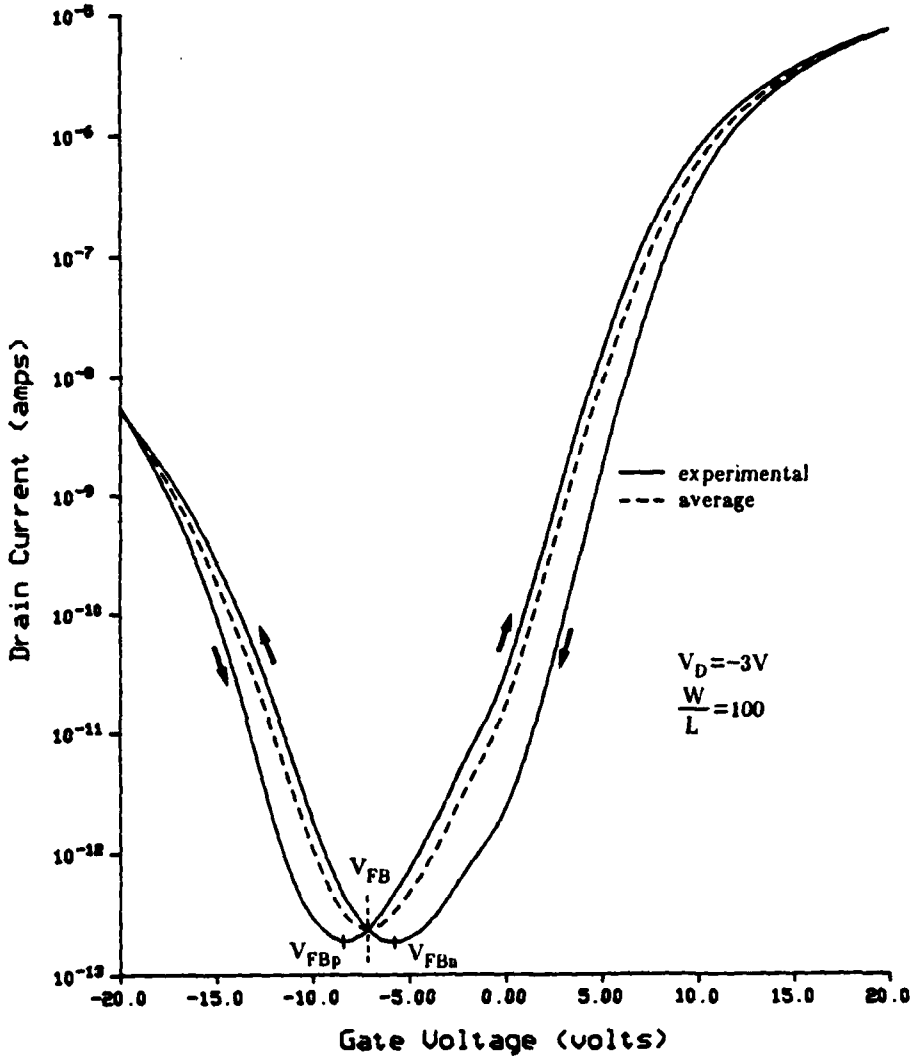

Figure 4.1 Experimental transfer curve for device 38-1(7,-1)I10x1000: (a) solid-line - forward and reverse measurement sweeps and (b) dashed-line - average of forward and reverse sweeps.

interpolation was then performed to obtain the sheet conductance curve at V_D = 0V. (The specific spline interpolation algorithm was that used by Grotjohn[149] in the TABLET transient analysis simulator). Figure 4.2 shows an interpolated G_s curve (dashed-line) plotted with two of the four experimental G_s curves (solid-line). As can be seen from this figure, the interpolation removes the inherent skew in the G_s curve determined at a single, low V_D[98]. This skew can have a noticeable effect when the G_s curve is used to model the device performance.

The output drain characteristics were recorded for several gate voltages in both the forward (V_D = 0V to 30V) and reverse (V_D = 0V to -20V) directions. I_D was measured at 0.5V increments after each V_D was applied for 10sec. Prior to recording a forward (n-channel) or reverse (p-channel) output drain characteristic, V_G was held at -20V or 20V, respectively, with the drain to source voltage open circuited for 3min. Figures 4.3 and 4.4 show experimental output drain characteristics for n-channel device operation, while Figures 4.5 and 4.6 show similar characteristics for p-channel device operation. Notice that at large $|V_D|$ the ambipolar effect of the opposite channel forming can be seen in all devices.

In comparing the transfer and output drain characteristic measurement techniques, it should be noted that each technique subjects the device under test to different operating conditions, particularly with regard to V_{FB}. For example, during the transfer characteristic measurements, V_{FB} was constantly shifting due to charge trapping as V_G was increased and then decreased. Alternately, during the output drain characteristic measurements, V_{FB} remained relatively fixed at each V_G, but changed down the channel as $|V_D|$ was increased.

4.3 Device Operation

In examining the n-channel output drain characteristics of Figures 4.3 and 4.4 for the ambipolar a-Si:H TFT, four regions of device operation can be seen. As indicated in Figure 4.7, the first region occurs at low V_D where the characteristic is linear. This corresponds to a low resistance enhanced electron channel existing along the SiO_2/a-Si:H interface in parallel with the bulk a-Si:H resistance. As the drain voltage is increased above 0V, electron current through the device increases linearly until the change in potential across the drain end of the device reduces the number of electrons at the drain end to a negligible amount (see Figure 4.8). As indicated in Section 2.3.2, this potential

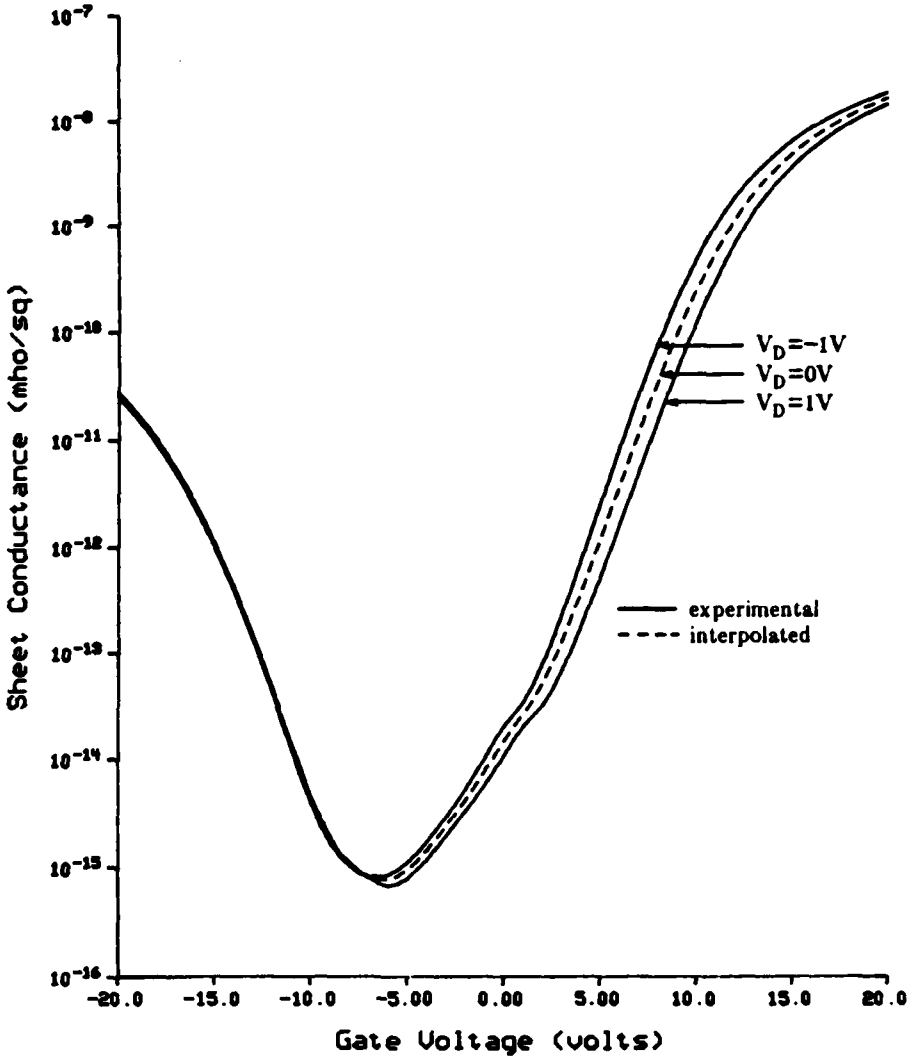

Figure 4.2 Sheet conductance functions for device 38-1(7,-1)110x1000: (a) solid-line - experimental data and (b) dashed-line - spline interpolated data.

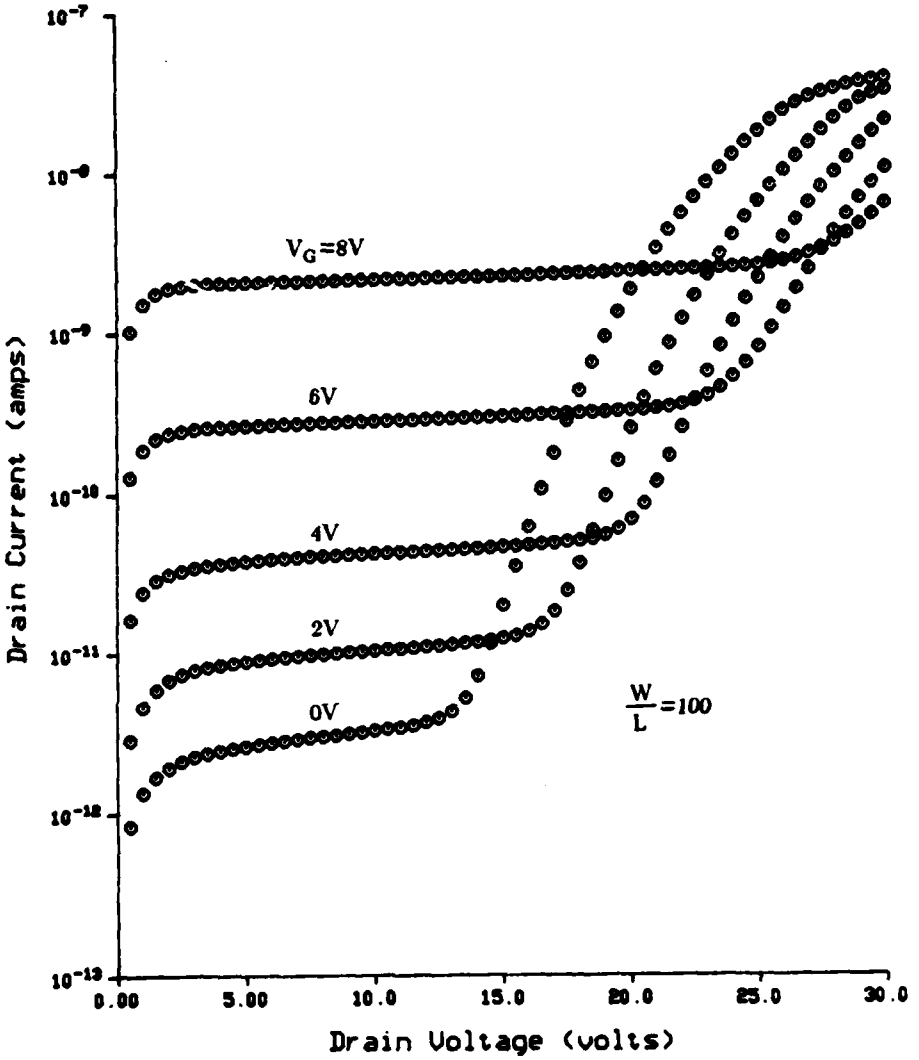

Figure 4.3 Experimental n-channel output drain characteristics of device 38-1(7,-1)I10x1000.

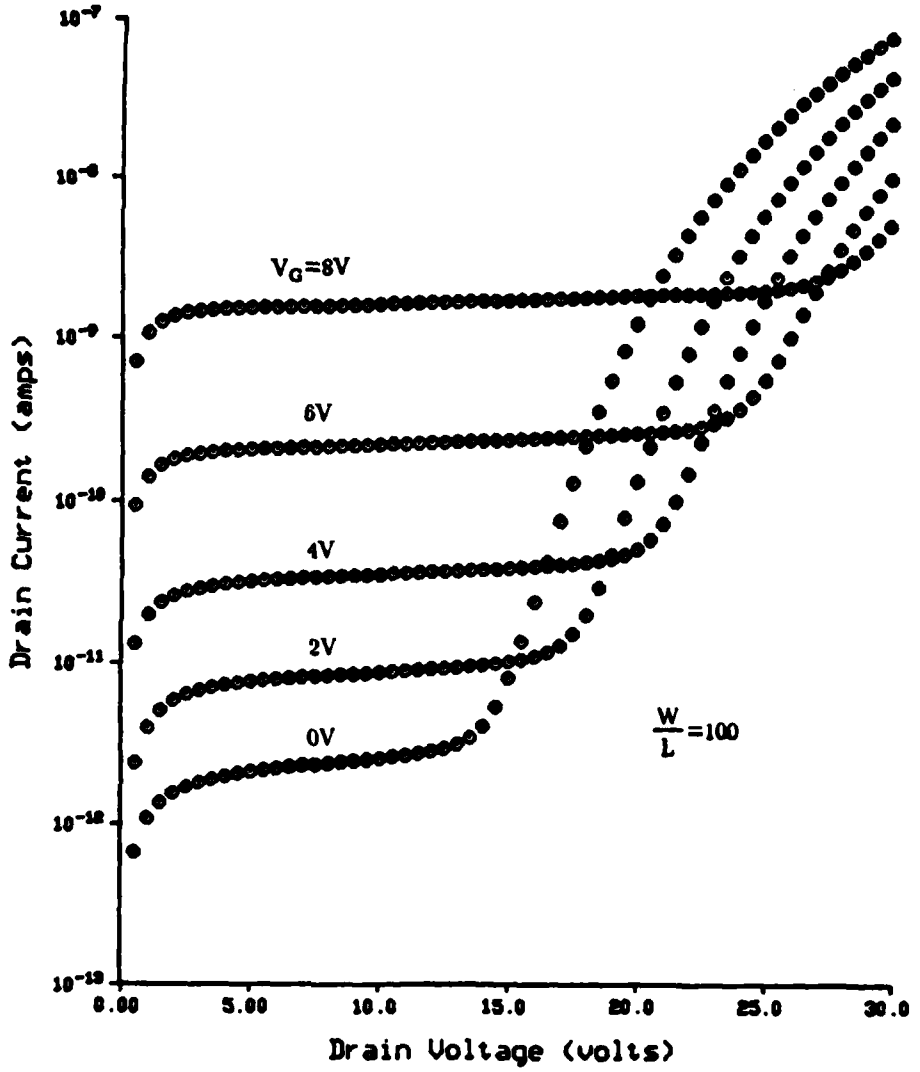

Figure 4.4 Experimental n-channel output drain characteristics of device 38-1(9,-2)I10x1000.

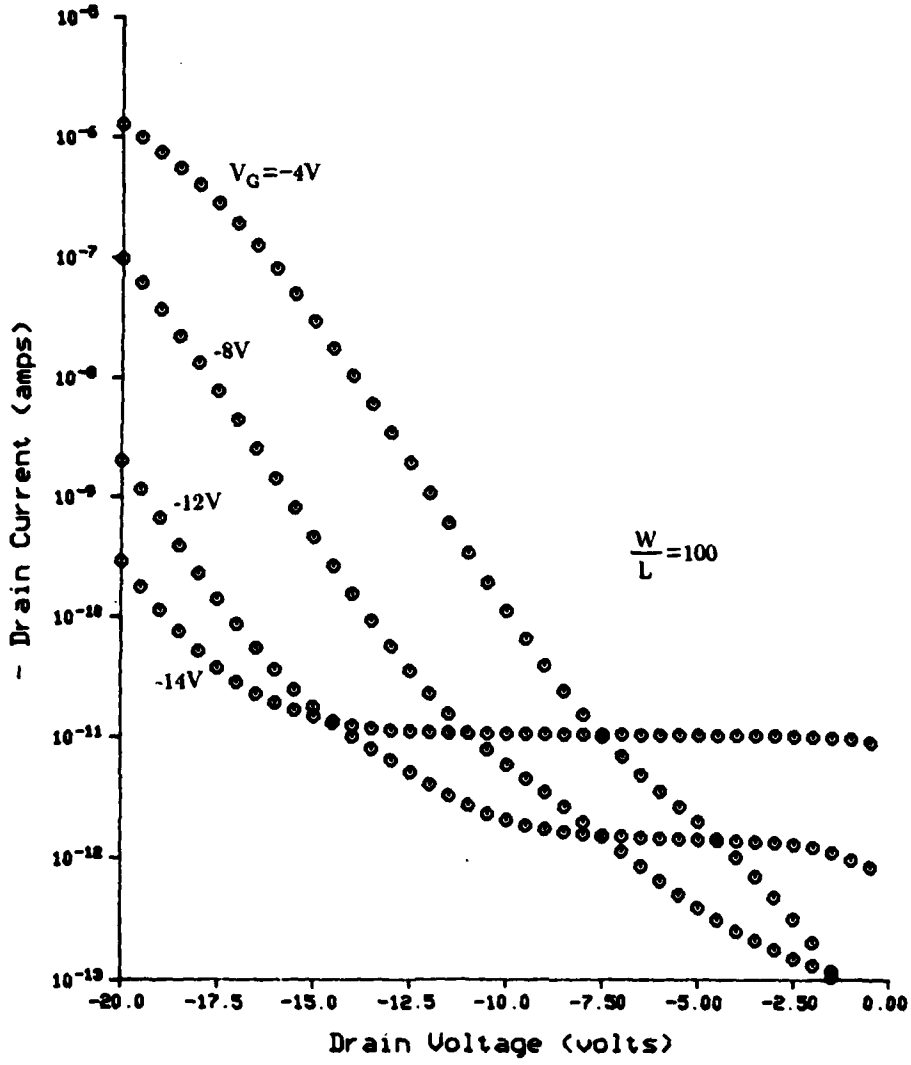

Figure 4.5 Experimental p-channel output drain characteristics of device 38-1(7,-1)I10x1000.

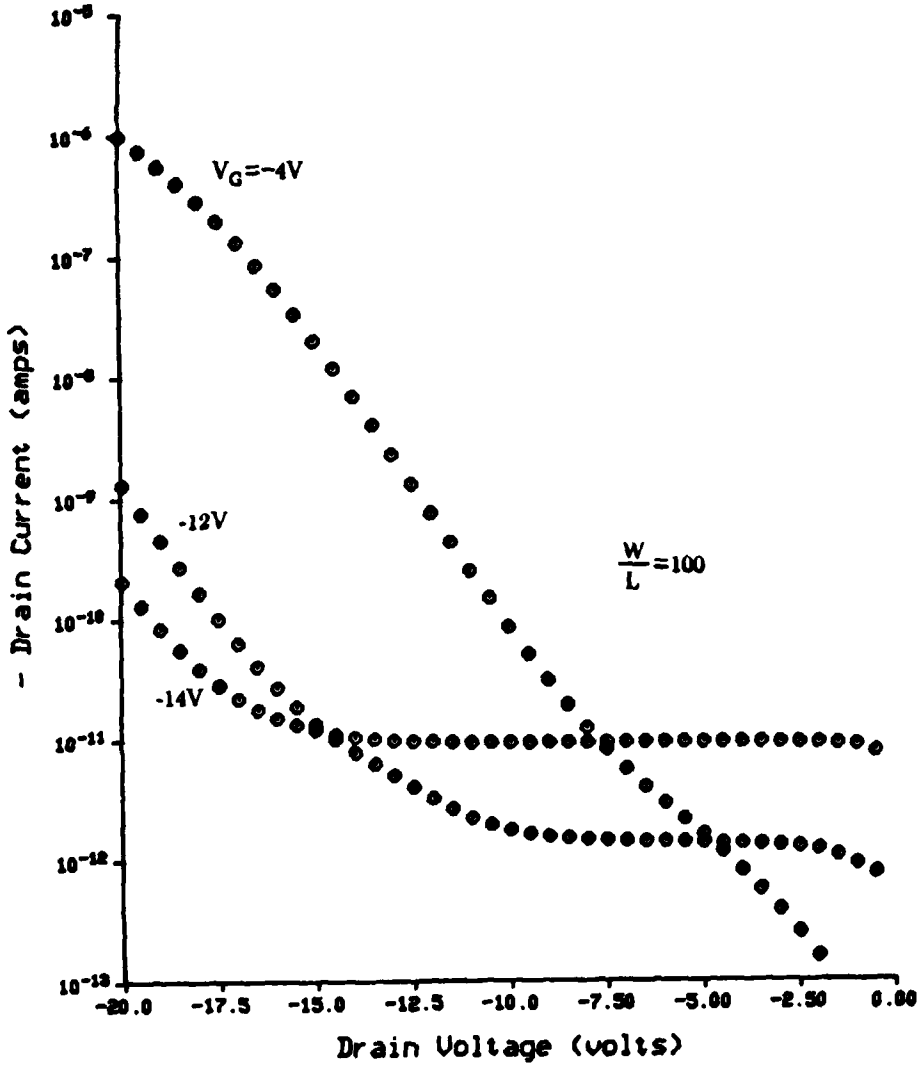

Figure 4.6 Experimental p-channel output drain characteristics of device 38-1(9,-2)I10x1000.

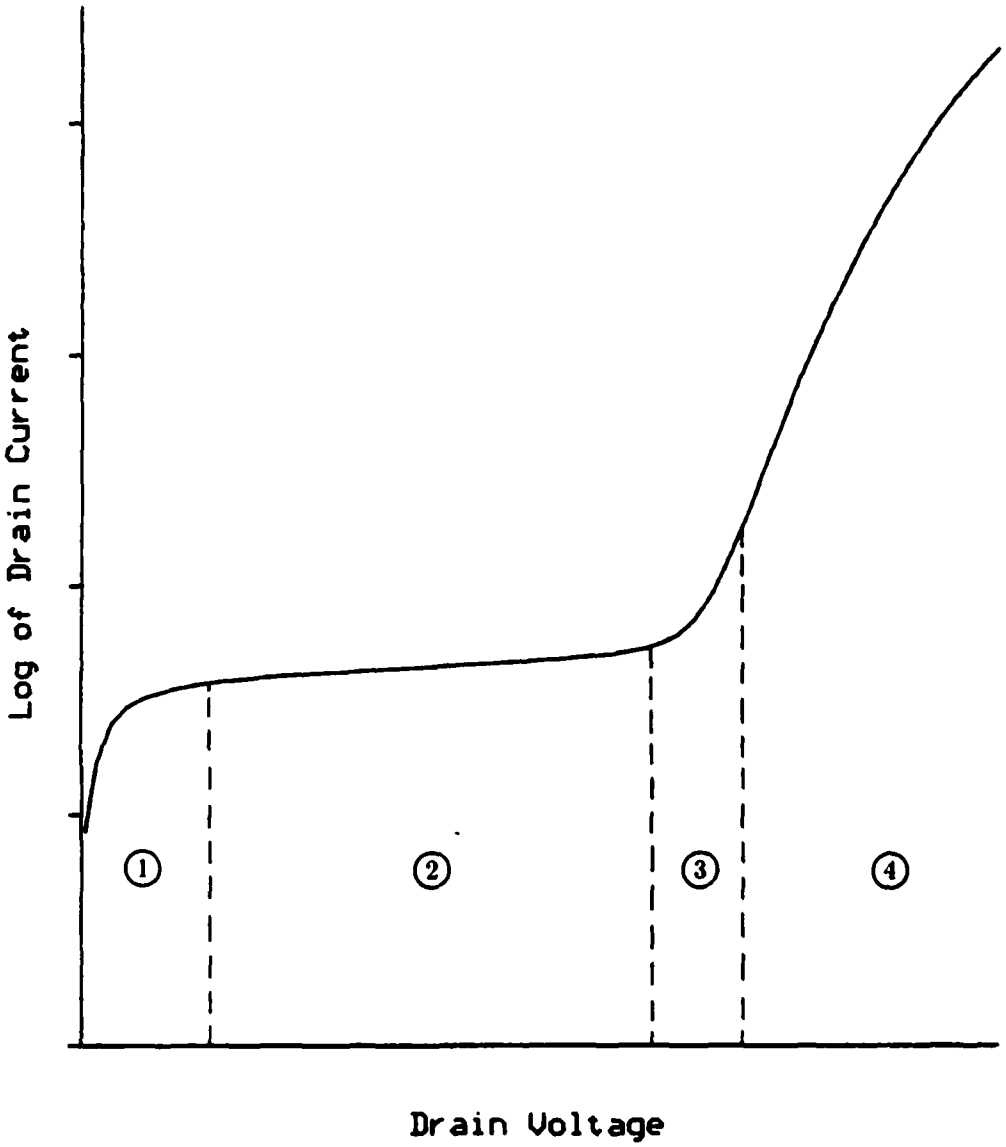

Figure 4.7 Ambipolar a-Si:H TFT regions of operation.

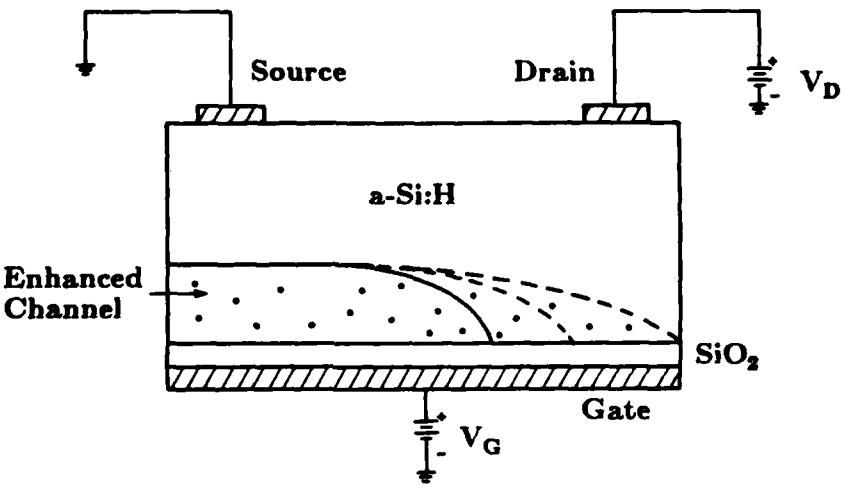

Figure 4.8 Enhanced electron channel of an a-Si:H TFT at pinch-off and beyond (dashed-lines show changing boundary of shrinking channel as V_D is changed).

is called the pinch-off voltage (V_P) and serves as the transition between the first and second regions of device operation.

In region 2, as V_D is increased beyond V_P, the electron current in the enhanced channel increases slightly because V_P is mildly dependent on V_D. While this electron current is increasing, the drain end of the enhanced channel is being depleted of electrons causing the enhanced electron channel to shrink towards the source (see Figure 4.8). Since the increase in V_D beyond V_P is applied between the drain and the end of the enhanced channel, the potential across the shrinking enhanced channel stays about the same, permitting the current to rise only slightly as V_D increases. In addition, the parallel current component through the bulk region of the device continues to increase slightly as the drain voltage is increased.

While the device is operating in region 2, an enhanced hole layer begins to form at the drain end of the device in the area previously occupied by the enhanced electron layer (see Figure 4.9). This hole layer forms as a result of the drain end potential being larger than the gate potential. A reversed biased situation then exists causing the formation of the enhanced hole layer. The effects of this hole layer are not observed in the device performance until the device enters region 3.

As the device enters region 3, the current begins to increase at a faster rate than in region 2. This increased rate is due to the superposition of the current flowing through the electron and hole layers. In this region, the dominant current carrier makes a transition from electron to hole, thereby demonstrating the ambipolar phenomena.

In region 4, the current initially increases exponentially and then tapers off. The initial increase is due to the p-channel being created by the drain to gate voltage (V_{DG}), while the gate to source voltage (V_{GS}) controls the n-channel conduction. Since V_{GS} does not change, the n-channel current increases very little. However, since V_D (and hence V_{DG}) increases, the p-channel conduction also increases resulting in the exponential current rise. The existence of a p-n diode at the a-Si:H interface where the enhanced electron and hole layers meet is of the correct polarity for I_D to continue to increase. The rate at which the current rises decreases as the localized state density at the band edges increases. This increased state density effectively reduces the ability of the Fermi energy to move, thereby reducing the rate at which current can increase through the device (i.e., less band bending per unit voltage).

By reversing the polarity of the applied biases and alternating the n- and p-channel device formation, a description similar to that given above could be

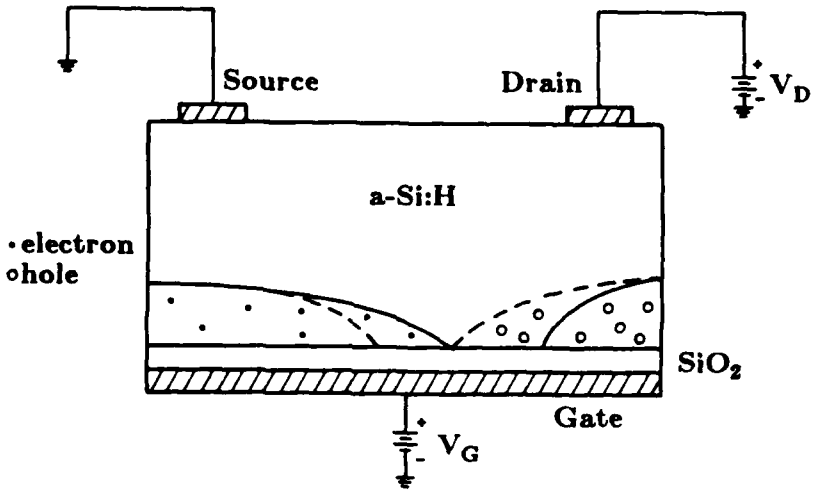

Figure 4.9 Shrinking electron and expanding hole layers in an ambipolar a-Si:H TFT beyond pinch-off (dashed-lines show changing boundaries of electron and hole layers as V_D is changed).

presented to explain the p-channel device output drain characteristics. Figure 4.4 contains an example of these characteristics.

4.4 Basic Model

As indicated in Section 2.3.2, the output drain characteristics of a TFT can be expressed as

$$I_D = (W/L) \int_{V_G-V_{FB}-V_D}^{V_G-V_{FB}} G_s(V)\, dV \tag{31}$$

where W/L is the device width to length ratio and V is the voltage across the gate insulator to the channel. Since $G_s(V)$ is only a function of voltage across the insulator and not of carrier type, equation (31) is applicable for ambipolar device operation. Hence, by integrating the $G_s(V)$ function and multiplying by W/L, the output drain characteristics can be realized.

To obtain a limited insight into the ambipolar operation of the TFT, consider modeling the $G_s(V)$ function as the sum of two exponentials, one for electron enhancement and one for hole enhancement:

$$G_s(V) = b_1 e^{a_1 V} + b_2 e^{a_2 V} \tag{32}$$

The "1" subscripts relate to electron enhancement and the "2" subscripts to hole enhancement. The constants a_1, b_1 and b_2 are positive while a_2 is negative. Using this $G_s(V)$ function in equation (1) yields

$$I_D = \frac{W}{L}\left\{\frac{b_1}{a_1} e^{a_1(V_G-V_{FB})}\left(1-e^{-a_1 V_D}\right) + \frac{b_2}{a_2} e^{a_2(V_G-V_{FB})}\left(1-e^{-a_2 V_D}\right)\right\} \tag{33}$$

When the enhanced channel is pinched-off at the drain end of the channel (i.e., no enhanced carriers are present at the drain end) and $V_G > V_{FB}$, then

$V_D=V_G-V_{FB}$. If $V_D=V_P$ when the channel is pinched-off then as V_D is increased beyond V_P, equation (33) becomes

$$I_D = \frac{W}{L}\left\{\frac{b_1}{a_1}e^{a_1V_P} - \frac{b_1}{a_1}e^{a_1(V_P-V_D)} + \frac{b_2}{a_2}e^{a_2V_P} - \frac{b_2}{a_2}e^{a_2(V_P-V_D)}\right\} \qquad (34)$$

In the n-channel mode of operation, V_D is positive. With a fixed gate voltage as V_D is increased beyond V_P, eventually the fourth term in equation (34), which relates to hole enhancement at the drain end, begins to dominate and I_D increases abruptly. (recall that a_2 is negative because hole enhancement corresponds to the negatively sloped portion of the $G_s(V)$ function). Thus, the ambipolar operation of the device is clearly seen in the output drain characteristics at large values of V_D as shown in Figures 4.3 and 4.4. This sharp rise in I_D corresponds to the device leaving predominantly n-channel operation and switching to predominantly p-channel ambipolar operation. A similar argument applies to the p-channel mode of operation where V_D and V_G are negative.

In using equation (31) to model ambipolar a-Si:H TFT performance, the $G_s(V)$ function (dashed-line of Figure 4.2) was obtained by interpolating from four equally spaced transfer curves to V_D = 0V. A trapazoidal numerical integration technique was then used to integrate the $G_s(V)$ curve to obtain the modeled output drain characteristics shown by the solid-line curves in Figures 4.10, 4.11, 4.12 and 4.13. Notice that for the n-channel output characteristics of Figures 4.10 and 4.11, the modeled I_D follows the magnitude and shape of the experimental I_D quite well up to where I_D rises sharply. Then the modeled I_D consistently begins to rise sharply at a value of V_D lower than the experimental I_D, but still follows the general shape quite well. Interestingly enough, the difference in V_D between where the two sharp I_D increases occur in each figure, seems to correspond to the difference in the flat-band voltages of the n-channel (V_{FBn}) and p-channel (V_{FBp}) devices seen in Figure 4.1 for device 38-1(7,-1) and in Figure 4.14 for device 38-1(9,-2).

In looking at the p-channel output characteristics of Figures 4.12 and 4.13, the modeled I_D follows the general shape and magnitude of the experimental I_D at low $|V_G|$. However, the model seems to fall off at higher $|V_G|$ where the experimental I_D is saturated, just before the devices switch from predominantly p-channel operation to predominantly n-channel operation.

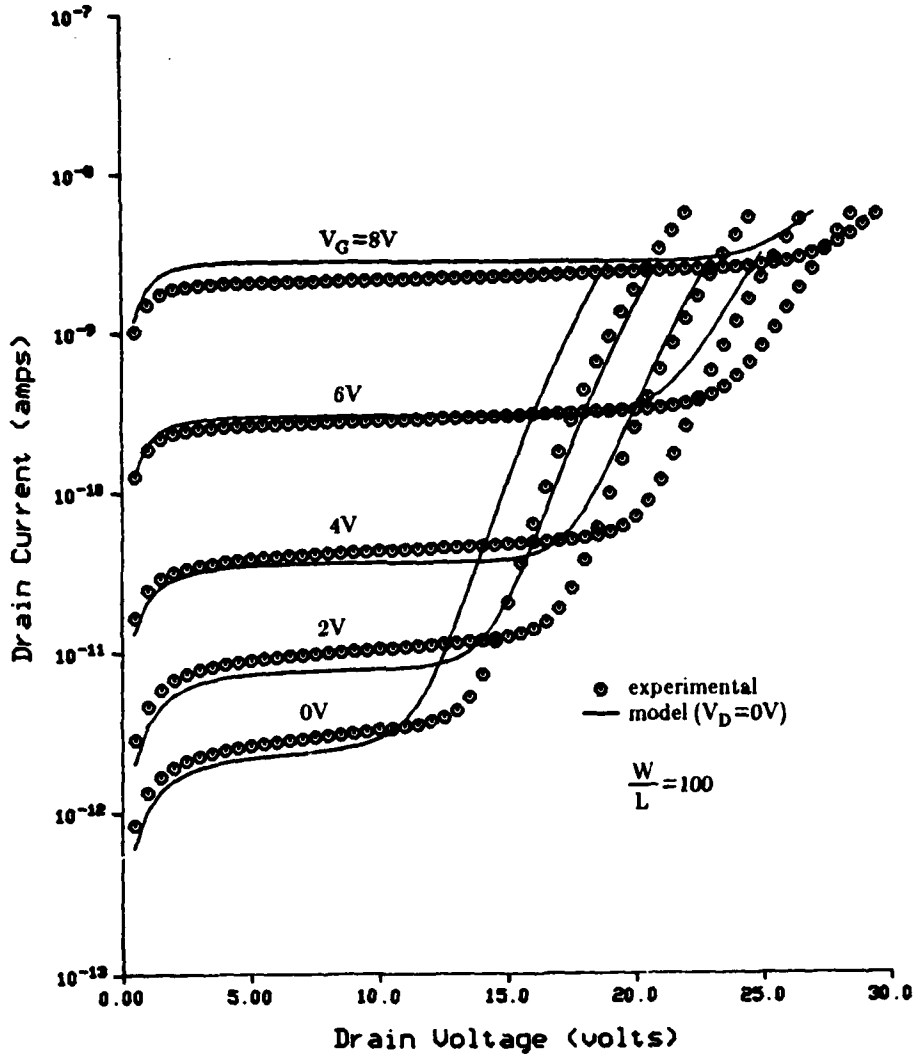

Figure 4.10 Experimental and modeled n-channel output drain characteristics of device 38-1(7,-1)I10x1000: (a) circles - experimental data and (b) solid-line - modeled data.

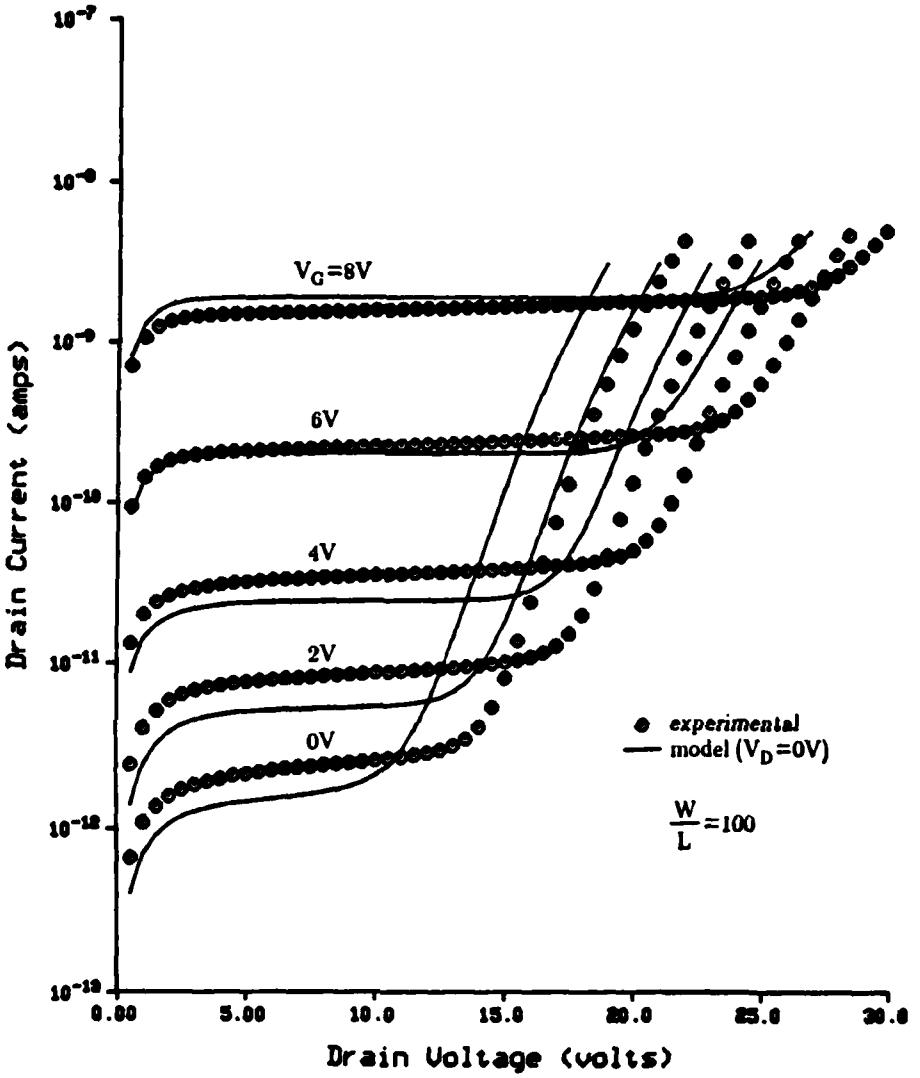

Figure 4.11 Experimental and modeled n-channel output drain characteristics of device 38-1(9,-2)I10x1000: (a) circles - experimental data and (b) solid-line - modeled data.

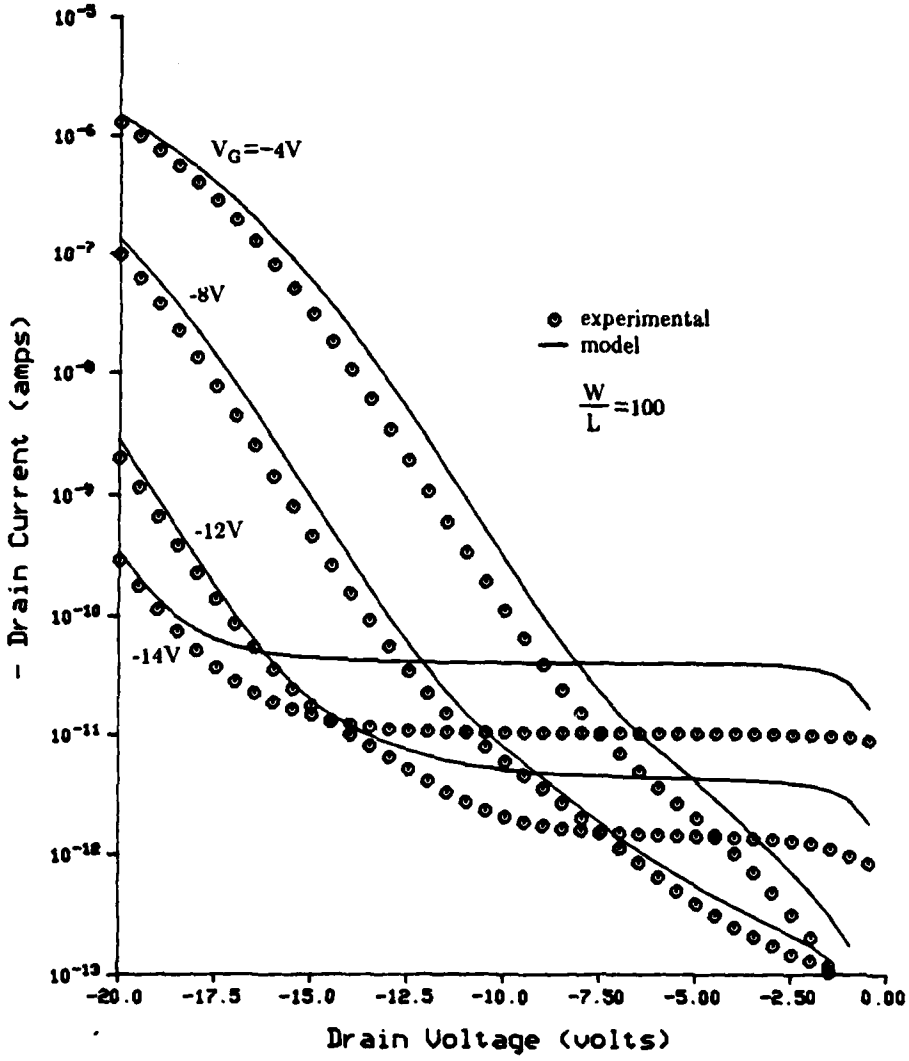

Figure 4.12 Experimental and modeled p-channel output drain characteristics of device 38-1(7,-1)I10x1000: (a) circles - experimental data and (b) solid-line - modeled data.

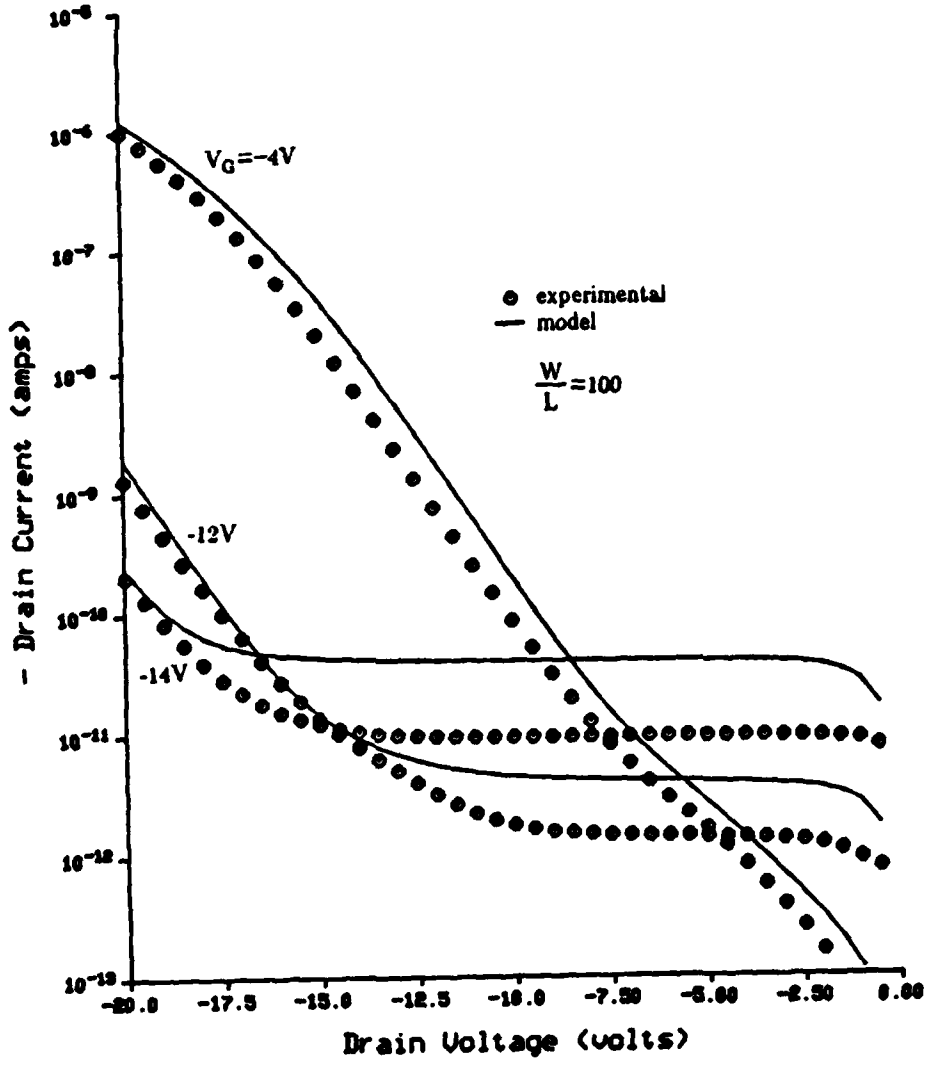

Figure 4.13 Experimental and modeled p-channel output drain characteristics of device 38-1(9,-2)I10x1000: (a) circles - experimental data and (b) solid-line - modeled data.

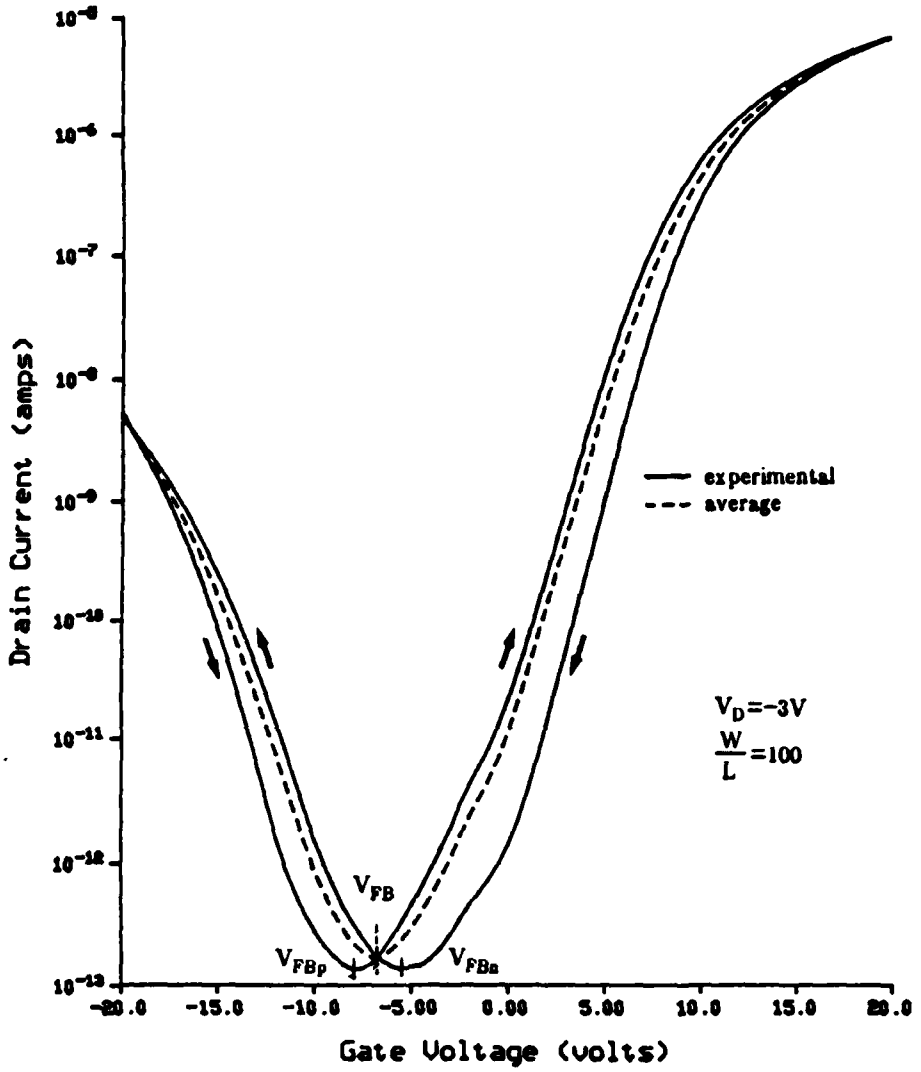

Figure 4.14 Experimental transfer curve for device 38-1(9,-2)I10x1000: (a) solid-line - forward and reverse measurement sweeps and (b) dashed-line - average of forward and reverse sweeps.

During this investigation, a brief study was conducted to verify the necessity of using an interpolated $G_s(V)$ function. Since the process involved in obtaining the interpolated $G_s(V)$ curve for $V_D = 0V$ is rather cumbersome compared to simply measuring a single G_s (V) curve at one, low V_D, a comparison was made between the output curves modeled from these two different sheet conductance functions. As shown in Figure 4.2, a noticeable variation exists between the interpolated and two of the experimental sheet conductance curves. Since these curves do not coincide, a different output drain curve was expected. This expectation was confirmed as shown in Figure 4.15. When the interpolated $G_s(V)$ curve was used in equation (31), the solid-line curves shown in Figure 4.15 resulted. In comparison, when a $G_s(V)$ curve measured at $V_D = 1V$ was used, the dashed-line curves of Figure 4.15 resulted. Clearly, the interpolated data gave a better fit between the simple theory and experimental data than did the uninterpolated data. Thus, the interpolated $G_s(V)$ curve was determined to be the desired function for use in equation (31).

4.5 Improved Model

In order to obtain a better match between the experimental data and the model described by equation (31), further consideration was given to the $G_s(V)$ function. Recall that this function was derived from I_D measurements averaged between forward and reverse gate voltage sweeps (See Figures 4.1 and 4.14). Although this averaging was done to compensate for the V_{FB} difference between n- and p-channel devices, it effectively gave the same V_{FB} to both type devices. As seen in Figures 4.1 and 4.14, and elsewhere[97], the n- and p-channel devices have different V_{FB} (See V_{FBn} and V_{FBp} in Figures 4.1 and 4.14).

Incorporating this V_{FB} difference into the interpolated $G_s(V)$ function yields a better match between the experimental data and the model described by equation (31) , particularly for the n-channel device. One procedure for incorporating the V_{FB} difference consists of breaking the interpolated $G_s(V)$ curve into two regions; $G_s(V)$ for $V > V_{FB}$ and $G_s(V)$ for $V < V_{FB}$ (See the solid-line curve of Figures 4.16 and 4.17). For $V > V_{FB}$, the $G_s(V)$ curves are used as shown. For $V < V_{FB}$, the $G_s(V)$ curves are altered by extending the $G_s(V)$ value at V_{FB} to $V_{FB} - \Delta V_{FB}$ where $\Delta V_{FB} = (V_{FBn} - V_{FBp})$. The $G_s(V)$ curves are shifted in the negative V_G direction by ΔV_{FB}. The resulting shifted $G_s(V)$ curves are shown by the dashed-lines in Figures 4.16 and 4.17. When these shifted curves are used in equation (31), the dashed-line curves of Figures 4.18, 4.19, 4.20 and 4.21 result.

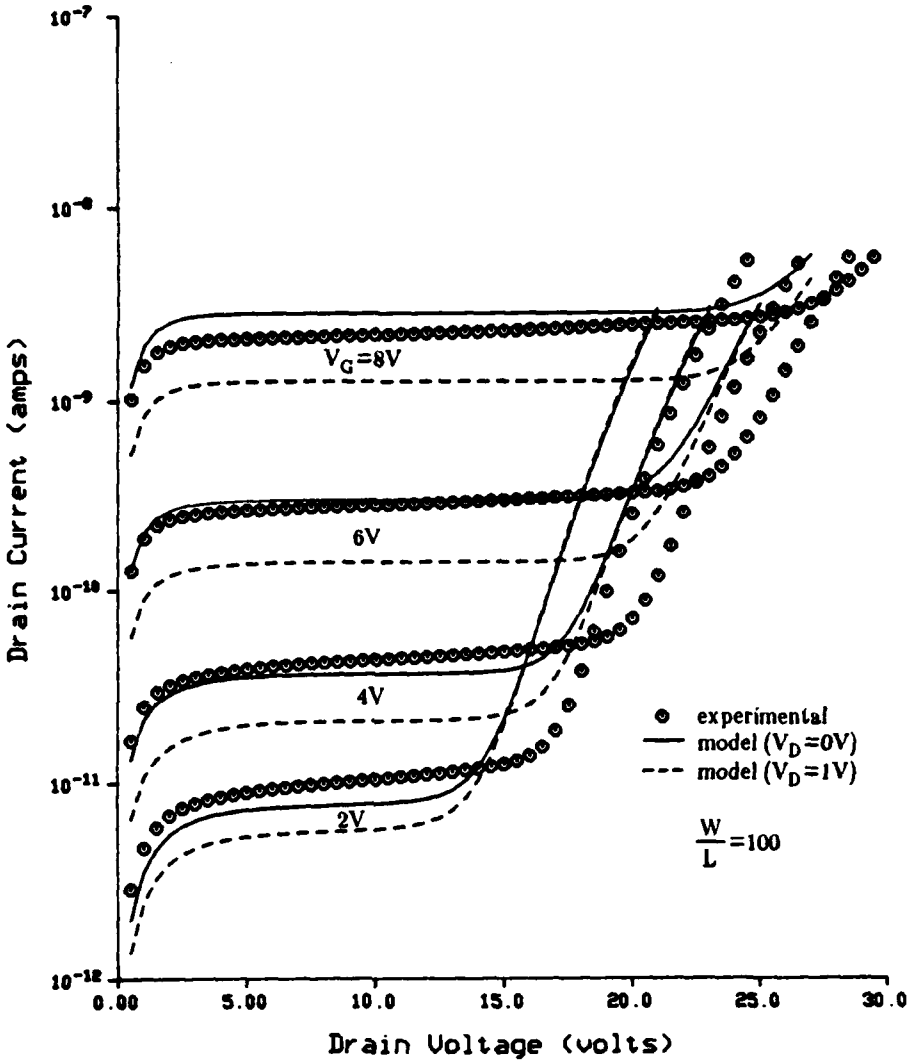

Figure 4.15 Experimental and modeled n-channel output drain characteristics of device 38-1(7,-1)I10x1000: (a) circles - experimental data, (b) solid-line - modeled data using a sheet conductance function interpolated to V_D = 0V, and (c) dashed-line - modeled data using a sheet conductance function determined from measurements at V_D = 1V.

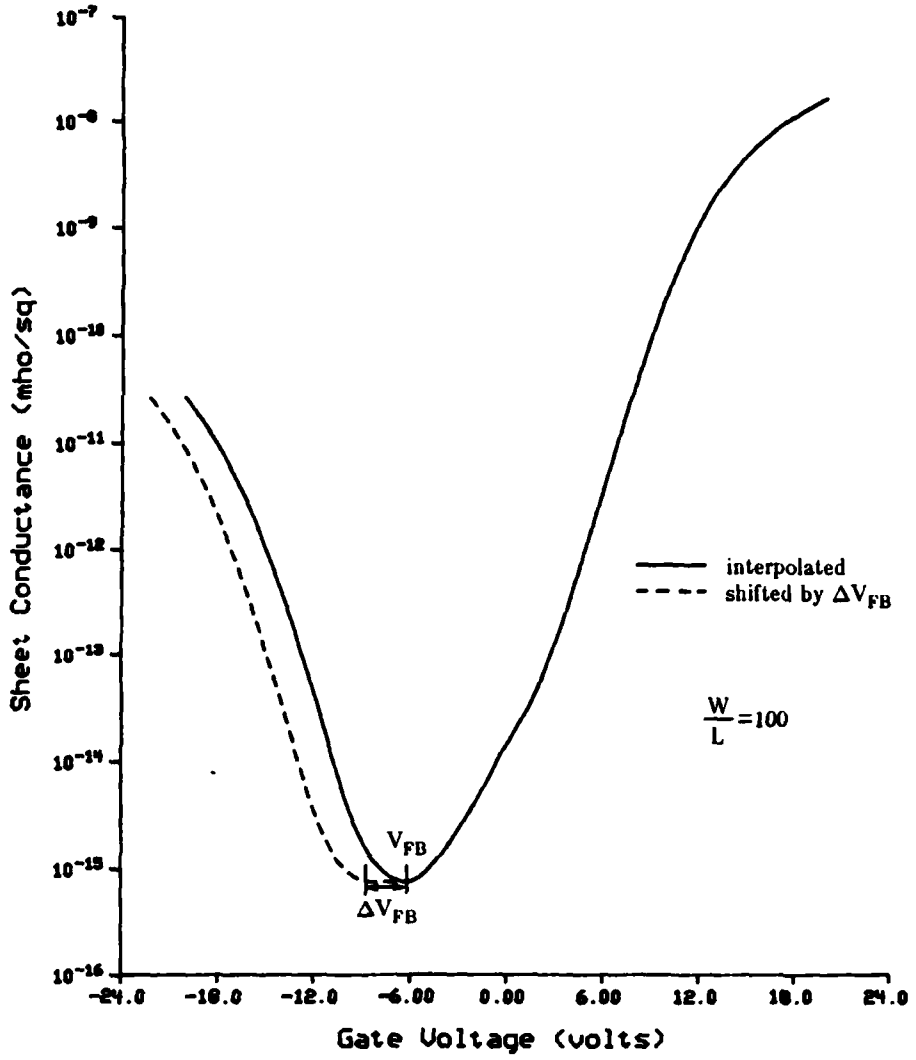

Figure 4.16 Sheet conductance functions for device 38-1(7,-1)I10x1000: (a) solid-line - interpolated sheet conductance with no shift and (b) dashed-line - interpolated sheet conductance shifted by the difference in the n- and p-channel device V_{FB}'s.

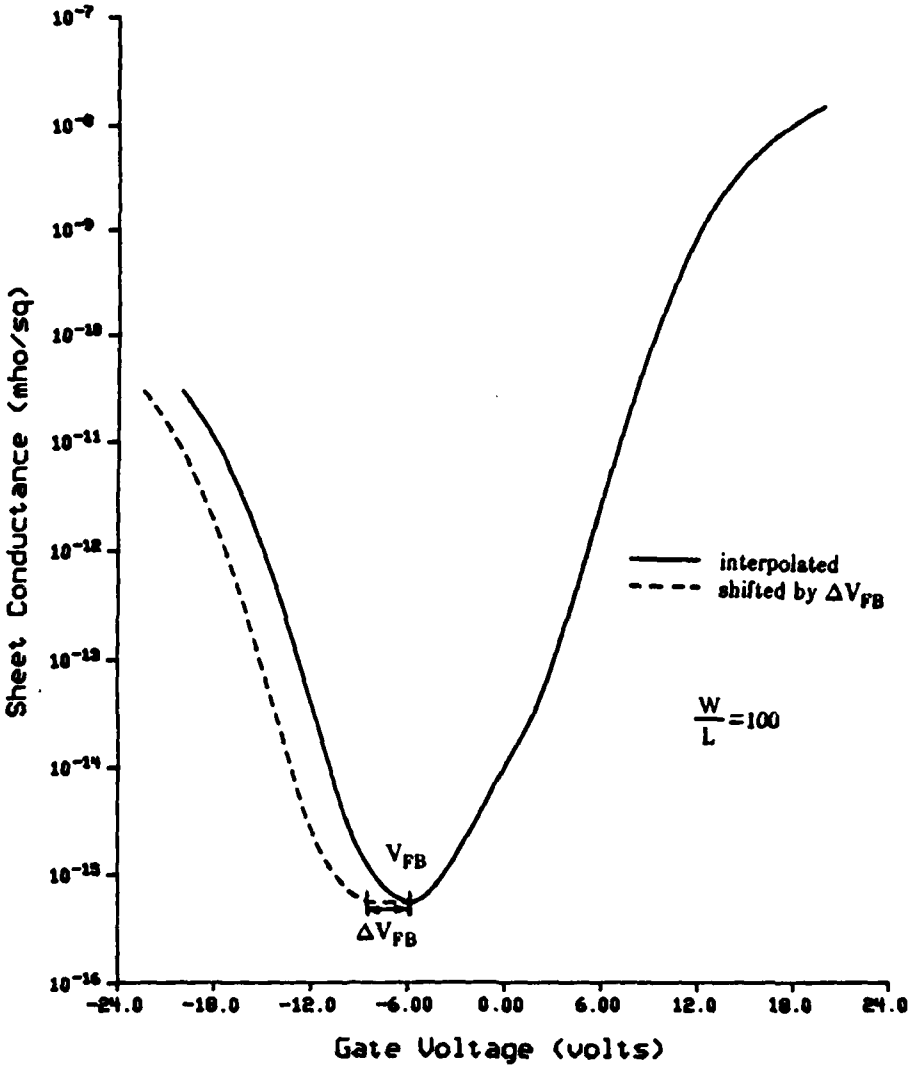

Figure 4.17 Sheet conductance functions for device 38-1(9,-2)110x1000: (a) solid-line - interpolated sheet conductance with no shift and (b) dashed-line - interpolated sheet conductance shifted by the difference in the n- and p-channel device V_{FB}'s.

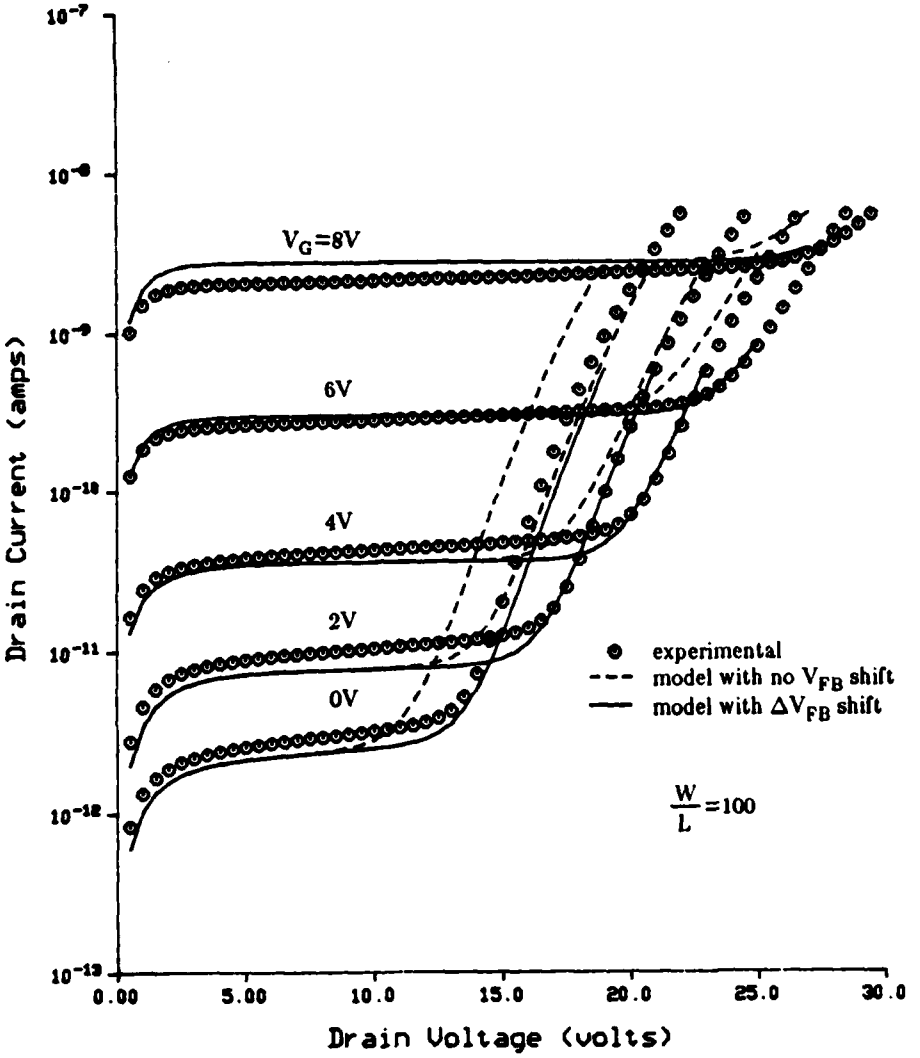

Figure 4.18 Experimental and modeled n-channel output drain characteristics for device 38-1(7,-1)I10x1000: (a) circles - measured data, (b) dashed-line - modeled data with no shift in the sheet conductance function, and (c) solid-line - modeled data with the sheet conductance function shifted by the difference in the n- and p-channel device V_{FB}'s.

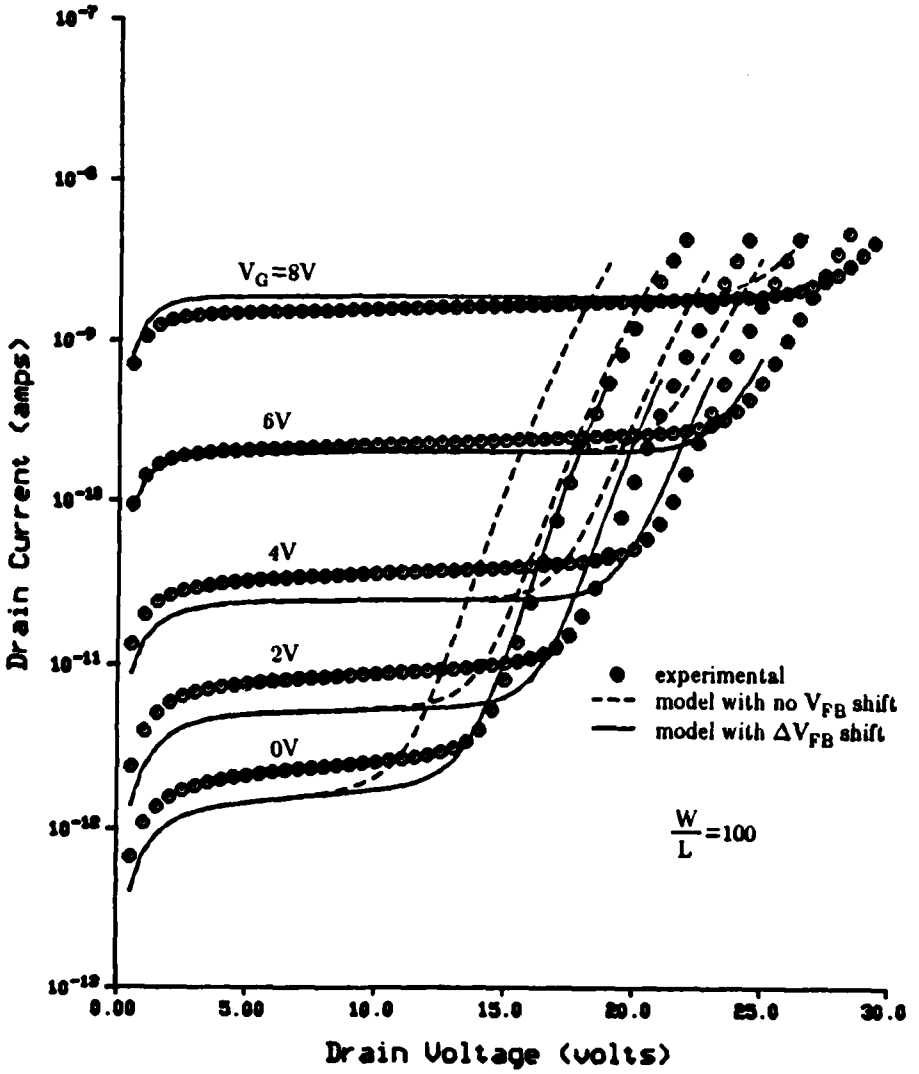

Figure 4.19 Experimental and modeled n-channel output drain characteristics for device 38-1(9,-2)I10x1000: (a) circles - measured data, (b) dashed-line - modeled data with no shift in the sheet conductance function, and (c) solid-line - modeled data with the sheet conductance function shifted by the difference in the n- and p-channel device V_{FB}'s.

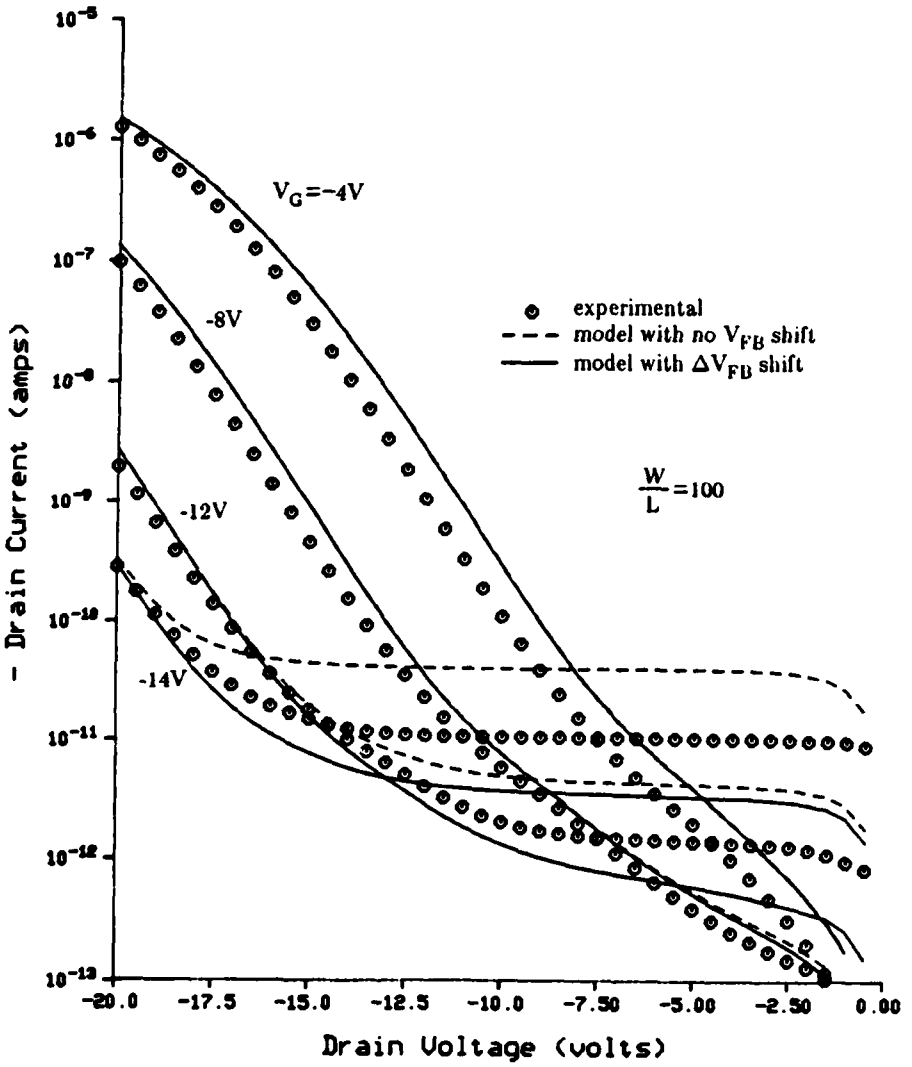

Figure 4.20 Experimental and modeled p-channel output drain characteristics for device 38-1(7,-1)I10x1000: (a) circles - measured data, (b) dashed-line - modeled data with no shift in the sheet conductance function, and (c) solid-line - modeled data with the sheet conductance function shifted by the difference in the n- and p-channel device V_{FB}'s.

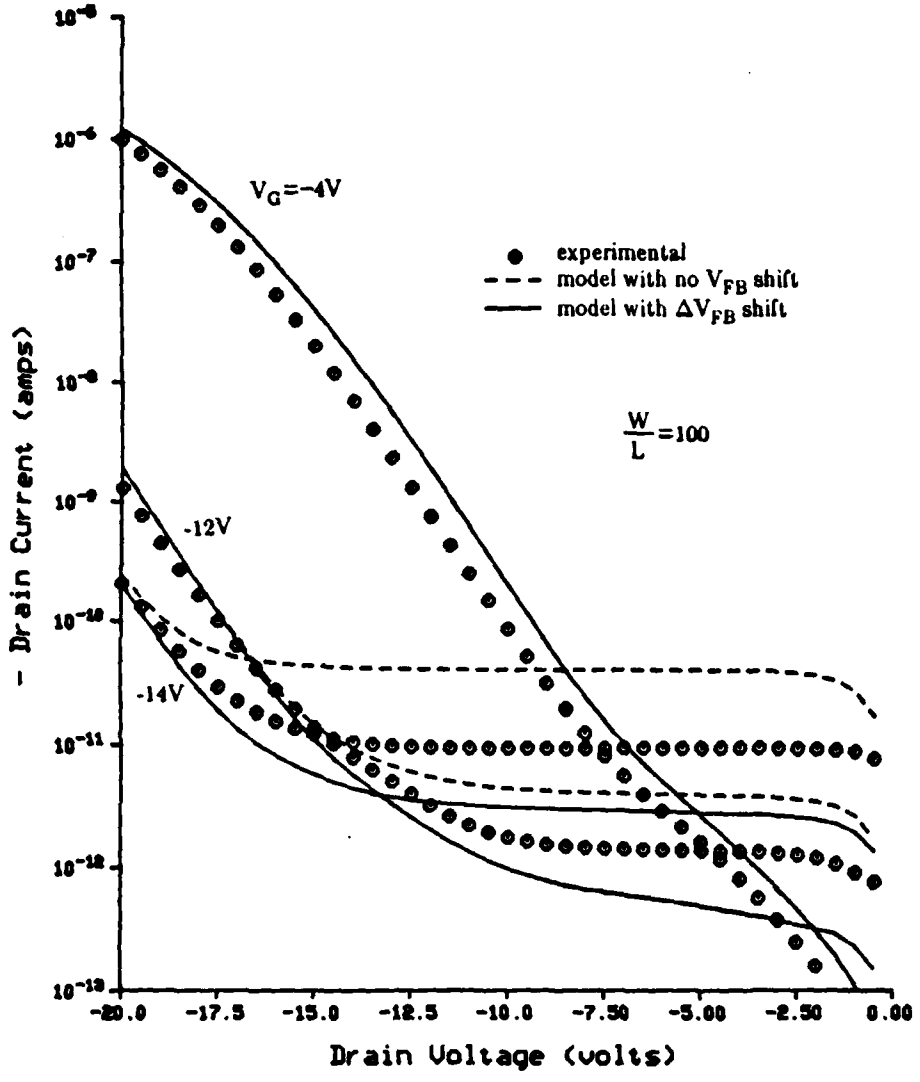

Figure 4.21 Experimental and modeled p-channel output drain characteristics for device 38-1(9,-2)I10x1000: (a) circles - measured data, (b) dashed-line - modeled data with no shift in the sheet conductance function, and (c) solid-line - modeled data with the sheet conductance function shifted by the difference in the n- and p-channel device V_{FB}'s.

In examining Figures 4.18 and 4.19 for the n-channel device, the solid-line curves obtained using the shifted $G_s(V)$ curve match the experimental data much better, especially after the opposite channel device is formed, than the dashed-line curves obtained using the unshifted $G_s(V)$ curve. Thus, shifting $G_s(V)$ by the difference between V_{FBn} and V_{FBp} yields an excellent match between the experimental and modeled output drain curves for the n-channel device.

In examining Figures 4.20 and 4.21 for the p-channel device, the solid-line curves obtained using the shifted $G_s(V)$ curve do not match the experimental data any better than the dashed-line curves obtained using the unshifted $G_s(V)$ curve. Both sets of modeled curves match the experimental curves fairly well in the unsaturated I_D regions and after the opposite device type is formed. However, in the saturated I_D region, the solid-line curves of Figure 14 obtained from the shifted $G_s(V)$ curve are below the experimental I_D values, while the dashed-line curves obtained from the unshifted $G_s(V)$ curve are above the experimental I_D values.

CHAPTER 5
CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE RESEARCH

5.1 Conclusions

This investigation has examined the ambipolar behavior of a-Si:H thin film transistors through the development of an a-Si:H TFT process sequence and subsequent modeling effort. Essential to the process development was the use of high quality a-Si:H films, ohmic source/drain contacts, and a high quality gate insulator. Such features were necessary to insure state-of-the-art devices which were capable of both n- and p-channel operation at reasonable voltage levels.

The high quality films were achieved using an improved set of optimized a-Si:H deposition parameters. These parameters consisted of the RF power level, substrate temperature, pressure and silane concentration used in the glow discharge deposition technique. The initial set of optimized parameters were determined through a series of parameter variation experiments which yielded the highest resistivity a-Si:H films. Simple TFTs were then fabricated with these high resistivity films and shown to possess acceptable performance characteristics. After the other process steps were completed, some additional adjustments were made to the optimized deposition parameters to insure the best device performance. These adjustments resulted in an improved set of deposition parameters which were used to fabricate the devices for the subsequent modeling effort.

The ohmic source/drain contacts resulted from a series of experiments which investigated the effect of the metal/a-Si:H contact scheme on TFT performance. These experiments demonstrated that ion implantation was an effective technique to dope the source/drain contact regions. In particular, by using a heated double-level P^+ ion implant scheme, a BHF dip to clean off the a-Si:H surface immediately preceding the Al metal deposition and a 200 °C anneal in dry N_2, contacts of sufficient quality could be made to the source/drain regions of a-Si:H TFTs.

The high quality gate insulator was obtained through the use of thermally grown SiO_2. Such an oxide has an inherently low fixed charge which, unlike an SiN_x insulator, allows for the formation of a p-channel device at reasonable voltage levels; a necessary requirement for practical ambipolar device operation. In addition, thermally grown SiO_2 is preferred for basic TFT research investigations because it permits small leakage currents and minimizes the effects of the insulator/a-Si:H interface trap density on device performance.

In addition, it was necessary to develop a technique to pattern a layer of a-Si:H into individual regions on a SiO_2 surface. Such a technique permitted the isolation of a-Si:H TFTs from one another on the same insulating substrate. The technique developed consisted of patterning the a-Si:H layer with photoresist and etching in a solution of H_3PO_4:HNO_3:HF =60:5:1 by volume. This technique was used to successfully define 5μm lines and spaces.

The performance of a-Si:H TFTs fabricated with the final process sequence was comparable to that observed for similar TFTs reported in the literature. In addition, the devices clearly displayed the desired ambipolar behavior. Hence, performance data measured on these devices was acceptable for use in the subsequent modeling effort.

The modeling of the ambipolar a-Si:H TFTs proceeded from basic TFT theory. The output drain characteristics of these devices were predicted quite simply and accurately by numerically integrating a spline-interpolated sheet conductance function obtained from averaged drain current measurements. An uninterpolated sheet conductance function yielded less accurate results.

The model was improved by including the effects of the different n- and p-channel device flat-band voltages in the interpolated sheet conductance function. By comparing the results of using the shifted and unshifted $G_s(V)$ curves, the importance of V_{FB} in modeling ambipolar a-Si:H TFTs was demonstrated. The improved model showed good agreement and consistency with experimental output drain characteristics over many orders of magnitude of I_D and for both electron and hole currents from a single sheet conductance function.

5.2 Recommendations for Future Research

The investigation described in this thesis has laid the foundation for additional research into the study of the ambipolar a-Si:H thin film transistor. In particular, additional work needs to be done in the areas of ambipolar device fabrication improvements and circuit applications.

Although the ambipolar devices fabricated with the final process sequence developed in this investigation are state-of-the-art, improvements are still desirable. For example, a non-interdiffusing metallization scheme would decrease the source/drain contact resistance, thereby permitting higher current levels in the devices. Candidates for this metallization include Cr-Au and Ti-Al. As described in Section 3.5, an improved contact scheme would then permit the use of a SiN_x passivation layer to protect the devices from harmful environmental effects.

Ion implanting the source/drain regions at three or more levels, instead of just the two used in the final process sequence, should also be investigated. With more dopant in the a-Si:H, the potential energy barrier at the metal/a-Si:H interface would be reduced from its present level. These additional implants would also have the effect of bringing the source/drain regions closer to the enhanced channel, thereby reducing the volume of intrinsic a-Si:H carriers must pass through as they traverse a device. Hence, higher current levels could be achieved.

Although thermal SiO_2 is the best insulator for a-Si:H TFTs, it is not practical for device applications such as switching elements in large area liquid crystal display arrays. Work needs to be done to develop an insulator with lower fixed charge than that currently observed in a-Si:H TFTs with glow discharge SiN_x and SiO_2 insulators. Perhaps a simple series of deposition parameter adjustment experiments would yield a reduced fixed charge which would permit ambipolar device operation at reasonable voltage levels.

With the demonstration of the ambipolar behavior in a-Si:H TFTs, the way has been opened for using this behavior in circuit applications. The ability to obtain both n- and p-channel device operation from the same device by merely changing the gate voltage polarity should lead to useful circuit configurations. For example, using a circuit topology scheme similar to complementary metal oxide semiconductor (CMOS) circuits, various digital logic functions could be realized. In addition, novel circuit design schemes could be developed which further exploit the ambipolar behavior. Hence, assuming acceptable circuit performance, the ambipolar behavior should lead to a greater utilization of a-Si:H TFTs.

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APPENDICES

Appendix A

GLODAS Test Pattern

This appendix contains information about the test structures located on the GLODAS test pattern. In particular, Table A.1 contains a list of test structures and corresponding probe pads. Figure A.1 shows the probe pad locations on the GLODAS pattern. Figures A.2, A.3 and A.4 are pen plots of GLODAS areas A, B and C, respectively. Note that the thin film transistors are referred to by the electrode type ("D" for interdigitated, "R" for rectangular), channel length and width (in micrometers), and implanted ("I") or unimplanted (no designation) source/drain regions. Thus, the designation R10x500I refers to a TFT with a rectangular electrode structure, drawn channel length and width of 10μm and 500μm, respectively, and implanted source/drain regions.

Table A.1 GLODAS test structures and corresponding probe pads.

Pad	Test Structure
A1	R10x500
A2	R10x200
A3	D10x84
A4	Common Source (Area A only)
A5	R10x100
A6	R10x1000
A7	D10x472
A8	R10x50
A9	D10x952
A10	R10x150
A11	D10x138
A12	R5x25
A13	Common Gate (entire pattern)
A14	R10x25
A15	D10x178
A16	D10x178
B1	Common Gate (entire pattern)
B2-B5	Intrinsic a-Si Van der Pauw (100x100μm)
B6	Intrinsic a-Si/substrate capacitor ($1.44x10^{-6}cm^2$)
B7	Intrinsic a-Si resistivity structure (10x10940μm)
B8	Intrinsic a-Si resistivity structure (10x10940μm)
B9	Common for resistivity structures
B10	Implanted a-Si resistivity structure (10x486μm)
B11	Implanted a-Si/substrate capacitor ($1.44x10^{-6}cm^2$)
B12	Metal/substrate capacitor ($1.44x10^{-6}cm^2$)

Table A.1 (continued).

Pad	Test Structure
C1	R10x500I
C2	R10x200I
C3	D10x84I
C4	Common Source (Area C only)
C5	R10x100I
C6	R10x1000I
C7	D10x472I
C8	R10x50I
C9	D10x952I
C10	R10x150I
C11	D10x138I
C12	R5x25I
C13	Common Gate (entire pattern)
C14	R10x25I
C15	D10x178I
C16	D10x178I

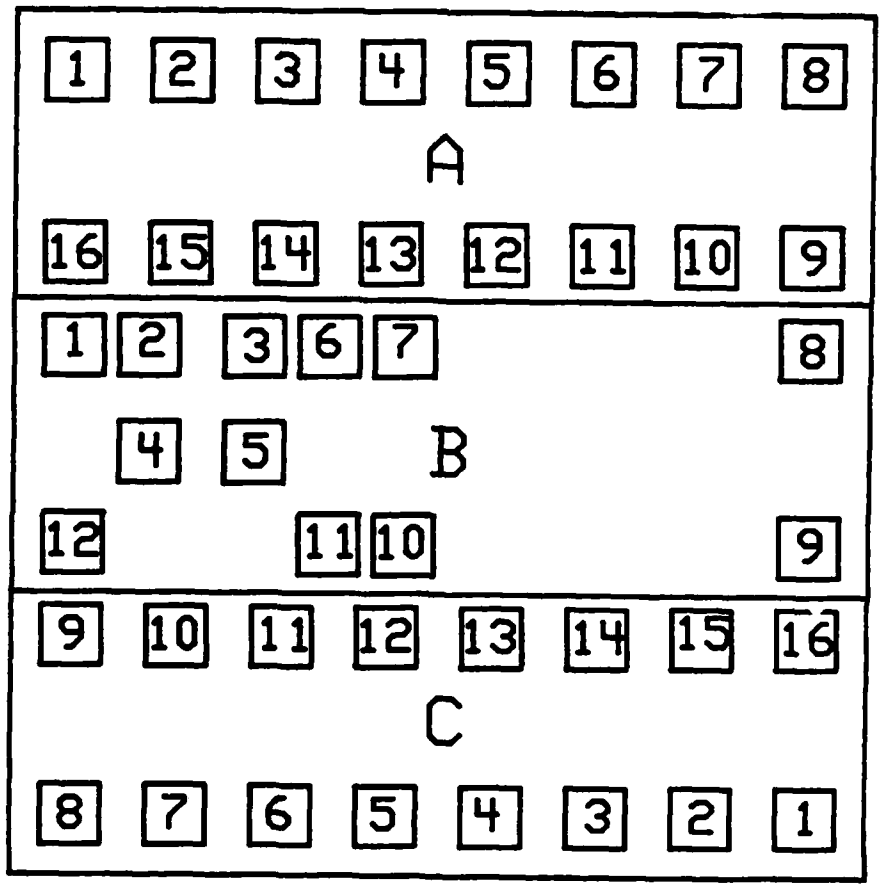

Figure A.1 GLODAS probe pad locator diagram.

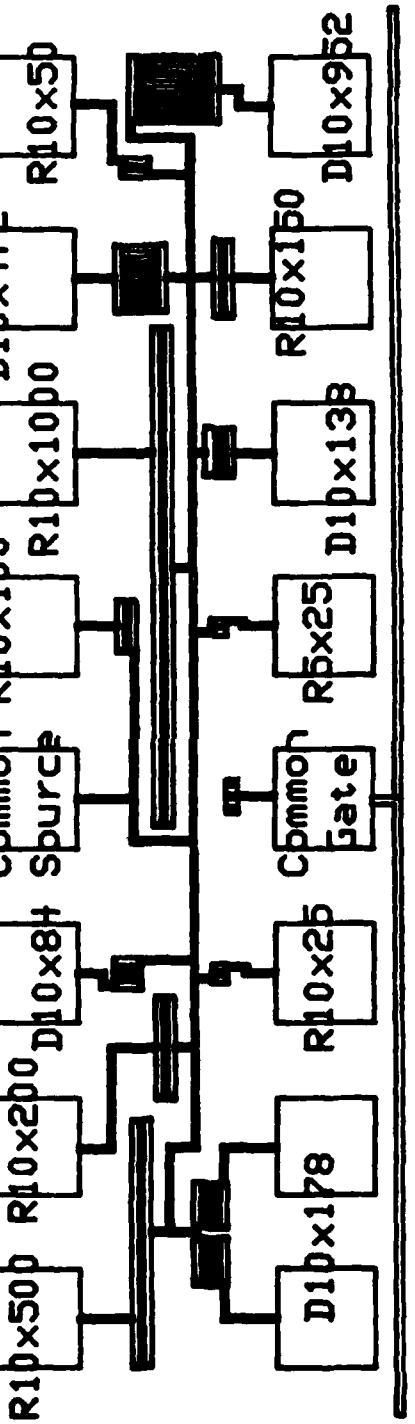

Figure A.2 Area A of GLODAS test pattern (all devices contain undoped source/drain regions).

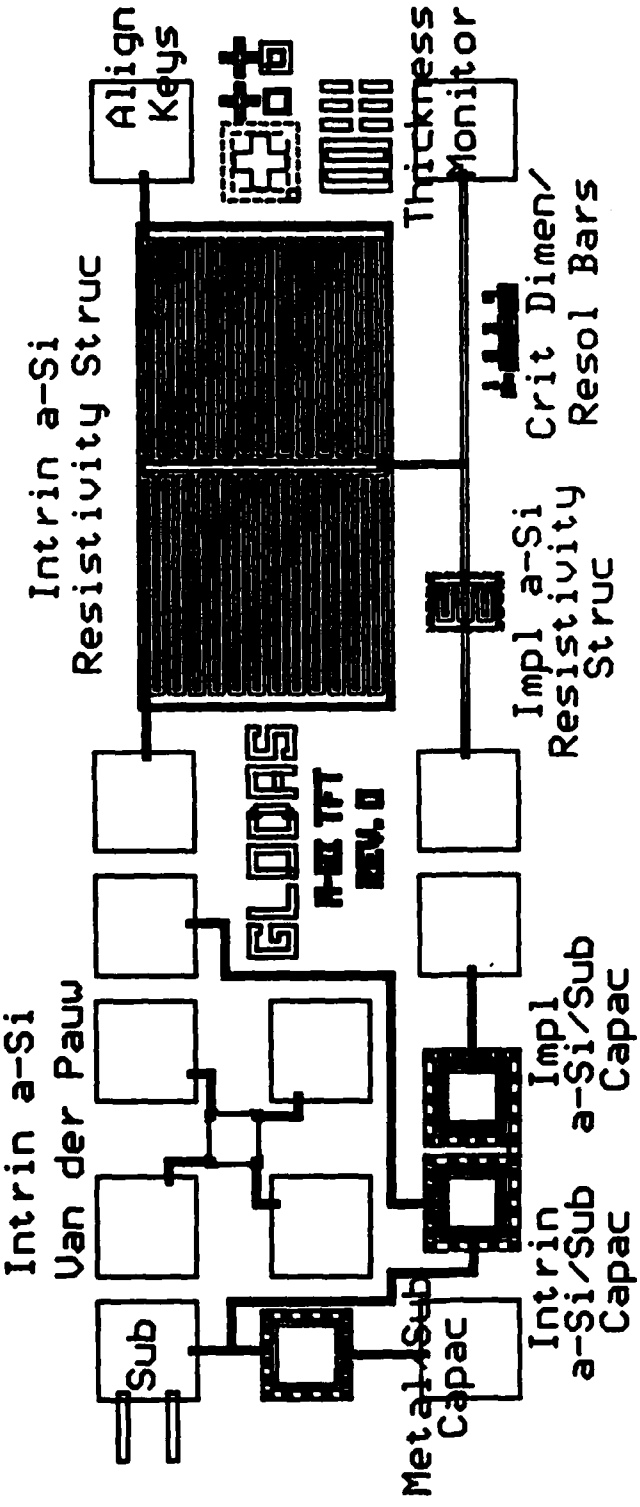

Figure A.3 Area B of GLODAS test pattern.

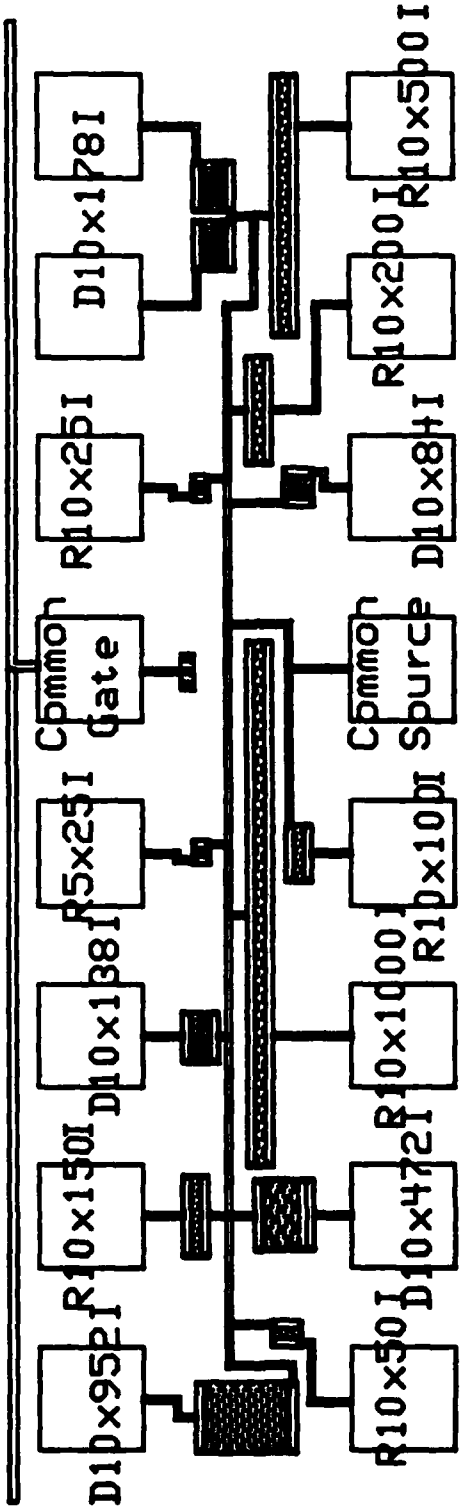

Figure A.4 Area C of GLODAS test pattern (all devices contain ion implanted source/drain regions).

Appendix B

Positive Photoresist Procedures

1. Using a pipette, cover substrate surface with AZ-1350J-SF positive photoresist and spin at 4Krpm for 40sec.
2. Softbake substrate at 90 ° C for 20min.
3. On the Kasper model 17A mask aligner, expose pattern at an exposure setting of 12.0.
4. Develop pattern in solution of AZ Developer:deionized water = 1:1 for 1min and rinse in deionized water.
5. Inspect pattern to insure good definition and proper alignment.
6. Hardbake patterned substrate at 120 ° C for 20min.
7. Perform desired etch/deposition step.
8. Strip photoresist in acetone and rinse substrate in deionized water. Blow dry in N_2.

Appendix C

Negative Photoresist Procedures

1. Using a pipette, cover substrate surface with KTI 747 negative photoresist and spin at 3Krpm for 30sec.
2. Softbake substrate at 90 ° C for 20min.
3. On the Kasper model 17A mask aligner, expose pattern at an exposure setting of 7.5.
4. Develop pattern in solution of KTI Developer for 90sec and rinse in KTI Rinse II for 60sec.
5. Inspect pattern to insure good definition and proper alignment.
6. Hardbake patterned substrate at 120 ° C for 20min.
7. Perform desired etch step.
8. Strip photoresist in heated EKC Nophenol 922. Remove Nophenol by rinsing substrate in trichloroethane, acetone, methonal and then in deionized water. Blow dry in N_2.

Appendix D

a-Si:H TFT Runsheet

Table D.1 a-Si:H TFT runsheet.

Step	Description	Date	Comments
1	Ultraclean <100> 4-6Ω-cm p-type wafer(s) a) H_2SO_4:H_2O_2=1:1 (15min) b) HF:H_2O=20:1 (2min)		
2	Dry oxidation at 1100 ° C (2000Å) a) 3min push in dry N_2 b) 150min oxidation in dry O_2 c) 3min pull in dry N_2		
3	Deposit a-Si:H (1.7Å/sec) a) VTE (300 ° C, 2hr) b) a-Si:H dep. (RF=5W, P=350mT, SiH_4=50sccm, T=250 ° C)		
4	Level 1 Definition a) HMDS precoat (10min) b) Positive PR c) Etch a-Si:H in H_3PO_4:HNO_3:HF=60:5:1 (Wait 7.5min after HF added) d) Strip PR e) Inspection		
5	Sputter Al-Si-Cu (>2000Å) a) Coat gun on at <$5X10^{-6}$T b) Stage rotating c) Dep rate=6Å/mA-min		
6	Level 2 Definition a) Negative PR b) Etch in H_3PO_4:CH_3COOH: HNO_3:H_20=18:1:1:2 at 45 ° C c) Strip PR d) Inspection		

Table D.1 (continued).

Step	Description	Date	Comments
7	Implant P^+ (2 doses) a) 3in matrix, area=20.27cm^2 b) Heat substrate to 250 ° C (Pot=22) c) Beam current $<100\mu A$ d) Dose 1-$10^{16}cm^{-2}$, 30KeV (Mag=1870) e) Dose 2-$10^{16}cm^{-2}$, 60KeV (Mag=2195)		
8	Strip Al-Si-Cu mask using 6b etchant		
9	Level 3 Definition a) Negative PR b) Etch SiO_2 in 6:1 premix BHF (1000Å/min) c) Strip PR d) Inspection		
10	Ultraclean wafer(s) a) ACE/TCA/ACE (3min each) b) H_2SO_4:H_2O_2=1:1 (10min) c) JUST PRIOR to Al dep - 6:1 premix BHF dip (10sec)		
11	Deposit Al (>1500Å) $P < 5X10^{-7}T$		
12	Level 4 Definition a) Positive PR b) Etch Al in H_3PO_4:CH_3COOH: HNO_3:H_2O=76:15:30:50 c) Strip PR		
13	Final Inspection		

Table D.1 (continued).

Positive PR

Step	Description	Level 1	Level 4
1	Apply AZ-1350J-SF (4000RPM, 40sec)		
2	Softbake (90 ° C, 20min)		
3	Exposure on Kasper 17A = 12.0		
4	Develop in AZ Dev:H_2O=1:1 (1min) Rinse in DI H_2O (1min)		
5	Hardbake (120 ° C, 20min)		
6	Etch step		
7	Strip PR in ACE, Rinse in DI H_2O		

Negative PR

Step	Description	Level 2	Level 3
1	Apply KTI-747 (3000RPM, 30sec)		
2	Softbake (90 ° C, 20min)		
3	Exposure on Kasper 17A = 7.5		
4	Develop in KTI Developer (90sec) Rinse in KTI Rinse II (60sec)		
5	Hardbake (120 ° C, 20min)		
6	Etch step		
7	Strip PR in Nophenol, Rinse in TCA/ACE/Meth/H_2O		

VITA

VITA

Harold F. Bare, Jr. was born on January 28, 1948 in Washington, D.C. He attended public schools in California, New York and Virginia, as well as U.S. military dependent schools in Japan. He graduated from McLean High School, McLean, VA, in 1966. In 1970, he received the Bachelor of Science Degree in Electrical Engineering from the Virginia Military Institute and was commissioned a Second Lieutenant in the U.S. Air Force. In 1972, he received the Master of Science Degree in Electrical Engineering from Pennsylvania State University and entered active duty in the U.S. Air Force. His assignments included research and development engineering positions in Air Force Systems Command and Electronic Security Command. In 1976, Mr. Bare left the Air Force and was employed as an electrical engineer by the U.S. Department of Defense. He was recalled to active duty in 1979 and again served in Air Force Systems Command, as well as at the Air Force Academy. He was then assigned to the Air Force Institute of Technology to pursue a Ph.D. degree at Purdue University.

Major Bare is married to the former Martha L. Davis and they have two children, Elizabeth and Mark.

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