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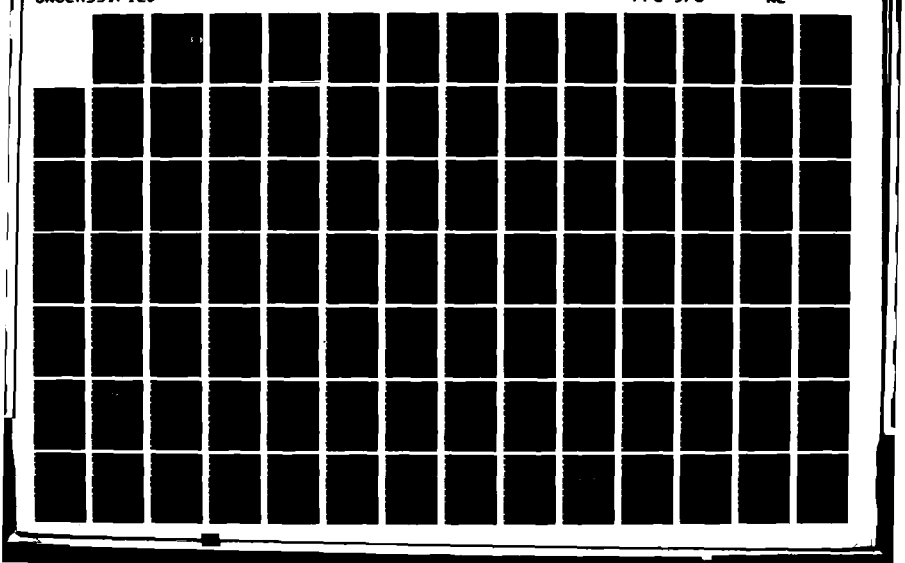

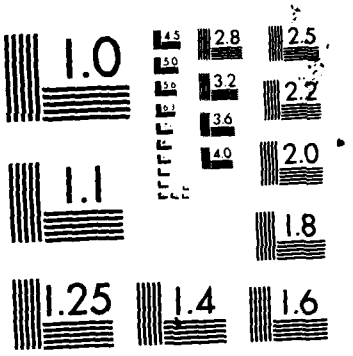

HIGH SPEED POLYCRYSTALINE SILICON PHOTOCONDUCTORS FOR ON-CHIP PULSING AND GATING

CPT Douglas R. Bowman
HQDA, MILPERCEN (DAPC-OPA-E)
200 Stovall Street
Alexandria, VA 22332

Final Report - June 1986

A thesis submitted to Stanford University, Stanford, California in partial fulfillment of the requirements for the degree of Doctor of Philosophy of Electrical Engineering

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Abstract

Photoconductor based time-domain measurement techniques for testing silicon integrated circuits are the focus of this research. The objective is to produce a very high speed sampling system which may be integrated using standard integrated circuit (IC) processing technology and provide for on-chip characterization at frequencies higher than current measurement systems allow.

Integrated photoconductors constructed on silicon wafers of 6 to 70 ohm cm resistivity from annealed polycrystaline silicon and damaged by ion-beam irradiation are reported. They are used in an optoelectronic sampling system to perform high frequency measurements of picosecond pulse propagation in IC microstrip interconnections. Optoelectronic correlation measurements of photoconductor pulsers and photoconductor sampling gates are used to characterize both the photoconductors and the IC interconnections. A subpicosecond pulsed laser system is used to excite the photoconductors to generate and sample the high frequency pulses.

Photoconductors processed as fast pulsers produced $\approx$ 20 mV peak magnitude, 3 picosecond Full Width at Half Magnitude (FWHM) pulses while photoconductors processed as large-signal step pulsers produced $\approx$ 200 mV peak magnitude, 6 picosecond risetime pulses of fifty picosecond duration. Sampling gate photoconductors demonstrated 3-dB measurement bandwidths in excess of 100 GHz. Due to the virtual absence of noise and jitter, high resolution sampling of small, high speed signals is possible with sub picosecond accuracy. High frequency losses and dispersive propagation in the integrated microstrip transmission system are measured and characterized.

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A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

By

Douglas Roland Bowman

June 1986

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as dissertation for the degree of Doctor of Philosophy.

Robert W. Dutton
(Principal Adviser)

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as dissertation for the degree of Doctor of Philosophy.

Krishna C. Saraswat

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as dissertation for the degree of Doctor of Philosophy.

Mark A. Linton

Approved for the University Committee on Graduate Studies:

Dean of Graduate Studies & Research

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Contents

List of Tables

List of Figures

Chapter 1

Introduction

The push toward ever faster digital and analog integrated circuits is rapidly causing changes in circuit design requirements as designers attempt to take full advantage of high-speed devices. Accurate high frequency characterization of high-speed integrated semiconductor devices and interconnections is required to provide these designers with the necessary information to properly design very fast circuits. The research reported in this thesis resulted in a device for doing very high speed time domain measurements, in situ, on a silicon integrated circuit. This device is used to characterize interconnecting transmission lines on silicon IC's at microwave frequencies. The subsequent modeling allows for the exploration of an area critical to the improved performance of integrated circuits and VHSIC technology.

Several methods are available for semiconductor device characterization at microwave frequencies.[1.1] Most of these methods work adequately for discrete microwave devices and circuits, but cannot be readily adapted for monolithic IC analysis. This is due to the parasitics introduced by making off-chip high frequency connections and the lack of accurate on-chip references for use as calibration standards. The use of integrated photoconductors overcomes these difficulties and facilitates microwave measurements on silicon substrates with high S/N ratios and excellent sensitivity.

Integrated circuit interconnections are becoming the limiting factor in chip performance and present a serious roadblock to future speed improvements. Signal

propagation delays can be as long as the device switching delays in fast circuits.[1.2] This trend becomes more severe as the minimum feature size is scaled down to submicron level and chip size is increased towards wafer scale integration.[1.3] Much effort is being expended to model and overcome the delay of the interconnections, but classic microwave measurement techniques are limited in their ability to verify these models. Picosecond integrated photoconductor measurements, however, have recently demonstrated the ability to make highly accurate picosecond measurements on silicon substrates.[1.4][1.5][1.6]

This thesis presents a description of the design, fabrication and modeling of integrated polycrystaline silicon photoconductors and measurement techniques for using them to make on-chip time domain measurements with subpicosecond resolution. Chapter 2 gives a presentation of previous work conducted in the area of pulsed laser measurements upon which this current research is based. Chapter 3 reports the development of polysilicon photoconductive circuit elements (PCE's) which are fully compatible with standard VLSI fabrication processes and demonstrate picosecond responses. Chapter 4 describes a first order device model developed to predict polysilicon PCE performance and compares the model with experimentally measured responses. This is then followed in Chapter 5 by an application of the PCE's to characterize high frequency pulse propagation on silicon IC interconnections. Finally, Chapter 6 summarizes the relative advantages of polysilicon PCE measurements on integrated circuits over other microwave measurement techniques and points out possible areas for future research.

1.1 Introduction to Pulsed Laser Measurements

Laser technological advances have made possible the generation of subpicosecond optical pulses. Using these lasers measurements are possible that surpass the ability of purely electronic pulse generators to generate short duration pulses. [1.7][1.8][1.9] By using an optoelectric transducer, such as a high speed photoconductor, the very short optical pulses can be converted to picosecond electrical pulses. Proper design and use of photoconductive circuit elements can then lead to high frequency time

domain signal measurements similar to those which would be taken by a very fast sampling oscilloscope.

A variety of methods have been used to generate short electrical pulses from optical pulses. D.H. Auston and A.M. Johnson of Bell Laboratories first demonstrated the generation of picosecond pulses on silicon by using optically triggered gating in 1975. [1.10][1.11] Their early method used quasimetallic photoconductivity produced by the absorption of short optical pulses in silicon transmission line structures to both turn on and off a switching gap. Different wavelength laser beams were required for the on and off triggers in this configuration. Later methods eliminated the need for two different wavelengths [1.12][1.13] and explored the use of high defect density materials for use as photoconductors.[1.4][1.14] The advantages of high defect density materials come from the reliance upon recombination mechanisms for the turn-off transient. All of these optoelectronic switching methods demonstrated the very fast responses possible—the switching being limited primarily by the duration of the optical pulses available. In Chapter 2 the various optoelectronic systems previously employed are briefly discussed. These methods, particularly the latest work of Eisenstadt, provide the foundation upon which the development of the polysilicon PCE is based. A description of the laser measurement system used in this work is also provided.

1.2 Introduction to High-Speed Polysilicon PCE's

The development of high speed photoconductors in thin film polycrystaline silicon comprises the bulk of the work reported in this thesis. The motivation behind using polysilicon for the PCE structure is to improve the compatibility of the fabrication process with standard IC fabrication schedules while achieving at least a factor of two improvement in PCE device performance. The resultant devices permit picosecond pulsing and sampling measurements on a silicon IC substrate with greater resolution than previously reported [1.15] while maintaining the desired fabrication compatibility.

Two fabrication processes are developed: a generic polysilicon PCE process and an NMOS–PCE process. The generic PCE process demonstrates the ease with which the basic device can be fabricated. The NMOS–PCE process demonstrates PCE compatibility with other devices. Both of these process schedules are detailed in Appendix C. After fabrication, the PCE's are damaged by ion implantation with other active devices masked by photoresist. The thin-film polysilicon allows for a large reduction in the implant energy from that reported in previous works and insures other devices may be easily masked. A 200 femtosecond colliding-pulse mode-locked (CPM) ring dye laser is used to excite the PCE's and cause rapid conduction during measurements. Trapping sites in the damaged polysilicon cause high recombination rates and lead to a fast turn-off transient when the laser pulse is removed.

Depending upon the specific implant damage process, the PCE's demonstrate both pulse and sampling type responses. Pulser PCE's produce electrical pulses with circuit limited rise times of less than 2 psec and peak amplitudes of up to 500 millivolts for a 50 pJ optical pulse. Sampling PCE's demonstrate a 3-dB measurement bandwidth in excess of 100 GHz. Limited optimization of these sampling PCE's for speed is reported, however, it is felt that further development could lead to even higher cutoff frequencies.

Chapter 3 describes the development of the polysilicon PCE as an integrable device. Improvements over previous PCE performances are enumerated and discussion is presented of how these improvements are achieved with polysilicon PCE's. A description of the process compatibility considerations and their impact upon the NMOS–PCE fabrication schedule is also included.

A simple model to predict polysilicon PCE performance is developed in Chapter 4 and compared with experimental measurements of the devices. It is generally found that the PCE is limited in its speed by the transmission line in which it is embedded. Except at the highest frequencies, the first order model does very well at describing the device's time response.

1.3 Introduction to Microstrip Measurements

Characterization of microstrip transmission lines has been important since the beginning of microwave technology.[1.16] This type of interconnection is readily adapted for use in IC's and has proven reliable and easy to fabricate. Understanding the propagation characteristics of these transmission lines on IC substrates has not been a simple task [1.17][1.18] and as semiconductor devices have increased in speed, the limitations of microstrip have become an important consideration in IC performance. Understanding the impact the interconnections have on system performance is vital and the topic of much current research. [1.3][1.19][1.20][1.21][1.22] A goal of these investigators is the development of a model for IC interconnections. High frequency measurement data is vital in the development and validation of such a model and it is in this area that PCE time domain measurements can contribute.

A variety of microstrip transmission lines are fabricated on SiO_2/Si substrates with PCE's embedded as pulsers and samplers to measure propagation characteristics. These structures comprise a small sampling of the materials, shapes, and sizes of interconnections common to today's IC's. High frequency pulse propagation is measured with subpicosecond accuracy and comparisons made with classical quasi-TEM models. By using measured data for input to the transmission line models the predicted response at various distances can be obtained without the influence of the PCE response. This method results in a close agreement between the measurements and theoretical predictions.

Chapter 5 provides a description of the experimental high frequency characterization of IC interconnections using polysilicon PCE time domain measurements. The structures measured are compared to theoretical calculations based upon a variety of analytical models. Limitations observed in microstrip propagation models are discussed.

1.4 Discussion of Future Work

The development and use of the polycrystaline silicon PCE is by no means completed with the conclusion of this thesis. Future efforts envisioned include the exploration of different thin films for use as the photoconductive layer and taylor-ing the specific film to the type of application. Chapter 6 briefly explores some of the possible materials which may be used. In addition, the development of specific measurement techniques are postulated. These include further characterization of microstrip and ultimately the calculation of s-parameters from PCE time domain data. This is a new field with much room for innovative applications in the future.

Chapter 2

Pulsed Laser Measurements

The ability to generate ultrafast pulses using state-of-the-art lasers has opened up new possibilities for high speed optoelectronic devices. The use of optoelectronic transducers allows the superior speed of the laser to be converted to fast electrical pulses. Optoelectronic transducers have been developed on a variety of substrates and demonstrated picosecond switching speeds. D.H. Auston, in particular, has done much to characterize generic optoelectronic switches. This chapter reviews the development of picosecond optoelectronic switching with emphasis on the uses of such switches as sampling gates on silicon substrates.

2.1 Picosecond Optoelectronic Switching

D.H. Auston and A.M. Johnson of Bell Laboratories first demonstrated the generation of picosecond pulses on silicon substrates in 1975 by using optically triggered gating. [2.1][2.2] They used quasimetallic photoconductivity produced by the absorption of short optical pulses in silicon transmission line structures to both turn on and off a switching gap. Figure 2.1 shows an optoelectronic switch using this technique. The 50 Ω microstrip transmission line is fabricated on high resistivity ($\rho = 10^4\ \Omega - cm$) silicon and contains a gap which forms the switch. The switching action is produced by two optical pulses generating mobile carriers within the silicon. One beam, in the green region of the spectrum at $\lambda = 0.53\ \mu m$, is used to turn

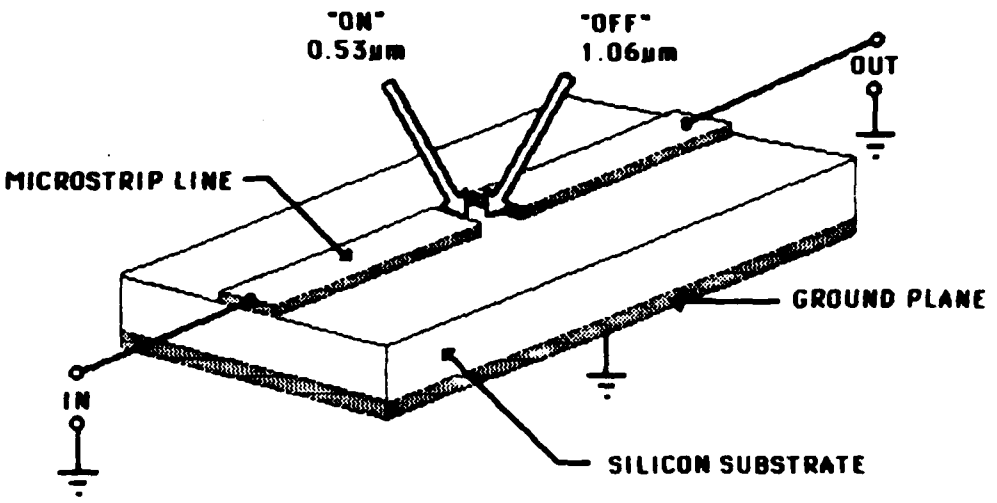

Figure 2.1: Diagram of D.H. Auston's picosecond photoconductor using two different optical beams.[2.1]

the switch on while a second beam, in the infrared at $\lambda = 1.06\ \mu m$, turns it off. The on/off effect of these two beams is caused by the different absorption properties in silicon of the two wavelengths. The green pulse has a large absorption coefficient ($\approx 8 \times 10^3/cm$) and produces only a thin surface layer of photoconductivity across the gap. Efficient transmission across the gap is achieved when the green pulse is sufficiently intense to produce a net gap resistance much less than Z_0, the characteristic impedance of the transmission line. The optical energy required varies as the square of the gap length. but is on the order of 1 μJ for typical structures. [2.2] The infrared beam is used to turn the switch off by effectively shorting the transmission line to prevent further transmission of an incident signal. This is possible because the absorption depth in silicon at this wavelength is large and the pulse penetrates through the substrate to the ground plane. A region of high conductivity between the upper and lower conductors is thus produced, creating the short.

Several advantages over pure electronic switching are immediately apparent in the use of this optoelectronic method. Unlike conventional semiconductor junction devices, recombination or carrier sweep out is not relied upon to achieve the switch action. The very fast response observed ($\approx$ 15 psec [2.2]) is therefore primarily

limited by the duration of the optical pulses used as triggering signals. Another advantage is that with the use of optical controlling pulses nearly perfect isolation exists between the switched and controlling signals. High power switches are readily formed since a reverse junction breakdown problem does not exist as with semiconductor junction switches.

The method of switching the microstrip gap employed by Auston in his earliest work also had some inherent disadvantages which became the driving force behind later improvements. A significant disadvantage is the repetition rate. Even though carrier recombination is not relied upon to switch the gap, the excess carriers generated by the switching action must either be swept out or allowed to recombine before the switch can be used again. This generally limits the repetition rate to less than 1 MHz.

Early efforts at improving the switching method of Auston and Johnson centered around simplifying the complex optical structure needed to generate the required synchronous pulses at two different frequencies which are used to perform the switching. This involved attempts at using a single frequency for both the turn-on and turn-off pulses. In 1976, two basic structures which accomplished this were proposed: a gap-shunt structure (by W. Platte[2.3]) and a coplanar structure (by R. Castagne et al. [2.4]).

The gap-shunt structure, shown in Figure 2.2, allows for the use of a single frequency ($\lambda = 0.906\ \mu m$ in Platte's experiment) for both pulses and requires only a variable delay between the on and off pulses. This delay is easily realized by changing the distance covered by the second pulse (the turn-off pulse) with a translation stage and greatly simplifies the optical setup. The switching action is performed in the same manner as Auston's technique except that the shorting path is now to a grounded structure brought around to the surface of the silicon instead of through the substrate. This facilitates the use of a wider range of optical pulse frequencies. The only constraint placed upon the pulse frequency choice is that the absorption depth at the frequency must be significantly less than the substrate thickness to avoid having the turn-on pulse short the transmission line to the ground plane on the back of the substrate. As with the two beam technique, repetition rate

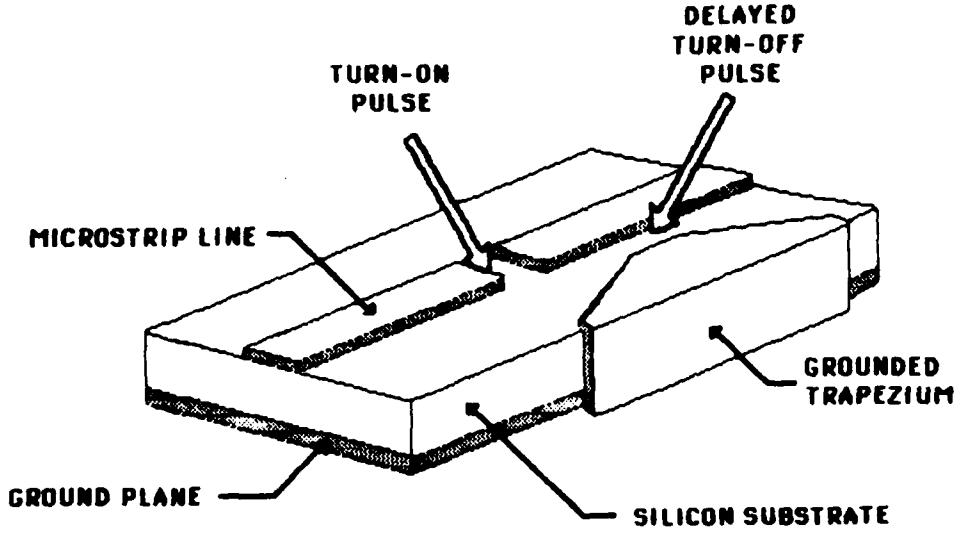

Figure 2.2: Gap-shunt structure used by W. Platte as a modification to Auston's basic switch.[2.3]

is limited to less than 1 MHz due to the need to sweep out or recombine the optically generated carriers prior to using the switch again.

A coplanar transmission line is another structure which can use a single frequency laser source for both beams. The theory of operation is the same as with the gap-shunt structure used by Platte. Switching is performed in exactly the same manner, with one side of the center conductor being shorted to ground (either outside conductor of the coplanar layout) to turn off the switch. Both of these single frequency structures provide switching speeds on the order of two times the rise time of the optical pulses used to control the switch.[2.3][2.4]

After simplification of the optical setup, the next improvements in picosecond optoelectronic switching came with modifications to the substrate so that the second, turn-off, pulse became unnecessary. Auston et al. reported the success of a single beam technique in 1980 using high-defect-density amorphous silicon. [2.5] With this new substrate the speed of response of the gap switch is determined by the relaxation of the photocurrent in the structure. The relaxation time in high-defect-density amorphous films is very short due to the trapping action exhibited

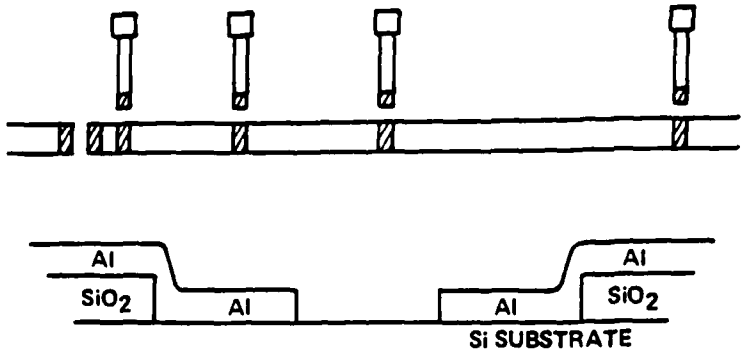

Figure 2.3: Photoconductor test structure used by W.R. Eisenstadt et al. on bulk silicon.[2.8]

by the defect sites. The rapid recombination of carriers (measured as $\approx$ 3-5 psec in [2.5]) is relied upon to turn off the switch instead of using a second beam. Auston's experiments with this technique and switching structures similar to his earlier work (Figure 2.1) resulted in autocorrelation measurements with a full width at half magnitude (FWHM) of 11 psec when triggered with a 3.5 psec optical pulse (λ = 0.58 μm, incident energy= 0.37 $nJ/pulse$). This corresponds to a switching response approximately two times broader than the triggering optical pulse. The circuit response of the gap causes a slight asymmetry in the switched pulse and is the predominant factor in limiting the switching speed. (See Section 2.2.2)

The work on amorphous silicon has been extended by W.R. Eisenstadt and R.B. Hammond to produce picosecond optoelectronic switches on bulk silicon. [2.6][2.7] Their effort was geared towards the production of high speed photoconductors which can be integrated along side of other devices on an integrated circuit using standard VLSI fabrication techniques. The photoconductors were fabricated directly on 70 $\Omega - cm$, < 100 > oriented, n-type Si wafers, similar to wafers used in standard device fabrication. Aluminum microstrip structures were placed on a field oxide with gaps and oxide cuts used to form the photoconductive switch area. (See Figure 2.3). To achieve the rapid recombination required for turn-off, the wafers were ion bombarded with 30 MeV oxygen to locally damage the crystal lattice. This provided the trapping sites needed for rapid carrier recombination after the laser

pulse was removed. High energy ions were used to insure that the damage was deep enough to collect carriers generated deep in the substrate under the switch. The switching action of these structures was measured to be on the order of 30 psec FWHM with very short ($\approx$ 2 psec) risetimes [2.6]. As with the amorphous silicon switches, the speed of response appeared to be limited by the circuit response of the gap.

2.2 Optoelectronic Sampling

The very fast pulses associated with optoelectronic switches triggered by the fast pulse lasers which have become available, lend themselves readily to high speed sampling applications. Several optoelectronic and electro-optic methods have been demonstrated and performance is generally better than the fastest sampling oscilloscope available commercially. These experimental sampling systems allow for time domain measurements on a sub-picosecond scale with excellent sensitivity.

2.2.1 Electro-optic Methods

The use of electro-optic crystals or the electro-optic effect of the substrate is one technique for using high speed laser pulses to sample voltage waveforms on integrated circuits. The electro-optic effect, which is prevalent in such crystals as gallium arsenide ($GaAs$), lithium niobate ($LiNbO$), and lithium tantalate ($LiTaO_3$), is a property of the crystal which causes the optical properties of the material to be modified in the presence of an electric field. The manner in which a laser pulse is modified by the birefringence as it passes through such a material can be directly related to the presence and strength of the electric field. J.A. Valdmanis et al. successfully used both $LiTaO_3$ and $LiNbO$ in sampling systems which achieved a temporal resolution of less than 5 picoseconds. [2.9] K.S. Weingarten et al. have made use of the intrinsic electro-optic properties of gallium arsenide to sample high speed $GaAs$ circuits.[2.10] In one method, shown in Figure 2.4, a $GaAs$ crystal with correct optical orientation is placed on top of the integrated circuit and used

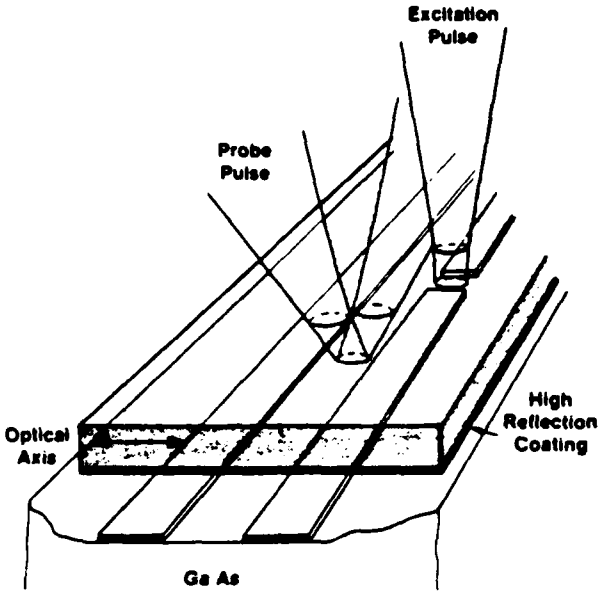

Figure 2.4: Electro-optic sampling method demonstrated by K.J. Weingarten et al. on $GaAs$.[2.10]

as the sampling medium. The electric field from the IC transmission line couples into this crystal and is then sensed by the laser pulse being used as a probe. If the substrate is correctly oriented the use of the second crystal can be eliminated and the substrate probed directly. A polarizer converts the change in polarization of the probe laser pulse into a change in intensity which can be easily monitored with a slow photodetector. Measurements of a $GaAs$ MESFET traveling wave amplifier and an 8-bit multiplexer/demultiplexer have been reported using this method.[2.10]

For materials which do not have a strong electro-optic effect the method of sampling with the second crystal on top of the substrate must be utilized. Silicon is such a material. In this case an electro-optic crystal such as $LiTaO_3$ is placed over the substrate at the point where sampling is to be done. The electric field from the propagating voltage pulse couples into this crystal, which replaces the air dielectric over the transmission line, and is sensed by the laser pulse in the same manner as described above for gallium arsenide. In either case, care must be taken in selecting the laser system to insure that the the photon energy is well below the band gap

energy of the electro-optic medium. This is necessary to allow the laser pulse to pass through the medium rather than be absorbed by it.

2.2.2 Integrated Optoelectronic Samplers

The integration of very high speed optoelectronic transducers within an integrated circuit has some inherent advantages over electro-optic sampling. For substrates without pronounced electro-optic effects, such as silicon, it allows for the exact placement of the sampling location at the time of fabrication rather than relying upon crystal placement during sample preparation. Also, by not using a separate material (the electro-optic crystal) the unknown effect of coupling the field through a different dielectric is removed and a more accurate representation of the actual voltage waveform may be obtained. Care must be taken in the design of the transducers, usually photoconductive switches, to insure that they do not alter the measured circuit performance. When not triggered and even when "on" the pertabation on the circuit from these devices must be negligible.

For simplicity of fabrication and operation, the Photoconductive Circuit Element (PCE) is the best laser driven optoelectronic transducer for sampling applications to integrate on a silicon substrate. The PCE itself is just a rectangular area of photoconductive semiconductor with metal transmission lines contacting the opposite sides of the rectangle. (See Figure 2.5). The PCE must have an extremely low conductivity between the metal lines when not illuminated by a laser pulse and a high conductivity when stimulated. Thus, the semiconductor material in which the PCE is fabricated must have a low conductivity and, therefore, a low doping level. Materials with greater than 10 $\Omega - cm$ resistivity have been shown to be acceptable for PCE use.[2.12]

For successful operation of an integrated PCE several features are desired. The primary goal is to achieve an ideal impulsive sampling gate using the PCE. As such, the unilluminated resistance of the switch must be several orders of magnitude greater than the highest resistance expected to be sampled from. This insures a minimum of leakage will occur during dark (off) periods and does not require the circuit designer to consider the PCE's impact upon the circuit performance, as it

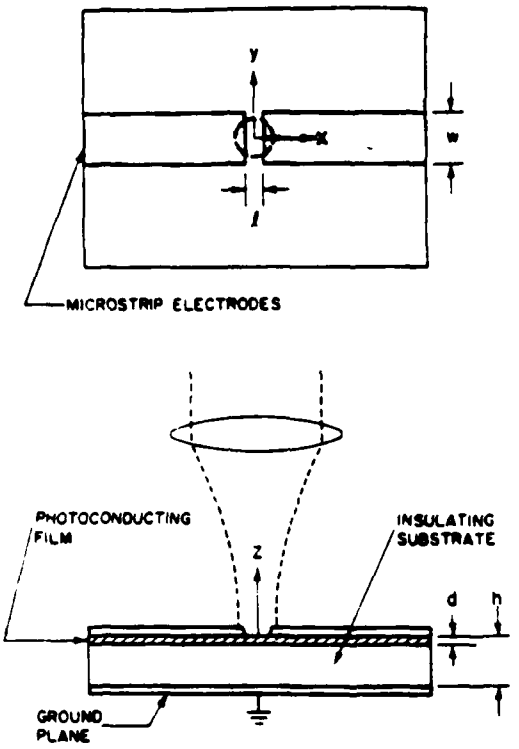

Figure 2.5: Schematic diagram of a generic thin-film photoconductor constructed in a microstrip transmission line.[2.11]

is effectively isolated from the circuit. To approximate impulsive sampling, the effective on time must be very short compared to the length of the event being sampled (At least an order of magnitude faster is desirable.) The effective on time is dependent upon the resistance of the circuit being sampled, ie when the resistance of the PCE becomes low enough to draw some percentage of the current relative to the circuit, it is considered on. To compensate for this circuit dependency, the turn-on and turn-off transients should be very rapid. This minimizes the differences in effective on time between circuits of different resistivities and is important in standardizing PCE performance across a chip or wafer. Another consideration in the design of PCE's is that the minimum on resistance should be small so as to generate a large sampled signal from even a weak input waveform, but not so low as to have a serious impact upon the circuit being sampled.

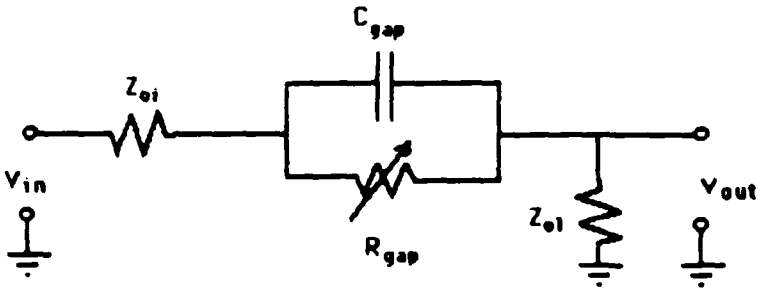

Figure 2.6: Circuit approximation of a photoconductive gap in a microstrip transmission line.

A simple device circuit model for the generic PCE shown in Figure 2.5 can be developed independent of the actual construction, when only considering first order effects. In this case the parasitics from the specific geometry can be ignored and the circuit of Figure 2.6 gives a good approximation for the PCE. In this circuit Z_{0i} and Z_{0l} represent the characteristic impedance of the transmission lines contacting the photoconductive region. The gap itself is modeled as a fixed capacitance between the ends of the transmission lines and a variable resistance modulated by the optical energy introduced via the laser pulse. Parasitic capacitances generally exist between the ends of the transmission lines and the substrate but these only have a second order effect and will be ignored until Chapter 4 when a model for the specific case of the polysilicon PCE is developed. Auston has analyzed the generic PCE model for a variety of configurations and found that an upper limit upon switching performance is set by the circuit limitations of the PCE gap capacitance and transmission line impedance. [2.11] As shown in Figure 2.6 the effective load seen by the PCE is the characteristic impedance of the transmission line in which it is imbedded. Focussing on the instantaneous charge, $q(t)$, on the gap capacitance, Auston has shown that the reflected and transmitted waveforms for an arbitrary incident signal, $v_i(t)$, are expressed by Equations 2.1 and 2.2 respectively.

$$v_r(t) = \frac{1}{2C_g} q(t) \tag{2.1}$$

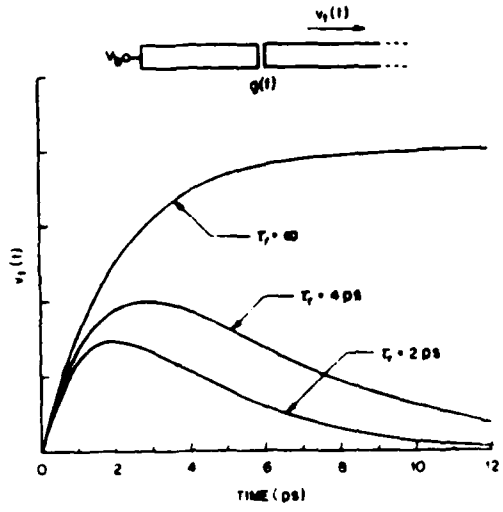

Figure 2.7: Predicted response of a photoconductive gap with varying carrier recombination times.[2.11]

$$v_t(t) = v_i(t) - \frac{1}{2C_g}q(t) \tag{2.2}$$

For the specific case of a DC bias of value V_b and a single exponential photoconductance, the transmitted signal is of the form:

$$v_t(t) = \frac{g_0 V_b}{2C_g}\left|\frac{e^{-t/\tau_r} - e^{-t/\tau_c}}{\frac{1}{\tau_c} - \frac{1}{\tau_r}}\right|; t \geq 0 \tag{2.3}$$

where $\tau_c = 2Z_o C_g$, τ_r is the carrier relaxation time, and g_o the maximum conductance.

Figure 2.7 shows the time response of the generic PCE as described by Equation 2.3 for varying relaxation times. Note that the peak amplitude of the signal is reduced as τ_r decreases and the peak delayed from the impulsive optical excitation assumed to occur at time zero.

The production of an electrical pulse from an optical one within the PCE is a very complex physical process which must be modeled if the magnitude of the transmitted pulse is to be determined. Several simplifying assumptions must initially be made if the task of understanding the laser pulse interaction with the PCE is to be made manageable. These assumptions include: 1) the laser pulse is short

enough to appear as an impulse to the PCE so that the laser delivers an impulse of optical energy which generates electrical carriers, 2) the laser is perfectly focused on the test substrate so that optimal energy transfer is obtained, and 3) the PCE absorbs all the light which is incident upon it. Describing the electrical operation of the PCE is simplified by assuming: 1) the connecting transmission lines make perfect ohmic contacts with the photoconductive region, 2) no significant surface charge effects are present, and 3) bulk recombination governs the PCE carrier lifetimes. These last three assumptions are the conditions most desirable for proper PCE electrical operation and enable PCE measurements to achieve large signal to noise ratios. [2.13] In Chapter 4 some of the laser assumptions will be reconsidered when a more rigorous model is developed.

If it is also assumed that one electron-hole pair is generated in the PCE gap by each incident photon, then the PCE resistance, mobility and peak current can be derived from the laser pulse energy and photon energy. For a laser with pulse energy, E, and photon energy, E_p, it can be shown that the on-resistance for the PCE, R_{on}, is represented by Equation 2.4, where w is the width of the PCE gap,

$$R_{on} = \frac{w^2 E_p}{q(\mu_n + \mu_p)(1 - R)E} \tag{2.4}$$

μ_n and μ_p the electron and hole mobilities respectively, R the surface reflectivity, and q the electronic charge. A desirable factor concerning PCE control is shown by this equation. Geometry, in the form of the gap width, and laser energy have a significant controlling effect upon the on-resistance of the PCE. This makes the PCE structure much easier to taylor to a specific application over a wide range of resistances independent of the photoconductive material chosen for its fabrication.

$$I_{max} = \frac{q(\mu_n + \mu_p)(1 - R)E\,V_b}{w^2 E_p} \tag{2.5}$$

The maximum current generated by the laser pulse due to conduction from the photogenerated carriers can be calculated by dividing the bias voltage applied to one side of the gap by the on-resistance of Equation 2.4. I_{max}, the peak current if the conductance is a step response is then represented by Equation 2.5 where V_b is the bias across the gap.

2.2.3 PCE Measurement System Considerations and Implementation

From the above discussion of PCE performance and the assumptions leading to the analysis, limitations upon the nature of the optical excitation become apparent. The choice of an excitation source has a significant impact upon the PCE performance. With the type of geometries considered in this research, the circuit limitations on the PCE result in a time constant on the order of 2 picoseconds. To insure that the laser pulse appears as an optical impulse to the PCE thus requires an ultrashort pulse width ($<$ 1 psec). This criteria removes the requirement to consider the laser pulse shape when determining the PCE response. A second consideration when selecting an optical source for excitation is the photon energy. To enable the laser pulse to create electron-hole pairs in the semiconductor material chosen for the photoconductor, the photon energy must be above the semiconductor's band gap energy. Higher energies are desirable since if the photon energy is well above the band gap then carrier generation will be confined to the surface or within the thin photoconductive layer. Deep generation adds to the time needed to remove the excess carriers and can significantly slow the PCE turn-off transient.

The colliding pulse mode-locked (CPM) ring dye laser is one optical source which meets the requirements for use in a PCE system. It has the demonstrated ability to generate 55 femtosecond pulses with optical compression techniques[2.14] and operates typically at a wavelength of 610 nm. This wavelength has a photon energy well above the band gap energy of most semiconductor materials used in integrated circuits and does not limit the choice of photoconductive layers. To operate, the CPM laser employs two counter-rotating beams of pulses propagating along the same optical path within the laser cavity. The pulses are timed to arrive simultaneously at a saturable absorber placed in their paths. This absorber produces a shorter set of optical pulses via a non-linear transient grating effect.[2.15]

The specific laser system used in this research is a CPM dye laser located at the Los Alamos National Laboratory. This laser is capable of producing 200 femtosecond FWHM pulses at a 125 MHz repetition rate and with optical energies

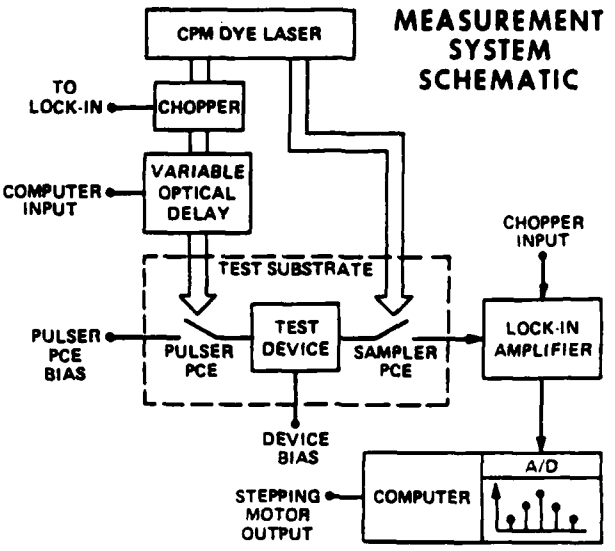

Figure 2.8: Optoelectronic measurement system block diagram.

in excess of 100 pJ. Figure 2.8 is a block diagram of the system used for PCE measurements. The CPM laser generates two synchronous pulse trains. One pulse train is passed through a mechanical chopper which turns the pulsed beam on and off at a fixed interval. The frequency of the chopper is fed directly to a Princeton Applied Research lock-in amplifier (Model 124A) for synchronization to insure that the PCE output charge is only measured in a low noise region. This pulse train also passes through a computer controlled translation stage to introduce a variable optical delay. The translation stage introduces a difference in path lengths which corresponds to a difference in the time of arrival of the laser pulses on the test substrate.

The test substrate shows two PCE's. One is biased and used as a pulser to provide an impulsive input to the device under test. This causes a transient response which is sampled by the second PCE. The sampling PCE is sampling charge from the output waveform at a constant difference in time from the pulser PCE as determined by the beam arrival times on the substrate. This sampled charge is integrated by the lock-in amplifier over many events and provided to an IBM PC for data display

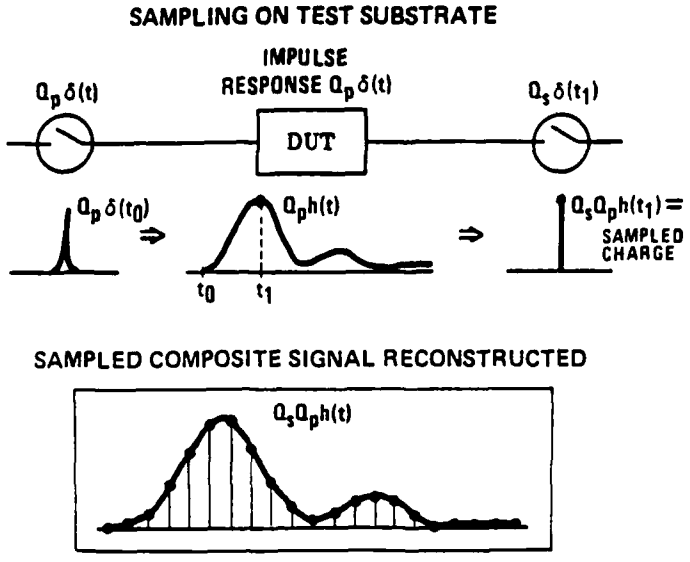

Figure 2.9: Reconstruction process for sampling a time varying waveform with an impulsive pulse and sample system.

and storage via an analog-to-digital converter. The data represents the output waveform at a single point in time. By varying the relative arrival times of the laser beams with the translation stage, the entire pulse response of the test device can be reconstructed as shown in Figure 2.9. This capability provides an extremely fast, low noise, sampling oscilloscope type trace when displayed after an entire sweep. Averaging data over multiple sweeps of the time range can also be done to further reduce any random noise present in the measurement.

When attempting to characterize the response of a device which is fast enough to negate the assumption of impulsive sampling, the above description does not adequately demonstrate the nature of the final output trace. This is the case when PCE's are used to measure their own response. The test device in Figure 2.8 is replaced by a short microstrip transmission line so that only the response of the PCE's themselves can be measured. The result is known as a cross-correlation measurement (or autocorrelation if two identical structures are used) and is commonly used in the field of lasers to measure extremely short duration optical pulses.

Eisenstadt et al. idealized the PCE response and illustrated the nature of the resultant cross-correlation waveform.[2.6] To achieve the idealized PCE waveform

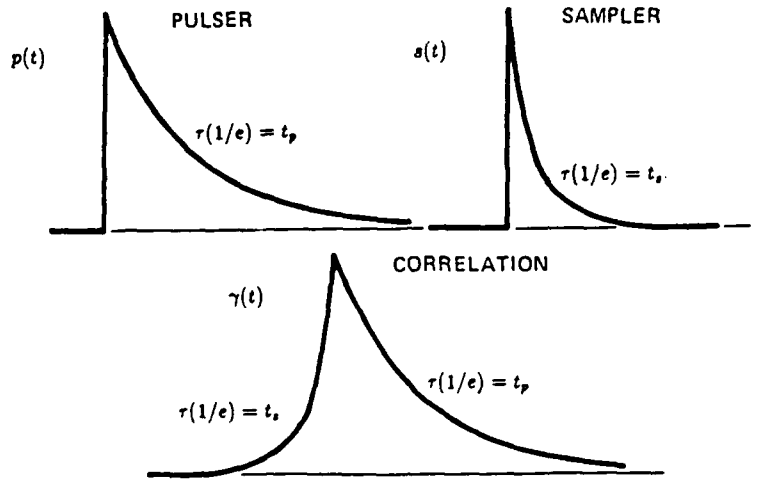

Figure 2.10: Idealized PCE waveforms with the resultant cross-correlation.[2.6]

the rising transient is assumed to be a step, followed by a decaying exponential. Hwang et al. showed that the decaying (turn-off) transient is at least a double exponential.[2.16] A reasonable approximation is, however, achieved by the use of a single time constant exponential decay. Given the resultant idealized PCE response and generalizing the functions such that the pulser and sampler PCE's have different characteristic decay times (τ_p and τ_s respectively) then Equation 2.6 shows the cross-correlation function, $\gamma(t)$. From this equation it is seen that the exponential decay of the sampling PCE waveform is mirrored by the left side of the cross-correlation peak while the pulser PCE waveform is equivalent to the right side. This is shown graphically in Figure 2.10.

$$\gamma(t) = \begin{cases} \frac{\tau_s \tau_p}{\tau_s + \tau_p} e^{\frac{t}{\tau_s}} & t < 0 \\ \\ \frac{\tau_s \tau_p}{\tau_s + \tau_p} e^{\frac{t}{\tau_p}} & t > 0 \end{cases} \tag{2.6}$$

As expected, actual PCE cross-correlation measurements vary from this ideal. As will be seen in the measurements presented in the following chapters, the most obvious differences lie in the rounding of the peak. This is due to the finite rise times actually observed in the experimental devices.

2.3 Summary

This chapter has traced the development of picosecond optoelectronic switching from its inception at Bell Laboratories in the mid-1970's. The use of high speed photoconductors and electro-optic transducers in sampling configurations was introduced with emphasis placed upon the optoelectronic sampling possible with photoconductive circuit elements (PCE's). Generic PCE responses and limitations were discussed as was the optoelectronic measurement theory and system used for the characterization of the polysilicon devices subsequently developed.

Chapter 3

Development of Polysilicon PCE's

Overcoming the limitations of previous photoconductive devices has been the goal of many researchers since Auston's introduction of the high speed photoconductive switch. This is true also for the development of PCE's fabricated in polycrystaline silicon. Several of the shortfalls of previous PCE's are specifically addressed by changing the photoconductive layer to polysilicon. This chapter describes the development of these polysilicon devices, which take advantage of material properties to achieve improved overall device performance and IC compatibility.

3.1 Advantages of Polysilicon PCE's

The choice of the photoconductive layer in the development of PCE's determines the ease with which the device can be fabricated and some of its performance limitations. Eisenstadt is the only researcher known to this author who has attempted to integrate an optoelectronic device using silicon integrated circuit processing techniques.[3.1] His bulk silicon PCE's demonstrate the feasibility of integrating this type of device along side of other silicon devices and using them to perform high speed measurements on-chip. There remain several important problems with the device and its fabrication which are overcome by changing the photoconductive film to polycrystaline silicon.

Most of the advantages of polysilicon PCE's over bulk silicon and other substrate PCE's come from its thin film nature. The use of a thin film in place of the substrate limits the region of photoconductivity to an area specifically delineated by the fabrication process and not by electrical mechanisms. Charges introduced into the layer by optical excitation are confined to a region where they can be controlled to achieve the desired time response. One of the limitations of the bulk silicon device's time response turned out to be long lived carriers generated deep in the substrate.[3.2] This factor limited recombination times to $\approx$ 20-30 picoseconds.[3.3] Deep carriers are not a problem (even if some are, in fact, produced) with thin film photoconductors. An insulating layer of oxide separates the active photoconductor layer from the substrate. Assuming that none of the circuit limiting parasitics change when the photoconductive layer is changed, the speed of the polysilicon PCE should be faster than the bulk silicon just on the basis of getting rid of the effect of the deep carriers.

To overcome the deep generated carrier problem in bulk silicon PCE's, very high energy implants (ie. 30 MeV oxygen) are used to produce trapping sites deep in the substrate and shorten the carrier lifetimes. Not only does the implant require special equipment to get the high energy ions, but masking other devices on the substrate from the damage created by the implant requires metal shadow masking, a technique not normally used in IC fabrication. Since deep carriers are not a problem with thin film polysilicon PCE's the implant energies can be lowered significantly. This allows for the use of standard implanters and photoresist masking techniques common in current VLSI fabrication processes. Process compatibility is enhanced by choosing thin film polysilicon for the PCE.

Another important advantage of polysilicon PCE's over their bulk substrate counterparts is derived from the isolation afforded by the oxide layer separating the polysilicon from the substrate. Since the PCE is not tied electrically to the substrate, any limitations on the substrate in terms of resistivity, doping type, orientation, etc. are removed. The desired low dark conductivity limits substrate PCE's in regards to how low a substrate resistivity can be used before excessive leakage renders the device useless. As a separate layer, the polysilicon can be

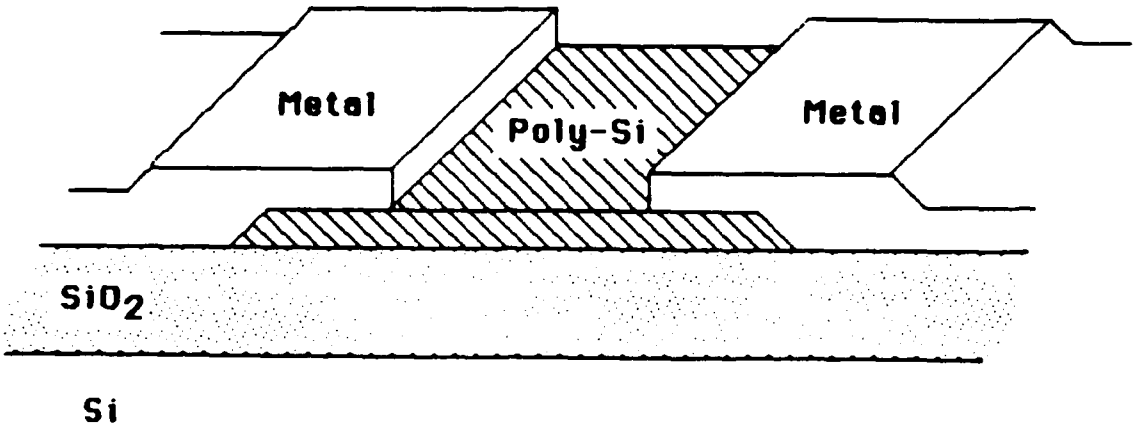

Figure 3.1: Generic polysilicon PCE structure.

tailored to meet the needs of the PCE without affecting the substrate (and, thus, other devices formed in the substrate). It can also be connected to electrically in a more reliable manner and with better isolation so that leakage to nearby devices is not a problem.

3.2 Device Design Optimization

Careful thought must be given to the design of any new device to insure that that design is consistent with the concept of the device's operation. Particular consideration must be given to design factors which impact upon performance, particularly those performance parameters which are the most important to the specific application which the designer has in mind. In the case of polysilicon PCE's this application is optoelectronic sampling for which speed and repeatability are the most important constraints placed upon the design.

3.2.1 General Layout

The physical layout of a polysilicon PCE must allow for optical access to enable the stimulating laser pulse to enter the photoconductive layer. This same requirement is present for all PCE structures regardless of the material they are fabricated

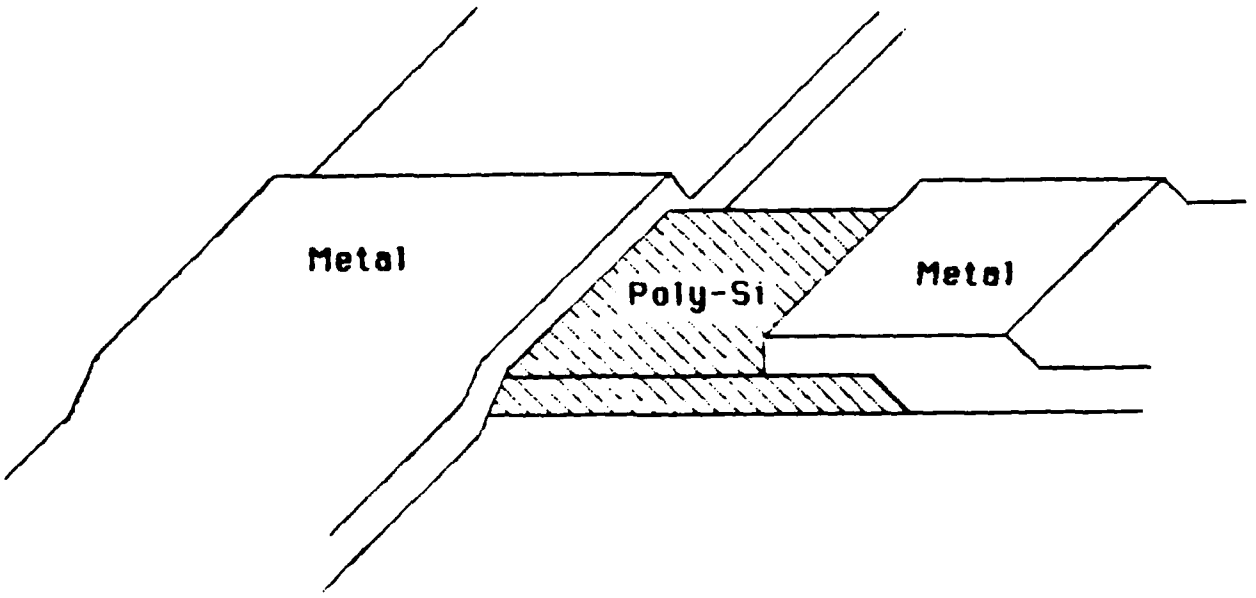

Figure 3.2: Modified polysilicon PCE structure for use as a sampling gate.

in and dictates that some type of planar surface structure be used. Thus, the geometry of the polysilicon PCE is very similar to that of Eisenstadt's or Auston's PCE's with minor changes to accommodate the thin film polysilicon. The device is composed of a rectangular photoconductive region (rectangular for ease of layout) with metallic contacts at opposite sides. These contacts are formed by bringing stub microstrip transmission lines into contact with the photoconductive layer, leaving a gap between them to form the active area of the device. In contrast to the substrate PCE's, the polysilicon PCE structure is placed on an isolation layer of SiO_2 which can vary in thickness to meet specific processing requirements. Figure 3.1 is a rendering of a generic polysilicon PCE structure. The polysilicon layer used for the device is undoped to achieve the desired high dark resistivity.

The structure of Figure 3.1 is satisfactory for in-line pulsing, but must be modified for sampling applications. Auston proposed a variety of configurations which

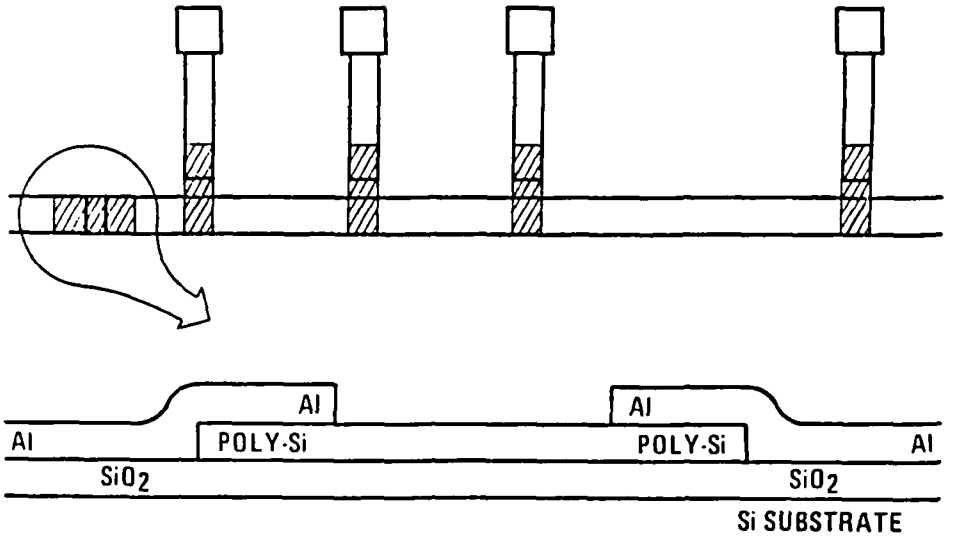

Figure 3.3: Polysilicon PCE test structure showing an in-line pulsing PCE (left) and four sampling PCE's with a typical device cross-section.

could be used for this purpose.[3.4] A stub-T arrangement is used for the polysilicon PCE samplers as it provides the fastest circuit limited response[3.4], is easy to layout, and allows adequate room for probing both optically and mechanically. Figure 3.2 is a representation of such a sampler. For the device characterization measurements these structures are combined into a test structure which contains an in-line pulsing gate and several samplers at various distances along a microstrip transmission line (See Figure 3.3). The sampling PCE's are placed at 100, 500, 1000, and 2000 μm from the pulsing PCE to be consistent with Eisenstadt's test structure[3.1] and allow direct comparisons of the results.

3.2.2 Size Optimization

The physical dimensions of the device are critical in determining its performance. If the carrier recombination time in the PCE is sufficiently short, then the time response becomes very sensitive to the gap capacitance and the characteristic impedance of the transmission line in which it is imbedded. (See Equation 2.3 in Chapter 2.) These circuit parameters then define the design criteria for the PCE

dimensions when optimum speed is desired. Coupled with the speed consideration is the desire for repeatability, both locally and on a wafer scale, of the device's performance. This results in a tradeoff between speed (C_g and Z_0 optimization) and sensitivities to process tolerances (small ΔC_g and ΔZ_0) when selecting PCE dimensions.

The capacitance across a series gap in a microstrip transmission line is used as an approximation of C_g, the PCE gap capacitance. Since a closed form analytical expression for the gap capacitance is not available, curve-fitted expressions are used.[3.5] These have been shown to be within 7% of the experimental data they model[3.6] and, thus, should be an adequate approximation for C_g since the physical deviation from the theoretical gap structure is small. The equations show that the microstrip transmission line width has a significant impact upon the gap capacitance and its sensitivity to variations in the gap width. (See Appendix A for the gap capacitance equations used.) The gap width dependence is minimized for narrow lines or large gaps. Substrate height dependence is present in all cases but is somewhat less for narrow microstrip. Figure 3.4 shows these dependencies for narrow (10 μm) and wide (100 μm) microstrip transmission lines on a silicon substrate. From this data, and considering only the gap capacitance, it is apparent that the polysilicon PCE should be imbedded in a narrow line on a thin substrate and have a gap width to microstrip width ratio of around one. This would minimize the capacitance (improve speed) yet allow for significant variation in processing tolerances without altering the capacitance much.

The characteristic impedance of the transmission line in which the PCE is placed is the other circuit parameter affecting performance and can be optimized by sizing the microstrip correctly. In addition to its influence on the gap capacitance discussed above, Z_0 also directly factors into the gap time constant (τ_τ in Equation 2.3). Analytic expressions for the static-TEM characteristic impedance have been developed and continuously refined.[3.7] [3.8] [3.9] Reported accuracies for these formula (see Chapter 5) are within 1 percent.[3.10] This accuracy is better than that generally achievable during processing, so they are more than sufficient to represent the structures actually being constructed. Figure 3.5 shows the variation in the char-

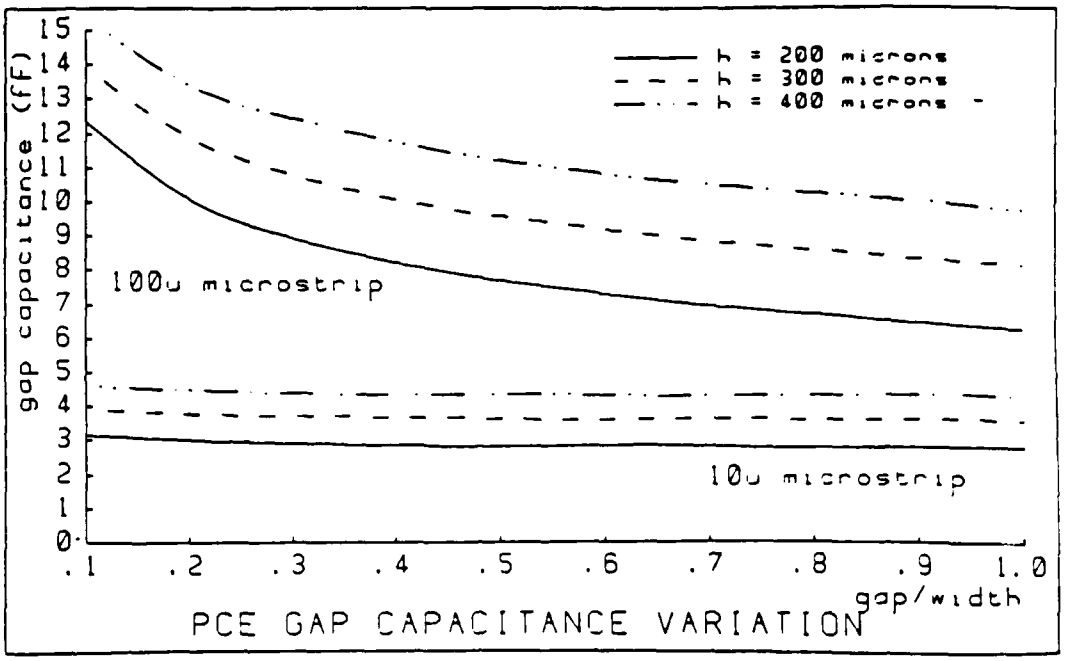

Figure 3.4: PCE gap capacitance variations with substrate height, microstrip width, and gap width–microstrip width ratio.

acteristic impedance of a microstrip transmission line on a silicon substrate as a function of the substrate height and line width. The trend is for lower impedances (faster PCE's) when using wide lines and thin substrates. Thinning the substrate is thus beneficial in terms of both gap capacitance and microstrip impedance, however, some tradeoff must be done with the microstrip width to optimize the PCE structure for speed.

For the fastest operation, the product of the PCE gap capacitance (C_g) and the microstrip impedance (Z_0) must be minimized. Because of the nature of the expressions describing these two quantities, this is not an easy task to perform rigorously. Graphical analysis is better suited to determine a range of values which can then be choosen among based upon secondary considerations such as ease of fabrication or other performance criteria. Figure 3.6 is a representative plot of the time constant for a PCE gap versus the gap width, microstrip width, and substrate height. As expected, the thinner substrates give improved speed response. This improvement is not considered significant in terms of the effort involved in thinning

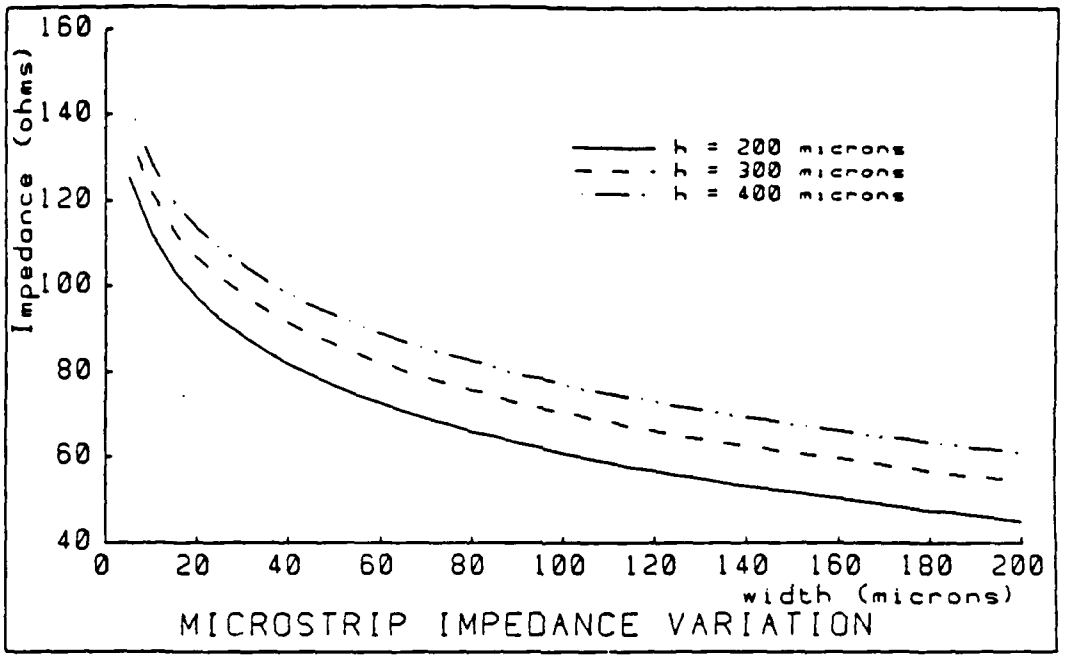

Figure 3.5: Characteristic impedance, Z_0, as a function of substrate height and microstrip width for a silicon substrate.

the substrates so no attempt has been made to exploit this characteristic. More importantly, however, the plots show that a lower limit on the gap width is present, below which a steep bend upward in the time constant plot will be experienced. The lower limit can be made smaller by going to narrower lines, but it still exists and provides a limitation (other than fabrication) on how narrow the PCE gap may become before speed, repeatability, and reliability are sacrificed. A range of gap widths from 10 μm to 50 μm appears to be acceptable for the microstrip widths of interest on integrated circuits ($< 100\mu m$). This range causes, at most, a 20% variation in the calculated time constant.

A secondary performance criteria, maximizing the PCE output signal, is used to determine where in the range of acceptable gap widths to actually design the PCE structure. From Eisenstadt's derivation of the maximum current produced by a PCE (see Chapter 2, Equation 2.5) it can be seen that the output signal is inversely proportional to the square of the gap width. To maximize the output thus requires a PCE with a gap width at the lower end of the acceptable range. Fabricating

polysilicon PCE's with gaps bracketing the minimum $10\mu m$ width ($\pm 5\mu m$) and imbedded in microstrip of several different widths gives enough of a variety to the structures to allow for the verification of the validity of the design assumptions made in optimizing for high-speed, high output performance. Characterization of the sensitivity of PCE performance to variations in these parameters is also possible.

3.3 PCE Process Development

One of the major motivations in using thin film polysilicon for the photoconductive layer in PCE's is to improve the device's fabrication compatibility with that of standard silicon VLSI devices currently being manufactured. Optimizing the fabrication process to achieve this compatibility while maintaining the desired high speed response involves careful consideration of the processing steps necessary to produce the PCE and their impact upon other devices. A generic polysilicon PCE fabrication schedule is used to produce PCE's and transmission line structures for

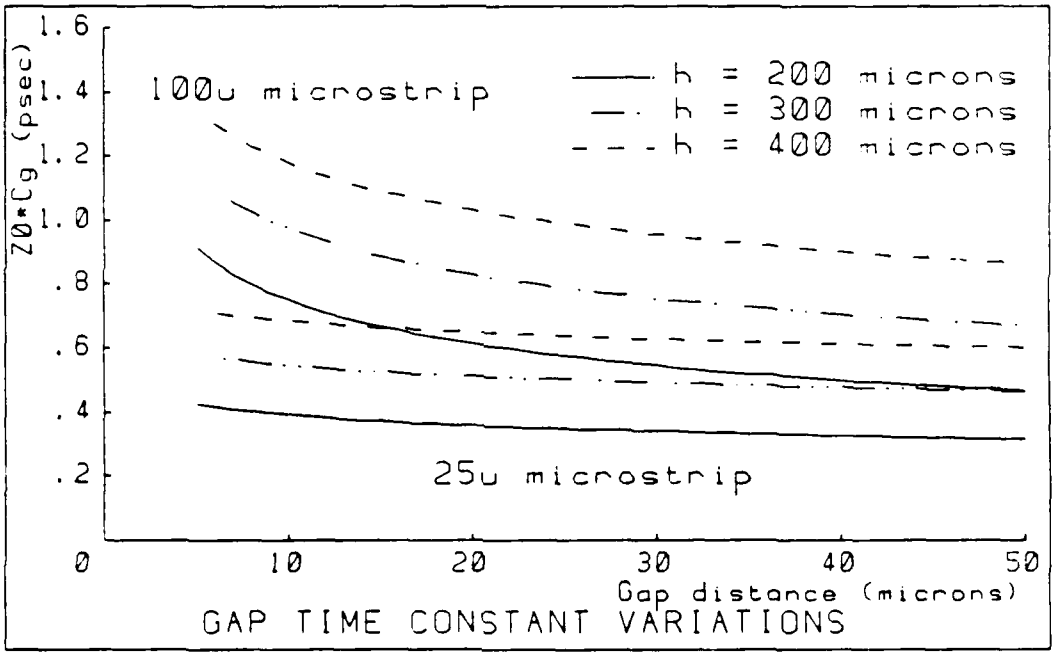

Figure 3.6: Calculated PCE gap time constant (Z_0C_g).

testing and measuring these components. (See Appendix C, Section C.1 for the specific fabrication schedule.) The device is very simple to fabricate in this environment, requiring only two masks, and very tolerant of processing inaccuracies such as lithography misalignments and over-etching. Two factors, anneal temperature and implant damage, are optimized over a limited range to achieve the best PCE performance in terms of speed and signal level.

Once the generic fabrication schedule is understood it becomes possible to integrate the polysilicon PCE into other processing schedules to produce complete integrated circuits containing high speed photoconductors. The feasibility of this is shown by adapting a simple NMOS process, used at Stanford University to teach a course in IC fabrication, to also produce polysilicon PCE's (see Appendix C, Section C.2). The modifications to the fabrication schedule are minor, adding one mask step, a high temperature anneal, and the post-processing implant damaging. The demands of the NMOS processing are much greater than those of the PCE so little extra effort is involved in adding the photoconductors to the IC.

3.3.1 Generic Polysilicon PCE Fabrication

The fabrication of a polysilicon PCE on a silicon substrate involves the deposition and patterning of only three layers—SiO_2 (oxide), undoped polysilicon (poly), and metal. Standard silicon wafers of any resistivity, doping, or orientation are used for the substrate. Oxide is thermally grown to a thickness ranging from $0.5\mu m$ to $1.5\mu m$ in a wet oxygen ambient. This layer acts as an insulation lay r for the polysilicon PCE and its thickness is not critical for the PCE operation. Depending upon the metal used for interconnections, however, spiking considerations may dictate that the thicker oxide be used.

Undoped polysilicon is deposited on the oxide using LPCVD deposition. Poly thicknesses of $0.5\mu m$ are used for this layer since this is a fairly standard deposition. Undoped polysilicon is required to achieve the high dark resistance needed for correct PCE operation. The layer is then patterned using standard photolithographic techniques and polysilicon etching methods to produce the poly islands which will form the photoconductors.

After an anneal, the wafers undergo metal deposition and patterning to make contact to the poly islands and form the PCE's and interconnections. One benefit of using undoped polysilicon is that there is no problem making these contacts ohmic, a necessity for correct PCE operation. Contacts to bulk substrate PCE's sometimes result in the formation of a Shottky barrier depending upon the doping type of the substrate.[3.11] This is not observed with polysilicon PCE's and no special processing is required to make the contacts ohmic.

Polysilicon Anneal

The anneal of the polysilicon islands prior to the metalization, mentioned above, is necessary to improve the output of the photoconductor and is included if the step is compatible with other devices. For the generic polysilicon PCE process there are no other devices and the anneal improves the peak output of the PCE's by up to an order of magnitude. The mechanism for this improvement is the increase in average grain size in the polysilicon and resultant improvement in the effective carrier mobility.

Conduction mechanisms in polycrystaline silicon have been investigated by numerous researchers.[3.12][3.13][3.14][3.15] The electrical properties of the material are greatly influenced by the grain-boundary properties, average grain size, and doping concentration.[3.12] Most authors agree that grain-boundary trapping is, at least in part, responsible for the conduction mechanism in polysilicon. [3.13][3.14][3.15] The impact of the average grain size is seen when considering that, by increasing the volume of the individual grains, the total perimeter area decreases. As a result the grain-boundary area is reduced—leading to a reduction in trapping sites at these locations and improving the effective mobility.

Increasing the average grain size in the polysilicon layer is accomplished via a high temperature anneal. Colinge et al. have shown that the mean grain diameter increases for anneal temperatures above 1000°C with an upper limit on the size being the thickness of the polysilicon layer.[3.16] Their data (shown in Figure 3.7) is directly applicable to the polysilicon PCE since it is derived from measurements on $0.5\mu m$ LPCVD polysilicon, virtually identical to the layer used in the PCE

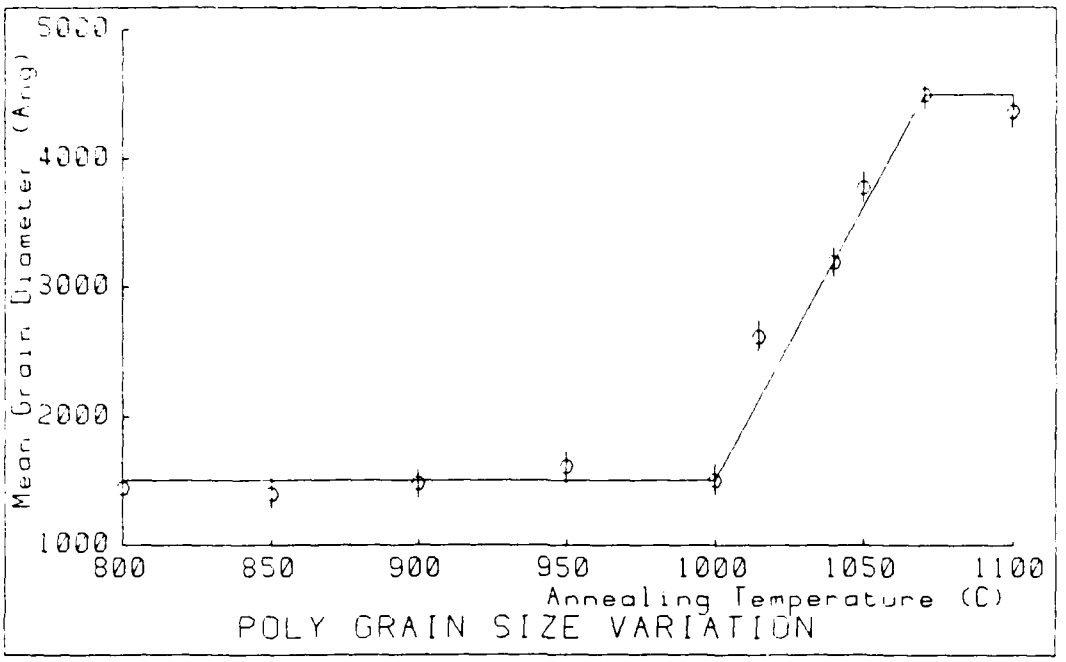

Figure 3.7: Polysilicon grain size increases with anneal temperature.[3.16]

structure. It is therefore expected that anneals above 1000°C are needed to improve the photoconductor's output level.

One hour anneals in an Argon ambient of the polysilicon layer are conducted at temperatures of 900, 950, 1000, 1100, and 1150°C to verify the expected behavior. Standardized structures ($15\mu m$ gaps in $100\mu m$ microstrip) and implant damage (250 KeV Si to a dose of $10^{14}/cm^2$) insure that any differences observed in peak output are due to the enhanced mobility within the photoconductive layer. Figure 3.8 shows a plot of the resultant output levels from auto-correlation measurements of the devices. Little improvement is seen until the anneal temperature is above 1000°C as predicted. At 1150°C the output is approximately ten times that of the lower temperature anneals.

Two interesting items come to light when studying the data in Figure 3.8. The upper limit on the mean grain size observed by Colinge has apparently not been reached in the PCE structures, since the improvement in signal levels did not taper off at the highest temperatures. Two possible explanations for this are proposed.

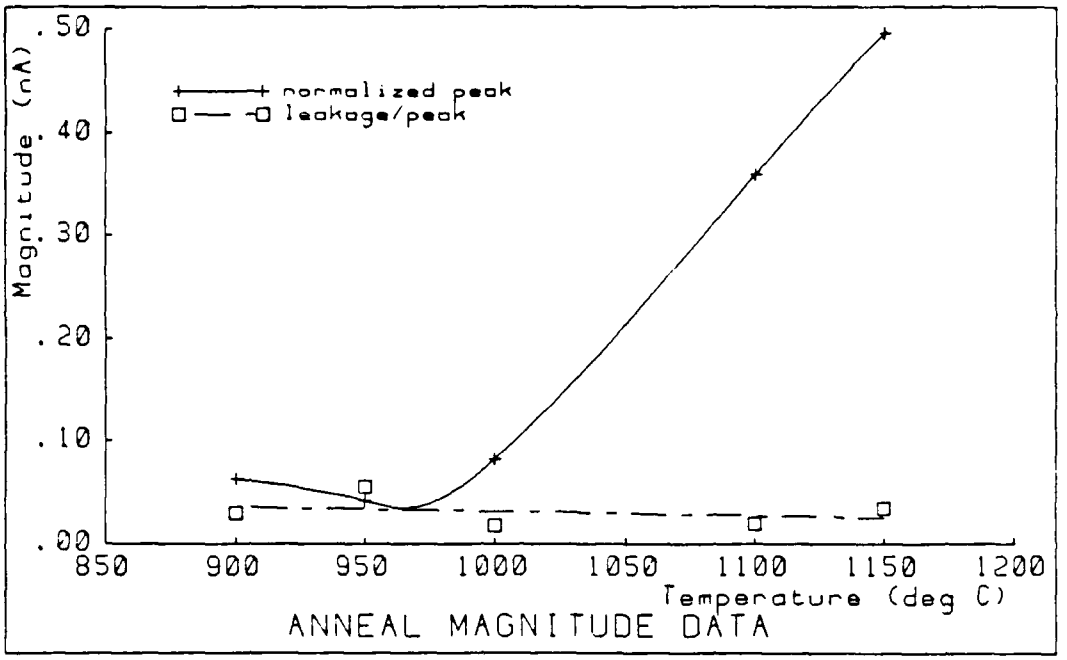

Figure 3.8: Auto-correlation peak signal measurements as a function of anneal temperature. Anneal time was 1 hour.

Colinge's anneals were done for 12 hours versus the 1 hour time for the PCE's. The shorter time may be insufficient to achieve the final grain size for a given temperature, thus, the PCE anneal at 1150°C did not produce the largest possible grain size or best mobility. Colinge's test structures were also capped with a thin oxide. This oxide layer tends to relieve the surface tension of the polysilicon grains as they increase in size and forces the poly to remain sandwiched between two oxide layers. For the PCE structures, no oxide layer is deposited on top of the polysilicon so the layer is free to expand upward. This resulted in a very rough surface topology for the layers annealled at the higher temperatures, as the polysilicon tended to clump locally. Grain sizes may grow larger than the original layer thickness in this manner and, thus, continue to improve the layer's mobility. It is unclear as to what the impact, if any, the roughness of the surface has on the absorption of optical energy from the stimulating laser beam. This may also be a contributing factor in the continued improvement of signal levels for the higher temperature anneals.

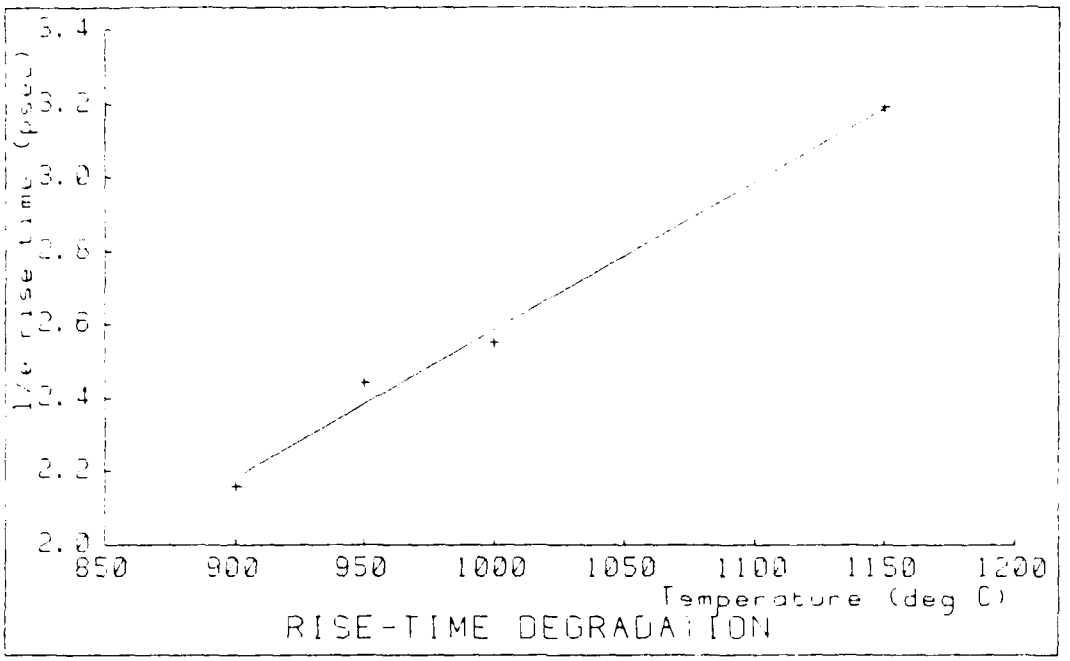

Figure 3.9: PCE $1/e$ risetime as a function of anneal temperature.

The order of magnitude increase in signal level is consistent with a study of mobility in polysilicon done by Hammond and Johnson.[3.17] They reported a change in photoexcited carrier mobilities from 6.8 to 104 $cm^2/v-sec$ between as-deposited and 1150°C annealed polysilicon films respectively. Since their films were not implant damaged, a process which degrades mobility, the reported mobility increase is expected to be somewhat greater than that observed in the PCE's. They also reported that the background (leakage) levels remained at $\approx$ 4–5% of the peak current, regardless of the mobility enhancement. Figure 3.8 shows that this is also the case with the PCE's since the plot of the leakage current over the peak current is flat at a value of approximately 3.5 percent.

While the percentage of leakage current remains constant there is some penalty to the increased signal level of the high temperature annealled films. This penalty is seen when looking at the PCE's speed as a function of the anneal temperature. Figure 3.9 uses the $1/e$ rising time of the auto-correlation measurements as an indicator of the photoconductor's speed performance. This parameter is the time it

takes the waveform to go from a value $1/e$ below the peak to the peak. For an autocorrelation measurement it should be the same as the $1/e$ decay time, in the absence of reflections on the decaying or positive time portion of the waveform. Since this ideal cannot be achieved the $1/e$ rise time is a better indicator of the speed of the photoconductor and is used in this comparison. The plot shows that the PCE speed degrades at a rate of 0.4 $psec/100°C$ for the range of anneal temperatures explored. This slowing of the PCE response is linear and present even when the signal level output is not improving with increased anneal temperature. This relationship tends to indicate that it is not solely related to the same mechanisms which lead to the mobility enhancement. One possible explanation is some kind of grain transit time limitation, particularly for large grains, but this is speculation at this point.

PCE Speed Tailoring

In addition to being able to produce very fast photoconductors for use as sampling gates in an optoelectronic sampling system, it is also desirable to have pulsing PCE's. The time response of such a device shows a very rapid turn on transient after which it remains on (or decays slowly) for a relatively long time. The sampling PCE's are made fast by the introduction of trapping sites via implant-induced damage within the photoconductive layer. Controlling the number of traps introduced should then enable the speed of the PCE response to be tailored over a limited range. The limits of the speed range are bounded on the high end by an undamaged PCE and on the low end by the circuit limitations of the structure (described in Section 3.2).

It is necessary to understand the mechanism by which the ion implantation produces damage in the polysilicon layer in order to control this process for speed tailoring. Fortunately, J.F. Gibbons has compiled a comprehensive collection of the theories proposed in this area. [3.18][3.19] Two items of interest concerning damage profiles should be noted: 1) the damage profile is generally shallower than the implanted ion profile and 2) to first order, only nuclear collisions cause damage.[3.19] The importance of this fact is that the damage, and hence the number of trapping sites, is predominately a function of the nuclear stopping power of the implant

ion. Nuclear stopping power is only a weak function of the implant energy, thus allowing the number of trapping sites to be tailored by controlling only the implant species and dose. The implant energy must only be sufficient to distribute damage throughout the photoconductive layer. This is significant in making the fabrication of PCE's directly compatible with standard IC fabrication processes and equipment. Not only is the lower energy within the capability of common implanters but they allow photoresist masking of areas where damage is undesirable.

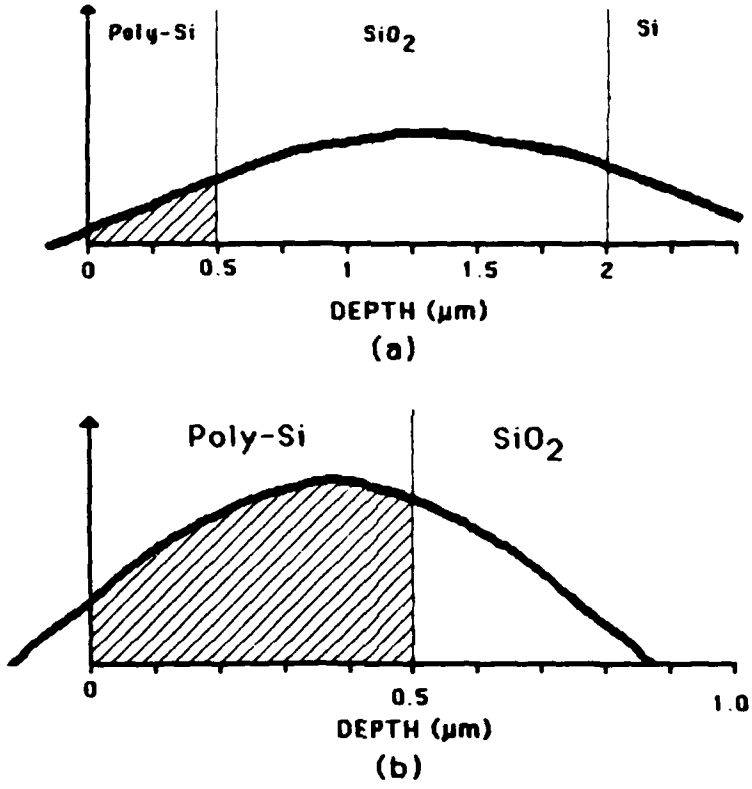

Figure 3.10: Typical damage profiles for (a) a high energy implant and (b) a low energy implant.

Figure 3.10 demonstrates the concept of optimizing the implant energy. In (a), a high energy ion is implanted resulting in a damage profile with most of the damage outside of the $0.5\mu m$ surface polysilicon layer. This is inefficient in introducing trapping sites into the PCE and requires a large dose to compensate for this. By decreasing the implant energy, as shown in (b), more of the damage profile is present

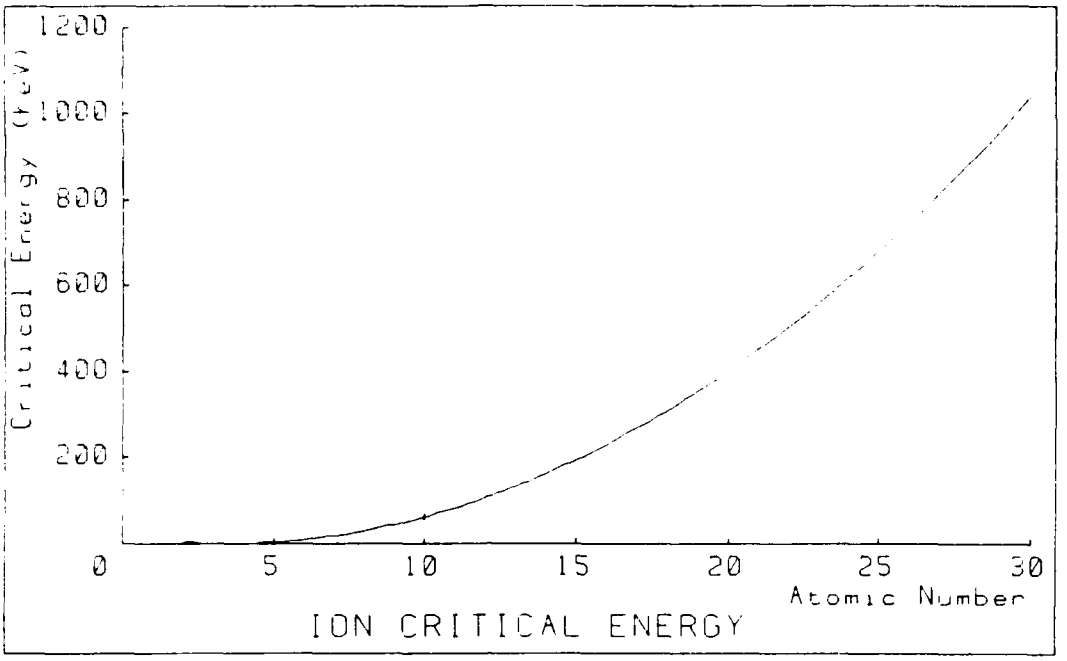

Figure 3.11: Approximation of critical energy, E_c, as a function of the implant ion atomic number.

within the PCE. Greater numbers of trapping sites are introduced for a given dose and species in this later case.

The implant energy cannot be arbitrarily reduced and still achieve the desired increase in damage production. Associated with each implant species is a critical energy, E_c, which indicates the energy below which most of the energy loss from the implant ion is due to electronic stopping, rather than the desired nuclear interactions. Care must be taken to insure that the implant energy is above E_c if significant damage is to result. For implants into amorphous silicon the critical energy can be approximated from Equation 3.1, where Z and M are the implant ion's atomic number and mass respectively. If it is assumed that the mass will be double the atomic number then Figure 3.11 is a plot of the critical energy versus atomic number. To keep E_c below 200 KeV, (the maximum capability of common implanters) species with atomic numbers below 16 are required. Silicon is the heaviest ion which can

be used for the damage implant and still meet this requirement.

$$\sqrt{E_c} = \frac{196ZM}{\sqrt{5.81 + Z^{0.667}(M+28)}}\ eV \tag{3.1}$$

Since the specific ion used for the implant has an impact upon how low an implant energy may be used there is some tradeoff in the choice of species and implant energy. Another constraint placed upon this tradeoff is that the implant species must be electrically inactive in silicon. If a dopant type ion is used the dark resistance of the PCE will decrease, rendering the device useless. Ions such as He, Ne, Ar, and Si are desirable, with the heavier species being more efficient at producing damage in the PCE. Table 3.1 gives some of the parameters for three species used in optimizing PCE damage.

Once a species and energy are selected, the dose of the implant is used to tailor the PCE time response. To estimate the dose required for a given PCE speed some mechanism is needed to compare doses of differing implants. An empirical number, the damage factor, is derived for each implant species to indicate the relative number of defects generated by a specified dose of the ion. The damage factor is based upon a Gaussian estimate of the damage profile as reported by Gibbons. [3.19] In deriving a species damage factor the implant profile is first estimated using Equations 3.2 through 3.4, whichever are appropriate for the implant energy. [3.18]

$$R \approx \begin{cases} 20\sqrt{E_o}\ \mathring{A} & E_o >> E_c \\ 0.05E_o \frac{\sqrt{5.81+Z^{0.667}(M+28)}}{Z\,M}\ \mathring{A} & E_o << E_c \\ \frac{1}{N}\int_0^{E_o} \frac{dE}{S_n^o + kE^{0.5}} & for\ all\ other\ E_o \end{cases} \tag{3.2}$$

	He	Ne	Si
Atomic Number (Z)	2	10	14
E_c (KeV)	0.32	63.8	162
Implant Energy, E_o (MeV)	6.0	1.6	0.25
Nuclear Stopping Power, S_n^0 ($eV\ cm^2$)	3.6×10^{-15}	5.1×10^{-14}	8.0×10^{-14}
Damage Profile Depth, R_d (μm)	1.32	1.39	0.37
Damage Profile Std Dev, ΔR_d (μm)	1.27	0.89	0.23

Table 3.1: Implant Species Parameters

$$\frac{R}{R_p} \approx 1 + \frac{28}{3M} \tag{3.3}$$

$$\Delta R_p \approx \frac{2\sqrt{28M}}{3M + 84} R_p \tag{3.4}$$

In these equations, R is the average total range in Angstroms, E_o the implant energy in eV, N the number of target atoms per volume, R_p the projected range, ΔR_p the standard deviation of R_p, and k a constant equal to $0.2 \times 10^{-15} eV^{0.5} cm^2$ for amorphous silicon. R_p and ΔR_p describe a Gaussian approximation of the implanted ion distribution in amorphous silicon. The polysilicon PCE layer is assumed to approximate this, allowing the results of the above calculations to be used as an estimate for the PCE structure.

Gibbons has reported a relationship between the profile of the implanted ion and the profile of the damage it causes.[3.19] Table 3.2 is a compilation of data for the specific case of a silicon target. This data relates R_p to the projected range of the damage profile, R_d, as well as their standard deviations. R_d and ΔR_d describe a Gaussian approximation of the damage distribution. By normalizing these distributions to a standard Gaussian, the relative percentage of the damage profile within a given layer (ie the PCE) can be calculated using probability tables. This method shows that approximately 11% and 10% of the damage is located within the half micron polysilicon layer for implants of 6 MeV He and 1.6 Mev Ne respectively. Contrasting to this is the 66% of the damage resident in the PCE layer for 250 KeV Si.

The percentage of the damage profile in the PCE layer does not indicate the absolute amount of damage created since, as previously pointed out, some ions are more efficient at producing damage. The damage is caused predominately by

	He	C	N	O	Ne	Si	Ar
$\frac{R_d}{R_p}$	0.893	0.819	0.811	0.808	0.804	0.799	0.810
$\frac{\Delta R_d}{\Delta R_p}$	0.782	0.842	0.857	0.872	0.899	0.939	1.071

Table 3.2: Damage profile estimates for common implant species in Silicon. [3.19]

nuclear collisions, therefore, the relative nuclear stopping powers of the implanted species are used as a normalizing factor for determining relative damage magnitudes. Nuclear stopping power, S_n^o, is estimated using Equation 3.5 [3.19] and shown in Table 3.1 for the implant species used in this research.

$$S_n^o = 2.8 \times 10^{-15} \frac{14MZ}{\sqrt{5.81 + Z^{0.667}}(M + 28)} \; eV \; cm^2 \tag{3.5}$$

By normalizing the product of an ion's nuclear stopping power and the percent of damage resident in the PCE layer to some reference condition, the relative amount of damage created for a given dose can be determined. Using 6 MeV He as a reference shows that 1.6 MeV Ne produces approximately thirteen times more damage within the PCE than the He implant for the same dose. For Si implanted at 250 KeV the damage is 133 times as much. The damage factor for a particular implant is this normalized product times the dose, again referenced to some base. A base dose of 10^{14} cm^{-2} is used in the damage factors presented here. Thus, an implant of 6 MeV He to a dose of 10^{14} cm^{-2} has a damage factor of one. A dose of 10^{16} cm^{-2} of the same ion has a damage factor of 100 and should produce 100 times more damage in the polysilicon photoconductor layer.

Assuming that the damage factor, and hence the amount of damage in the PCE, is proportional to the density of trapping sites created by the implant, then it should also be inversely proportional to the recombination time in the PCE. It is the carrier recombination time which determines the speed of the PCE's time response until the circuit limitations dominate. Figure 3.12 is a plot of PCE auto-correlation FWHM times as a function of damage factor. The expected downward trend in times as the density of traps is increased (indicated by increasing damage factors) is observed. A minimum time of approximately 5 psec is reached for damage factors above 140. For the structures used in this experiment ($15\mu m$ gaps in $100\mu m$ lines) the circuit limited FWHM should be 3.8 psec ($Z_0 C_g = 1.4$ $psec$) if the PCE's are ideal devices. Since this is obviously not the case, the observed 5 psec time is likely the circuit limited response for these devices and increasing the damage factor above the point where the plot becomes horizontal does not improve the PCE's speed response. Below this portion of the curve, however, the damage factor can be used as an

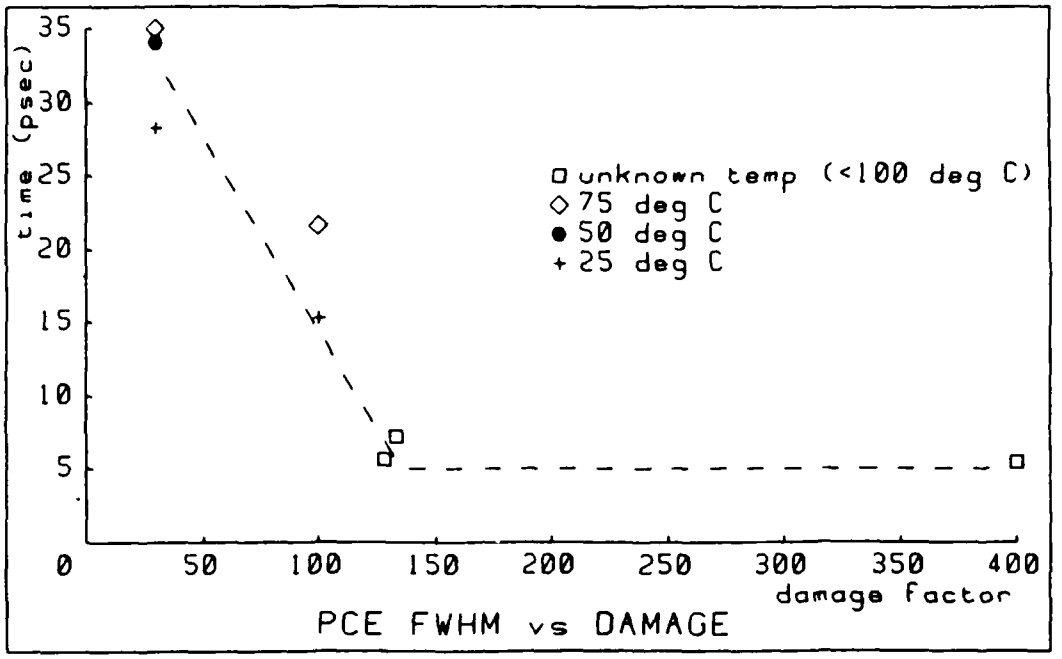

Figure 3.12: Auto-correlation FWHM times for varying damage factors and substrate temperatures during implant.

indicator of the speed response of the PCE. This allows the implant to be tailored to produce speeds slower than the circuit limited response, if that is desirable.

The spread of data points for the same damage factor in Figure 3.12 is bothersome in that it indicates a possible problem in repeatability on a wafer scale. Investigation of the cause of this dispersion shows that it is a function of the temperature of the substrate during the implantation process. The amorphousation dose of silicon is strongly temperature dependent around room temperature.[3.20] This effect allows implants at slightly lower temperatures to amorphize the layer with a much smaller dose. Figure 3.13 displays this effect by showing the deposited energy density (proportional to dose) versus 1/T for several implant species in silicon. [3.21] The steepness of the curves around room temperature result in the extreme temperature sensitivity of the amorphousation dose in this regime. In terms of PCE speed this implies that the lower temperature substrates will have relatively more damage done at a given damage factor. This is consistent with the data in Figure 3.12 and

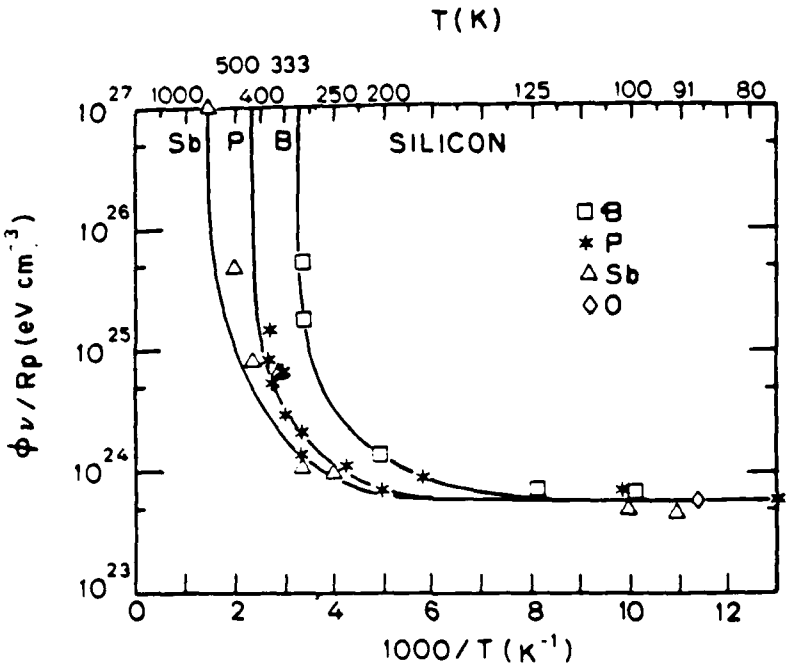

Figure 3.13: Universal curves calculated by Vook for the deposited energy density necessary to amorphize silicon as a function of reciprocal temperature. [3.21]

suggests that the substrate temperature during implantation should be controlled for optimum repeatability.

3.3.2 IC Fabrication Compatibility

The utility of very fast photoconductors on silicon substrates is enhanced if those devices can be integrated into standard IC device process schedules. Several considerations influence the meshing of the fabrication requirements of both polysilicon PCE's and other silicon devices. Figure 3.14 shows what a cross-section of an IC fabricated with such a combined process would look like. Generally, such a combined process is nothing more than a two level polysilicon process similar to those which are used to fabricate some types of Random Access Memories (RAM's).

In both the RAM and PCE applications, one level of poly is undoped for use as high value resistors or photoconductors respectively. The other layer of polysilicon is doped in some manner to be used in interconnections and transistor gates. The difference in the two level poly process used for RAM fabrication is that no high

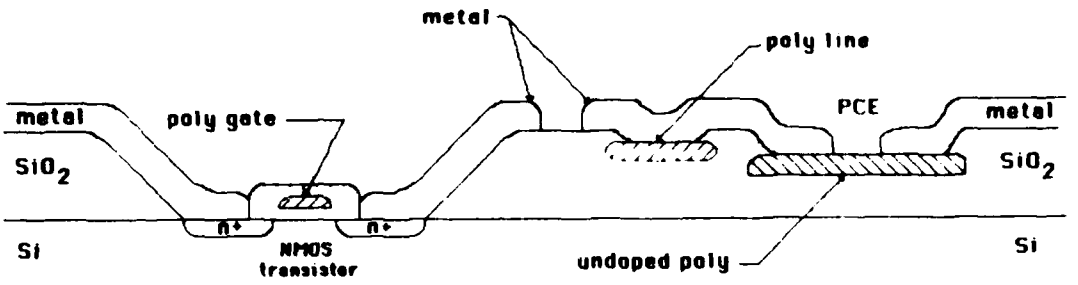

Figure 3.14: Cross-section of an NMOS-polysilicon PCE integrated circuit.

temperature anneal of the undoped polysilicon layer is performed. In order for this step to be included in the PCE fabrication (it is not necessary for PCE operation, but highly recommended to improve performance) then the undoped layer must be deposited and annealed prior to any processing steps forming critical junctions. The high temperature nature of the PCE anneal acts to substantially deepen any junctions present at the time it is performed. This dopant drive-in limits the flexibility of the process designer because the undoped poly deposition must come very early in the fabrication schedule to overcome this problem.

As in RAM fabrication, care must be taken in the design of the processing steps following the undoped poly layer deposition to insure that they do not cause this layer to become doped. This usually involves depositing oxide over the polysilicon to act as a mask. Except for contacts to high value resistors this oxide may remain over the undoped poly in RAM applications. This is not the case for the PCE as such an oxide would also mask the damage implant. This is also true of any scratch mask oxide placed over the chip to protect it after fabrication. The damage implant must be done without any interfering layers over the PCE regions if it is to be maximally effective. A scratch mask could be added after this implant, if desired, but would result in some annealing of the implant damage and degradation of the PCE's expected performance.

The PCE damage implant is not a step which is compatible with other devices fabricated on the same wafer. It is not, however, a problem after the process has been optimized to produce fast photoconductors, as described in Section 3.3.1 above. At the low implant energies which result from this optimization, non-PCE

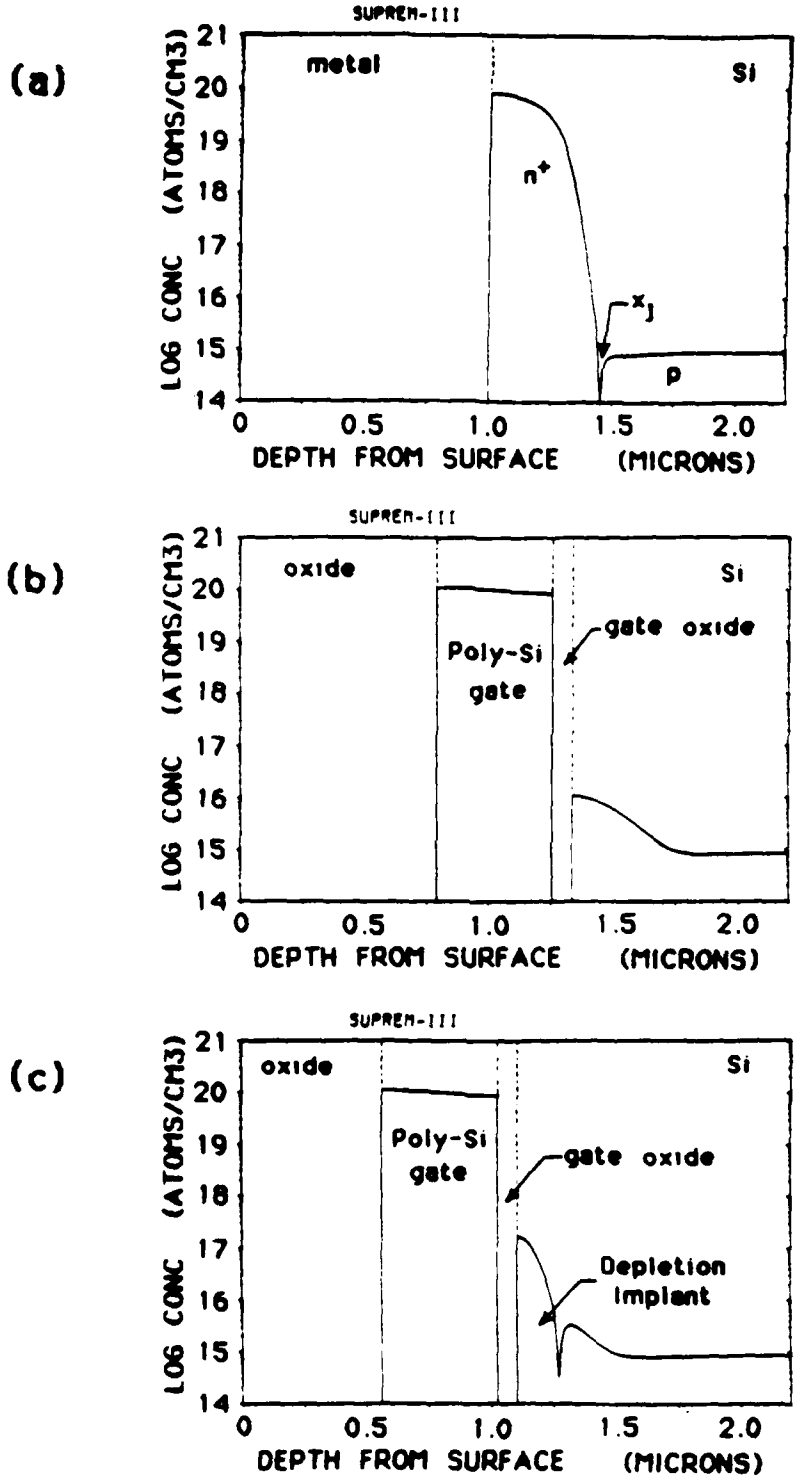

Figure 3.15: SUPREM-III profile plots of NMOS-poly PCE transistor regions: (a) source/drain region, (b) enhancement transistor gate region, and (c) depletion transistor gate region.

structures can be protected from the damage implant by photoresist. Standard photolithographic techniques can be used to define these areas at the cost of an additional mask in the process schedule.

The feasibility of developing a combined process to fabricate both PCE's and other devices on the same integrated circuit is demonstrated by the development of an NMOS-poly PCE process. This process is an adaptation of the NMOS fabrication schedule used at Stanford University to teach IC fabrication techniques to graduate students. SUPREM-III, a process simulation program capable of modeling multilayer structures [3.22], is used to aid in the optimization of the design of the fabrication schedule. Simulations of profiles at various points in a cross-section such as that shown in Figure 3.14 are performed to insure that all devices, transistors and photoconductors, are fabricated satisfactorily. Figure 3.15 shows some of the resultant profiles for different regions in the transistors. A gate oxide of 700 Å and source/drain junction depth of 0.45 μm are predicted. Calculations of threshold voltages show an enhancement threshold of $\approx$ 1.1 V and a depletion device threshold of -2 V.

The resultant NMOS-poly PCE fabrication schedule is detailed in Appendix C, Section C.2. Monitoring of different parameters during processing shows close agreement with the SUPREM-III simulations. The integrated circuits contain working transistors and PCE's in close proximity to each other. (Due to mask limitations they were not placed in the same physical circuit.) Figure 3.16 is a cross-correlation of an undamaged (pulser) PCE and a damaged (sampler) PCE on one of the wafers produced with this fabrication schedule. Because of the very fast response of the sampler compared to the pulsing PCE the correlation is a very good approximation of the time response of the pulser. It shows a step rising transient and flat pulse, both desirable if the PCE's are to be used as a source of high speed pulses for digital circuits. Figure 3.17 shows a representative drain characteristic for an enhancement mode transistor on the same chip. While the transistor is marginal in its overall performance, it demonstrates the practicality of using a PCE in an integrated circuit environment and the compatibility of polysilicon PCE fabrication with other devices.

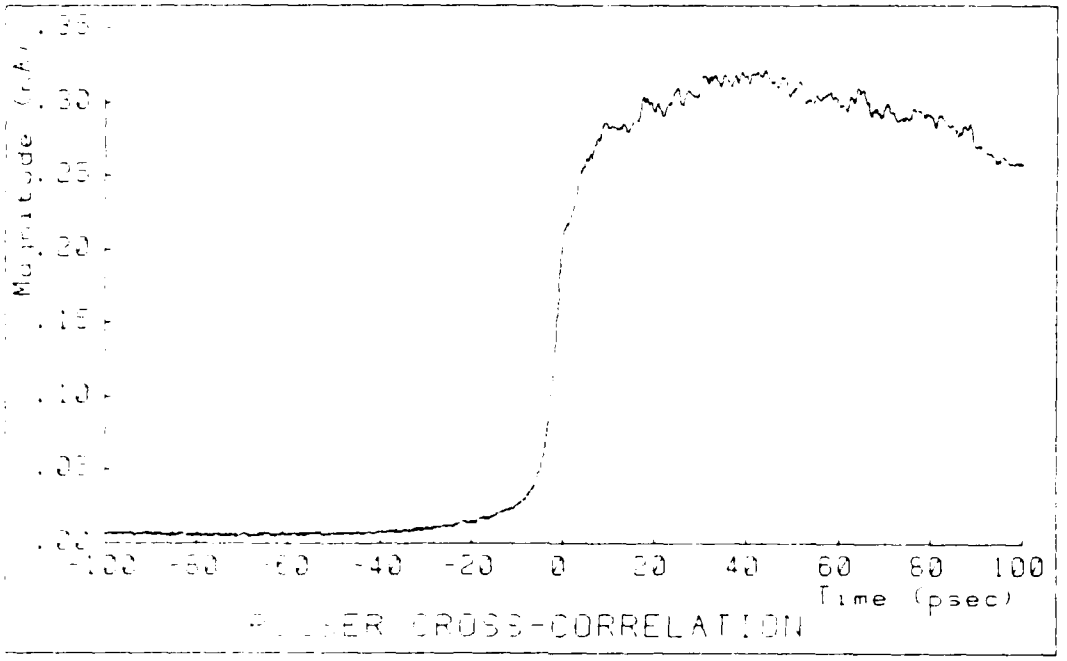

Figure 3.16: Cross-correlation measurement on a wafer processed using the NMOS-poly PCE fabrication schedule. The PCE is a 10 μm gap in a 30 μm transmission line.

3.4 Summary

This chapter provides the necessary design criteria for the fabrication of very high speed polysilicon PCE's and their placement into silicon integrated circuits. The general PCE operation requirements identified in Table 3.3 are achieved by utilizing various fabrication, material, and laser properties. Optimization of device geometry and fabrication steps produces fast photoconductors when excited by short pulse duration lasers. Using these techniques, PCE's with greater than 100 GHz sampling bandwidth have been fabricated. (See Figure 3.18) Compatibility with standard VLSI fabrication schedules was demonstrated via the development and implementation of an NMOS-poly PCE fabrication process.

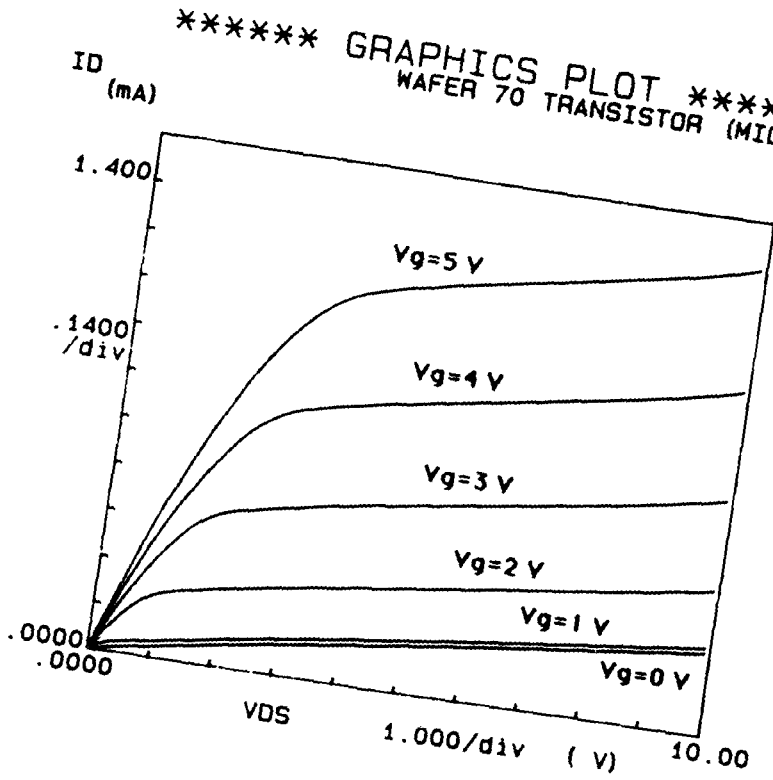

Figure 3.17: Transistor drain characteristics from NMOS-poly PCE processed wafer.

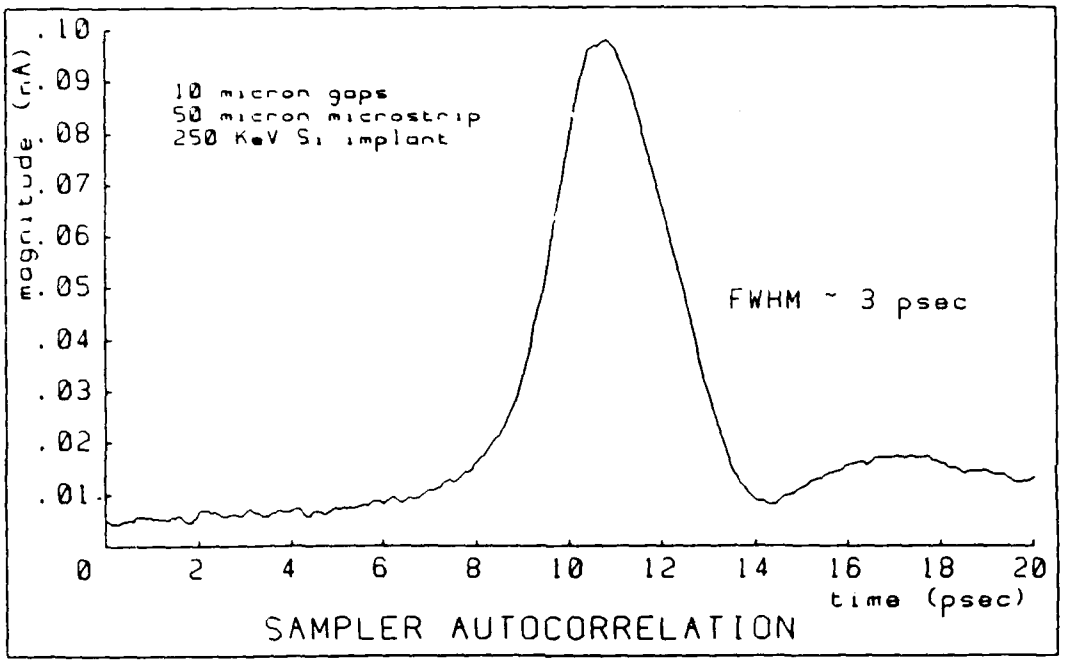

Figure 3.18: Auto-correlation measurement of PCE's demonstrating a sampling bandwidth in excess of 100 GHz.

General Requirement	Achieved by
low dark conductivity	undoped poly
rapid turn-on transient	200 fs laser excitation
rapid carrier recombination	damaged induced traps
large signal levels	improved mobility due to large poly grains

Table 3.3: PCE Operation Requirements

Chapter 4

Poly-PCE Device Modeling

To effectively use any type of device in a circuit it must be characterized and modeled so that the circuit designer can take into account its weaknesses and strengths. For a new device, such as the PCE discussed in Chapter 3, characterization of the device's performance as actually fabricated is necessary to verify that an application exists for the new circuit element. This characterization, when coupled with theoretical considerations, provide the basis for a derivation of some type of device model. If done correctly, the resultant model predicts the device's performance over a wider range than what has actually been measured during the characterization process. This chapter presents a first order attempt at such a model for the polysilicon PCE, based on measurements and theoretical analysis of the device structure. The validity of the model is verified by comparison with other measurements.

4.1 Circuit Approximation

As with other semiconductor devices, and because the photoconductor is used in a circuit, it is desirable to be able to model it in terms of standard circuit components. In the case of the PCE, the circuit approximation is suggested by an analysis of the physical structure of the device. Figure 4.1 is a cross-section of a polysilicon PCE with the device and parasitic circuit components drawn in.

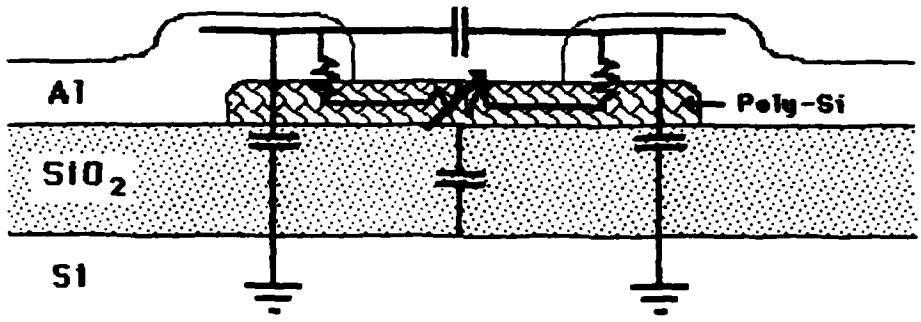

Figure 4.1: Poly-PCE cross-section with device circuit components indicated

The PCE gap is a discontinuity in a microstrip transmission line which is modeled as a capacitive π network.[4.1] The series capacitance is due to the gap in the microstrip while the shunt capacitances are from the stub end transmission lines thus formed. Another capacitance is present for the thin film PCE. It is a capacitance associated with the oxide isolation layer and shown in the figure as being between the polysilicon layer and the silicon substrate.

The polysilicon layer itself is modeled as a variable resistor. This represents the photoconductivity and the ability of the laser to modulate the conductivity of the PCE by introducing optically generated carriers. Parasitic contact resistances, generally very small, are also found between this layer and the metallic contacts. They are fixed resistances in the PCE current path. Although not shown on the figure, source and load impedances are present in the form of the microstrip characteristic impedance.

As a general circuit analysis problem this model is not exceptionally complex. It is simplified further by making some assumptions about the relative values of the elements. The first assumption is that the contact resistance from the metal transmission lines is negligible compared to the PCE gap resistance. This is a very good approximation since the contact resistance is usually on the order of 10's of ohms while even the smallest on resistance for the gap will be in the 100's of ohms.

Three of the four capacitances shown in Figure 4.1 could also be removed for a first order analysis of the device. The microstrip shunt capacitances are very small

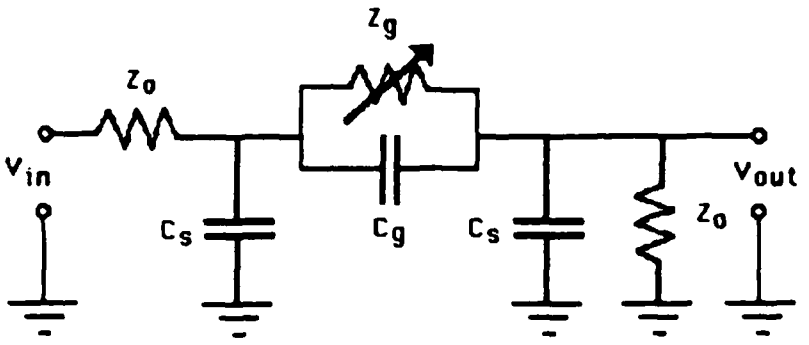

Figure 4.2: First order PCE device circuit model.

for typical IC structures (less than 1% of the gap capacitance) and do not play a significant role in determining the PCE transient response. The PCE to substrate capacitance is also ignored for the first order analysis because of its distributed nature and small relative value. For thin oxide layers this component may influence the PCE response and reduce its speed.

With all of these assumptions, the PCE could be represented by the circuit model shown in Figure 2.6. (See Chapter 2.) By keeping the shunt capacitances, however, the microstrip gap model is kept intact and this part of the PCE structure is better represented. The circuit shown in Figure 4.2 then becomes the first order circuit model for the photoconductor. This is valid for the in-line PCE and will be applied to the sampling T configuration with the minor modification of replacing the input impedance with a value of half the characteristic impedance of the microstrip. This accounts for the apparent parallel microstrip lines at the input in this configuration.

Calculating values for most of the circuit components shown in Figure 4.2 for a specific PCE geometry is done by using analytical expressions found in the literature. (See Chapter 5 for the expressions for Z_0 and Appendix A for the gap capacitance formulas.) The characteristic impedances of the microstrip are described by expressions developed by Schneider [4.2] and Wheeler [4.3] which have been modified to account for the multilayer semiconductor dielectric and the fringing fields caused by non-ideal microstrip geometries. [4.4][4.5][4.6] Gap capacitances

(both series and shunt) result from a closed form expression derived in terms of symmetrical and asymmetrical excitation circuit parameters.[4.1] Gap resistance variations, however, have not been previously modeled. Some effort is required to derive an expression for this circuit parameter before the PCE circuit model can be completed.

4.2 Gap Resistance Model

The time variation of the resistance of the photoconductive region of the PCE is a complex function of the laser pulse parameters (pulse energy, duration, wavelength, etc.), polysilicon optical properties (absorption, reflection, etc) and carrier transient response within the gap. The interaction of all of these parameters cannot be explicitly analyzed because their nature is not known exactly. Reasonable approximations are used to simplify the problem and allow for the development of an expression describing the optical modulation of the gap resistance.

4.2.1 General Expressions

The resistance of a block of any material is described by Equation 4.1 in terms of ρ, its resistivity, and its physical dimensions. Here w is the width, h the height, and l the length of the material. For a semiconductor the resistivity is a function of the carrier concentration (doping) and mobility as shown by Equation 4.2. Electron and hole concentrations are represented by n and p respectively while μ is the average carrier mobility and q the unit electric charge.

$$R = \rho \frac{l}{w\ h} \tag{4.1}$$

$$\rho = \frac{l}{q\mu(n+p)} \tag{4.2}$$

When the PCE is not illuminated, Equations 4.1 and 4.2 describe the dark resistance of the device. SUPREM III simulations of the PCE fabrication schedule indicate that the doping of the PCE layer should be approximately $10^{12} cm^{-3}$. This doping results from impurities trapped in the thermally grown oxide which later

diffuse into the polysilicon layer during the high temperature anneal. The carrier concentration in the PCE layer is approximated by this doping level (the majority carrier concentration). [4.7] For a 0.5 μm thick PCE fabricated as a 10 μm gap in a 100 μm microstrip, a dark resistance of 12.5 MΩ is therefore predicted, assuming an effective mobility of 100 $cm^2/v-sec$. The value of mobility is based upon measurements made by Hammond and Johnson on similar polysilicon films [4.8] and is also consistent with results reported by Kim et al.[4.9]

Illuminating the PCE gap causes photogeneration of excess carriers. Equations 4.1 and 4.2 still describe the gap resistance except that now the resistivity is modified by the additional holes and electrons present. For a pulse optical stimulation (as opposed to constant illumination) it is the transient nature of these excess carriers which determines the time response of the gap resistance.

4.2.2 Continuity Solutions

The time response of the carrier concentrations in the PCE can be found from a solution to the continuity equations. (Equation 4.3) For this analysis it is assumed that a constant applied electric field is present and that the carrier lifetimes are short enough when coupled with the material's low mobility to prevent a significant space charge from developing. The illumination is also assumed uniform, even though the exponential absorption of the optical energy with depth makes this assumption valid only for relatively thin films. With these assumptions, however, the continuity equations lose their spatial dependence and reduce to expressions in terms of the generation rate, G, and the recombination rate, R, for the respective carriers. Equation 4.4 shows the simplified expressions.

$$\begin{aligned}\frac{\partial p}{\partial t} &= -\mu_p p(x)\frac{\partial E(x)}{\partial x} - \mu_p E(x)\frac{\partial p(x)}{\partial x} + D_p\frac{\partial^2 p(x)}{\partial x^2} + (G_p - R_p)\\ \frac{\partial n}{\partial t} &= \mu_n n(x)\frac{\partial E(x)}{\partial x} + \mu_n E(x)\frac{\partial n(x)}{\partial x} + D_n\frac{\partial^2 n(x)}{\partial x^2} + (G_n - R_n)\end{aligned} \tag{4.3}$$

$$\frac{\partial p}{\partial t} \approx G_p - R_p \qquad \frac{\partial n}{\partial t} \approx G_n - R_n \tag{4.4}$$

Carrier Recombination

Recombination rates for the continuity equations are approximated using Schockley, Read, Hall recombination. Surface recombination effects are ignored for a first order estimate and it is assumed that the capture cross-section for holes and electrons are equal. This later assumption is consistent with defect concentrations of mixed deep donor and acceptor levels as generally exhibited by near intrinsic polycrystaline semiconductors.[4.10] The resultant expression for recombination becomes:

$$R_n = R_p \approx \frac{(pn - n_i^2)}{(n + p + 2n_i \cosh\left(\frac{E_t - E_i}{kT}\right))\tau_0} \tag{4.5}$$

where n_i is the intrinsic carrier concentration, E_t the energy of the traps, E_i the intrinsic Fermi energy, and τ_0 the carrier characteristic time which is inversely proportional to the density of traps, the thermal velocity and the capture cross-section. The carrier concentrations, n and p, are the total number of carriers and may be rewritten as $n_0 + \Delta n$ and $p_0 + \Delta p$ respectively, where the subscript 0 denotes equilibrium concentrations and the Δ prefix indicates changes from that condition.

A variety of implants are used to generate the trapping sites in the photoconductive region and a determination of the effectiveness of these sites for the different species has not been done. An optimistic approach is adopted, and the energy of the traps, E_t, assumed to be in the middle of the band-gap. It is when this condition of $E_t = E_i$ is met that the traps display maximum efficiency. [4.11] Equation 4.6 is now used to describe the hole and electron recombination rates.

$$R_n = R_p = \frac{(p_0\Delta n + n_0\Delta p + \Delta n\Delta p)}{(p_0 + n_0)\tau_0 + (\Delta n + \Delta p)\tau_0} \tag{4.6}$$

This expression is valid for both the low and high level injection regimes experienced during the excitation and decay of a typical photoconductor. Integrating the continuity equations with R_p and R_n approximated as shown leads to a double exponential decaying transient. This is consistent with the work of Hwang et al. on InP photoconductors [4.10] as well as the measurements made by Hammond and Johnson on polysilicon films. [4.8] The general validity of the assumptions made in this derivation seem to be independently verified experimentally.

Optical Generation of Carriers

The generation rates for holes and electrons are equal since a hole-electron pair is generated for each incident photon (assuming unity quantum efficiency). The actual rate at which these carriers are produced by a laser pulse is dependent upon the energy, wavelength, and time response of the pulse in addition to the absorption and reflective properties of the photoconductive layer. For annealled polysilicon, it is assumed that it demonstrates the same optical characteristics as bulk silicon because of its large average grain size.

The percentage of optical energy absorbed by a material from a perpendicularly incident source is determined by three factors: (1) the surface reflectivity, (2) the material's absorption coefficient at the wavelength of the incident light, and (3) the thickness of the material. With $\mathcal{R}$, α, and T representing each of these factors respectively, Equation 4.7 represents the fraction of the optical energy absorbed in a thin film.[4.12] This fraction is proportional to the total number of photogenerated carriers which will be generated in the PCE.

$$\frac{E_a}{E_i} = (1 - \mathcal{R})(1 - e^{-\alpha T}) \tag{4.7}$$

The time response of a CPM dye laser is usually assumed to follow a $sech^2$ temporal behavior.[4.13] Thus, if E_{max} is the peak laser pulse energy, then the carrier generation rate is:

$$G = \frac{(1 - \mathcal{R})(1 - e^{-\alpha T})A_{eff}}{\hbar\omega} E_{max} sech^2(t) \tag{4.8}$$

where ω is the laser pulse frequency and A_{eff} the effective illuminated area of the gap.

The peak energy of the laser pulse is not a parameter easily measured, particularly on the femtosecond time scales common with the pulses produced by CPM lasers. However, the total pulse energy, E, is easily measured and represents the time integral of the product of the peak energy and the $sech^2$ time response. The expression which results from this integration (Equation 4.9) describes the time response of the cumulative energy in the pulse after some scaling and time shifting

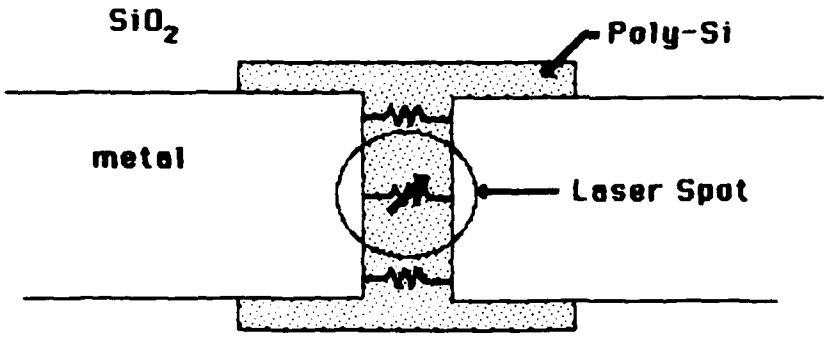

Figure 4.3: Rectangular PCE illuminated by a circular laser spot.

are preformed. In this expression the argument of the tanh term scales the time to the laser pulse's FWHM time[4.14] and shifts the pulse start time to time zero (as opposed to being centered at zero).

$$E(t) = E\left(\tanh\left(\frac{t}{0.567t_{FWHM}} - 4\right) + 1\right) \tag{4.9}$$

The time response of the number of photogenerated carriers is calculated from Equation 4.9 and the time constant terms in Equation 4.8. This gives the total number of carriers optically generated as a function of time:

$$c_g(t) = \frac{E(1-\mathcal{R})(1-e^{-\alpha T})A_{eff}}{\hbar\omega}\left(\tanh\left(\frac{t}{0.567t_{FWHM}} - 4\right) + 1\right) \tag{4.10}$$

Integrating Equation 4.6 with respect to time and subtracting the result from Equation 4.10 provides a solution to the continuity equations (Equation 4.4) which describe the time dependent excess carrier concentrations. These excess carriers provide the mechanism for the time varying gap resistance.

4.2.3 Gap Geometry Modifications

The effective illuminated area of the gap used in Equation 4.10 is neither the total gap area nor the area of the laser beam incident on the structure. In Figure 4.3 it can be seen that three regions of different illumination are present when a circular laser beam is focused on a rectangular gap. Physically, there is no sharp

delineation between these various regions, except at the gap-metal transitions. Assuming a uniform illumination within a circular focused laser spot enables simple geometrical relationships to be used in establishing the actual area of the gap which is illuminated. Within the gap, but outside of the laser spot, are regions denoted by fixed resistors in the figure. These peripheral areas do not receive any optical stimulation and remain at constant values associated with the dark resistance of the PCE material of the appropriate dimensions. In this configuration, the gap width and thickness are constant and the only dimensional parameter varying is the length of the unilluminated region. This length will be the total gap length (the microstrip width) minus the effective length of the illuminated area.

Within the laser spot are two different regions of illumination, the PCE gap and the region of overlap with the metal transmission lines. There is an optimal focusing condition associated with this overlap. The resistance of the gap will be very high if there is little or no overlap, but it will also be high if the overlap is too great and the majority of the optical energy wasted on the metal. Auston [4.15] has determined that optimum focusing occurs when the ratio of the gap width to spot diameter is two thirds.

Within the portion of the gap illuminated by the laser beam there are also two regions displaying different characteristics, although only a single variable resistance is shown in the figure. In the central region of the spot, the beam overlaps the metal contacts and uniform illumination is present in a rectangular area of photoconductive material. Geometric relationships are used to determine the area of this region based upon the gap width, x, and the focusing ratio. (See Appendix A) On either side of this region are areas of the beam spot which do not overlap with the contacts. The distributed resistance across the gap in these regions is a combination of illuminated and dark resistances. As an approximation of this effect the area is calculated as if the regions were triangular in shape and then modeled as a rectangular region of the same total area, but extending completely across the gap. This introduces some errors since the region is modeled as parallel resistances instead of series resistances. The portion of the spot which falls in these regions is small and does not have a major impact upon the resistance calculation.

The effective illuminated area, A_{eff}, is calculated by summing the areas of the last two regions. The method described above is not the quickest way to calculate A_{eff}. For the calculation of the optically generated carrier time response, it is much easier to subtract the areas subtended by the arcs of the overlapping regions from the total spot area. This subtraction method, however, does not lend itself readily to calculating the total gap resistance from a parallel resistive network model. On the other hand, the method described first is particularly suited for the calculations required by the model.

4.2.4 Simplified Gap Resistance Model

An adequate first order model of the PCE gap resistance is based on the expressions derived for the carrier recombination rate (Equation 4.6), the generation rate (Equation 4.8), and the effective illuminated area. The results of these calculations can be put into Equation 4.4 and integrated to solve for the time dependent carrier concentrations needed by Equations 4.1 and 4.2 to ultimately calculate the gap resistance. This procedure is computationally intensive and slow when simulated using a computer. Since numerous geometries are possible and multiple simulations are to be performed it is desirable to simplify the model to decrease the computation time required for each iteration. The integration of Equation 4.4 is the most time consuming step, so it is here that the most benefit can be gained from simplification.

Equation 4.6 describes the carrier recombination rate for both carrier types in the gap. This equation is characterized by a double exponential decay in the time domain of the excess carrier concentrations due to the presence of both high and low level injection. The nature of the decay transient in polysilicon films is such that one exponential term accounts for greater than 95% of the total response.[4.8] It is, therefore, reasonable to approximate this decay as a single exponential and expect that the results will not differ significantly from a full solution. This is borne out by actual calculations, as Figure 4.4 shows. In this graph both the full solution and the single exponential approximation are plotted for the same gap, excitation and characteristic time conditions. The only difference in the curves comes at the end of the transient where the resistance is returning to its dark value. The high dark

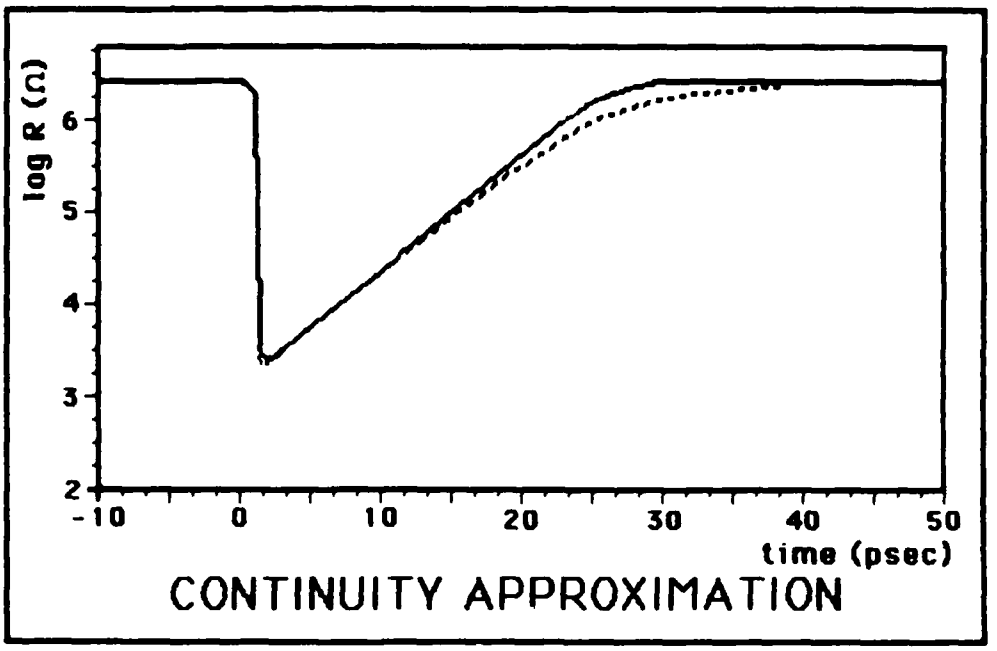

Figure 4.4: Gap resistance calculations using full SRH recombination (—) and single exponential decay approximation (- -).

resistance allows substantial errors to be tolerated in this region without impacting adversely on the gap model. Even though Hwang et al.[4.10] report errors of as much as a factor of 2.5 when using such a single exponential approximation, their work describes only the carrier concentrations. Incorporating the concentrations into the PCE gap resistance model makes the single exponential response tolerant of these approximation errors. The estimated error in the resistance transient is much less than 10% for all cases explored. This is acceptable given the accuracy of the expressions used to calculate the other circuit components.

Using the single exponential decay allows the gap resistance calculation to be simplified by skipping the integration required by the use of the continuity equations. The time response of the optically generated carriers (Equation 4.10) can be multiplied directly by the exponential decaying term to determine the time dependent excess carrier concentration (Equation 4.11). A carrier recombination rate, τ_r,

is used to define the single exponential decay.

$$\Delta c(t) = c_g(t)e^{\frac{-t}{\tau_r}} \tag{4.11}$$

The excess carrier concentration of Equation 4.11 is combined with the general resistance and resistivity formulas (Equations 4.1 and 4.2) to derive a time dependent resistance in terms of the gap width, x, illuminated area, A_{eff}, thickness, T, and carrier parameters. The steady state carrier concentrations are combined into a single term, $c = n_0 + p_0$, and represented by a single average mobility, μ.

$$R(t) = \frac{x}{q\mu(c + \Delta c(t))A_{eff}T} \tag{4.12}$$

The complete gap resistance model is composed of a parallel resistance network to account for the differing resistance of each of the varying illumination conditions described in Section 4.2.3 above. The individual resistances are calculated using Equation 4.12 with A_{eff} representing only the area of the particular region of concern. The excess carrier concentration, $\Delta c(t)$, is also only that portion of the excess carriers which are present in the region for which the resistance is being calculated. For the unilluminated portion of the gap it is zero, while the other regions contain a proportion of the carriers based upon that proportion of the total illuminated area which is resident in the region. Combining all the resistances in a parallel network then allows the model to account for all of the geometry, laser, and material parameters which impact upon the time response of the gap resistance. The resultant time response for the resistance is demonstrated in Figure 4.5 for various assumed carrier recombination times. The structure simulated is a polysilicon PCE fabricated as a 10 μm gap in a 100 μm microstrip line on 0.5 μm thick annealed polysilicon. The turn-on transient is seen to be controlled by the laser excitation, while the turn-off is determined by carrier recombination.

4.3 Model Verification

A polysilicon PCE device model results from the use of the gap resistance expression, derived in Section 4.2, in the circuit approximation of Section 4.1. The time

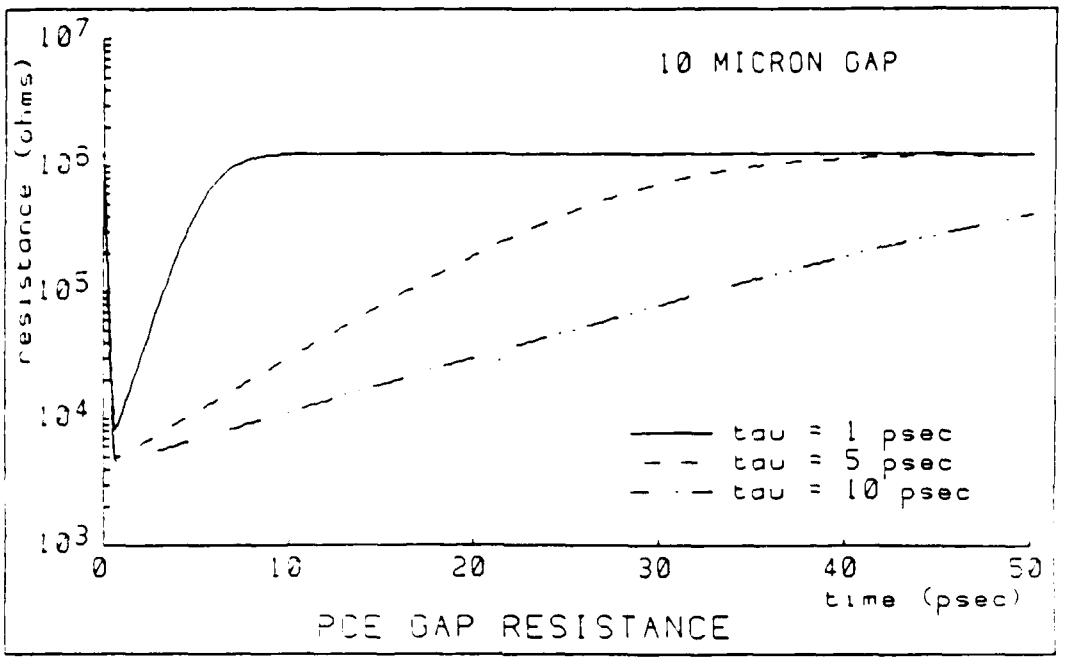

Figure 4.5: Gap resistance response for varying recombination times using the simplified model.

response (or frequency response) of the circuit is then determined using circuit analysis techniques. The complex nature of the resulting expressions (See Appendix A) makes it imperative to use numerical analysis to determine the PCE response. The PCE model is implemented in a computer simulation program, MIPCEM (See Appendix D), which provides the PCE output response for a structure and excitation defined by the user. Figure 4.6 is a plot of a pulser (undamaged) PCE (10 μm gap in a 100 μm microstrip) response for three assumed carrier characteristic times. The substrate is 350 μm silicon with a 1.5 μm oxide isolation layer. Optical excitation is assumed to be a 610 nm pulse of 200 femtosecond duration and 40 pJ energy. The plots show not only the increased on-time and peak magnitude with increased recombination times, but also the increasing $1/e$ rise time with increased peak magnitude. This later result is the same phenomena observed in the data for the PCE response versus anneal temperature presented in Chapter 3. Since an increasing recombination time correlates with an increasing mobility, as observed with annealling the polysilicon film, the model is apparently consistent with the

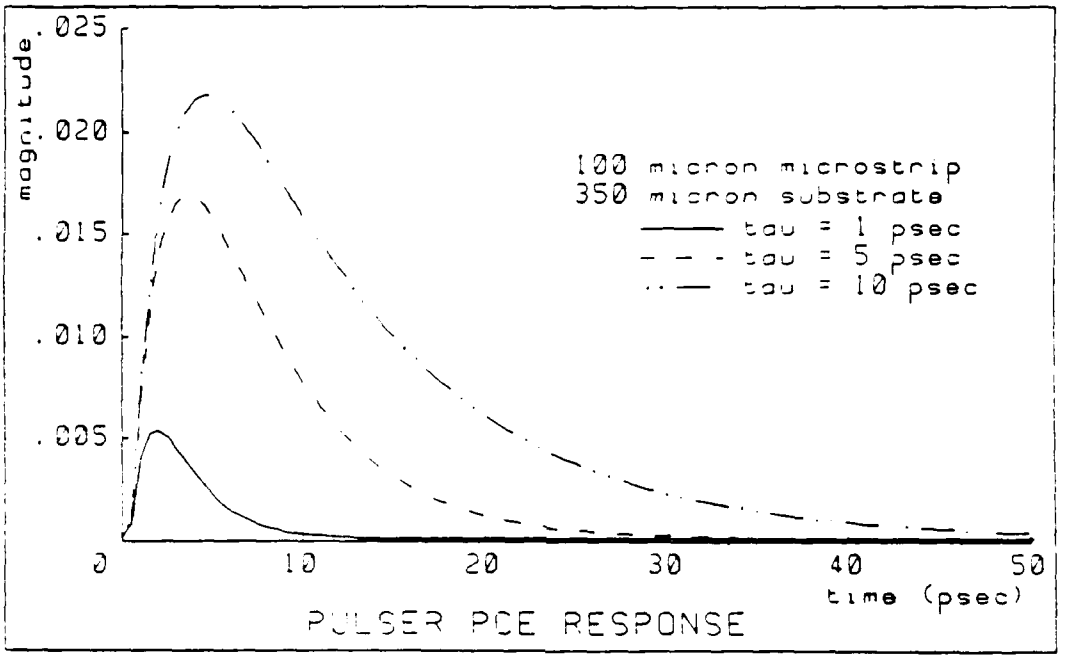

Figure 4.6: Calculated PCE responses for varying recombination times.

data from the anneal experiment. Another consistency is the slight delay observed in the model's response before the PCE begins to react to an optical excitation occurring at time zero. It is caused by the charging of the gap capacitance [4.16] and has been measured by Auston et al. for amorphous silicon. [4.17] Further verification of the applicability of the PCE model is obtained by comparing the predicted steady state and time responses with experimental measurements.

4.3.1 DC Response

The circuit of Figure 4.2 reduces to a single variable resistance for the steady state case. This resistance is the optically modulated gap resistance. If the gap is protected from all optical stimulation it should be possible to measure the dark resistance predicted by the gap resistance model of Section 4.2.

The high resistances expected make it impossible to use a standard ohmmeter for the measurement of dark resistances. An alternative method is to perform I-V measurements of the gap and then calculate the slope of the curve to determine the

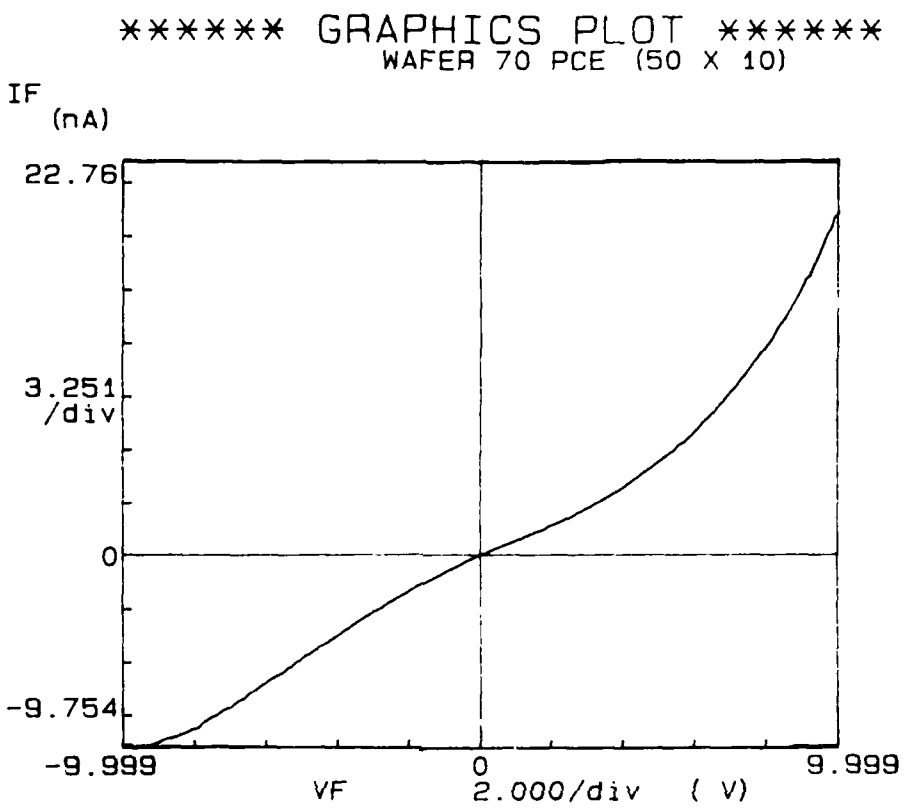

Figure 4.7: I-V curve for a PCE (10 μm gap in 50 μm line) prior to receiving the damage implant.

resistance. For the current research this is accomplished using an HP4145 Parametric Analyzer to automatically sweep the applied voltage, monitor the current, and plot the I-V curve. The sample is placed on a grounded vacuum chuck in an enclosed and darkened probe station. Figures 4.7 and 4.8 show representative I-V curves for polysilicon PCE's prior to receiving the damage implant and after the implant respectively.

The non-linear I-V characteristic shown in Figure 4.7 is disturbing from the stand point that the resistive polysilicon layer should demonstrate a linear behavior, regardless of the lifetime of the carriers within the gap. Several authors have offered theories to explain the tendency of polysilicon resistors to display this type of non-linear behavior. They may provide some insight into the PCE measurement. Korsh and Muller [4.18] postulate that the non-linearity is due to the creation of a surface

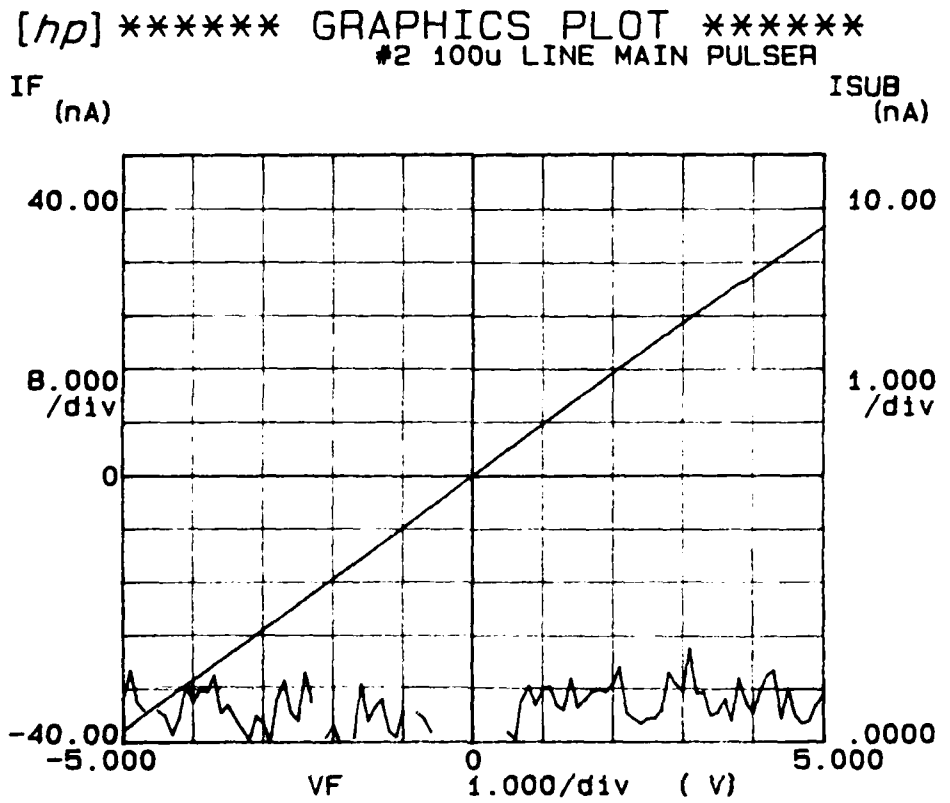

Figure 4.8: I-V curve for a PCE (15 μm gap in a 100 μm line after receiving a damage implant of 6 MeV He to a dose of $3 \times 10^{15}/cm^3$. The lower curve is the leakage current from the PCE to the substrate and shows only noise.

depletion zone and potential barrier at the polysilicon grain boundaries. Lu et al. [4.19] attribute the same phenomena to high field conduction in the non-uniform structure of the polysilicon film. Both theories, however, predict and model I-V curves which tend to decrease in slope with increasing voltage rather than the observed increasing slope.

A more recent theory of conduction in polysilicon [4.9][4.20] proposes a model which is consistent with the undamaged PCE data. This theory uses a novel treatment of the grain boundary in predicting general I-V characteristics. The predicted curves are linear, but an explanation for the non-linear measured curves is provided. I-V curves such as that shown in Figure 4.7 are the result of two series p^+i junctions operating in forward and reverse bias modes. These junctions mask the intrinsic

I-V characteristics of the undoped polysilicon. For the data shown in Figure 4.7, the junctions are not identical since the curve is not symmetric about the origin.

The diode-like behavior and non-ohmic nature of the contacts is a serious problem for a sampling PCE if it persists after the damage implant. Fortunately, as Figure 4.8 demonstrates, this is not the case. This I-V curve is from a PCE (15 μm gap in a 100 μm line) which received a relatively small amount of damage (damage factor = 30) and represents a dark resistance of approximately 120 $M\Omega$. The implant used to tailor the carrier lifetimes also apparently destroys the diode characteristics of the contacts and makes them ohmic. This is essential to using the PCE as a sampler. An undamaged PCE may be used as a pulser without problems, since a constant voltage is applied across the gap and the linearity of the I-V response does not come into play in determining its performance.

Measurements of the dark resistance of 15 μm polysilicon PCE's after the damaging implant resulted in values ranging from 25 $M\Omega$ to 200 $M\Omega$, with most of the values under 90 $M\Omega$. The predicted value for the structure is 18.7 $M\Omega$. The higher measured values are likely due to a combination of lower doping levels and lower mobility in the polysilicon than predicted. It is expected that the mobility should be somewhat lower than the 100 $cm^2/v–sec$ assumed, because this value comes from undamaged polysilicon measurements and ion implantation tends to lower carrier mobility. A difference of up to an order of magnitude may be possible, although a lowering of the mobility to 25-50 $cm^2/v-sec$ is probably more reasonable. The remaining errors in the dark resistance calculations are easily attributable to doping variations.

4.3.2 Transient Response

Verification of the PCE device model's transient response is inherently difficult due to the inability to directly measure the actual transient response of a single polysilicon PCE. The extremely fast nature of the device precludes the use of standard measurement equipment such as sampling oscilloscopes. An alternative is to use the device to measure itself, in a cross-correlation measurement. This is what is done by the pulsed laser measurement system at Los Alamos. (See Chapter 2) To

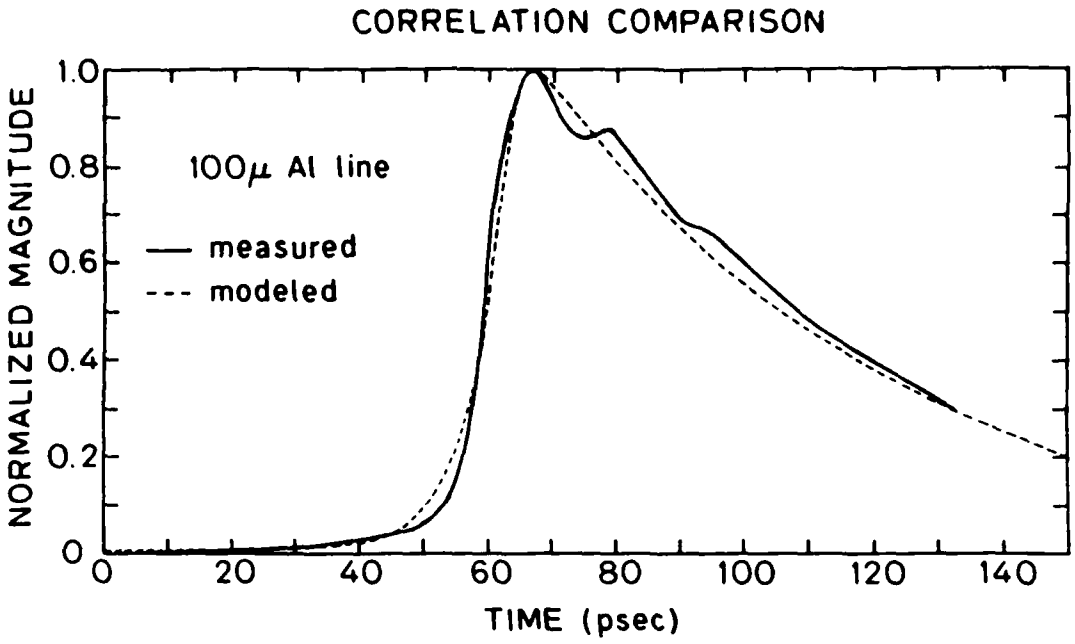

Figure 4.9: Comparison of measured and modeled correlation results for a 15 μm gap sampler at a distance of 500 μm from an undamaged pulser.

compare the model with the measurements of actual devices, the same type of environment must be created for the model as that used in the experiment. This is accomplished via a computer simulation of the experimental measurement process using the MIPCEM program developed by the author. (See Appendix D)

MIPCEM uses the PCE model to calculate the cross-correlation between a pulsing and sampling PCE separated by a specified distance of transmission line. Simulations are run of several measurements taken on a wafer with PCE structures consisting of 15 μm gaps in 100 μm microstrip lines. The samplers on the wafer received a damage implant of 1.6 MeV Ne to a dose of $3 \times 10^{15}/cm^3$ (damage factor = 384) and should have a response which is circuit limited. The pulsers are masked during the implantation process and, therefore, have a long decay time. Due to the uncertainty of the mobility and doping concentrations within the gap, the magnitudes of the measurements are not considered when comparing experimental and simulated correlations. The linearity of the PCE response makes this unnecessary for verifying the transient response.

Figure 4.9 is a comparison of the model performance and the measured data for the second sampler (distance = 500 μm) along the transmission line. Both curves have been normalized to their peak values to remove any magnitude disparity and allow direct comparison of the waveforms. The only parameter used to fit the model is the recombination time of the sampling PCE. The measurement is assumed to be close to an ideal cross-correlation and the decaying transient is therefore used to give an estimate of the pulsing PCE's recombination time. This recombination time is approximately 53 psec.

The simulated correlation plot resulted from a sampler recombination time of 5 psec and demonstrated the best fit with all other parameters constrained. Shorter recombination times gave a better fit to the leading edge of the waveform at the expense of the decay transient, while the opposite is true of longer times. The best fit occurs at a recombination time longer than the circuit limited response time predicted theoretically. This may be due to errors introduced by using experimental data as a source for the decaying transient's characteristic time, rather than allowing that parameter to vary also.

For the simulation plotted, two regions showing error are evident. The decaying transient of the measurement shows a secondary peak which the simulation does not model. This second peak is due to the reflection of the pulser's electromagnetic pulse from the backplane of the wafer. The excitation of the pulsing PCE produces a spherical wave, which not only launches a signal on the microstrip, but also spreads through the substrate. [4.21] The reflected signal is picked up by the sampling PCE at some delay in time from the primary signal because of the longer path length and different effective dielectric constant for a wave propagating entirely through the substrate. No attempt has been made to model this effect other than to estimate the relative delay of the reflected pulse compared to the primary peak. Calculations of the delay time assume that the low frequency dielectric constant for silicon is applicable and are within 20% of the observed times.

The rising portion of the simulated waveform differs from the measured data in that it does not rise as steeply as actually observed. This is the region where the highest frequency components of the response dominate. For a circuit limited

sampler ($\tau = 1.5$ *psec*) the sampling bandwidth is approaching 100 GHz. (See Appendix B for how this is determined.) At these high frequencies, the models used to calculate the component values of the gap capacitances and microstrip impedances are questionable. Unfortunately, there are no models available for these parameters in this frequency range and the PCE model is limited by their restrictions. Capacitance and impedance values are assumed to be valid to enable PCE model calculations to be performed, but using these inaccurate values will generate errors of the type seen in the rising transient of the simulation. It is estimated that the maximum error observed in this plot is 10%. The worst case component model, excluding the high frequency range, has a reported error of less than 7% so this does not represent a serious degradation of the PCE model. The predicted performance of the PCE is reasonably accurate except for the fastest devices and acceptable for a first order model.

4.4 Summary

Development of a device model which accurately predicts the device's performance over its useful application range is a requirement for good circuit design. Constant effort is expended to update and develop models for new configurations or applications. This chapter has presented a first order model of the polysilicon PCE and validated its applicability by experimental comparison.

The PCE model is based upon fundamental semiconductor theory through the use of the continuity equations. While a model using the equations directly is possible, its computational complexity precludes rapid turn around of iterative calculations. Several approximations are proposed to simplify the computations while maintaining reasonable accuracy. This is true, not only of the continuity equations, but also of the device circuit approximation. The resultant model is readily implemented via a computer simulation program, MIPCEM.

Comparisons of the model with experimental data is given for both the DC and transient responses. Anomalies observed in the DC response are explained using a current theory of polysilicon conduction. Accounting for these anomalies and

process uncertainties brings the DC model in close agreement with measured results. The transient response is also found to be in close agreement with experiment, demonstrating less than 10% error. Most of the error can be traced to a break down in published models for the gap capacitance and microstrip impedance at the extremely high frequencies found in the PCE. First order approximations are successfully made with the proposed model.

Chapter 5

IC Microstrip Characterization

The increasing speed of integrated circuits is resulting in designs which are limited by the propagation characteristics of the interconnections.[5.1] This tendency becomes even more predominate as devices and circuits are scaled to smaller dimensions. [5.2][5.3][5.4] An important application of the polysilicon PCE developed during this research is its use in a very fast optoelectronic sampling system. Such a system is capable of high signal to noise measurements to bandwidths in excess of 100 GHz. An implementation of this sampling system is demonstrated in this chapter. The propagation characteristics of microstrip transmission lines fabricated on silicon substrates are explored. Measurements of picosecond pulse propagation allows for the verification of microstrip models at frequencies where no experimental data currently exists. If the models are verified and the propagation on IC interconnections characterized, then their impact upon high speed circuits may be more fully understood. This understanding is necessary if the speed of devices being developed is to be fully taken advantage of.

5.1 Propagation on IC's

Integrated circuit interconnections (Figure 5.1) can be described in terms of microstrip transmission lines because of the similarity in their geometries. It is thus

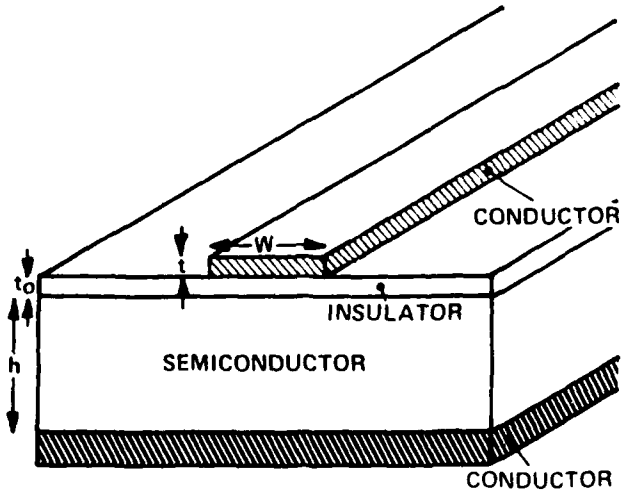

Figure 5.1: General microstrip structure on a semiconductor substrate.

possible to analyze IC interconnections as microstrip lines and compute parameters which characterize the transmission line. The type and detail of the analysis required for a particular system depends upon its performance and purpose. For simple, low speed circuits, a simple analysis is all that is needed to characterize signal propagation. On the other hand, complex models are needed to represent high speed systems.[5.5]

5.1.1 General Microstrip Theory

Models for microstrip transmission lines have been the object of much research over the last twenty years. [5.6][5.7][5.8][5.9] Various computational approaches have been taken to analyze and model microstrip on different substrates. (Ruehli provides a good overview of these in [5.5]) Accurate and complete analysis, however, requires elaborate mathematical models and time consuming numerical techniques. Simpler approaches are available utilizing quasi-TEM mode calculations combined with frequency dependent expressions that can achieve accuracies within one percent of the full analysis. [5.10] It is this later approach which is taken in this work.

The abrupt dielectric interface associated with the microstrip geometry of Figure 5.1 makes it impossible for the structure to support a single mode of propagation. Microstrip, however, transmits the bulk of its energy in a field distribution which closely resembles the TEM mode and is usually referred to as quasi-TEM. [5.9] Analysis of these fields has been done using various static techniques [5.8][5.11] [5.12][5.13] which, when combined with closed form frequency dependent functions, describe high frequency microstrip operation.

The characteristic impedance, Z_0, of a TEM transmission line describes the square root of the ratio of the line inductance to line capacitance.

$$Z_0 = \sqrt{\frac{L}{C}} \tag{5.1}$$

If this microstrip structure is related to the same structure, but with the substrate replaced by an air dielectric, then the ratio of the resulting line capacitances defines the effective dielectric constant, ϵ_{eff}, for the original transmission line. This parameter is used to transform calculations based upon air dielectric microstrip to other substrates, including mixed dielectric substrates.[5.14] At zero frequency an expression for ϵ_{eff} has been calculated by Schneider [5.15] and subsequently modified by Owens. [5.16]

$$\epsilon_{eff} = \begin{cases} \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2}\left(1+\frac{10h}{w}\right)^{-0.555} & for\ \frac{w}{h} > 1.3 \\ \frac{\epsilon_r+1}{2}\left(1 - \frac{1}{2H'}\left(\frac{\epsilon_r-1}{\epsilon_r+1}\right)\left(\ln\frac{\pi}{2} + \frac{1}{\epsilon_r}\ln\frac{4}{\pi}\right)\right)^{-2} & for\ \frac{w}{h} < 1.3 \end{cases} \tag{5.2}$$

$$where\ H' = \ln\left(\frac{4h}{w} + \sqrt{16(\frac{h}{w})^2 + 2}\right)$$

Using this parameter, the characteristic impedance at TEM frequencies for the particular substrate under investigation is then calculated. [5.15][5.17]

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\epsilon_{eff}}}\ln\left(\frac{8h}{w} + \frac{w}{4h}\right) & w < h \\ \frac{120\pi}{\sqrt{\epsilon_{eff}}}\left(\frac{w}{h} + 1.393 + 0.667\ln\left(\frac{w}{h} + 1.444\right)\right)^{-1} & w > h \end{cases} \tag{5.3}$$

These expressions assume a zero thickness conductor and have a reported relative error of less than 2% when compared to a rigorous analysis. [5.18] This is improved

somewhat by applying a corrective factor to account for the fringing fields present with a finite conductor thickness. Bahl et al. [5.19] have suggested the use of an effective width parameter in Z_0 to account for this effect. The effective width, w_e, replaces w in Equation 5.3.

$$w_e = \begin{cases} w + \frac{1.25t}{\pi}\left(1 + \ln\left(\frac{4\pi w}{t}\right)\right) & \frac{w}{h} \leq \frac{1}{2\pi} \\ w + \frac{1.25t}{\pi}\left(1 + \ln\left(\frac{2h}{t}\right)\right) & \frac{w}{h} \geq \frac{1}{2\pi} \end{cases} \tag{5.4}$$

In addition, the effective dielectric constant must also be modified. Equation 5.2 is used to calculate a base number and then corrected for the finite conductor thickness by subtracting the term $\Delta\epsilon_{eff}$.

$$\Delta\epsilon_{eff} = \frac{(e_r - 1)\frac{t}{h}}{4.6\sqrt{\frac{w}{h}}} \tag{5.5}$$

The use of Equations 5.2 through 5.5 provides a representation of microstrip structures at TEM frequencies. They provide the basis for the high frequency model which is used for picosecond pulse propagation.

5.1.2 High Frequency Microstrip Models

The quasi-TEM analysis of microstrip transmission lines begins to loose accuracy at frequencies above 1 or 2 GHz. Above these frequencies, in the super high frequency (shf) range and above, the characteristic impedance and effective dielectric constant become frequency dependent. In addition, new loss mechanisms become important and the attenuation also demonstrates a frequency dependence.

The cause of the frequency dependence of the microstrip parameters is the hybrid mode of propagation which is supported. Since pure TE or TM modes cannot exist on a microstrip some coupled version of these is the actual mode of propagation. As the frequency is increased, the mode-coupling efficiency increases and the effective dielectric constant rises. This leads to the phenomena, present on all microstrip lines, of dispersive propagation—signals at different frequencies propagate with different phase velocities.

Several methods for evaluating the variation of ϵ_{eff} with frequency and the resultant dispersion are available. [5.20][5.21][5.22] [5.23][5.24][5.25] [5.26] Most are

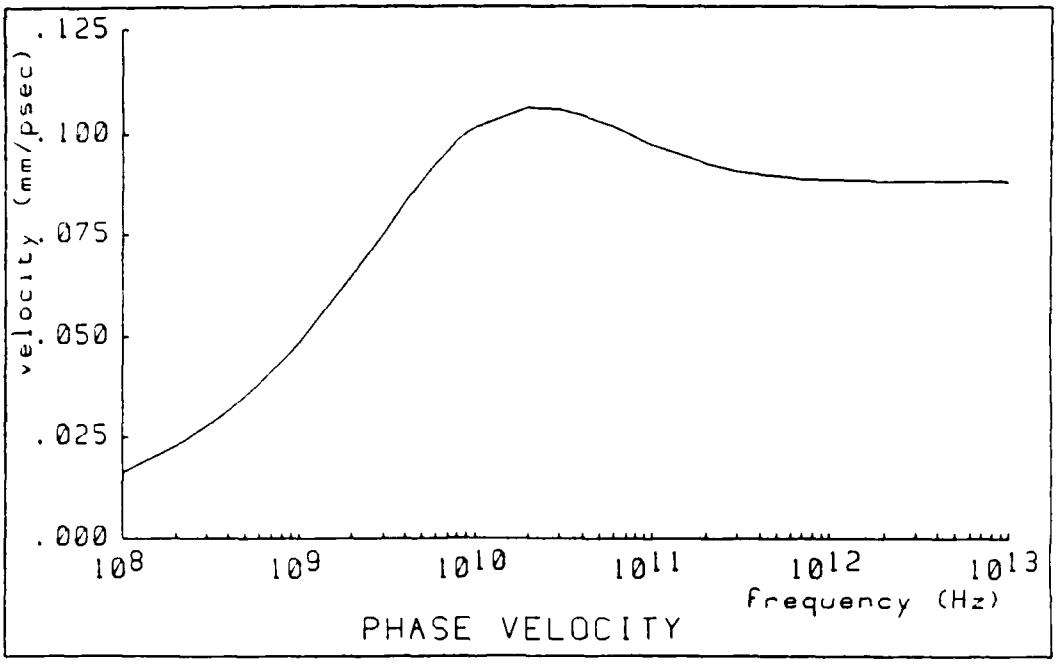

Figure 5.3: Calculated phase velocity variation on silicon substrates with frequency.

For semiconductor substrates, where the finite conductivity of the substrate and the finite resistivity of the metal conductor introduce attenuation, this expression is not valid. It has been shown [5.27] that by using previously derived expressions for conductor loss, α_c,[5.7] and dielectric loss, α_d, [5.28] available in the literature, the attenuation (α) and phase (β) factors for the transmission line may be calculated.

$$\alpha^2 = \frac{-f_1 + \sqrt{f_2}}{2} \tag{5.8}$$

$$\beta^2 = \frac{f_1 + \sqrt{f_2}}{2} \tag{5.9}$$

where $f_1 = \beta_0^2 - 4\alpha_c\alpha_d$ and $f_2 = (\beta_0^2 + 4\alpha_c^2)(\beta_0^2 + 4\alpha_d^2)$

These equations are arrived at by an analysis of a transmission line modeled with shunt and series resistances to represent the dielectric and conductor respectively. Figure 5.3 illustrates the resultant variation in phase velocity when considering losses in both the substrate and dielectric. Figure 5.4 shows these losses. The increase in the conductor loss at frequencies above 10 GHz is due to the skin effect in the metal conductor. [5.29]

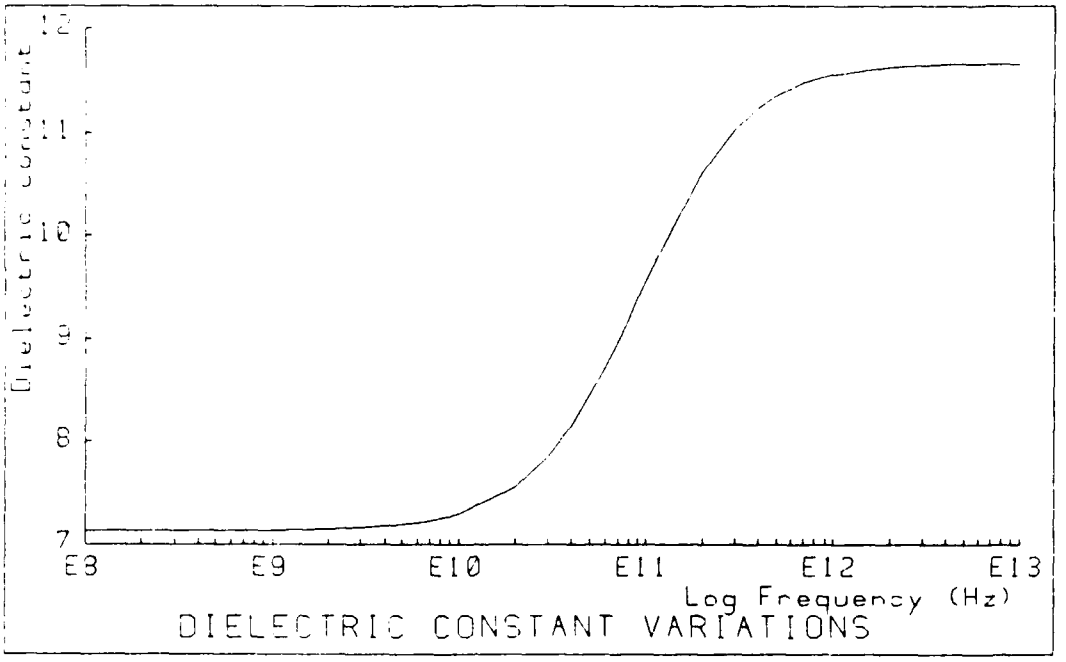

Figure 5.2: Computed frequency dependence of microstrip effective dielectric constant, ϵ_{eff}, for a silicon substrate (e_r=11.7).

very complicated and require detailed calculations. However, Yamashita et al [5.23] have derived an expression by curve-fitting to data from a full-wave analysis of the problem.

$$\sqrt{\epsilon_{eff}(f)} = \sqrt{\epsilon_{eff}(0)} + \frac{\sqrt{e_r} - \sqrt{\epsilon_{eff}(0)}}{1 + 4F^{-1.5}} \tag{5.6}$$

where $F = \frac{4fh}{c}\sqrt{e_r - 1} \times \left(0.5 + \left(1 + 2\log\left(1 + \frac{w}{h}\right)\right)^2\right)$

In this expression, f is the frequency and c is the speed of light in a vacuum. Figure 5.2 is an example of the application of this formula, which is accurate to approximately 1 percent. The microstrip simulated is 100 μm wide aluminum on a 350 μm silicon (e_r=11.7) substrate. It can be seen that the frequency dependence does not begin until above 1 GHz as expected.

If the substrate material is lossless (ie insulating) then a propagation factor, β_0, is expressed as [5.27]:

$$\beta_0 = 2\pi f \frac{\sqrt{\epsilon_{eff}}}{c} \tag{5.7}$$

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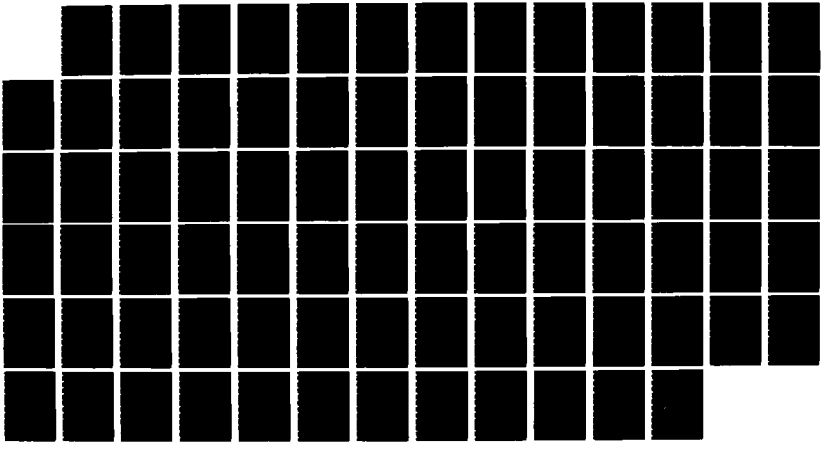
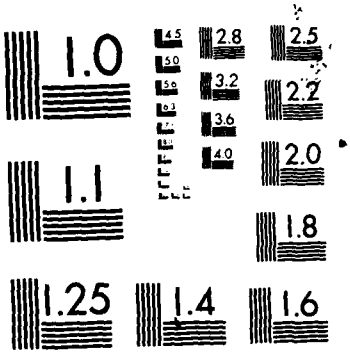




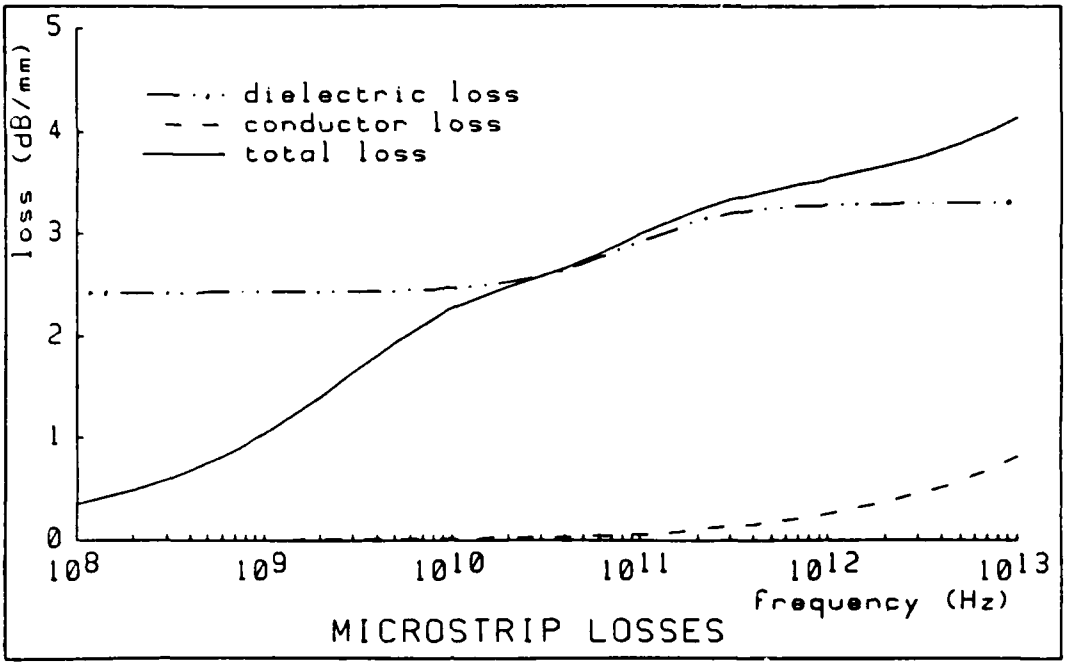


Figure 5.4: Modeled conductor loss, α_c, dielectric loss, α_d, and total loss, α, as a function of frequency on silicon.

5.1.3 Picosecond Pulse Propagation

Recent interest in picosecond pulses on integrated circuits is the result of the demands for faster circuits and the reported decrease in propagation delays per gate to 10–30 picoseconds. [5.30] Few authors, however, have adequately combined all the microstrip parameters in a comprehensive model capable of predicting the actual pulse waveshape with propagation on a lossy semiconductor substrate. Li et al. [5.31] calculated microstrip time-domain waveforms using the dispersion models of Yamashita et al. [5.23], but could not produce exact pulse shapes due to approximation limitations. Hasegawa reported the first calculated time-domain representations of propagating waveforms using his equivalent circuit model. [5.32] This model allows exact waveforms to be computed, however, the fastest response modeled in this manner was on the order of only 100 psec. Goossen combined much of the previous work into an analysis of the dispersion and loss on microstrip transmission lines fabricated on silicon substrates. [5.29][5.33] Propagating waveforms

calculated based upon this effort are consistent with previous results and show the effects of dispersion and the high loss regime at super high frequencies. Figure 5.5 is an example of exponential pulse propagation on an aluminum microstrip line on 100 $\Omega - cm$ (a) and 10 $\Omega - cm$ (b) silicon substrates. The impact of substrate conductivity is readily observed.

5.2 Sampling Measurements for Model Verification

Polysilicon PCE's produce pulses of the type modeled by Goossen in his theoretical analysis. This opens up the possibility of directly verifying the microstrip model with measured data. A series of measurements are made by using the same test structure used for PCE characterization. This time, however, the PCE generated pulse is measured at all of the sampling points and comparisons made with the theoretical analysis.

5.2.1 Measurement and Simulation Techniques

The polysilicon PCE test structure (Figure 3.3 in Chapter 3) is ideal for measuring microstrip propagation characteristics as it provides for waveform sampling at four different distances from the pulse source. A sufficient length of transmission line is also available beyond the last sampler to prevent any reflections from the open stub end from returning in time to interfere with the measurement. This is important in acquiring clean data which does not have to be mathematically deconvolved from the reflected signal—an operation which introduces additional errors.

The procedure for making a series of propagation measurements is the same as that for doing PCE characterization except that four measurements are made in succession. The incident laser energy on both the pulser and sampler PCE's is monitored to allow any short term fluctuations in the laser between measurements to be compensated for. Care is taken to insure that the measurement environments (ie pulser bias, focus, etc) for each of the four samplers are as close to identical

as possible. This minimizes any errors introduced between measurements by the experimental procedure.

To provide a mechanism for the comparison of measured and theoretical waveforms, the microstrip propagation model is included in the MIPCEM program. A variety of parameters can be calculated, but the utility of the program allows for an exact simulation of the measurement process based upon the PCE model developed in Chapter 4 and the microstrip model presented in Section 5.1 above. Since this effort is directed towards the validation of the microstrip model, various methods are used to minimize any errors introduced by the PCE model. Usually this involves fitting the MIPCEM output to the measured data at the first (100 μm) sampler to determine the parameters to be used for the PCE model. These parameters are then assumed to be valid at the other three samplers.

Figure 5.6 shows how this technique is applied for the case of a 100 μm wide microstrip. The experimentally measured data are shown in (a) with magnitudes normalized to the peak of the first sampler. Successive curves are the measurements at the second (500 μm), third (1000 μm), and fourth (2000 μm) samplers. In (b) are seen the plots of the MIPCEM simulations of the same measurements, again normalized to the peak of the first sampler's output. This first curve is fit to the measured data taken at the first sampler by varying the sampling and pulser PCE carrier recombination times until a reasonable agreement with the measurement is achieved. Subsequent curves are produced by using the same recombination times, but allowing the pulse waveform to propagate a longer distance down the microstrip.

The similarities between the measured and simulated waveforms in the figure can easily be observed. Both the model and the simulation show the expected dispersive propagation with high losses. This is evident from the increasing rise times of the pulses (pulse broadening) and smaller peak magnitudes with increasing propagation distance. There are, however, some important differences which indicate some limitations to the microstrip simulation. These are addressed in the following sections.

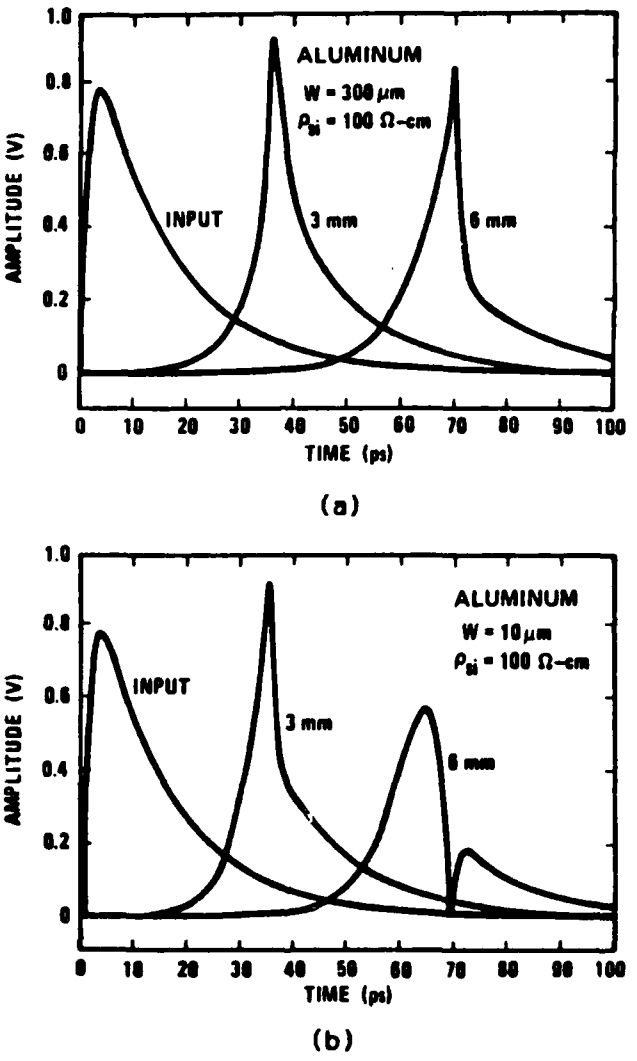
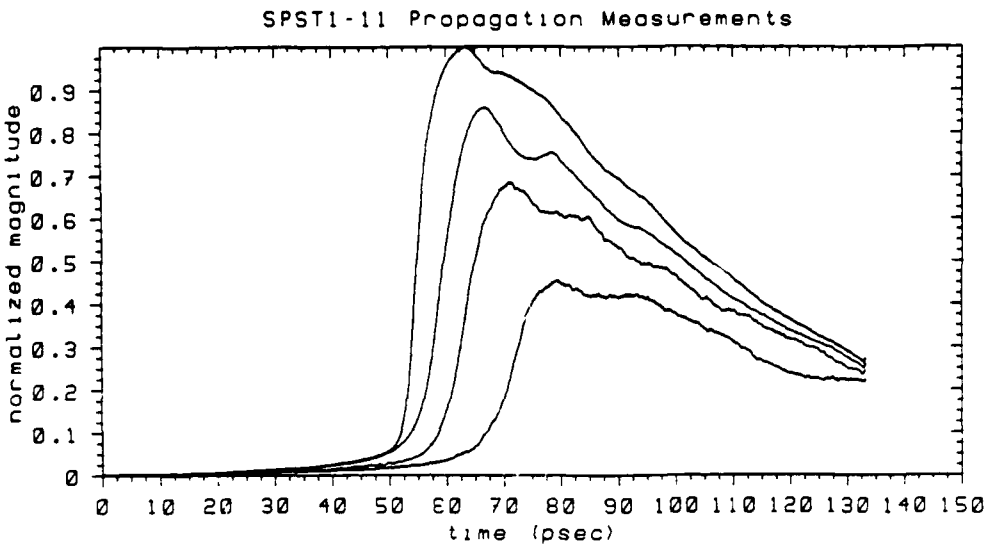


Figure 5.5: Predicted picosecond pulse propagation on a (a) 100 $\Omega - cm$ and (b) 10 $\Omega - cm$ silicon substrate. [5.33]



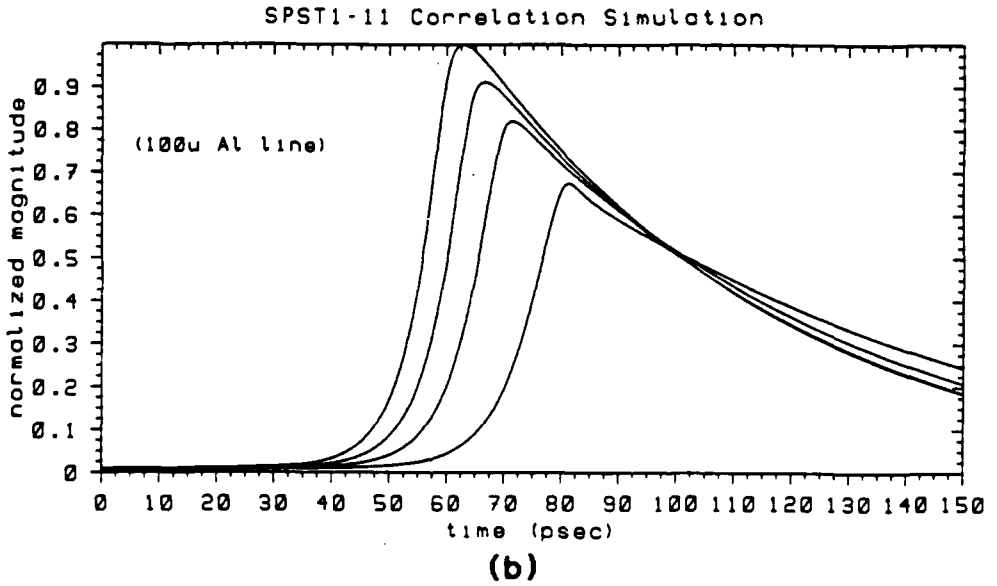


Figure 5.6: High frequency waveform propagation measurement (a) and simulation (b).

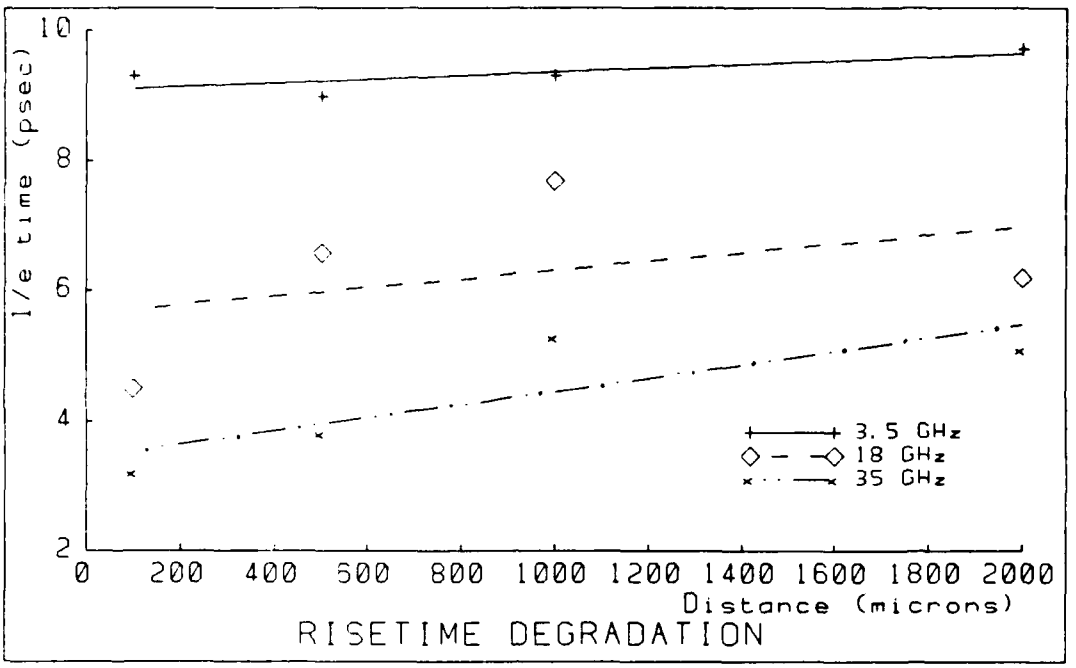


Figure 5.7: Dispersion induced risetime degradation for pulses of varying frequency ranges.

5.2.2 Dispersive Propagation

The data shown in Figure 5.6 is the first that shows actual dispersive propagation on a silicon substrate. The degradation in the rise time of the pulse as it propagates down the microstrip is due to a broadening caused by the slower velocity of the lower frequency components (as shown in Figure 5.3). The pulse produced by the pulser PCE, which is undamaged in this sample, has a long decay time and is thus fairly broadband in the frequency components it contains. Other measurements of faster, higher frequency pulses also exhibited the same phenomena of rise time degradation with propagation distance.

Figure 5.7 plots the $1/e$ rise time as a function of the sampler distance from the pulser PCE for three different sets of measurements. All of the structures are identical 100 μm wide, 0.8 μm thick aluminum lines with 15 μm PCE gaps fabricated on the same substrate (350 μm p-type $< 100 >$ silicon with a resistivity of 14.5 $\Omega - cm$ topped by a 1.5 μm oxide layer). The damage factor for the

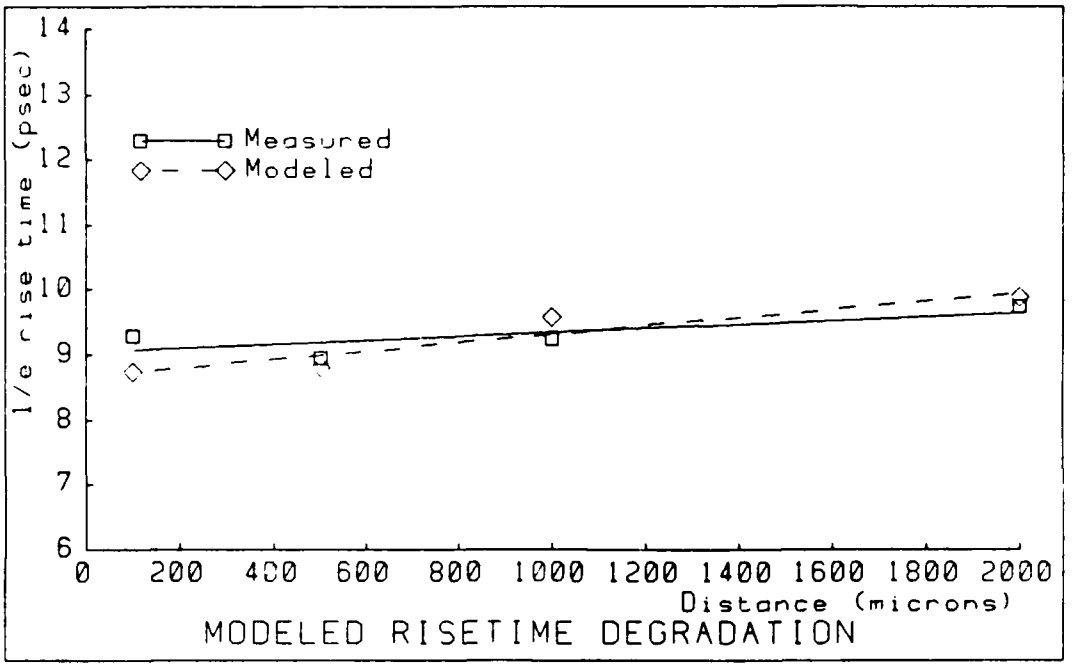


Figure 5.8: Measured and simulated risetime degradation comparison for the 3.5 GHz pulse.

pulser PCE is successively increased for curves 1, 2, and 3 yielding faster pulses. Using the derivation outlined in Appendix B, the 3 dB frequency for the pulses are estimated to be 3.5 GHz, 18 GHz, and 35 GHz respectively. The resultant data shows that all of the pulses exhibit dispersive propagation with the higher frequency pulses demonstrating increased rates of rise time degradation. (Degradation is 0.277 psec/mm for curve 1, 0.688 psec/mm for curve 2, and 1.02 psec/mm for curve 3.) This is an expected result based upon the microstrip model. The faster pulses contain a proportionally greater percentage of frequencies in the higher, more dispersive, range and should therefore demonstrate greater dispersive effects.

The microstrip model implemented in the simulation program predicts the extent of the dispersion induced rise time degradation with reasonable accuracy. Using the simulation shown in Figure 5.6 as representative, Figure 5.8 compares the measured and simulated $1/e$ rise times. The model tends to overestimate the degradation ($\approx$ 0.5 psec/mm), but most of this error may be attributed to errors in fitting the data to the first sampled waveform. There is a difference of $\approx$ 0.7 psec between the

measured and fitted model values at the 100 μm sampler. The PCE parameters used in the model result in a slightly faster (higher frequency component) pulse than is in fact present. This error causes the dispersive rise time degradation to be greater in the simulated pulse because it contains more of the faster frequencies.

5.2.3 Propagation Velocity

The rate at which a pulse moves down a transmission line is a very important parameter, particularly for circuits involving critical timing applications or pulse synchronization. At the high frequencies present with picosecond pulses, propagation velocity varies with frequency and hence with the shape and duration of the pulse. The optoelectronic measurements of waveforms after varying propagation distances provides a method to characterize this effect.

The relative time at which the peak magnitude of pulse occurs is used as a reference point for velocity determination. With four sampling measurements, a total of six propagation times can be calculated for distances ranging from 400 μm up to 1900 μm. The time from the pulser PCE to the first sampler is not used because of delays associated with the generation of the pulse and the point source nature of the excitation. This later problem results from focusing the laser beam on a gap much smaller than the microstrip width. The wavefront produced at this point is not totally perpendicular to the direction of propagation until it has gone some distance down the microstrip line. It is initially assumed that by the time the wave reaches the first sampler it has established itself as a perpendicular front, although this may not be rigorously true for the wider microstrip lines.

Figure 5.9 reports the results of calculating the various time differences between the peak magnitudes of the measurements for each of the three samples used above. What is interesting about this data is the almost identical slope for the three cases shown. This indicates a relatively constant velocity of $\approx$ 113–114 μm/psec regardless of the duration of the pulse. This is somewhat surprising considering all three pulses are definitely in the dispersive propagation range of frequencies. The explanation is straight-forward, however, when it is realized that by observing the

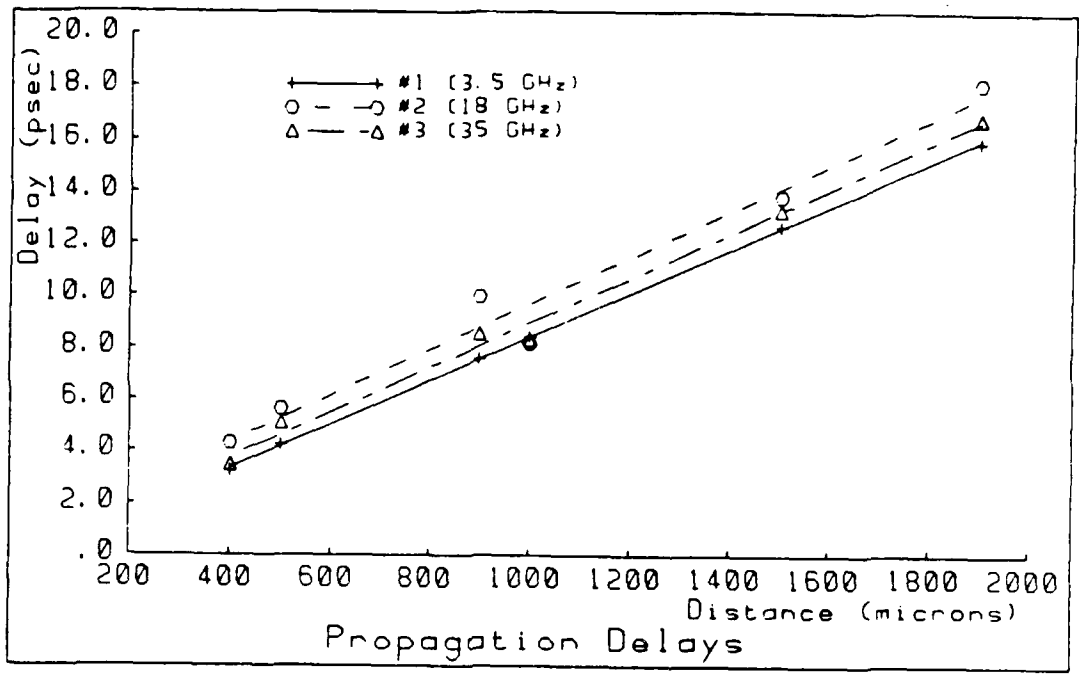


Figure 5.9: Propagation delays for pulses of varying frequencies: (1) 3.5 GHz, (2) 18 GHz, and (3) 35 GHz.

relative delays of the peak magnitude we are actually measuring the group velocity and not the phase velocity of the signal.

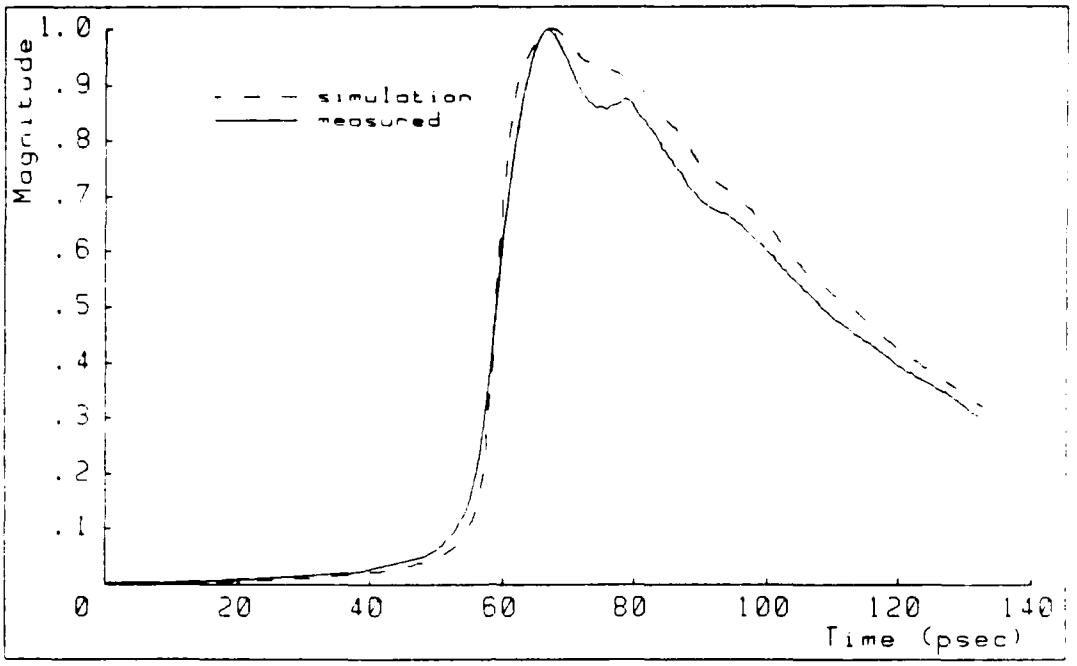
Since the phase velocity is not measured with the technique above, an alternative approach must be used to compare the measured data with the model. A direct comparison of delay times between the simulation and the measurements could be used, but this would have imbedded in it the errors from fitting the first sampler's waveform, as well as errors from the PCE model itself. This can be overcome by removing the PCE model from the simulation entirely. Using measured data as the input waveform, the change in the pulse shape is simulated by using the microstrip model implemented in MIPCEM and letting the input propagate an appropriated distance. In this manner, neither the pulser PCE's nor the sampler PCE's response enters into the simulation. If the sampler's on the structure being measured are identical to each other, and the microstrip model is accurate, then the output of the simulation will conform to the measured waveform at the appropriate sampler. The agreement between the measured and simulated pulses thus corresponds to the

relative accuracy of the propagation velocity model for all of the frequencies present in the signal and not just the group velocity.

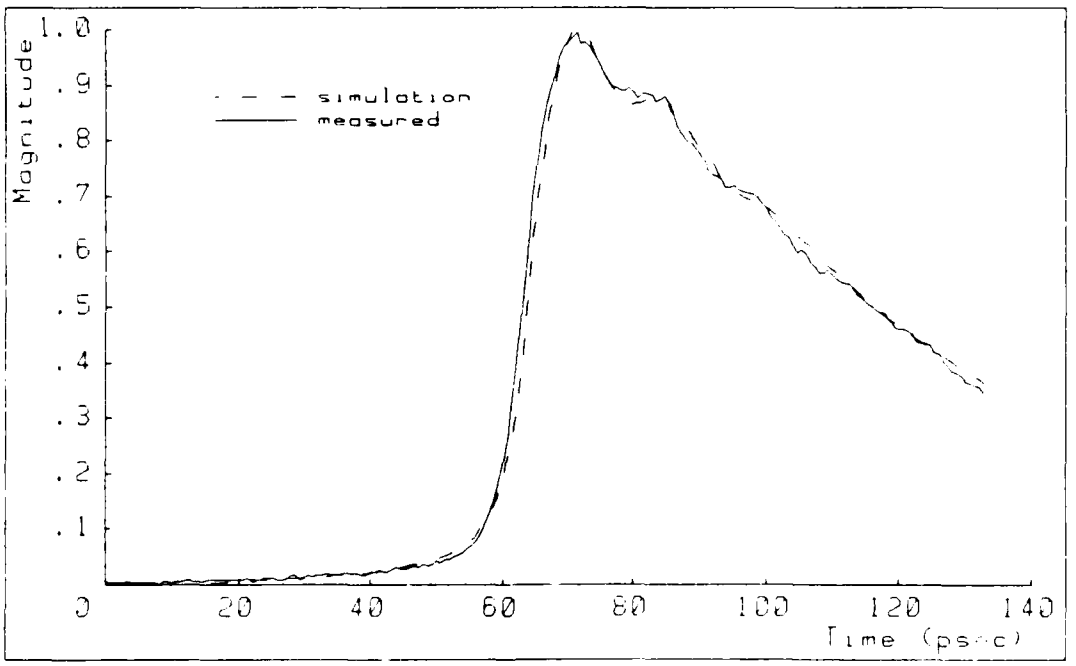
Figure 5.10 demonstrates this technique. In this figure, all pulses are normalized to their peak magnitude to remove any discrepancies caused by errors in the loss mechanisms. (Losses are addressed in Section 5.2.4 below.) Simulated pulses are shown by dash lines while the measurements are indicated with solid lines.

In Figure 5.10(a), the measurement from the 3.5 GHz pulse at the second sampler is simulated by using MIPCEM to propagate the first sampler's measurement an additional 400 μm. The general shape of the simulation is representative of the data, however, there are some significant discrepancies. Two possible causes are suggested from the measurement geometry. On the decaying transient the measurement contains a second peak caused by a reflected signal from the backplane of the substrate. This phenomena is not modeled in the simulation program because of its complex wave nature. Second, because the measurements are from a 100 μm wide line and the first sampler is the same distance from the pulser, the assumption of a propagating plane wave is not likely to be valid for the first part of the distance between the first and second samplers. By using the measured waveform from the second sampler instead of the first, this later problem should be removed. A side benefit of this is that the delays for the backplane reflection become similar and discrepancies from this source are also decreased. Figure 5.10(b) graphically demonstrates this effect. Here, the measured data at the third sampler is simulated by propagating the second sampler's data an additional 500 μm with MIPCEM. The agreement between the measurement and simulation is outstanding.

As the frequencies present in the pulse are increased, the discrepancies between the simulation and the measurement waveforms increase. Figure 5.11 shows the same type of measurements/simulation as that in Figure 5.10, but for the 18 GHz pulse. The curves in (a) are a comparison between the third sampler's data and a simulation done by propagating the first sampler's waveform 900 μm. Errors are obvious in both the rising and decaying transients, again indicating a possible problem with using the first sampler's data. Data from the second sampler is used as the basis for the simulation in (b) with a substantial improvement in accuracy.

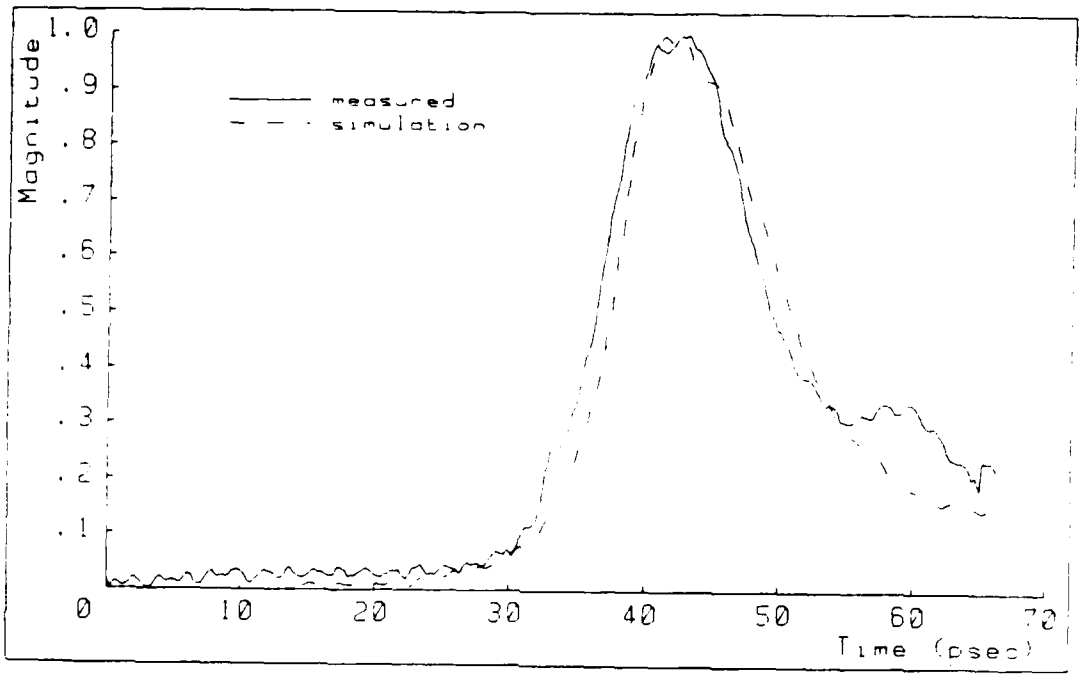


(a)

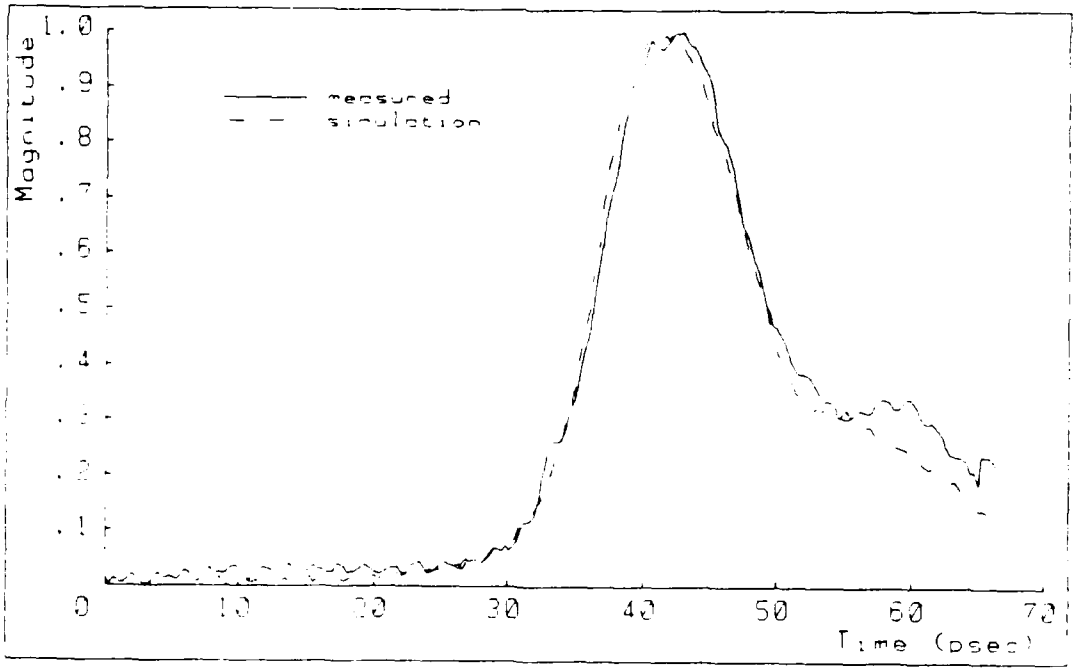


(b)

Figure 5.10: Waveform propagation comparisons for a 3.5 GHz pulse. (a) Measured waveform at the 2nd sampler compared with a simulation from the 1st sampler's data. (b) Measured waveform at the 3rd sampler compared with a simulation from the 2nd sampler's data.



(a)



(b)

Figure 5.11: Waveform propagation comparisons for a 18 GHz pulse. (a) Measured waveform at the 3rd sampler compared with a simulation from the 1st sampler's data. (b) The same measurement compared with a simulation from the 2nd sampler's data.

The most noticeable error is the slight shift in the timing of the simulated waveform. This is most likely caused by a slight difference in the delays associated with the actual sampler's which, although present in all the plots, is more noticeable on this expanded time scale.

Simulation comparisons of numerous waveform measurements on these structures (100 μm microstrip) show an overall outstanding agreement. The simulated delays are generally within 3% of the measured results but tended to under estimate the delay slightly. This is well within experimental error and the smaller delay tendency is easily explained by the sub-picosecond delay associated with the sampling action of the PCEs. Discrepancies in waveform shape tend to be in the fastest pulses and on the fast rising transients of the waveforms. Again, this is expected since the highest frequency components of all the pulses measured are in the range where the quasi-static TEM assumptions used in developing the microstrip propagation model are questionable. The fact that the simulations appear accurate at all at these frequencies is evidence that the upper bound on quasi TEM propagation is higher than currently believed.

5.2.4 Losses

The rapid decrease in the peak magnitude of the propagating waveform with distance seen in Figure 5.6(a) is indicative of the large losses present at picosecond speeds. It is also obvious from the simulation results shown in Figure 5.6(b), that the microstrip model does not accurately predict these losses. Figure 5.12 shows this more clearly. The peak magnitudes are plotted as a function of propagation distance, normalized to the first sampler's curve. The simulation results in a loss of 1.7 dB/mm while the measurements indicate over twice this (3.6 dB/mm) loss is actually occurring. A possible explanation for this would be a variation in the sensitivities of the sampling PCE's, however, this is discounted since such a change should be random over the waver or chip and not linear as observed.

A more likely explanation for the large discrepancy between the modeled loss and the measured loss is that the model incorrectly predicts the effects of one of the loss mechanisms present. From Figure 5.4 it is seen that the model predicts

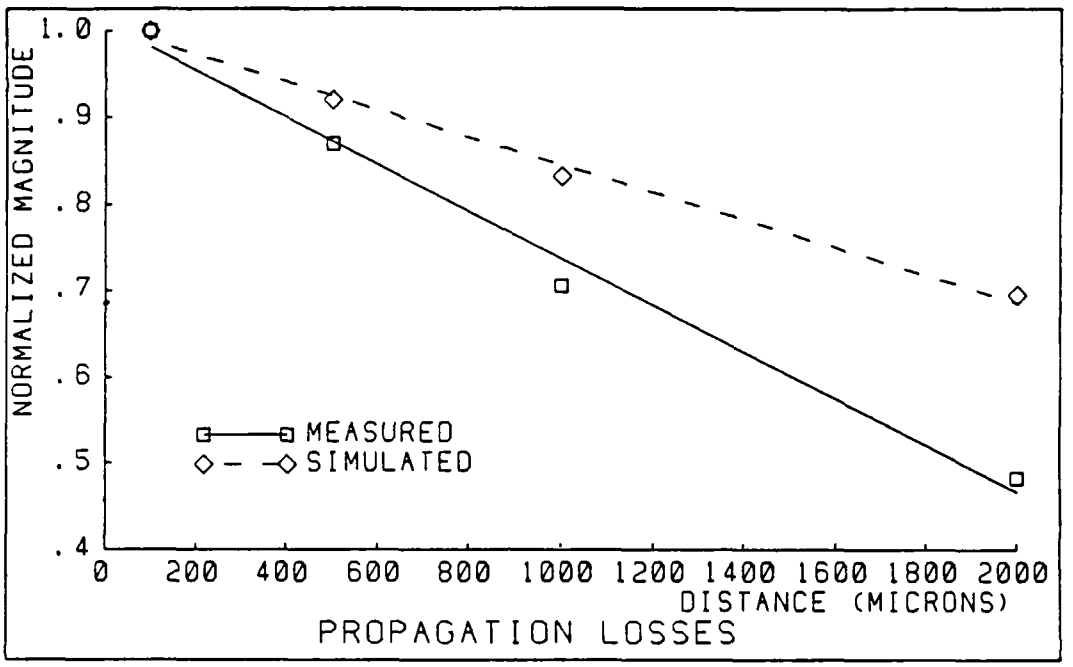


Figure 5.12: Comparisons of simulated and measured microstrip propagation losses for the silicon test structures.

virtually no conductor loss for this pulse (3.5 GHz), but that the dielectric loss should be above 2 dB/mm. While the dielectric loss is assumed to dominate in this region its contribution to the total loss is apparently not enough. This is caused by a combination of two factors — (1) the return path of the current passes through the semiconductor more than predicted and (2) the skin effect present at high frequencies is not modeled in the dielectric. Both of these factors would tend to increase the proportion of the dielectric loss which is actually accounted for in the model at any given frequency and, thus, tend to shift the total loss curve in Figure 5.4 upwards. The magnitude of the upward shift must be determined by a more rigorous analysis of the propagating fields than has been done. This is an area in which the microstrip models need significant improvement.

5.3 Summary

This chapter has demonstrated the use of polysilicon PCE's in an optoelectronic sampling system. Specifically, the generation and subsequent measurement of picosecond pulses on an integrated circuit microstrip transmission line has been demonstrated. Applicability of this type of measurement is shown by its use in the verification of a microstrip propagation model.

To verify the microstrip model, measurements were made of varying duration pulses and compared with theoretical predictions for the same conditions. Care was taken to insure that comparisons were made with simulations that did not contain PCE model assumptions or errors, but only the microstrip model implementation. In terms of dispersion and propagation velocity over the 10's of GHz range, the model proved to be very accurate. Only in the loss mechanisms did significant errors occur. In this respect the model seriously under estimates the loss which will be observed with propagation on a semiconductor substrate.

The PCE measurement technology demonstrates a significant advancement in the capability to make accurate, high resolution time domain measurements. Its high frequency performance shows potential for the measurement of integrated devices capable of operating near 100 GHz. Given good approximations, a detailed knowledge of the PCE performance is not needed to extract useful information from the measurements. It is in these applications that the PCE sampling system can provide immediate benefits.

Chapter 6

Summary and Conclusions

With the ever increasing speed of transistors being fabricated comes the problem of how to characterize these devices. The use of optoelectronic techniques lends itself to this problem by offering a high speed, low parasitic environment in which to perform measurements. This thesis has presented a device and technique to realize such an optoelectronic measurement system.

6.1 Summary of Results

The polysilicon photoconductive circuit element reported in this thesis marks a significant improvement in the performance of devices of this type. Several significant advances have been made in terms of fabrication compatibility and speed. Previous bulk silicon PCE's were limited in process compatibility by the very high energy implants needed to damage the substrate to avoid deep generated carriers which would slow down the device's response. The speed of these PCE's, however, still did not approach the circuit limited response predicted for the device geometry. By changing the photoconductor to a thin layer polycrystaline silicon structure, the need for a high energy implant is removed. An implant is used to tailor device response over an order of magnitude range, but it is a comparatively low energy process capable of being masked by standard IC photomasking techniques. This allows for PCE fabrication on the same substrate as other conventional devices without

radically modifying the process schedule. Working polysilicon PCE's and NMOS transistors were fabricated on the same integrated circuit as a demonstration of this compatibility.

The speed performance of the polysilicon PCE shows an order of magnitude improvement over earlier devices. Autocorrelations as fast as 3 psec FWHM have been measured, indicating bandwidths in excess of 100 GHz for devices used in an optoelectronic sampling system. The response is tailored via the implant by a choice of ions, energies and doses up to the point where the circuit limitations of the gap capacitance and characteristic impedance dominate. This circuit limitation can be optimized by considering the geometry of the structure and trading signal level for speed. Thus, the fundamental limitation on the PCE response is strongly linked to the specific geometry of the device.

Understanding the mechanisms contributing to the PCE response is necessary if the device is to have useful applications. A first order model of the PCE was developed using a combination of analytical expressions available in the literature and original analysis by the author. Simplifying assumptions as to the nature of the optical excitation, carrier behavior, and dominant circuit parameters were made to make the problem manageable. The model is implemented in a computer program, MIPCEM, so that detailed theoretical analysis can be performed. Comparisons of the predicted PCE response with optoelectronic correlation measurements indicates an outstanding agreement between the two. Errors which are present tend to be located in the regions of the waveform containing the highest frequency components, a region where the models obtained from the literature become questionable. Unfortunately, to this author's knowledge, more accurate expressions for these parameters are not available at these frequencies and the errors must be tolerated.

As a demonstration of the applicability of the PCE, an optoelectronic measurement system was constructed to measure the picosecond pulse response of silicon IC interconnections. This system uses a pulse and sample method to reconstruct the entire time domain response of a device under test. Measurement of GHz microstrip propagation were accomplished by using an unimplanted PCE for a pulser

and sampling at various distances with very fast PCE's ($\approx$ impulsive). The resultant data showed dispersive propagation on silicon for the first time. It also allowed tentative verification of a propagation model for high speed interconnects. Losses at these frequencies are substantial and this proved to be one area not adequately predicted by the models. All of the loss mechanisms are not apparently accounted for or not well understood.

6.2 Conclusions

The research conducted for this thesis has shown that it is possible to directly sample signals on semiconductor substrates without introducing significant parasitics. This allows for sampling bandwidths to exceed 100 GHz, a requirement to measure the next generation of transistor circuits. The measurements conducted and reported in this work allow it to be concluded that high speed optoelectronic devices are compatible with current IC fabrication technology. Furthermore, PCE's may be produced reliably and tailored to a multitude of specific applications in terms of signal level, speed, and geometry.

The verification of dispersive propagation on silicon microstrip structures is significant because it points to a limitation in IC speeds even when transistor switching speeds continue to improve. A different type of interconnection structure will have to be found if high speed signals are to be propagated any distance, particularly in a digital environment. As an example of the type of problem faced at even moderate speeds, Figure 6.1 shows the predicted pulse propagation for a 150 psec pulse across a silicon wafer. The simulation assumes an optimistic case where there are no discontinuities or loading present on the interconnect. With an input waveform shown on the left, the next three curves represent the pulse at distances of 1 mm, 5 mm, and 10 mm along a straight transmission line. Considering that the model used predicts only about half of the losses actually present, it may be concluded that the signal would be considerably less than actually shown. Compounding this would be reflections along the transmission line and losses at connected devices,

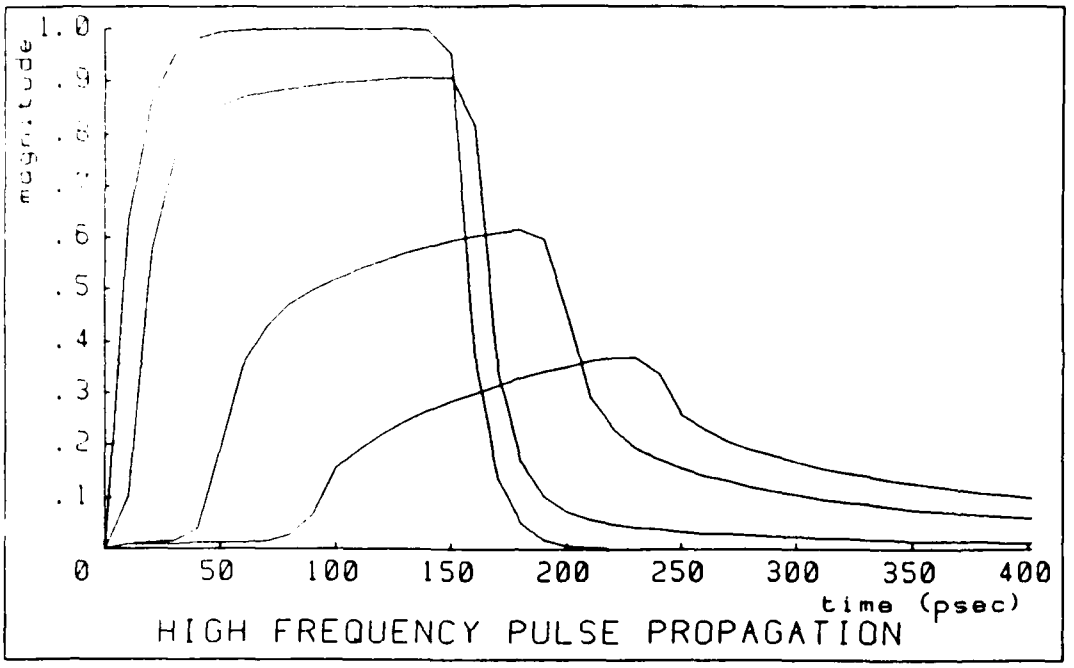


Figure 6.1: Propagation of a 150 psec exponential pulse down a straight microstrip line with no discontinuities or connections. Substrate and structure are typical of silicon IC's. Pulses represent the signal at (from left to right) the input, 1 mm, 5 mm, and 10 mm.

etc. The figure paints a gloomy picture for the use of large scale, very high speed circuits unless some alternative interconnection structure is found.

6.3 Future Directions

The possible uses of optoelectronic systems are just beginning to be explored. This includes the photoconductive circuit element. Future efforts envision the use of a variety of materials for the thin film photoconductive layer so that signal levels and speed may be further improved. The use of *GaAs* grown on silicon particularly, may provide the key to achieving 5 V pulses from PCE's for use in digital circuits. Also desirable is a high mobility film which would allow larger signal to noise ratios and open up the possibility of sampling even extremely small signals, such as those present due to coupling from adjacent lines.

The high frequency sampling capability demonstrated promises some applications in the microwave environment for PCE's. One such application which the author is beginning to research is the use of PCE time domain sampling measurements of high frequency transistors for S-parameter characterization. This involves accurately deconvolving transmission line responses from those of the transistor's and then converting the data to frequency domain S-parameters. The large bandwidth of the PCE's would allow a single set of time domain measurements to be used in generating S-parameters over two decades of frequency. Implicit in accomplishing this is further characterization and understanding of high frequency propagation on IC interconnect structures, microstrip as well as alternative structures. Many such high frequency characterization tasks are possible with PCE based optoelectronic sampling systems.

Appendix A

PCE Model Equations

This Appendix describes the remaining analytic equations used in the first order model for the polysilicon PCE developed in Chapter 4. The circuit components used in the model are approximations of parasitics and desired resistances based upon the specific geometry of the device (see Figure 4.2). Expressions for the characteristic impedance of the transmission lines, Z_0, are found in Chapter 5 while the time dependent gap resistance is derived in Chapter 4 with the model. Equations for the capacitances present and the derivation of the A_{eff} ratio are given below.

A.1 PCE Capacitances

The predominate capacitances present in the PCE structure arise from its form as a series gap in a microstrip transmission line. This is an important discontinuity in microstrip theory with many applications and has been rigorously analyzed.[A.1] Figure A.1 shows the general structure and its equivalent lumped capacitive circuit model. C_g denotes the significant capacitance which must be present across the gap for energy to be coupled across the open-circuit microstrip ends. The grounded capacitors, C_s, account for the fringing fields coupled directly to ground from each stub end.

Closed form analysis of the capacitances of Figure A.1 is a very difficult task which has not, to the author's knowledge, been accomplished. Analytic expressions

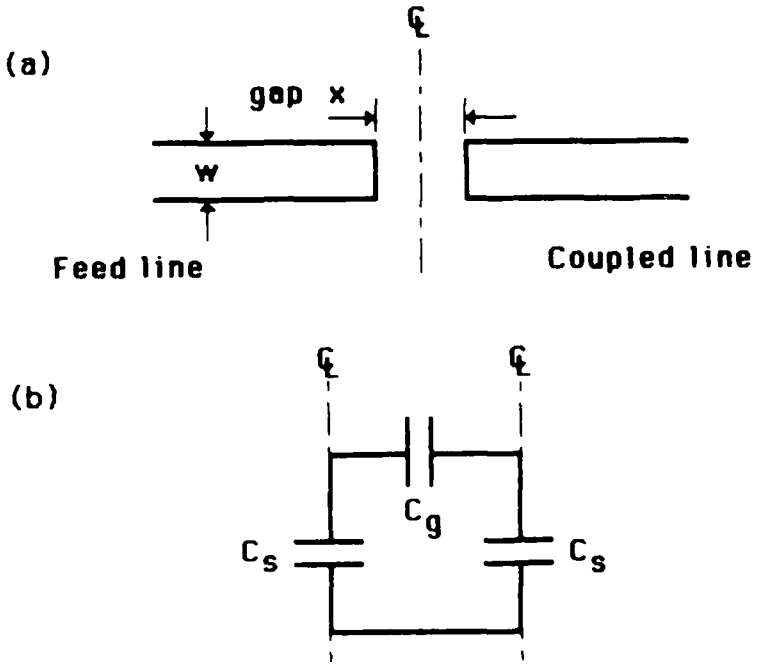


Figure A.1: A series gap in a microstrip. (a) Physical arrangement (b) Lumped capacitive equivalent circuit. [A.1]

have been developed, however, based upon curve fitting of data from end-coupled filters, coupling resonators and other circuits. Garg and Bahl [A.2] report curve fitted expressions based upon an odd and even mode coupling analysis. Equation A.1 relates the capacitances of Figure A.1 to the even mode capacitance, C_e, and the odd mode capacitance, C_o, which may be calculated from Equation A.2.

$$\begin{aligned} C_o &= 2C_g + C_s \\ C_e &= 2C_s \end{aligned} \tag{A.1}$$

$$\begin{aligned} \frac{C_o}{w} &= \left(\frac{x}{w}\right)^{m_o} e^{k_o} \quad pF/m \\ \frac{C_e}{w} &= \left(\frac{x}{w}\right)^{m_e} e^{k_e} \quad pF/m \end{aligned} \tag{A.2}$$

The indices and arguments are defined by the following set of equations:

$$\left.\begin{aligned} m_o &= \tfrac{w}{h}\left(0.619\log\left(\tfrac{w}{h}\right) - 0.3853\right) \\ k_o &= 4.26 - 1.453\log\left(\tfrac{w}{h}\right) \end{aligned}\right\} 0.1 \leq \frac{x}{w} \leq 1.0 \tag{A.3}$$

$$\left.\begin{aligned} m_e &= 0.8675 \\ k_e &= 2.043\left(\frac{w}{h}\right)^{0.12} \end{aligned}\right\} 0.1 \leq \frac{x}{w} \leq 0.3 \tag{A.4}$$

$$\left.\begin{aligned} m_e &= \frac{1.565}{(w/h)^{0.16}} - 1 \\ k_e &= 1.97 - \frac{0.03}{w/h} \end{aligned}\right\} 0.3 \leq \frac{x}{w} \leq 1.0 \tag{A.5}$$

In these expressions, h is the substrate height, w the width of the microstrip transmission line, and x the width of the gap in that line.

The curve fitting done by Garg and Bahl to derive Equations A.1 through A.5 was done on data from an experiment where $\epsilon_r = 9.6$ and is thus not directly applicable to materials of different dielectric constants. The appropriate values for C_o and C_e can be found for different materials by modifying the basic result to account for the different dielectric constant.

$$\begin{aligned} C_o(\epsilon_r) &= C_o(9.6)\left(\frac{\epsilon_r}{9.6}\right)^{0.8} \\ C_e(\epsilon_r) &= C_e(9.6)\left(\frac{\epsilon_r}{9.6}\right)^{0.9} \end{aligned} \tag{A.6}$$

This modification to the basic equations is valid over a range of ϵ_r from 2.5 to 15 with a reported accuracy of better than 7 percent. [A.1]

A.2 Effective Illuminated Area

Calculation of the time dependent gap resistance (Equation 4.12) requires the use of an effective illuminated area, A_{eff}. This is the area of the laser spot which is incident upon photoconductive material. For a typical circular laser spot, as shown in Figure A.2, three regions of illumination can be described for the gap (excluding the metal overlap). Region 1 is the center of the spot where full illumination occurs over the entire gap width. This area may be calculated if the gap width, x, is known assuming a laser focussing parameter, $\frac{x}{d}$, which is the ratio of the gap width and laser spot diameter. Geometrically, the length of the region is then:

$$l_1 = 2x\frac{1}{x/d}\sin\frac{\alpha}{2} \tag{A.7}$$

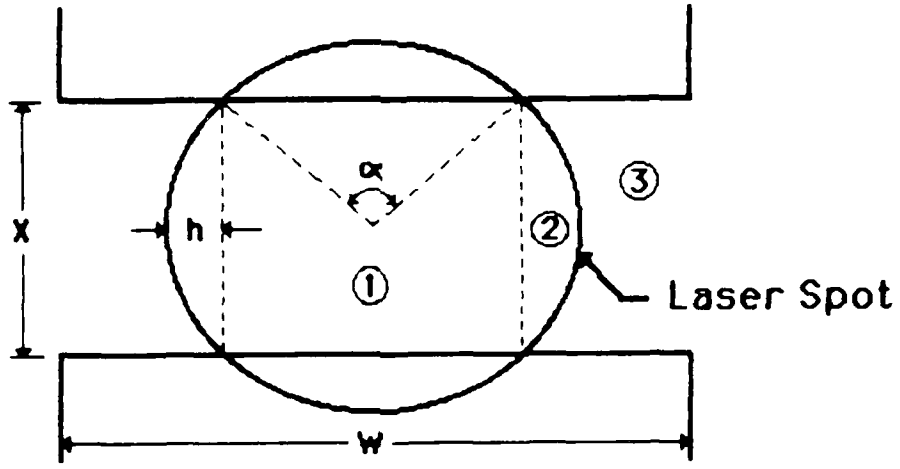


Figure A.2: Focused laser spot for effective illuminated area calculation.

where $\alpha = \pi - 2\sin^{-1}\frac{x}{d}$. The area within the region is simply the length multiplied by the gap width.

$$A_1 = 2x^2 \frac{1}{x/d} \sin\frac{\alpha}{2} \tag{A.8}$$

The remainder of the laser spot incident on the gap is located in Region 2 (on both sides of the spot) where there is no overlap with the metal transmission line. This causes the photogenerated carriers to be less efficient in moving charge across the gap. Approximating the area as a smaller right triangle instead of an arc accounts for this loss of conductivity. Using trigonometry it can be shown that the height of the enclosed right triangle, h, is:

$$h = 0.5\left(d - \left(\frac{x}{x/d}\right)\sin\frac{\alpha}{2}\right) \tag{A.9}$$

The area of each triangular region is $\frac{1}{2}hx$ yielding a total area for Region 2 as:

$$A_2 = \frac{xd}{2}\left(1 - \sin\frac{\alpha}{2}\right) \tag{A.10}$$

The effective illuminated area, A_{eff}, can now be calculated by summing the illuminated region areas shown in Equations A.8 and A.10.

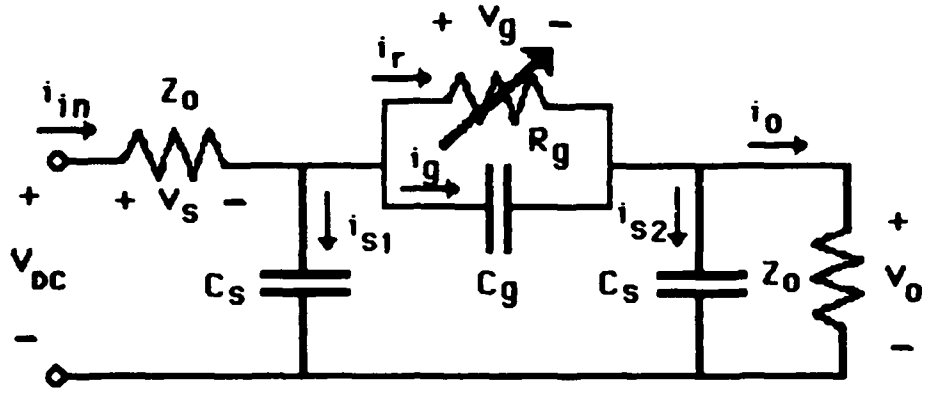


Figure A.3: PCE model for circuit analysis

Region 3 is the remainder of the gap which is unilluminated. It does not contribute to the effective illuminated area, but may be important when considering the total gap resistance, depending upon the specific geometry. This region represents a high resistance in parallel with the illuminated regions and can influence the gap resistance for wide transmission lines and narrow gaps. The area present in this region is merely the difference between the total gap area, $x \times w$, and the effective illuminated area, A_{eff}.

A.3 PCE Model Circuit Analysis

To describe the time domain response of the polysilicon photoconductor a circuit analysis of the model is performed. Establishing voltage and current polarities as shown in Figure A.3 the analysis is done,starting from basic I-V relationships and nodal equations.

$$\begin{aligned} v_o &= i_o Z_0 & i_g &= C_g \frac{dv_g}{dt} \\ v_s &= i_{in} Z_0 & i_{s1} &= C_s \frac{d(v_g + v_o)}{dt} \\ v_g &= i_r R_g & i_{s2} &= C_s \frac{dv_o}{dt} \end{aligned} \tag{A.11}$$

At the output node:

$$i_o = i_r + i_g - i_{s2} \tag{A.12}$$

while at the input node:

$$i_{in} = i_{s1} + i_r + i_g \tag{A.13}$$

From the I-V relationships and Equations A.11 and A.12 two simultaneous equations may be written.

$$\frac{v_o}{Z_0} = \left[\frac{v_g}{Z_0} + C_g\frac{dv_g}{dt} - C_s\frac{dv_o}{dt}\right] \tag{A.14}$$

$$\frac{v_o}{Z_0} = \left[\frac{V_{DC} - v_g - v_o}{Z_0} - C_s\frac{d(v_g + v_o)}{dt} - C_s\frac{dv_o}{dt}\right] \tag{A.15}$$

Subtracting Equation A.14 from Equation A.15 and multiplying by Z_0 yields:

$$0 = V_{DC} - v_g - v_o - \frac{Z_0 v_g}{R_g} - \left[(C_s + C_g)\frac{dv_g}{dt} - c_s\frac{dv_o}{dt}\right] Z_0 \tag{A.16}$$

To use this equation it is desirable to solve for v_g and $\frac{dv_g}{dt}$ in terms of known quantities. This can most easily be accomplished by assuming that C_s is very small relative to the other capacitances in the PCE structure. The current through the input shunt capacitance is then approximately zero.

$$i_{s1} = C_s\left(\frac{dv_o}{dt} + \frac{dv_g}{dt}\right) \approx 0 \tag{A.17}$$

Rewriting the nodal equations and solving for v_g yields:

$$v_g = V_{DC} - 2v_o - Z_0 C_s\frac{dv_o}{dt} \tag{A.18}$$

which in turn may be used to find an expression for the time derivative of the gap voltage.

$$\frac{dv_g}{dt} = \frac{v_o}{C_s}\left[\frac{1}{Z_0} + \frac{2}{R_g}\right] + \frac{dv_o}{dt}\left[1 + \frac{Z_0}{R_g}\right] - \frac{V_{DC}}{C_s R_g} \tag{A.19}$$

Substituting Equations A.18 and A.19 into Equation A.16, expanding and solving results in the desired first order differential equation.

$$\frac{dv_o}{dt} = \frac{\frac{C_g Z_0 V_{DC}}{C_s R_g} - \left(\frac{2C_g Z_0}{C_s R_g} + \frac{C_g}{C_s}\right) v_o}{Z_0 C_s + Z_0 C_g + \frac{Z_0^2 C_g}{R_g}} \tag{A.20}$$

This expression describes the output response of the PCE when the time varying gap resistance is used for R_g. Because of its complexity, numerical techniques are used to solve for $v_o(t)$ when necessary. This model is implemented in the MIPCEM program described in Appendix D.

Appendix B

PCE Bandwidth Derivation

This appendix derives the frequency bandwidth of the Photoconductive Circuit Elements (PCEs) from a Full Width at Half Maximum (FWHM) duration. The FWHM time is the interval during which a pulse rises from half its peak magnitude, through the peak and down to the half magnitude value again. It is easily extracted from PCE measurements and provides an indication of the speed of the photoconductor response. To simplify the bandwidth derivation, a simpler model of the PCE response is assumed than that derived in Appendix A and discussed in Chapter 4. The spectrum derivation of Eisenstadt[B.1] is then applicable.

The PCE frequency spectrum has its maximum value at DC and decreases monotonically as the frequency goes to infinity. The Fourier transforms shown in Equations B.1 and B.2 are used to relate the frequency and time responses of the

$$f(t) = \int_{-\infty}^{\infty} F(s) e^{j2\pi ts} ds \qquad (B.1)$$

$$F(s) = \int_{-\infty}^{\infty} f(t) e^{-j2\pi st} dt \qquad (B.2)$$

photoconductor and comprise the basis for this derivation.[B.2] The function $f(t)$ is an arbitrary time domain function with a frequency domain representation of $F(s)$. Equation B.1 is the Fourier transform and Equation B.2 the inverse Fourier transform.

Assuming the decaying exponential of the photoconductor response is sufficiently greater than the rise time, the PCE pulse waveform can be approximated as a step rise and exponential decay as represented by Equation B.3. Here τ is the characteristic decay time, P_0 the response at time zero, and $u(t)$ the unit step function.

$$p(t) = P_0 u(t) e^{-(t/\tau)} \tag{B.3}$$

Since this is an asymmetric pulse with zero risetime, the FWHM time can easily be derived from the characteristic decay time:

$$\begin{aligned} p(t_{FWHM}) &= 0.5 P_0 \\ 0.5 &= e^{-\left(\frac{t_{FWHM}}{\tau}\right)} \\ \tau &= \frac{t_{FWHM}}{-\ln(0.5)} = 1.44 t_{FWHM} \end{aligned} \tag{B.4}$$

The waveform approximation is now rewritten as:

$$p(t) = P_0 u(t) e^{-\left(\frac{t}{1.44 t_{FWHM}}\right)} \tag{B.5}$$

If c is an arbitrary constant, then the similarity theorem[B.2] allows the Fourier transform of $f(ct)$ to be calculated by:

$$\int_{-\infty}^{\infty} f(ct) e^{-j2\pi ts} dt = \frac{1}{|c|} F\left(\frac{s}{c}\right) \tag{B.6}$$

Defining a constant such that $c = \frac{1}{1.44 t_{FWHM}}$, Equation B.5 becomes:

$$p(t) = P_0 u(t) e^{-ct} \tag{B.7}$$

The Fourier transform for the pulse $f(t) = u(t)e^{-t}$ is[B.3]:

$$F(s) = \int_{-\infty}^{\infty} u(t) e^{-t} e^{-j2\pi st} dt = \frac{1}{1 + j2\pi s} \tag{B.8}$$

The similarity theorem shown in Equation B.6 is now applied to Equations B.7 and B.8 to solve for the Fourier transform of $p(t)$. The result is the frequency domain representation of the PCE pulse.

$$P(s) = 1.44 t_{FWHM} \frac{1}{1 + j2.88\pi s t_{FWHM}} \qquad (B.9)$$

The bandwidth of the PCE is defined as the frequency at which the signal power has dropped 3dB, or to half its peak magnitude. Using Equation B.9, the magnitude of the frequency response is:

$$|P(s)| = 1.44 t_{FWHM} \frac{1}{\sqrt{1 + (2.88\pi t_{FWHM} s)^2}} \qquad (B.10)$$

At DC ($f = 0$) this response is at a peak of $1.44 t_{FWHM}$. Setting the magnitude to half this level and solving for $s = f_{-3dB}$ results in the photoconductor bandwidth.

$$\begin{aligned} |P(f_{-3dB})| &= \tfrac{1.44 t_{FWHM}}{2} \\ &= 1.44 t_{FWHM} \tfrac{1}{\sqrt{1+(2.88\pi t_{FWHM} f_{-3dB})^2}} \qquad (B.11) \\ f_{-3dB} &= \tfrac{\sqrt{3}}{2.88\pi t_{FWHM}} \approx \tfrac{1}{5.22 t_{FWHM}} \end{aligned}$$

The cross-correlation measurement results from the experiments conducted give t_{FWHM} directly if the sampler is impulsive, otherwise an approximation of this time can be made as the period from the peak to the half magnitude point on the decaying transient. Autocorrelation FWHM times are approximately double the

Bandwidth Conversion Table*

$t_{FWHM} \Rightarrow f_{-3dB}$		$f_{-3dB} \Rightarrow t_{FWHM}$	
1	192	200	0.96
5	38.3	100	1.9
10	19.2	50	3.8
25	7.7	10	19.2
50	3.8	1	192

*(time in psec, freq in GHz)

Table B.1: Photoconductor Bandwidth Estimates

individual pulse t_{FWHM} and should be modified accordingly prior to calculating the bandwidth based upon the above derivation. Table B.1 provides some quick conversion estimates for reference.

Appendix C

PCE Fabrication Schedules

Two different processing schedules were successfully used to produce the high speed polycrystaline silicon PCEs fabricated during this research. This appendix provides a list of those processing steps used in each schedule. Section C.1 details the generic processing schedule used to fabricate PCEs and aluminum transmission lines. An NMOS compatible process was developed by modifying a simple process schedule used to teach fabrication at Stanford University and is shown in Section C.2.

C.1 Poly PCE Fabrication Schedule

1. Select starting wafers and scribe wafer's backsides (near the flat) with reference numbers.
2. Characterize wafers: measure resistivity in a five point pattern across the wafer with the four point probe. Also record wafer thickness.
3. Wafer degrease and clean:
   (a) 10 min in 4:1 $H_2SO_4 : H_2O_2$
   (b) 4 min DI rinse in dumper
   (c) standard RCA clean (do this just before next step)

4. Thermal SiO_2 insulator growth (1.5 μm): 10-230-10 cycle

T1 setting _____= 800 C Actual temp _____
T2 setting _____=1150 C Actual temp _____

Step	Time	N2	H2	LgO2	SmO2	Ar	T1	T2	Stop	Condition
0	0	X					X			Slow Push
1	45					X		X		Ramp Up
2	10			X				X		Dry O2 Oxidize
3	10s	X		X				X		Torch-prepurge
4	230		X	X				X		Steam Oxidize
5	10s	X		X				X		Torch-postpurge
6	10			X				X		Dry O2 Oxidize
7	45					X	X			Ramp Down
8	1					X			X	Stop/Alarm

5. Oxide thickness test: Measure and record oxide thickness in a five point pattern across wafers. Use the Nanospec thick oxide program.

6. Standard RCA clean. Use predeposition procedure with 50:1 HF dip last. This step must be done shortly before the LPCVD poly deposition. See the Lab technician about including a poly test wafer in the cleaning process.

7. Poly deposition (5000 Å): LPCVD deposition at 620°C for 70 minutes. This must be done by a technician and scheduled in advance.

8. Measure poly thickness on the Nanospec in a five point pattern across the test wafers. This must be done on one of the poly test wafers with only 1000 Å of oxide under the poly.

9. Poly Photolithography: Singe wafers in oven at 125°C for 20 minutes unless they were just removed from the furnace. Spin on resist at 5000 rpm for 30 seconds and then prebake for 10 minutes at 90°C. Expose using mask #1 (no alignment necessary). Develop using standard resist develop cycle and inspect wafers for good resolution. Postbake for 20 minutes at 120°C to harden resist.

10. Poly etch: Use a descum and poly etch process on the Drytek to remove the poly in all exposed areas. Insure that the laser in on and that a 10% over-etch is set. Since this is undoped poly the total time to etch should be about 2:45 minutes. Inspect the wafers under a microscope to insure the etch is complete.

11. Remove photoresist: Follow standard resist removal procedure.

    (a) 20 min in H_2SO_4 followed by a 4 min DI rinse

    (b) 10 min in H_2SO_4/H_2O_2 followed by a 4 min DI rinse

    (c) Dry and inspect for resist residue. Repeat step 11b if necessary.

12. Poly anneal: Increase poly grain size by an hour anneal at 1150°C. This will improve PCE performance if the step is compatible with other devices on wafer.

T1 setting ________= 800 C Actual temp _______
T2 setting ________=1150 C Actual temp _______

Step	Time	N2	H2	Lg02	Sm02	Ar	T1	T2	Stop	Condition
0	0	X					X			Slow Push
1	45					X		X		Ramp Up
2	50					X		X		Anneal
3	60					X	X			Ramp Down
4	1	X					X		X	Stop/Alarm

13. Premetal clean: 10 min in H_2SO_4/H_2O_2 followed by a standard RCA clean just prior to metal deposition.

14. Aluminum deposition: Have 1.0μm to 1.5μm of either Al, Al:Cu, or Al:Cu:Si put on the wafers. This must be done by a technician and scheduled in advance.

15. Metal Photolithography: Singe wafers at 175°C for 25 min. Spin resist on at 5000 RPM for 30 seconds and then prebake at 90°C for 10 minutes. Define

metal pattern using mask #3 which must be aligned to the previous mask. Expose and develop using a standard resist development cycle. Postbake at 120°C for 20 minutes.

16. Metal etch: Etch Aluminum in metal etch at 40°C for $\approx$ 10 minutes. Time for the etch will be dependent upon the thickness of the Al. Etch until the metal clears visually across the wafer except under the patterned features then slightly overetch for another 15 to 30 seconds. Follow with two DI rinses for 4 minutes. Inspect wafers under a microscope to insure that no metal bridges exist, especially near the smallest metal features.

17. Resist strip/clean: Strip resist in resist stripper as required followed by two 4 minute DI rinse cycles. This step acts as a solvent clean for the wafers and should be done within one hour of the next step.

18. Anneal/Alloy: Alloy wafers at 450°C in the Forming Gas Anneal Furnace for approximately one hour. Insure that the forming gas is turned on.

This completes the processing of the wafers. They may be tested for continuity, photosensitivity, and processing parameters prior to PCE damage and laser testing.

C.2 NMOS-Poly PCE Fabrication Schedule

1. Select starting wafers and scribe wafer's backsides (near the flat) with reference numbers. Wafers should be $< 100 >$ p-type 10-20 $\Omega - cm$. Include four test wafers labeled T-1 through T-4.

2. Characterize wafers: Measure resistivity in a five point pattern across the wafer with the four point probe. Also record wafer thickness.

3. Wafer degrease and clean:

   (a) 10 min in 4:1 $H_2SO_4 : H_2O_2$

   (b) 4 min DI rinse in dumper

   (c) standard RCA clean (do this just before next step)

4. Thermal SiO_2 insulator growth (7500 Å): 5-60-5 cycle Include all four test wafers.

T1 setting _____= 800 C Actual temp _____
T2 setting _____=1150 C Actual temp _____

Step	Time	N2	H2	LgO2	SmO2	Ar	T1	T2	Stop	Condition
0	0	X					X			Slow Push
1	50					X		X		Ramp Up
2	5			X				X		Dry O2 Oxidize
3	10s	X		X				X		Torch-prepurge
4	60		X	X				X		Steam Oxidize
5	10s	X		X				X		Torch-postpurge
6	5			X				X		Dry O2 Oxidize
7	60					X	X			Ramp Down
8	1					X			X	Stop/Alarm

5. Oxide thickness test: Measure and record oxide thickness in a five point pattern across wafers. Use the Nanospec thick oxide program.

6. Standard RCA clean. Use predeposition procedure with 50:1 HF dip last. This step must be done shortly before the LPCVD poly deposition. See the Lab technician about including a poly test wafer in the cleaning process. Include two test wafers from the poly test wafer box (1000Å oxide) as well as T-1 through T-4.

7. Poly deposition (5000Å): LPCVD deposition at 620°C for 70 minutes. This must be done by a technician and scheduled in advance.

8. Measure poly thickness on the Nanospec in a five point pattern across the test wafers. This must be done on one of the poly test wafers with only 1000Å of oxide under the poly.

9. Poly Photolithography: Singe wafers in oven at 125°C for 20 minutes unless they just were removed from the furnace. Spin on resist at 5000 rpm for 30 seconds and then prebake for 10 minutes at 90°C. Expose using mask #1 (no alignment necessary). Develop using standard resist develop cycle and inspect wafers for good resolution. Postbake for 20 minutes at 120°C to harden resist.

10. Poly etch: Use a descum and poly etch process on the Drytek to remove the poly in all exposed areas. Insure that the laser is on and that a 10% over-etch is set. Since this is undoped poly the total time to etch should be about 2:45 minutes. Inspect the wafers under a microscope to insure the etch is complete. Include all test wafers which may be used to determine the correct etch time.

11. Remove photoresist: Follow standard resist removal procedure.

    (a) 20 min in H_2SO_4 followed by a 4 min DI rinse

    (b) 10 min in H_2SO_4/H_2O_2 followed by a 4 min DI rinse

    (c) Dry and inspect for resist residue. Repeat step 11b if necessary.

12. Poly PCE anneal: Increase poly grain size by an hour anneal at 1150°C. Include all four test wafers.

T1 setting _____= 800 C Actual temp _____
T2 setting _____=1150 C Actual temp _____

Step	Time	N2	H2	LgO2	SmO2	Ar	T1	T2	Stop	Condition
0	0	X					X			Slow Push
1	50					X		X		Ramp Up
2	50					X		X		Anneal
3	60					X	X			Ramp Down
4	1	X					X		X	Stop/Alarm

13. SiO_2 Deposition: Use the SILOX to deposit 4000Å of oxide on the wafers. Deposition time is 6:30 at 450°C ($\approx$ 600Å/min). Allow wafers to heat up to 450°C for 10 minutes prior to the deposition. Follow the SILOX procedures for flow settings and do a test run prior to doing device wafers to coat the boat and reactor. If this step is not done immediately after the poly PCE anneal then the wafers must go through a standard clean prior to the deposition.

14. Oxide Densification: This step must immediately follow the oxide deposition. Note that there is no ramp up or down associated with this step.

T1 setting _____ = 800 C Actual temp _____
T2 setting _____ = 900 C Actual temp _____

Step	Time	N2	H2	LgO2	SmO2	Ar	T1	T2	Stop	Condition
0	0	X						X		Slow Push
1	30			X				X		Dry O2 Oxidation
2	1	X						X	X	Stop/Alarm

15. Transistor Well Photolithography: Singe wafers in oven at 125°C for 20 minutes unless they were just removed from the furnace. Spin on resist at 5000 rpm for 30 seconds and then prebake for 10 minutes at 90°C. Expose using mask #2 (after alignment). Use wafers T-2 and T-3 to adjust the exposure times. Develop using standard resist develop cycle and inspect wafers for good resolution. Postbake for 20 minutes at 120°C to harden resist. Do NOT include wafer T-1 in this step.

16. Oxide Etch: Etch in 6:1 buffered HF for approximately 14 minutes. Use wafer T-1 to determine appropriate etch time for the device wafers. Inspect under a microscope to insure that all of the oxide is removed from the transistor well areas.

17. Remove photoresist: Follow standard resist removal procedure.

    (a) 20 min in H_2SO_4 followed by a 4 min DI rinse

    (b) 10 min in H_2SO_4/H_2O_2 followed by a 4 min DI rinse

    (c) Dry and inspect for resist residue. Repeat step 17b if necessary.

18. Pre-oxidation clean: 10 min in H_2SO_4/H_2O_2 followed by a standard RCA clean just prior to the oxidation. If this step is done immediately after the resist strip then the H_2SO_4/H_2O_2 step may be deleted.

19. Gate Oxidation (700Å):

T1 setting _____ = 800 C Actual temp _____
T2 setting _____ =1000 C Actual temp _____

Step	Time	N2	H2	LgO2	SmO2	Ar	T1	T2	Stop	Condition
0	0	X					X			Slow Push
1	30					X		X		Ramp Up
2	120			X				X		Dry O2 Oxidize
3	45					X	X			Ramp Down
4	1					X	X		X	Stop/Alarm

20. Oxide Thickness Testing: Use the Nanospec thin oxide program to measure the gate oxide thickness on T-1 and the thick oxide program to measure the field oxide thickness on T-2. Measure in a five-point pattern across each wafer.

21. Enhancement Implant: Implant Boron as indicated below. This is done through the gate oxide. Include T-2, T-3 and T-4. This step must be done by a technician and scheduled in advance.

Species: B^+

Dose: $2.5 \times 10^{11}/cm^2$

Energy: $35KeV$

Orientation: 7 deg

22. Pre-deposition clean: 10 min in H_2SO_4/H_2O_2 followed by a standard RCA clean prior to deposition (50:1 HF dip last). Include two test wafers from the Poly LPCVD box (1000Å oxide). Put wafer T-1 aside for later measurement of the final gate oxide thickness.

23. Poly Deposition (5000Å): LPCVD deposition at 620°C for 70 minutes. This must be done by a technician and scheduled in advance.

24. Poly Thickness Testing: Measure the poly thickness on the Nanospec in a five point pattern across the poly test wafers. Insure that this measurement is done on one of the wafers with only 1000Å oxide under the poly.

25. Poly doping: Dope the poly interconnects and gates in the $POCl_3$ Furnace. Include wafers T-2 through T-4. If this step is not done immediately after the polysilicon deposition then the wafers must be given a standard cleaning procedure.

    The tube and boat should be pre-doped by running the following program just prior to loading the wafers. Note that the doping does not use a ramp up/down, so the manual temperature set point switch should be set to T2 to set the temperature at 950°C and keep the furnace from trying to ramp down between the dummy and real runs.

T2 setting _____ = 950 C Actual temp _____

Step	Time	N2	O2	HCl	POCl	Ar	T1	T2	Stop	Condition
0	0	X	X					X		Slow Push
1	5	X	X					X		N2 + O2
2	25	X	X		X			X		POCl Source
3	5	X	X					X		Post N2 + O2
4	1	X						X	X	Alarm/Step/Run
5	10	X						X		Slow Pull
6	1	X						X	X	Alarm/Reset

The wafers should be loaded so that all of the polished surfaces are facing another wafer and so there are two empty spaces between each pair of wafers.

Dummy wafers may have to be added to acheive this configuration, but this insures that all wafers will be equally doped.

26. Polysilicon de-glaze: Include wafers T-2 through T-4. If this step is not done immediately after the polysilicon doping, the wafers must be given a standard cleaning procedure.

    (a) DI soak - overflow rinse - 15 sec

    (b) 50:1 $H_2O : HF$ dip - 30 sec

    (c) Overflow rinse - 4 min followed by spin dry.

27. Polysilicon testing: Measure the poly resistivity using the four point probe on wafers T-2 and T-3. Measure in a five point pattern across both wafers.

28. Poly Photolithography: Include wafers T-3 and T-4. Singe wafers at 125°C for 20 minutes. Spin on resist at 5000 rpm for 30 seconds and then prebake at 90°C for 10 minutes. Expose using mask #4 (after alignment). Use wafers T-3 and T-4 to adjust the exposure times. Develop using standard resist develop cycle and inspect wafers for good resolution. Postbake for 20 minutes at 120°C to harden the resist.

29. Poly Etch: Use the standard Drytek poly descum and etch program. Include wafers T-3 and T-4. Insure that the laser is on and that a 10% over-etch is set. Since this is doped poly the etch rate will be somewhat higher than for the undoped poly. Inspect the wafers under a microscope to insure the etch is complete and the poly lines are well defined.

30. Remove Photoresist: Follow standard resist removal procedure. This resist is extremely difficult to remove. Include wafers T-3 and T-4.

    (a) 20 min (or more as required) in H_2SO_4 followed by a 4 min DI rinse.

    (b) 10 min in H_2SO_4/H_2O_2 followed by a 4 min DI rinse.

    (c) Dry and inspect for resist residue. Repeat step 30b if necessary.

31. Source-Drain Implant: Include wafers T-3 and T-4. Implant Arsenic as indicated below. This must be done by a technician and scheduled in advance.

Species: As
Dose: $6 \times 10^{15}/cm^2$
Energy: $100KeV$
Orientation: 7 deg

32. Pre-Drive-in Clean: 10 min in H_2SO_4 followed by a standard RCA clean just prior to the drive-in/anneal.

33. Source-Drain Drive-in/Anneal: Include wafers T-3 and T-4.

T1 setting _____ = 800 C Actual temp _____
T2 setting _____ =1000 C Actual temp _____

Step	Time	N2	H2	LgO2	SmO2	Ar	T1	T2	Stop	Condition
0	0	X					X			Slow Push
1	5					X	X			Pre-Heat
2	30					X		X		Ramp-up and Anneal
3	30			X				X		Dry O2 oxidation
4	30					X		X		Drive-in
5	30					X	X			Ramp-down
6	1					X	X		X	Alarm/Step/Run
7	10					X	X			Slow Pull
8	1	X					X		X	Alarm/Reset

34. Oxide Testing: Use the Nanospec thin oxide program to measure the source/drain oxide on wafers T-3 and T-4. These are patterned wafers so appropriate points must be found for the measurement. Measure the gate oxide thickness on wafer T-1. Measure a five point pattern across all wafers.

35. SiO_2 Deposition (5000Å): Use the SILOX to deposit 5000Å of oxide on the wafers. Include wafers T-2 through T-4. If this step is not done immediately after the source/drain drive-in then the wafers must go through a standard

clean prior to deposition. Allow the wafers to heat up to 450°C for 10 minutes and then deposit for 8 minutes.

36. SiO_2 Densification: This step must be done immediately following the oxide deposition. Note that there is no ramp up or down associated with this step.

T1 setting _____ = 800 C Actual temp _____
T2 setting _____ = 900 C Actual temp _____

Step	Time	N2	H2	LgO2	SmO2	Ar	T1	T2	Stop	Condition
0	0	X						X		Slow Push
1	30			X				X		Dry O2 Oxidation
2	1	X						X	X	Stop/Alarm

37. Contact Photolithography: Singe wafers in oven at 125°C for 20 minutes unless they were just removed from the furnace. Include wafer T-4. Spin on resist at 5000 rpm for 30 seconds and then prebake for 10 minutes at 90°C. Expose using mask #5 (after alignment). Use wafer T-4 to adjust the exposure time. Develop using standard resist develop cycle and inspect wafers for good resolution. Postbake for 20 minutes at 120°C to harden the resist.

38. Oxide Testing: Use the Nanospec thick oxide program to measure the field oxide on wafer T-2 and the source-drain oxide on wafer T-3. The measurement on wafer T-3 will give an indication of the required etch time in the next step. Measure in a five point pattern across all wafers.

39. Contact Etch: Etch wafers in 6:1 H_2O : HF for approximately 5 minutes. (Time may need adjusting depending upon actual thickness measured in step 38 .) Use wafers T-3 and T-4 to determine the correct etch time.

40. Remove Photoresist: Follow standard resist removal procedure.

    (a) 20 min in H_2SO_4 followed by a 4 min DI rinse.

(b) 10 min in H_2SO_4/H_2O_2 followed by a 4 min DI rinse.

(c) Dry and inspect for resist residue. Repeat step 40b if necessary.

41. Premetal clean: 10 min in H_2SO_4/H_2O_2 followed by a standard RCA clean just prior to metal deposition. If this step is done immediately after the resist removal then the H_2SO_4/H_2O_2 step may be deleted.

42. Aluminum deposition: Have $1.0\mu m$ to $1.5\mu m$ of either Al, Al:Cu, or Al:Cu:Si put on the wafers. This must be done by a technician and scheduled in advance. Include wafers T-3 and T-4.

43. Metal Photolithography: Singe wafers at 175°C for 25 min. Spin resist on at 5000 RPM for 30 seconds and then prebake at 90°C for 10 minutes. Define metal pattern using mask #6 which must be aligned to the previous mask. Expose and develop using standard resist development cycle. Wafers T-3 and T-4 may be used to adjust the exposure time. Postbake at 120°C for 20 minutes.

44. Metal etch: Etch Aluminum in metal etch at 40°C for 10–15 minutes. Time for the etch will be dependent upon the thickness of the Al. Use wafers T-3 and T-4 to determine the correct etch time. Etch until the metal clears visually across the wafer except under the patterned features then slightly overetch for another 15 to 30 seconds. Follow with two DI rinses for 4 minutes. Inspect wafers under a microscope to insure that no metal bridges exist, especially near the smallest metal features.

45. Resist strip/clean: Strip resist in resist stripper as required followed by two 4 minute DI rinse cycles. This step acts as a solvent clean for the wafers and should be done within one hour of the next step.

46. Anneal/Alloy: Alloy wafers at 450°C in the Forming Gas Anneal Furnace for approximately one hour. Insure that the forming gas is turned on.

This completes the processing of the wafers. They may be tested for continuity, photosensitivity, and processing parameters prior to PCE damage and laser testing.

Appendix D

MIPCEM Program

To provide a basis for experimental and theoretical comparisons during this research, a comprehensive microstrip and PCE simulation program was written. The FORTRAN program, called MIPCEM (for MIcrostrip and Photoconductor Circuit Element Model), brings together various analytical models and allows the entire measurement process to be simulated in whole or part. This appendix provides an overview of the basic structure of MIPCEM and how it calculates the various results. The user interface is discussed and available output results explained. The program and further documentation is available through Stanford University's Office of Technology Licensing. Since the numerical techniques used are not optimized for efficiency, but rather those with which the author was familiar, the program tends to be computationally intensive and room for improving execution speed exists.

D.1 Simulation Overview

The measurement process is modelled as it physically occurs during experimental measurements and is numerically evaluated in the frequency or time domains, whichever is analytically easier to specify or for which a model already existed. A Fast Fourier Transform (FFT) routine is used to move between the two domains, as required, and comprises the bulk of the computation time.

The simulation involves accurately modelling microstrip parameters and propagation (in a variety of conductors) and photoconductor gaps (PCEs) used as both pulsers and samplers on an SiO_2/Si substrate. The details of the expressions used in the models can be found in the body of this thesis and will not be repeated here. The microstrip frequency domain models are the most accurate expressions found in the literature for a given parameter at lower frequencies ($\leq$18 GHz) and then assumed to be valid for the entire frequency range needed by the simulation. This is generally not the case, but provides the required accuracy for a first order comparison with the measured results. Time domain models come from the literature, however, where a specific model was lacking or not directly applicable to the measurement geometry an expression was derived based upon other circuit and physical models. The program is written in modules corresponding to important parameters so that more accurate expressions can easily be incorporated as they become available. This also allows for the dynamic development of the program as research progresses.

D.2 Available Simulation Results

Since MIPCEM is designed as a comprehensive program, a large number of intermediate results are available which aid in the understanding of the physical mechanisms present in the measurements themselves. This data includes such things as the voltage waveforms produced by dispersive propagation down a microstrip transmission line as well as microstrip loss and phase velocity information. These results may be calculated separately or as part of a larger simulation, but may have a significant impact upon execution time. The results available from the program are enumerated below. How each result is requested, calculated, and output is discussed in the following two sections.

- Voltage waveforms: Four types of waveform results may be obtained. They consist of the voltage waveform as it is launched from the pulser PCE, what it looks like after propagation along a dispersive microstrip, the sampling PCE

function, and the normalized cross-correlation of the sampler PCE input with the sampling PCE function.

- Frequency spectrums: The frequency spectrum of the pulser PCE output waveform and the sampling PCE input waveform may be requested.

- Microstrip parameters: The frequency dependence of five microstrip parameters and one substrate parameter are calculated and may be requested as output. The microstrip frequency dependent parameters are:

  1. α_c - microstrip conductor attenuation
  2. α_d - microstrip dielectric attenuation
  3. α - total microstrip attenuation
  4. ν_p - microstrip phase velocity
  5. Z_0 - characteristic impedance

  The substrate parameter ϵ_{eff} is also available.

D.3 Computation Algorithms

To compute the desired results MIPCEM uses large data arrays, the size of which may be set within the main program. Currently, arrays of 40,000 elements are used, however, only half of each array is actually necessary unless the cross-correlation calculation is required. These large arrays make the program computationally intensive, but are necessary to achieve reasonably accurate results when considering very high frequencies and long time windows in a discretized environment. Smaller data sets may be used and some user control over the number of data points is provided via an input flag which may be used to speed up the execution time at the cost of accuracy. (See the Output and Format Statements found in the program documentationd.) The default mode does frequency calculations to ten times that required by the requested time window and then sets all values above the normal maximum to zero. This avoids aliasing and discretization problems in the FFT

which could lead to oscillations in the computed results. Experience has shown that only the full data set will give satisfactory results for most of the situations encountered in the measurements, however, a speed-up option is provided for quick estimates.

The first thing that the program does is to read in the *"input deck"* and process the information contained in it. If no errors are detected and some type of output is requested, calculations are begun. To minimize run time, MIPCEM attempts to calculate only those results which are either explicitly requested or necessary in the calculation of a result which is explicitly requested. For this reason, execution times may vary substantially depending upon the output requested.

Computations are begun by calculating the static circuit parameters for the specific simulation geometry. This includes estimates of gap capacitances and microstrip TEM impedances. These parameters are common to all simulations and will be done if any type of output is requested. From this point, calculations are conditional.

The pulser PCE response is generally determined next if it is not read in from a data file. Since several models are available several different calculations are possible. If only a fixed impedance microstrip load is to be assumed then numerical integration is used to solve the initial value differential equation which describes the PCE time domain response. A time variable load model is also offered and is somewhat more complex. The microstrip impedance versus frequency is first determined and then inverted in the time-domain to approximate the time varying load. A routine which uses and interpolates this data is then used during the numerical integration and the calculation proceeds as for the fixed impedance.

The next series of calculations are done in the frequency domain. MIPCEM converts the pulser PCE response using an FFT. Pulser spectrum information is directly available from the data in this form and is output, if requested, at this point. Propagation down a dispersive microstrip line is done by applying the propagation distance and the corresponding microstrip loss and phase information to the transformed PCE response. Any of the frequency dependent microstrip and substrate parameters are available during this calculation and are output as required by the

output requests. The result of this computation is the sampling PCE input in the frequency domain. Again, since the spectrum information is directly available from the data in this form it is optionally output at this point. The data is also stored in this form if a cross-correlation calculation will be done later. This is to avoid one FFT call during the later computation.

The sampler input waveform is desired in the time domain to show the effects of dispersive propagation. An inverse FFT is run on the frequency domain data and the result output to a data file if necessary. Equation D.1 shows mathematically the entire process of obtaining the time domain sampler input from the time domain pulser response, $v(t,0)$, previously calculated[D.1]. Propagation distance is denoted by z with α and β representing microstrip loss and phase parameters respectively.

$$v(t,z) = F^{-1}\left(F(v(t,0))e^{\left(-(\alpha+j\beta)z\right)}\right) \qquad (D.1)$$

The sampling function of the sampler PCE is calculated in the same manner as the pulser PCE response and the same mix of models are offered. The time domain response is available as an output, however, the computation is usually done as a prerequisite for the cross-correlation calculation. The cross-correlation of the sampler input and sampling function is done in the frequency domain since it then transforms into a simple multiplication [D.2]. This is shown by the Fourier transform pair in Equation D.2 .

$$\int_{-\infty}^{+\infty} h(\tau)x(t+\tau)d\tau \leftrightarrow H(f)X^{*}(f) \qquad (D.2)$$

The sampling function is converted to the frequency domain using an FFT call. It is then multiplied (a complex multiplication) by the frequency domain input function stored from a previous calculation. This product is converted back to the time domain with an inverse FFT and the resultant time domain waveform output to a data file. Note that the frequency domain multiplication needs twice the number of data points for the cross-correlation results to retain the same accuracy (time step) of the original functions [D.2]. The original time domain functions are therefore padded with zeroes to twice their normal size when calculated to facilitate

the cross-correlation computation. If the original time window is not sufficient to insure a decay of the waveforms to zero then this padding will introduce some error into the calculation due to the resultant discontinuity created. Care should be taken to avoid this situation.

The cross-correlation computation is the last performed during a full simulation run. At least three FFT calls are required on full data set arrays and take up the bulk of the execution time. The numerical techniques used in these calculations are not optimized for speed and this particularly is true for the FFT routine. The particular routine used is chosen because it does not limit the number of data points to a power of two. Faster FFT routines stipulate this requirement and are considered incompatible with a general purpose simulation program where the number of data points could easily change. The price of this generality is computation speed.

D.4 User Interface

MIPCEM input and output is made simple and flexible to meet the needs of the several users running the program on a variety of systems at Stanford University, the University of Florida, the U.S. Military Academy and the Los Alamos National Laboratory. It is file oriented and no user interaction is required once the simulation is started. It may thus be run in a batch or background mode if the operating system provides such a capability. This is particularly useful considering the long execution times usually encountered.

D.4.1 Output

Calculated results which are requested to be output are placed in ASCII data files named according to the information contained in them. These names are specified within the program code in such a manner so as to use FORTRAN errors to prevent overwriting previously calculated results unintentionally. As a consequence, output files must either be deleted or renamed between successive runs of MIPCEM. Failure to observe this requirement results in fatal runtime errors which halt execution and

preserve the previous data files.

The format for the data contained in the output files is the same regardless of the actual data contained in the file. The data is placed in associated pairs with the independent variable (time or frequency) first, followed by the dependent variable, one pair per line. For the independent variable, time values are in picoseconds while frequency values are in Hertz. The units for the dependent variable are specific to the data and are indicated under the allowable parameters for the FLAGS input statements. The number of data points actually written to the file is some percentage ($\approx 20\%$) of those actually calculated unless the full data set is specifically requested. This allows for sufficient information about the waveform or data set to be retained without an excessive amount of output and the resultant increase in execution time. The data is still evenly spaced and generally compatible with generic plotting programs. The exceptions to this are the frequency-domain results. The frequency spectrum data points are spaced in a pseudo-log frequency distribution so that the spacing between points is less at lower frequencies. The full data set may be requested, in which case, they are evenly spaced in frequency. If only the microstrip and substrate frequency dependent parameters are requested then the output is provided in a $\log_{10}$ frequency step and only 50 data points are calculated for each parameter in the frequency range of 10^8 to 10^{13} Hertz.

A summary of the input specifications and calculated results may also be optionally obtained during runtime in a list format. (See the example output listings in Section D.5.) The information is a record of the model, measurement and physical parameters used for the particular simulation run (either default or set), specific models chosen for the pulser and sampler, and some statistical information on the calculated time domain waveforms. This listing is sent to the standard output which may vary with the operating system. Commented code in the main program is provided to explicitly define this output as a data file, if desired.

D.4.2 Input

Two types of input are possible during the use of MIPCEM, one of which is required. The optional input is the use of a previously saved pulser PCE response waveform

as the initial input to the microstrip line. This input is in the form of a data file identical to the file which is output for the calculated pulser PCE response, to include its name. If the appropriate flag is set then some computation time may be saved by reading in the results of a previous run or measured data. If experimentally measured data is to be used the file format must conform to those described in Section D.4.1 with the points evenly spaced in time. The correct values for the time window and frequency bandwidth for the simulation are calculated from the input waveform and the simulation continued as if the program had calculated the pulser PCE waveform itself. Caution must be exercised to insure that other parameters such as gap size, microstrip width, etc. are correctly set with the appropriate input cards to be consistent with the waveform being read in.

The MIPCEM program receives its instructions on what models to use, optional parameter values, and output requests via an *"input deck"*. This *"input deck"* is expected to originate at the standard input device and is usually a data file, although some operating systems expect the user to type in the commands at a terminal. As with the output listing, commented code exists in the main program which may be used to explicitly define a file from which the *"input deck"* will be read. This is the recommended procedure since a text editor can then be used to generate and easily modify an input file prior to running MIPCEM. On operating systems where the standard input can be defined at run time (ie. UNIX), this code is not necessary. Due to the fact that the entire input file is read prior to processing any of it, some difficulties may occur if the commands are typed in at run time. Specifically, no prompting for input is provided and several blank lines (carriage returns) may be required after the last card to get the program to begin execution again. This later problem will also generate a warning message which may be ignored in this instance.

D.5 Examples

Three example runs of MIPCEM are provided in this section to show how an *"input deck"* is put together and the resultant output provided. They cover the range from a simple microstrip loss calculation to a simulation of a full cross-correlation

measurement. For each example a brief narrative of what is being simulated is provided. Following this is the *"input deck"* needed to perform the simulation, the output listing produced, and plots of any data files requested during the run.

D.5.1 Microstrip Loss Calculation

This is a relatively simple example which calculates the loss in a microstrip transmission line as a function of frequency. The default structure for the microstrip is used ($100\mu m$ wide, $1\mu m$ thick aluminum), but the substrate is redefined. A substrate of $350.5\mu m$ total thickness and resistivity of 14.5 $\Omega-cm$ is topped by $1.49\mu m$ of oxide. Note that the total thickness includes the oxide. All three loss parameters (α, α_c, α_d) are requested as output along with an output listing. The output listing will include an echoed version of the *"input deck"*.

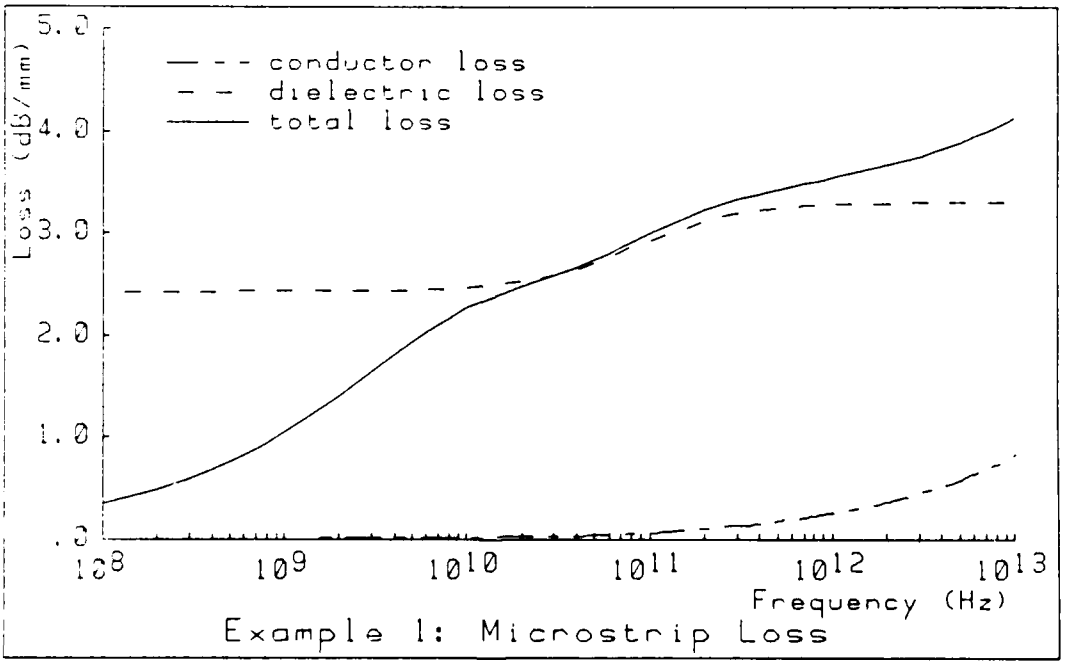


Figure D.1: Plot of the calculated loss results from the simulation run for Example 1.

Example 1 Input Deck

```
TITLE   Example 1: Microstrip Loss Calculations
COMM
COMM    Will use the default values for the microstrip
COMM    but change the wafer specifications.
WAFER   350.5 1.49 14.5
FLAGS   LIST ECHO AC AD LOSS
END     Example 1 Input Deck
```

This simulation runs very quickly since only fifty points are calculated for each of the loss parameters. This is possible because PCE responses were not also requested which would have required an FFT call and a larger data set. The output listing produced is shown below. Figure D.1 shows plots of the output data files.

Example 1 Output Listing

```
**********************************
*                                *
*   MICROSTRIP TRANSMISSION LINE *
*               AND              *
* PHOTOCONDUCTIVE CIRCUIT ELEMENT *
*        MODELLING PROGRAM       *
*                                *
*        VERSION 3.1 (7/85)      *
*                                *
**********************************

          Input Deck

 1 ... TITLE   Example 1: Microstrip Loss Calculations
 2 ... COMM
 3 ... COMM    Will use the default values for the microstrip
 4 ... COMM    but change the wafer specifications.
 5 ... WAFER   350.5 1.49 14.5
 6 ... FLAGS   LIST ECHO AC AD LOSS
 7 ... END     Example 1 Input Deck


Example 1: Microstrip Loss Calculations

SUBSTRATE PARAMETERS:
    THICKNESS =  350.5 MICRONS
    FIELD OXIDE THICKNESS =  1.490 MICRONS
    RESISTIVITY =  14.5 OHM-CM
```

```
MICROSTRIP PARAMETERS:
    WIDTH =  100.0 MICRONS
    CONDUCTOR THICKNESS = 1.00 MICRONS
    CHARACTERISTIC IMPEDANCE (Z0) =  74.28 OHMS
    RESISTIVITY = 0.262e-05 OHM-CM


REQUESTED OUTPUT RESULTS:

    CONDUCTOR ATTENUATION FACTOR VS FREQUENCY
    SUBSTRATE ATTENUATION FACTOR VS FREQUENCY
    LINE ATTENUATION FACTOR VS FREQUENCY


*****************************END MIPCEM*********************************
```

D.5.2 Pulser PCE Response

This example demonstrates how a pulser PCE simulation is requested for later use as an input to subsequent MIPCEM runs. The same microstrip and wafer structures used in Example 1 are used with a $15\mu m$ gap now defined to form the pulser PCE. The PCE parameters are set explicitly to give a carrier recombination time of 26.5 psec and leave the remaining parameters at their default values (mobility = 100 $cm^2/v-sec$, doping = 10^{14} $/cm^3$, and thickness = $0.5\mu m$). A DC bias of 10 volts is applied to the pulser and Auston's pulser model with constant load impedance specified for the simulation. Note that in the output listing the *"input deck"* is not echoed and that the full data set is requested to be output for the pulser PCE response. Also note that the **MODEL** card must contain parameters for both a pulser and sampler model even though no sampler PCE is included in this simulation.

This simulation requires more time to execute than the previous example. Two sources can be blamed for this — the larger data set needed for a possible FFT calculation (although none is actually done in this case) and the large amount of output required to write all of the data points to the data file PULOUT. Figure D.2 shows a plot of the data contained in this file. The output listing produced by the run is below. Note that the *"input deck"* is not echoed this time.

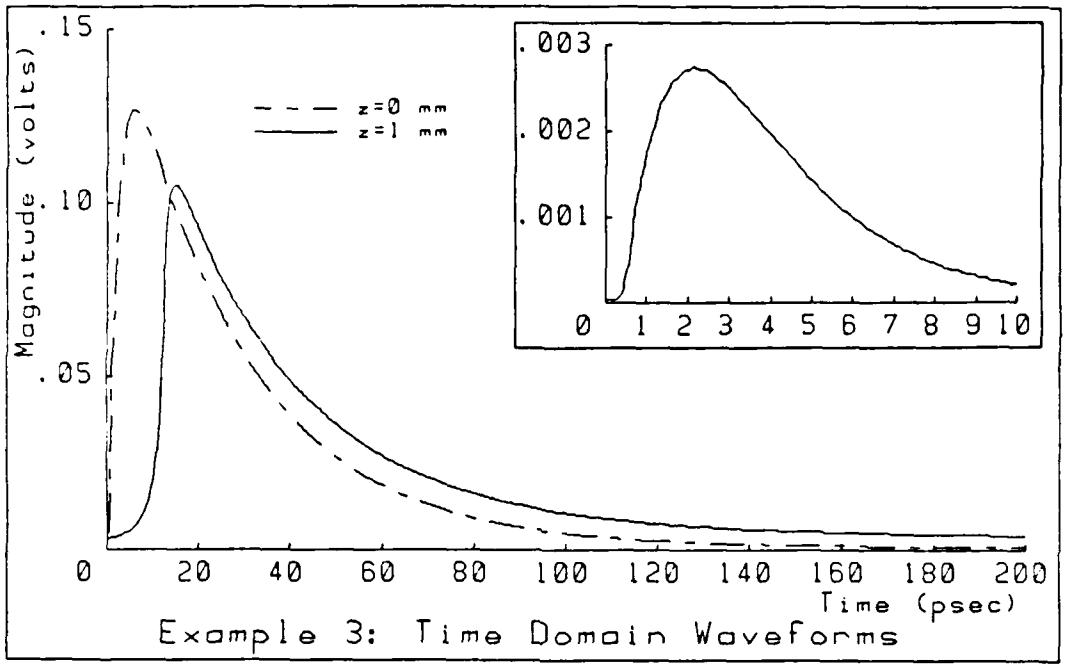


Figure D.2: Plot of the pulser PCE time domain response calculated in Example 2. The inset is a magnified plot of the rising edge of the waveform and shows the small delay in the response of the pulser PCE which is expected.

Example 2 Input Deck

```
TITLE   Example 2: Pulser PCE Response
COMM
COMM    Will use the default microstrip parameters but
COMM    explicitly define 15 micron gap parameters.
WAFER   350.5 1.49 14.5
PCE     100 1E14 0.5 26.5
GAP     15
COMM
COMM    Auston's model with fixed load impedance will be used
MODEL   3 3
BIAS    10
FLAGS   LIST INPUT FINE
END     Example 2 Input Deck
```

```
************************************
*                                  *
*   MICROSTRIP TRANSMISSION LINE   *
*              AND                 *
* PHOTOCONDUCTIVE CIRCUIT ELEMENT  *
*        MODELLING PROGRAM         *
*                                  *
*        VERSION 3.1 (7/85)        *
*                                  *
************************************

 Example 2: Pulser PCE Response

SUBSTRATE PARAMETERS:
    THICKNESS =  350.5 MICRONS
    FIELD OXIDE THICKNESS =  1.490 MICRONS
    RESISTIVITY =  14.5 OHM-CM

MICROSTRIP PARAMETERS:
    WIDTH =  100.0 MICRONS
    CONDUCTOR THICKNESS = 1.00 MICRONS
    CHARACTERISTIC IMPEDANCE (Z0) =  74.28 OHMS
    RESISTIVITY = 0.262e-05 OHM-CM

PULSER  PCE PHYSICAL PARAMETERS:
    GAP WIDTH =   15.0 MICRONS
    AVG CARRIER MOBILITY =  100.0 CM^2/V-SEC
    CARRIER RECOMBINATION TIME =  26.500 PSEC
    DOPING CONCENTRATION =  0.10e+15 CM^-3
    PCE THICKNESS =   0.50 MICRONS

PULSER  PCE CIRCUIT PARAMETERS:
    DARK RESISTANCE = 0.188e+07 OHMS
    SHUNT CAPACITANCE = 0.666e-01 FF
    SERIES CAPACITANCE = 0.135e+02 FF

PULSER  PCE MODEL USED: 3 (SEE NOTE 1)

LASER SOURCE PARAMETERS:
    WAVELENGTH =  610. NM
    FOCUS RATIO (X/D) = 0.67
    FWHM = 0.20 PSEC
    ABSORPTION COEFFICIENT =0.35e+04
    SURFACE REFLECTION COEFFICIENT = 0.30
    PULSE ENERGY (PULSER) =  40.00 PJ
    PULSE ENERGY (SAMPLER) =  40.00 PJ

PULSER PCE BIAS =  10.00 VOLTS
PCE TEMPERATURE = 300.0 K
```

```
 REQUESTED OUTPUT RESULTS:

     PULSER PCE VOUT VS TIME

  -->REQUESTED OUTPUT OF FULL DATA SET USED<--

   NOTES:
     (1) MODEL NUMBERS INDICATE THE USE OF THE FOLLOWING
     MODELS DURING THE APPROPRIATE CALCULATIONS.
         1=DERIVED MODEL WITH CONSTANT Z0
         2=DERIVED MODEL WITH FREQUENCY DEPENDENT Z0
         3=AUSTON MODEL WITH CONSTANT Z0
         4=AUSTON MODEL WITH FREQUENCY DEPENDENT Z0

*********************************************************************

 TIME INCREMENT USED IN CALCULATIONS:      0.100 PSEC
 TIME WINDOW CONSIDERED:  200.0 PSEC
 FREQUENCY INCREMENT USED IN CALCULATIONS:    500.0 MHZ
 UPPER CUTOFF FREQ CONSIDERED:   2000.0 GHZ

 AUSTON MODEL USED FOR PULSER PCE CALCULATIONS
 CIRCUIT TIME CONSTANT (Z0*CG)=    1.0 PSEC
 CIRCUIT TAU =    2.0 PSEC
 CIRCUIT RISE TIME =    4.6 PSEC

 CALCULATED:     PULSER OUTPUT
     MAX AMPLITUDE = 0.127e+00  AT TIME =   6.00 PSEC
     FWHM =   25.3 PSEC
     1/E TIME (RISE) =    4.8 PSEC
     1/E TIME (DECAY) =   29.1 PSEC
     RISE TIME (10-90) =    2.9 PSEC
     MIN AMPLITUDE = 0.   e+00  AT TIME = 200.00 PSEC

*******************************END MIPCEM**************************
```

D.5.3 Cross-correlation Calculation

This is a comprehensive example of the capability of MIPCEM to simulate the entire measurement process. The pulser PCE response from Example 2 is used as a starting point, therefore the *"input deck"* contains the same cards for the wafer and PCE as were used in that example. The pulser waveform is then allowed to propagate $1000\mu m$ down the microstrip where it is sampled by a sampling PCE. The

sampling PCE is defined to be the same as the pulser except that the recombination time is shortened to 2.0 picoseconds. In addition to the cross-correlation results, the pulser power spectrum, the sampler input and sampling functions are also requested as output.

Example 3 Input Deck

```
TITLE   Example 3: Cross-Correlation Calculation
COMM    This part is the same as Example 2 since are going
COMM    to use its calculated pulser response.
WAFER   350.5 1.49 14.5
PCE     100 1E14 0.5 26.5
GAP     15
MODEL   3 3
BIAS    10
COMM    Define the sampler PCE and place it on the microstrip.
SAPCE   15 100 2.0
DIST    1000
FLAGS   LIST PULIN SAMPL OUT CORR PPWR
END     Example 3 Input Deck
```

This simulation takes significantly longer than the previous examples because of the extra number of data points required by the cross-correlation calculation and the multiple output requests. Figure D.3 shows the individual time-domain waveforms (as well as the pulser waveform from Example 2) while Figure D.4 is a plot of the pulser power spectrum. Figure D.5 is the data from the cross-correlation calculation contained in the file COROUT. The output listing produced by this run is also provided.

Example 3 Output Listing

```
************************************
*                                  *
*   MICROSTRIP TRANSMISSION LINE   *
*              AND                 *
* PHOTOCONDUCTIVE CIRCUIT ELEMENT  *
*        MODELLING PROGRAM         *
*                                  *
*        VERSION 3.1 (7/85)        *
*                                  *
************************************
```

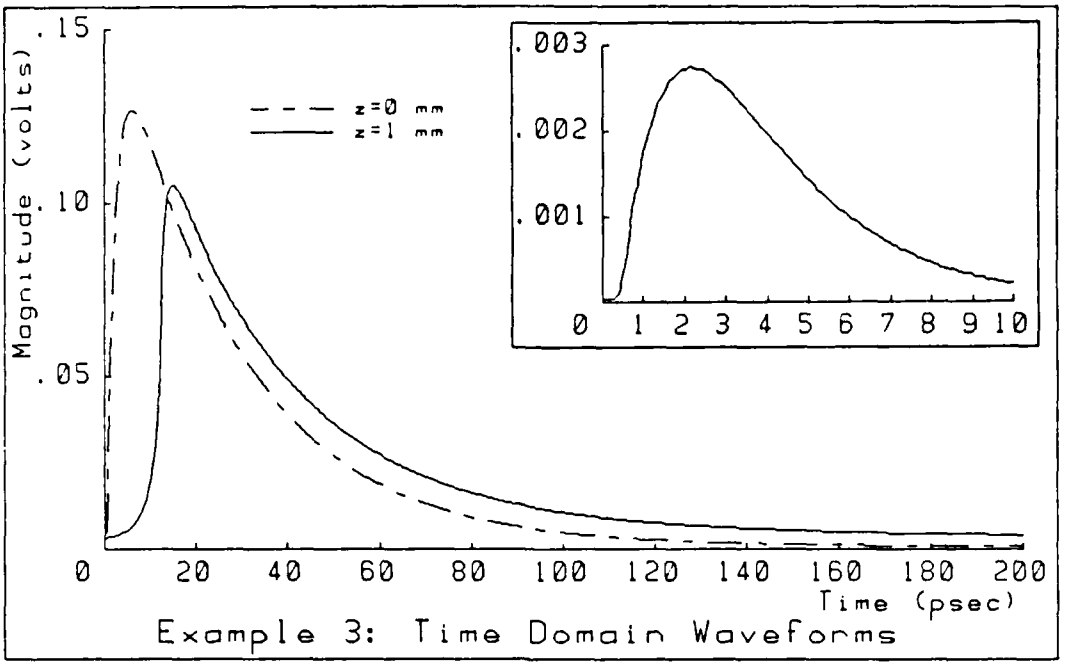


Figure D.3: Plot of the PCE time domain waveforms of Example 3. The input waveform for the sampler is the solid line. It shows readily the attenuation expected from the microstrip propagation. The inset shows the sampling function of the sampler.

```
 Example 3: Cross-Correlation Calculation

SUBSTRATE PARAMETERS:
    THICKNESS =  350.5 MICRONS
    FIELD OXIDE THICKNESS =  1.490 MICRONS
    RESISTIVITY =  14.5 OHM-CM

MICROSTRIP PARAMETERS:
    WIDTH =  100.0 MICRONS
    CONDUCTOR THICKNESS = 1.00 MICRONS
    CHARACTERISTIC IMPEDANCE (z0) =  74.28 OHMS
    RESISTIVITY = 0.262e-05 OHM-CM

PULSER  PCE PHYSICAL PARAMETERS:
    GAP WIDTH =   15.0 MICRONS
    AVG CARRIER MOBILITY =  100.0 CM^2/V-SEC
    CARRIER RECOMBINATION TIME =  26.500 PSEC
    DOPING CONCENTRATION =  0.10e+15 CM^-3
```

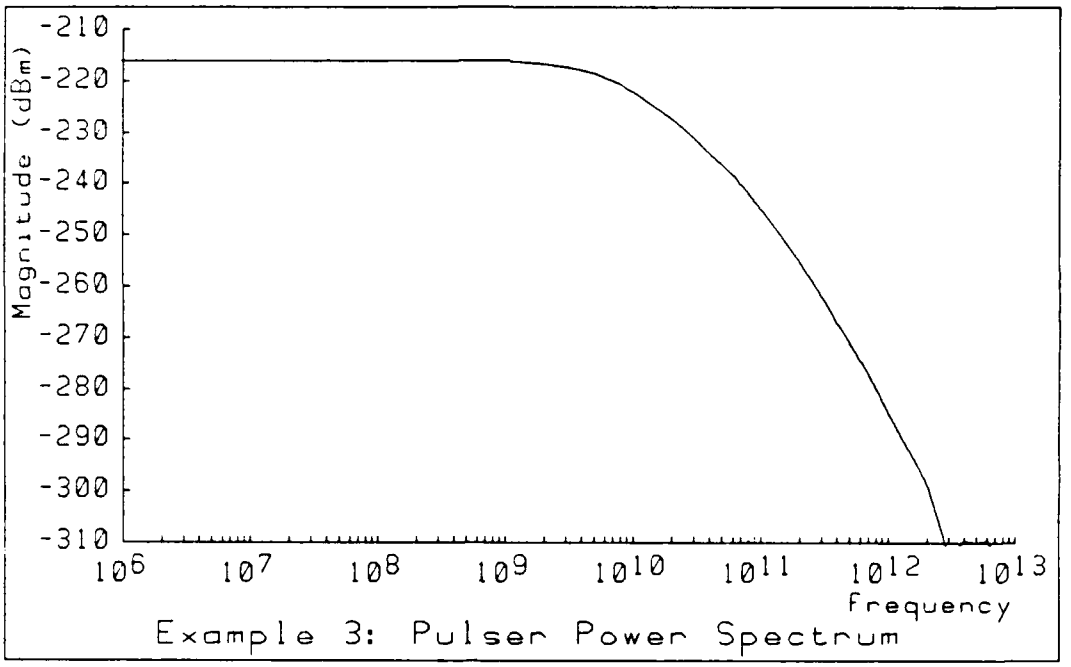


Figure D.4: Plot of the Pulser PCE power spectrum. The time domain waveform was actually calculated in Example 2 but is used as input for Example 3 where the spectrum result is requested.

```
     PCE THICKNESS =    0.50 MICRONS

 PULSER  PCE CIRCUIT PARAMETERS:
     DARK RESISTANCE = 0.188e+07 OHMS
     SHUNT CAPACITANCE = 0.666e-01 FF
     SERIES CAPACITANCE = 0.135e+02 FF

 PULSER  PCE MODEL USED: 3 (SEE NOTE 1)



 SAMPLER PCE PHYSICAL PARAMETERS:
     GAP WIDTH =    15.0 MICRONS
     AVG CARRIER MOBILITY =  100.0 CM^2/V-SEC
     CARRIER RECOMBINATION TIME =    2.000 PSEC
     DOPING CONCENTRATION =  0.10e+15 CM^-3
     PCE THICKNESS =    0.50 MICRONS
     SAMPLER MICROSTRIP WIDTH =  100.0 MICRONS
     SAMPLING DISTANCE =  1000. MICRONS

 SAMPLER PCE CIRCUIT PARAMETERS:
     DARK RESISTANCE = 0.188e+07 OHMS
```

```
     SHUNT CAPACITANCE = 0.666e-01 FF
     SERIES CAPACITANCE = 0.135e+02 FF

 SAMPLER PCE MODEL USED: 3 (SEE NOTE 1)

 LASER SOURCE PARAMETERS:
     WAVELENGTH =  610. NM
     FOCUS RATIO (X/D) = 0.67
     FWHM = 0.20 PSEC
     ABSORPTION COEFFICIENT =0.35e+04
     SURFACE REFLECTION COEFFICIENT = 0.30
     PULSE ENERGY (PULSER) =  40.00 PJ
     PULSE ENERGY (SAMPLER) =  40.00 PJ

 PULSER PCE BIAS =  10.00 VOLTS
 PCE TEMPERATURE = 300.0 K

 REQUESTED OUTPUT RESULTS:

     PULSER PCE POWER SPECTRUM
     SAMPLER PCE VOUT VS TIME
     CROSS-CORRELATION CALCULATION RESULTS

    PULSER PCE VOUT VS TIME DATA READ FROM DATA FILE   PULOUT

   NOTES:
     (1) MODEL NUMBERS INDICATE THE USE OF THE FOLLOWING
     MODELS DURING THE APPROPRIATE CALCULATIONS.
         1=DERIVED MODEL WITH CONSTANT Z0
         2=DERIVED MODEL WITH FREQUENCY DEPENDENT Z0
         3=AUSTON MODEL WITH CONSTANT Z0
         4=AUSTON MODEL WITH FREQUENCY DEPENDENT Z0

*****************************************************************


 ESTIMATE BACK-PLANE REFLECTION AT  13.92 PSEC

 READING PULSER PCE TIME RESPONSE FROM DATA FILE
 2000 DATA POINTS READ
 RESETTING TIME WINDOW TO  200.0 PSEC TO CONFORM TO THIS DATA

 TIME INCREMENT USED IN CALCULATIONS:      0.100 PSEC
 TIME WINDOW CONSIDERED:  200.0 PSEC
 FREQUENCY INCREMENT USED IN CALCULATIONS:    500.0 MHZ
 UPPER CUTOFF FREQ CONSIDERED:   2000.0 GHZ

            PULSER OUTPUT
```

```
MAX AMPLITUDE = 0.127e+00  AT TIME =   6.00 PSEC
FWHM =   25.3 PSEC
1/E TIME (RISE) =    4.8 PSEC
1/E TIME (DECAY) =   29.1 PSEC
RISE TIME (10-90) =    2.9 PSEC
MIN AMPLITUDE = 0.   e+00  AT TIME =   0.   PSEC

     PULSER OUTPUT POWER SPECTRUM ESTIMATE
     DC VALUE = -216.0 DBM
     -3DB FREQ =     6.0 GHZ

       SAMPLER INPUT
MAX AMPLITUDE = 0.104e+00  AT TIME =  15.30 PSEC
FWHM =   24.8 PSEC
1/E TIME (RISE) =    3.7 PSEC
1/E TIME (DECAY) =   30.9 PSEC
RISE TIME (10-90) =    4.5 PSEC
MIN AMPLITUDE = 0.206e-02  AT TIME =   0.   PSEC

AUSTON MODEL USED FOR SAMPLER PCE CALCULATIONS
CIRCUIT TIME CONSTANT (Z0*CG)=    1.0 PSEC
CIRCUIT TAU =    1.5 PSEC
CIRCUIT RISE TIME =    5.0 PSEC

      SAMPLER FUNCTION
MAX AMPLITUDE = 0.273e-02  AT TIME =   2.20 PSEC
FWHM =    4.3 PSEC
1/E TIME (RISE) =    1.5 PSEC
1/E TIME (DECAY) =    3.8 PSEC
RISE TIME (10-90) =    1.0 PSEC
MIN AMPLITUDE = 0.   e+00  AT TIME = 200.00 PSEC

   CROSS-CORRELATION
MAX AMPLITUDE = 0.100e+01  AT TIME =  12.50 PSEC
FWHM =   27.4 PSEC
1/E TIME (RISE) =    6.5 PSEC
1/E TIME (DECAY) =   32.2 PSEC
RISE TIME (10-90) =  105.1 PSEC
MIN AMPLITUDE = 0.164e-01  AT TIME =-200.00 PSEC


**************************END MIPCEM*****************************
```

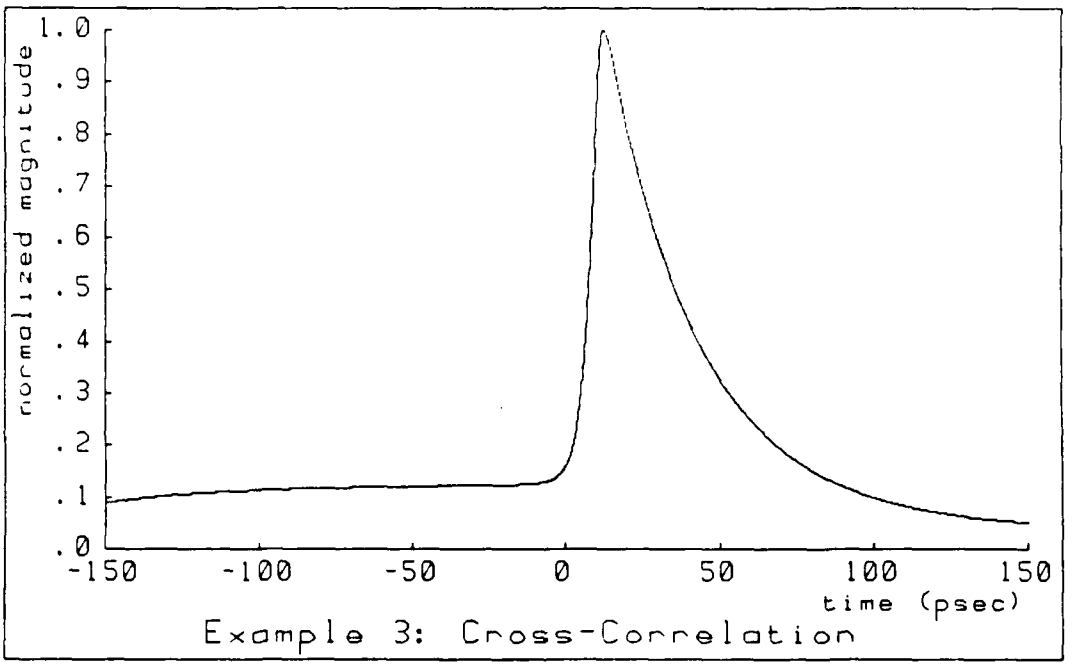


Figure D.5: Plot of the cross-correlation results calculated during the simulation run for Example 3.

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