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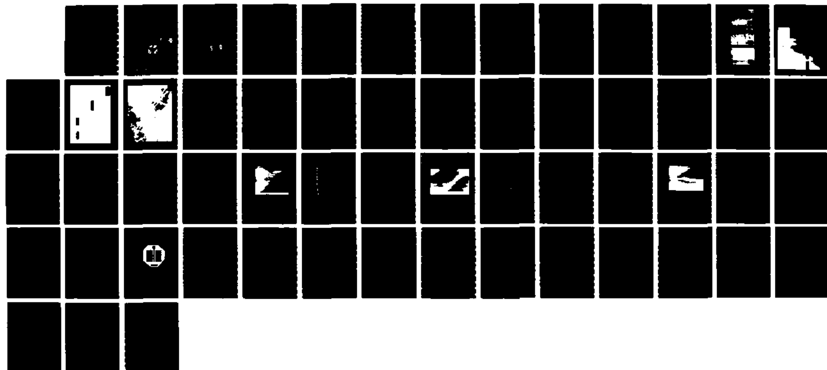

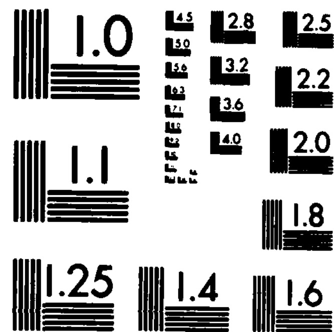

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Semi-annual Progress Report

on

FUNDAMENTAL STUDIES AND DEVICE DEVELOPMENT
IN BETA SILICON CARBIDE

Supported by ONR Under Contract N00014-82-K-0182 P0005

For the Period February 1, 1986 - August 31, 1986

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The research of this period has involved the growth and characterization of cubic β-SiC on hexagonal α-SiC substrates. The resulting films were virtually defect free in contrast to those grown on Si. Additional research has included ion implantation at temperatures sufficient to achieve significant dynamic annealing and p-type samples in the as-implanted state. Efforts geared to making devices have included (1) the use of the new etchant gas, NF_3, in the RIE mode and SF_6 in the plasma etching mode with very positive results in terms of high etch rate and surface smoothness. MESFET and MOS structures have also been fabricated.

1 Introduction

Silicon carbide is the only compound species that exists in the solid state in the Si-C system and can occur in the cubic (C), hexagonal (H) or rhombohedral (R) structures. It is also classified as existing in the beta and alpha modifications. The beta, or cubic, form crystallizes in the zincblende or sphalerite structure; whereas, a large number (approximately 140) of the alpha occur in the hexagonal or rhombohedral forms known as polytypes.

Because of the emerging need for high temperature, high frequency and high power electronic devices, blue L.E.D.'s, Schottky diodes, U. V. radiation detectors, high temperature photocells and heterojunction devices, silicon carbide is being examined throughout the world for employment as a candidate material in these specialized applications. The electron Hall mobility of high purity updoped β-SiC has been postulated from theoretical calculations to be greater than that of the α-forms over the temperature range of 300-1000K because of the smaller amount of phonon scattering in the cubic material. The energy gap is also less in the β-form (2.3 eV) compared to the α-forms (e.g., 6H = 2.86 eV). Thus, the β-form is now considered more desirable for electronic device applications, and therefore, improvements in the growth and the characterization of thin films of this material and device development from this material constitute principal and ongoing objectives of this research program.

The research of this reporting period has involved the growth and characterization of cubic β-SiC on hexagonal α-SiC substrates, ion implantation of Al^+ and N^+ at elevated temperatures sufficient to achieve dynamic annealing and n- and p-type conduction in the as-implanted state and efforts geared to the fabrication of devices including dry etching studies, and the production of MOS structures and MESFET devices.

2 Beta Silicon Carbide Growth Research

2.1 Introduction

Although crack-free, reproducible β-SiC (100) monocrystalline thin films are currently being grown heteroepitaxially on Si(100) wafers[1-4*], these films contain, within an $\approx$3 μm thick interface region, residual strain, a high density of misfit dislocation and stacking faults. This region of high defect density is formed primarily as a result of the differences in the lattice parameters ($\approx$20%) and in the coefficients of the thermal expansion ($\approx$8% at 473K) between the substrate and film. Many of the dislocations and most of the stacking faults actually extend to the surface of the as-grown film. As a result of these defects, charge carrier redistribution occurs and the introduction via diffusion of impurity dopants from the β-SiC film into the Si substrate is facilitated.[5] It is also probable that these defects reduce the carrier mobilities. In addition to the above effects, it has been ascertained that temperatures considerably above the melting point of the Si substrates are normally required to electrically activate certain ion implanted impurities via thermal annealing. All of these factors provide an impetus to conduct exploratory research using substrates other than Si.

The substrate of choice is monocrystalline SiC. The primary source of these crystals has been and continues to be the commercial Acheson furnace used to make SiC grit for abrasive applications. However, recent research[6,7] into the growth of high purity, bulk crystals via other sublimation techniques appears promising.

The growth of SiC on SiC substrates via CVD has been reported by several investigators[8-14] since the late 1960's. There are a number of papers which have reported the growth of α-SiC on α-SiC substrates in the temperature ranges and companion growth directions of 1773K to 2023K[8,9,10] (parallel to the [0001] axis) and 1593K to 1663K (perpendicular to the [0001] axis). A few papers also reported the growth of β-SiC on α-SiC substrates in the temperature range of 1773K to 1973K[12,13] and the growth of β-SiC on β-SiC substrates in the temperature range of 1473K to 2073K[14]. In some of these cases, the investigators were able to achieve single crystal β-SiC epilayers. However, the interface between the SiC epilayer and the SiC substrate has not previously been studied. In recent research at NCSU an examination of this interface in cross section via transmission electron microscopy (TEM) and transmission electron diffraction (TED) has been conducted. The determination of the optimum growth conditions in the current CVD apparatus for obtaining high quality β-SiC films on 6H-SiC substrates has also been carried out.

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*References for this and succeeding sections appear at the end of the last technical section of this report.

2.2 Experimental Procedures

2.2.1 Substrate Preparation

To examine the potential of using SiC substrates for β-SiC thin film CVD growth, black, industrial 6H-SiC (0001) wafers, obtained at random from an Acheson furnace, were employed. Each 6H-SiC substrate was preoxidized at 1473K in flowing dry oxygen for 1.5 hours to remove approximately 50 nm of the as-grown surface. The resulting oxide layer was removed using a solution of 1:1 $HF+HNO_3$ immediately prior to loading on a SiC-coated graphite susceptor for the CVD operation. The carbon $(000\bar{1})$ face and the silicon (0001) face were easily distinguished following the oxidation, since the former is more thermally reactive. Thus a thick oxide layer relative to that obtained on the Si face was always produced.

2.2.2 Growth Procedure

The same CVD system used for the growth of β-SiC on Si, and described in earlier reports, was also employed for the deposition of β-SiC on 6H-SiC. The system was evacuated to 10^{-5} Torr to remove air and moisture before growth. The complete procedure is illustrated in Figure 1.

The substrates were initially heated at 1683K for 600 s in 1 atm. of flowing H_2 (3000 sccm) to effect etching of the SiC surface. The reactive gases of SiH_4 and C_2H_2 were subsequently introduced into the H_2 stream to allow SiC deposition under the same temperature and total pressure. The ratio of the sum of the flow rates (sccm) of SiH_4 and C_2H_4 to the flow rate (sccm) of H_2 was varied from 3:3000 to 1:3000. The optimum ratio was found to be 1:3000. The SiH_4/C_2H_4 flow rate ratio was kept at two in every experiment.

2.2.3 Growth Rate Determinination

The thickness of the resulting films and the growth rates at the various experimental conditions were measured via a combination of angle lapping and observation with an optical microscope having a calibrated eyepiece.

The interface between the as-grown film and the substrate were easily distinguishable in the microscope.

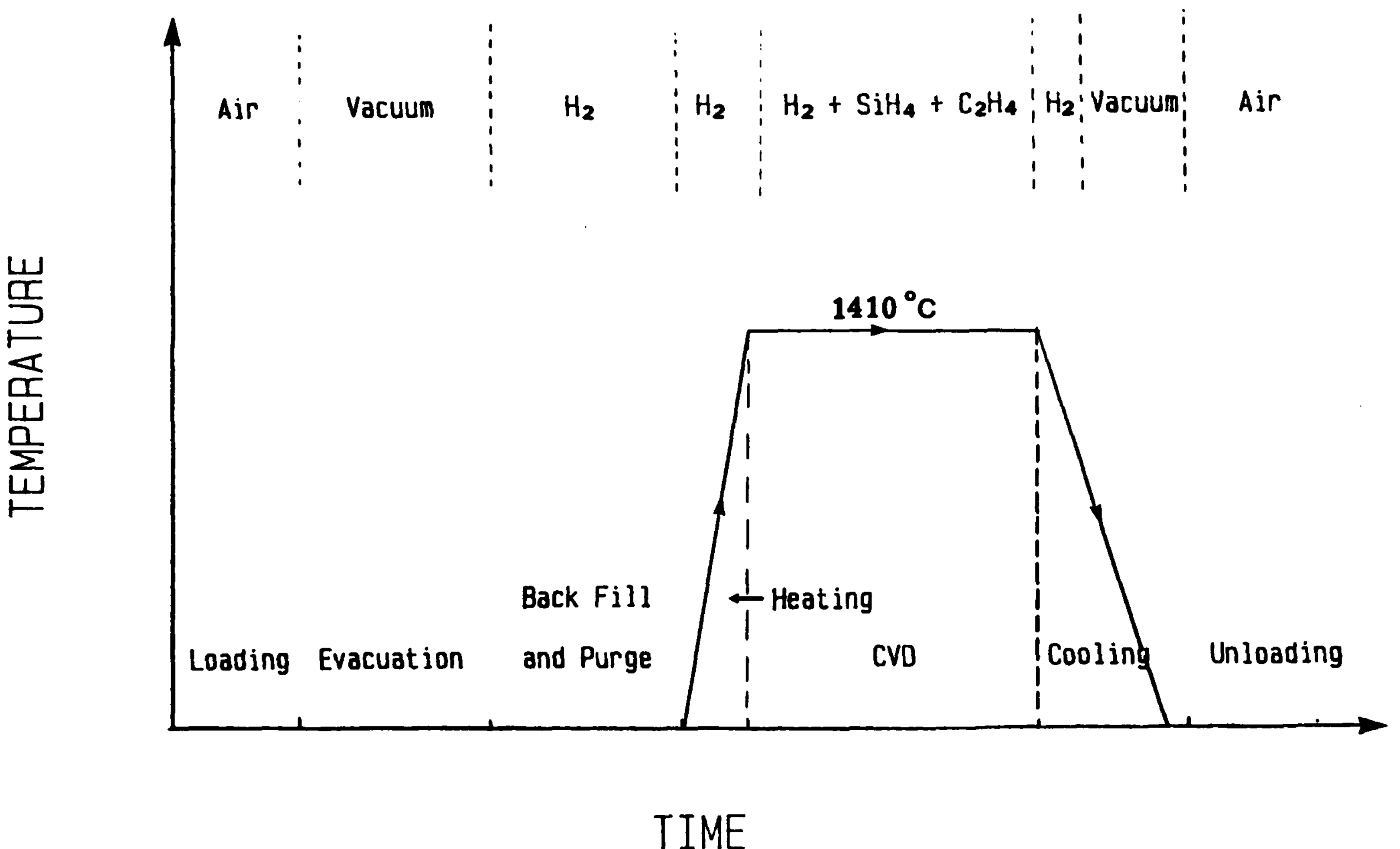


Figure 1. **Schematic diagram for the growth sequence employed to grow monocrystalline β-SiC thin films on 6H α-SiC substrates.**

2.3 Results and Discussion

2.3.1 Growth Rate

The growth rate on the (000$\bar{1}$) C face decreased as the ratio of the flow rates of the source gases to the H_2 gas was decreased, as shown in Figure 2. Similar behavior was found in the case of growth on the Si(0001) face. However, the growth rates on the C(000$\bar{1}$) face were always higher for a given ratio. The remainder of this Section is concerned exclusively with growth on the C face.

2.3.2 Surface Morphology

The effects of altering the source gas-to-carrier gas flow ratio on the surface morphology of the thin films grown on the C(000$\bar{1}$) face of a 6H-SiC wafer are shown in the optical micrographs of Figure 3. A decrease in this ratio changed the crystallization behavior from polycrystalline to monocrystalline.

The use of the flow ratio of 3:3000 results in the deposition of polycrystalline films having a very rough surface, as shown in Figure 3(a). In this case, during the initial growth stage, a high density of nuclei having different orientations are formed which grow and impinge to produce the polycrystalline character. If the flow ratio is decreased to 1.5:3000, monocrystalline films having a pyramidal surface morphology are observed (see Figure 3(b)). However, the concentrations of the reactive gases are sufficiently high such as to yield an undesirably high density of critical nuclei. The close proximity of the resulting growth pyramids limits the surface migration of adatoms between the pyramids. This decreases the lateral growth rate, and vertical growth dominates. At the lowest source/carrier gas ratio of 1:3000, sufficient time is available for the formation of smooth flat growth steps on the final surface, as shown in Figure 3(c). The small number of critical nuclei present allows enhanced lateral growth of the film. On-going research is concerned with the influence of temperature on the onset of layer-type growth at various source/carrier gas ratios.

2.3.3 Cross-sectional Transmission Electron Microscopy

XTEM was used in conjunction with TED to identify the structure and to characterize the microstructure of the epilayer and the epilayer/substrate interface region. The results of this research are presented collectively in Figure 4. Diffraction patterns (1) and (3) were observed from the 4.5 μm thick epilayer and the substrate, respectively, and show reflections characteristic of the β-SiC [10$\bar{1}$] pole and the 6H-SiC [11$\bar{2}$0] pole. Pattern (2), taken from the interface region, is a mixture of patterns (1) and (3) as a result of the overlap of the beam onto both parts of the sample. According to these patterns, the β-SiC (10$\bar{1}$) face is parallel to the 6H-SiC (11$\bar{2}$0) face and the β-SiC (111) face is parallel to the 6H-SiC (0001) face.

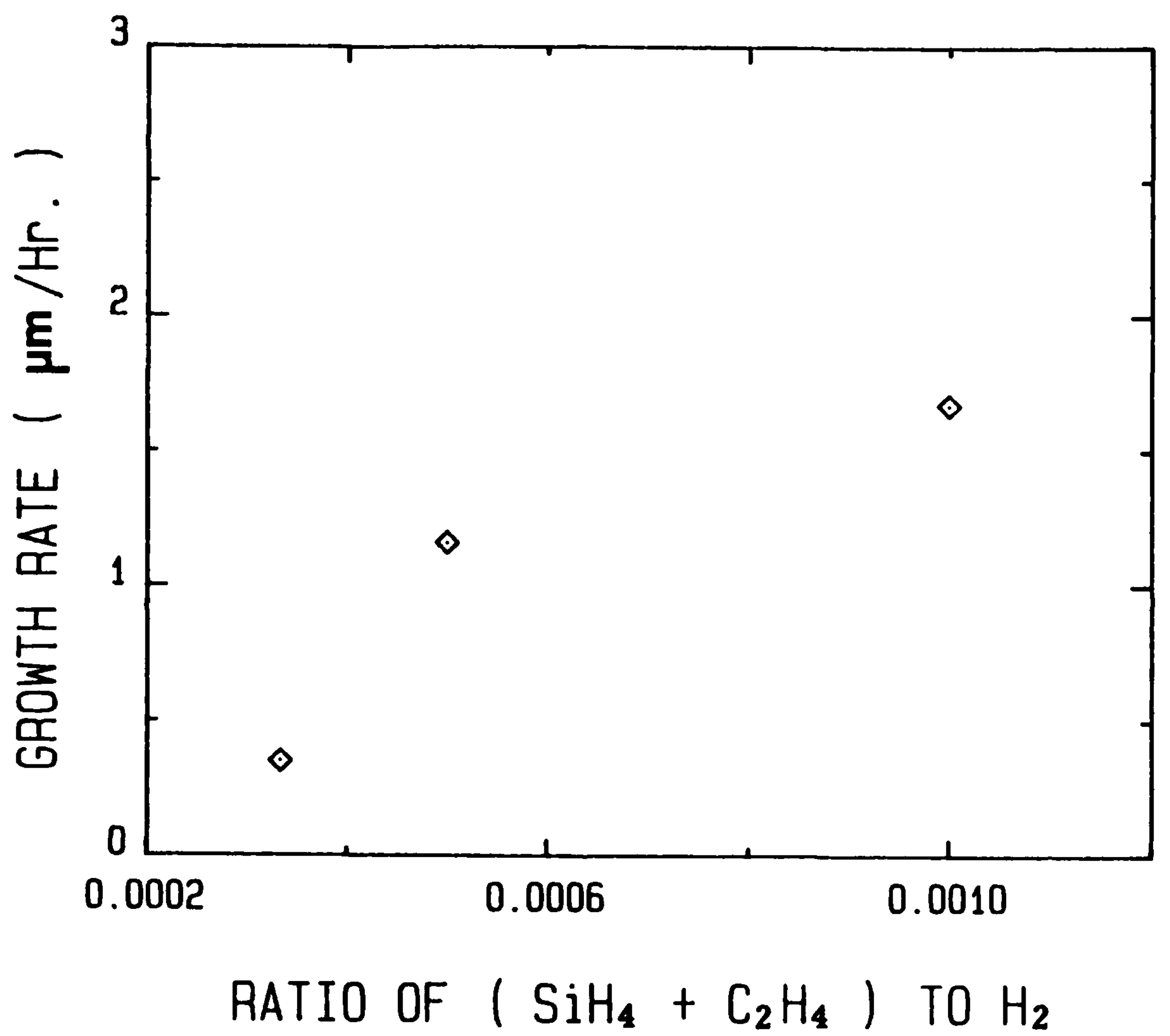
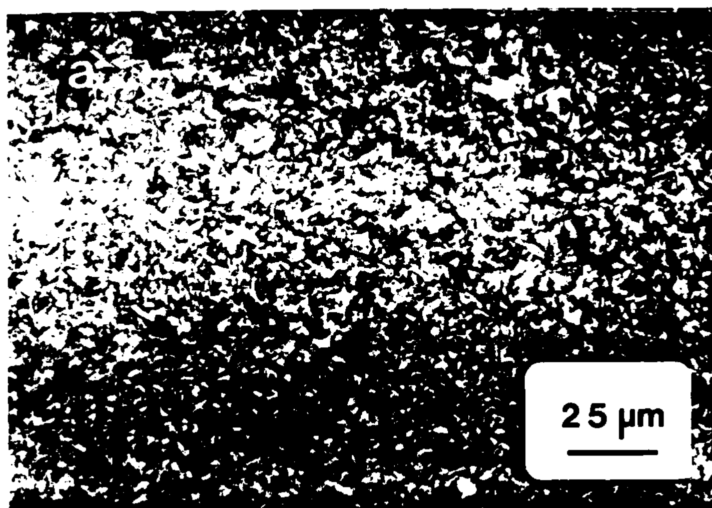
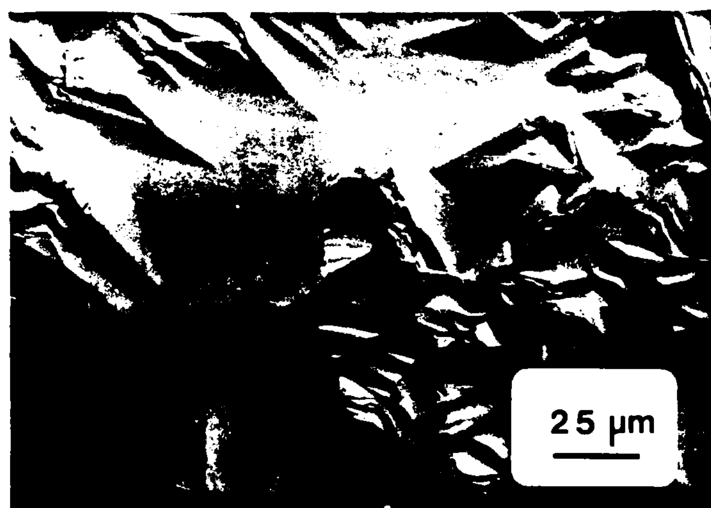


Figure 2. Deposition rate of the β-SiC films on 6H α-SiC as a function of the ratio of the gas flow rates of the source gases to H_2.





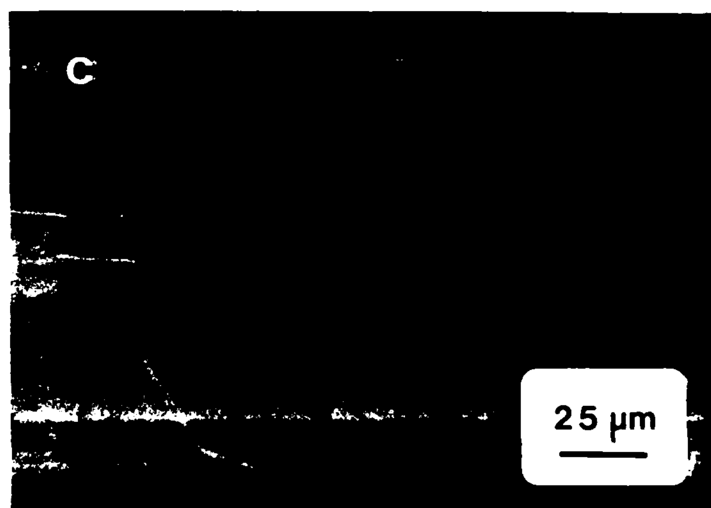


Figure 3. Optical micrographs of the surface morphologies of β-SiC films grown on the (000$\bar{1}$) C face of 6H-SiC at 1683 K. The gas flow rate ratios of SiH_4 + C_2H_4 to that of H_2 were (a) 3:3000, (b) 1.5:3000 and (c) 1:3000.

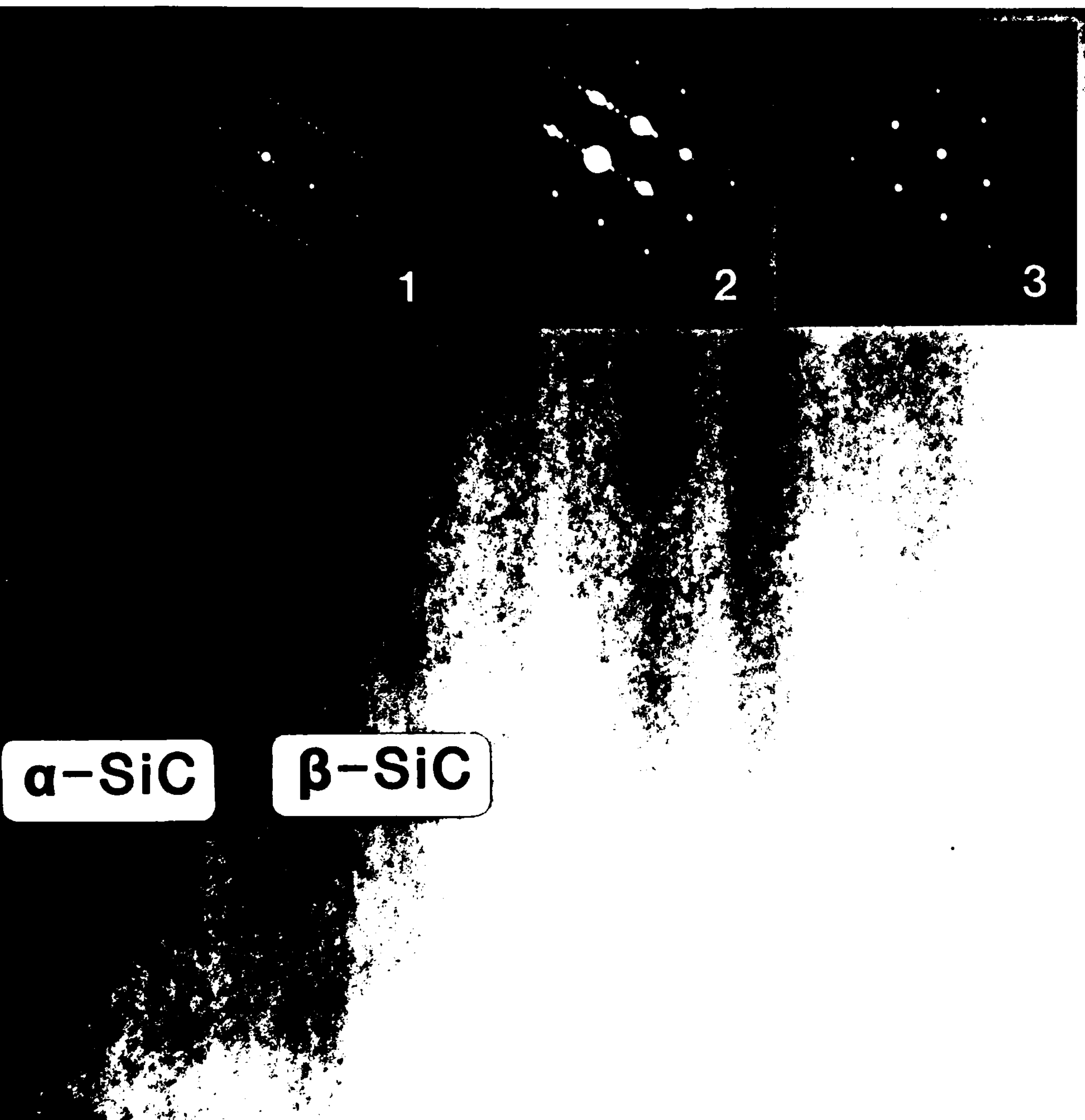


Figure 4. TEM micrograph of the cross-section of the β-SiC/6H-SiC interface region. The three TED patterns in the upper part of the micrograph show (a) the 6H-SiC[$11\bar{0}$] pole diffraction pattern taken from the substrate, (b) the diffraction pattern taken from the β-SiC/6H-SiC interface region and (c) β-SiC[$10\bar{1}$] pole diffraction pattern taken from the epilayer. This micrograph also shows no line or planar defects either in the bulk of the β-SiC epilayer or at the interface.

The most significant observation in Figure 4 is that no line or planar defects can be seen either in the "bulk" layer of the β-SiC film or at the interface. A higher resolution image of the interface region of another TEM sample is shown in Figure 5. The electron beam is parallel to the $[10\bar{1}]$ direction of the epilayer. Even at this magnification, the interface is very clean and free of defects. The lattice fringes of the α-SiC substrate can be clearly seen and represent the traces of the $(000\bar{1})$ planes. One of the fringes runs completely across the interface which indicates that the growth direction of the β-SiC film is exactly $[\bar{1}\bar{1}\bar{1}]$.

The bulk of each of the β-SiC films was also essentially defect free. This is in strong contrast with films grown on Si substrates which, as noted above and shown in Figure 6, contain numerous defects in the interface region. Thus, the crystalline perfection of the β-SiC epilayer is dramatically improved by using 6H-SiC rather than Si(100) as the substrate.

2.3.4 Carrier Concentrations as a Function of Sample Depth

The top surface of a β-SiC film was initially polished with 0.25 μm diamond paste and subsequently oxidized and etched in an acid solution of 1:1 HF:HNO_3 to remove the subsurface polishing damage. This produced a very flat, smooth and damage-free surface having the lowest possible leakage current for the electrical studies noted below.

The concentration of active carriers and the distribution of these carriers as a function of depth in a β-SiC film were measured using a Miller profile. A 7 mm$\times$8 mm$\times$4.5 mm thick unintentionally doped sample (#860619(3)) was used for this purpose. The polished β-SiC film was not removed from the n-type α-SiC substrate prior to the measurements.

The β-SiC epilayer was found to be n-type with a carrier concentration of $\approx 7\times10^{16}cm^{-3}$ as shown in Figure 7. This value of the concentration remained constant as a function of sample depth and is in the range normally measured for the undoped β-SiC on Si(100). Thus, the greatly improved crystalline perfection of the film has not resulted in a reduced value of the charged carrier concentration. Reasons for this are now under investigation.

3 Ion Implantation and Annealing Studies

3.1 Basic Studies in Amorphization Processes During Ion Implantation

3.1.1 Implantation of $^{30}Si^+$ and $^{13}C^+$

The solid phase epitaxial (SPE) regrowth at 1973K for 300 s of a β-SiC layer preamorphized by implantation of $^{28}Si^+$ plus $^{12}C^+$ was previously reported. As a result of the extremely

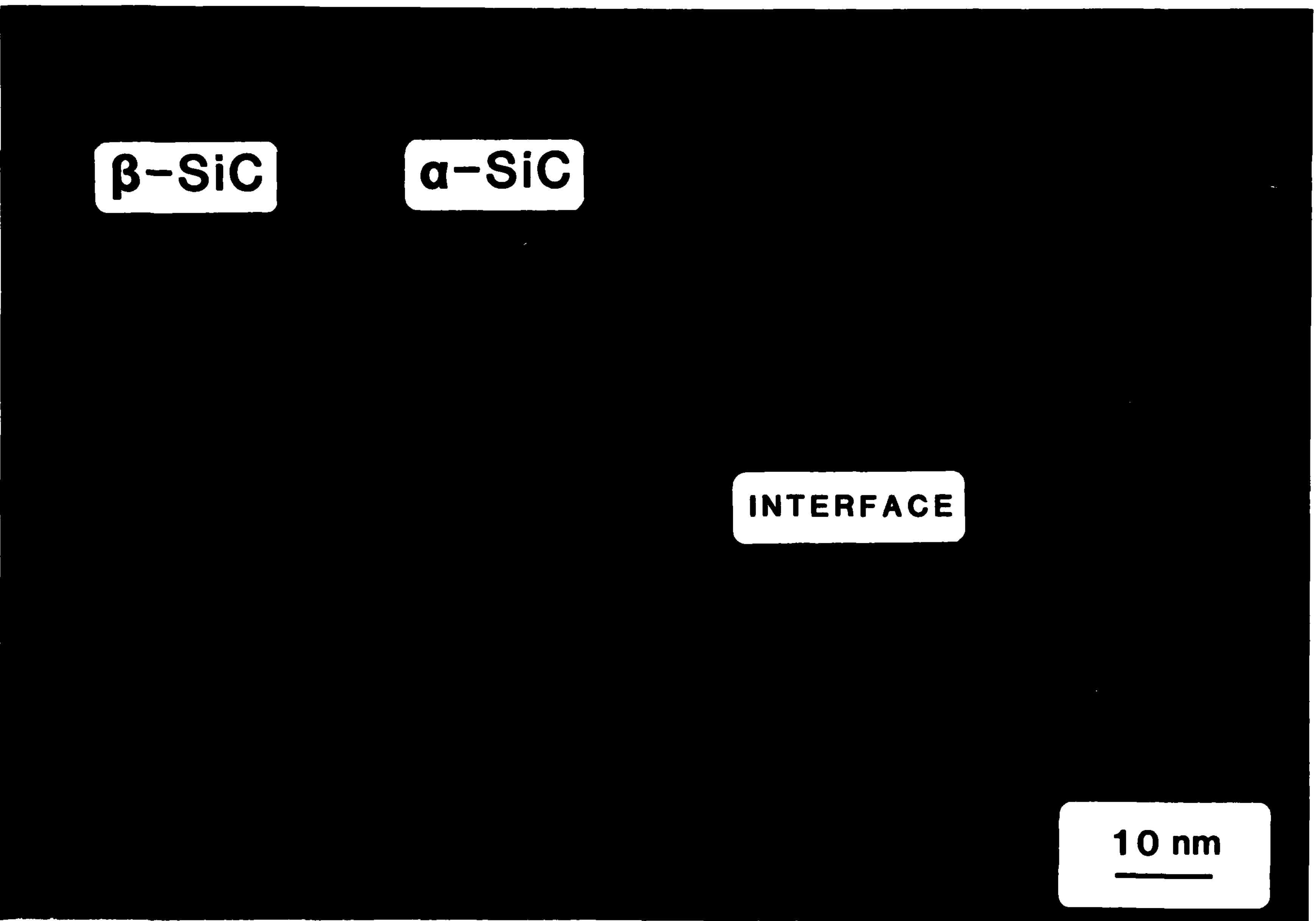


Figure 5. TEM micrograph of the cross-section of the β-SiC/6H-SiC interface region at high magnification. A lattice image is formed in the α-SiC substrate. One of the fringes in the image crosses the interface into the film which indicates that the growth direction of β-SiC was exactly [1$\bar{1}$1].

Figure 6. TEM micrograph of the cross-section of a single crystal thin film of undoped CVD β-SiC deposited on a single crystal Si (100) substrate at 1683K at 1 atm. using a gas mixture of SiH_4, C_2H_4 and H_2. The micrograph shows the full range of defects present in the as-grown film including stacking faults, partial and misfit dislocations and interfacial strain contrast g = [022].

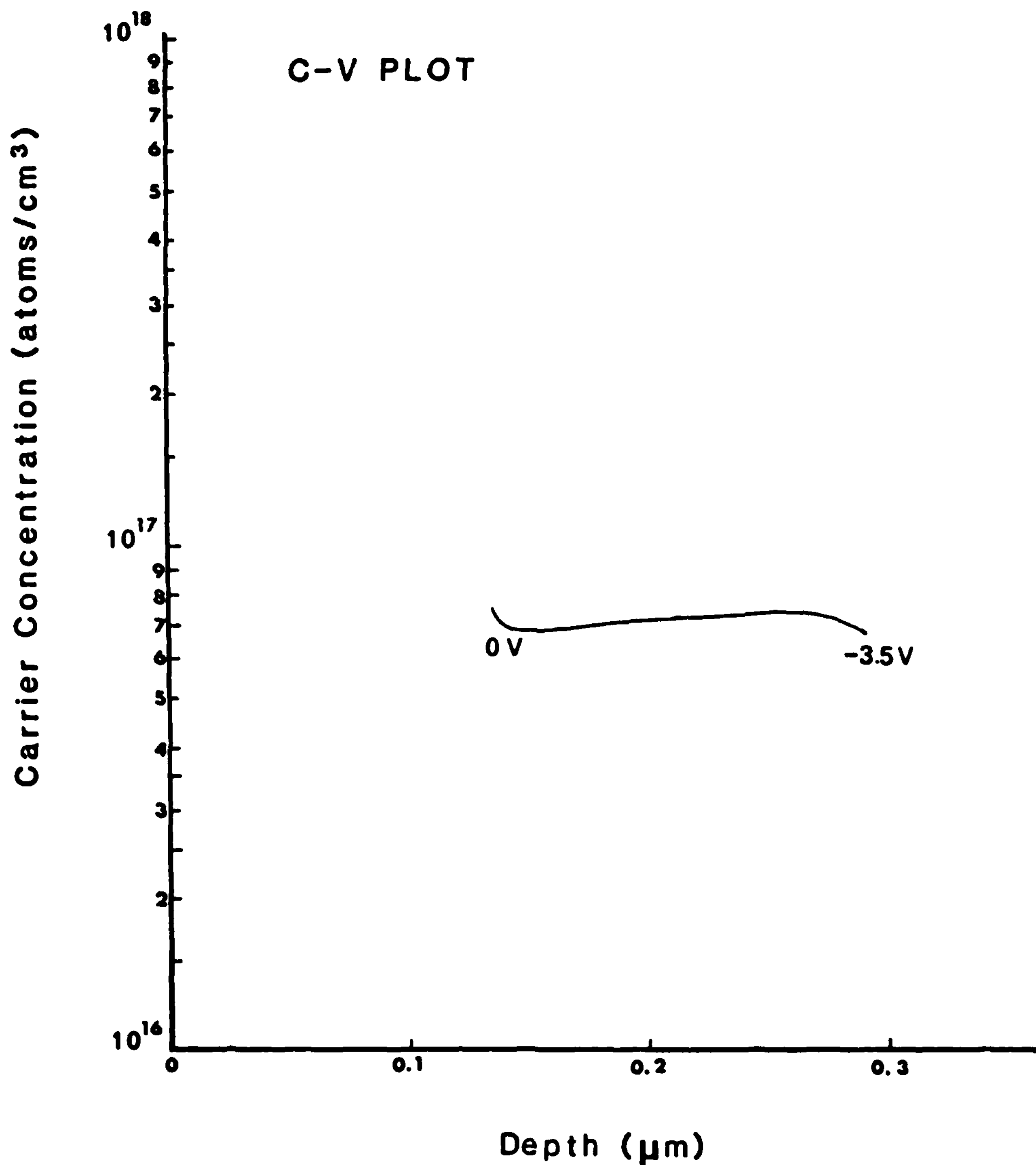


Figure 7. Carrier concentration as a function of sample depth in a 7 x 8 mm x 4.5 μm thick, undoped β-SiC thin film grown on a 6H α-SiC substrate (sample #860619C3).

Table I: $^{30}Si^+$ and $^{13}C^+$ Implant Conditions

Sample #	Figure	Ion	Energy	Dose(cm^{-2})	Temp.
850904-5	8(a)	$^{30}Si^+$	160	5.39×10^{16}	LN
	8(a)	$^{13}C^+$	67	5.40×10^{16}	LN
850523-1	8(b)	$^{30}Si^+$	128	4.70×10^{16}	LN
	8(b)	$^{13}C^+$	67	5.40×10^{16}	LN

high concentration of stacking faults which occurred during this high temperature recrystallization of these samples, it was speculated that a 1:1 Si-to-C ratio was not achieved during implantation. To verify this, ^{30+}Si and $^{13}C^+$ isotopes were implanted under the same experimental conditions as before. Secondary Ion Mass Spectrometry (SIMS) was utilized to obtain a depth profile of each isotope. Figure 8(a) shows the resulting log-linear plots. Clearly, the two profiles deviate greatly from one another. The $^{13}C^+$ profile is as predicted by LSS theory; whereas, the contrary is true for the $^{30}Si^+$ implant. As shown, the peak atomic concentration for the latter was 33% low, the implant straggle 15% high and projected range 33% high.

In an attempt to correct this problem, the implant conditions were appropriately altered as summarized in Table I. Figure 8(b) shows the SIMS plot as a result of the modifications in the implant dose and energy. The implant energy was adjusted so that the projected range of each ion was matched, as shown in Figure 8(b). Although these profiles overlap to a greater extent than those from the previous attempt, a 1:1 Si to C ratio was not achieved throughout the profile. Cross-sectional TEM is presently being performed in order to compare the regrowth quality of the two samples described above.

3.1.2 Comparison of Theoretical and Experimental Values of the Critical Energies Necessary to Cause Amorphization at LN Temperature

As part of an ongoing study of electronic device fabrication in β-SiC Rutherford backscattering (RBS) in an ion channeling geometry was used to study damage accumulation as a function of dose for Al ion implantation at liquid nitrogen temperature. The RBS damage depth profile results have been compared to damage depth profiles using a computer simulation program in order to calculate the critical energy deposition needed to cause amorphization of the crystalline lattice.

Samples were implanted at LN temperature with 123 keV $^{27}Al^+$ at various doses. The increase in lattice damage as a result of implantation was characterized by the Si RBS signal obtained using a 2.0 MeV He incident along the <110> direction. The spectra in Figure 9 illustrate the accumulation of damage. Damage increased in the crystal lattice with increasing dose until the sample became amorphous at a dose of $3\times10^{14}cm^{-2}$. At

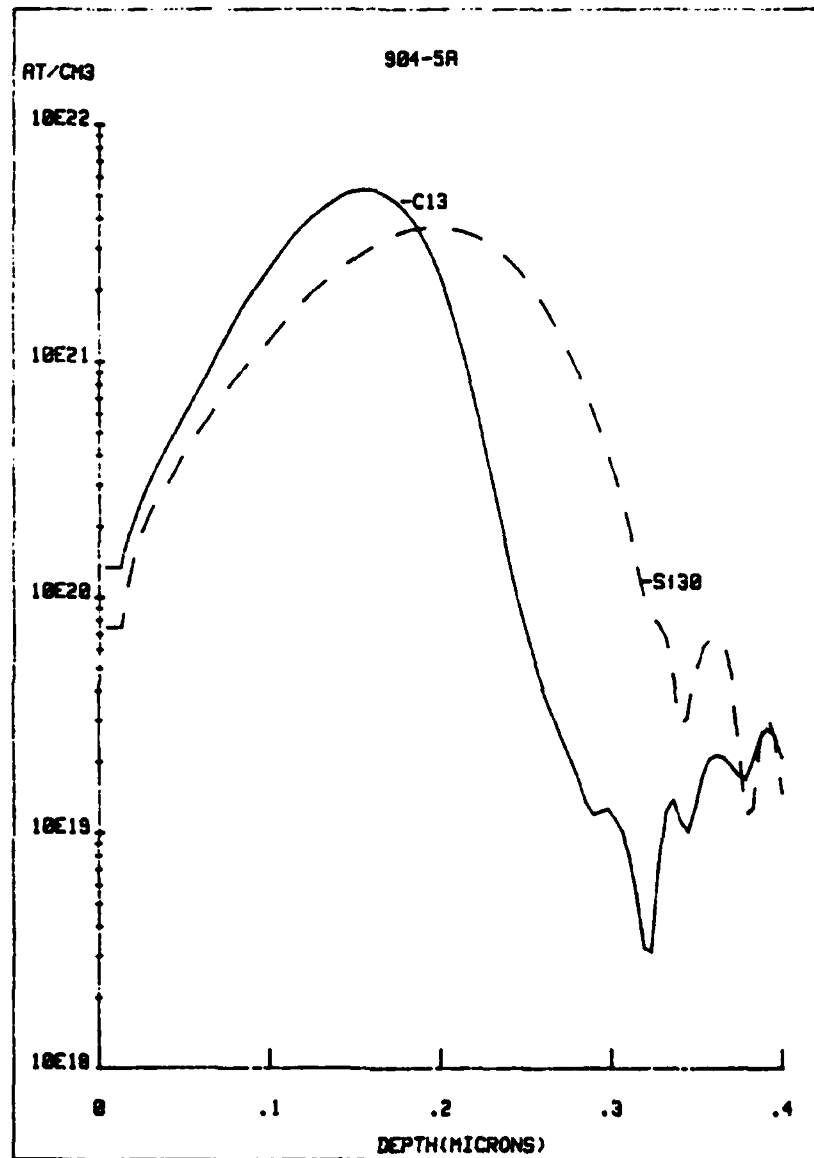


Figure 8a. SIMS profiles of $^{30}Si^{+}$ and $^{13}C^{+}$ implants (a) before correction of implant energy and straggle.

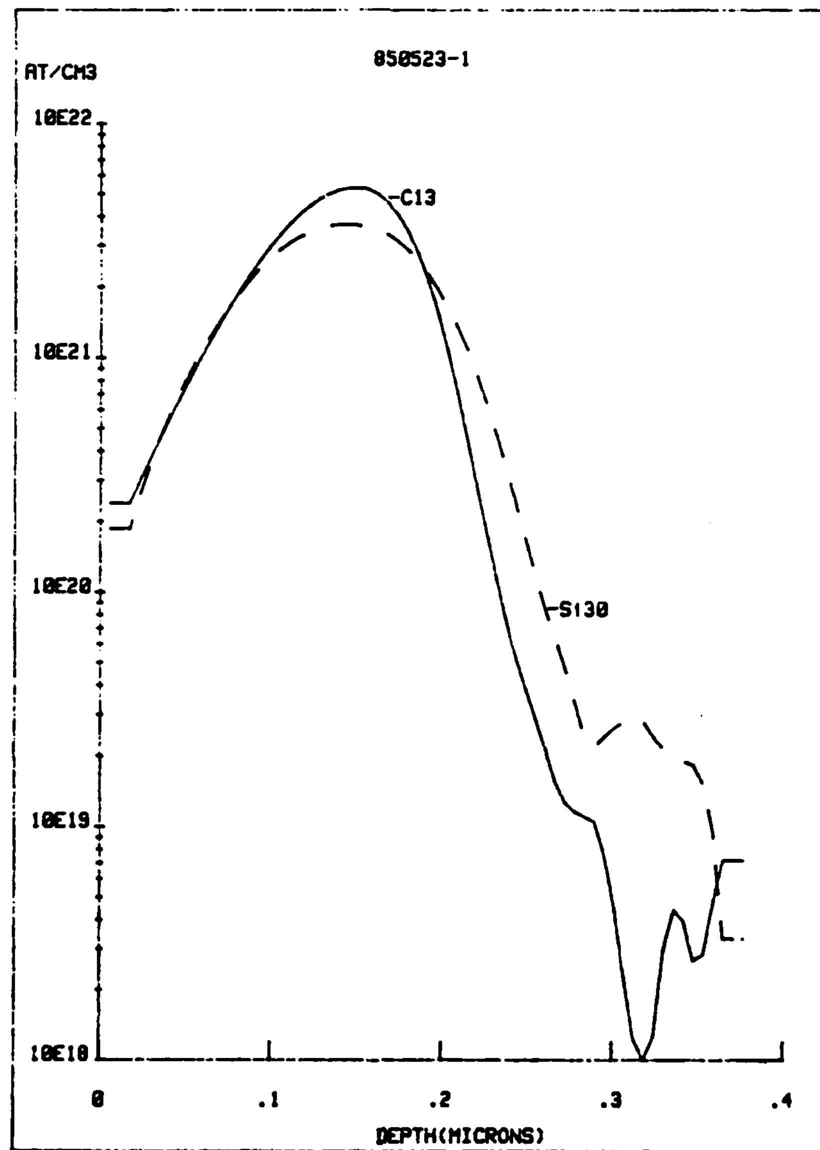


Figure 8b. SIMS profiles of $^{30}Si^{+}$ and $^{13}C^{+}$ implants after correction of implant energy and straggle.

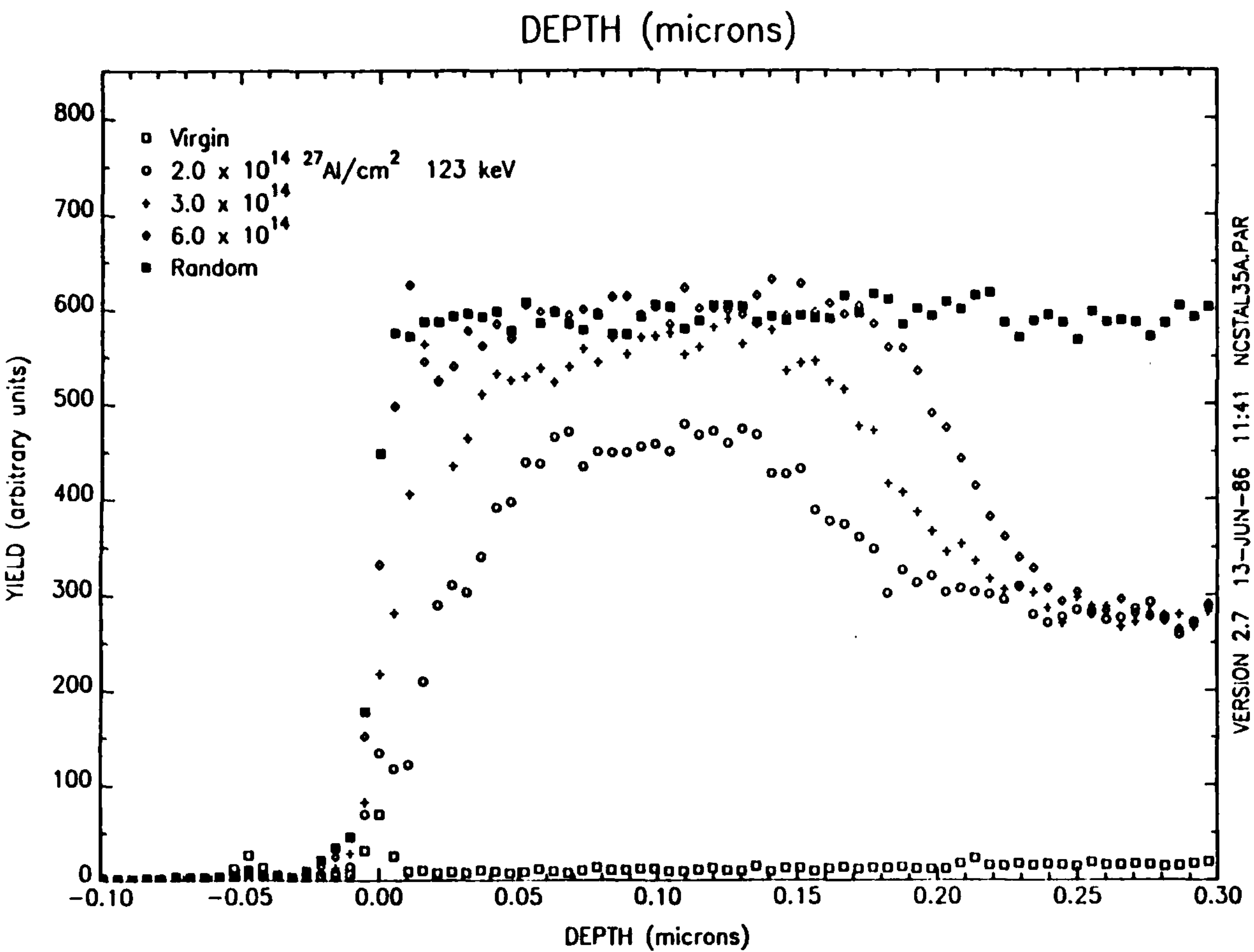


Figure 9. **RBS/channeling spectra showing the accumulation of damage with an increasing Al dose at LN temperaure in β-SiC along the <110> direction.**

Table II: $^{27}Al^+$ Implant Doses and Depths of the Corresponding Amorphous Layers

Sample #	Dose(cm^{-2})	Amorphous Layer Width (Å)*
851212-I	2.0×10^{14}	N/A
851212-J	2.25×10^{14}	N/A
851212-K	2.5×10^{14}	N/A
851212-E	3×10^{14}	830–1450
851212-F	4×10^{14}	450–1600
851212-G	6×10^{14}	300–1720
851212-H	10×10^{14}	0–1950

*Widths obtained from RBS were verified using TEM

higher doses, the amorphous layer widened until it included the surface. The random spectrum shown was obtained by rotating the sample around its normal axis during the RBS analysis to approximate the yield expected from amorphous SiC. Not all spectra taken are shown in this figure. Table II summarizes the implant doses used and the corresponding depths of the amorphous layers that resulted.

The critical energy required for the amorphization of β-SiC was estimated using damage depth profiles calculated using the TRIM84 computer code coupled with the results of the amorphous depths obtained using the RBS/ion channeling analyses. These damage-energy profiles are shown in Figure 10. As shown, the theoretical and experimental results are in approximate agreement. The resulting value for the critical energy density for amorphization of β-SiC at LN temperature is 8.0×10^{23} eV/cm^3, or 8.2 eV/atom.

Scattering yield data in excess of that obtained for random scattering was observed at a depth of 100–200Å for samples implanted with 4.6 and 10×10^{14} Al/cm^2, as shown in Figure 9. These unexpected results were seen for channeling along several axes. However, this phenomenon did not occur in rotating randoms. It is suggestive of greater than random scattering predicted for incidence along specific directions in a crystalline lattice[15]. High Resolution TEM micrographs are presently being obtained to determine the type of implantation induced structure responsible.

Solid phase epitaxial regrowth was achieved after annealing at 1973K for 300 s. Structural characterization of the recrystallized layers as a function of implant dose is being performed.

3.2 High Temperature Implantaton

Ion implantation has been utilized in order to introduce dopants into β-SiC thin films as an alternative to diffusion which requires extremely high temperatures and long times in

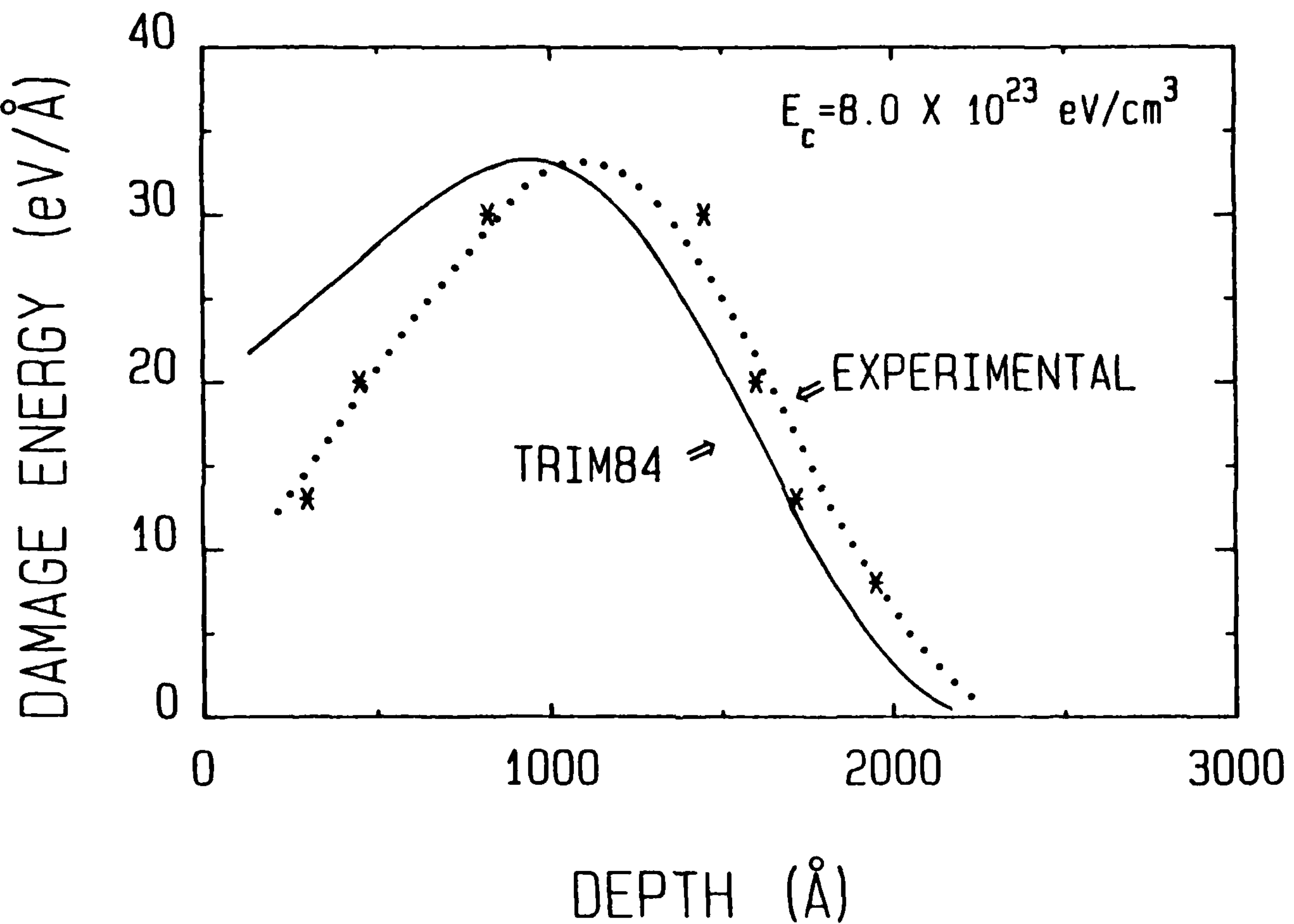


Figure 10. Comparison between theoretical (TRIM84) and experimental damage-energy profiles for 123 keV Al-implanted β-SiC at LN temperature.

this material. At the start of this endeavor, room temperature implants were conducted followed typically by a 2073K anneal cycle. This latter procedure was conducted in order to structurally heal the implant-induced damaged surface and near-surface region and to electrically activate the introduced dopant. This resulted in both recrystallization of the lattice but also the formation of residual defects. Furthermore, the percentages of ionized and activated dopants of $\approx$20% and 0.5% for P and Al, respectively, were attained from electrical measurements conducted on samples at room temperature. In an attempt to increase the percentage of activated dopant, the samples were held at liquid nitrogen temperature during implantation. It was discerned that both electrical and structural properties suffered as a result of this change. Therefore, a study of high temperature implantation was initiated. In this way structural annealing and activation of the dopant atoms can occur simultaneously during implantation.

Three different ions have been used in this study: aluminum and gallium as p-type dopants and nitrogen as an n-type species. Samples were held between 623K and 1053K during each implant. Table III summarizes the implantation conditions utilized for this work.

In order to structurally characterize the residual lattice damage caused by hot implantation, RBS/ion channeling techniques were again performed. Figures 11(a), (b) illustrate the damage accumulation as a function of implant temperature for N and Al implanted samples, respectively. In both cases, damage decreased with increasing implant temperature; the spectra for the higher two temperatures were nearly the same. Clearly, as-implanted, little residual damage occurred. This *in situ* annealing effect did not, however, result in complete electrical activation of the implanted species. In order to increase the percent of electrical activation, samples were annealed at 1473K for 1800 s following implantation. Differential capacitance-voltage, spreading resistance and sheet resistance measurements were made in order to electrically characterize these layers.

The electrical properties for each implanted sample are also given in Table III. A p-type signal in the C-V measurements was obtained for every Al-implanted sample. Electrical activation and ionization ranged between 0.1 and 0.5 percent as has previously been observed for annealed LN and room temperature implants for this dopant in β-SiC as noted above. For this reason, sheet resistance measurements for these samples yielded unmeasurably high resistances with the 4-point probe method. Spreading resistance data as a function of depth for sample 860512-3 is shown in Figure 12. The implant profile after annealing is also shown for comparison. The near-surface region of this sample showed an increasing resistance. This follows the inverse implant profile closely up to 0.3 μm. Between 0.3 and 0.5 μm an anomolous resistive layer was present. Presently, this is not explainable. The plot then dropped to the resistance value of the n-type substrate.

To study the hot implantation of N in β-SiC p-type substrates were utilized. Capacitance-voltage measurements taken on the implanted samples were inconclusive; the resulting carrier concentration appeared to be above the profiling range for the instrument. The sheet resistance decreased from a highly resistive p-type substrate to $\approx 1000\Omega/\square$. Furthermore, spreading resistance data, shown in Figure 13 for sample 841116-1, indicated that

Table III: Conditions for the high temperature implants of Al^+, N^+ and Ga^+

Sample No.	Starting type and carrier concentration(cm^3)	Starting sheet resistance (Ω/□)	Implant Species	Energy (keV)	Dose(cm^{-2})	Implant Temp.(K)	Resulting type and carrier concentration(cm^{-3})	Resulting sheet resistance (Ω/□)
851028-1	n=3E16	289	Al^+	130	3.9E14	1023	p 1E16	HR
851028-2	n=2E16	283	Al^+	185	1.8E14	1023	p 4E16	HR
851028-3	n=2.5E16	258	Al^+	160	2.3E14	1023	p 1E16	HR
851028-4	n=4E16	243	Al^+	100	4.8E14	1023	p 4E16	HR
860512-2	n=1.8E16	1117	Al^+	185	6.29E14	623	p 5E15	HR
860512-3	n=2E16	1206	Al^+	185	6.29E14	823	p 1E16	~4000
860512-4	n=1.8E16	1420	Al^+	185	6.29E14	1023	p 1E16	HR
860512-7	n=2E16	1277	Al^+	185	1.26E15	1023	p 6E16	HR
860513-6	n=2E16	935	Al^+,Al^{++}	150,300	4.34E14,6.81E14	1053	p 5E15	HR
860513-2	n=1.7E16	1024	Al^+	300	6.81E14	1023	p 5E16	HR
841116-4	p=9E17	HR	N^+	90,180	1.17E14,1.70E14	973	I	1041
841116-1	p=4E17	HR	N^+,N^{++}	180,360	1.7E14,2.2E14	993	I	935
841116-2	p=2E17	HR	N^+	90,180	9.36E13,1.36E14	623	?	?
841128-1	p=1E17	HR	N^+	90,180	9.36E13,1.36E14	823	?	?
841128-3	p=2E16	HR	N^+	90,180	9.36E13,1.36E14	1023	?	?
860508-1	n=1.8E16	1958	Ga^{++}	360	7.26E13	1013	I	1000
860508-2	n=3.3E16	1055	Ga^{++}	360	1.04E14	1023	I	792
860513-7	n=1.7E16	1113	Ga^{++}	360	3.11E14	1013	I	620
860508-3	n=1.5E16	3106	Ga^{++}	360	7.26E14	1013	I	1046
860512-5	n=2E16	1179	Ga^{++}	360	1.04E15	1043	I	HR

HR = highly resistive layer

I = inconclusive results

? = samples have not been measured

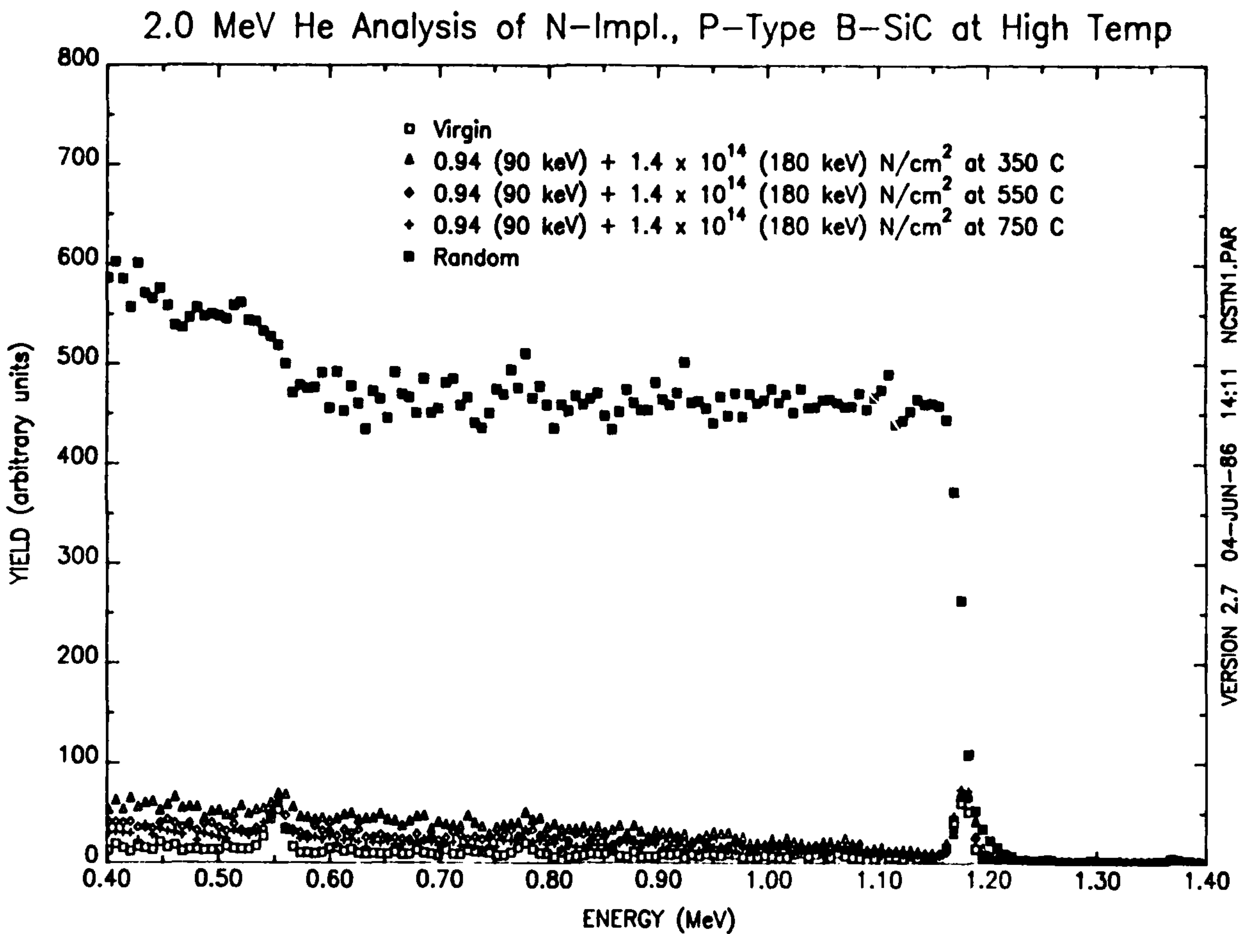


Figure 11a. RBS/channeling spectra showing the accumulation of damage with increasing sample temperature during Al implantation in β-SiC. The channel direction was ‹ 110 ›.

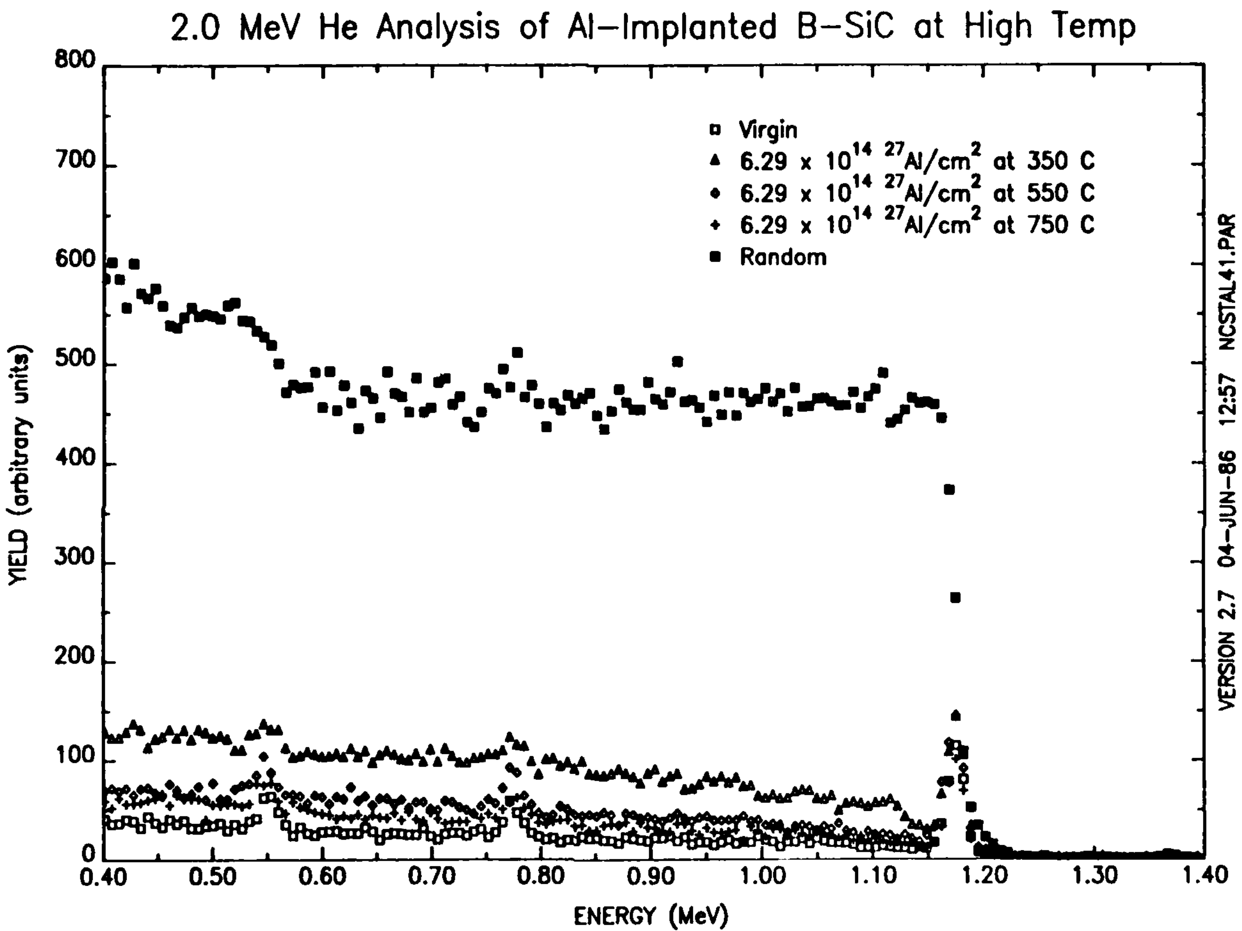


Figure 11b. RBS/channeling spectra showing the accumulation of damage with increasing sample temperature during N implantation in β-SiC. The channel direction was <110>.

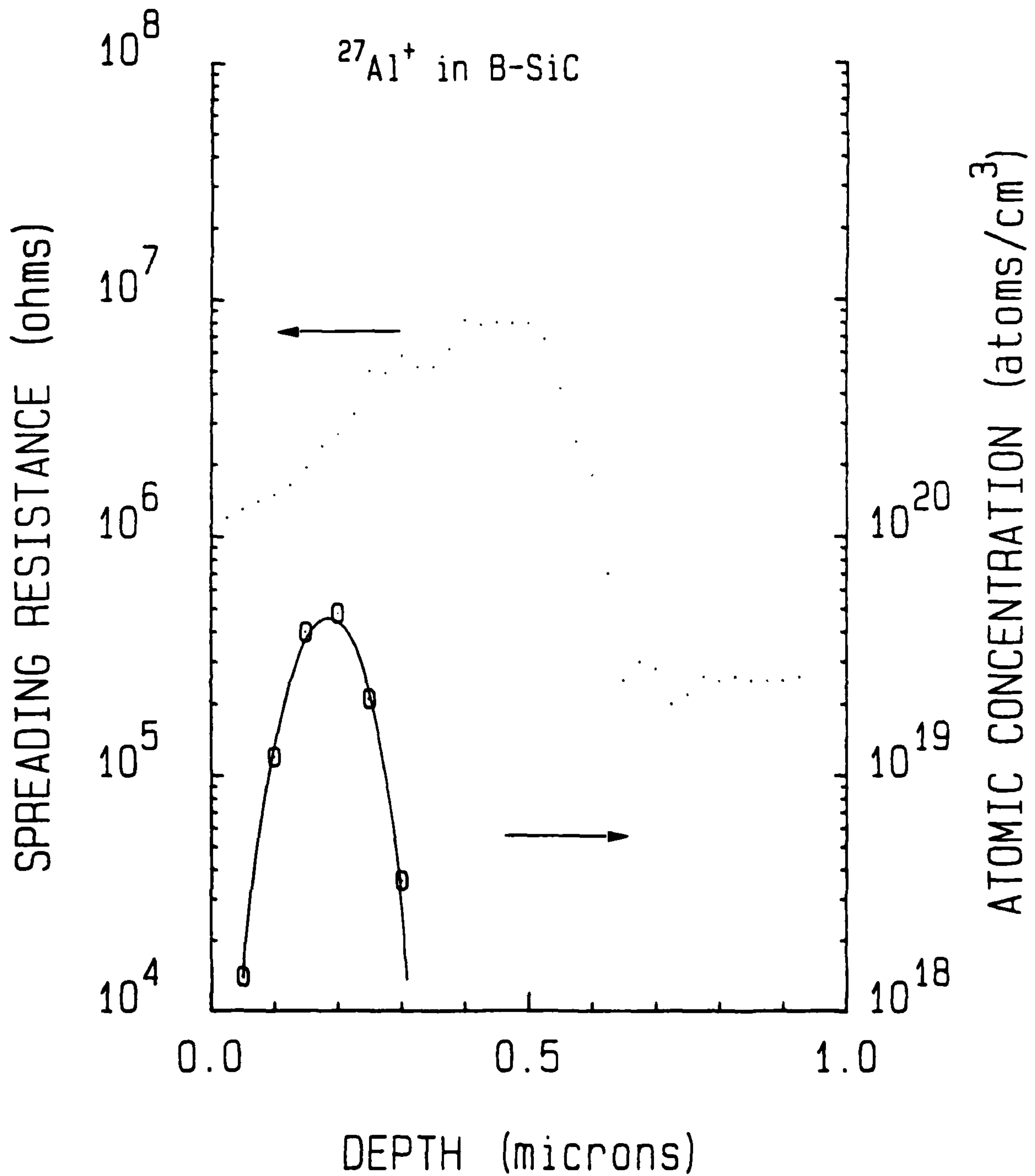


Figure 12. Spreading resistance depth profile for 185 keV Al implanted into β-SiC at 823K. The atomic concentration depth profile for the implant is shown for comparison.

there was indeed a low resistance surface with a profile shape closely mimicking the inverse implant profiles. The spreading resistance of the p-type background was ≈7E7, as shown between 0.9 and 1.2 μm in Figure 13.

Beta-SiC samples were also implanted with Ga at elevated temperatures. As was the case for N-implanted sample, C-V measurements were inconclusive in determining the type or the carrier density. It should be noted, however, that Ga, a trivalent ion, has been shown to be p-type in SiC[16]. Sheet resistance measurements also decreased significantly indicating dopant activation. The spreading resistance data for sample 860508-2 is shown in Figure 14. A low resistance surface, relative to that of the n-type background, was present in the implanted region. This is consistant with the sheet resistance data. However, these measurements do not indicate the carrier type in this low resistance surface region.

The investigators are presently preparing the aforenoted samples for the fabrication of new diode structures. Assuming Al and/or Ga are p-type dopants and N is n-type, p-n and n-p diodes, respectively, should result.

The important fact to note is that if diodes do result, a method to simultaneously implant, structurally anneal and electrically activate dopants in β-SiC has been developed. This is at a temperature below which requires removal of the Si substrate on which these films are grown.

4 Dry Etching

For fabrication of mesa structures for p-n junction measurements on SiC, further investigation of dry etching processes was performed. Previously, reactive ion etching (RIE) of SiC in CF_4, while having good etch rates, was found to leave a very rough, spiked surface. Also, Auger electron spectroscopy (AES) detected the presence of Fe on the etched surface, supposedly sputtered from the stainless steel electrode. Since the etched surfaces will have contacts deposited on them, a flat, uncontaminated surface is a necessity. Therefore, RIE in NF_3, NF_3+0_2, CF_4, and plasma etching in SF_6 were performed in a different laboratory to determine the effects of gas chemistry and electrode materials on the physical and chemical characteristics of the etched surfaces.

The spiked structure observed after RIE in CF_4 and noted above is believed to have been caused by the accidentally deposited Fe acting as a micromask. This micromask effect disallowed etching under the Fe particles. When the identical conditions were used in a different RIE chamber containing an anodized aluminum electrode, surface roughening was greatly reduced. There was, however, some roughness present, as shown in Figure 15. This roughness may be due to micromasking to a lesser degree, by Al from the electrode. The AES spectrum in Figure 16 shows the presence of Al peaks at 38 and 53 eV on the etched surface. More importantly, this spectra shows a very high C and F content, which is indicative of polymer formation. This is a common problem associated with dry etching

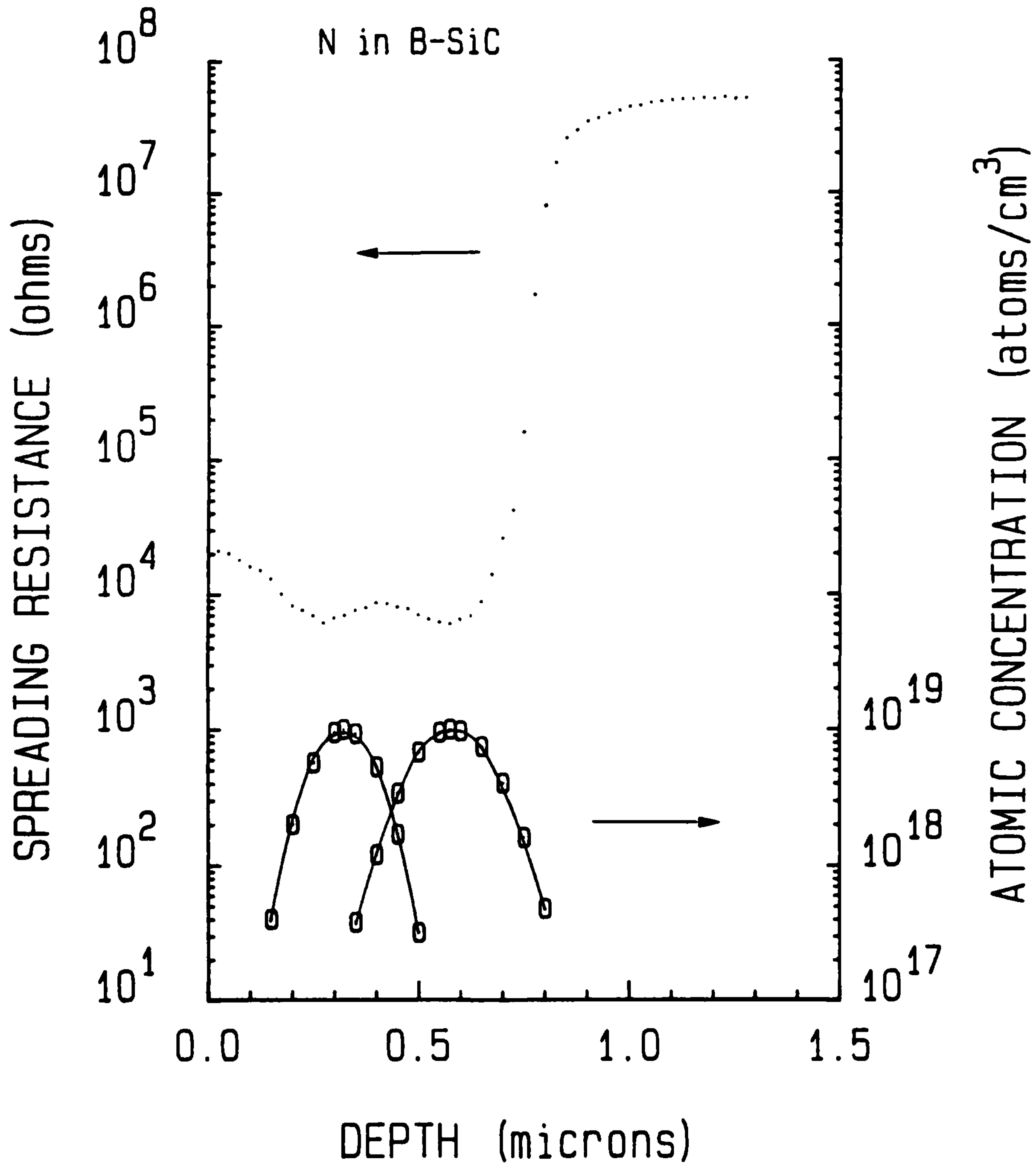


Figure 13. Spreading resistance depth profile for 180 and 360 keV N implanted into β-SiC at 973K. The atomic concentration depth profile for the implants are shown for comparison.

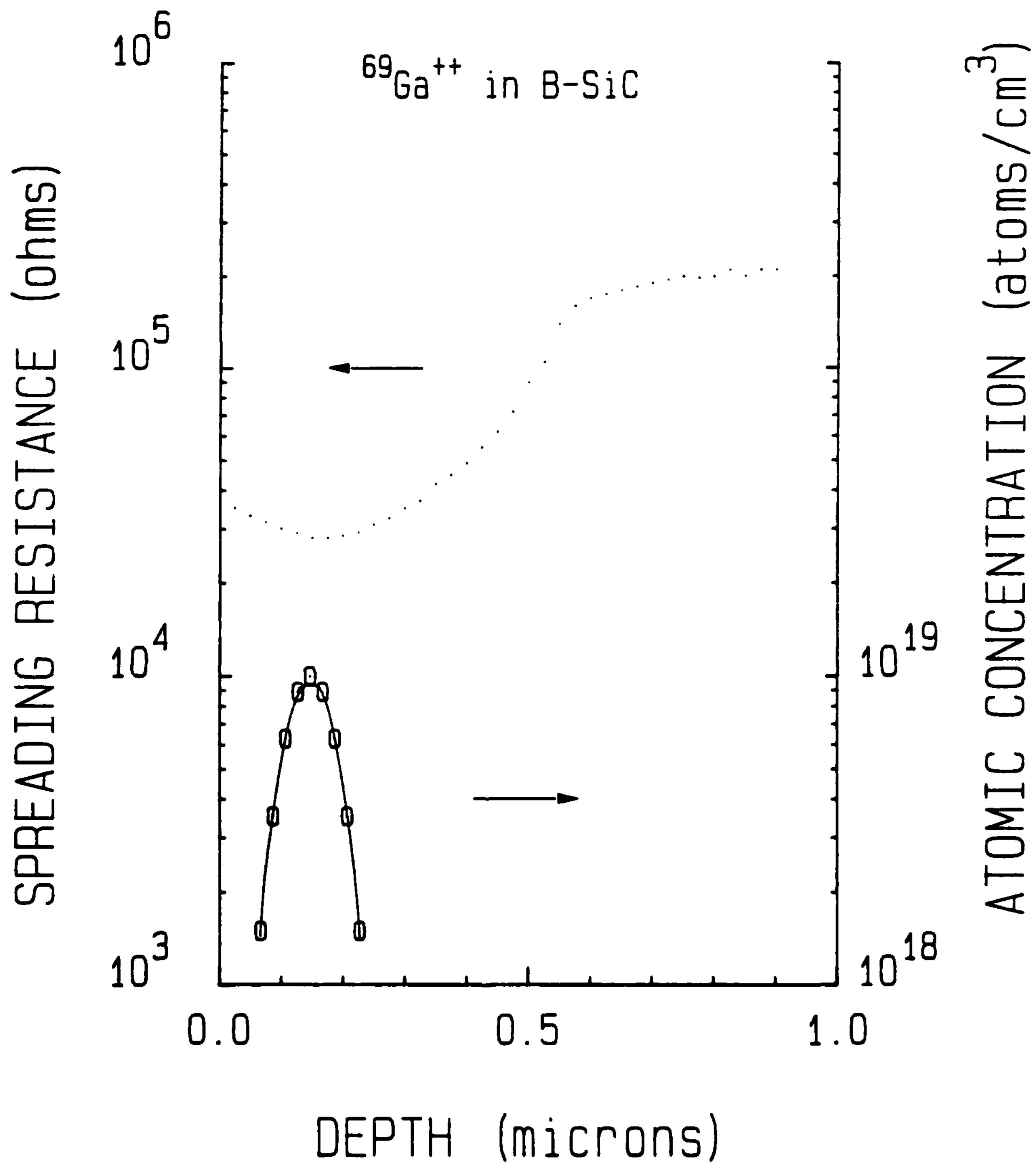


Figure 14. Spreading resistance depth profile for 360 keV Ga implanted into β-SiC at 1013K. The atomic concentration depth profile for this implant is shown for comparison.

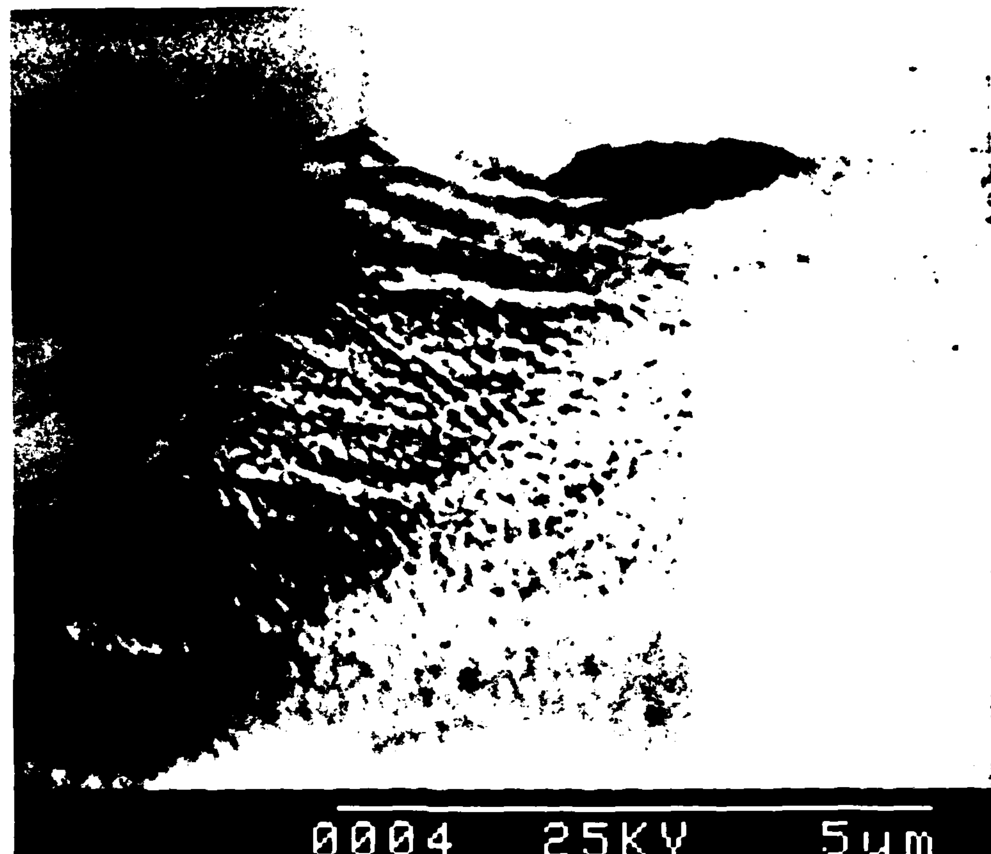


Figure 15. Etched step in SiC fabricated via RIE in 40 mTorr pure CF_4 at 125 watts RF power. (Etched surface on right).

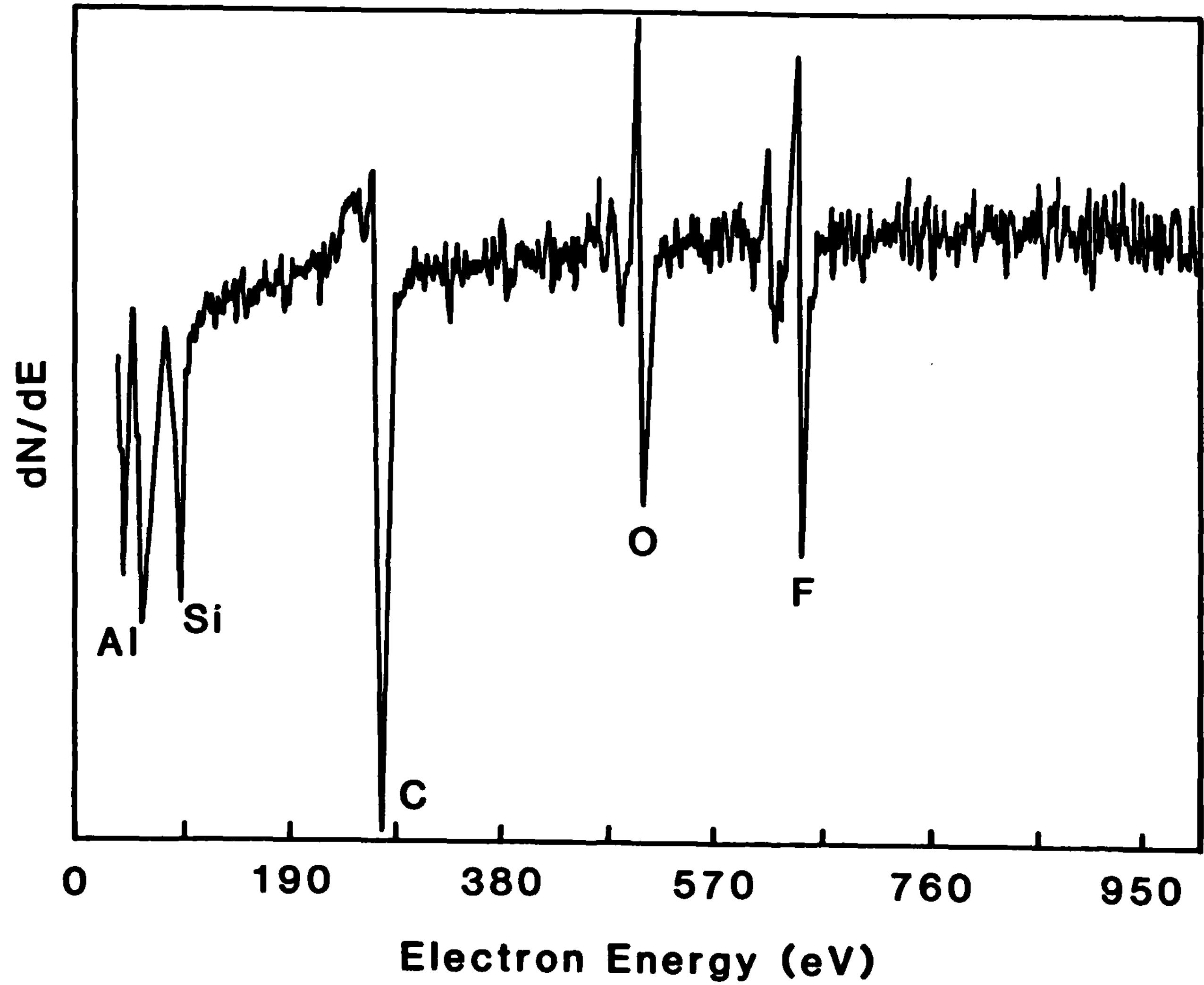


Figure 16. Auger spectrum obtained at 3kV and 5 mA for SiC surface reactive ion etched in 40 mTorr pure CF_4 at 125 W on an anodized Al electrode.

in pure CF_4, but was not detected in the previous SiC RIE experiments using this gas. It is possible that there was C-F polymer present on these previous samples, but the severe roughness only allowed Auger signals to be collected from the tops of the spikes. Also, the Fe peaks overlapped the position of the F peak at 649 eV.

Because of the problem of polymerization with CF_4, and the previous finding that the addition of O_2 does not affect etch rates, indicating that F is the chief reactant for both Si and C, other gases were investigated. The most desirable gas that was found was NF_3, because (1) it is more efficiently broken into free flourines, and (2) all of the possible by-products of ionization are gaseous.

Reactive ion etching in NF_3 and NF_3+0_2, using a carbon electrode, produced a very smooth surface, comparable to that of the unetched material. As shown in Figure 17, roughness appeared only on the step sidewalls, with some pitting near these walls. The smoothness of the etched surface was present despite etch rates as high as 2110Å/min., the highest etch rates ever reported for SiC.

The AES spectrum shown in Figure 18(a) is for a SiC surface that was reactive ion etched in pure NF_3. This spectrum is virutally identical to that of an unetched surface, showing the presence of a small amount of native oxide. The only difference is the presence of a very small N peak at 383 eV for the etched sample. When SiC is etched in $NF_3+70\%0_2$, the AES spectrum showed a more oxidized surface, indicated by the stronger O peak in Figure 18(b). Again, a hint of a N peak can be seen at 383 eV. No F peak was detected for either spectra in Figure 18! Since the electrode material was carbon, it would be difficult to determine if any of the C present was due to the electrode, but there was no significant increase of C signal as compared with an unetched sample. Further research will be conducted to determine whether the smooth surface is due to the carbon electrode or due to the gas phase chemistry.

As mentioned, the etch rates in NF_3 were very fast. Preliminary results of etch rates as a function of pressure and power were obtained. Etch rate versus pressure is shown in Figure 19. The etch rate reaches a maximum at around 30 mTorr and falls off, because of the drop in DC bias associated with higher pressures. A similar curve was observed for the case of RIE in CF_4. As power is increased, the etch rates increase sharply at first, as shown in Figure 20. However, at higher powers, the rate of increase falls indicating that the etch rate is not strictly dependent on ion energy, but also on F concentration. These etch rates for RIE in NF_3 are 5–10 times faster than any previously reported methods. Addition of 0_2 to NF_3 appeared to decrease the etch rates, but more experimentation is needed to confirm or deny this supposition.

Plasma etching of SiC was performed in SF_6 on an aluminum electrode resulting in good etch rates with no large spikes. However, there was roughening of the etched surface, as shown in Figure 21. While this surface is the roughest of the three methods discussed in this report, it is still acceptable for device fabrication. This process yielded the cleanest surface, evidenced by its AES spectrum in Figure 22. This spectra shows less native oxide

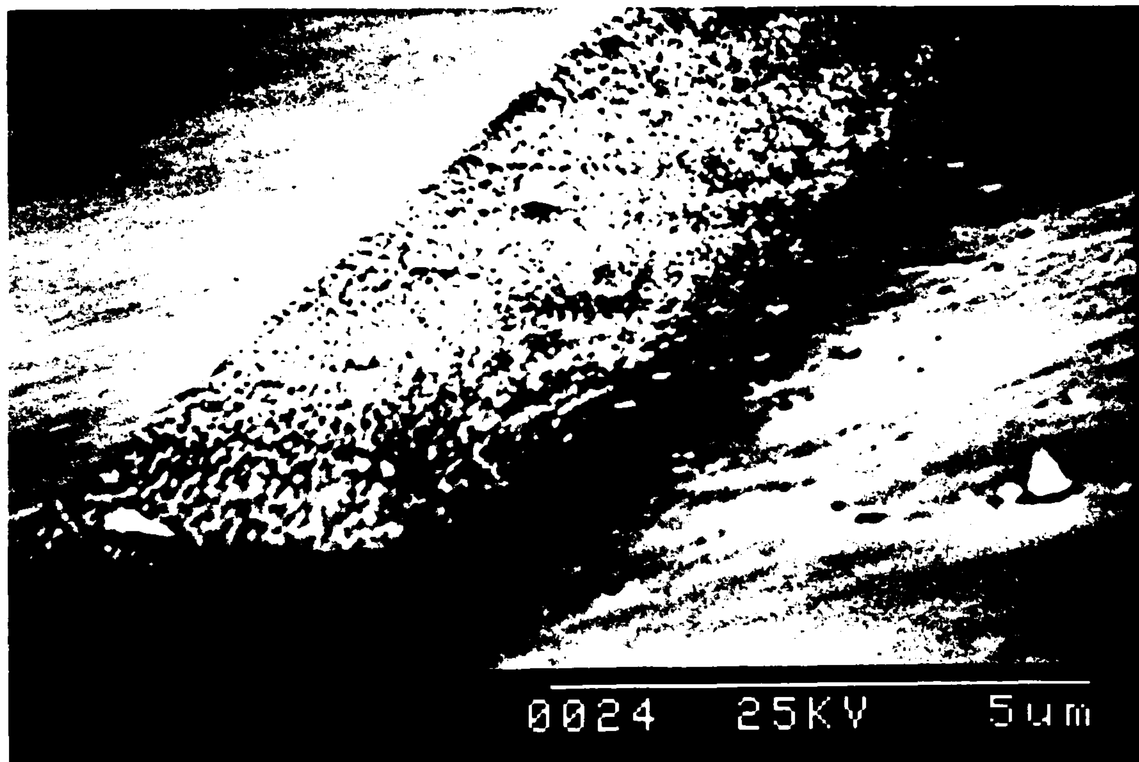


Figure 17. Etched step in SiC fabricated via RIE in NF_3/50% O_2 at 40 mTorr and 100 watts RF power. (Etched surface on right).

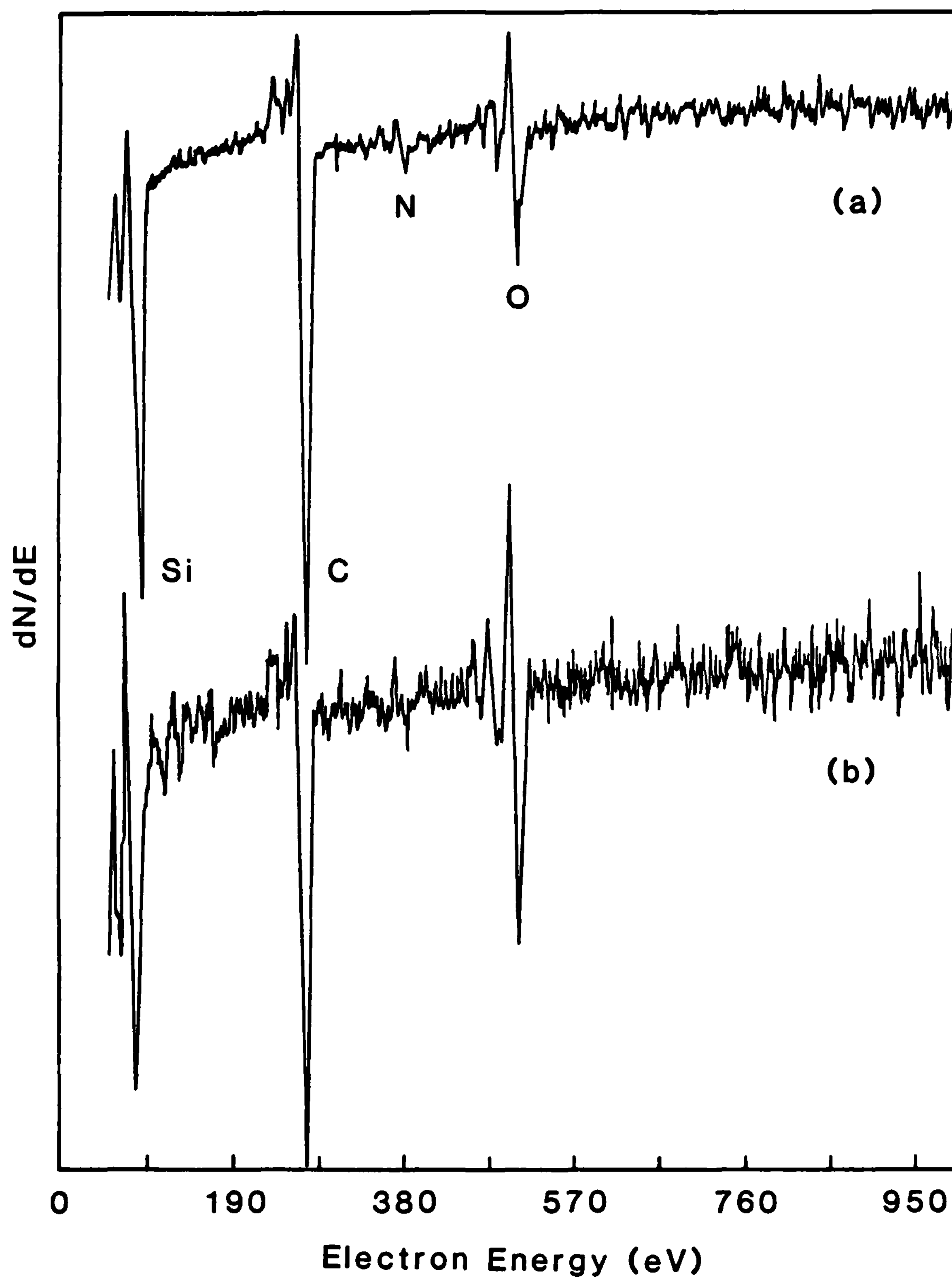


Figure 18. Auger spectra obtained at 3kV and 5 mA for (a) SiC surface after RIE in NF_3, and (b) SiC surface after RIE in NF_3/70% O_2. Both were etched at 40 mTorr and 100 W RF power.

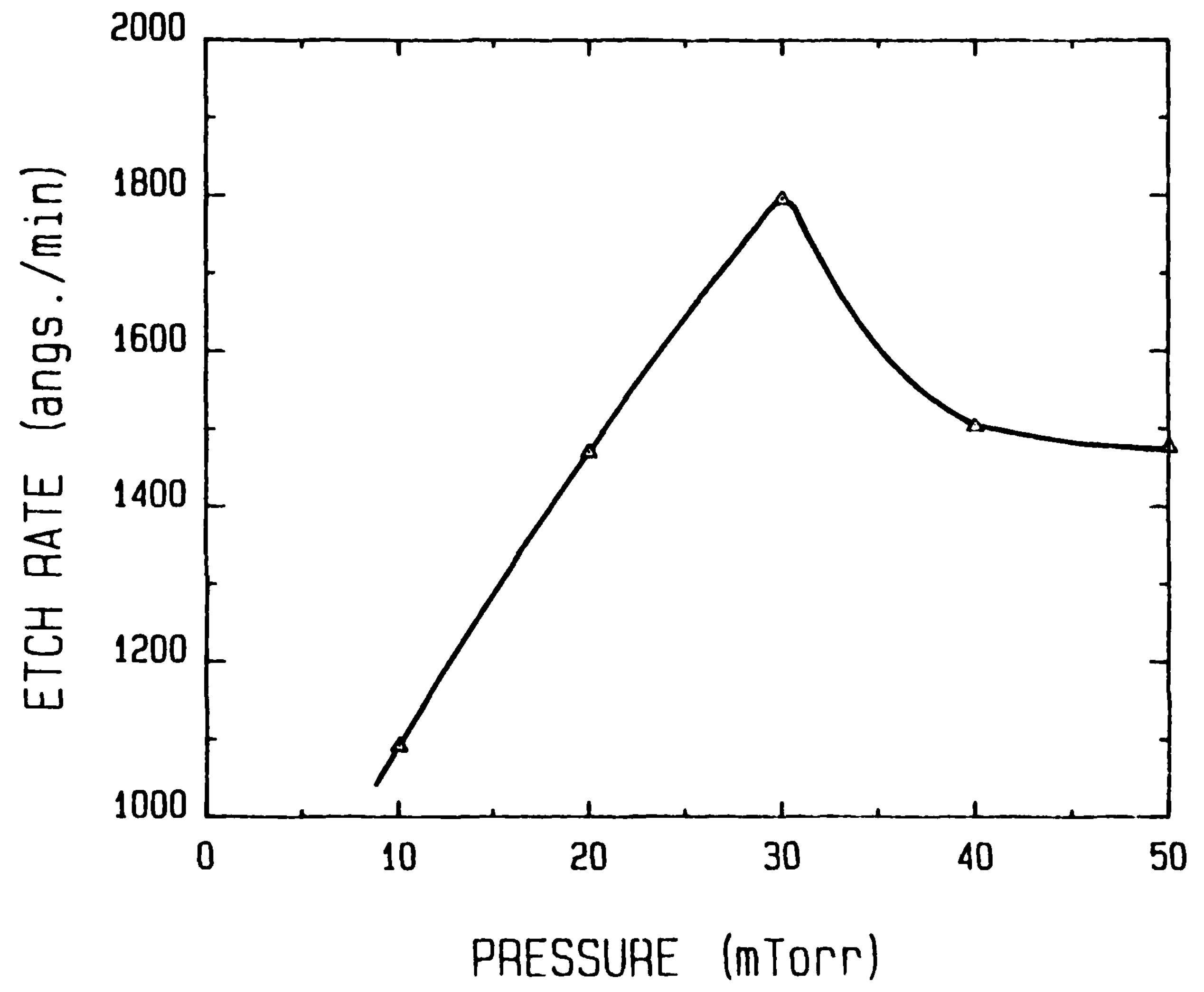


Figure 19. RIE rates vs. NF_3 pressure at 100 watts.

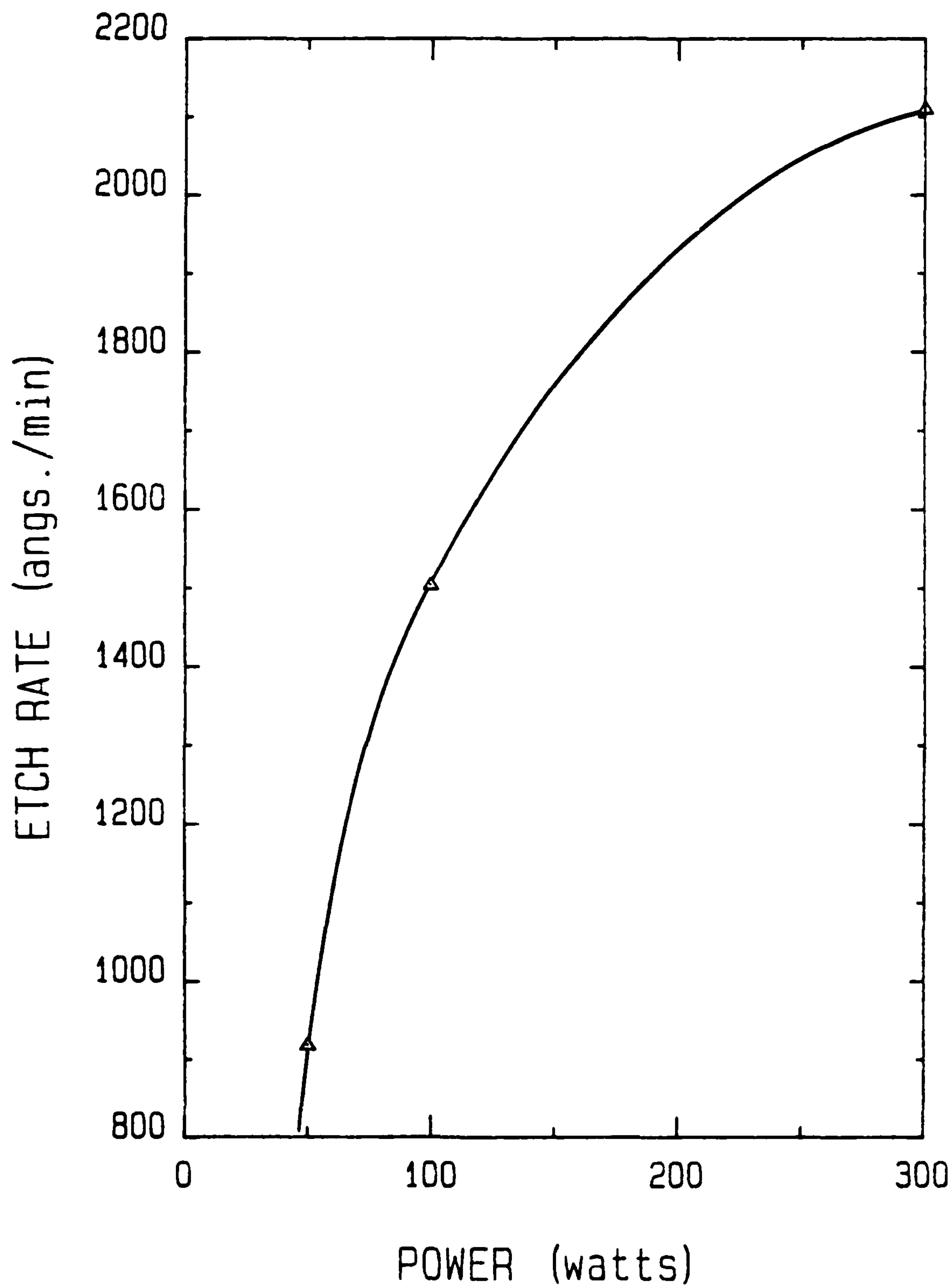


Figure 20. RIE rates vs. RF power in pure NF_3 at 40 mTorr.

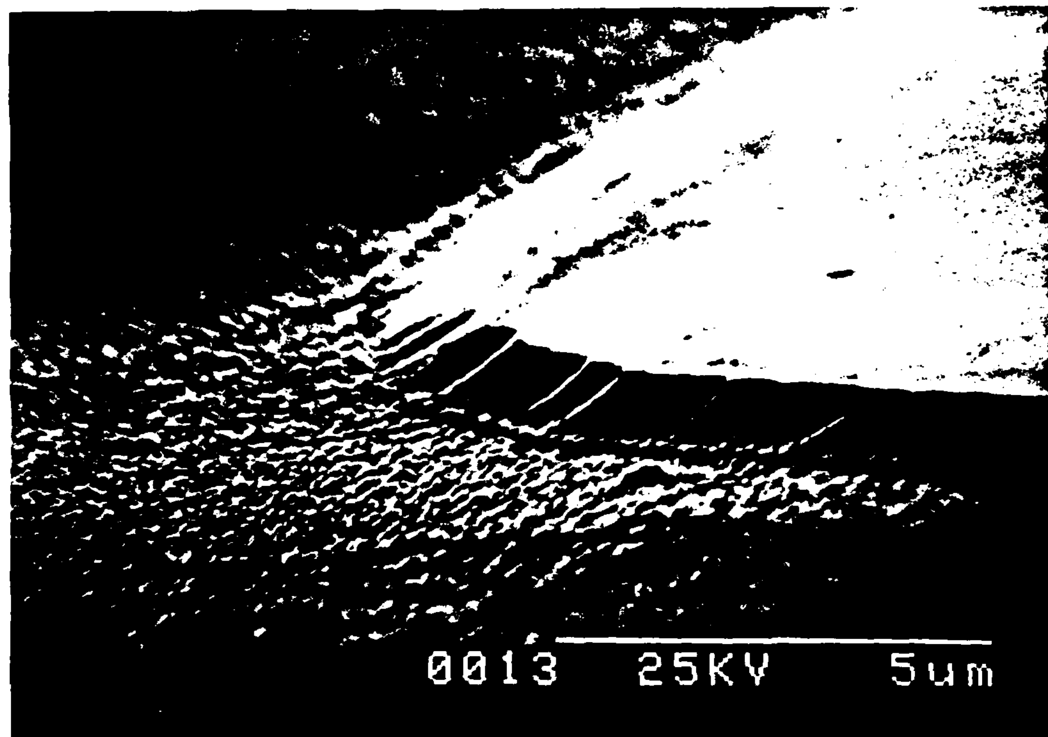


Figure 21. Etched step in SiC fabricated via plasma etching in SF_6 at 0.2 Torr and 275 watts RF power.

than that of an unetched sample, approaching the spectra of an Ar sputter cleaned sample. There is a possibility of a small S peak at 657 eV, but this cannot be positively determined. No traces of Al from the electrode were found as there is no DC bias in plasma etching that would cause sputtering of the electrode material. The reason for the smaller amount of O on the surface cannot be explained at present, but it is possible that a small amount of S is passivating the Si of the β-SiC.

Initial results of etch rates as a function of pressure, shown in Figure 23, for plasma etching in SF_6 indicated a maximum etch rate of 472Å/min. at 0.1 Torr and 200 W. The etch rates as a function of RF power are shown in Figure 24. Although there was a large amount of scatter in the points, probably due to experimental error, it is believed that the increase of etch rate with power is linear.

In summary, the spikes previously reported after RIE in CF_4 have been eliminated by changing electrode materials. However, a large amount of fluorocarbon polymerization is suspected. Very smooth, clean surfaces, along with very fast etch rates, were obtained via RIE in NF_3 with a carbon electrode. However, the small amount of N detected on the surface could act as a dopant, possibly causing device problems. Plasma etching in SF_6 left a very clean surface, having less native oxide than unetched SiC, but this process leaves a fairly rough surface.

5 Device Fabrication and Characterization

5.1 Metal Semiconductor Field Effect Transistor (MESFET)

MESFETs composed of Au rectifying contacts (gate) and $TaSi_2$ ohmic contacts (source and drain) were fabricated using unintentionally doped n-typed thin (2 μm thickness) beta-SiC films. The channel lengths were 10, 20 and 50 μm, and the channel width was 200 μm for all MESFETs. The resulting structure of the 50 μm width MESFET is shown in Figure 25.

The I-V characteristics between source and drain contacts (ohmic) and gate and drain contacts (rectifying) are shown in curves (a) and (b) respectively, in Figure 26. Although proper junction characteristics were obtained for each contact, the resulting MESFET did not function properly. The reasons for this are not clear, although several possibilities exists: (1) the channel depth (2 μm in this case) is too large to deplete the carriers from this region with an applied gate voltage less than the breakdown voltage, (2) improper isolation of the junctions allowed too much leakage current from the source to the drain, (3) contamination of the gate metal-SiC interface, and (4) effects of the defect structures at the SiC/Si interface region.

It is possible to evaluate the likelihood of this first speculation. The depletion width (which determines the effective cross-sectional area of a conducting channel) of the Schottky diode

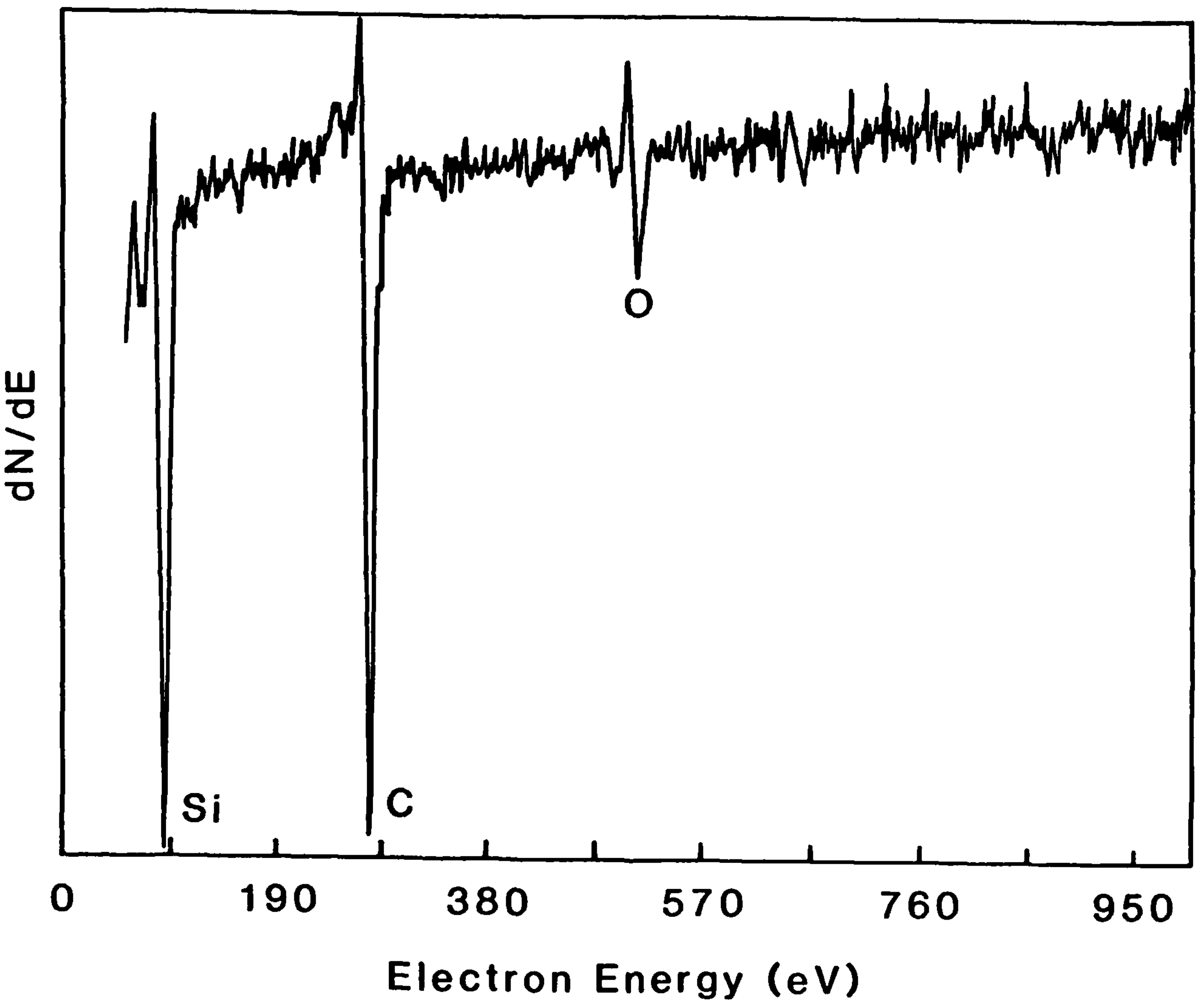


Figure 22. Auger spectrum obtained at 3 kV and 5 mA for SiC surface plasma etched in 0.2 Torr at 200 watts RF power.

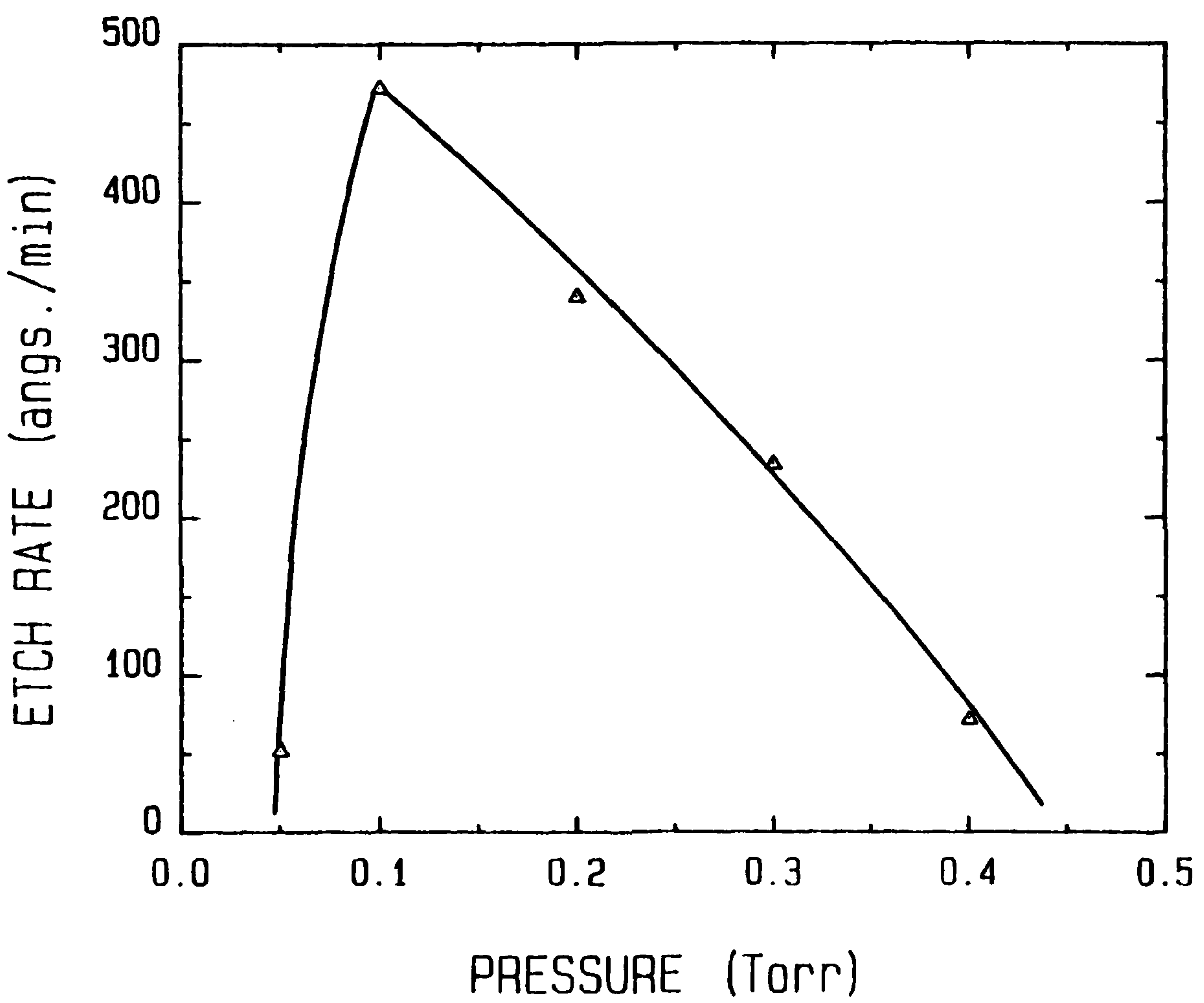


Figure 23. Plasma etching rates vs. SF_6 pressure at 200 watts.

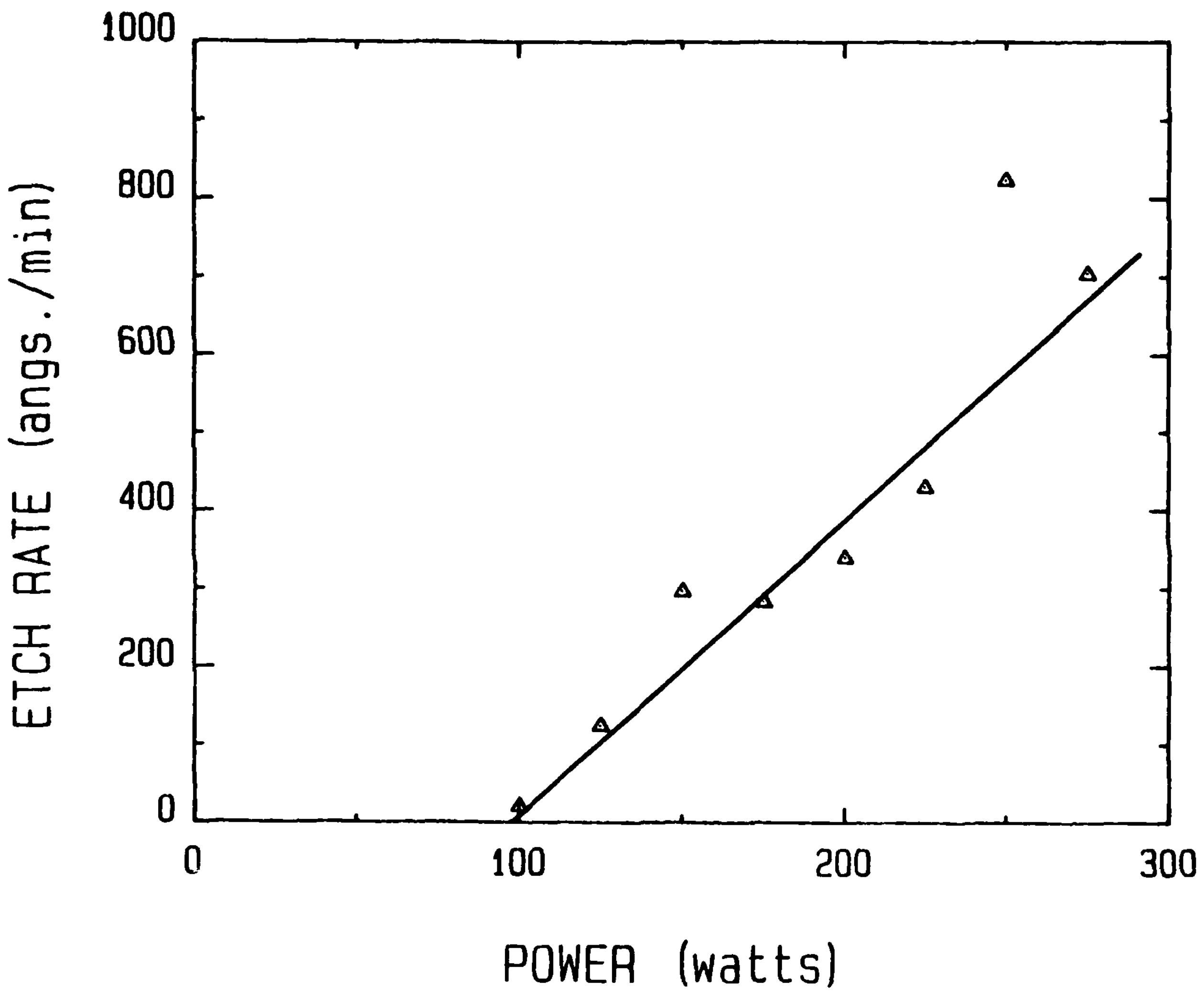


Figure 24. Plasma etching rates vs. RF power in pure SF_6 at 0.2 Torr.

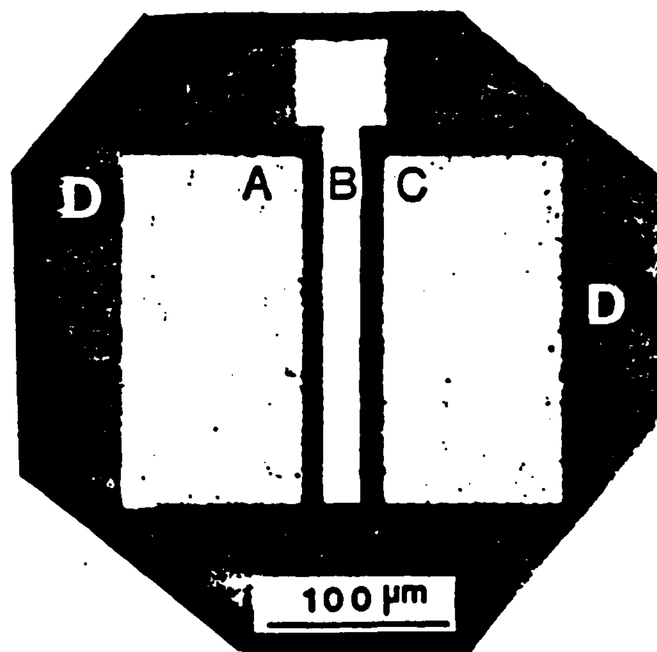


Figure 25. Fifty micron channel-length device pattern for MESFET fabrication. A and C are $TaSi_2$ ohmic contacts for the source and drain, B is a Au rectifying contact for the gate, and D is an oxide layer for passivation.

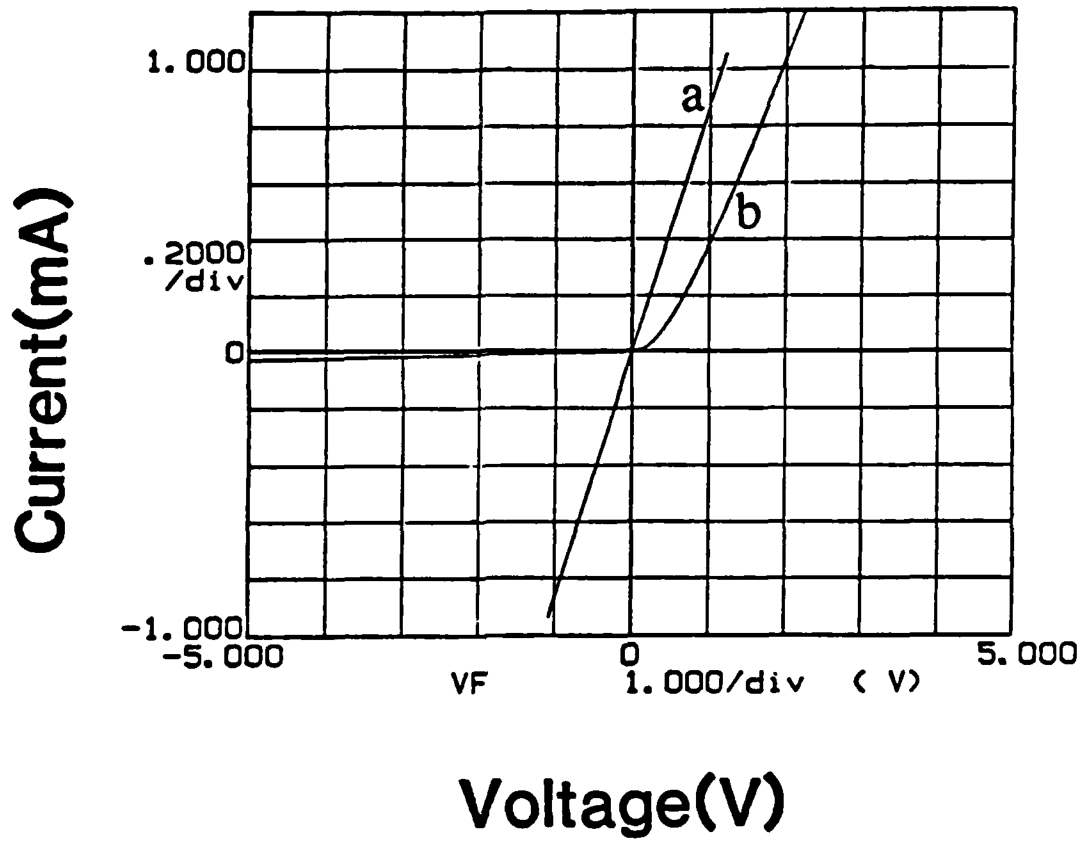


Figure 26. I-V characteristics of the fabricated MESFET: (a) ohmic contact property between source and drain and (b) rectifying character between gate and drain.

is expressed as [17]

$$W = [2\epsilon_s/q\; n\; x\; (V_{bi} - V - kT/q)] \quad (1)$$

where W is depletion width, ϵ_s is the dielectric constant of the SiC under investigation, n is the carrier concentration, V_{bi} is the barrier height, V is the applied voltage, and kT is the thermal energy. The value of ϵ_s for SiC is 9.7 [18], V_{bi} for Au/SiC is 1.1 eV, kT is 0.025V at room temperature, and the carrier concentration of this sample was $5\times10^{16}cm^{-3}$. Therefore, the depletion widths at -5, -10, -20 volts are only 0.36, 0.49 and 0.67 μm, respectively. Thus, it is reasonable to speculate that the cross-sectional area of the channel region could not be effectively controlled with the gate bias voltage up to -20 volts.

The aforementioned second possible cause of the poor MESFET performance is difficult to quantitatively evaluate. However, it can be avoided by utilizing a concentric ring or an enclosed rectangle geometry for the MESFET [19]. Therefore, a new mask set employing these geometries has been designed and is shown in Figure 27. Gate lengths are 50, 20, 10, 5 and 3.5 μm. These designs have been digitized onto a Calma computer system and will be ready for mask fabrication in the near future.

The third cause relates to the performance of the Schottky contacts. If care is taken in the MESFET fabrication, the rectifying characteristic of this Au-beta-SiC junction should be sufficient. However, the additional steps in the MESFET fabrication, as opposed to producing a single Schottky contact, may add contaminants which degrade the junction properties. In the present investigation, this is believed to be a minor problem compared to the other possibilities.

The fourth and final potential problem with the MESFET involves interfacial defects. These defects were revealed in Figure 6 in Section II of this report. As noted, the density of these defects was observed to be very high near the SiC/Si interface. These defects may affect the MESFET performance since they are located in the thin active channel region. Interference from these defects can be avoided by utilizing a lightly doped p-type buried layer rather than the Si substrate as the insulator for the n-type channel region. A thin n-type layer can then be grown on top of this p layer and utilized as the channel for the MESFET. This structure has recently been grown in the present CVD apparatus and is presently being electronically characterized.

In summary, the first attempt at MESFET fabrication has been completed but was not successful. The cause of the problems, however, are not believed to be material related but rather related to the structure of the device and the high defect density at the Si/SiC interface. Two unique ideas have been employed to resolve these problems, and the fabrication of a second generation of MESFETS will be completed in the near future.

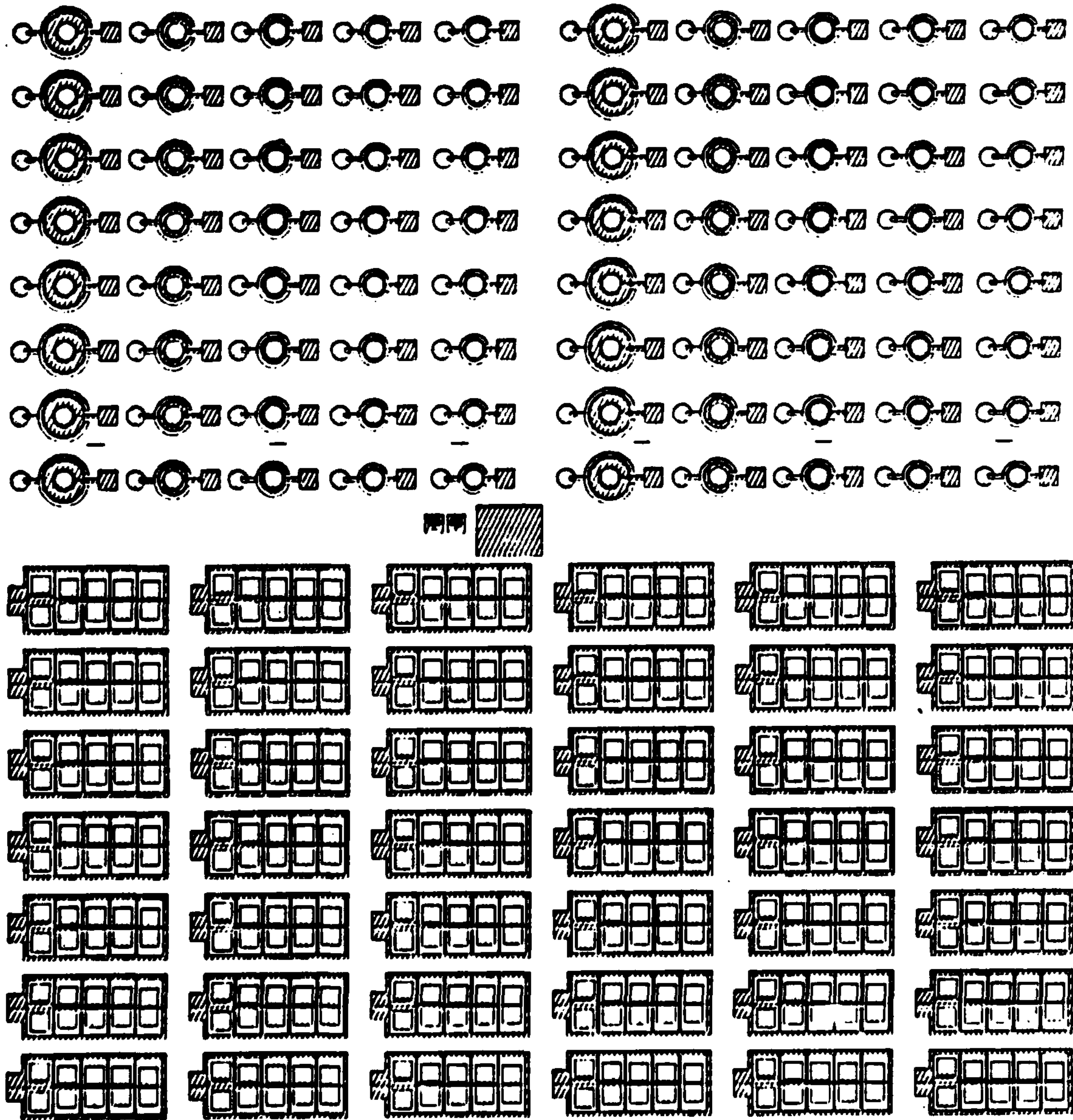


Figure 27. New mask pattern for MESFET fabrication. Pattern has been digitized onto Calma computer system in preparation for fabrication of mask set.

5.2 Metal-Oxide-Semiconductor (MOS) Structures

For the fabrication of a MOSFET, it is very important to first characterize and optimize the electrical behavior at the oxide-SiC interface. The best way to do this is to study the more basic MOS capacitor structure. Therefore, MOS structures were fabricated and characterized using capacitance-voltage (C-V) techniques.

Two methods were employed to form the MOS capacitors. The first involved growing the oxide, masking approximately two-thirds of its area and etching away the unmasked oxide with HF acid. $TaSi_2$ was subsequently sputtered onto the bare SiC to make an ohmic contact to this n-type sample. The oxide was then unmasked and Cr dots ($10^{-3}cm^2$) were evaporated onto the oxide as the gate metal. This process produces an MOS structure using topside contacts and allows the SiC thin film to remain on the Si substrate.

The other method employed involved making a backside ohmic contact. The samples were again oxidized, and the Cr dots evaporated onto the surface for gate metal contacts. The sample top surface was then embedded in wax, and the Si substrate removed by etching in a 1:1 mixture of HF and HNO_3. The wax was removed from the film using TCE. Thus the remaining structure consisted of a thin SiC film having $Si0_2$ with Cr dots only on the topside of the film. The backside of the film was then sputter coated with $TaSi_2$ to form the ohmic contact.

The samples fabricated by the former method yielded good C-V curves on a PAR 410 C-V plotter operating at a frequency of 1 MHz. However, subsequent measurements on an MDC CSM 16, which performs a leakage test showed these same devices to possess a moderate leakage current. The samples fabricated by the latter method had no leakage current, but yielded very unusual C-V curves. It is believed that since the thin films do not sit perfectly flat on the contact plate, much of the capacitance measured results from air between the sample and the contact plate. Efforts are underway to eliminate this problem. Therefore, the best results to date have been obtained using the topside contact configuration and the PAR C-V plotter.

MOS structures (with topside contacts) measured on the PAR 410 C-V plotter were fabricated with oxides grown on the β-SiC in dry O_2 at 1273K, 1473K, and at 1473K with an Ar anneal at 1473K for 3600 s. The sample grown at 1273K had a very poor C-V curve, but the three samples grown at 1473K displayed typical MOS C-V curves. The best C-V curve was obtained for a 945Å thick oxide film grown at 1473K followed by the Ar anneal. The results of this measurement are in Figure 28.

The C-V characteristics of the aforenoted samples grown at 1473K were determined using the following steps. The data from these measurements is given in Table IV.

1. The C-V data may be considered valid if the C-V curve has the typical flat maximum capacitance in the accumulation region. (See Figure 28) This value denotes the

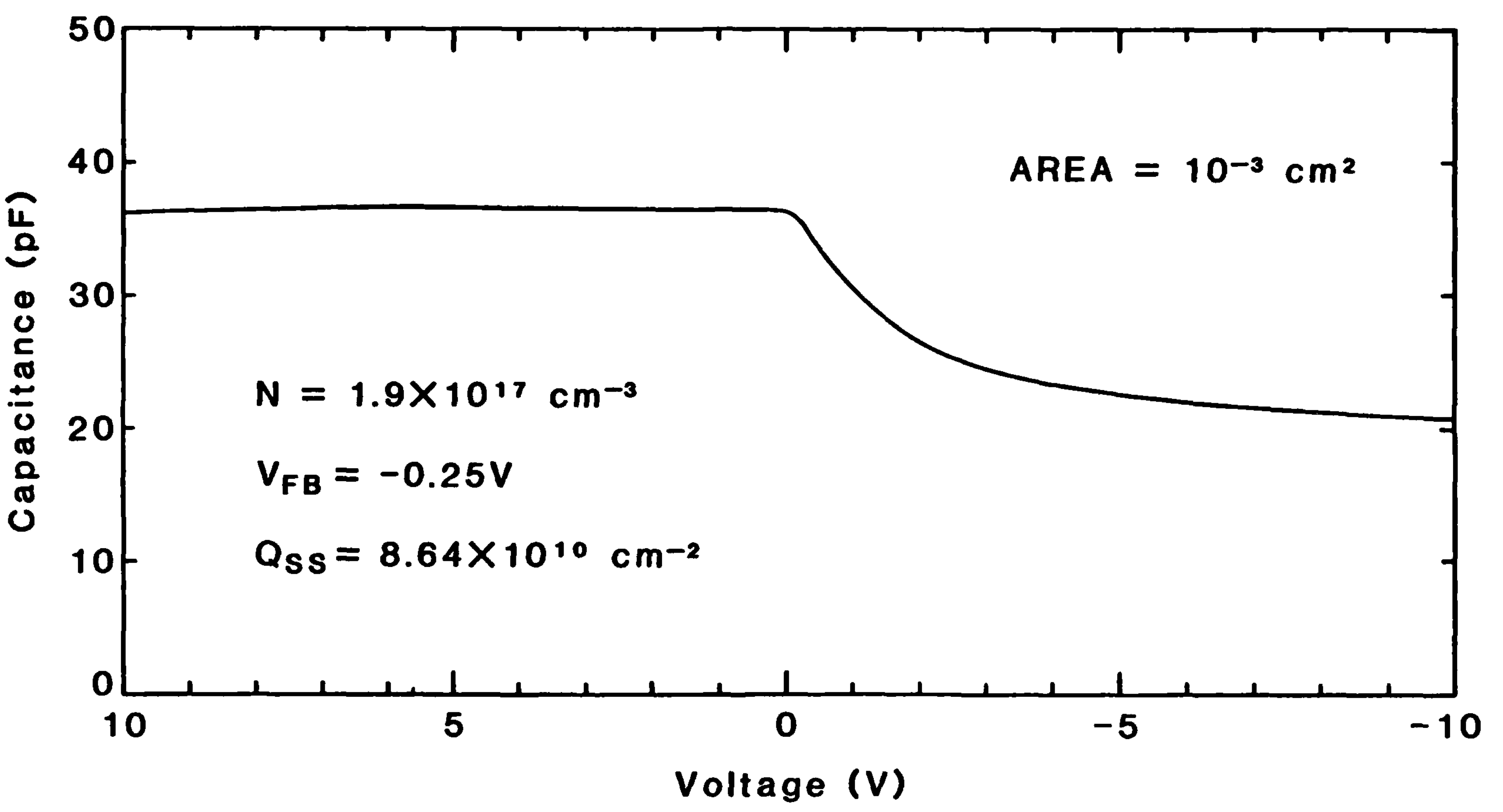


Figure 28. C-V characteristics of an MOS structure on β-SiC. Oxide was grown in dry 0_2 at 1473K, followed by a 3600 s. Ar anneal at 1473K. Oxide thickness was 945 Å. Voltage sweep rate was 20 mV/sec.

Table IV: Data obtained from C-V measurement of MOS structures

Sample #	d_{ox}(Å)	C_{ox}(pF)††	C_{min}(pF)	C_{min}/C_{ox}	W_{DR}(Å)	n($\times 10^{17} cm^{-3}$)	$C_{MEAS(FB)}$(pF)	V_{FB}(V)	Q_{ss}($\times 10^{10} cm^{-2}$)
*850220#1	1042	37.1	23.5	.633	1414	1.86	35.9	+0.55	8.76
*851011#5	894	38.6	25.5	.661	991	5.69	37.8	-0.24	9.55
†851011#5	945	36.5	20.8	.570	1775	1.93	35.2	-0.25	8.64

*Oxidized at 1473K in dry O_2.

†Oxidized at 1473K in dry O_2 and annealed in Ar at 1473K.

††The reason that C_{ox} does not uniformly decrease as d_{ox} increases is that 850220#1 had a slightly larger contact size ($1.12 \times 10^{-3} cm^2$) than the others had ($10^{-3} cm^2$) due to using different masks.

oxide capacitance, C_{ox}. The value of a given oxide thickness, d_{ox}, was checked using equation (2) against values obtained directly in profilometry measurements.

$$d_{ox} = \frac{\epsilon_{ox} A}{C_{ox}} \tag{2}$$

In this equation, ϵ_{ox} = dielectric const. = 3.45×10^{-13} fd/cm for SiO_2 and A=area of the metal contact = 10^{-3}cm^2.

The value of the oxide thickness was usually comparable to that obtained by profilometry. Occasionally, however, the Cr contacts would chip off when probe contact was made, reducing the contact area, thus giving a false d_{ox} value. Also, the breakdown voltage was occasionally exceeded and pinhole conduction would occur.

2. The high frequency minimum MOS capacitance, C_{min}, was measured in the inversion region. Thus, the min/max ratio, or C_{min}/C_{ox} was determined. This minimum value corresponds to having two capacitors in series, the oxide capacitance and the capacitance from the depletion region in the SiC. Thus, the capacitance of the SiC depletion region anywhere on the curve was:

$$C_{SiC} = \frac{C_{ox} C_{meas}}{C_{ox} - C_{meas}} \tag{3}$$

and the width of the depletion region, W_{DR}, in the SiC was:

$$W_{DR} = A\epsilon_{SiC} \left(\frac{1}{C_{meas}} - \frac{1}{C_{ox}} \right) \tag{4}$$

Of course $C_{SiC} = 0$ in accumulation because C_{meas}=C_{ox}.

3. By computing C_{SiC} as the curve falls off from accumulation, through depletion, and into inversion using eq.(3), then one could plot $1/C^2_{SiC}(F^{-2})$ vs. V(volts). The maximum slope of this curve is $d(1/C^2)/dV$. With this value, the ionized doping density of the SiC surface region, n, could be computed as follows:

$$n = \frac{2}{A^2 q \epsilon_s} \left[\frac{1}{d(1/C^2)/dV} \right] \tag{5}$$

4. With this value of n, the flat band capacitance, C_{FB}, was calculated. This is the capacitance of the depletion region at the point where the work function difference between SiC and metal is compensated, and the valence and conduction bands are flat.

$$C_{SiC(FB)} = \sqrt{\frac{q^2 \epsilon_s n}{kT}} \tag{6}$$

Since this value is the capacitance of the depletion region, the measured capacitance corresponding to this value must be determined. Rearranging eq. (3):

$$C_{meas} = \frac{C_{ox} C_{SiC}}{C_{ox} + C_{SiC(FB)}} \tag{7}$$

The flat-band voltage, V_{FB}, was obtained by finding the point on the measured MOS C-V curve that corresponded to $C_{meas(FB)}$ and reading off the voltage at which this occurs.

5. In order to calculate the surface state density, one must first know the work function difference, ϕ_{ms}, at zero applied bias:

$$\phi_{ms} \equiv \phi_m - \left(X + \frac{E_g}{2q} - \psi_B\right) \quad for\ n - type \tag{8}$$

$$\phi_{ms} \equiv \phi_m - \left(X + \frac{E_g}{2q} + \psi_B\right) \quad for\ p - type \tag{9}$$

where ϕ_m is the metal work function (ϕ_m = 4.5 eV for Cr), X the semiconductor electron affinity (X = 4.3 eV for β-SiC), E_g the gandgap (E_g = 2.2 eV for β-SiC at 297K), and ψ_B the potential difference between the Fermi level E_f and the intrinsic Fermi level, E_i. The difference between E_f and E_i changes with carrier concentration. To determine the position of E_f, the following was used:

$$E_c - E_f = -kTln\frac{n}{N_c} \quad for\ n - type \tag{10}$$

$$E_f - E_c = -kTln\frac{p}{N_v} \quad for\ p - type \tag{11}$$

where $N_c(3.1\times10^{24}m^{-3})$ and $N_v(2.48\times10^{25}m^{-3})$ are the calculated density of states at room temperature.

Given ϕ_{ms} and V_{FB}, the fixed oxide charge density, Q_{ss}, was then calculated as follows:

$$Q_{ss} = \frac{C_{ox}}{q}(V_{FB} - \phi_{ms}) \tag{12}$$

For all the MOS structures fabricated at 1473K, the oxide thickness measured by profilometry was very close to the thickness calculated from the C-V curves. The calculated carrier concentrations, however, were always 1 to 1.5 orders of magnitude higher than those measured using the differential C-V Miller profiler. It is possible that the leakage current associated with this MOS configuration caused this anomaly.

Leakage current causes the slope of the depletion curve to change, as well as causing C_{ox} to decrease as the accumulation voltage is increased. This latter phenomenon can be seen in Figure 28. Using the carrier concentrations obtained from the MOS curves, the flat band voltages that were calculated were typically in the range of -0.24 to -0.55V. The fixed oxide charge densities, Q_{ss}, were determined to range from $8.6\times10^{10}cm^{-2}$ to $9.5\times10^{10}cm^{-2}$. These values are very good for SiC, but more experimentation must be done to assure the validity of these values.

All the curves indicated that the SiC deep depleted instead of inverting, as shown in Figure 28 by the steadily decreasing capacitance – even at -10V. This effect is seen even at very

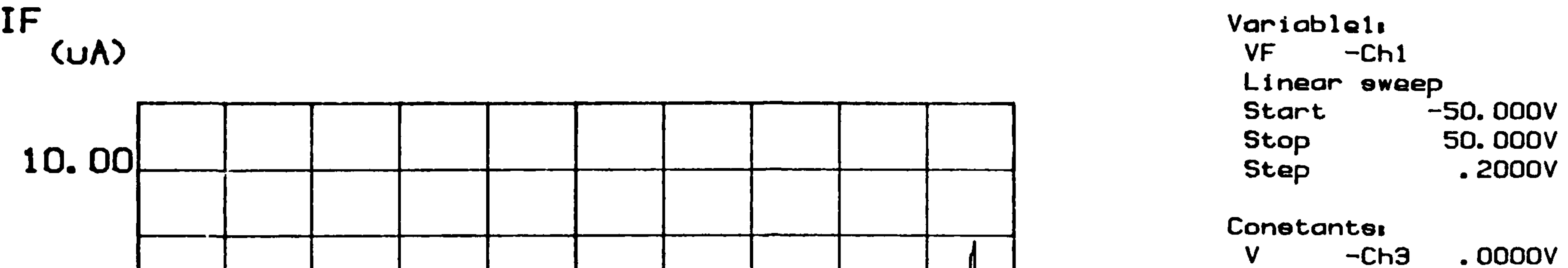


Figure 29. I-V curve of MOS capacitor with 915 Å of oxide grown in dry O_2 at 1473K and annealed in Ar for 3600 s at the same temperature. Oxide breaks down at 29 V.

low sweep rates (e.g., 20 mV/sec). It is likely that this behavior is caused by the fact that minority carriers are so rare in SiC at room temperature that inversion is difficult to achieve, therefore the increased gate voltages are compensated by increasing the depletion depth. Some higher temperature measurements (e.g., at 473K) have been made and the SiC appears to invert, but more experimentation is needed.

The breakdown electric field for the thermally grown oxides is generally quite good, having a range of $(2.5 - 3.0)\times10^{-6}$ V/cm. An example of 3.07×10^{6} V/cm for the 1473K Ar annealed sample is shown in Figure 29. The oxide thickness was 945Å and it reached breakdown at +29 V. The oxides always fail when the SiC is in accumulation.

To summarize, initial C-V curves for MOS structures with oxides grown at 1473K in dry 0_2 look very good. At room temperature, SiC deep depletes instead of inverting, but the fixed oxide charge densities are desirably low. However, because of problems with leakage current and consistency, device improvement is needed.

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