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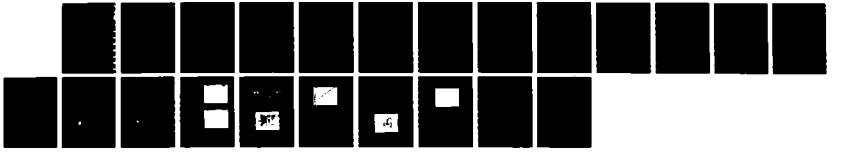

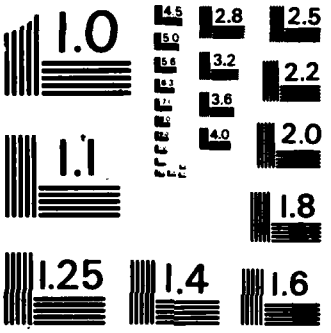

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A novel process suitable for fabricating superconducting circuitry based on the all refractory material NbN is described. In this process, an in-situ trilayer film composed of NbN/MgO/NbN is used to fabricate Josephson tunnel junctions. Reactive ion etching processes are used to—

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delineate devices and pattern insulators and metallizations. Fabricated junctions have yielded good tunneling characteristics with reasonable current density uniformity and reproducibility. Devices with gap voltages close to 5mV have been achieved for high quality junctions (Vm > 20 mV). In addition to the trilayer, there are two wiring layers, two resistor depositions, and two insulation layers, constituting a full NbN based fabrication technology. Using this process, we fabricated and successfully tested thin film DC SQUID and time domain reflectometer (TDR) circuits. Preliminary measurements suggest that the critical temperature of these circuits is well within the operating temperature of commercial two-stage closed cycle refrigerators.

A-1

INTRODUCTION

There has been considerable interest in recent years in the fabrication of all refractory Josephson tunnel junctions. The mechanical stability and excellent cycleability of superconducting materials such as Nb and NbN make them very attractive for robust integrated circuits. In addition, the Selective Niobium Anodization Process (SNAP), and its modifications, such as SNEP which incorporates dry Etching in its process, have greatly improved junction fabrication process because of their inherent cleanliness during junction fabrication.

Early Nb and NbN devices were fabricated by growing the native oxide on the base electrode. However, device quality for such junctions were less than ideal, presumably due to the formation of the niobium suboxides in the barrier. Recent success by several groups in using oxidized aluminum as a barrier has dramatically changed the Nb based circuit process[1,2]. Oxidized aluminum has proven to be an excellent choice for all niobium devices, because it forms a stable and uniform oxide after thermal oxidation.

The success in fabricating niobium devices with artificial barriers has led several groups to focus their attention on NbN based junctions with artificial barriers[3-5]. The high transition temperature of NbN is technologically important because NbN based circuits have greater stability than Nb devices in liquid Helium. Moreover, such a high transition temperature allows NbN based devices to be cooled with small reliable closed-cycle refrigerators. Sub-compact coolers would then greatly expedite the use of certain subsystems such as SIS mixers, magnetometers, and signal processors in non-laboratory applications.

In addition to its high transition temperature, NbN has the added advantage of good surface stability. Such a property makes NbN films attractive for further complicated processing needed for circuit fabrication. The inertness of NbN surface suggests the possible use of artificial oxides as the tunnel barrier in NbN based devices. Thermally oxidized aluminum and deposited MgO have been used by a few researchers as artificial barriers for such devices[3,5]. We have also developed a process capable of producing high quality NbN/MgO/NbN devices. This fabrication process which is compatible with Integrated Circuit (IC) processing has led to an eight-level circuit process capable of producing complex NbN-based circuits.

In this paper, we report on our NbN circuit fabrication in which reactive ion etching techniques are used to pattern junctions, electrodes, and insulating layers. The process has four niobium nitride layers, two SiO_2 insulating layers, and two resistor levels, in addition to a deposited MgO as a tunnel barrier. This circuit process has been utilized to fabricate thin film DC SQUIDs as well as Time Domain Reflectometer (TDR) circuits. A detailed description of this circuit process as well as preliminary measurements on the fabricated circuits are reported in this paper.

FABRICATION

Fig. 1 shows the process for NbN/MgO/NbN Josephson tunnel junction fabrication. First, a multilayer of NbN, MgO, and NbN is deposited, in situ, on silicon or fused quartz substrates. An NbN base electrode of approximately 800Å is DC magnetron sputtered onto substrates at 15 mtorr of argon and nitrogen pressure. Nitrogen partial pressure is kept at 3.5 mtorr during the base electrode deposition. The NbN deposition rate is approximately 1700 Å/min. The substrates are not intentionally heated or cooled during the deposition of the base electrode. MgO is then RF sputtered at a rate of 40 Å/min. in argon pressure of 20 mtorr. The wafers are subsequently heated to 300 ℃ prior to deposition of the NbN counterelectrode. The NbN counterelectrode is approximately 800Å thick and is deposited under the same condition as the base electrode.

Device geometry is defined using a modified version of SNEP technology. A schematic cross-section of the Josephson junction device fabrication is shown in Fig. 1. Various layers and processes used in the junction fabrication are listed in Table I. The base electrode is defined by using the first mask and reactively etching the counterelectrode in CF_4/O_2 plasma.

Table II summarizes the etch rates for various materials under CF_4/O_2 condition. The RF power density during the etch is approximately 0.1 W/cm^2. Since MgO is an excellent etch stop, the base electrode etch cannot be completed in a single step. The MgO barrier is subsequently wet etched in buffered HF solution and wafers are then patterned with the second mask for junction definition. The counterelectrode and the remainder of the base electrode are then reactively etched together. Since the base and the counterelectrode have the same thicknesses, both electrodes are consumed at the same time. In addition, due to the presence of an MgO barrier, several minutes of overetch does not affect junction fabrication process. If desired, the base electrode can be made much thicker than the counterelectrode and the same process can still be used to define junctions.

Device fabrication is completed by addition of an SiO_2 layer and an NbN metallization. SiO_2 is rf deposited at a rate of 55 Å/min. from an SiO_2 target. The nominal thickness of the SiO_2 is about 2300Å. SiO_2 is reactively etched in CHF_3 plasma at a power density of 0.25 W/cm^2. Table III lists the SiO_2 etch conditions in the reactive ion etching system. The NbN metallization layer is approximately 3000Å and is deposited and patterned under the same condition as the NbN base electrode. Fig. 1 shows the schematic cross-section of a completed device.

The fourth step is the deposition and patterning of a Ti layer to form resistors (Fig. 2). The resistors are patterned on the SiO_2 layer to minimize step coverage problem. The resistivity of the 1500Å Ti film is about 15 μOhm-cm at 4.2 K. Ti resistors are defined by wet chemical etching in a commercial Ti etch solution.

The next step in the process is the deposition of an SiO_2 layer. The deposition and patterning of this layer is similar to the previous layer except that the second insulating layer is about 5000Å thick.

The sixth step involves another NbN deposition (6000Å) and patterning. This layer is normally used as additional wirings or as control lines for Josephson junctions. The presence of two NbN metallization layers separated by the second SiO_2 film allows crossovers which facilitates circuit design. Finally, a 6500Å Al layer which is deposited by a DC magnetron source completes the circuit fabrication. The implementation of this 8-level process allows fabrication of complex Josephson junction based circuits with magnetically controlled interferometers and densely populated circuits. Fig. 2 shows the cross-section of a fabricated circuit.

EXPERIMENTAL RESULTS

In order to determine current density uniformity over a 3" area, numerous wafers populated with as many as 500 junctions were fabricated. Fig. 3a shows a typical volt-ampere characteristic for all NbN devices with the gap voltage of 4.9 mV. Fig. 3b is the volt-ampere characteristic of 80 such devices in series. The quasi-particle current at the sum of the gaps is approximately 450 A/cm^2. The current density uniformity over 1/4 X 1/4" area is generally better than 10%. Such a uniformity is about 15% over 1 in^2 area and 30% over a 3 in^2 area. These non-uniformities are combined effects of mask, photolithography, and variation in the MgO thickness.

This all NbN process has been used to fabricate thin film DC SQUIDs and Time Domain Reflectometers (TDR) circuits. Even though several layers of metallizations, insulators, and resistors follow the junction trilayer in this process, no degradation in device characteristics have been observed. In addition, the step coverage of all layers are rather good, considering the fact that the vertical structures grow with each successive deposition.

The SQUID layout is very similar to the design by Ketchen[6]. It contains two resistively shunted junctions and one inductively coupled control line. The physical layout of this SQUID is shown in Fig. 4. Tunnel junctions are 10 X 10 μm^2 and each device is shunted by a 2 Ohm resistor.

The tested SQUID has a primary coil consisting of 50 turns with 4 μm wide linewidth on a 10 μm pitch. The SQUID loop inductance as determined by self modulation is estimated to be 4 pH. The mutual inductance is measured to be approximately 0.7 nH. Assuming unit coupling, the input coil inductance is about 120 nH. Fig. 5 shows the SQUID characteristics for various input coil currents.

The TDR circuit is composed of a sampling gate, a pulse generator, a step generator, and a superconducting transmission line and is identical to the circuit described by S. Whiteley[7]. The block diagram of the sampling TDR system and the photograph of the TDR circuit are shown in Fig. 6. The waveform generated by the step generator and reflected from the 1 cm transmission line is shown in Fig. 7. The operation of the sampling system has been described extensively elsewhere[8,9]. An external pulse triggers the step generator directly and the pulse generator through an electronically variable delay circuit. The sampling gate voltage is kept at a reference voltage set by a comparator and a feedback loop. The current needed to maintain such a voltage across the sampling gate is a measure of the TDR waveform which drives the vertical axis of the plotter. The present design which has been optimized for a Nb based circuit resulted in the waveform exhibited in Fig. 7. The lack of performance is mainly attributed to the large penetration depth of NbN films.

CONCLUSION

In summary, all NbN Josephson junction based circuits have been successfully fabricated by using dry etching techniques for patterning. The fabricated junctions exhibited relatively good tunneling characteristics and repeatability. This dry etching process is quite applicable to making large scale integration circuits for logic, memory, and other applications. The fabricated DC thin film SQUID circuit is suitable for applications in magnetometry. A modified circuit design without any change in the fabrication process has applications in digital logic and memory circuits. The TDR circuit, once optimized, in conjunction with the cryogenic system can be a high performance TDR system[10]. Because of niobium nitride's high critical temperature, such systems can then use inexpensive closed cycle refrigerators for commercial applications.

TABLE I

ALL NbN CIRCUIT FABRICATION PROCESS

	Material	Purpose	Type of Etch
	NbN	Base electrode	RIE
1	MgO	Barrier	Wet etch
	NbN	Counterelectrode	RIE
2	SiO_2	First insulator	RIE
3	NbN	First metallization	RIE
4	Ti	First resistor	Wet etch
5	SiO_2	Second insulator	RIE
6	NbN	Second metallization	RIE
7	Al	Second resistor	Wet etch

TABLE II

REACTIVE ION ETCHING OF NbN

CF_4 flow rate	=	75 SCC/Min.
O_2 flow rate	=	9 SCC/Min.
Power density	=	0.1 W/cm^2
Pressure	=	200 mtorr

Material	Etch Rate (A/min)
NbN	1000
SiO_2	60
Ti	50
Photoresist	200

TABLE III

REACTIVE ION ETCHING OF SiO_2

CHF_3 flow rate = 75 SCC/Min.

Power density = 0.25 W/cm^2

Pressure = 20 mtorr

Material	Etch Rate (A/min)
SiO_2	180
NbN	60
Ti	20
Photoresist	200

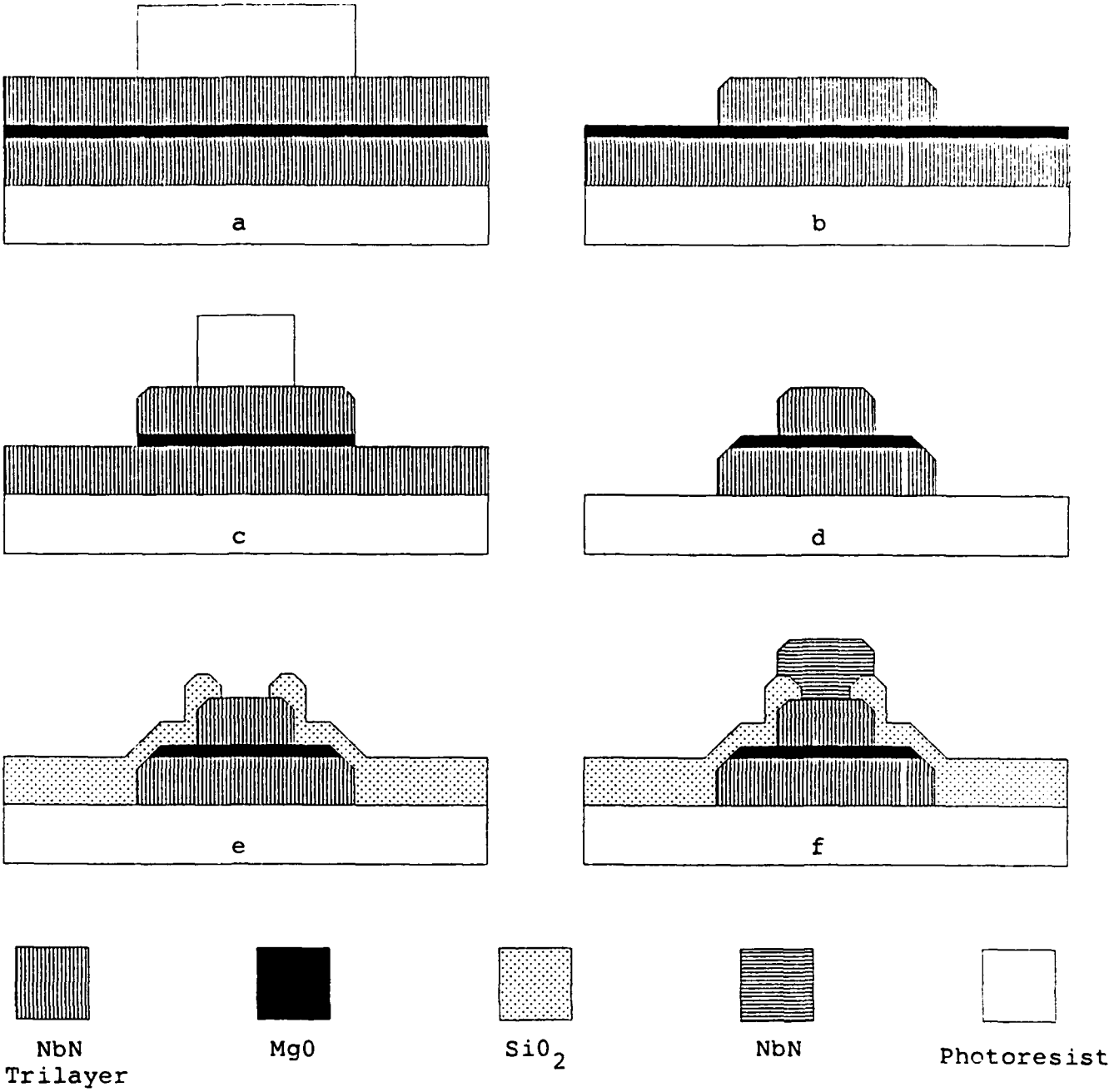


Fig. 1 Fabrication processes of NbN/MgO/NbN Josephson tunnel junctions

a. Deposit NbN/MgO/NbN trilayer.

b. Reactively etch counterelectrode with the first mask to define the base electrode pattern.

c. Etch MgO.

d. Define junctions and etch remainder of the base electrode.

e. Deposit and pattern SiO_2.

f. Deposit and pattern NbN metallization.

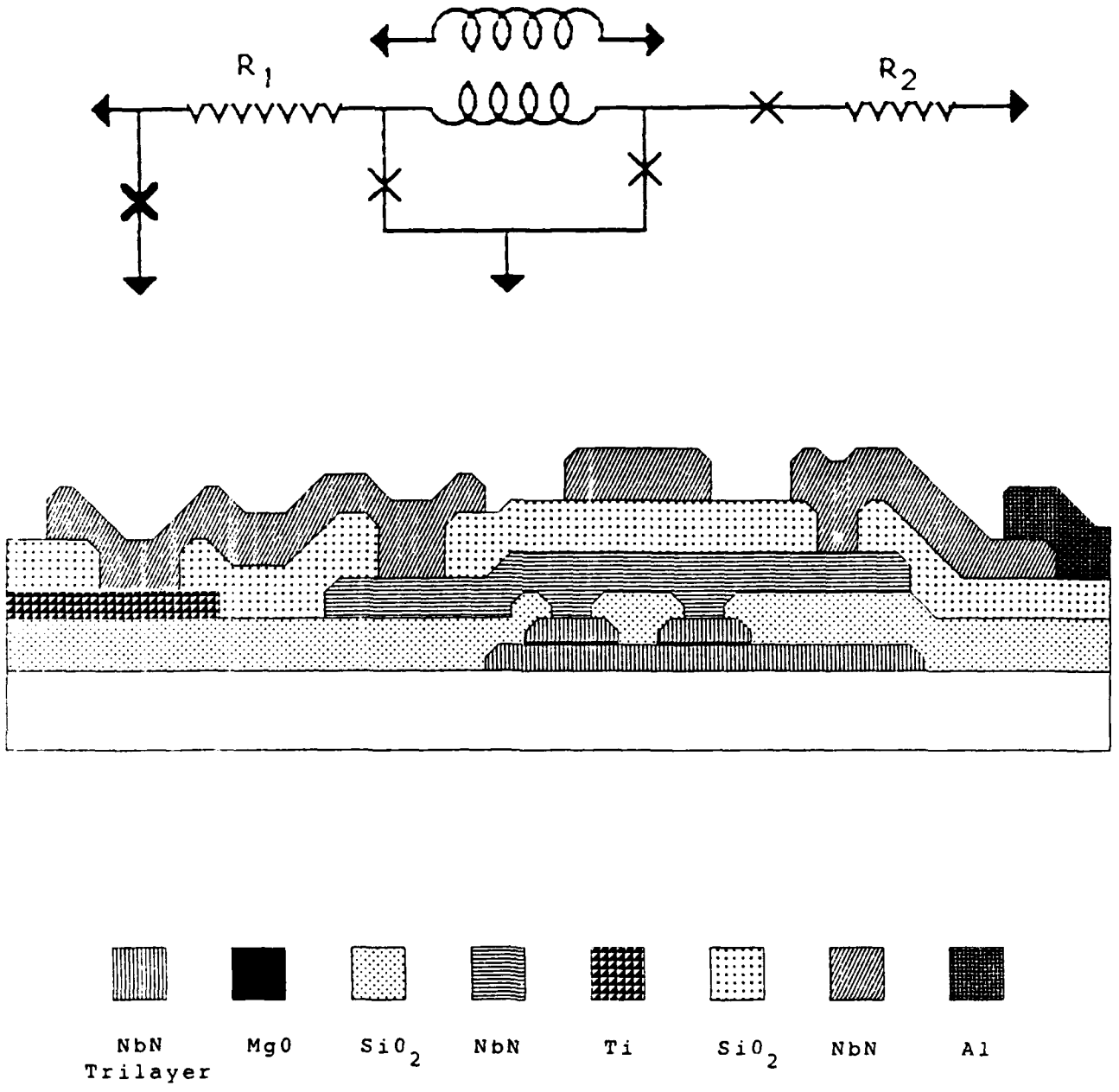
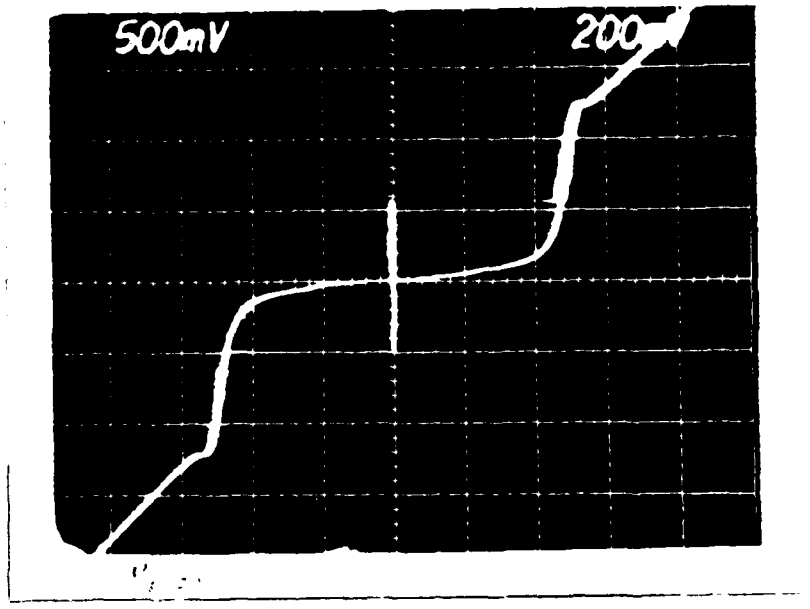
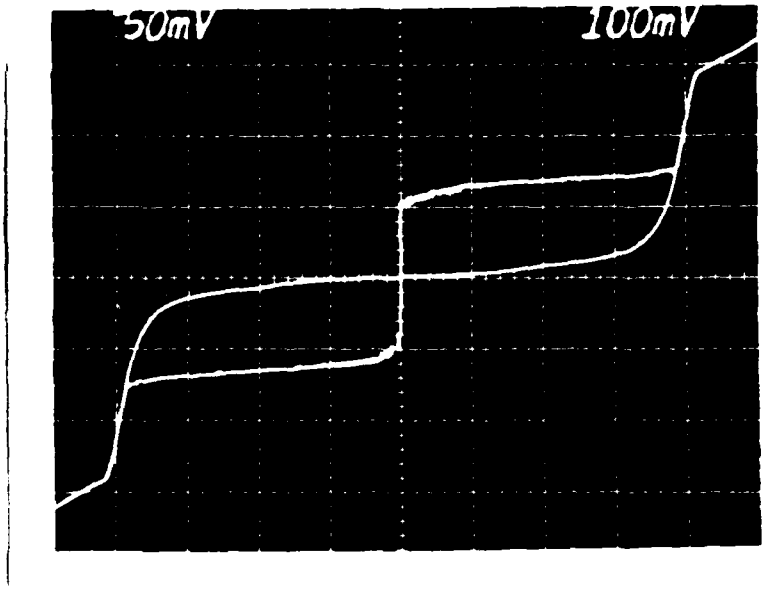


Fig. 2 Cross-section of a two-junction interferometer with magnetically controlled line. R1 and R2 are Ti and Al resistors, respectively.



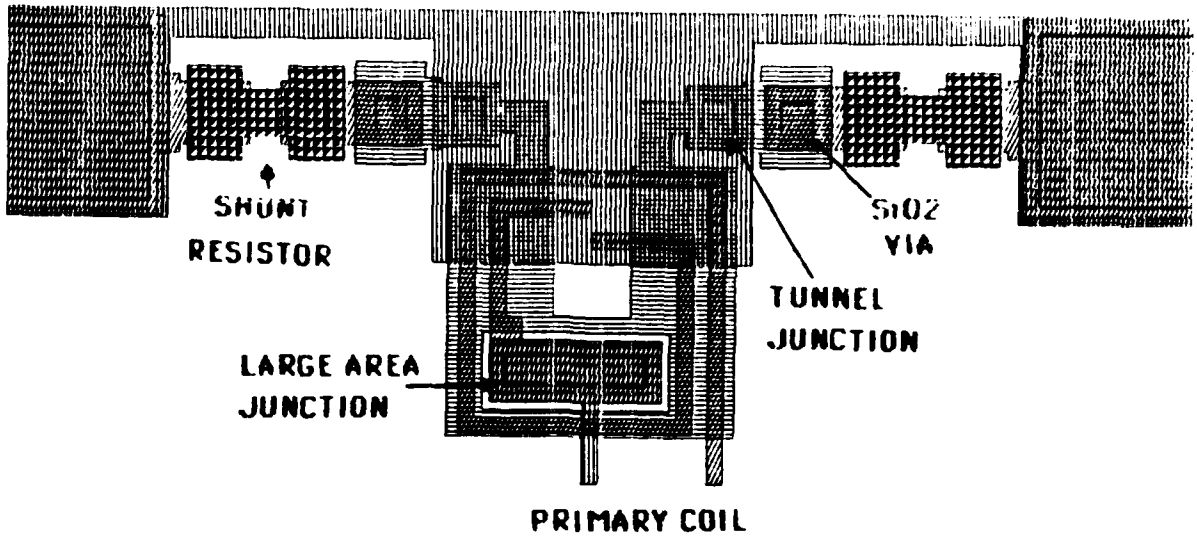
Vert. scale = 0.5mA/div.
Horiz. scale = 2.0mV/div.



Vert. scale = 0.5mA/div.
Horiz. scale = 100mV/div.

Fig.3a. Volt-ampere characteristics of an NbN/MgO/NbN device at 4.2 K. Junction size is nominally 16 X 16 um^2.

b. Eighty junctions in series.



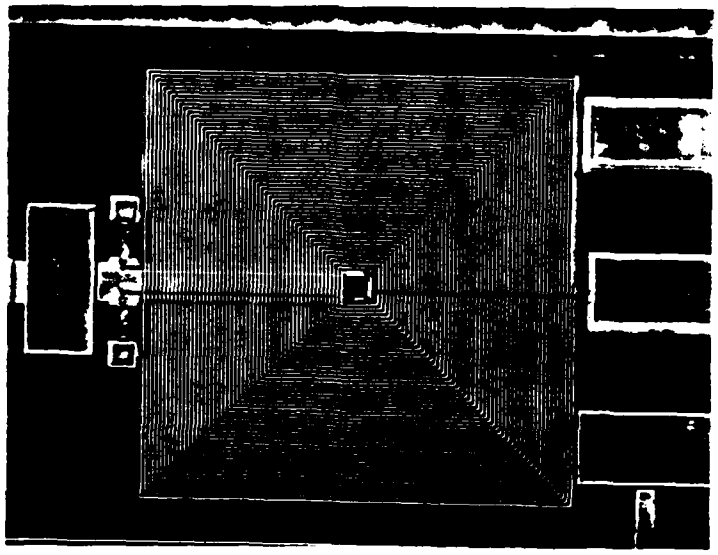


Fig. 4 Inductively coupled SQUID layout.

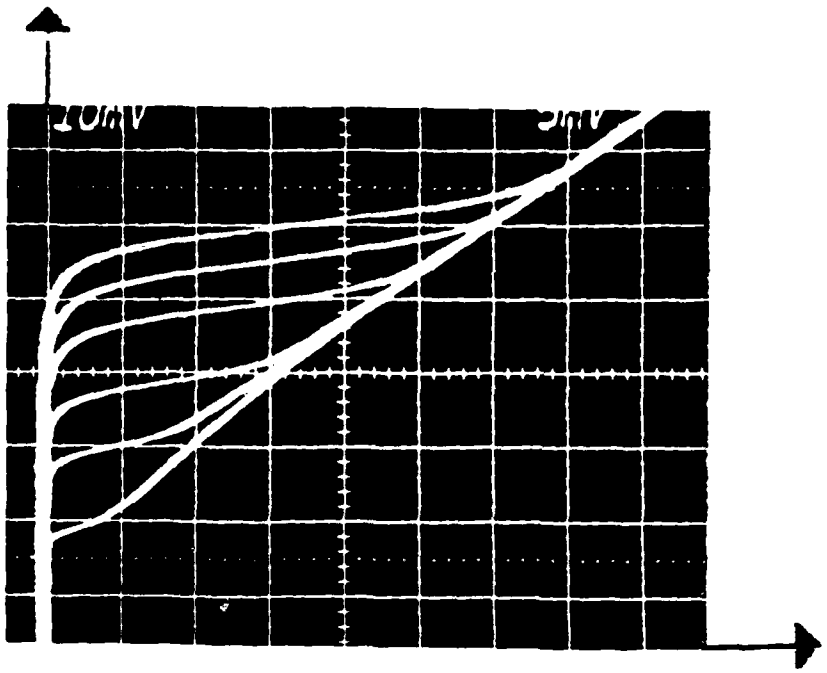
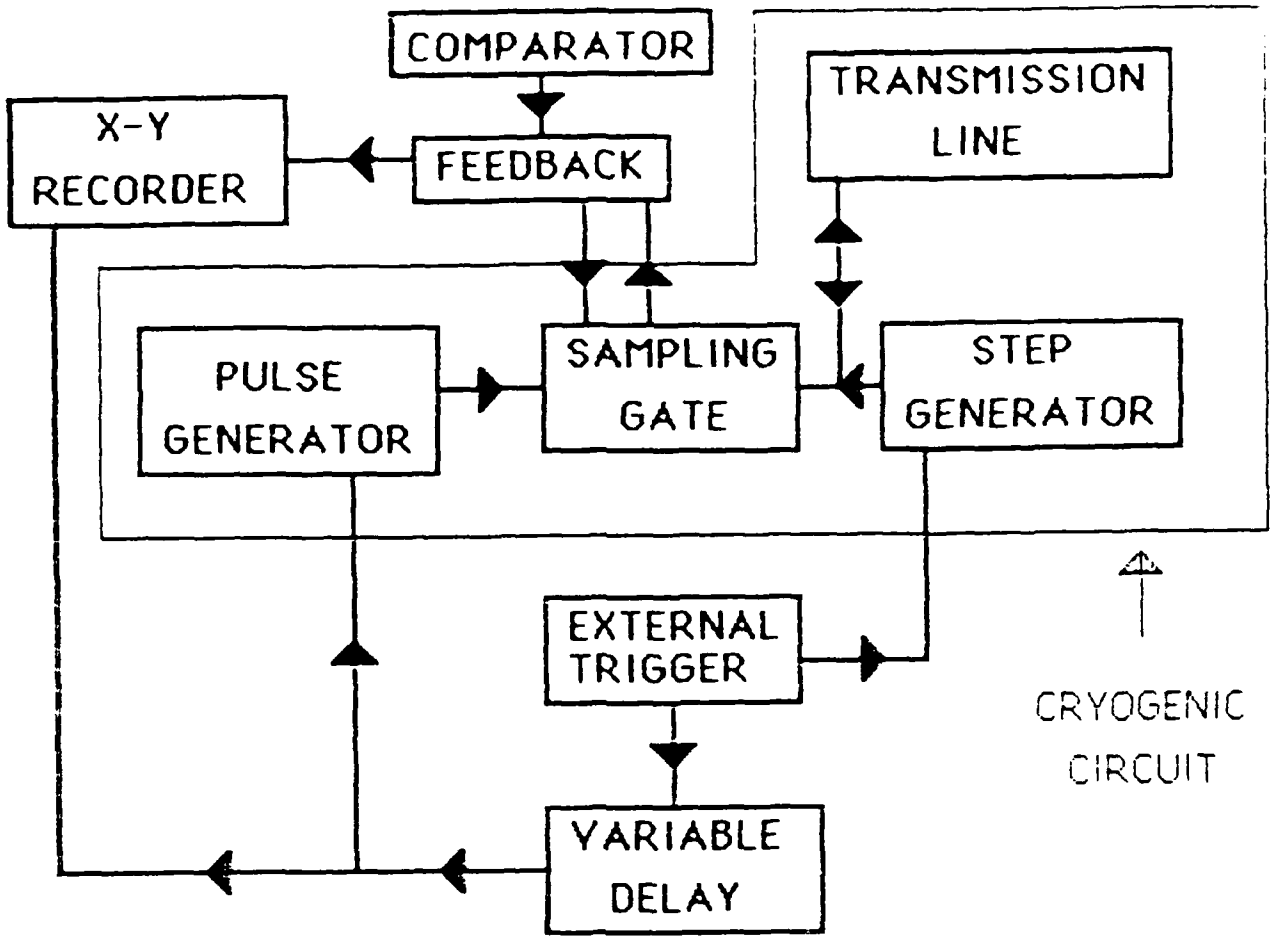


Fig. 5 Volt-ampere characteristic of a SQUID.

Verticle scale = 0.1 mA/div.
Horizontal scale = 50 μV/div.

The family of curves are for 0, 0.6, 0.8, 1.0, 1.2, and 1.4 μA input coil currents.



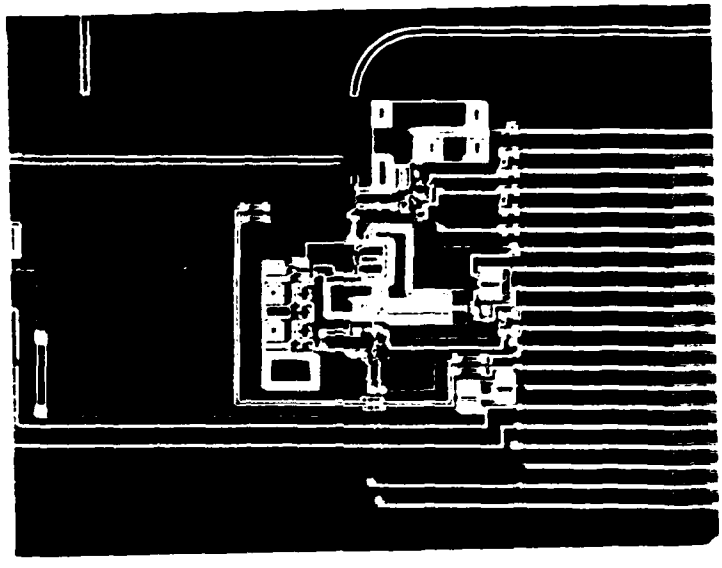


Fig. 6 Block diagram of the TDR circuit sampling system.

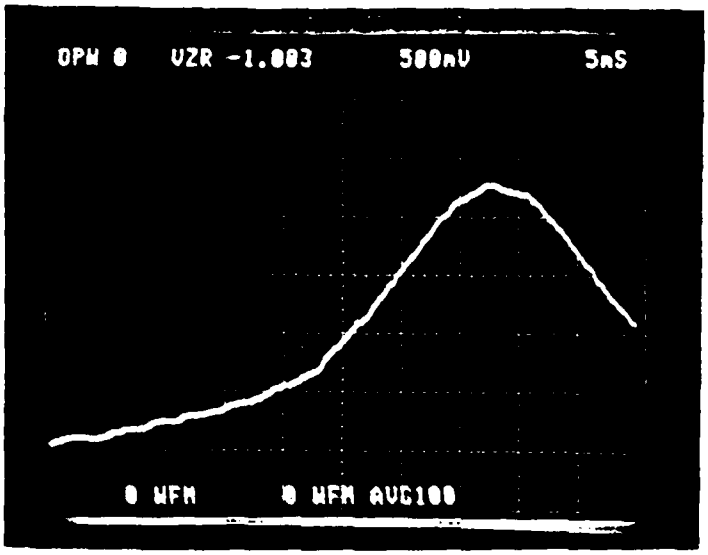


Fig. 7 TDR waveform for an open circuit transmission line.

Horizontal scale = 20 ps/div.
Vertical scale = 0.1 μA/div.

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