

AD-A170 772

INVESTIGATION OF A NEW CONCEPT IN SEMICONDUCTOR
MICROWAVE OCCILLATORS(U) PURDUE UNIV LAFAYETTE IN
SCHOOL OF ELECTRICAL ENGINEERING J A COOPER 20 MAY 86

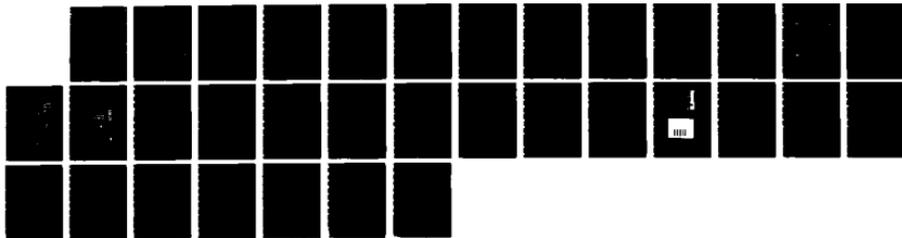
1/1

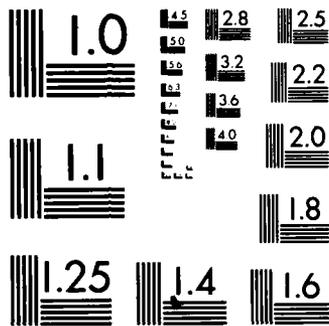
UNCLASSIFIED

AFOSR-TR-86-0527 AFOSR-85-0193

F/G 9/5

ML





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

2

Investigation of a New Concept in Semiconductor Microwave Oscillators

AD-A170 772

James A. Cooper, Jr.
School of Electrical Engineering
Purdue University
West Lafayette, IN 47907

Approved for public release,
distribution unlimited

20 May 1986

Annual Report for Period 1 May 1985 - 30 April 1986

DTIC
ELECTE
AUG 13 1986
S B D

FILE COPY

Prepared for

Air Force Office of Scientific Research
Building 410
Bolling AFB, DC 20332-6448

*Originals are on microfilm
plates: All DTIC reproductions
will be in black and
white.

AD-A170772 (2)

REPORT DOCUMENTATION PAGE

1a REPORT SECURITY CLASSIFICATION Unclass		1d RESTRICTIVE MARKINGS	
2a SECURITY CLASSIFICATION AUTHORITY		3 DISTRIBUTION AVAILABILITY OF REPORT Approved for public release, distribution unlimited	
2b DECLASSIFICATION/DOWNGRADING SCHEDULE			
4 PERFORMING ORGANIZATION REPORT NUMBER(S)		5 MONITORING ORGANIZATION REPORT NUMBER(S) AFOSR-TR- 86-0527	
6a NAME OF PERFORMING ORGANIZATION Purdue University	6b OFFICE SYMBOL (If applicable)	7a NAME OF MONITORING ORGANIZATION AFOSR/NE	
6c ADDRESS (City, State and ZIP Code) West Lafayette, IN 47907		7b ADDRESS (City, State and ZIP Code) Building 410 Bolling AFB, DC 20332-6448	
8a NAME OF FUNDING/SPONSORING ORGANIZATION AFOSR	8b OFFICE SYMBOL (If applicable) NE	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER AFOSR-85-0193	
8c ADDRESS (City, State and ZIP Code) Bolling AFB DC 20332-6448		10 SOURCE OF FUNDING NOS	
		PROGRAM ELEMENT NO. 61bar	PROJECT NO. 2305
		TASK NO. C1	WORK UNIT NO.
11 TITLE (Include Security Classification) Investigation of a New Concept in Semiconductor Microwave Oscillators			
12. PERSONAL AUTHOR(S) James A. Cooper, Jr.			
13a TYPE OF REPORT Annual	13b TIME COVERED FROM 85/5/1 TO 86/4/30	14. DATE OF REPORT (Yr., Mo., Day) 86/5/20	15. PAGE COUNT 23
16 SUPPLEMENTARY NOTATION			
17 COSATI CODES		18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)	
FIELD	GROUP	SUB GR.	
19 ABSTRACT (Continue on reverse if necessary and identify by block number)			
<p>The goal of this research is to fabricate and characterize a new type of semiconductor device known as a contiguous-domain transferred oscillator. This device differs from existing semiconductor oscillators in several fundamental ways, and should be capable of direct electronic tuning in the range from a few gigahertz to a few hundred gigahertz.</p> <p>During the first year of this project, test chips were designed, masks were made, and a processing schedule was worked out. Three aspects of the processing required special attention: implant activation, resistive gate formation, and silicon nitride deposition.</p> <p>Uncapped flash annealing was used for implant activation, and satisfactory results were achieved.</p> <p style="text-align: right;">(Continued ...)</p>			
20 DISTRIBUTION AVAILABILITY OF ABSTRACT UNCLASSIFIED UNLIMITED <input checked="" type="checkbox"/> SAME AS RPT <input type="checkbox"/> DTIC USERS <input type="checkbox"/>		21 ABSTRACT SECURITY CLASSIFICATION Unclassified	
22a NAME OF RESPONSIBLE INDIVIDUAL Gerald L. Witt	22b TELEPHONE NUMBER (Include Area Code) (202) 767-4931	22c OFFICE SYMBOL AFOSR/NE	

19. ABSTRACT (continued)

For the resistive gate, thin metal films were investigated. Nickel and manganese films were not stable after deposition. Nickel-chromium films were stable, but did not provide high enough resistivity to allow continuous operation of the device. It was decided to build the first devices with nickel-chromium and to operate them in a pulsed mode.

Silicon nitride layers were deposited on gallium arsenide by plasma assisted chemical vapor deposition, and the interface was found to have a high density of surface states. It was decided that the initial devices will use silicon nitride only between the gate and drain electrodes

Two test wafers were begun, and at the time of this report both wafers were about midway through the fabrication schedule.



Accession For	
NTIS	<input checked="" type="checkbox"/>
DTIC	<input type="checkbox"/>
Unannounced	<input type="checkbox"/>
Justification	
Date	
Disc	
A-1	

**Investigation of a New Concept in
Semiconductor Microwave Oscillators
Annual Report**

**James A. Cooper, Jr.
School of Electrical Engineering
Purdue University**

AIR FORCE OFFICE OF SCIENTIFIC RESEARCH (AFOSR)

NOTICE OF TRANSMITTAL TO DTIC

This technical report has been reviewed and is
approved for public release IAW AFR 190-12.

Distribution is unlimited.

MATTHEW J. KEEPER

Chief, Technical Information Division

I. INTRODUCTION

The goal of this project is to build and operate a contiguous-domain transferred-electron oscillator. The contiguous-domain oscillator (CDO) is a millimeter wave semiconductor device which operates in a manner fundamentally different from conventional microwave diodes such as the Gunn, IMPATT, TRAPATT, or BARITT. The contiguous domain oscillator is not a transit-time device. It does not require a short drift region to achieve high frequency operation. Since the internal fields are isolated from the load, the CDO does not require a tuned output circuit. Since the oscillation frequency is determined by the spatial period of the contiguous domains in the drift channel, which in turn depends upon the average electron density in the channel, the frequency can be electrically varied over a wide range during operation.

At the beginning of this research project, the operation of the contiguous domain oscillator had been studied only by computer simulation. The goal of this project is therefore to build and characterize an experimental device. We considered two possible implementations: a device based on the GaAs MESFET geometry, or a device based on the GaAs MODFET (or HEMT) geometry. Because of the simpler fabrication sequence, we decided to build the MESFET version first.

In the next section we discuss the design of the prototype device and the fabrication sequence we are using to build it. In Section III we identify three processing problems which arose and discuss our progress in dealing with them. Section IV concludes this report with a summary of our present status and plans for the coming year.

II. DESIGN AND FABRICATION EFFORTS

A cross section of the initial prototype device is shown in Fig. 1. As seen, the device is essentially a GaAs MESFET with a resistive gate. The resistive gate has contacts at each end, and the gate and contacts must overlap the source and drain. It is this latter requirement which places the most strenuous demands on the fabrication.

We have designed a comprehensive test chip for the MESFET oscillator. The test chip consists of three individual chips, shown in Figs. 2 through 4. The chip in Fig. 2 contains two oscillators, with fan-shaped microstriplines to carry the AC signal to the chip edge. Figure 3 shows a chip containing several oscillators and a variety of special elements which can be wire bonded to the oscillator to create microwave antennas for radiating the AC signal to a nearby pickup loop. Figure 4 shows a chip containing two oscillators and several special structures for process monitoring. The smallest features on these chips are 5 μm . The masks were made using our Cambridge electron beam exposure machine, and all the lithography steps will be optical.

The chip layout and mask fabrication were done by Robert E. Beaty, a Ph.D. student who has been working on GaAs processing for about two years. Bob is responsible for the overall processing of the MESFET oscillator, and he has developed the fabrication technology discussed below.

The fabrication sequence is listed in Appendix I, and is illustrated for the 20 x 50 μm oscillator by a series of transparencies in Fig. 5. We begin with an undoped semi-insulating (100) GaAs substrate. Following cleans, a initial lithography step is performed to etch registration marks into the substrate for subsequent mask alignment. A second lithography step establishes the area for ion implantation of the n-type channel region. The channel is implanted with silicon at 120 keV to an average doping of 10^{17} cm^{-3} . A third lithography step localizes the source and drain regions, which are implanted with silicon to a doping level of around $5 \times 10^{17} \text{ cm}^{-3}$. The implants are then activated by flash annealing to 900 C for five seconds. Next, 80 nm of SiN is deposited at low temperature (225 C) using plasma assisted CVD and etched as shown in the figure. Photoresist is then applied and patterned for the alloy contacts, and Au-Ge is evaporated. The photoresist is lifted off and the Au-Ge alloyed at 450 C. Next, the gate lithography is performed and a resistive Ni-Cr film is evaporated and patterned by liftoff. Finally, the metal lithography is performed and Al is evaporated and defined by liftoff. At this time, the device is

completed, although an additional layer of SiN may be added for scratch protection. The devices are diced from the wafer and mounted on a 50 Ω ceramic strip line for DC and microwave testing.

This fabrication sequence is similar to that routinely used for GaAs MESFETs except for the SiN layer and the resistive Ni-Cr gate. These two steps required special attention before we could begin processing. In addition, we had to learn to activate ion implants in GaAs by flash annealing. These three procedures occupied most of our attention during this first year, and will be fully described in the next section.

III. PROCESSING STEPS REQUIRING SPECIAL ATTENTION

A. Ion Implantation and Activation

Activation of implants in GaAs is a problem because at the temperature needed to activate the dopants (750 - 900 C), GaAs dissociates due to loss of As from the compound. For activation, we flash anneal in a Research, Inc. radiant thermal annealer, which uses four 2kW lamps in a quad-elliptical heating chamber. The uncapped sample is heated to around 900 C in a pulse whose full width (half maximum) is about five seconds. We have found that anneals below about 900 C cause no surface degradation of the GaAs. The activation ratio is only slowly dependent on temperature in the range from 750 to 900 C. A thorough wafer clean is necessary after the implantation and before activation to remove Mn and other impurities picked up during implantation. These residual impurities tend to be incorporated into the GaAs at levels in the low to mid 10^{16} cm^{-3} range and compensate the implanted Si at the lower doses. We can now achieve 50-60% activation for implants in the range from 2×10^{17} to 2×10^{18} cm^{-3} , yielding activated concentrations from 1×10^{17} to 1×10^{18} cm^{-3} . This range is adequate for the fabrication of the prototype devices.

The implant and activation work was performed by John S. Kleine, a Masters student who will receive his degree in August. John solved some tricky practical problems with measuring temperature transients in the annealer and in comparing uncapped versus proximity-capped anneals. He is now doing measurements of activation ratio and compensation ratio as a function of dose.

B. Resistive Gate Deposition

The CDO requires a resistive gate in order to establish a uniform electric field in the drift channel. For CW operation, the gate needs a sheet resistance of at least $10 \text{ k}\Omega/\square$ to limit heating. If we are willing to operate in pulsed mode, the resistance can be as low as $100 \Omega/\square$.

We initially studied thin metal films of Mn, Ni, and Ni-Cr. Mn films were deposited by completely evaporating a carefully weighed charge. For thicknesses from 200 \AA to 800 \AA , the sheet resistivity ranged from about $300 \Omega/\square$ down to $50 \Omega/\square$. Ni films were evaporated using an in-situ resistance monitor, and resistivities from about $3000 \Omega/\square$ to $20 \Omega/\square$ were obtained. Both Mn and Ni, however, showed an aging effect after several days of exposure to air at room temperature, manifested by a gradual increase in the resistivity.

Ni-Cr films were also evaporated using an in-situ monitor, and resistivities ranging from $341 \Omega/\square$ to $13 \Omega/\square$ were obtained. The Ni-Cr films were stable in air at room temperature, and showed only a slight reduction in resistivity when annealed in air at 250 C for 10 minutes. Although these resistivity values are not high enough to allow CW operation of the oscillator, we have decided to use Ni-Cr for the prototype devices, restricting ourselves to pulsed operation for the time being.

The work cited above was performed by Ming Fang, who received the MS degree in December, 1985. Unfortunately, Mr. Fang decided to terminate his graduate program after the MS degree.

Based on the results of Mr. Fang's work, we have concluded that metal films cannot provide high enough resistivity for CW operation of the CDO. However, we have discovered that sputtered CERMET films are capable of resistivities considerably higher than the minimum needed for CW operation. After discussions with workers at Rockwell International who have considerable experience with CERMETS, we ordered a target with the Cr/SiO composition needed to produce films in the $10 \text{ k}\Omega/\square$ -- $50 \text{ k}\Omega/\square$ range with a thickness in the neighborhood of 3000 \AA . The target has now been received, and after some experimentation we intend to incorporate CERMET gates on future devices.

C. Electrical Quality of SiN Layers

We have been depositing SiN films on both silicon and GaAs substrates for about a year using plasma assisted CVD. The DC electrical properties, i.e. breakdown strength and dielectric constant, have been good, and the CV curves have also appeared normal. However, we have recently looked at CV curves with frequency as a parameter. A typical set of curves is shown in Fig. 6. The hysteresis and frequency dispersion indicate a high density of surface states and traps in the bulk SiN. It is our judgment that the density of traps in our films would probably interfere with the operation of the oscillator. Accordingly, we have modified the original design for the MESFET version of the oscillator (as described in the proposal) to remove the SiN from the active portion of the channel. We retain SiN between the gate and drain to reduce the gate-to-drain capacitance and to prevent edge breakdown. The new design is shown in Fig. 1 and Fig. 5.

By removing the SiN from the active channel, we reduce the operating margins of the device. We are working to improve the electrical quality of the SiN to the point where it can be used in the channel area in the future. Recently, workers at Hughes Research have reported improvements in the electrical quality of plasma-deposited SiN on GaAs by use of a predeposition surface treatment and a postdeposition anneal. We plan to investigate their technique in the near future.

The silicon nitride deposition and characterization was done by Bob Beaty.

IV. PRESENT STATUS AND GOALS

As of this writing we are processing two device wafers. The first wafer was fabricated using a slightly different procedure from that outlined above: instead of using an ion implanted channel, we grew the n-type channel layer with molecular beam epitaxy (MBE) and performed a mesa etch to isolate the channel regions. (This approach was taken because at the time the first wafer was started, we had not been able to activate implant doses low enough for the channel implant.) The second wafer uses an ion implanted channel, as described above. As of this time, both wafers are holding at SiN deposition awaiting the modified nitride etch mask. This places them about halfway through the processing sequence. Although the first (MBE) wafer appears to have a large density of surface defects, the

second wafer looks very good optically. Figure 7 shows the photoresist pattern of the process monitor chip just prior to channel implant. The darker features are registration marks and the lighter features are openings for the implant. The smallest vertical bars are 5 μm wide with 5 μm spaces. As seen, the optical lithography is easily capable of resolving these features.

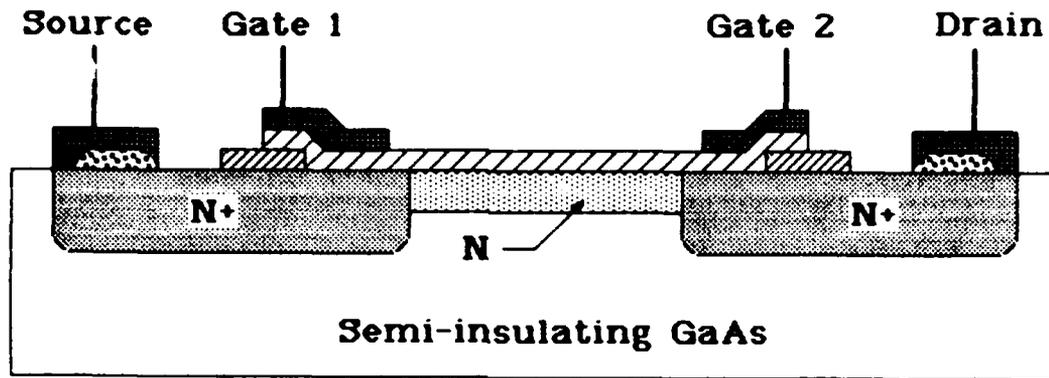
Our immediate goal is to complete the processing of these two test wafers. If the DC characterization looks good, we can test the devices for oscillation. Depending on the results, decisions will be made about starting new wafers or modifying the processing or design. We intend to continue work on improving the quality of the deposited nitride, and hope to return to the original design which includes nitride between the gate and channel, a configuration which would give improved operating margins. Finally, we need to consider a processing sequence for the MODFET version of the oscillator.

V. LIST OF PUBLICATIONS

- (1). J. A. Cooper, Jr. and K. K. Thornber, "Screened-Charge Transferred-Electron Oscillators," IEEE Electron Device Letters, Vol. EDL-6, pp. 50-53, January 1985.
- (2). J. A. Cooper, Jr. and K. K. Thornber, "Contiguous-Domain Transferred-Electron Oscillators," IEEE International Microwave Symposium, St. Louis, MO, June 4-6, 1985.
- (3). J. A. Cooper, Jr. and K. K. Thornber, "A Contiguous-Domain Transferred-Electron Oscillator," IEEE Device Research Conference, Boulder, CO, June 17-19, 1985.

VI. LIST OF PROFESSIONAL PERSONNEL

- (1). James A. Cooper, Jr., Professor of Electrical Engineering (Principal Investigator)
- (2). Michael R. Melloch, Assistant Professor of Electrical Engineering (Consultant on processing, performs MBE growth)
- (3). Robert E. Beaty, Ph.D. Student (Responsible for design, layout, processing, and characterization of test wafers)
- (4). John S. Kleine, M.S. Student (Now completing work on flash annealing of ion implants in GaAs)
- (5). Ming Fang, M.S. Student (Received the MS degree in December, 1985. Thesis title: Fabrication and Characterization of Thin Metal Films. Now no longer associated with this research program.)



-  Channel Implant 150 nm
-  Source/Drain Implant 300 nm
-  Au-Ge Alloy Contact
-  Silicon Nitride 80 nm
-  Ni-Cr Gate 40 nm
-  Al Metal 1 μ m

Figure 1. Cross section of the ion-implanted MESFET version of the contiguous-domain oscillator.

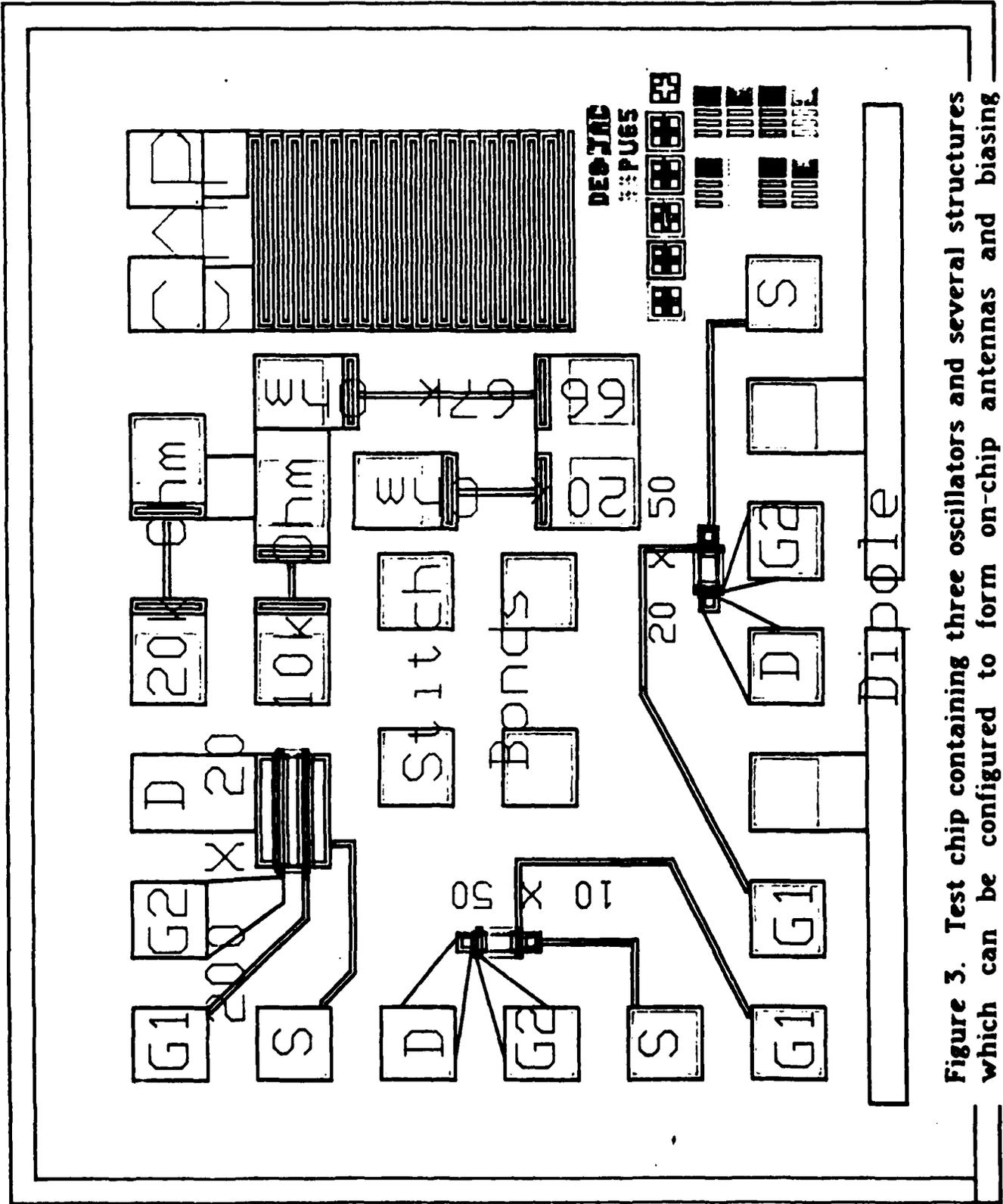
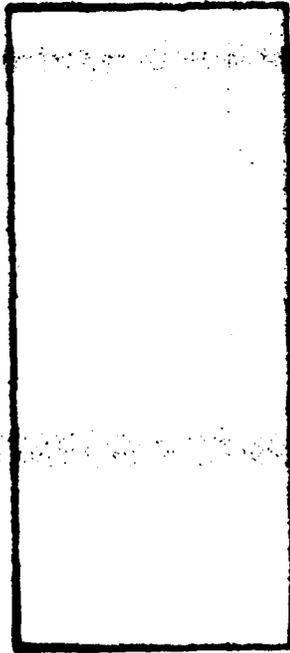


Figure 3. Test chip containing three oscillators and several structures which can be configured to form on-chip antennas and biasing circuitry.

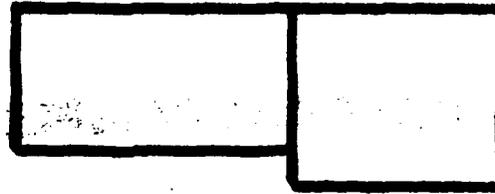
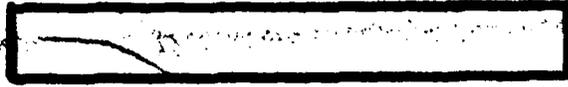
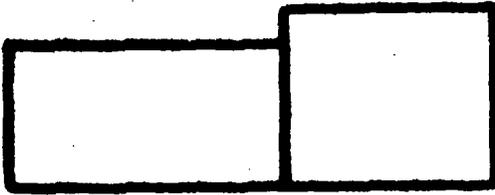
Figure 5. (Following Sheet). Transparent overlays showing the six primary mask levels for the 20 x 50 μm oscillator.

20um x 50um Buried Channel CDO
Resistive Gate

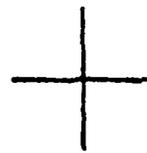


$\square = 5\mu\text{m} \times 5\mu\text{m}$

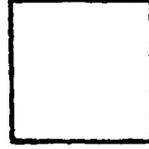
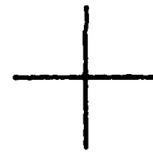
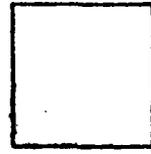
20um x 50um Buried Channel CDO
Top Metal



$$Q = 5um \times 5um$$

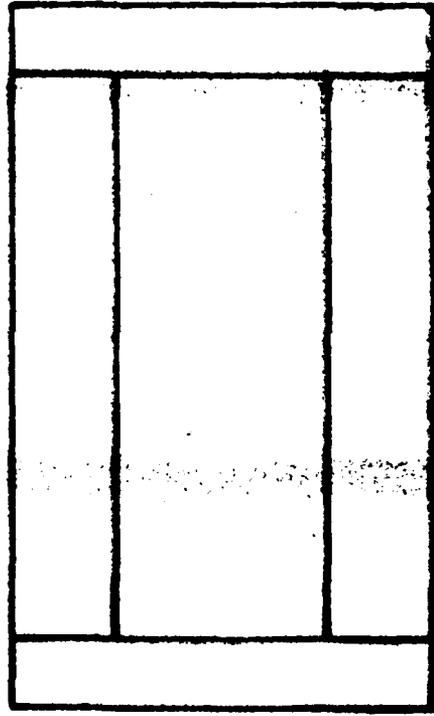


20um x 50um Buried Channel CDO
Alloy Contacts

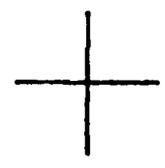


$\square = 50\mu\text{m} \times 20\mu\text{m}$

20um x 50um Buried Channel CDO
Nitride Definition

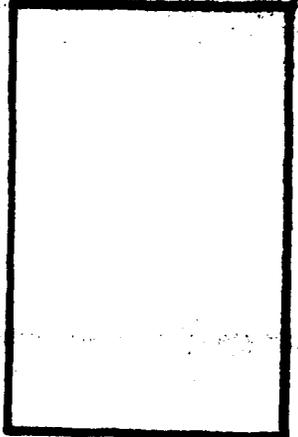
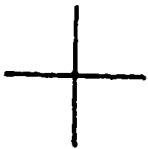
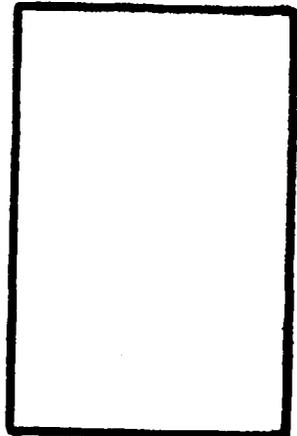


$\square = 5\mu\text{m} \times 5\mu\text{m}$



20um x 50um Buried Channel CDO

Source/Drain Definition



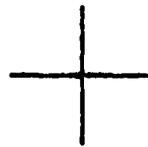
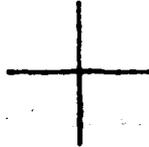
$\square = 5\mu\text{m} \times 5\mu\text{m}$



20um x 50um Buried Channel CDO
Channel Definition



$\square = 5\mu\text{m} \times 5\mu\text{m}$



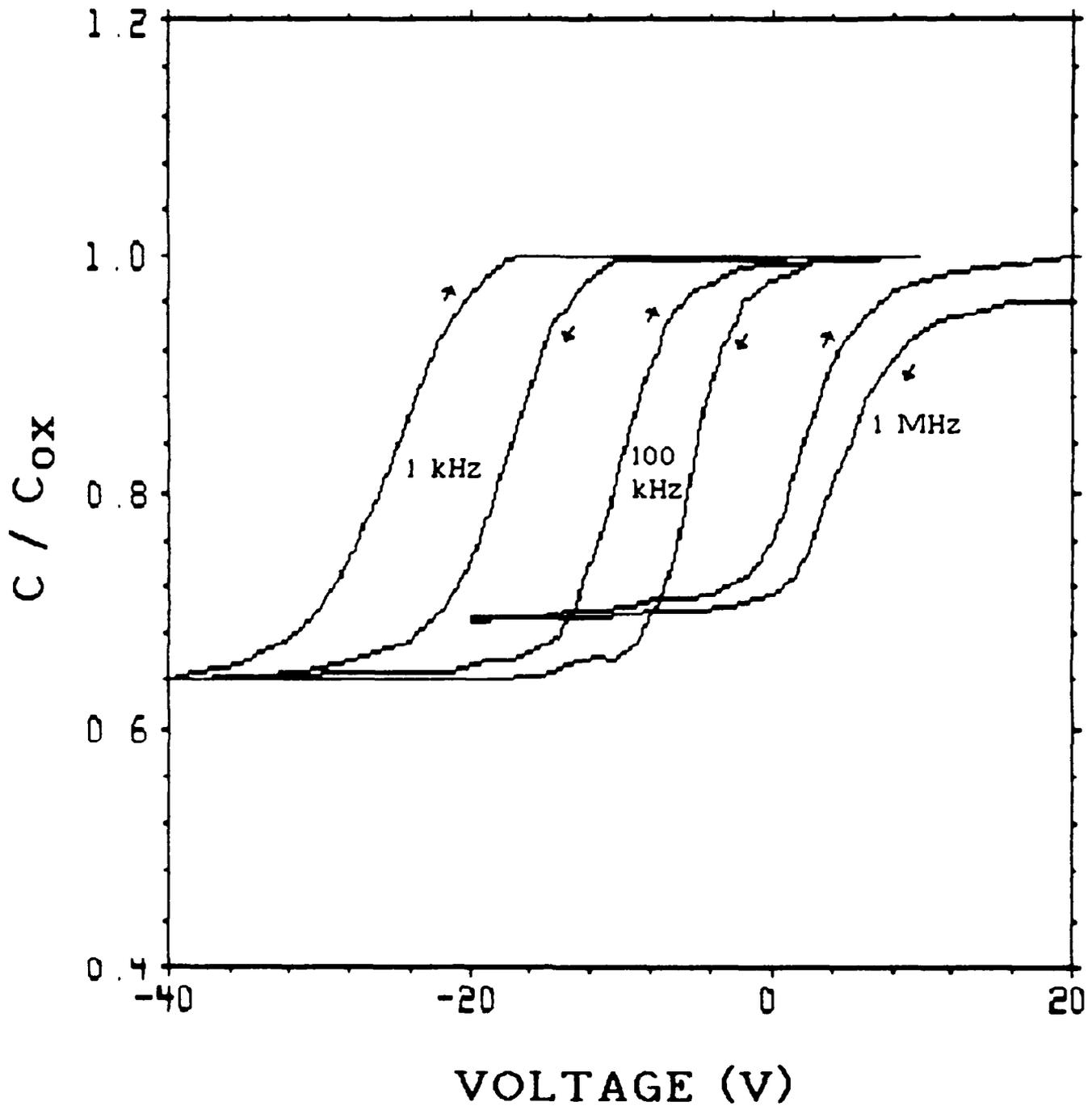


Figure 6. CV curves for a SiN / n GaAs MIS capacitor at several frequencies. The hysteresis and frequency dispersion indicate a large density of surface states at this interface.

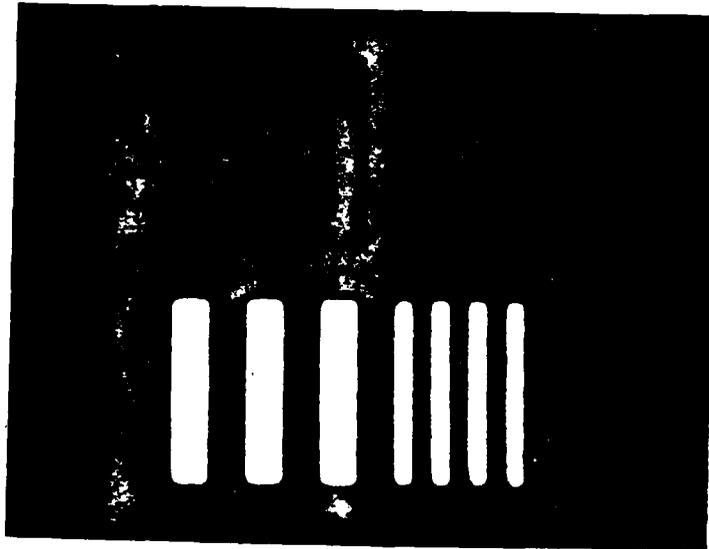
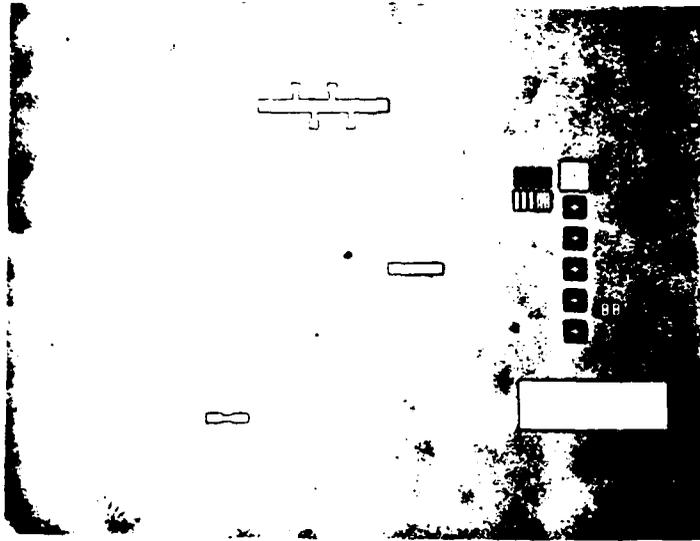


Figure 7. Optical microscope photographs of the ion-implanted wafer after channel lithography. The smallest vertical bars are 5 μm wide with 5 μm spaces.

Appendix I. Fabrication Sequence for Contiguous Domain Oscillator

Starting material: SI GaAs wafer oriented at (100)

Source of GaAs wafer: Sumitomo

Thickness of wafer: 450 μm

Resistivity: $> 10^7 \Omega\text{-cm}$

Clean the wafer before processing

- 1) TCE in the Ultrasonic Clearer for 5 min.
- 2) Methanol in the USC for 5 min.
- 3) Acetone in the USC for 5 min.
- 4) DI rinse(s).
- 5) N_2 blow dry.

Do These Steps ONLY If The Device Is To Be Of The MBE, ETCHED CHANNEL Variety! If not, skip these next steps!

Grow a 1.0 μm buffer layer of P- (10^{15}cm^{-3}) GaAs and then a 0.3 μm thick layer of GaAs doped with Si to a density of $5 \times 10^{16} \text{cm}^{-3}$

Remove In off back side by mounting sample face down on Black Wax and using DMF/ZnCl In etch.

Make sure the back of the wafer is planar by scraping the back with a razor blade while still mounted to the Black Wax.

Remove excess Black Wax with TCE in Ultrasonic Cleaner (USC).

Clean Time: 10 min.

**** Both versions now are processed similarly ****

Deposit AZ1350J-SF positive photoresist

Spin speed: 4400 r.p.m.

Spin time: 40 sec.

Softbake resist

Temperature: 90 C

Time: 15 min.

Expose wafer with level 1 mask (Registration Etch)

Mask Aligner used: Kasper 1:1

Exposure time: 12.5 units

Develop and rinse resist

Develop in AZ Developer 1:1 with DI, Rinse in DI.

Develop time: 30 sec.

Rinse time: 40 sec.

Optically inspect wafer

Hardbake resist

Temperature: 120 C

Time: 20 min.

Etch GaAs (Registration Etch)

Chemical: 485 DI : 10 NH₄OH : 3.5 H₂O₂ (30 Å/sec → 240 sec. = 4 min.)

Rinse: DI 2+ min.

Optically inspect wafer

Strip resist

Chemical: Acetone

Strip time: 5 min.

Optically inspect wafer

Deposit AZ1350J-SF positive photoresist

Spin speed: 4400 r.p.m.

Spin time: 40 sec.

Softbake resist

Temperature: 90 C

Time: 15 min.

Expose wafer with level 2 mask (Channel Definition)

Mask Aligner used: Kasper 1:1

Exposure time: 12.5 units

Develop and rinse resist

Develop in AZ Developer 1:1 with DI, Rinse in DI.

Develop time: 30 sec.

Rinse time: 60 sec.

Optically inspect wafer

Hardbake resist

Temperature: 120 C

Time: 20 min.

"Do This Step For The MBE, CHANNEL ETCHED Version"

Etch GaAs (Mesa Etch)

Chemical: 485 DI : 10 NH₄OH : 3.5 H₂O₂

Etch time: 3 min.

"Do This Step For The ION IMPLANTED Version"

Ion implant Si for the Channel

First implanted species: Si+

Accel. Voltage: 120 kV

Dose: 1.275×10^{12} cm⁻²

Second implanted species: Si+

Accel. Voltage: 30 kV

Dose: 1.4×10^{11} cm⁻²

Third implanted species: Si+

Accel. Voltage: 10 kV

Dose: 7×10^{10} cm⁻²

"**** Both Versions processed similarly ****"

Strip resist

Chemical: Acetone

Strip time: 5 min.

Optically inspect wafer

Deposit AZ1350J-SF positive photoresist

Spin speed: 4400 r.p.m.

Spin time: 40 sec.

Softbake resist

Temperature: 90 C

Time: 15 min.

Expose wafer with level 3 mask (Source/Drain Implants)

Mask Aligner used: Kasper 1:1

Exposure time: 12.5 units

Develop and rinse resist

Develop in AZ Developer 1:1 with DI, Rinse in DI

Develop time: 30 sec.

Rinse time: 40 sec.

Optically inspect wafer

Hardbake resist

Temperature: 120 C

Time: 20 min.

Ion implant Si for source and drains

Implanted species: Si⁺⁺

Accel. Voltage: 200 kV

Dose: 1.46×10^{13} cm⁻²

Strip resist

Chemical: Acetone

Strip time: 10 min.

Optically inspect wafer

Anneal implant(s) with the Rapid Thermal Annealer.

- 1) TCA - Bring to Boil
- 2) TCA - Bring to Boil
- 3) ACE Rinse
- 4) Methanol Rinse
- 5) DI Rinse and Blow dry
- 6) 40 sec. HCl Dip
- 7) DI Rinse and Blow dry
- 8) 5 min. purge of RTA at 12 on flowmeter (Nitrogen)
- 9) 5 sec. @ 900 C

Optically inspect wafer

Pre-Clean the surface for the Nitride deposition

- 1) TCA - Bring to Boil
- 2) TCA - Bring to Boil
- 3) ACE Rinse
- 4) Methanol Rinse
- 5) DI Rinse and Blow dry
- 6) 40 sec. HCl Dip
- 7) DI Rinse and Blow dry

Deposit silicon nitride insulator

Thickness of cap: 800 Å

SiH₄ flow rate: 20 sccm

NH₃ flow rate: 60 sccm

Chamber Pressure: .430 Torr

Platen Temperature: 225 C

RF Power: 50 W

Optically inspect wafer

Deposit AZ1350J-SF positive photoresist

Spin speed: 4400 r.p.m.

Spin time: 40 sec.

Softbake resist

Temperature: 90 C

Time: 15 min.

Expose wafer with level 4 mask (Nitride Mask)

Mask Aligner used: Kasper 1:1

Exposure time: 12.5 units

Develop and rinse resist

Develop in AZ Developer 1:1 with DI, Rinse in DI.

Develop time: 30 sec.

Rinse time: 40 sec.

Optically inspect wafer

Hardbake resist

Temperature: 120 C

Time: 20 min.

Etch the nitride away except for the desired areas.

Etch: Buffered HF

Time: 20 sec.

Optically inspect wafer

Strip resist

Chemical: Acetone

Strip time: 10 min.

Optically inspect wafer

Deposit AZ1350J-SF positive photoresist

Spin speed: 4400 r.p.m.

Spin time: 40 sec

Softbake resist

Temperature: 90 C

Time: 15 min.

Expose wafer with level 5 mask (Alloy Contacts)

Mask Aligner used: Kasper 1:1

Exposure time: 12.5 units

Aid Liftoff with Xylenes soak

Soak: Xylenes

Time: 3 min.

Develop and rinse resist

Develop in AZ Developer 1:1 with DI, Rinse in DI.

Develop time: 30 sec.

Rinse time: 40 sec.

Optically inspect wafer

Hardbake resist

Temperature: 120 C

Time: 20 min.

Evaporate Au:Ge preform

Number of pellets of preform in boat: 3

Evaporation time: 8 min.

Thickness: 1200 Å

Lift-off alloy materials with resist removal

Chemical: Boiling Acetone w/ Room Temp. ACE rinse & DI Rinse

Time: 5 min.

Optically inspect wafer

Alloy contacts

Temperature: 450 C

Time: 2 min.

Optically inspect wafer

Deposit AZ1350J-SF positive photoresist

Spin speed: 4400 r.p.m.

Spin time: 40 sec.

Softbake resist

Temperature: 90 C

Time: 15 min.

Expose wafer with level 6 mask (Resistive Gate)

Mask Aligner used: Kasper 1:1

Exposure time: 12.5 units

Aid Liftoff with Xylenes soak

Soak: Xylenes

Time: 3 min.

Develop and rinse resist

Develop in AZ Developer 1:1 with DI, Rinse in DI.
Develop time: 30 sec.
Rinse time: 40 sec.

Optically inspect wafer

Hardbake resist

Temperature: 120 C
Time: 20 min.

Evaporate Nichrome Resistive Gate material

Evaporation parameters:

Material: Ni-Cr

Measured Resistance at end of evaporation: 250 Ω /square

Lift-off Ni-Cr with resist removal

Chemical: Boiling Acetone w/ Room Temp. ACE and DI Rinses
Time: 5 min.

Optically inspect wafer

Deposit AZ1350J-SF positive photoresist

Spin speed: 4400 r.p.m.
Spin time: 40 sec.

Softbake resist

Temperature: 90 C

Expose wafer with level 7 mask (Top Metal)

Mask Aligner used: Kasper 1:1
Exposure time: 12.5 units

Aid Liftoff with Xylenes soak

Soak: Xylenes
Time: 3 min.

Develop and rinse resist

Develop in AZ Developer 1:1 with DI, Rinse in DI.
Develop time: 30 sec.
Rinse time: 40 sec.

Optically inspect wafer

Hardbake resist

Temperature: 120 C
Time: 20 min.

Evaporate Al top metal
Thickness: 1 μm

Lift-off Al with resist removal
Chemical: Boiling Acetone w/ Room Temp ACE and DI Rinse
Time: 5 min.

Optically inspect wafer

Pre-Clean the surface for the Nitride deposition

- 1) TCA - Bring to Boil
- 2) TCA - Bring to Boil
- 3) ACE Rinse
- 4) Methanol Rinse
- 5) DI Rinse and Blow dry
- 6) 40 sec. HCl Dip
- 7) DI Rinse and Blow dry

Deposit silicon nitride cap
Thickness of cap: 1 μm
 SiH_4 flow rate: 20 sccm
 NH_3 flow rate: 60 sccm
Chamber Pressure: .430 Torr
Platen Temperature: 225 C
RF Power: 50 W

Optically inspect wafer

Deposit AZ1350J-SF positive photoresist
Spin speed: 4400 r.p.m.
Spin time: 40 sec.

Softbake resist
Temperature: 90 C
Time: 15 min.

Expose wafer with level 8 mask (Nitride Cap)
Mask Aligner used: Kasper 1:1
Exposure time: 12.5 units

Develop and rinse resist
Develop in AZ Developer 1:1 with DI, Rinse in DI.
Develop time: 30 sec.
Rinse time: 40 sec.

Optically inspect wafer

Hardbake resist
Temperature: 120 C
Time: 20 min.

Etch off Nitride over bonding pads
Chemical: Buffered HF
Time: 1 min.

Optically inspect wafer

Strip Resist
Chemical: Acetone, NO USC TO BE USED! WILL DAMAGE A!
Time: 5 min.

Optically inspect wafer

Electrical Test

DONE!!

END

DTIC

9-86