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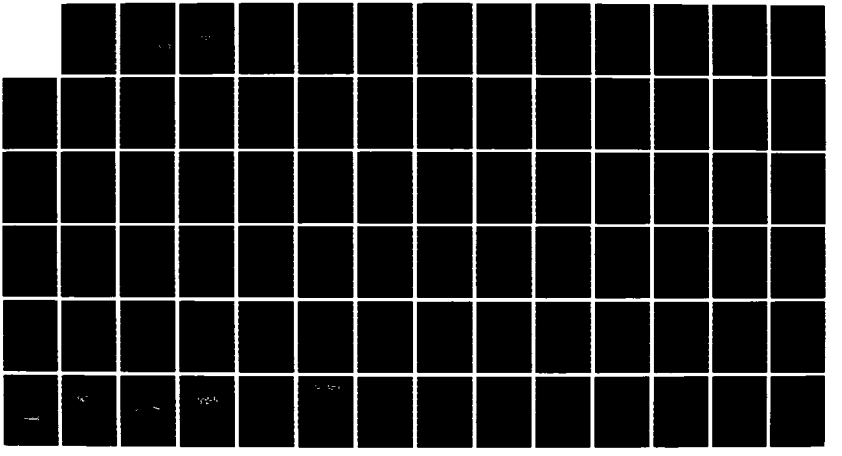

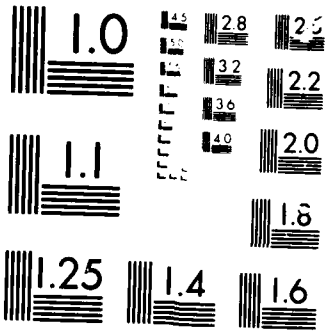
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THE DEPARTMENT OF DEFENSE VERY HIGH SPEED INTEGRATED CIRCUIT (VHSIC) TECHNOLOGY AVAILABILITY PROGRAM PLAN

FOR THE

COMMITTEES ON ARMED SERVICES
UNITED STATES CONGRESS

30 JUNE 1986

THE DEPARTMENT OF DEFENSE

VERY HIGH SPEED INTEGRATED CIRCUITS

(VHSIC)

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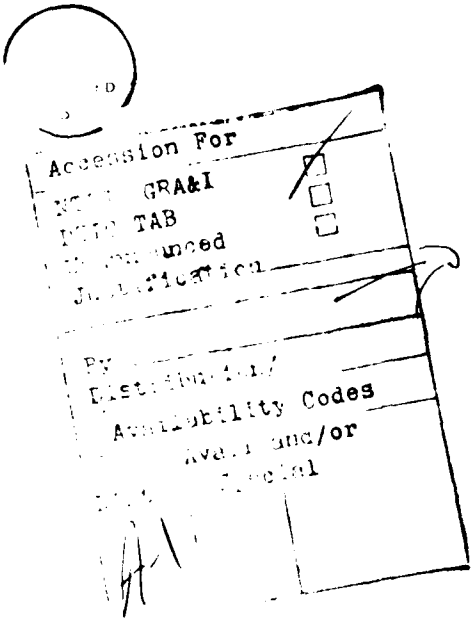

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Per Mr. Vincent Hurteau, OUSDRE/VHSIC Program Office

EXECUTIVE SUMMARY

INTRODUCTION

The House and Senate Conferees on Armed Services requested that the Secretary of Defense "develop a plan to be submitted to the Committees on Armed Services of the Senate and the House of Representatives for a program to ensure that Very High Speed Integrated Circuit (VHSIC) technology is made available to weapon system developers as VHSIC components become available and mature." This report will show in summary form how all of the activities of the VHSIC program are directly aimed at making the most advanced integrated circuit technology available to weapon system developers.

BACKGROUND -

IC Technology is vital to National Defense

Integrated circuit (IC) technology has been described as the "crude oil" of the 80's. Over the past century, the discovery and exploration of oil has led to the development of transportation systems, a major portion of the chemical industry and many other vital technologies. Access to it is vital for national defense. Today, integrated circuit technology is forming a new base for profound and rapid advances in telecommunications, automation, data processing and electronics. IC technology has also revolutionized the concept of weapon system design. For the past three decades, since the invention of the silicon integrated circuit, the western world's free enterprise economies have produced an incredibly rapid rate of advance in IC technology and an explosive growth in industries based on this technology. Given this inherent advantage, the free world has adopted a defense posture based on this

technology which counters numerical superiority in military forces with sophisticated weapons. The outcome of both the Falklands and Israeli-Syrian conflicts have dramatically illustrated how effective a technology edge can be.

Experts in the field of integrated circuits foresee a continuation of the advance in IC technology well into the 21st century. Current weapon systems have become dependent upon their computer and signal processor "brains" to accomplish their mission. Future generations of weapon systems will be wholly dependent on advances in IC technology to continue to counter increased threats in both the conventional and strategic arenas. The President, in his 1986 State of the Union address, stated that "Defense is the prime directive of the Federal Government". Access to and utilization of state of the art IC technology by weapon system developers is a keystone in the free world's defense strategy.

Commercial IC Products Not Readily Adaptable to Defense Needs

Only a few years after the invention of the integrated circuit, the Defense Department began to design weapon systems based upon these new devices. The Minuteman II program in the early 60's committed itself to converting the guidance control computer from germanium discrete transistors to silicon integrated circuits. That decision had two major consequences: first, it enhanced the range and accuracy of the missile; and, second, it provided a production base from which a new industry emerged - the commercial IC industry. Only a few years later, commercial IC requirements dominated product development and products tailored to military applications became less financially attractive to the IC industry. During the 70's the Defense Department adjusted to this situation by adapting standard commercial products

to military end use. This was attractive since it minimized the "front-end" engineering design costs, minimized unit costs and seemed to reduce the need to support R&D.

A decade of this "hands-off" policy, however, led to the acquisition of a variety of programmable device types, proliferation of costly software support systems, and an increasingly difficult, expensive qualification process. Most alarmingly, it led to a serious erosion of the comfortable ten year lead we once enjoyed in deployed military digital processor hardware. Thus the "force multipliers" no longer existed.

VHSIC Program Plan to Make ICs Available to Military Weapon Systems Developers

The VHSIC program was initiated in order to accelerate the insertion of advanced IC technology into military systems. The VHSIC plan consists of the following components:

- Definition of two generations of ICs to set the pace for IC use over the decade of the 80's. This is embodied in first generation VHSIC products, (Phase 1), 1.25 micrometer minimum feature size circuits, and second generation VHSIC products, (Phase 2), 0.5 micrometer mimimum feature size circuits.
- Establishment of requirements and definition of military unique IC designs not available on the commercial market.
- Establishment of pilot production facilities to assure early access to prototype devices for system experimentation and to stimulate private investment thoughout the defense industry.

- Demonstration of "proof of principle" system brassboards to establish credibility with military system developers.
- Substitution of planning for hoping - demonstration of how product planning for the next generation of ICs must take place concurrently with implementation of the current generation in order for rapid utilization in deployed military systems to keep pace with commercial development.

Based on the early success of the VHSIC program, in focusing attention on military IC development, the program was expanded to assure greater availability to weapon system developers with the addition of the following components:

- Technology Insertion - a unique approach to technology transition in which 'joint ventures' with system program offices were established. This is a 'risk reduction' technique, which by 'proof of principle' encourages all weapon system program offices to plan for use of advanced IC technology.
- Yield Enhancement - acceleration of the learning curve in IC fabrication so that lower cost, higher quantity chips are available for sale to military systems developers.
- Design Automation - development of a variety of computer aided design (CAD) tools to upgrade the weapon system developers' ability to rapidly assimilate the latest IC technology.
- Industry wide training of weapon system designers in the use of complex ICs in their systems through VHSIC application workshops which have been held throughout the country

- VHSIC Manufacturing Technology - enhancement of the producibility of VHSIC circuits at an affordable cost.
- Development of a uniform DOD policy on use of ICs in weapon systems which will establish ground rules for weapon system developers and military system acquisition planners to use as a yardstick on what IC technology should be incorporated into their system design to assure that DOD is at the forefront of IC utilization.

VHSIC Is Paying Off

- Establishment of the program has focused attention throughout the weapon system community within DOD and in industrial concerns which provide weapon systems to DOD.
- The early DOD investment has stimulated further investment of over a billion dollars by weapon system developers in state of the art IC facilities to make this vital technology available. Venture capital has also been attracted to provide capability for military ICs.
- Devices are now available for sale to all weapon system developers.
- Over 40 military system programs are actively engaged in technology insertion.
- VHSIC application workshops have trained over 2,500 weapon system engineers, from over 250 companies, on use of the technology.
- VHSIC reliability testing has verified that VHSIC devices exceed reliability goals which are 5 times better than those of commercial practice.
- A comprehensive program to put VHSIC and VHSIC-like parts on the military Qualified Parts List (QPL) is underway.

- The first VHSIC insertion into an operational weapon system was demonstrated in 1985 (AN/ALQ-131).
- Major weapon system programs are publicly announcing that their absolute success is a direct function of VHSIC Technology (e.g. - LHX).
- All Phase 1 Technologies are now being transferred from a R&D base to a production base.
- Radiation hardness test results indicate that all the Phase 1 chips will exceed the goals of Phase 1 program.
- Key advanced avionic program developments (e.g. ICNIA, INEWS, Ultra Reliable Radar, etc.) have fully certified the firm requirements for VHSIC Technology.
- Many weapon system programs are now planning for VHSIC to be in the active inventory before the end of the decade (e.g. AN/ALQ-131, F-15 Central Computer, MK-50 Torpedo, TOW Missile, F-16 Radar Signal Processor, etc.)
- A DOD directive which keeps DOD use of advanced ICs in military weapon systems in step with the emergence of the technology is being put in place.

CHAPTER I

VHSIC RATIONALE AND PROGRAM STRUCTURE

The United States defense posture is increasingly based upon the concept of a military force that is technologically superior to any and all potential adversaries. We must use technology whenever possible to ensure our ability to defend against a potential numerically greater force . The technology of the integrated circuit has become the foundation of the complex electronic systems that are employed as force multipliers in our Nation's defense. It is essential then, that our IC technology remain well ahead of that available to potential adversaries.

In the past, we were able to maintain a comfortable lead in integrated circuit technology. However, by the late 1970's it was determined our "comfortable" lead in IC technology had seriously eroded. As a result, our ability to maintain a superior military force, assisted through the advantage of having sole access to advanced electronic technology, was in question.

One of the major reasons for this erosion was the difficulty DOD experienced in moving state of the art ICs from the design laboratory to military systems in a timely fashion. On the other hand, commercial applications of a given level of IC technology often preceded military applications by several years. This jeopardized the security and integrity of eventual military applications. Military applications had reached a delay time of 8 to 10 years behind commercial applications, rendering military weapon systems obsolete (in technology terms) before a normal, effective logistic life cycle could be achieved. This delay in the insertion of technology by the military was the result of four major obstacles:

1. Military market share in the IC industry had dwindled to approximately 7%, causing IC manufacturers to place a higher priority on commercial needs rather than critical defense requirements.

2. Design costs of military ICs had increased disproportionately with time. Small quantity procurements produced, on average, much higher unit costs compared with commercial ICs.

3. Rapidly evolving IC production technology caused severe logistic support (parts availability) problems for fielded systems.

4. Military system program managers were overly cautious about the risks of applying new IC technology to a developing system while remaining within the constraints of limited program resources and critical schedule requirements.

The goal of the VHSIC program is to reverse this lag in military technology insertion by substituting planning for hoping. A primary challenge for the 1980's within DOD was the development of a family of military unique integrated circuits that greatly enhance our ability to reduce the acquisition time to field these devices in Army, Navy and Air Force weapons systems. DOD also needed to gain the attention and support of industry to ensure development and continued support of these devices. We are highly confident the VHSIC Program is making a major contribution to achieving these objectives by providing the tools for development, production, testing and support of devices that can be fielded quickly and in a cost effective manner.

The next two figures (figures 1 and 2) illustrate the problem of advancing semiconductor technology in an environment of longer acquisition cycles. The following figures (figures 3 and 4) illustrate how the VHSIC program strategy will solve this problem and reduce the time to deploy new technologies in current and future weapon systems.

Figure 1, below, illustrates the life cycle profile of a typical integrated circuit technology. The life cycle is broken into four phases. The first phase is technical development and design. In this phase the level of production is low and gradually increases. During the second phase prototype application systems are developed and the level of production increases rapidly. During the third phase application systems require large quantities of devices and the level of production reaches its highest point. During the fourth phase new generations of IC products enter production driving the demand for the older generation down. It is this phase in which a semiconductor technology is gradually phased out of production and becomes obsolete. The length of time from the beginning of phase one to the end of phase four is currently about four years.

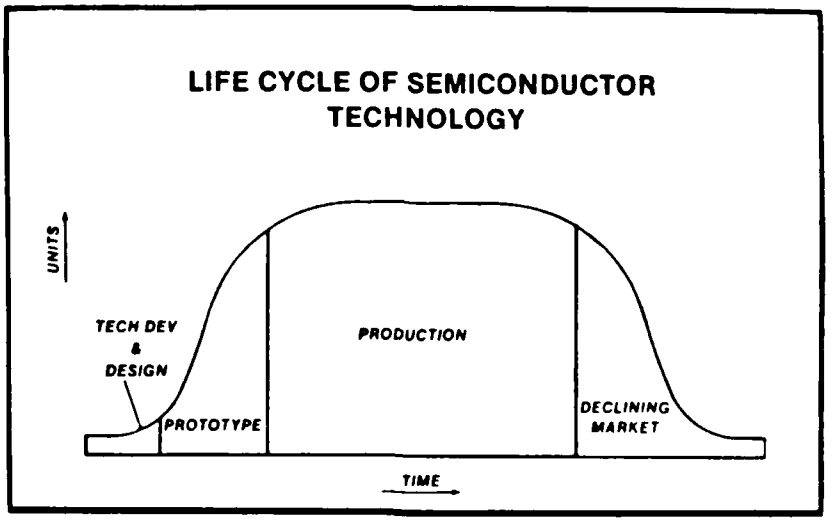


Figure 1

Figure 2 below combines the semiconductor life cycle profile from Figure 1 with the DOD system acquisition cycle. The three technology profiles represent the major semiconductor technologies developed from the late 1960's through the late 1970's. The three system acquisition cycles do not represent any specific systems, instead they represent the trend of DOD system acquisition cycles over the same period of time.

In the late 1960's Small Scale Integration (SSI) was the state of the art in semiconductor technology. As such, it was used in the research and development (R&D) of new DOD weapon systems (depicted as 6.2). As this technology matured, so did the weapon systems. The result was that DOD weapon systems were entering production while the SSI devices were also in production. This DOD acquisition cycle took seven to eight years. Additionally, SSI was used in those weapon systems throughout their operation and support (O&S) life cycles.

In the early 1970's Medium Scale Integration (MSI) was state of the art technology. As with SSI, MSI was used in the R&D (6.2) of new DOD weapon systems. By now however, the typical DOD system acquisition cycle was being interrupted at each milestone (note the gaps between 6.2, 6.3, 6.4 and production). The result of these interruptions was that affected DOD weapon systems did not enter production until MSI semiconductor technology was nearing its declining market. None-the-less, this nearly obsolete technology was carried through production and into the operation and support phase of programs initiated during the early 1970's.

In the late 1970's Large Scale Integration (LSI) was state of the art and was used in the R&D of new DOD weapon systems. The trend of expanding the time required to develop weapon systems continued (note the larger gaps between

6.2, 6.3, 6.4 and production). The result was significant in that it took almost fifteen years to get a new weapon system from concept development into production and the LSI semiconductor technology used in development was then in its declining market, obsolete and generally hard to procure. Again, LSI remained in these weapon systems through production into operation and support.

This is the primary problem that the VHSIC program strategy will resolve.

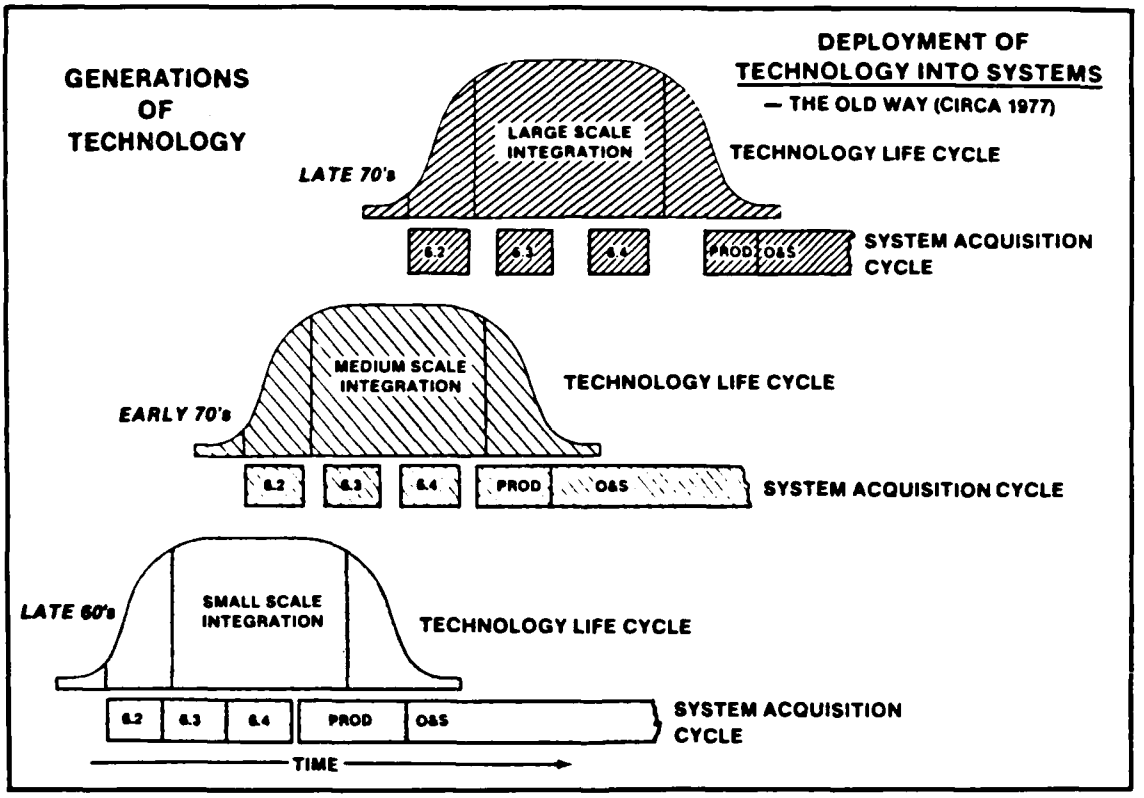


Figure 2

Figure 3 illustrates two major goals of the VHSIC program strategy. First, that state of the art electronic technology; VHSIC Phase 1 now, VHSIC Phase 2 in the next few years, and beyond VHSIC in the 1990's, can be integrated into all DOD weapon systems regardless of their stage in the acquisition cycle (note the vertical integration of new technologies). Second, through aggressive system development and support, the protracted and interrupted system acquisition cycle can be reduced to its original length (note there are no gaps between milestones 6.2, 6.2, 6.4, and production).

The three semiconductor life cycle profiles depicted in figure 3 represent the next three generations of state of the art electronic technology, VHSIC Phase 1, VHSIC Phase 2 and beyond VHSIC. The system acquisition cycles depicted, again do not represent specific systems, instead they represent systems at each milestone from present systems in R&D (6.2) to older systems already in the field and operational.

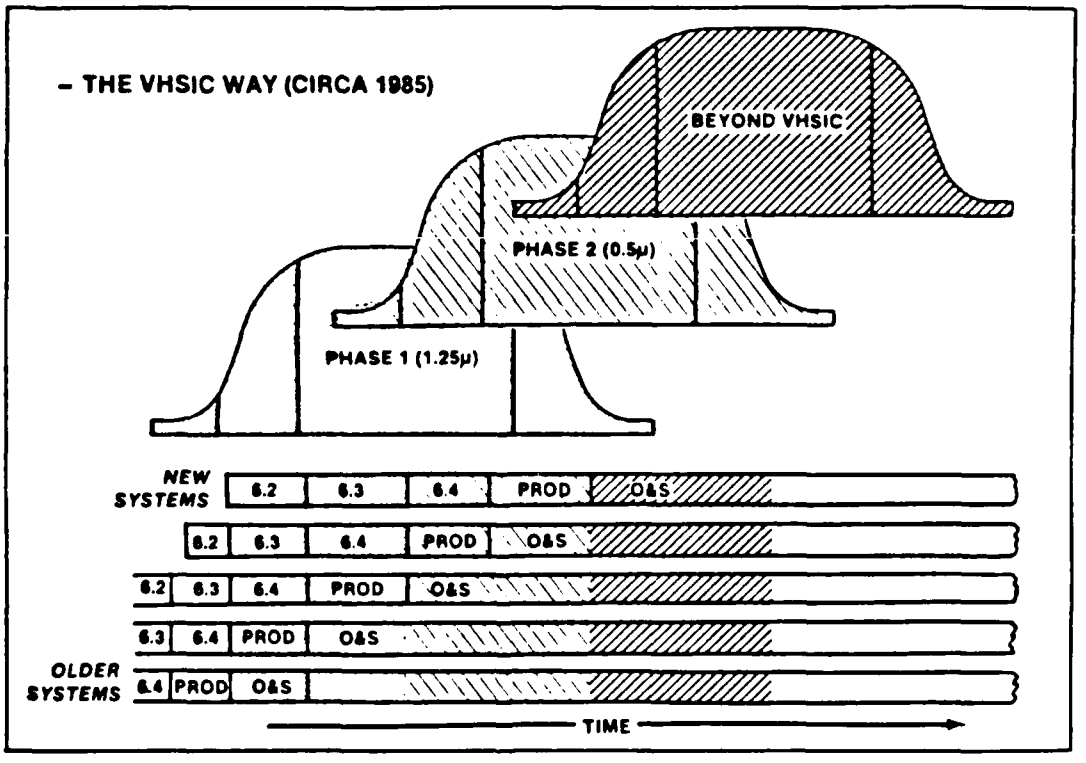


Figure 3

Figure 4 illustrates the previous increasing time required to deploy state of the art electronic technology in military systems and how the VHSIC program strategy is changing this trend. The VHSIC program strategy will allow the U.S. to recover critical years in the deployment of state of the art electronic technology in our weapon systems.

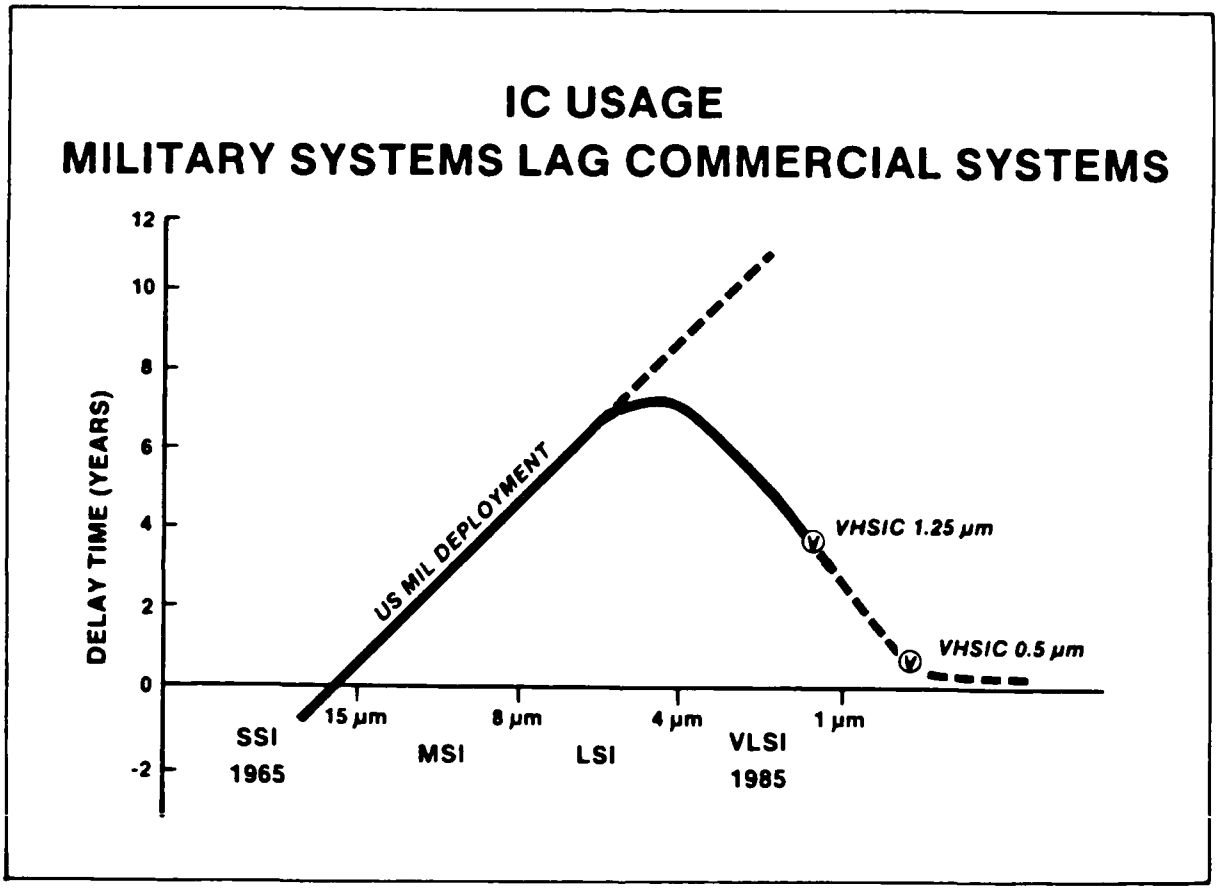


Figure 4

To summarize, there is a distinct and measurable life cycle for each generation of semiconductor technology. The commercial market typically sets the pace at which new generations are introduced. The current pace calls for a new generation of semiconductor devices every four years, although this pace is quickening. For the DOD to deploy state of the art electronics, it must

absorb these new generations of technology into all types of weapons systems in all phases of development. Furthermore, DOD must, in a competitive market place, plan for and lead the development of military specific integrated circuits. The VHSIC program will demonstrate that the DOD can accomplish these tasks.

VHSIC PROGRAM STRUCTURE

DOD recognized that the VHSIC program had to address and solve problems of developing military specific ICs while at the same time maintaining the security and control necessary to prevent compromise of the program and its goals. In 1978, DOD adopted the following management plan to:

Establish the VHSIC Program Office within the Office of the Secretary of Defense supported by similar offices in the Army, Navy and Air Force.

Develop an industrial contracting program for two new generations of advanced integrated circuits specifically designed to meet military system needs and provide the capability to support long term use of the circuits.

Initiate an aggressive technology insertion program which minimizes the financial and schedule risks to the weapon system developer.

Provide leadership and guidance for the semiconductor industry to develop a VHSIC production capability that will continue to meet specific military needs while complementing the commercial goals of semiconductor manufacturers.

The VHSIC Program has been established in the Office of the Under Secretary of Defense for Research and Engineering (OUSDR&E). With the assistance of Program Directors from each of the three Services, the VHSIC Program Director manages overall technical, financial and policy matters. Day-to-day contract management and technical expertise are provided by the three Services, under the leadership of the Service Program Directors. Together they conduct frequent program reviews and monitor the overall technical progress of contractors in each of the various phases of the program. Several other Defense agencies work in cooperation with the VHSIC Program office to assist in solving specific problems.

The VHSIC Program was designed with four complementary phases, structured so that as the technology developed, it could be transitioned directly into production. The program also provides for extensive technology transfer between participating contractors and DOD weapon system developers. Phases 0 and 1 of the program are essentially complete and have been successful.

PHASE 0 - March 1980 to March 1981 Defined specific tasks necessary to develop and produce ICs with 1.25 micrometer minimum feature sizes. Contracts were awarded to nine teams of defense contractors to conduct intensive preliminary studies and then define a detailed development program to accomplish the technical objectives set out by the VHSIC program office.

PHASE 1 - May 1981 to November 1985 Contracted for the development and pilot production of silicon chips with 1.25 micrometer minimum feature sizes and demonstration of associated brassboards. Prime Phase 1 contracts were awarded to six major contractors, or teams, with weapon systems development and semiconductor manufacturing expertise. System

applications addressed by the six brassboards include the following: electro-optical signal processing, anti-jam communications, acoustic signal processing, multimode fire-and-forget missile guidance, electronic warfare and advanced airborne tactical radar.

This phase was expanded to include an aggressive Technology Insertion Program and Yield Enhancement Program. The Insertion Program initially included the requirement for the development of an Integrated Design Automation System (IDAS); however, IDAS is now a separate entity. These expansions to Phase 1 were necessary to ensure sustained and cost effective application of 1.25 micrometer technology.

PHASE 2 - October 1984 to 1989 Will provide for the development and pilot production of silicon chips with 0.5 micrometer minimum feature sizes and for the demonstration of associated brassboards by mid-1988. Three prime contracts for this phase were awarded in October 1984. Early program reviews indicate encouraging progress. System applications addressed by the three brassboards include the following: radar and electro-optic imaging, sonar, electronic warfare and radar applications, and cruise missile, satellite and avionics applications.

PHASE 3 - FY 1980 to FY 1989 Will provide support for various efforts dedicated to solving technical and management problems that arise in pursuit of main program objectives. Specific efforts have been undertaken to deal with technology application, materials requirements, lithography and fabrication tools, design software development, packaging, chip qualification and radiation hardness. Included in this phase is the growing activity for the transfer of VHSIC information and products to the defense community and, in particular, the weapon system developers in industry and government.

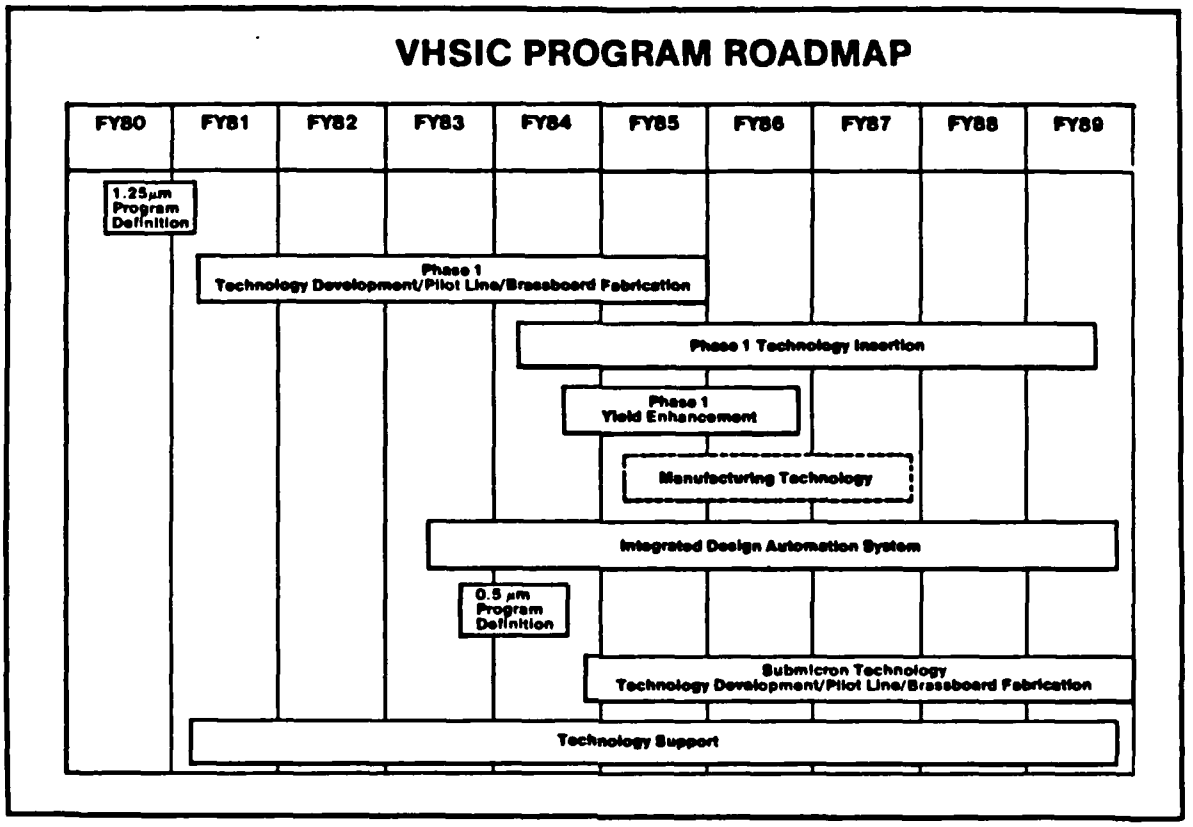


Figure 5

The VHSIC program expresses DOD's confidence in the ability of industry to provide superior IC technology and production capacity for use by the military in a timely and cost effective manner. By establishing the VHSIC program office within the Office of the Secretary of Defense, with full participation of the Army, Navy and Air Force, DOD ensured the support and resources necessary to accomplish program goals. The VHSIC program demonstrates that DOD can field state of the art electronic technology for use in military specific systems in as timely a fashion as commercial IC users field their products, while still providing a fertile market place for U.S. manufacturers. NOTE: The first insertion of VHSIC into an operational weapon system occurred in December, 1985 (AN/ALQ-131 Electronic Warfare Pod).

CHAPTER II

VHSIC TECHNOLOGY

WHAT IS AN INTEGRATED CIRCUIT AND WHAT IS VHSIC?

An integrated circuit is an electronic device which performs one or more digital functions such as arithmetic operations or memory storage in a computer. A typical IC is about the size of a thumbnail. Each IC is designed for a specific set of functions and then manufactured with specific system requirements and constraints taken into consideration. ICs are typically made from very pure silicon with wiring and electronic devices formed on the surface. Current ICs may have more than 300,000 transistors all formed on the surface of a tiny silicon chip. VHSIC chips will ultimately contain as many as 20,000,000 devices.

As our electronic system needs progressed, our ability to manufacture increasingly complex ICs also progressed. The trend in this industry has gone from producing large, simple ICs with devices and wires (features) with dimensions as small as 20 micrometers in the early 1960's, to current production of very small, complex ICs with minimum feature sizes ranging from 2 to 3 micrometers. For comparison, the average human hair is about 60 micrometers in diameter (Figure 6).

The ultimate goal of the VHSIC program is to develop ICs with minimum feature sizes of 0.5 micrometer. This will be accomplished in Phase 2. This program's established intermediate goal of producing ICs with 1.25 micrometer feature sizes was accomplished in Phase 1.

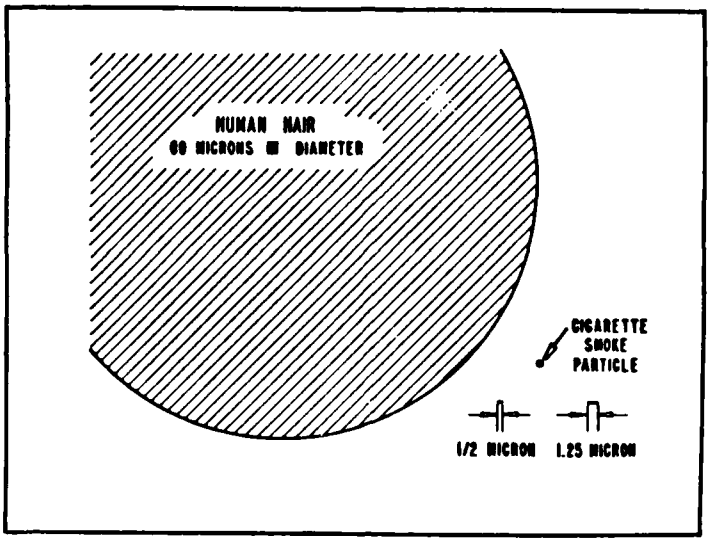


Figure 6

The key elements needed to fabricate such devices are:

- Materials of very high quality including silicon, aluminum, oxygen, boron, arsenic and many others. The term "semi-conductor grade" material has come to be synonymous with the most carefully prepared host material available.

- A patterning process which can define half micron size features on a chip's surface. This is usually a photolithographic process, although electron-beam or X-ray lithography is now becoming necessary to retain sharp definition of the features as they become smaller than optical wavelengths. The 0.5 micrometer dimension of the Phase 2 devices is shorter than the optical wavelength of the color red.

- A set of highly controlled processes for etching, implanting, diffusing, oxidizing, etc. - all of which result in the precise fabrication of the thousands of transistors and wires that constitute the IC.

- A technique for packaging the chip and providing it with accessible terminals so that electrical signals can be sent to and from the chip.

The result is an IC - a small, low power, highly reliable circuit that can perform the electronic functions needed by computers, radars, communication systems, electronic warfare equipments, and the many other information management systems used by our modern society in the conduct of its business and by our modern military forces in defense of that society.

Technical requirements for the VHSIC program were established in Phase 0. Nine contracts resulted in intensive preliminary studies which detailed viable development programs. Technical requirements are detailed below.

- MINIMUM FEATURE SIZE:

  PHASE 1 1.25 Micrometers

  PHASE 2 0.5 Micrometers

- FUNCTIONAL THROUGHPUT RATE:

  PHASE 1 5×10^{11} Gate-Hz/cm^2

  PHASE 2 1×10^{13} Gate-Hz/cm^2

- MINIMUM ON-CHIP CLOCK SPEED:

  PHASE 1 25 MHz

  PHASE 2 100 MHz

o BUILT-IN-TEST: Focused on significant coverage at chip level to provide thorough maintenance and testability capabilities.

o TECHNOLOGY INSERTION: Brassboard designed for system demonstration of each chipset and each type of digital processing technology.

o RADIATION HARDNESS:

PHASE 1	REQUIRED
TOTAL DOSE:	10^4 rad (Si)
DOSE RATE:	10^8 rad (Si)/sec
NEUTRONS:	10^{11} n/cm ^{2}

PHASE 2	
TOTAL DOSE:	$2x10^5$ rad (Si)
DOSE RATE:	10^{10} rad (Si)/sec
NEUTRONS:	10^{12} n/cm ^{2}
SOFT ERROR RATE:	$<10^{-10}$ (errors/bit/day)

o CHIP AVAILABILITY: Second sources for chips to promote a competitive procurement environment. Transfer of design technology and services to qualified defense contractors to encourage continued and widespread development of additional applications of the technology.

CHAPTER III

VHSIC Phase 1

INTRODUCTION

At the beginning of the VHSIC Program (Phase 0 - concept definition) the need was established to set and reach an ambitious yet, seemingly attainable goal of developing and producing ICs with minimum feature size of 1.25 micrometers. Phase 1 subsequently pursued this goal and pushed both the IC design community and manufacturing community to the very edge of known capabilities. Feature size of 1.25 micrometers was chosen for Phase 1 as an intermediate step toward the ultimate program goal of 0.5 micrometer integrated circuits. The 1.25 micrometer technology is in step with current commercial standards. It required improvements in both tooling design procedures and production techniques but is now available for introduction into military systems at the beginning of the technology life cycle (see Fig 3, pg. 12). It also provides system developers with significant improvements in system performance capabilities much more quickly than was possible in recent years. Services have recognized that the Phase 1 chips, design tools and performance capabilities can be applied to a growing array of weapon system and signal processing applications.

TECHNICAL APPROACH

A principal Phase 1 objective was to develop pilot production lines for silicon chips with 1.25 micrometer minimum feature sizes and to demonstrate system brassboards which contained these chips by mid-1984. Prime Phase 1 contracts were awarded to: Honeywell Inc. (Solid State Electronics Division), Hughes Aircraft Company, IBM Corp. (Federal Systems Division), Texas

Instruments, TRW Inc. (Electronic Systems Group), and Westinghouse. System applications addressed by the six brassboards include: electro-optical signal processing, anti-jam communications, acoustic signal processing, multimode fire and forget missile guidance, electronic warfare and advanced airborne tactical radar.

Figure 7 details the Phase 1 contractors, their approaches to accomplishing the Phase 1 goals and the initial Phase 1 chip list.

VHSIC PHASE 1 CONTRACTORS

CONTRACTOR (SUBCONTRACTOR	HONEYWELL	HUGHES (PERKIN-ELMER)	IBM	TI	TRW (SPERRY UNIVAC) (MOTOROLA)	WESTINGHOUSE (NATIONAL) (CONTROL DATA) (HARRIS) (CHU)
TECHNOLOGY	BIPOLAR–CML ISL	CMOS/SOS	NMOS	BIPOLAR–STL NMOS	BIPOLAR–3D I2L CMOS	CMOS/BULK
BRASSBOARD	ELECTRO OPTIC SIGNAL PROCESSOR	AJ COMMUNICATIONS	ACOUSTIC SIGNAL PROCESSOR	MULTIMODE FIRE AND FORGET MISSILE	ELECTRONIC WARFARE SIGNAL PROCESSOR	ADVANCED TACTICAL RADAR PROCESSOR
DESIGN APPROACH	CUSTOM CHIPS BASED ON MACROCELL LIBRARY	CUSTOM RECONFIGURABLE CHIPS	MASTER IMAGE WITH MACROCELL/MICROCELL LIBRARY	PROGRAMMABLE CHIP SET	STANDARD CHIP SET	STANDARD CHIP SET
SPECIAL FEATURES	MULTI SITE CAD NETWORK	HIGHLY SPECIALIZED CHIPS E-BEAM MACHINE DEVELOPMENT	SOFTWARE STRENGTH HIGH DENSITY CHIP DESIGN	OPERATIONAL FABRICATION FACILITY DESIGN UTILITY SYSTEM	INNOVATIVE MEMORY VERSATILE CHIP SET	MULTI-CHIP FUNCTIONAL MODULES ARCHITECTURE
CHIP LIST	PPP PARALLEL PIPELINE PROCESSOR CHIP SEQUENCER CHIP ARITHMETIC CHIP	CORRELATOR CHIP STS SIGNAL TRACKING SUBSYSTEM ENCODER/DECODER CHIP	CMAC COMPLEX MULTIPLY AND ACCUMULATE CHIP	1750A GENERAL PURPOSE PROCESSOR 8K x 8 SRAM STATIC RANDOM ACCESS MEMORY VAG VECTOR ADDRESS GENERATOR ACS ARRAY CONTROLLER SEQUENCER VALU VECTOR ARITHMETIC LOGIC UNIT DIU DEVICE INTERFACE UNIT GBU GENERAL BUFFER UNIT MPS MULTIPATH SWITCH	MATRIX SWITCH CAM CONTENT ADDRESSABLE MEMORY WAM WINDOW ADDRESSABLE MEMORY MAC MULTIPLY ACCUMULATE CHIP 4 PORT MEMORY ADDRESS GENERATOR MICROCONTROLLER RALU-RANDOM ACCESS LOGIC UNIT	10K GATE ARRAY 8K SRAM STATIC RANDOM ACCESS MEMORY PAU PIPELINED ARITHMETIC UNIT EAU EXTENDED ARITHMETIC UNIT EAUM EXTENDED ARITHMETIC UNIT MULTIPLIER

Figure 7

Demonstrated products delivered to date include 1.25 micrometer chips, system brassboards, design tools necessary for further chip development and unique production processes required for chip fabrication. Three contractors were selected to deliver a similar set of products for 0.5 micrometer devices in Phase 2. Phase 2 will be discussed in Chapter V.

The program also called for extensive technology transfer between participating and other qualified contractors.

The technical requirements of the VHSIC Program, as described earlier, call for development of two generations of integrated circuit technology. The VHSIC Program Management Plan instituted to carry out these requirements represented a significant challenge to OSD and the Services since it relied upon true tri-Service cooperation and procurement cycle reduction as the keys to re-establishing the U.S. electronics technological lead. Phase 1 demonstrated that all the goals of the VHSIC Program could be achieved through this unique management process.

The OSD and Services responded with lean, direct organizations connected vertically at each level in the Services and horizontally in the VHSIC community. Each Service Program Director is a member of the VHSIC steering committee. This enhances interaction on issues dealing with day-to-day progress, problem resolution and strategic planning recommendations for OUSDR&E relative to long term VHSIC strategy. Experts from the field and research activities have been pooled; each service has detached personnel to serve in the OUSDR&E organization; and organizations like the Defense Nuclear

Agency participated by providing their unique expertise when necessary. The result is an efficiently managed organization, focused on meeting program goals on time and providing superior defense systems for the Nation.

Industry, as well, has responded to the challenge. Interest and participation in the VHSIC Program continues to be strong. Proposals were received from many semiconductor manufacturers and teams of circuit and system contractors. In addition to the initial program devices, each VHSIC contractor, and many non-VHSIC contractors, have initiated development of new and unique devices. Industry is using the design tools and processes developed by the VHSIC Program to focus this versatile and powerful technology on their best, most innovative ideas for new weapon systems. This is in complete harmony with early desires to let the open market set the stage for the widespread use of this next generation of integrated circuit technology.

Pilot production lines for 1.25 micrometer chips have been established by each of the six contractors and all have demonstrated functional chips. Three of the contractors have completed their entire chipsets and demonstrated system brassboards. Over forty system specific technology insertion programs are underway with some demonstrations already complete. Benefits in improved performance, new capabilities, enhanced reliability and maintainability, reduced life cycle costs, reduced size, weight and power characteristics and profound system flexibility are all easily recognized in these first Technology Insertion programs.

TECHNOLOGY INSERTION

Paramount to the success of the VHSIC Program is the rapid deployment of military systems designed or improved through the use of 1.25 and 0.5 micrometer feature size ICs. The goal of VHSIC Technology Insertion is to ensure that Phase 1 chips, chipsets and brassboards, or similar devices designed with Phase 1 tools, are not only made available to weapon system developers but will, in fact, be used in military systems before the close of the decade.

> "The greatest risk in the VHSIC program, in our judgement, is not that we will fail to achieve the technical objectives, but that we will make a sluggish or incomplete implementation of the technology" Defense Science Board, 1982.

To help reduce this risk, OUSDR&E developed and is managing the Phase 1 Technology Insertion Program. The VHSIC Program office and the Services have jointly selected insertion candidates, and the VHSIC program is providing seed money to share the development costs for systems utilizing VHSIC devices.

Starting in 1983, the Services have been asked each year to select Technology Insertion candidates that could benefit from improved performance capabilities and/or life cycle cost reductions. Candidates are selected for OUSDR&E seed money funding based upon the following criteria:

Early insertion and subsequent deployment.

Strong system program office commitment to the use of VHSIC.

Significant life cycle cost reduction.

Use of VHSIC Phase 1 devices or processes.

Maximize use of generic brassboards.

Access to VHSIC technology and expansion of participation by non-VHSIC contractors.

The Technology Insertion Programs, and their objectives, that have been or are currently being jointly funded by the VHSIC Program Office and the representing Service are described below.

ARMY

PLRS/JTIDS HYBRID (PJH)

- 0 Man Portable Anti-Jam Communications Units, Interfaces with JTIDS
- 0 VHSIC Signal Message Processing Unit
- 0 Enhanced Capabilities, Reduced Size and Weight

The Position Locating and Reporting System (PLRS)/ Joint Tactical Information Distribution System (JTIDS) Hybrid will consist of three major hardware elements. Enhanced PLRS User Units (EPUU), JTIDS Terminals and Network Control Units. VHSIC technology will be inserted into the signal message processor segment of the EPUU to accommmodate upgraded mission requirements while retaining critical portability.

AIRBORNE SIGNAL PROCESSOR FOR LHX

- 0 Army Attack/Scout Helicopter
- 0 VHSIC Avionics and Navigation Processors
- 0 Mission Required Capabilities Unattainable Without VHSIC

Phase 1 VHSIC Technology is being evaluated by each of the five Advanced Rotorcraft Technology Initiative teams to result in an optimum approach to using the capabilities becoming available.

TOW TARGET TRACKER

- O Tube Launched, Optically Tracked, Wire Guided Anti-Armor Missile
- O VHSIC Automatic Tracker
- O Automatic Target Tracking, Multiple Engagement Guidance

A VHSIC based signal processor is being developed that will replace the current guidance set. This will provide improved probability of hit and improved rate of fire capabilities, a critical consideration when the gunner is exposed to counter fire.

TOW WIRELESS COMMAND LINK

- O Tube Launched, Optically Tracked, Wire Guided Anti-Armor Missile
- O VHSIC Wireless Missile Command Link
- O Enhanced Speed/Range Characteristics, Multiple Missile Guidance

The current TOW missile system is range and speed limited by the existing wire guided control system. VHSIC technology will be used to develop a wireless command link allowing improvements in weapon lethality and range.

HELLFIRE FIRE AND FORGET MISSILE

- 0 Laser Guided Anti-Armor Missile
- 0 VHSIC Imaging Infrared Seeker
- 0 Enhanced Performance and Logistics Characteristics

The HELLFIRE anti-armor weapon system currently uses a semi-active laser seeker. VHSIC technology will be used to deploy a modular, high data throughput, low power, light weight processor to provide true fire and forget capabilities.

TARGET ACQUISITION/FIRE CONTROL FOR GROUND VEHICLES

- 0 Fire Control Processor for Present and Future Ground Vehicles
- 0 VHSIC Fire Control, Command, Communications, and Vehicle Status Processor
- 0 Enhanced First Round Hit Probability, Reduced Life Cycle Costs

The generic fire control processor will consist of several VHSIC modules which can be configured as required to accommmodate the processing needs of various types of ground vehicles. Capabilities will include fire control, target designation, command control and communication, maintenance and crew training. The M-1 tank will be the first ground system to test VHSIC fire control technology.

PROGRAMMABLE SIGNAL PROCESSOR (PSP) FOR ARMY AIR DEFENSE RADARS

- 0 Short/Medium Range Air Defense System Radars like SHOMADS
- 0 VHSIC Generic Programmable Signal Processor
- 0 Commonality in Design, In House Custom Software Development, Improved Logistic Support Characteristics

A programable signal processor for Army short and medium range air defense radar systems (SHOMADS) is being developed with current VHSIC technology. Specific capabilities of a VHSIC PSP include high precision tracking of multiple targets in a 360 degree search area, low battlefield signature and high survivability.

FIREFINDER

- 0 Enemy Missile, Artillery and Mortar Locating Radar System
- 0 VHSIC Digital Signal Processor for Operations Control
- 0 Single Vehicle Radar System, Enhanced Firing Battery Characterization

The FIREFINDER radar system consists of an artillery locating radar, a mortar locating radar, a command and control trailer and a power generating trailer. The system is used to locate, identify and track hostile fire and provide reverse azimuth information for counterfire direction. The system can also be used to project the impact point of our return fire for targeting correction. VHSIC technology will be used to reduce the current five vehicle system down to a single vehicle system and reduce crew size from 15 to 7.

MEDFLI

- 0 Remotely Piloted Vehicle for Non-Communication Threat Emitter Identification
- 0 VHSIC Electronic Support Measures Processor and Threat Association Module
- 0 Enhance Complex Emitter Processing, Real-Time Threat Analysis and Logistic Support Characteristics

The miniaturized electronic direction finding locating indicator (MEDFLI) is a remotely piloted vehicle for use in the identification and location of hostile, non-communication emitters. The complex battlefield of the 1990s requires the increased processing speeds and reduced component size available only with VHSIC technology.

NAVY

ENHANCED MODULAR SIGNAL PROCESSOR (EMSP)

- Next Generation Acoustic Signal Processor
- VHSIC Floating Point Arithmetic Processor
- Enhanced Processor Throughput and Future Upgrade Capabilities

The EMSP is the next generation standard Navy signal processor, AN/UYS-2. It will be a high throughput programmable signal processor, developed as a family of modular and configurable functional elements. The modular architecture will permit simple integration of follow on technologies as they are developed.

MK-50 ADVANCED LIGHTWEIGHT TORPEDO

- Next Generation Torpedo for air and surface launched ASW
- VHSIC Receiver/Transmitter and Signal Processor
- Increase Available Volume in Torpedo for Warhead and Propulsion System Improvements

The advanced lightweight torpedo is the next generation torpedo weapon system to counter the evolving Soviet submarine threat. A VHSIC signal processor will provide smaller lighter modules for the receiver/transmitter electronics, command/control electronics and

the AYK-14 onboard computer. Reductions in size and weight of these components will allow for additional warhead and powerplant improvements, thereby improving weapon system lethality.

PSP FOR THE AN/APG-65

- 0 Advanced Multimode Airborne Radar
- 0 VHSIC Programmable Signal Processor
- 0 Enhanced Throughput and Memory Characteristics, Reduced Size and Weight

A programmable signal processor for the APG-65 fire control radar will provide an increase in processing capability for current radar modes and will provide the capacity for additional processing modes. A VHSIC processor will also provide additional memory capabilities and enhanced radiation hardness qualities.

AN/AYK-14(V)

- 0 Navy Standard Airborne Computer
- 0 VHSIC Processor and Memory Expansion
- 0 Enhanced Processing Capability, Reduced Size and Weight

The AN/AYK-14 Navy standard airborne computer is a modular, general purpose computer used in almost all Navy airborne weapon systems including aircraft, missiles and torpedos. VHSIC technology will be used to improve size, weight and performance characteristics such that the computer can be upgraded to meet current and future processing requirements.

HF/EHF COMMUNICATIONS TERMINAL

- O Navy Telecommunications Terminal for Minimum Essential HF/EHF Communications
- O VHSIC HF Processor/Modem and Controller
- O Size/Weight Reductions Necessary and Only Possible With VHSIC

The VHSIC HF/EHF communications terminal will combine the Navy's primary enduring telecommunications capability, EHF, with HF communications as the back up system. Size, weight and processing speed requirements make VHSIC technology essential.

COMMUNICATIONS BRASSBOARD INSERTION

- O Standard Electronic Modules for HF/EHF Communications Systems
- O VHSIC Communications Processor
- O Performance Improvements and Enhanced Flexibility for Varied Configurations

This effort is aimed at packaging the TRW communications brassboard in a standard electronic module format and will provide the basis for future packaging of HF/EHF terminals for use in aircraft and other space limited platforms.

ADVANCED ANTI-RADIATION MISSILE (ARM) SIGNAL PROCESSOR (AASP)

- O Air Launched Anti-Radar Missile
- O VHSIC Signal Processor
- O Enhanced Processor Throughput and Memory, Avionics/Missile Interface and Life Cycle Cost Characteristics

Future anti-radiation missile systems will face a variety of new and complex electronic challenges. High pulse rate densities and multi-mode phased array pulse doppler radars will require AASP systems to process more data more quickly. VHSIC technology offers the capabilities required for this next generation requirement.

AIR FORCE

AN/ALQ-131

- Electronic Warfare POD
- VHSIC Transmit/Control Assembly
- Enhanced Reliability/Maintainability

The AN/ALQ-131 electronic warfare pod is a modular electronic countermeasures system providing protection for tactical aircraft against threat radars. VHSIC technology is being used to provide substantial maintainability and availability improvements. In December 1985, this program was the first demonstration of VHSIC Phase 1 technology in an operational weapon system.

AUTONOMOUS GUIDED WEAPONS (LAUNCH AND LEAVE GUIDED BOMB)

- Next Generation Stand-Off, High Value Target Guided Bomb
- VHSIC Imaging Infrared Seeker
- Autonomous, Lock-On After Launch Capability

The launch and leave guided bomb is a stand-off weapon which employs an infrared seeker for high value target acquisition and tracking. VHSIC technology will be used to provide an advanced seeker that can

lock on its target after launch, proving a true stand-off capability wherein the delivering aircraft can remain much farther away from the target.

COMMON SIGNAL PROCESSOR

- O Modular, Flexible Digital Signal Processor
- O VHSIC Signal Processor
- O Flexible to Meet Electronic Warfare, Radar, Communications and Electro-Optical System needs

The common signal processor (CSP) program offers the opportunity to develop a modular VHSIC based digital signal processor system. This system is being designed from the ground up with VHSIC technology.

MIL-STD-1750A GENERAL PURPOSE COMPUTER

- O General Purpose Computer
- O Entirely VHSIC Design
- O Provide Common, Powerful Computer for Tactical Systems

This program will result in a VHSIC general purpose computer using the Air Force MIL-STD-1750A instruction set architecture. The eventual applications include the common signal processor, Pave Sprinter, Pave Pillar, ICNIA, ATF and many others.

PAVE SPRINTER

- O Advanced Modular Avionics Subsystem
- O VHSIC CSP and General Purpose Computer
- O Enhanced Performance and Support Characteristics

PAVE SPRINTER is a modular avionics demonstration program. It marries VHSIC technology with ICNIA/Pave Pillar architectures and provides the opportunity for an early demonstration of a highly modular system with wide application to varied weapons systems and missions.

AUTOMATIC TARGET RECOGNIZER

- Imaging Sensor Autoprocessor For Use With Advanced Target Acquisition Sensor
- VHSIC Electro-Optic Signal Processor
- Enhanced Automatic Target Detection, Ranging, Tracking and Classification

This effort will result in a VHSIC Imaging Sensor Autoprocessor (VISA) for demonstration in automatic target recognition activities. The system will be able to automatically recognize and classify targets such as tanks and trucks. The VISA will allow for integration of second generation FLIR technology as well.

ADVANCED ON-BOARD SIGNAL PROCESSOR (AOSP)

- Array of Mutually Asynchronous Processing Elements For On-board Communications, Radar and Electro-Optical Processing
- VHSIC Radar and Communication Processing Elements
- Required Size and Weight Constraints Possible Only With VHSIC

The AOSP is a general purpose array of processing elements that are interconnected and combined to do asynchronous processing. It

features ultra high reliability, flexibility, multi-mission performance and growth potential. The AOSP is a critical technology for future space applications.

MILSTAR TERMINAL MODEM PROCESSOR

- O EHF Satellite Communication System
- O VHSIC Terminal Modem Processor
- O Reduced Size and Weight Characteristics, Allows Use Where Current Devices are Otherwise Too Large

This effort will develop and demonstrate a MILSTAR terminal modem processor with VHSIC technology. This joint Navy/Air Force program will result in satellite communications devices for use in platforms where size and weight are critical.

SPEECH ENHANCEMENT UNIT

- O Advanced Development Speech Processor
- O VHSIC Speech Enhancement Unit Modules
- O Remove Noise From Speech Channels, Reduce Size and Weight

VHSIC technology will make possible speech enhancement for use in voice recognition equipment and voice actuated control systems in areas where current speech recognition technology cannot operate. Cost, size, weight and power requirements are leading areas of improvement with the application of VHSIC technology.

ALR-56 RADAR WARNING RECEIVER (RWR)

- O F-15 Threat Radar Warning Detector
- O VHSIC MIL-STD-1750A, Advanced Memory and Data Processing
- O Enhanced Screening and Histogramming Functions, Improved Logistic Support Characteristics

The ALR-56 RWR is used to detect ground based and airborne threat radar emissions so the pilot can locate, identify and evade enemy radar installations. The prevalent opportunity for VHSIC technology in the ALR-56 is a significant improvement in processing capability required for the evolving threat environment.

F-15 CENTRAL COMPUTER

- O F-15 Pilot Display, Weapon Launch and Aircraft System Computer
- O VHSIC Line Replaceable Modules
- O Enhanced Performance and Repairability

The F-15 central computer controls pilot displays, weapons launch solutions and the aircraft G-load warning system indicator. VHSIC technology will be used to develop a line replaceable unit that will greatly improve the computer's maintainability and availability.

F-16 PROGRAMMABLE SIGNAL PROCESSOR (AN/APG-68)

- O AN/APG-68 Fire Control Radar Set
- O VHSIC Programmable Signal Processor, MIL-STD-1750A
- O Reduced Size, Weight and Power Requirements, Reduced Life Cycle Cost

The APG-68 is the fire control radar for the F-16 aircraft. It provides air to air target detection and tracking as well as information for weapons selection and status. The radar programmable signal processor will contain VHSIC array processors memory devices and an integrated power supply.

LOGISTICS RETROFIT ENGINEERING

- Retrofit Engineering Capability to Replace Unavailable Integrated Circuits
- VHSIC Computer Aided Design and Engineering Tools
- Extend, Improve Operational Life and Effectiveness of Systems, Otherwise Obsolete Due to Lack of Spares

Often, electronic devices become unavailable in the spare parts sources pipeline. This effort is aimed at developing a generic capability to design and retrofit operational systems using VHSIC Phase 1 technology when older components are no longer available.

MODULAR AUTOMATIC TEST EQUIPMENT

- Perform Operational and Maintenance Testing of Avionics, Electronic and Electro-Mechanical Systems
- VHSIC Design Entirely
- Allow for "Suitcase" Testers at the Organization, or Squadron, Level

Automatic test equipment is often very large and harder to maintain than the systems for which it is designed to test. Mobility and acquisition requirements are driving developers to assess the

applicability of VHSIC technology to automatic test equipment. The goal of suitcase size testers can only be achieved with the application of VHSIC technology.

VHSIC REPLACEMENT FOR 54XX TTL CIRCUITS

- All Systems Containing Transistor-Transistor-Logic Devices
- VHSIC Computer Aided Design Tools and Standard Devices
- Improved Supportability of Systems Containing TTL Devices That Are No Longer Manufactured

This is a specific application of VHSIC technology to replace a semiconductor technology that is rapidly becoming impossible or very expensive to acquire. Transistor Transistor Logic (TTL) circuits are in many operational systems, and the development of a VHSIC gate array for general purpose replacement will mean many more years of operational life for these critical systems.

MIL-STD-1750A FOR SPACE APPLICATIONS

- Generic Spaceborne Computer
- VHSIC MIL-STD-1750A
- Introduction of a Radiation Hard, High Power Generic Processor Comparable to Non-Radiation Hard Processors in Performance

The Air Force MIL-STD-1750A architecture has multiple space applications. For this reason, a generic spaceborne processor is being developed that will provide the same VHSIC capabilities under space radiation hardness conditions.

SUPPORTING SUBPHASES

The VHSIC program also calls for the development of necessary design, production, software, testing, packaging and qualification products. Each of several subphases will ensure that the knowledge necessary to go forward with production and deployment of advanced integrated circuit technology is developed.

Specifically, these subphases include:

YIELD ENHANCEMENT AND MANUFACTURING TECHNOLOGY

LITHOGRAPHY AND MATERIALS

CHIP QUALIFICATION

RADIATION HARDNESS

INTEGRATED DESIGN AUTOMATION SYSTEM

YIELD ENHANCEMENT AND MANUFACTURING TECHNOLOGY

To support the technology insertion efforts, substantial Yield Enhancement and Manufacturing Technology programs have been initiated. The first is aimed at increasing the yield of the Phase 1 pilot production lines at least ten-fold in order to reduce the cost of the VHSIC chips. This program will also ensure Phase 1 chip availability to the present and future weapon systems planning to utilize the technology. The goals and current status of the yield enhancement efforts are summarized in the table below:

	YE Goal*	Accomplishment
Honeywell		
Sequencer (136,000 devices)	13.6%	25%
Hughes		
Correlator (45,000 devices)	10%	7.5%
IBM		
CMAC (101,000 devices)	4%	8.4%
SPE (20,000 devices)	12%	35%
TI		
72K SRAM (465,000 devices)	12%	69%
ACS (170,000 devices)	11%	21%
TRW		
CAM (66,000 devices)	6.6%	4.7%
WAM (58,000 devices)	5.7%	20.5%
Motorola		
4PM (59,000 devices)	8.8%	7.9%
Westinghouse/ National		
64K SRAM (400,000 devices)	10%	25%

* Represents wafer probe, best production lot at this time (June 1986).

The Army, Navy and Air Force were directed to implement a total of $90M of Manufacturing Technology (MT) program funding to directly support future production of VHSIC components. To date, $37.6 M of these efforts have been initiated. This program is being closely coordinated in time and topic with the VHSIC Yield Enhancement program and will provide the means for translating all the VHSIC efforts into a broad, affordable, national industrial capability.

LITHOGRAPHY AND MATERIALS

One area where keystone manufacturing equipment had to be developed for the VHSIC program was the 0.5 micrometer lithography tools for Phase 2. Electron beam lithography equipment has been successfully developed and an x-ray step and repeat machine will be prototyped later this year.

A second key area of investment is the Laser Pantography project being supported jointly by DOD and DOE (Department of Energy) at Lawrence Livermore National Laboratory. This project has already demonstrated much of the technology required for eventual wafer scale signal processors, including the ability to program gate arrays at 2 micrometer line widths, the ability to remove large amounts of heat from "silicon circuit boards", the ability to re-planarize surfaces of interest and the ability to write lines in real time on wafers for interconnect. By the end of the VHSIC project, the Laser Pantography project should provide DoD with a much needed capability to rapidly prototype both gate array and signal processor designs.

The VHSIC Program has initiated efforts to develop improved semiconductor starting materials. Lithography research has focused on electron beam and X-ray techniques.

CHIP QUALIFICATION

The VHSIC Qualification Program is a two step program. In the first step a representative chip from each contractor will be subjected to established military standard qualification requirements. This will test the basic integrity of each supplier's process and design system. By meeting the MIL-STD requirements the supplier will demonstrate his ability to provide microcircuits that meet the quality and reliability requirements essential to any weapon system intended for world wide deployment. The second part of the qualification program is aimed at assuring potential users that all members of a chip set are (and will continue to be) equally suited for insertion into military systems. This step of the VHSIC qualification program will include revision of the military standards, where necessary, to make the qualification requirements more efficient and responsive to the government's need for complex military application of specific parts while at the same time allowing for the advantages of design for quality features of computer aided design systems and statistical quality control procedures that are generic to chip sets and processes.

RADIATION HARDNESS

The VHSIC Program Office is working closely with the Defense Nuclear Agency on radiation hardness issues relative to both Phase 1 and Phase 2 device requirements and development.

Phase 1 development was expanded to include the requirement to establish and demonstrate tactical level radiation hardness for all the devices. All the Phase 1 contractors have met these requirements, and some have exceeded

them by a significant margin. Space level radiation hardness capabilities will be developed for those Phase 1 technologies which best lend themselves to space applications.

INTEGRATED DESIGN AUTOMATION SYSTEM

The long term approach to designing systems which include chips of the Phase 1 (25 MHz, 30K gates, 500K transistors) and Phase 2 (100 MHz, 100K gates, millions of transistors) complexity requires the concurrent development of an Integrated Design Automation System (IDAS). As a first step, a common design language has been established for use by designers at all levels of system development. The VHSIC Hardware Description Language (VHDL) and a framework sufficient to acquire and manage design information throughout a system's life cycle is the goal of the design automation task of the VHSIC program.

VHDL efforts are concentrating on tools for design from the system level down to modules/boards and chips. Tools are becoming available that allow designers to write an algorithm for an implied structure and then to synthesize an architecture that will run the initial algorithm. By doing this, designers can determine, through simulation, early in development if the projected architecture will perform the desired functions adequately. Approximately $15 million is being invested in VHDL through 18-20 small development contracts.

The problem of establishing a common framework to acquire and manage design information is being approached from the standpoint of establishing a standard design/system interface for each level of design and across all types

of systems. This will serve to establish a powerful database for design of VHSIC systems as well as to allow for effective design configuration management of these highly complex systems throughout their entire life cycle.

These design automation aides are a key element of making VHSIC available to system developers. Simulation and synthesis software tools allow the system designer to rapidly assimilate new chip technology into weapon system capability.

Design automation accomplishments to date:

- o VHSIC Hardware Description Language developed.
- o VHDL adopted as an IEEE standard.

Programs underway

- o Silicon compiler for National Semiconductor and Honeywell processes.
- o Microcode compiler.

CHAPTER IV

VHSIC Training and Policy

The VHSIC Program Office, from the outset, recognized that the transfer of VHSIC technology and products to both the DOD contractor community and DOD acquisition managers is essential for program success. It also recognized that historically this had been a difficult task to achieve. Novel approaches were needed to ensure that system designers would not only have access to VHSIC technology, but also to VHSIC software and devices as quickly as they became available. Part of this effort is being carried out in the military weapon system technology insertion projects described in chapter III. An additional part of this effort is the VHSIC Training and Policy Program. It is planned that this effort will perpetuate the long term national goals of the VHSIC program. The VHSIC Training and Policy Program was started in January 1984 and has been structured as a three part effort:

Part I	1984-1986	Awareness and Initial Training
Part II	1986-1988	Extended Training and Policy Development
Part III	1988-	Institutionalization of VHSIC Technology for System Development and Acquisition

PART I: Awareness and Initial Training

The objective of Part I of the VHSIC Training and Policy Program was to provide for initial education and training during which:

- o System managers and senior engineers were made aware of VHSIC products and design technologies being developed. The primary technique used has been through regional workshops but has also included conferences, presentations, and brochures.

- o Working level engineers were trained in the design of systems using VHSIC products through hands-on design workshops. For these workshops VHSIC has developed special software for using VHSIC design tools and has prepared detailed technical reference material in the form of application notes, performance data, and text books.

A. Workshops

VHSIC Application Workshops have been prepared and held throughout the country on a regional basis. The workshops continue to provide comprehensive training and education in VHSIC technology for defense contractor personnel to accelerate the application and insertion of VHSIC technology into military electronics. A list of all the workshops held and those scheduled for the near future is shown below.

The scope and depth of coverage of VHSIC technology at these workshops has enabled each attendee to evaluate the feasibility of using VHSIC technology in specific military system applications. Attendees are given the opportunity to present both application and work-related problems which are discussed by the group in terms of how VHSIC can be applied. The attendees are provided approximately three days of instruction using text material which they take with them for future use in electronic design and interface with the VHSIC community.

The instructional material includes:

- o Student Guide - a compilation of VHSIC design data and chip architectures; used as the text material by the workshop instructors.

- o VHSIC Specification Guide - an abbreviated version of all of the VHSIC chip specifications.

- o Interface Reference Guide - a collection of technical and management information about ICs, Computer Aided Design (CAD) availability, documents available, as well as key government and industry personnel.

A number of similar workshops have been held for DOD and other government personnel at such in-house facilities as the Naval Ocean Systems Center (San Diego), the Naval Weapon Center (China Lake), Eglin Air Force Base (Florida) and NASA's Johnson Spaceflight Center (Houston).

VHSIC APPLICATIONS WORKSHOPS

1984 - 1985

	SITE	DATE
1	The Lockheed-Georgia Company/ Georgia Tech Microelectronics Research Center, Atlanta, Georgia	April 1984

	SITE	DATE
2	The Environmental Research Institute of Michigan, Ann Arbor, Michigan	May 1984
3	Northrop Corporation Anaheim, California	May 1984
4	Grumman Aerospace Bethpage, New York	June 1984
5	E-Systems Dallas, Texas	June 1984
6	Lockheed Missiles and Space Co. San Francisco, California	July 1984
7	The Colorado/Wyoming Chapter of the American Defense Preparedness Association	July 1984
8	Johns Hopkins University Applied Physics Laboratory Laurel, Maryland	August 1984
9	Litton Data Systems Los Angeles, California	August 1984
10	The Mitre Corp./ Raytheon Company Boston, Massachusetts	October 1984
11	Gould, Inc. Chicago, Illinois	October 1984
12	Martin Marietta Orlando Aerospace Orlando, Florida	November 1984
13	The Boeing Aerospace Company Seattle, Washington	February 1985

	SITE	DATE
14	McDonnell Douglas Astronautics Company St. Louis, Missouri	March 1985
15	Sanders Associates, Inc. Nashua, New Hampshire	April 1985
16	Johns Hopkins University Applied Physics Laboratory Laurel, Maryland	June 1985
17	RCA Princeton, New Jersey	September 1985
18	United Technologies Microelectronics Center, Colorado Springs, Colorado	October 1985
19	Rockwell International Anaheim, California	November 1985
20*	NAVAL Ocean Systems Center San Diego, California	March 1984
21*	National Aecronotics and Space Administration Johnson Space Center Houston, Texas	November 1984
22*	NAVAL Weapons Center China Lake, California	January 1985
23*	US Army LABCOM Ft. Monmouth, New Jersey	October 1985

	SITE	DATE
24*	Ford Aerospace Newport Beach, California	October 1985
25*	Eglin AFB	March 1986
26	General Dynamics San Diego, California	April 1986
27	Lockheed Plainfield, New Jersey	May 1986
28*	Wright-Patterson AFB Wright-Patterson AFB, Ohio	June 1986
29	Johns Hopkins University Applied Physics Laboratory Laurel, Maryland	August 1986
30	Rockwell International Anaheim, California	November 1986

* Indicates an in-house conference for host facility personnel.

A major follow-on effort to the Applications Workshops has been developed and was initiated in June 1985. It is called "Applications II" and is intended for those system designers who have attended the regional workshops. It builds on their knowledge from earlier workshops and concentrates exclusively on how to design electronic components using VHSIC products. This two day training program allows hands-on use of some of the CAD tools developed for the VHSIC Program. Four Applications II workshops have been held.

B. Conferences

Each year, in December, the VHSIC Program Office holds a VHSIC Conference to which a broad representation of defense industry managers are invited. This three day meeting is structured to present industry with an update report on the status of the VHSIC program and an indication of the directions and plans for the next year. The meeting is well attended; in addition to discussions of VHSIC technology issues, the concerns of system designers who are not VHSIC contractors are openly discussed.

C. Brochures

In order to bring an awareness of the VHSIC program to as wide a group of industrial and DOD people as possible, a semi-technical brochure has been prepared and distributed. The brochure describes the purpose, the content and the goal of the VHSIC program. It stresses the potential for widespread application of the technology and hence the need for widespread participation of system developers in using the technology. Approximately 5,000 of these brochures have been printed and distributed throughout the defense community.

PART II Extended Training and Policy Development

As a result of the Awareness and Initial Training efforts described as PART I, a number of adjunct activities are being undertaken.

- Applications Workshop efforts are being followed up with increasingly detailed technical design information and data. As they reach the detailed design of specific systems, design level

engineers need both tools and data which will allow them to determine specifications, performance, cost, configuration and reliability of a system and its components.

- o A larger number of people at both the technical and the managerial level are being made aware of the content, the products and the advantages of VHSIC technology.

- o Information generated by the VHSIC program has become sufficiently voluminous and complex that a formal system is being devised to organize it for most effective use by managers and engineers.

The following specific efforts are being taken:

A. Extended Training

VHSIC Seminars/Courses:

a.) Production of a one hour multi-media briefing for use at Service schools, defense contractor facilities, and System Program Offices. This briefing is designed to serve both as an introduction to VHSIC and a means to provide information on gaining access to VHSIC design data.

b.) A three hour multi-media presentation for middle managers, in both industry and in the government, which covers more technical detail and serves to suggest specific areas of

application that could be served by VHSIC technology. This presentation is scheduled to be available in 1986.

c.) The development of a two day technical seminar on VHSIC design software. The seminar will cover software availability and how it can be used. As part of this effort a Rule Based Format Translator is being developed which provides for translation between various VHSIC software design tools and selected engineering graphic work stations. The translator will enable a system designer to learn how to put VHSIC design tools to use in solving his particular design problems.

d.) The sponsoring of a two day seminar at the Naval Post Graduate School (Monterey) on VHSIC signal processing. This seminar is intended to highlight the increase in signal processing throughput and system performance improvements that can be gained from VHSIC technology.

e.) As a result of the impetus provided by VHSIC education programs a number of independently sponsored courses are being offered which focus on specific areas of VHSIC design methodology. One course on the VHSIC Hardware Design Language is offered by the Air Force Institute of Technology (AFIT). A second course is being scheduled by the Johns Hopkins Applied Physics Laboratory on the use of VHSIC in the design of high speed parallel processors.

On-Site Training Kit/VHSIC Text Book

In order to reach a much wider group of design level engineers, an On-Site Training Kit is being developed. The kit consists of much of the written material distributed at the Applications Workshops but with the texts expanded so that the kit may be used independently. Additionally, a textbook is being prepared which will cover the system level engineering details of how to design a system using VHSIC ICs.

VHSIC Data Base

The management and technical data base being generated by VHSIC Program efforts is very large. A centralized information system is in development to organize this data and provide access to it by the entire defense community. This data base is an on-line system that will be available 24 hours a day, seven days a week. With the relational data base presently residing on a DEC VAX 11/780 computer, the data base structure will consist of the following eight areas:

- Personnel
- Integrated Circuits
- Applications
- Technical Documents
- Projects and Contracts
- Briefing Materials
- Software Tools
- Training

The data base is menu driven and highly interactive. The complete data base is intended to be operational by the end of 1986 at which time the most up-to-date versions of VHSIC IC specifications will be accessible, as well as current chip availability and cost data.

Regional Workshops

In addition to the extended training and education efforts described above, industrial and in-house Applications Workshops will be conducted as interest requires.

B. Policy Development

The wide spread use of VHSIC technology in military systems will have a profound impact on the process by which DOD acquires its weapon systems. New procedures must be implemented for the detailed specification of hardware and software components, the standards by which these components are tested and qualified for military use and the specification and control of the logistics pipeline from manufacturer to field depot to fielded system and back. A policy stance must be adopted which supports the advances in military capability offered by VHSIC Technology.

The development of a DOD directive for the use of state of the art/VHSIC technology in weapon systems has begun. Supporting high level statements have already been issued by the Army, Navy and Air Force. Additionally, each Service is preparing a VHSIC Technology Transition Plan in accordance with specific service needs. Draft versions of the Army, Navy and Air Force Transition plans have been prepared. Final versions for all three Services should ready be in 1986.

PART III Institutionalization of VHSIC

By 1988 it is expected that the actions taken during Parts I and II of the VHSIC technology availability program plan will provide a sound basis for the orderly and routine application of Phase 1 VHSIC products to military systems. They will provide the framework for the introduction of newer Phase 2 VHSIC products scheduled to be available at that time. As a means of institutionalizing this process, a VHSIC Information Analysis Center (IAC) will be proposed.

The VHSIC IAC would be organized in accordance with DOD Regulation 3200.12-R-2 which defines an IAC as follows:

> "A Center for Analysis of Scientific and Technical Information is a formal organization with a primary mission to acquire, digest, analyze, evaluate, synthesize, store, publish, and provide advisory and other user services concerning available worldwide scientific and technical information and engineering data in a clearly defined specialized field or subject area of significant DOD interest or concern. Information Analysis Centers (IACs) are distinguished from technical information centers and libraries whose functions are primarily concerned with providing reference or access to the documents themselves rather than the information contained in the documents."

The VHSIC IAC would meet DOD and Defense Contractor needs insuring that VHSIC technology and product information is made available to weapon system developers in a cost effective and timely manner. The IAC would take over the

training and education responsibilities currently performed under the VHSIC Program Office including maintenance and operation of the VHSIC data base. It would also include expanded services to the VHSIC community as needed.

In addition to the VHSIC IAC, a major source of information for the defense community is and will continue to be the Defense Technical Information Center (DTIC). DTIC has on file well over 1000 documents relative to VHSIC and VHSIC related technology. DTIC is accessible to qualified users which include U.S. Government agencies, their contractors, subcontractors, and approval potential contractors who have established a "need to know" at DTIC.

VHSIC devices are on the US Munitions list and are subject to International Traffic in Arms Regulations (ITARS). Availability and dissemination of all documentation is regulated accordingly.

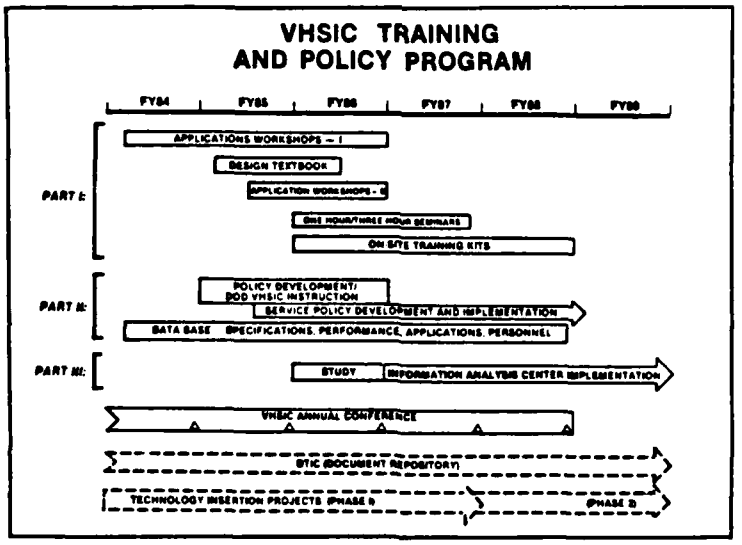


Figure 8

CHAPTER V

VHSIC Phase 2

INTRODUCTION

The second generation of military integrated circuits being developed by the VHSIC program is called Phase 2. The goals of Phase 2 are to design and build integrated circuits with minimum feature sizes of 0.5 micrometers. With these dimensions, the IC chip will contain from 100,000 to 20,000,000 transistors and truly become a "system on a chip". It will provide another 100:1 advance in system performance, reliability, size, weight, power requirements and cost urgently needed by military system designers. It will be the quickest and surest path by which military managers will be able to plan for future advances in system capabilities. Ideas for new military functions and operations which would otherwise not be possible are now being conceived and carried out with VHSIC Phase 2 technology.

An initial Program Definition effort was carried out by several major defense companies (A.T.T., Harris, Honeywell, Hughes, IBM, RCA, Texas Instruments, TRW, and Westinghouse). A number of others such as National Semiconductor, E-Systems, Motorola, and General Dynamics were closely involved as team members of the prime contractors. From among these participants, Honeywell, IBM and TRW were selected in November 1984 to carry out VHSIC objectives. Each Phase 2 contract is a four year effort which includes the development of submicron VHSIC technology. A principle goal of phase 2 is the production of a prototype set of chips and the design of a system module using these chips so that the increased signal processing power of the phase 2 chips may be demonstrated.

A comparison of the technical characteristics and goals between Phase 1 and Phase 2 is shown below:

	Phase 1	Phase 2	
Feature size	1.25	0.5	micrometers
Functional throughput	$5x10^{11}$	$1x10^{13}$	gate-Hz/cm^2
Chip complexity	10-25K	50-100K	gates
Clock speed	25	100	MHz
Power dissipation	1-4	0.5-2	Watts
Pin connections	100-240	100-625	
Radiation hardness	10-50K	200K	Rads(Si)

TECHNICAL APPROACH

The magnitude of the task of developing 0.5 micrometer devices was graphically illustrated in Figure 6 where 0.5 and 1.25 dimensions are compared with the cross section of a typical human hair. Furthermore, the contractors will have to put as many as 20 million transistors with these 0.5 micron dimensions on a single chip in order to make the ICs required for the Phase 2 program.

The requirement for 0.5 micrometer feature sizes in Phase 2 represents a major advancement in traditional semiconductor processing technology. Many of the current techniques for fabricating IC chips were pushed to their physical limits in the Phase 1 portion of the program. Some materials and tools used in fabricating 1.25 micrometer chips must be improved to address submicrometer dimensions. For example, current production optical lithography equipment is not capable of producing the 0.5 micrometer feature size chips.

The tools for Phase 2 are being evolved from the tools used in Phase 1. The electron beam lithography machine developed by Perkin-Elmer Corporation in Phase 1 is a key resource for Phase 2. Phase 2 activity has stimulated additional commercial efforts to improve optical lithography techniques. Submicron optical equipment has already been demonstrated. Another technique for achieving submicron lithography is the use of soft X-rays as a light source. This approach is being explored both within the scope of the VHSIC program and by several independent industrial efforts. This activity will lead to the future availability of the advanced materials and machinery needed for volume production of VHSIC submicron chips.

The contractors selected for Phase 2 are IBM, TRW and Honeywell. Their contracts are being administered by the Army, Navy, and Air Force respectively. All three industry programs are complementary both in fabrication technology and system application. Stringent, aggressive technical requirements have been placed on these contractors to ensure that the DOD will once again have established the means for regaining our technological superiority in weapon systems development.

The approach taken by each of the contractors is summarized below:

VHSIC PHASE 2 SUBMICRON TECHNICAL SUMMARY

CONTRACTOR	TECHNOLOGY	DESIGN APPROACH	BRASSBOARD MODULE APPLICABILITY
HONEYWELL	CML BIPOLAR E-BEAM LITHO SINGLE & MULTI-CHIP PACKAGE RADIATION HARD TO 200K RADS	CELL LIBRARY CONFIGURABLE GATE ARRAY 100% TESTABILITY ~80K EQUIV. GATES	RADAR, EO SYSTEMS
IBM	CMOS BULK E-BEAM/U-V LITHOGRAPHY SINGLE & MULTI-CHIP RADIATION HARD TO 200K RADS	CELL LIBRARY MASTER IMAGE CHIP STRUCTURE ~75K EQUIV. GATES	SONAR, EW, RADAR SYSTEMS
TRW	3-D BIPOLAR/CMOS E-BEAM FOR 3-D E-BEAM/OPTICAL LITHO FOR CMOS 1400 MIL SUPER CHIP RADIATION HARD TO 200K RADS	CELL LIBRARY WAFER SCALE INTEGRATION VIA REDUNDANCY ~4M EQUIV. GATES	CRUISE MISSILE, SATCOM,AVIONICS SYSTEMS

Figure 9

SYSTEM PAYOFF

The payoff expected from the Phase 2 submicron program is the ability for the Services (1) to greatly improve the performance of weapon systems currently being designed and (2) to consider the design of systems which could not be implemented with current or even VHSIC Phase 1 technology. Some of these possibilities are described below.

The success of the Strategic Defense Initiative program depends on advances in many highly advanced and difficult technologies. One of the most critical requirements is for an enormous amount of high speed signal and data processing as shown in Figure 10.

The system must operate ultra-reliably in the space environment over a 10 year period with the ability to reconfigure itself automatically as the signal environment changes and if individual system components fail.

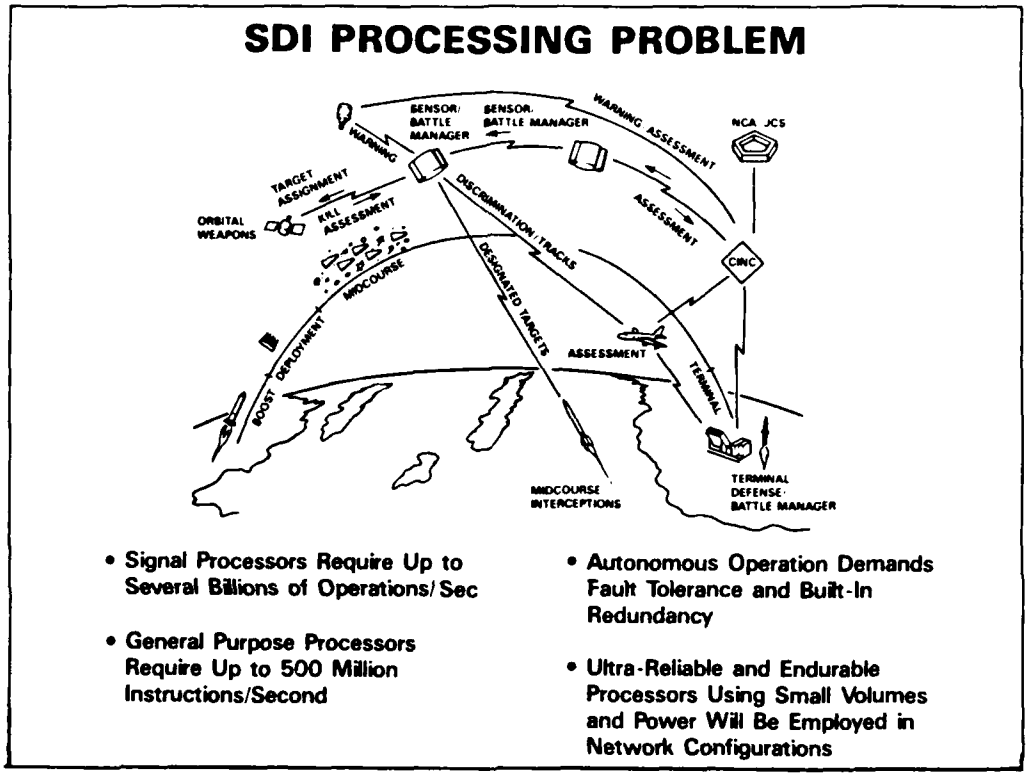


Figure 10

Engineering analysis indicates the only feasible way to achieve this capability is to use an unprecedented amount of on-board processing - that is, to include a major part of the signal and data processing equipment onboard the spacecraft. VHSIC submicron technology can make this possible within the constraints of allowable weight, space and power. An estimate of the computational capability of an advanced on-board signal processor for a specific mission is shown in Figure 11.

ADVANCED ONBOARD SIGNAL PROCESSOR

- AOSP objectives achievable with VHSIC Submicron technology
  - High performance (ACE capable of 20 MIPS)
  - Programmable in Ada
  - Low power
  - Small size and weight
  - High reliability
  - Radiation hardness
- Implementation comparison using VHSIC Submicron technology

Single ACE	Current Technology	VHSIC II Technology
Computational capability (OPS)	4×10^5	2×10^7
Volume ($in.^3$)	6900	9
Power (W)	400	40

Figure 11

Two of the Army's future weapon system requirements are for greatly increased munitions kill ratios and for single man crew attack helicopters. Phase 2 components make it feasible to consider fully functional "brilliant" munitions whose cost per round is comparable to current guided projectiles but whose cost per destroyed target is an order of magnitude lower (Figure 12). Similarly, the VHSIC equipped LHX shown in Figure 13 has the potential of becoming a weapon system that constitutes a significant force multiplier needed by the United States to counter potential superior numerical ground and tactical helicopter forces. Army sponsored analysis has determined that to remain within the weight restrictions for LHX electronics, VHSIC Phase 2 technology is required.

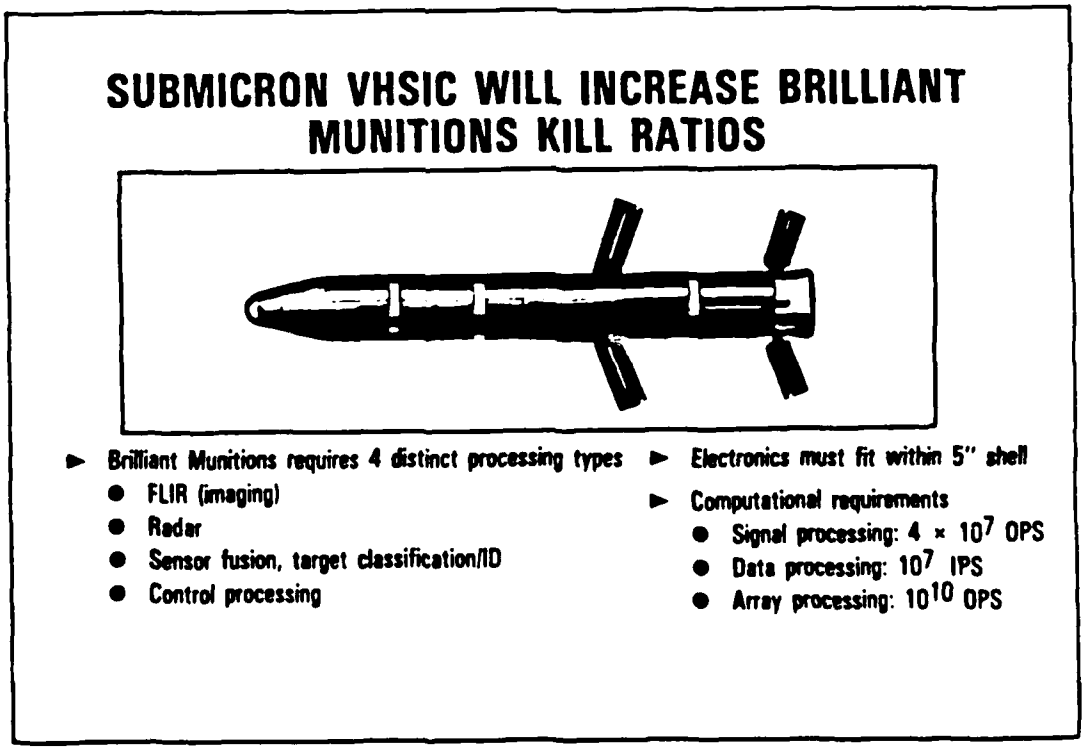
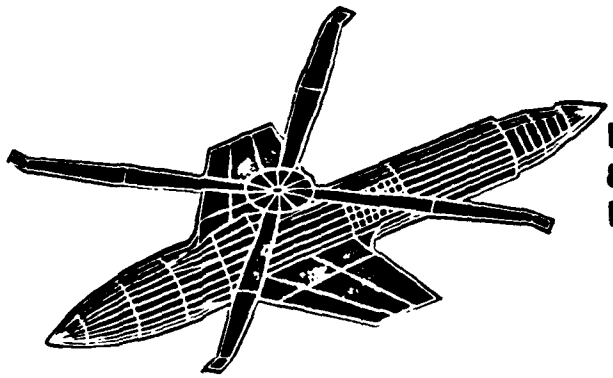


Figure 12

VHSIC Submicron Technology Will Optimize the Performance of an Advanced Light Helicopter



Light Helicopter, Experimental (LHX)
8,000 LB, Single Crew
Preliminary ATR Targets
- 0.25 FT^3
- 30 LB
- 500 Watts

- Multiple Target Detection & Track
- Multiple Sensor
  - TV
  - MMW
  - FLIR
  - LASER
- Auto Weapon Handoff
- AI Algorithm Capability
- Programmable For Mission Flexibility
- Threat Prioritization
- Real Time Fault Detection & Reconfiguration
- 200 HR Availability

Figure 13

The Navy's potential for improved undersea anti-submarine warfare capabilities centers on being able to handle signal processing for advanced signal detection and beamforming. Hundreds of acoustic signals gathered by the large, wide aperture and conformal arrays shown in Figure 14 must be processed in real time to perform these functions. They impose an increased signal processing load on the system that can most effectively be met with the high speed, high throughput devices of VHSIC Phase 2.

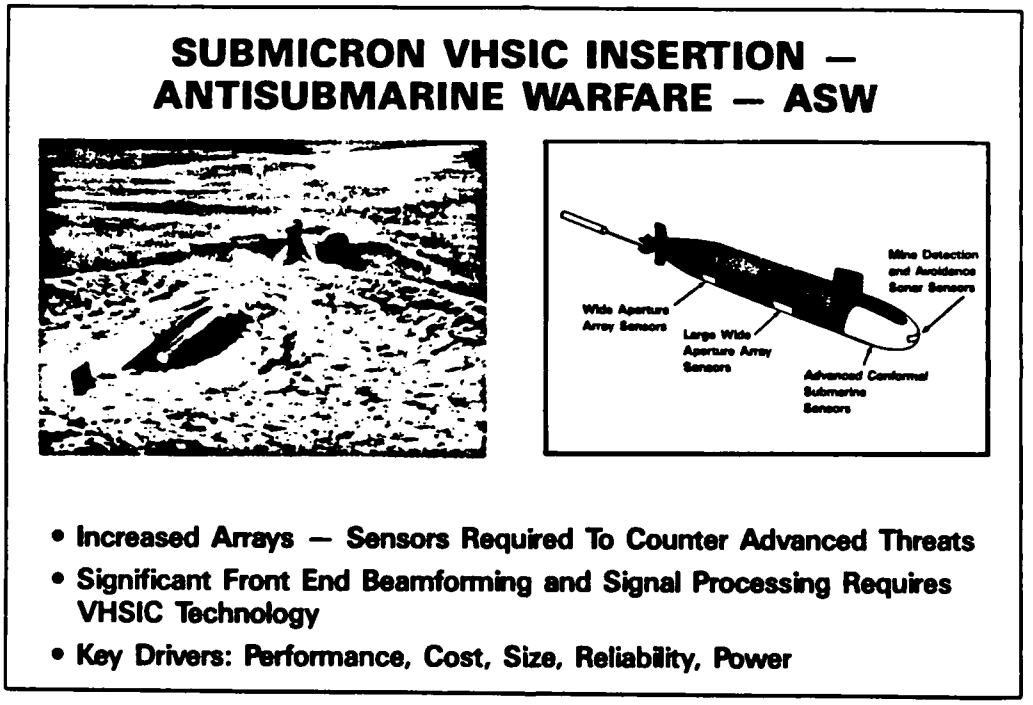


Figure 14

The increased system performance in radar surveillance from carrier-based aircraft, shown in Figure 15, is needed to detect, track, and counter the higher target densities postulated for future engagements.

ADVANCED SURVEILLANCE RADAR REQUIRES SUBMICRON VHSIC

- ► Advanced surveillance radar requirements
  - Increased range and resolution
  - Surface surveillance
  - Missile launch alert
  - Weapon delivery/interrupt control
  - Non-cooperative target recognition
- ► Computational requirements
  - Preprocessing: 10^{11} OPS
  - Signal processing: 4×10^{8} OPS
  - Data processing: 10^{8} IPS
  - Associative processing: 10^{7} OPS

Figure 15

Air Force requirements for intelligent avionics, Figure 16, and increased ICBM performance, Figure 17, must be met within the tight constraints of advanced airborne and space platforms. In addition, to utilize this increased performance effectively, reliability of the electronic components must be increased by a factor of 100 or more. This will permit achievement of total system reliability at a level consistent with required operational readiness and availability. Techniques needed to provide increased component reliability are part of the built-in-test and fault tolerance requirements of the Phase 2 submicron design development tasks. The feasibility of including such additional "housekeeping" functions on a complex chip depends on the submicron electronic technology which can build the required additional number of transistors into the chip, interconnect them, and still keep the overall chip size small enough so that an economical production yield will result.

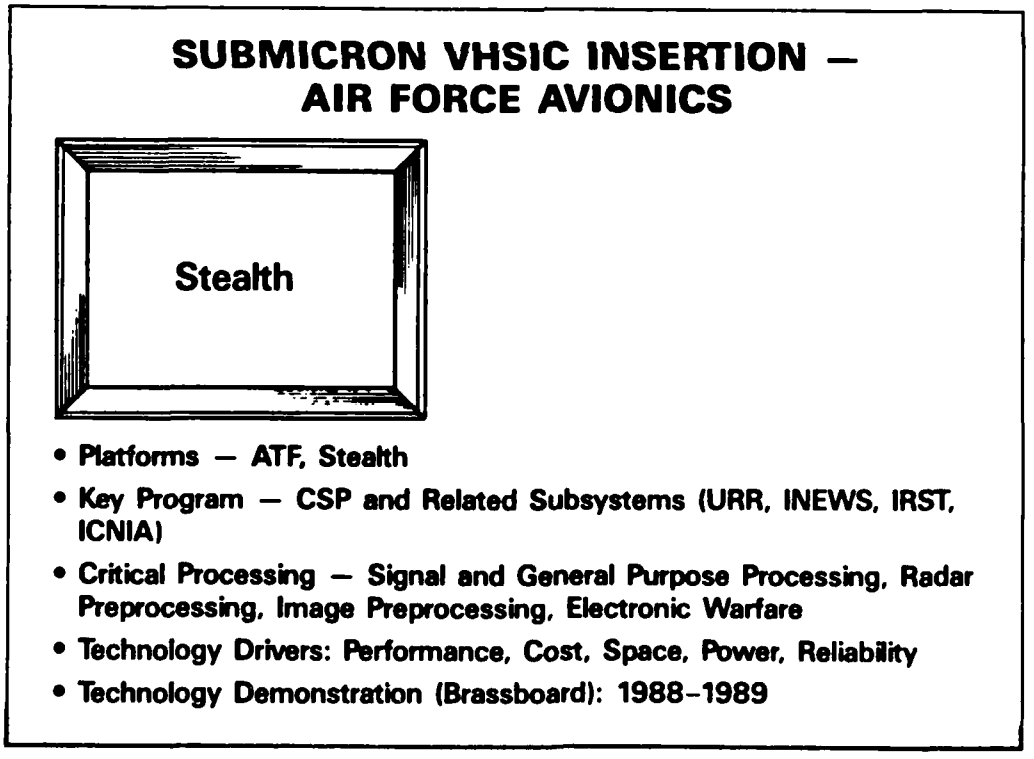


Figure 16

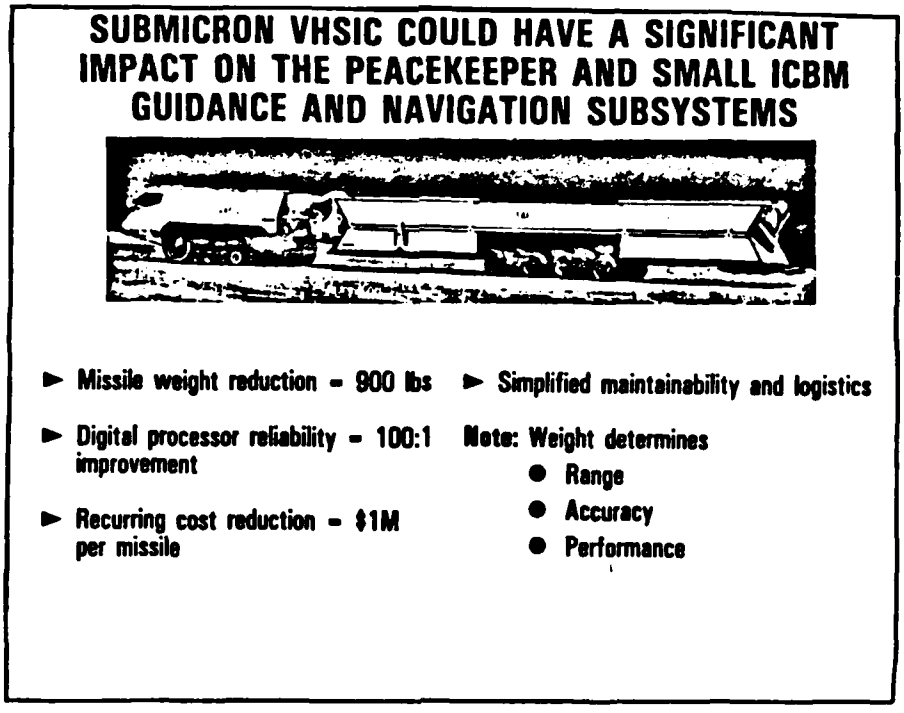


Figure 17

The above applications are selected illustrations of the wide spectrum of advanced systems requirements and operational capabilities which are being addressed by VHSIC Phase 2 technology. In each case, potential improvements in functional performance, weight, space, power, reliability, or logistic maintenance may be estimated. And in each case the amount of real time signal processing throughput that is needed under realistic conditions can only be met by the submicron IC technology being developed under VHSIC Phase 2.

SUMMARY

This report has summarized all the activities of the VHSIC Program and identified key elements, accomplishments and goals of each activity which demonstrate how VHSIC components have been and will continue to be made available to weapon system developers.

The United States must maintain its technological lead in semiconductor devices. The Department of Defense must have access to and be able to utilize state of the art technology in order to deploy superior weapon systems. This is in response to numerically superior forces that may oppose us or our allies.

Commercial semiconductor products are not readily adaptable to Defense needs. While Defense needs pioneered early development of semiconductor technology, commercial applications soon overtook the market place.

Defense users then followed industry's "front end" research and development. This resulted in the availability of a variety of programmable devices, costly software systems, expensive qualification processes and an alarming erosion of our comfortable lead in deployed military processor hardware capability.

The VHSIC Program Plan outlines the course of action necessary to recover this technological lead and make advanced state of the art devices available to weapon system developers. As stated, this includes:

- Define two generations of ICs to set the pace for IC use over the decade of the 80's. This is embodied in the products of Phase 1, 1.25 micrometer minimum feature size circuits, and Phase 2, 0.5 micrometer minimum feature size circuits.
- Establish requirements and define military unique IC designs not available on the commercial market.
- Establish pilot production facilities to assure early access to prototype devices for system experimentation - DOD's investment in 6 pilot production facilities has stimulated private investment throughout the defense industry.
- Select "proof of principle" system brassboard demonstrations to establish credibility with military system developers. This caused many weapon system developers to initiate similar demonstrations.
- Substitute planning for hoping - demonstrate how product planning for the next generation of ICs must take place concurrently with implementation of the current generation in order for rapid utilization in deployed military systems to keep pace with commercial development.

Based on early success of the VHSIC program in focusing attention on military IC development, the VHSIC program was expanded to include:

- Technology Insertion
- Yield Enhancement
- Design Automation
- Applications Workshops
- Uniform DOD policy on the use of ICs in weapon systems.

The VHSIC program, though midway through its final phase, is already paying dividends that should exceed DOD's investment. These include:

- Establishment of the program has focused attention throughout the weapon system community within DOD and in industrial concerns which provide weapon systems to DOD.
- The early DOD investment has stimulated further investment of over a billion dollars by weapon system developers in state of the art IC facilities to make this vital technology available. Venture capital has also been attracted to provide capability for military ICs.
- Devices are now available for sale to all weapon system developers.
- Over 40 military system programs are actively engaged in technology insertion.
- VHSIC application workshops have trained over 2,500 weapon system engineers, from over 250 companies, on use of the technology.
- VHSIC reliability testing has verified that VHSIC devices exceed reliability goals which are 5 times better than commercial practice.
- A comprehensive program to put VHSIC and VHSIC-like parts on the military Qualified Parts List (QPL) is underway.
- The first VHSIC insertion into an operational weapon system was demonstrated in 1985 (AN/ALQ-131).
- Major weapon system programs are publicly announcing that their absolute success is a direct function of VHSIC Technology (e.g. - LHX).
- All Phase 1 Technologies are now being transferred from an R&D base to a production base.
- Radiation hardness test results indicate all the Phase 1 chips will exceed the goals of Phase 1 program.

- Key advanced avionic program developments (e.g. ICNIA, INEWS, Ultra Reliable Radar, etc.) have fully certified the firm requirements for VHSIC Technology.
- Many weapon system programs are now planning for VHSIC to be in the active inventory before the end of the decade (e.g. AN/ALQ-131, F-15 Central Computer, MK-50 Torpedo, TOW Missile, F-16 Radar Signal Processor, etc.)
- A DOD directive which keeps DOD use of advanced ICs on military weapon systems in step with the emergence of the technology is being put in place.

The final phase of the VHSIC program is well underway. Successes realized in earlier phases of the program have made available the tools required for continued achievement of aggressive technical goals.

The unique program management approach taken by DOD for the VHSIC initiative has resulted in a highly successful tri-Service program. Products from the VHSIC program will continue to provide weapon system developers state of the art semiconductor technology long after the program is completed. This critical technology, now being designed into the systems of the 90's, will provide the United States with the strategic and tactical advantages required to discourage confrontation at all levels and to defeat numerically superior forces in the event of engagement.

LIST OF FIGURES

GLOSSARY

ACE	Asynchronous Processing Element
AI	Artificial Intelligence
AJ	Anti-Jam or Jam Resistant
ASW	Antisubmarine Warfare
ATF	Advanced Tactical Fighter
ATR	Auto Target Recognition
Brassboard	Field Demonstratable Electronic Model
Breadboard	Laboratory Demonstrable Electronic Model
CAD	Computer Aided Design
CSP	Common Signal Processor
DOD	Department of Defense
DTIC	Defense Technical Information Center
EHF	Extremely High Frequency
EO	Electro-Optic
EW	Electronic Warfare
FLIR	Forward Looking Infrared
HF	High Frequency
IAC	Information Analysis Center
IC	Integrated Circuit
ICNIA	Integrated Communication Navigation Identification Avionics
IDAS	Integrated Design Automation System
IEEE	Institute of Electrical and Electronic Engineer
INEWS	Integrated Electronic Warfare System
IPS	Instructions Per Second

IRST	Infrared Search and Track
ITAR	International Traffic in Arms Regulation
JTIDS	Joint Tactical Information Distribution System
LRM	Line Replaceable Module
LSI	Large Scale Integration
MIL-STD	Military Standard
MIPS	Millions of Instructions Per Second
MMW	Millimeter Wave
MSI	Medium Scale Integration
OPS	Operations Per Second
OUSDR&E	Office of the Under Secretary of Defense for Research and Engineering
PLRS	Position Locating Reporting System
PSP	Programmable Signal Processor
SSI	Small Scale Integration
TOW	Tube Launched, Optically Tracked, Wire Guided
TTL	Transistor Transitor Logic
VHSIC	Very High Speed Integrated Circuit
VLSI	Very Large Scale Integration

END

DTIC

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