AD-A169 242 REFRACTORY METALS AND SILICIDES FOR VERY LARGE SCALE INTEGRATION APPLICATIONS(U) STANFORD UNIV CA CENTER FOR INTEGRATED SYSTEMS K C SARASWAT NOV 85 1/1

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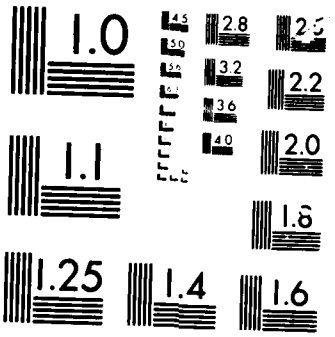

Refractory Metals and Silicides for Very Large Scale Integration Applications

NOV-1985

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Continuous advancements in technology have resulted in integrated circuits with smaller device dimensions, and larger area and complexity. The overall circuit performance has depended primarily on the device properties. However, the parasitic resistance and capacitance associated with interconnections and contacts, as shown in Fig. 1(a) for an MOS transistor, are now beginning to influence the circuit performance and will be the primary factors in the evolution of submicron VLSI technology. Fig. 1(b) - 1(d) show examples of contact resistance, shallow junction series resistance and RC time delay of interconnections, respectively. Results of theoretical modeling indicate that below 1 μm minimum feature size the impact of these parasitics will seriously hurt the circuit and system performance [1]. The RC time delay, the IR voltage drop, the power consumption and the crosstalk noise due to these parasitics will become appreciable. Thus even with very fast devices the overall performance of a large circuit could be seriously affected by the limitations of interconnections and contacts.

During the last few years a good amount of work has been done on new and innovative materials, device structures and fabrication technology to overcome these problems. Fig 2 shows the past, present and the future status of the technology. It is evident that refractory metals and silicides are playing increasingly important roles. It must also be pointed out that these materials will not replace aluminum but compliment it.

In order for a certain conductor to be used to form multilayer interconnections, several requirements which are imposed by fabrication technology and required circuit performance must be met.

The main requirement is good conductivity, because it can substantially improve the resistance and delay times of the electrical interconnection lines used for VLSI structures. In general, several other requirements are imposed on interconnection materials by fabrication technology. In a multilayer interconnection structure, the layers incorporated early in the process sequence might be subjected to several fabrication steps, that layers incorporated later might not be subjected to. The most rigorous set of requirements are, low resistivity, ease of deposition of thin films of the material, ability to withstand the chemicals and high temperatures required in the fabrication process, good adhesion to other layers, ability to be thermally oxidized, stability of electrical contacts to other layers, ability to contact shallow junctions, good MOS properties, resistance to electromigration and ability to be defined into fine patterns.

The materials which have been used or proposed for forming interconnections can be broadly classified into four categories: heavily doped polysilicon, low temperature metals, high temperature refractory metals and metal silicides. Table [1] compares properties of some of these materials showing their compatibility with present silicon fabrication technology.

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For a long time, aluminum has been used to form the metal interconnects, however as device dimensions are scaled down, its reliability is becoming a major issue. Some of the problems are, electromigration, high solubility of silicon leading to poor contact reliability to shallow junctions, hillock formation causing electrical shorts between successive layers fo A1, and corrosion. Many of these problems have been solved by using alloys of aluminum with Si, Cu and recently Ti [2].

With the advent of silicon-gate MOS technology, polycrystalline silicon has been extensively used to form gate electrodes and interconnections. The success of the silicon-gate MOS technology can be largely attributed to the use of polycrystalline silicon as an additional layer of interconnections. In many applications two or even three layers of polycrystalline silicon have been used. From numbers shown in Table [1] and Fig. 1(d) it is evident that the resistivity of polycrystalline silicon is too high and is beginning to limit the performance of large circuits with small dimensions. In all other respects, it is a very nice material to work with because basically it is silicon and therefore highly compatible with silicon technology.

During the last few years, use of refractory metal silicides have been heavily investigated for this application and for silicidation of diffusions and the results have been very exciting. From Table [1] it can be seen that silicides of tungsten (W), molybdenum (Mo) and tantalum (Ta) have reasonably good compatibility with IC fabrication technology. They have fairly high conductivity, they can withstand all the chemicals normally encountered during the fabrication process, thermal oxidation of their silicides can be done in oxygen and steam to produce a passivating layer of SiO_2, their contacts to shallow p-n junctions are reliable, and fine lines can be etched by plasma etching these materials. The formation of thin films of silicides is not as straightforward as that of aluminum and polycrystalline silicon, but it can be done by a variety of deposition techniques. These properties suggest that the silicides of W, Mo and Ta can be used in all of the applications where polycrystalline silicon has been used so far. While $TiSi_2$ is very attractive for this application, its etch rate in hydrofluoric acid (HF) is very fast. If the use of HF can be avoided during the fabrication by employing dry etching techniques, $TiSi_2$ can also be used successfully.

Several problems remain to be solved before silicides can be used on a routine basis in production. Deposition techniques will have to be much more controllable and reproducible than those being used today. CVD technology offers the most promising results [3]. Silicide films as deposited by current deposition techniques have very low conductivity, and additional high temperature annealing is required to increase it. These temperatures might be too high for the VLSI technology of the the future, since these deposited films can have tensile or compressive stress in them the type and magnitude of which change as a function of processing temperature. The magnitude of this stress can be enough in some cases to cause cracks and poor adhesion. This poses serious yield and reliability problems.

During the early seventies, several attempts were made to develop refractory metal (tungsten and molybdenum) gate technology. However, in comparison to silicon gate technology it had no apparent advantage. The minimum feature size at that time was around 10 μm and the chip area was rather small. Therefore the RC time delay was not a big issue, and the industry's interest in refractory metal gate technology gradually cooled off. As circuit complexity and size grew, and the inadequacies of polycrystalline silicon and Al started surfacing, interest in refractory metals was rejuvenated. During the last

few years, W and Mo have been successfully used to form gate electrodes and interconnections in several VLSI applications and it appears that this trend will grow.

These materials have very attractive properties for multilayer interconnection applications. Their resistivities are only slightly higher than that of Al, their melting points are much higher than silicon, the thermal expansion coefficients are closer to that of silicon (see Table 1) and they are highly resistant to electromigration. They are inert to many chemicals allowing the use of patterned films of these materials as etching masks for both SiO_2 and Si_3N_4. They are easy to etch using the plasma technology and thus fine lines can be defined with relative ease. At temperatures below the silicide formation temperature (~600°C) the solubility of silicon is negligible and thus the stability of contacts is excellent.

Deposition of the thin films of Mo and W has been investigated by electron beam evaporation, sputtering and recently by chemical vapor deposition. The films deposited by CVD generally have such superior properties as low contamination, lower resistivity, better step coverage, lower stress and better compatibility with batch production techniques. Selective CVD of W appears to be a very promising technology for many VLSI applications [4].

The major disadvantage of W and Mo is that their oxides are volatile at high temperatures (~ > 400°C). Therefore these metals can be used only when all of the steps where exposure to high temperature oxidizing ambient might occur are over, but high temperature steps in inert ambient are still remaining. Recent work involving the use of H_2 rich H_2O to avoid oxidation of W yet oxidize Si appears to be very promising and may provide the necessary ingredients of the submicron MOS technology [5].

References

[1] K.C. Saraswat and F. Mohammadi, "Effect of Interconnection Scaling on Time Delay of VLSI Circuits", *IEEE Trans. Electron Dev.*, Vol. ED-29, April, 1982., pp. 645-650.

[2] D.S. Gardner, T.L. Michalka, K.C. Saraswat, T.W. Barbee Jr., J.P. McVittie and J.D. Meindl, "Layered and Homogeneous Films of Al and Al/Si with Ti and W for Multilayer Interconnects" *IEEE Trans. Electron Dev.*, Vol. ED-32, February, 1985, pp. 174-183.

[3] K.C. Saraswat, D.L. Brors, J.A. Fair, K.A. Monig and R. Beyers, "Properties of Low Pressure CVD Tungsten Silicide for MOS VLSI Interconnections", *IEEE Trans. Electron Dev.*, Vol. ED-30, November, 1983, pp. 1497-1505.

[4] K.C. Saraswat, S. Swirhun and J.P. McVittie, "Selective CVD of Tungsten for VLSI Technology", *VLSI Science and Technology*, Electrochemical Society, 1984, pp. 409-419.

[5] S. Iwata, N. Yamamoto, N. Kobayashi, T. Terada and T. Mizutani, " A New Tungsten Gate Process for VLSI Applications," *IEEE Trans. Electron Dev.*, Vol ED-31, pp.1174-1179, September 1984.

PROPERTIES OF INTERCONNECTION MATERIALS

SILICIDE	THIN FILM RESISTIVITY ($\mu\Omega$ CM)	EUTECTIC TEMP. WITH SI (°C)	PROCESS COMPATIBILITY	REACTION WITH AL (°C)	THERMAL EXPANSION COEFFICIENT (PPM/°C)
WSi_2	30-70	1440	GOOD	500	12.5
$MoSi_2$	40-100	1410	GOOD	500	8.25
$TaSi_2$	35-55	1385	ETCHES SLOWLY IN HF	500	8.8-10.7
$TiSi_2$	13-16	1330	ETCHES IN HF	450	12.4
$CoSi_2$	18-25	1195	ETCHES IN HF	400	10.14
PtSi	28-35	830	HIGH TEMP.?	250	---
$Si(N^+)$	500	---	---	577	3
W	8-10		POOR OXIDATION RESISTANCE	500	4.5
Mo	8-10		POOR OXIDATION RESISTANCE	500	5.0

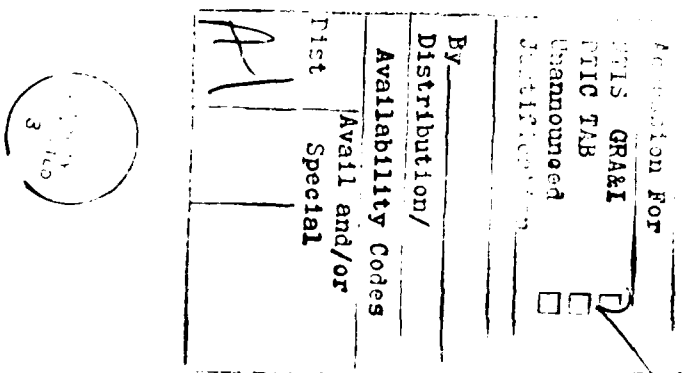


Fig. 1

(a)

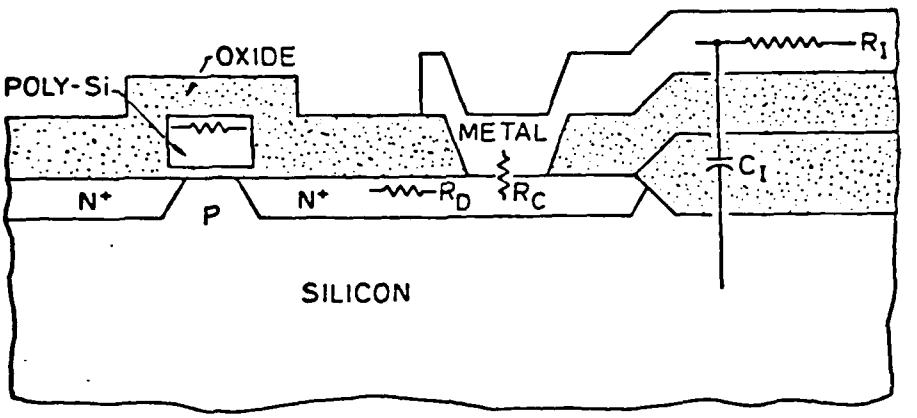


Fig. 1(a) A cross section of an MOS transistor with parasitic elements associated with poly-Si, shallow diffusions, contacts and interconnections.

(b)

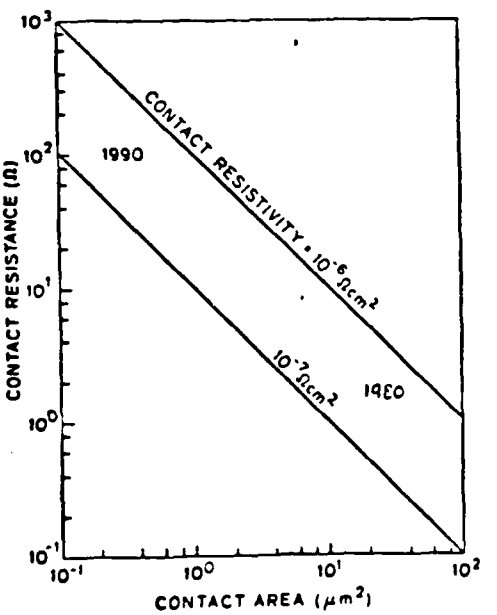


Fig. 1(b) Contact resistance vs contact area

Fig. 1

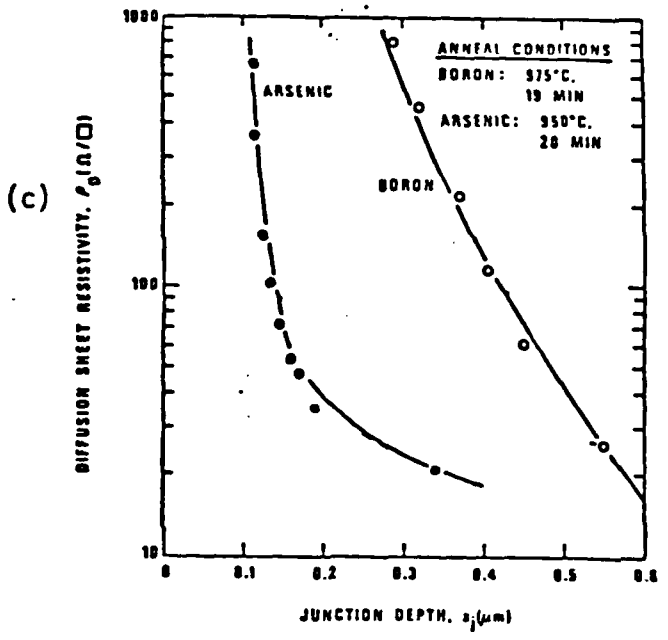


Fig. 1(c) Diffusion sheet resistance vs juntion depth

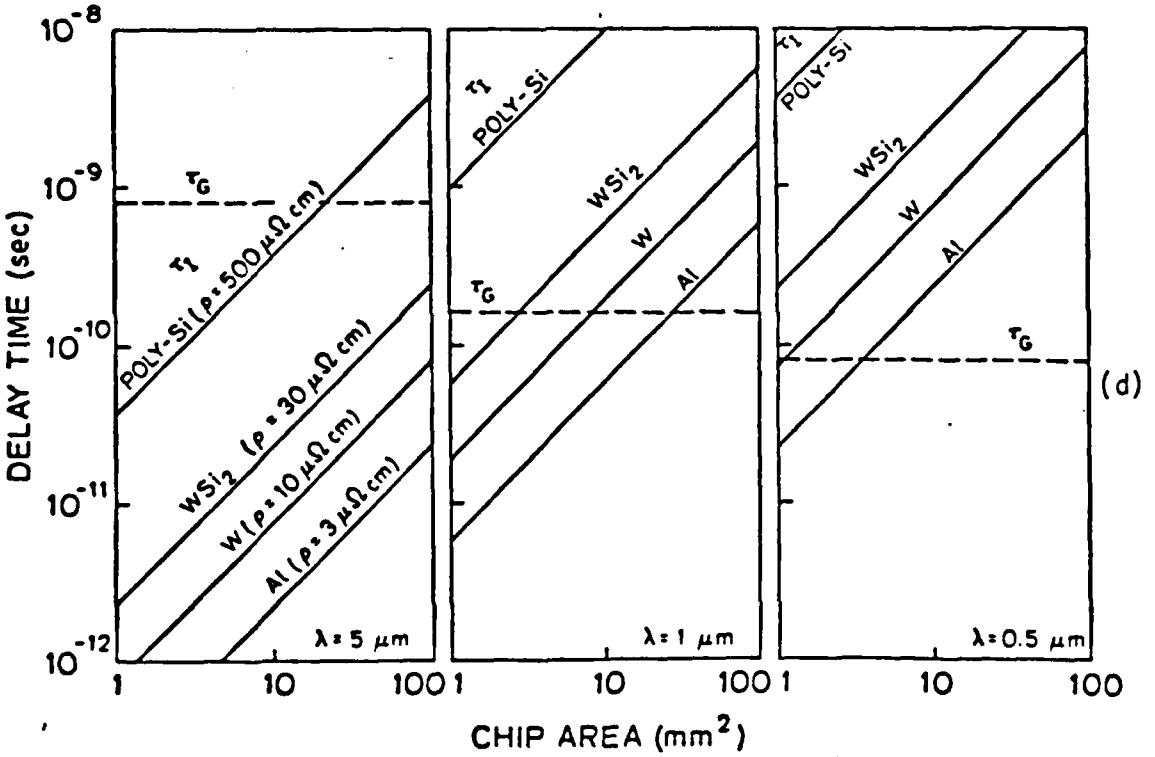


Fig. 1 (d) RC time delay τ_I vs chip area for minimum feature size, λ of 5,1 and 0.5 μm. Also shown is the intrinsic device delay τ_G

Fig 2

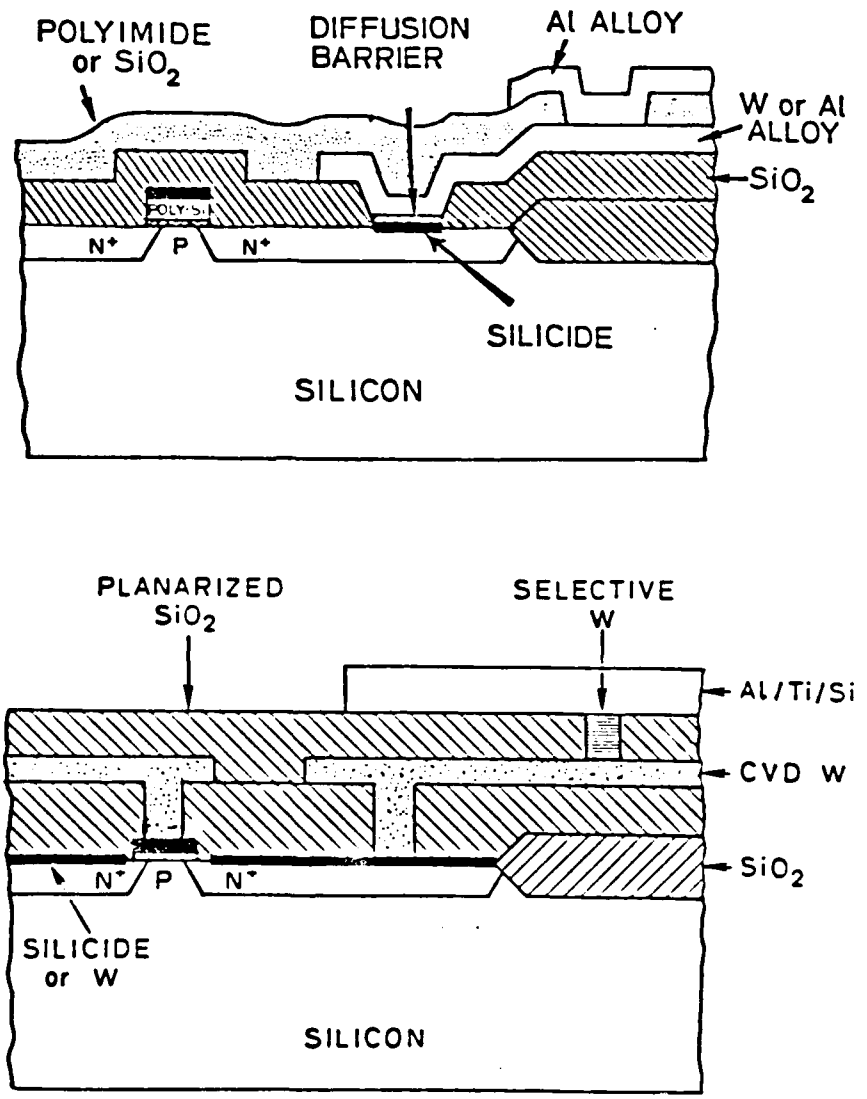
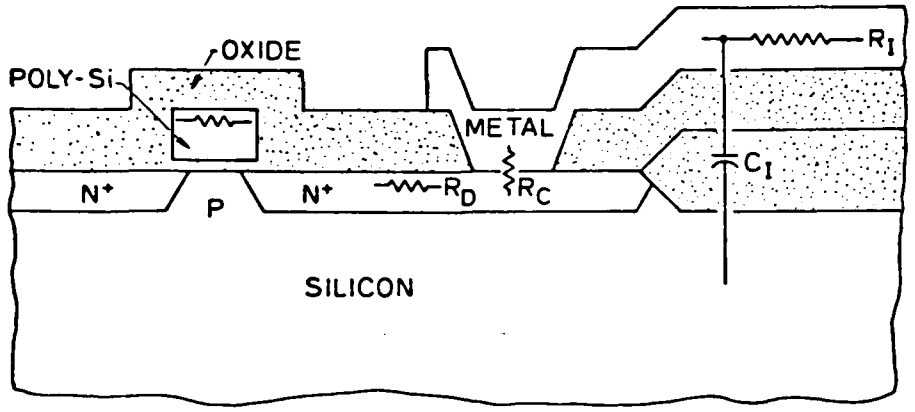
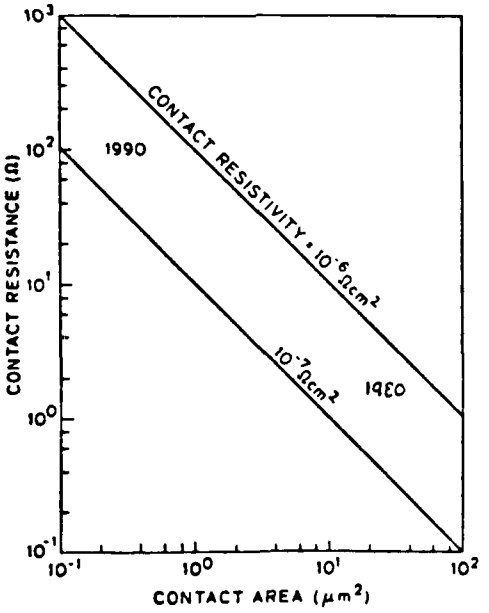
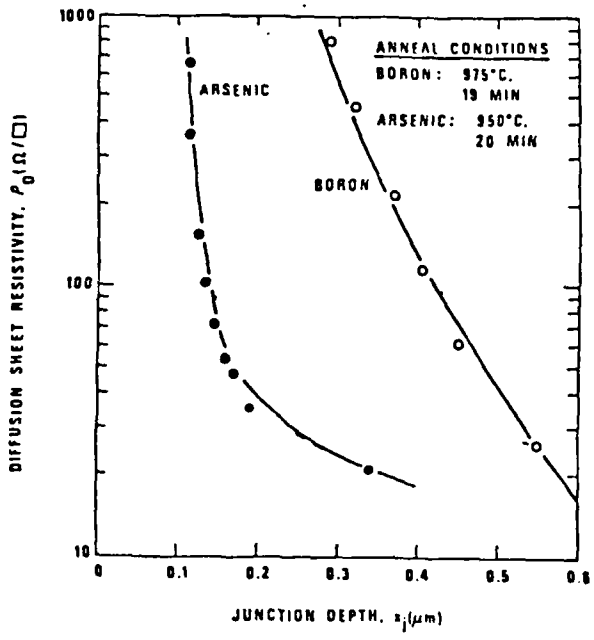
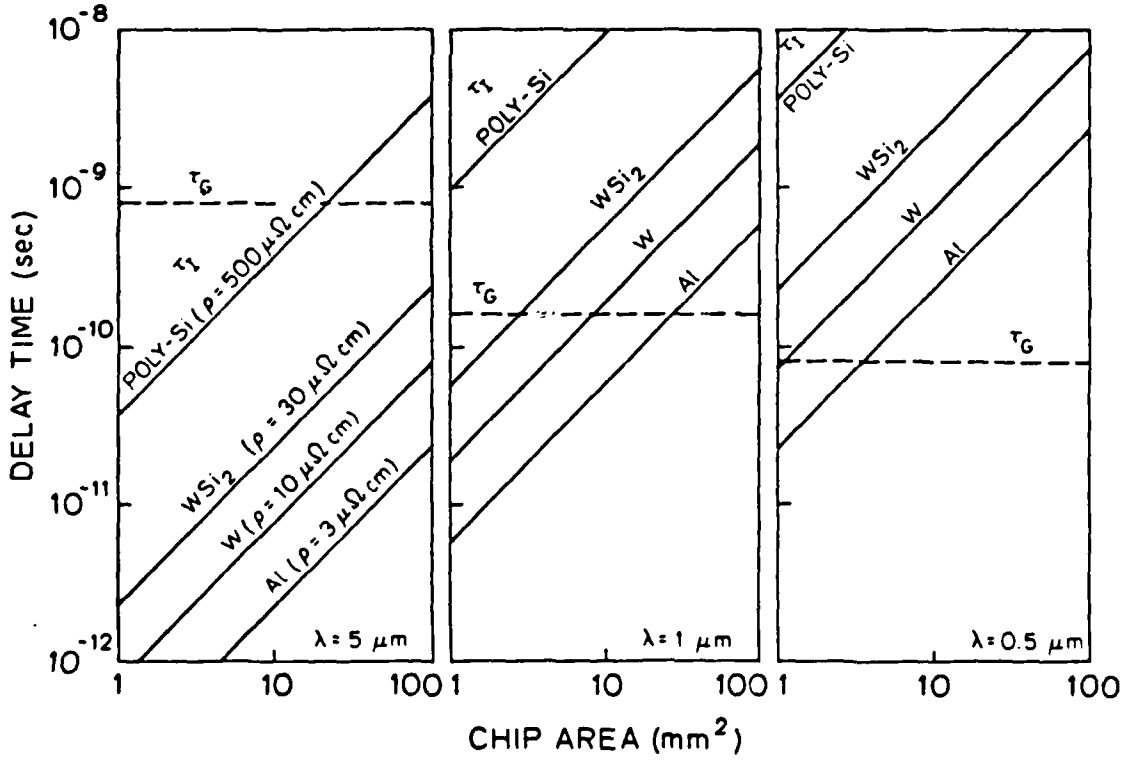


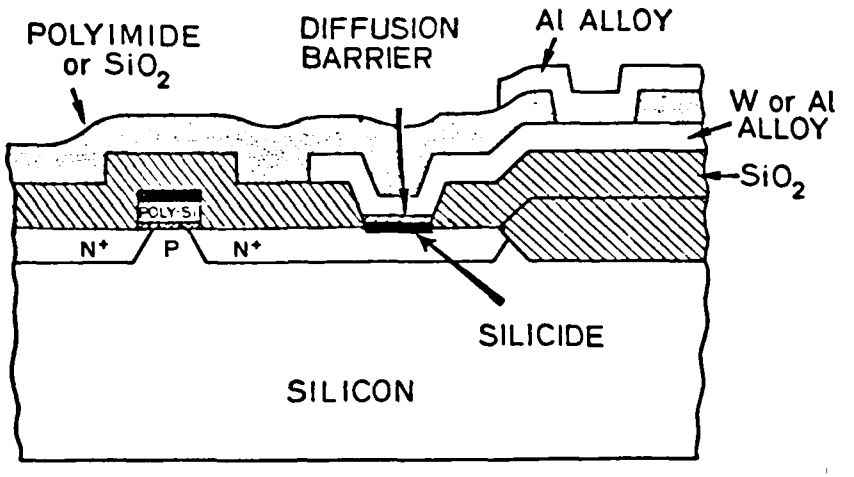
Fig. 2. Use of refractory metals and silicides to solve the problems created by parasitics shown in Fig. 1(a) (a) present technology (b) Future technology

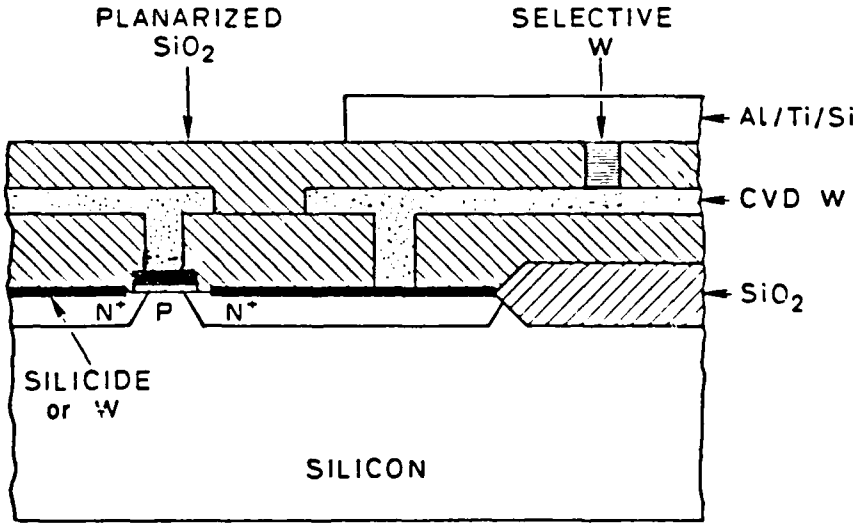

POLY-Si
OXIDE
METAL
R_I
C_I
N+
P
N+
R_D
R_C
SILICON


CONTACT RESISTANCE (Ω)
CONTACT AREA (μm^2)
CONTACT RESISTIVITY = 10^{-6} Ωcm^2
10^{-7} Ωcm^2
1990
1980
10^3
10^2
10^1
10^0
10^{-1}


ANNEAL CONDITIONS
BORON: 975°C. 19 MIN
ARSENIC: 950°C. 20 MIN
ARSENIC
BORON
DIFFUSION SHEET RESISTIVITY, ρ_D (Ω/□)
JUNCTION DEPTH, x_j (μm)
1000
100
10
0
0.1
0.2
0.3
0.4
0.5
0.6


DELAY TIME (sec)
CHIP AREA (mm²)
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
τ_G
τ_I
POLY-Si (ρ = 500 μΩ cm)
WSi₂ (ρ = 30 μΩ cm)
W (ρ = 10 μΩ cm)
Al (ρ = 3 μΩ cm)
POLY-Si
WSi₂
W
Al
λ = 5 μm
λ = 1 μm
λ = 0.5 μm
1
10
100


POLYIMIDE
or SiO_2
DIFFUSION
BARRIER
Al ALLOY
W or Al
ALLOY
SiO_2
POLY-Si
N+
P
N+
SILICIDE
SILICON


PLANARIZED
SiO_2
SELECTIVE
W
Al/Ti/Si
CVD W
SiO_2
N+
P
N+
SILICIDE
or W
SILICON

END

DTIC

7-86