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High-speed wide-band microwave synthesizers are required for many frequency-hopped satellite communication systems. These synthesizers must be of high-reliability design, of compact size, and light weight, in addition to having low DC power requirements.

This paper describes a space-flight qualified synthesizer system which meets these requirements and provides operational redundancy. The circuit technology utilized to implement an indirect synthesis technique using a VCO and phase-locked loop is described, together with circuitry for fast frequency switching, fine frequency tuning and control. The performance of major components is discussed in addition to overall synthesizer system performance.

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High Speed Synthesizers for Satellite Application

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HIGH SPEED SYNTHESIZERS FOR SATELLITE APPLICATION

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Abstract

High-speed wide-band microwave synthesizers are required for many frequency-hopped satellite communication systems. These synthesizers must be of high-reliability design, of compact size, and light weight, in addition to having low DC power requirements.

This paper describes a space-flight qualified synthesizer system which meets these requirements and provides operational redundancy. The circuit technology utilized to implement an indirect synthesis technique using a VCO and phase-locked loop is described, together with circuitry for fast frequency switching, fine frequency tuning and control. The performance of major components is discussed in addition to overall synthesizer system performance.

Introduction

The design of a frequency synthesizer system for use in a frequency-hopped satellite communication link requires careful attention to several performance parameters. These parameters include frequency switching time, bandwidth, frequency resolution, spurious signals, and noise levels. An experimental synthesizer architecture which addresses some of the tradeoffs in these requirements has been reported previously.[1]

A space-flight qualified synthesizer system has been developed for the FLTSAT EHF Package. This synthesizer system incorporates architecture which is similar to that of the experimentsl system with additional circuit development to realize the performance needed for the EHF system. High-rel components configured for efficient operation, careful construction techniques, and thorough testing are utilized to achieve the reliability which is necessary for satellite application in addition to the size, weight, and DC power requirements.

Synthesizer Configuration

The overall synthesizer system is shown in the block diagram of Figure 1. The system is comprised of a synthesizer controller, a receive synthesizer, and a transmit synthesizer in addition to the frequency conversion and multiplication circuitry which is required to provide the frequency-hopped local oscillator signals for two receiver channels and a single transmitter carrier signal. This paper describes

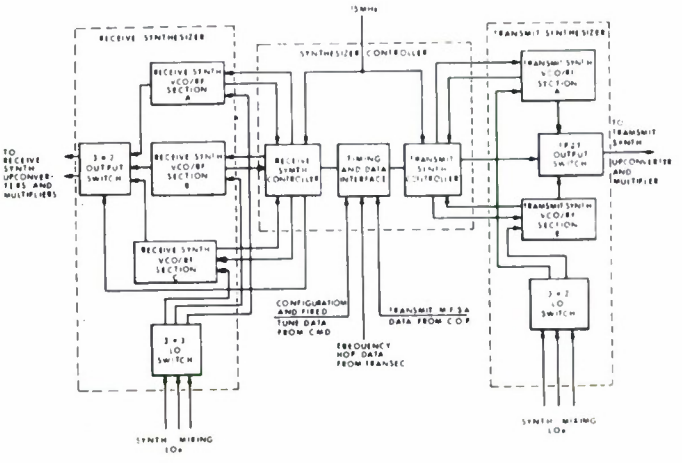

Fig. 1. Frequency Synthesizer System Block Diagram

the receive and transmit synthesizers and the synthesizer controller.

The receive synthesizer subsystem utilizes three identical synthesizers configured with a 3 x 2 switch matrix to provide both rapid frequency switching of any two synthesizers and simultaneous low hop rate operation of the third synthesizer. The third unit may also serve as a backup for either of the other two synthesizers. This partial operational redundancy represents a compromise between complete redundancy and the limits in size and weight allocated for the synthesizer system. Each synthesizer includes a VCO/RF section located in the RF portion of the receive synthesizer subsystem, and phase-locking and control circuitry located in the synthesizer controller.

The RF portion of the transmit synthesizer subsystem is comprised of two synthesizers identical to those of the receive synthesizers which are configured with a 2 x 1 switch to provide rapid frequency switching or low hop rate operation of either synthesizer with back-up capsbility.

Both the receive and transmit synthesizer subsystems also include switching matrices to supply any of three local oscillator frequencies which are used to downconvert the RF source for phase-locking by the synthesizer controller. The receive synthesizer utilizes a 3 x 3 LO switch matrix, and the transmit synthesizer uses a 3 x 2 LO switch matrix to implement the switched LO arrangement which provides wideband operation.

Switching Circuitry

The 3 x 3 LO switch configuration is shown in the block diagram of Figure 2. Three identical channels, each of which includes a

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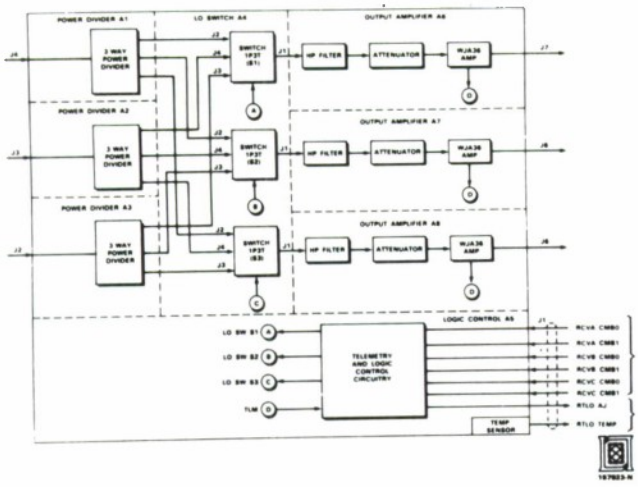


Fig. 2. Local Oscillator Switch (3 x 3) Functional Block Diagram

3-way power divider, a 1P3T switch, filtering, and level adjustment using an attenuator and an amplifier, provide any of the three input frequencies to each of the output ports. Switch position is selected by the synthesizer controller via the logic control circuitry, and telemetry provisions for amplifier current and housing temperature are included. The 3 x 2 LO switch for the transmit synthesizer has a similar topology differing only in that the module utilizes two-way power dividers and two 1P3T switches to realize two channels, in addition to housing the 2 x 1 output switch. The 3 x 2 output switch for the receive synthesizer is also of similar topology with the exception that bandpass filters replace the amplifier boards.

The photograph of Figure 3 depicts the 3 x 3 LO switch module assembly. High channel isolation (60 dB) is achieved by incorporating shielded compartments, semi-rigid coaxial cable to interconconect circuitry, and covers for shielding the junction of switch terminals and coaxial cables. Each 1P3T switch is housed in a hermetically sealed kovar package which is bolted to an epoxy-glass PC board. Each 1P3T switch is comprised of three 1P1T PIN diode switches connected with a common pole which are mounted in an alumina microstrip environment. Hybrid driver circuitry which is integral to the switch package provides control of the switches. These switches were developed specifically for this satellite application.

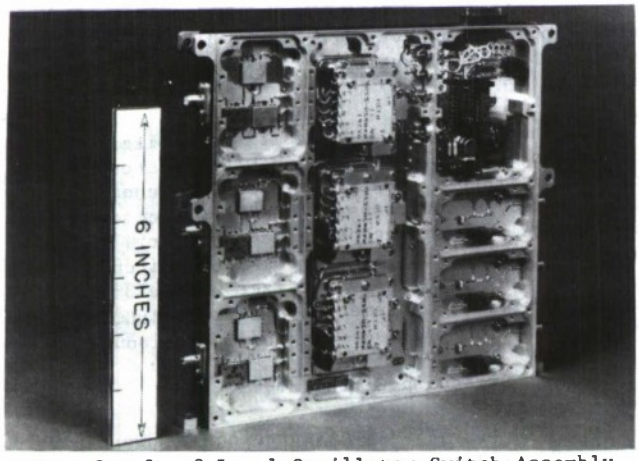


Fig. 3. 3 x 3 Local Oscillator Switch Assembly

The power divider network is comprised of two-way flat-pack power dividers mounted on duroid PC boards. Modular amplifiers are mounted on similar boards together with discrete component filters and attenuators. RFI filtering is employed on the DC power and telemetry lines.

In addition to the high isolation requirement, the switch module must perform at high speed. The performance achieved by the PIN diode switch is illustrated in Figures 4a and 4b. Including a propagation delay of ≈ 50 nanoseconds associated with control and driver circuitry, the switch turns on in ≈ 200 nanoseconds; the turnoff time is slightly less as shown in the figure. Figure 4b shows the phase-settling time. During switch turn-on, the phase of the output signal settles to within two degress of final phase in less than 200 nsec, or to a small fraction of one degree in about 300 nsec; at turn-off, the phase settles somewhat faster. Switches with characteristics similar to these are used in all of the output and LO switch modules although only the output switches need these switching speeds.

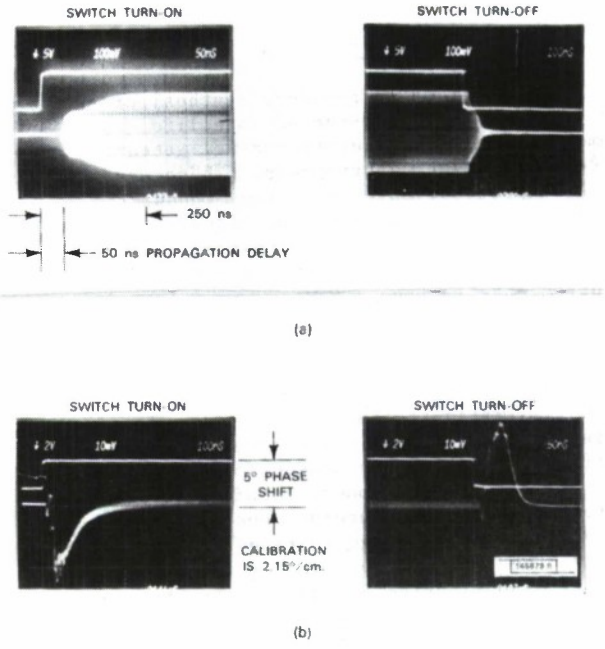


Fig. 4. PIN Diode Switch Characteristics

VCO/RF Section

Figure 5 is the block diagram for the five identical synthesizer VCO/RF sections. A voltage-controlled oscillator (VCO) provides

the RF source for each synthesizer. The buffer amplifier section provides isolation between the VCO and the output switch module, sets the output power level by adjustment of attenuator value, and provides a VCO signal input to the mixer section. The mixer down-converts the VCO by mixing it with one of the three fixed LO frequencies supplied from the LO switch module to provide an IF feedback signal to the synthesizer controller for phase-locking the VCO. The IF signal is amplified and then modulated in a single-sideband modulator by a signal from the controller which provides fine frequency control. The fine tune signal is applied through a phase-quadrature network which includes a 180° phase shifter to provide sideband selection. The modulator output is amplified and filtered to attenuate harmonically-related responses. The remainder of the phase-lock loop is discussed further in the synthesizer controller section of this paper. Telemetry monitoring of RF signals is also provided at the RF output, IF output, and LO input ports.

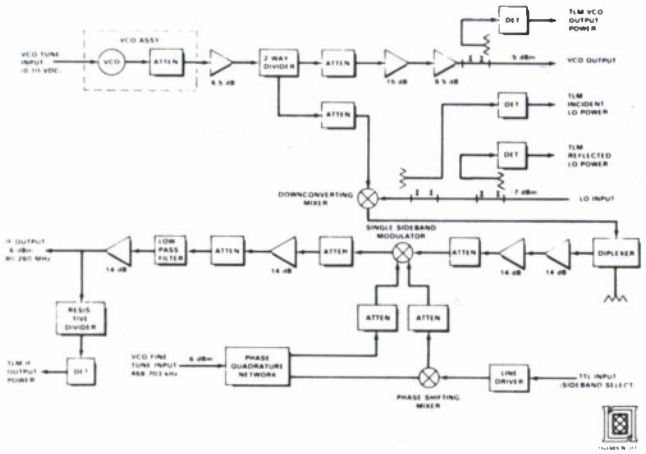


Fig. 5. VCO/RF Section Functional Block Diagram

The voltage-tuneable RF source for each of the five synthesizers is provided by a bipolar microwave transistor (Avantek AT41470) configured as a common base, negative-resistance oscillator with the tank circuit connected to the emitter and the RF output taken from the collector (Figure 6). The output frequency (< 2 GHz) is tuned over a several hundred MHz range by applying a DC voltage to the varactor diode in the tank circuit. Inductance in the base circuit ensures the presence of a negative input resistance at the emitter. The output network includes three circuit features: a series trap which flattens the output power frequency response; a π-attenuator to improve matching and isolation; and a notch filter to reduce the second harmonic level at the lower end of the operating band. In order to achieve the desired oscillator phase-noise performance, transistors with low 1/f noise levels were selected. In addition, DC power is filtered and regulated to provide stable oscillator performance. The VCO circuitry utilizes a low dielectric constant teflon fiberglass PC board to reduce stray capacitance and to interconnect the discrete components comprising the oscillator. Top and bottom covers attach to the PC board to provide an enclosure for isolating the VCO.

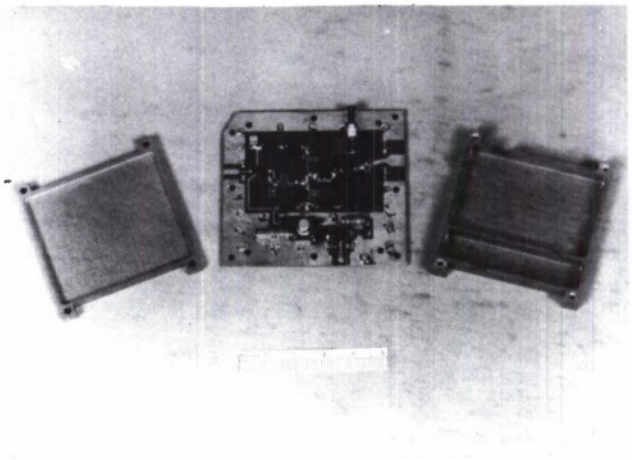


Fig. 6. VCO Circuitry

The performance achieved by the VCO is shown in Figures 7 and 8. The normalized frequency, VCO tuning slope, and output power are plotted vs. input tuning voltage in Figure 7. Typical tuning sensitivity varies from 50 to 100 MHz/volt over the tuning range, while the corresponding output power variations of 1.0 to 1.5 dB are typical for this oscillator design. Table I tabulates the measured phase noise performance

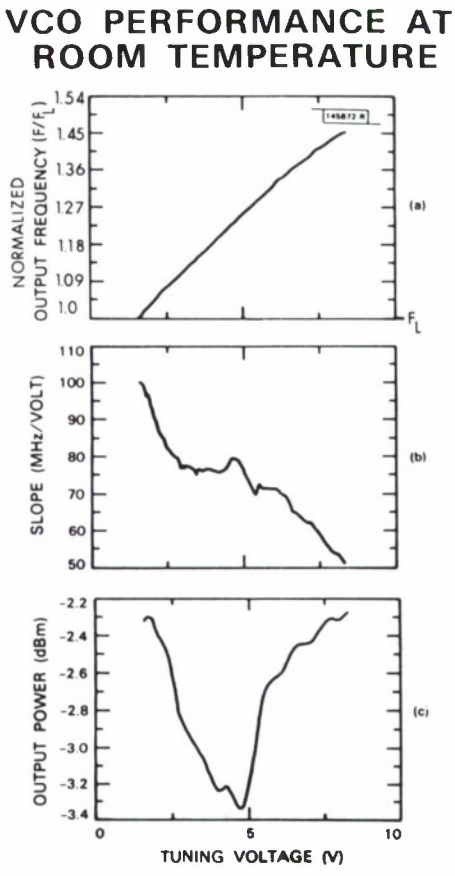
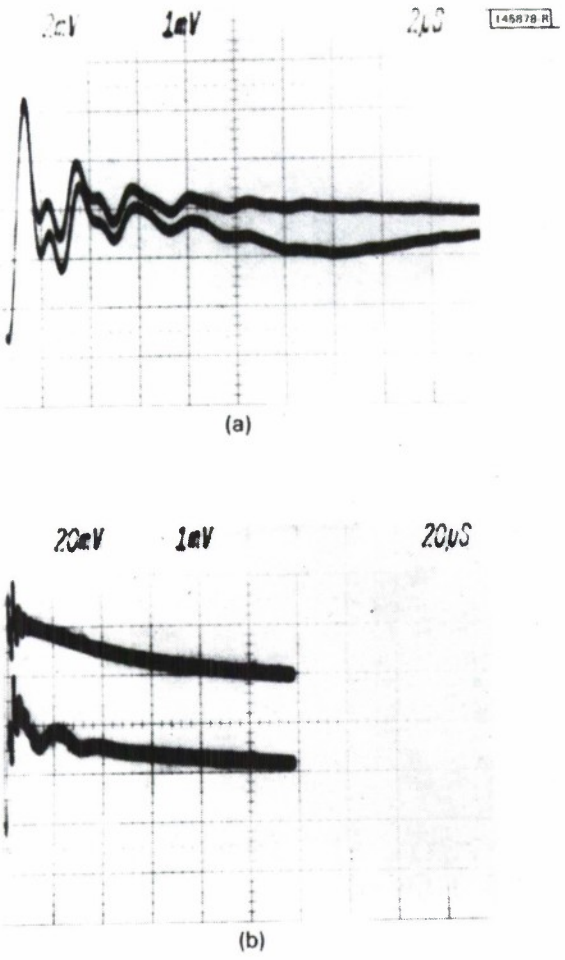


Fig. 7. VCO Normalized Frequency, Tuning Slope And Output Power



NOTE: UPPER TRACE IS TUNING VOLTAGE DRIVE
LOWER TRACE IS DISCRIMINATOR OUPUT (100 KHz/div)

Fig. 8. VCO Settling Time And Post Tuning Drift

TABLE 1. VCO PHASE NOISE PERFORMANCE WITH TEMPERATURE AS A PARAMETER.

Temperature (°C):	REF	24	40	66	10	-20	-40
Tuning Voltage (V.)	SSB PHASE NOISE IN dBc/HZ						
1.178888684140							
1.377709067845	-101.4	-100.3	-102.9	-101.7	-100.8	-100.5	-100.1
1.577562271542	-102.2	-102.1	-102.5	-103.6	-101.8	-100.8	-100.0
1.778112230140	-104.2	-103.8	-104.1	-104.6	-102.8	-102.5	-102.5
1.98533728856	-105.8	-104.9	-105.7	-105.5	-104.0	-104.0	-104.3
2.284800822240	-106.6	-106.8	-106.4	-106.4	-106.8	-106.1	-106.0
2.438816429587	-107.3	-106.9	-107.1	-106.9	-107.8	-107.4	-107.5
2.677411344487	-107.7	-107.4	-107.4	-106.5	-107.5	-107.0	-107.5
2.925734805603	-107.5	-107.5	-107.4	-106.9	-107.6	-107.0	-107.8
3.180828875417	-107.3	-107.7	-107.4	-106.4	-107.7	-107.4	-107.5
3.437550858772	-107.3	-107.6	-107.3	-106.6	-107.1	-107.3	-107.2
3.695544805606	-107.2	-107.1	-106.8	-106.4	-106.8	-107.1	-106.9
3.953138893515	-106.3	-106.7	-106.4	-105.7	-106.6	-106.5	-106.6
4.211662751113	-106.2	-106.7	-106.4	-105.9	-106.7	-106.6	-106.8
4.469637856697	-106.3	-106.4	-106.1	-106.8	-106.2	-106.2	-105.9
4.719072508958	-105.6	-106.3	-106.0	-105.3	-106.8	-106.8	-105.8
4.971862727747	-106.8	-106.3	-105.8	-105.8	-106.8	-105.7	-105.3
5.237541154505	-106.1	-105.9	-105.9	-105.8	-105.9	-105.7	-105.6
5.512888617755	-106.2	-106.6	-106.8	-105.4	-106.5	-106.5	-106.1
5.795168722282	-106.5	-106.8	-106.5	-105.9	-106.2	-106.1	-105.6
6.088858306873	-106.8	-106.5	-106.2	-105.5	-106.2	-105.9	-105.8
6.335651648876	-106.4	-106.8	-106.3	-105.7	-106.5	-105.6	-105.4
6.626842240879	-107.1	-106.4	-106.4	-105.7	-106.2	-105.6	-105.4
6.920815241105	-106.0	-106.9	-106.6	-105.9	-107.8	-106.7	-106.1
7.23824480552	-106.4	-106.9	-106.8	-105.7	-106.6	-106.8	-105.5
7.556180833187	-106.4	-106.3	-106.2	-105.5	-106.4	-106.2	-105.4
7.890681080886	-106.4	-105.8	-105.6	-105.1	-106.1	-105.7	-105.5
8.263548711180	-105.7	-105.6	-105.7	-104.8	-106.8	-105.9	-105.8
8.617482905224	-105.2	-105.3	-105.1	-104.6	-105.6	-105.5	-105.8
8.97421570780	-104.9	-104.4	-104.3	-104.4	-104.6	-104.9	-105.2
	-103.8	-103.6	-103.8	-103.9	-103.3	-103.8	-104.8

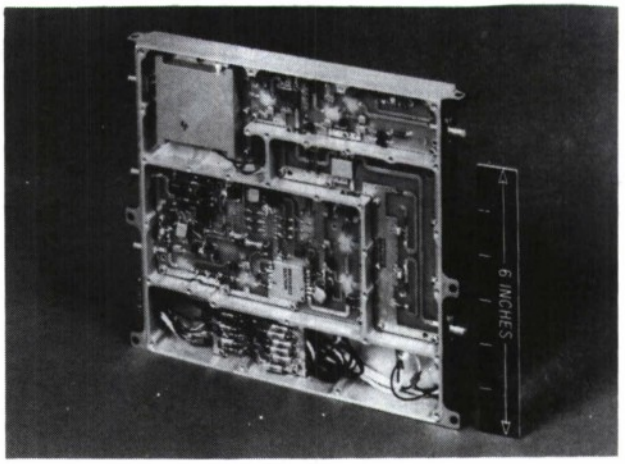


Fig. 9. VCO/RF Section Assembly

for several operating temperatures; typical SSB phase noise at 50 KHz offset is less than -100 dBc/Hz. The VCO settling time and post-tuning drift are shown in Figure 8. A settling time of 40 microseconds and post-tuning drift of less than 100 KHz/100 microseconds are also characteristic of this design.

Each VCO/RF section is packaged separately to eliminate cross talk between synthesizers. A complete VCO/RF section module is shown in the photograph of Figure 9. Individual compartments for each of the circuit boards provide the necessary isolation between circuits. Conventional hybrid circuit fabrication techniques are utilized throughout the module. High-rel components including miniaturized flatpack circuits (power divider, mixer, single-sideband modulator, phase-shifter) and modular cascadable amplifiers are used in conjunction with discrete components. The amplifiers are operated at a supply voltage of 5.0 volts to conserve dc power. RF signal paths are realized by microstrip transmission lines on glass-epoxy printed circuit boards. Microstrip couplers which are integral to the PC boards are used for monitoring RF power levels in conjunction with back diode detectors to provide telemetry information. The phase-quadrature network, filter, diplexer, and all attenuators are comprised of high-rel discrete components. RFI filtering of the DC power and telemetry lines is also employed as in the switch modules. Each VCO/RF section requiresapproximately 1.5 watts of DC power and weighs approximately 1.5 pounds.

The VCO/RF sections are tested extensively over temperature to verify performance. Prior to installing the VCO, the RF monitors are calibrated with respect to frequency, power level, and temperature. After installation of the VCO, both stabilized temperature testing and continuous temperature cycling over the range of -40°C to +66°C are repeated for each module as with each of the switch modules.

Careful alignment of the phase-quadrature network and IF filter, together with high-quality

single-sideband modulators, are required to achieve the necessary spurious signal rejection on the IF feedback signal. The graph of Figure 10 plots typical spurious signal rejection relative to the used sideband level. In addition to maximizing carrier and unused sideband suppression, supression of responses at and around the second and third harmonics of the carrier is required in this system. The development of single-sideband modulators with low modulation products was an essential factor in obtaining the desired spurious signal performance.

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SUPPRESSION OF MODULATION PRODUCTS (dB),(Carrier/Modulation Harmonic)

IF																	
FREQUENCY	1,3	1,1	1,0	1,1	1,3	2,2	2,1	2,0	2,1	2,2	3,3	3,2	3,1	3,0	3,1	3,2	3,3
120.74000	60	41	40	0	52	46	56	53	41	35	00	00	69	77	62	65	33
137.43900	68	35	40	0	49	46	58	54	42	33	00	00	63	71	66	71	33
146.29100	60	31	42	0	50	56	67	50	44	31	79	79	63	74	52	67	33
155.41000	58	30	40	0	48	55	63	51	53	34	00	70	63	73	53	65	35
164.47900	59	32	41	0	49	65	76	54	63	38	00	79	66	70	55	63	37
173.81200	59	33	44	0	49	82	70	57	64	38	79	70	69	73	58	68	39
183.00300	59	34	42	0	49	81	74	57	64	33	00	79	70	00	61	69	39
192.15100	58	37	39	0	49	70	74	58	60	30	01	70	72	77	63	67	40
200.97300	58	39	40	0	52	76	75	60	61	29	00	01	72	70	66	67	40
209.00900	56	37	41	0	54	71	76	55	58	27	79	70	72	79	64	69	41
218.56400	56	33	41	0	51	70	70	52	61	27	01	00	75	79	63	70	43
227.52000	59	31	42	0	52	71	76	50	61	27	79	79	76	79	63	72	45
236.73400	63	30	45	0	52	74	78	50	63	28	02	00	78	78	64	77	47
246.65200	58	30	45	0	49	75	00	52	66	29	78	00	01	77	66	78	48
256.61600	55	33	45	0	51	74	76	55	69	31	79	79	79	79	69	77	50

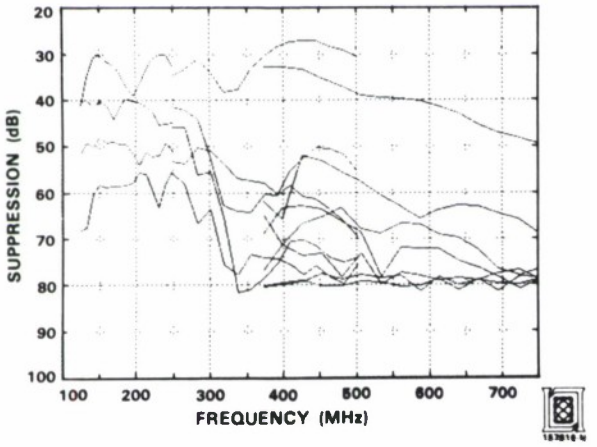

Fig. 10. IF Feedback Signal Spurious Signal Rejection

The output power vs. tuning voltage for one channel of the receive synthesizer is plotted in Figure 11 for temperatures of -40°C, 25°C, and 60°C. These responses include that of the output switch module in addition to the VCO/RF section. Total power variation of 2 dB over the tuning range and operating temperature range is observed for this channel; variations of < 3 dB are typical.

The RF portion of the receive synthesizer, including three VCO/RF sections and two switch modules, is assembled as shown in Figure 12. Each individual module is attached to the adjacent one, and each module includes provisions for attachment to the spacecraft. Electrical connections are accomplished with semi-rigid coaxial cables between modules and individual DC/telemetry connectors for each module. The RF portion of the

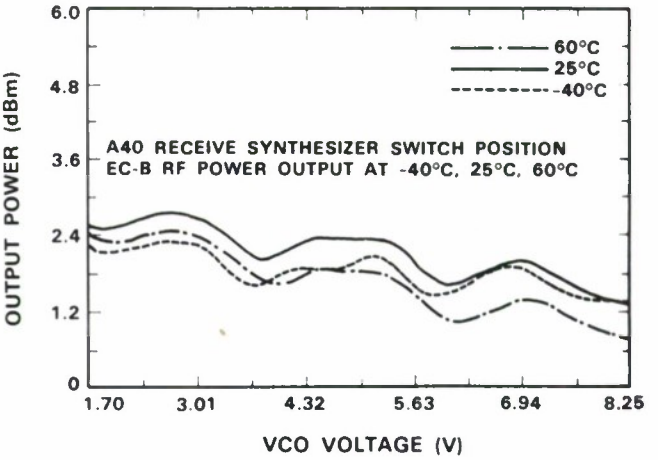

Fig. 11. Synthesizer Output Power With Temperature As A Parameter

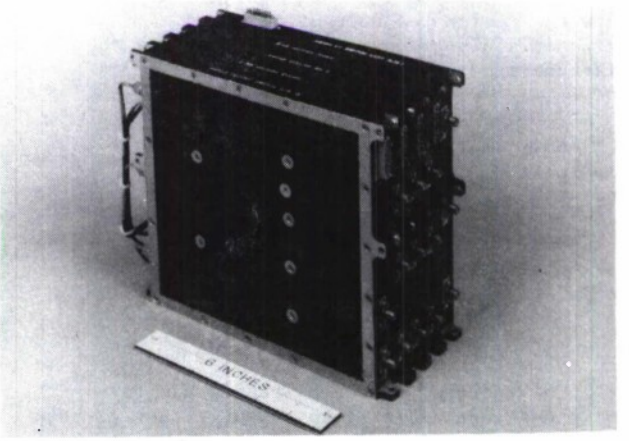

Fig. 12. Receive Synthesizer RF Section

transmit synthesizer, comprised of one switch module and two VCO/RF sections is assembled in a similar fashion. Complete performance testing, including stablized temperature testing and continuous cycling, is repeated on these assemblies. Qualification-level shock and vibration testing of the prototype system and acceptance-level vibration testing of the flight systems is also performed at this level of assembly, and the synthesizer controller is tested separately.

Synthesizer Controller

Figure 1 shows the interconnections of the synthesizer controller and the frequency synthesizers. This system consists of five identical phase lock loop synthesizers, three of which are used for the receiver and two for the transmitter. Hopping or fix-tuned frequencies are outputted over the two receiver channels and the single transmitter channel.

The signals which drive the controller provide mode, configuration, fix tune commands, hopping data and timing signals. MFSK data commands are also inputted as a transmitter mode of operation.

Hop Rate Control

In operation any one of the three receiver synthesizers is configured to be low-hop rate, and by default, the other pair are high-hop rate.

The high-hop rate pair are pinged-ponged in order to obtain high switching speed. The high-hop rate ping-ponged output and the low-hop rate unit drive the dual single pole-three throw output switch.

The transmitter frequency synthesizers are ping ponged in either high or low-hop rate, and provide a single output to the transmitter with low-hop rate operational redundancy.

Hop Control

Any of the high or low hop rate units can be commanded to NO HOP. Execution of this command puts the designated unit at mid band. A no hop command is also required before entering the fix-tune mode.

Fixed Tuning

Any combination of the receiver and transmitter frequency synthesizers can be independently commanded to be fix-tuned. In this mode the frequency synthesizers can be tuned over a band of frequencies that is ∿ 60 MHz wider than the hopping bandwidth. The additional tuning bandwidth is used for test purposes.

Receiver Output Control

The receiver output switching can be commanded independently to output either or both the high-hop rate or low-hop rate frequencies in any combination; for example, high-hop rate or low-hop rate may be outputted to both channels or high-hop rate to one and low-hop rate to the other.

Controller Configuration

Figure 13 shows the details of the controller topology. The section enclosed in dotted lines is blocked off into 12 units which represent the 12 circuit boards in the controller module. The data controller handles the incoming hopping, fix tune and MFSK data. It stores and translates the incoming data and selectively outputs the encoded data over a 36 bit data bus which drives all five programmable dividers and loop filters. The timing controller generates all of the internal timing signals required. It provides the data strobes and enables which capture and store the incoming data, the ping-pong timing signals and the clocks which strobe the 36 bit data bus into the designated frequency synthesizer which is to be tuned.

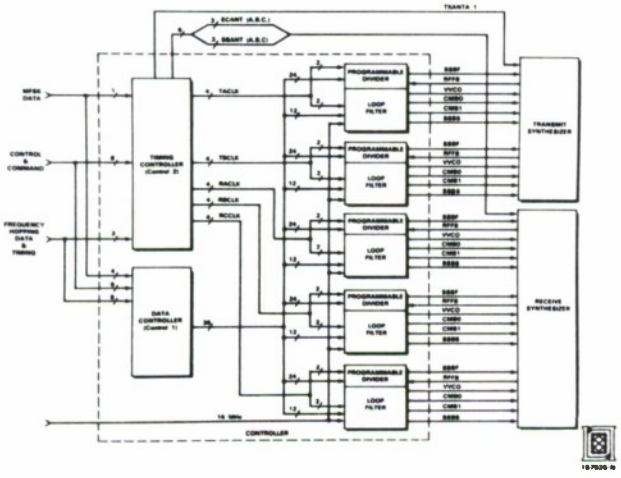

Fig. 13. Controller Configuration

There are also five pairs of identical programmable divider and loop filter boards. Each pair is associated with one of the three receiver and two transmitter frequency synthesizers.

The reference frequency used by the phase detector on the loop filter board is derived from a 15 MHz input signal.

Figure 14 shows the phase lock loop (PLL) topology for any one of the five frequency synthesizers; they are all identical. The dotted lines indicate the circuit division between the various units. The VCO and associated circuits are on the right side of the diagram. The controller module which contains the loop filter and programmable dividers are on the left. A fine frequency synthesizer which is digitally implemented is also part of the programmable divider.

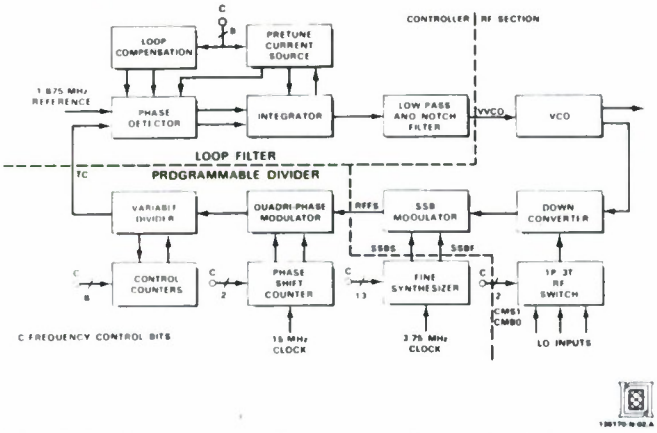

Fig. 14. Synthesizer Phase-Lock Loop Block Diagram

The control or frequency command data from the data controller drives all of the various circuits designated with the letter "C" over the 36 bit data bus. These are the commands which tune the synthesizer.

Loop Operation

The RF feedback signal (RFFB) which contains the fine frequency steps drives the programmable divider board. A sideband select signal (SSBS) determines whether upper or lower sideband is selected. The feedback signal drives a quadriphase modulator which is controlled by a phase shift counter and advances the phase by 0, 90, 180 or 270°. This has the effect of adding multiples of 1/4 of the reference frequency step sizes to the feedback signal. The quadriphase modulator output then drives a programmable variable modulus divider to produce an output at

the reference frequency called TC or terminal count.

Loop Filter

At the start of a hop, the frequency synthesizer that is to be tuned receives the command data over the data bus and initiates the pretune cycle. In this operation, pretune data which is stored in a ROM in the pretune current source drives the integrator and produces a voltage which tunes the VCO to a frequency close to the commanded value.

When the pretune voltage equals the tuning voltage a comparator shuts off the pretune cycle and enables the phase detector.

The phase detector is driven by TC and the reference frequency. It outputs a pair of pulses offset in time proportional to the phase difference between TC and the reference frequency. The pulse pair drive the differential integrator which generates an error signal to tune the VCO in the proper direction to time align the pulses. When this occurs, the VCO is phase locked to the reference, and the frequency synthesizer is ready for use on the next hop. Loop compensation is implemented in order to obtain optimum performance across the whole band.

As a power saving measure, the pretune and compensation data are stored in the same prom. After the pretune cycle is completed, the compensation data is loaded into a CMOS buffer and the prom is put into a low power mode until the next tune cycle. This feature conserves about a watt of DC power for the five synthesizers.

Telemetry

The tuning voltage and lock/unlock status for each of the five frequency synthesizers as well as an assortment of command indicators are outputted from the controller for telemetry use.

Hardware

Figure 15 shows the controller module hardware. There are 12 circuit boards, which includes the timing and data controller and five pairs of programmable dividers and loop filters. The coaxial connectors on the side panel are grouped in clusters of three to connect the feedback signal, tuning voltage and fine frequency steps to each of the five units. The last connector on the right provides the 15 MHz input. The side connector plate contains the power and other I/O signals required for controller operation.

Fig. 15. Controller Module

Figure 16 is a photograph of the loop filter (one of five identical circuit boards). This unit contains an assortment of digital and analog circuits mounted on a multilayer printed circuit board. The two coaxial connectors on the top are for the tuning voltage output and 15 MHz input. The bottom edge connector provides the interface for the power, data bus and telemetry signals.

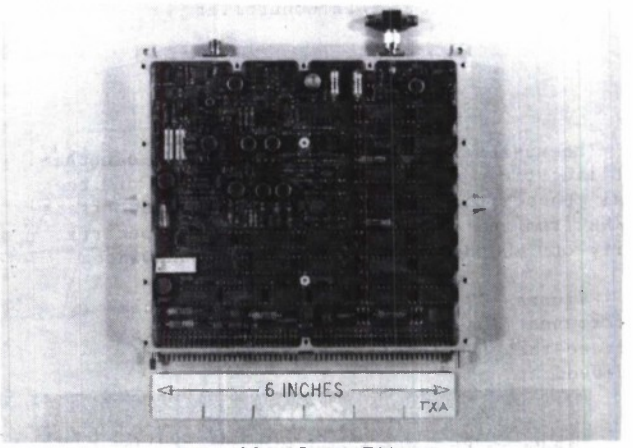

Fig. 16. Loop Filter

Figure 17 is a photograph of the programmable divider. There are also five identical programmable divider printed circuit boards. The two top connectors are for the fine synthesizer output and the feedback input signal. At the upper right corner is the SSBM input and the left side contains the DAC and output filter for the fine synthesizer.

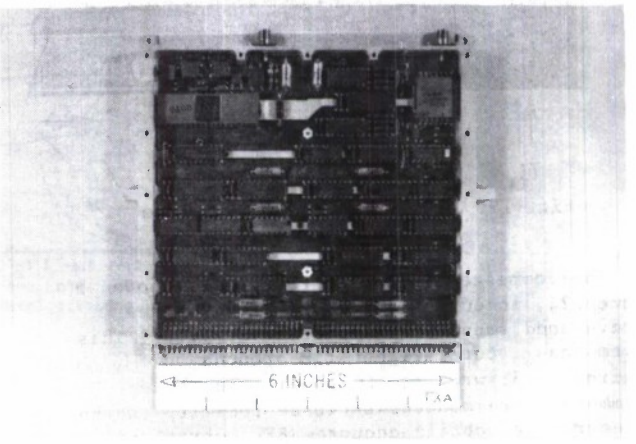

Fig. 17. Programmable Divider

Figure 18 depicts the controller board. This photograph shows one of the digital controller boards which contains a combination of LS series and CMOS IC's. The board is wired with stitch-weld wiring.

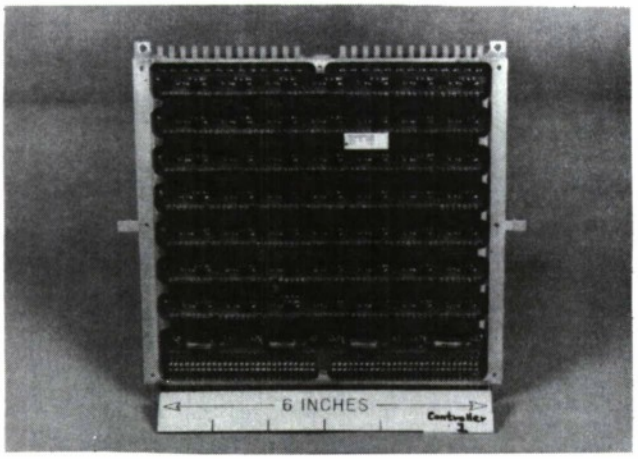

Fig. 18. Data Controller

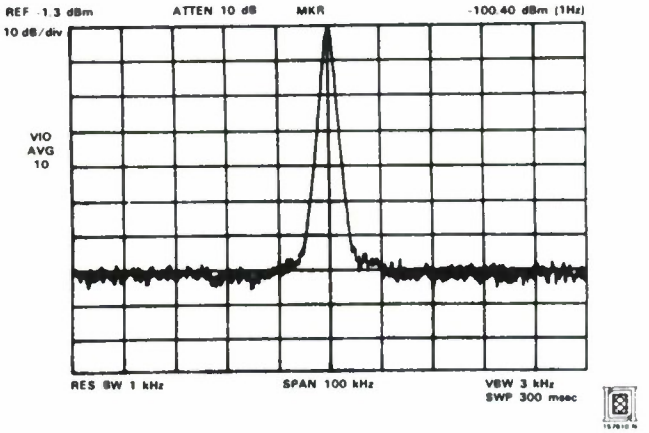

Fig. 20. Synthesizer Phase Noise

System Performance

The system specification goals were to obtain settling times of < 50 μs to be within 5° of the final phase, phase noise of < 90 dBc/Hz at offsets 30 KHz from the carrier, and an average spectral purity of -40 dBc across the hopping bandwidth.

Figures 19, 20 and 21 show the typical performance measurements and the data plots indicate that the specification goals were achieved.

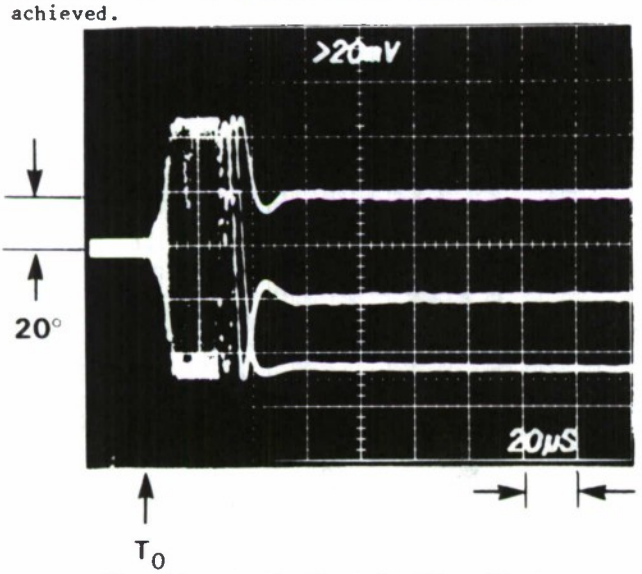

Fig. 19. Synthesizer Settling Time

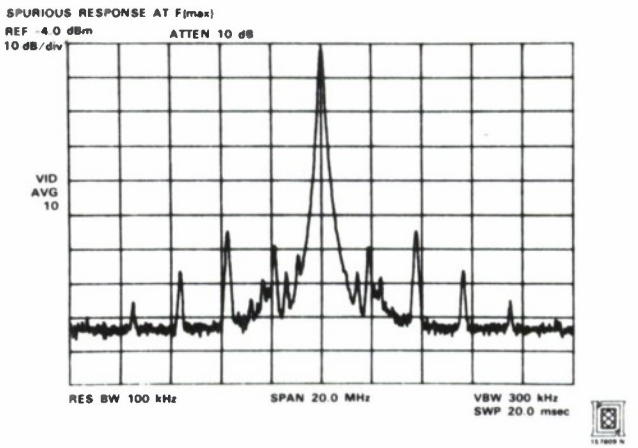

Fig. 21. FEP Frequency Synthesizer Output Spectrum

The complete synthesizer system is shown in Figure 22, including the controller and the receive and transmit RF module assemblies. This system has a total weight of 28 pounds and requires ∿ 35 watts of DC power. The three assemblies are mounted in close proximity on the spacecraft to obtain adequate RFI control and to facilitate electrical interconnection.

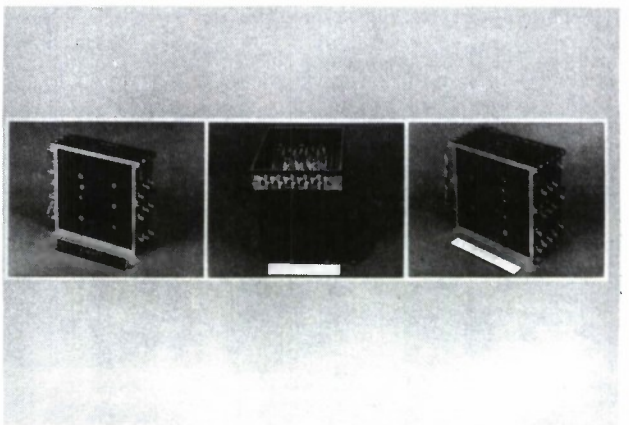

Fig. 22. Frequency Synthesizer System

Conclusion

A space-flight qualified synthesizer system with operational redundancy has been realized. This system is capable of frequency switching over several hundred megahertz at rates of many kilohertz. Each PLL synthesizer requires ≈ 7 watts of DC power and weighs ≈ 5.6 pounds including the representative proportions of control and switching circuitry. High-rel components, careful construction techniques, and thorough testing were used to ensure the reliability necessary for this satellite application.

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Technical support in fabricating and testing the synthesizer components and system was provided by Thomas Hotaling, Timothy King, Vincent McCabe and John Newey.

Reference

1. R. R. Rhodes, W. K. Hutchinson and B. H. Hutchinson, Jr., "Frequency Agile Phase-Locked Loop Synthesizer for a Communication Satellite"; IEEE 1980 National Telecommunications Conference Record, Vol. 1, pp. 22.3.1 - 22.3.6.

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