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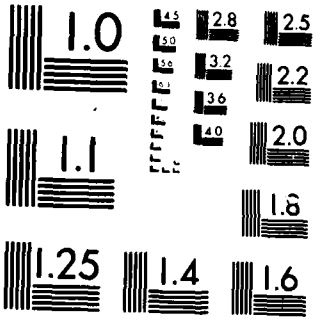

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The main scientific achievements have been in the following areas: Theory of communication complexity, lower bounds for VLSI computations, algorithms and special - purpose architectures for VLSI, theory of computation, CAD tools, parallel computation and fault-tolerant distributed computation.

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Research in Distributed and Parallel Systems

Final Report

Joseph Ja'Ja'
and
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US Army Research Office
Contract Number DAAG 29-82-K-0110

The Pennsylvania State University

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Summary of Most Important Results

We have proposed to do research in four related areas: design of parallel algorithms, design of efficient VLSI circuits, study of movement in distributed computations and the use of randomness in parallel computations.

We have been quite successful: the project has yielded well over 30 publications, two completed Ph.D. dissertations (all recipients are currently holding academic positions, one at University of Southern California, and one at Harvard University), several MS papers, and three additional Ph D dissertations in final phase of completion. We discuss the scientific accomplishments of some of the papers below. It may be significant to note that the results are not only appearing in prestigious journals (SIAM J. COMPT., JACM, Journal of Computer and Systems Sciences, IEEE Transactions on Computers) but they have been presented at *very selective conferences* (like the MIT VLSI Conference (1 paper) the IEEE Foundations of Computer Science (5 papers) and the ACM Principles of Programming Languages Conference (1 paper)). Usually only one of 4 or 5 submissions are accepted at these conferences, and the submitted papers are generally of very high quality.

On the more applied end of things, as a result of ARO support there are now active VLSI design facilities at Penn State. Several chips have been designed and fabricated. In addition, considerable progress has been made in research about synthesis of VLSI circuits and CAD tools for VLSI design. At university of Maryland, J. Ja'Ja' and his students have developed a new methodology to compile logic that does not use the PLA approach. At Penn State, Larry Jones, a Ph.D. student supported by the contract, and J. Simon have developed on incremental hierarchical circuit editor based on the precise

and rigorous foundations of attribute grammars.

We believe that our main scientific achievements have been the following:

Theory of Communication Complexity: Together with our students V.K. Prasanna Kumar and R. Paturi, we have contributed significantly to this new theory. Our reported results characterize precisely the amount of information that needs to be exchanged between two computing agents in order to compute a given function. We have extended the theory to interesting new models of computation and obtained elegant mathematical charecterizations. Our work is extensively referenced and has inspired new theoretical developments.

Lower Bounds for VLSI Computations: Using information transfer arguments (and in many cases, developing new powerful methods to account for information flow), we have been able to prove minimal requirements on the area and the time of VLSI chips to compute a large number of problems. Some of the lower bounds are general, while many are applicable to interesting problems like graph connectivity, sorting and problems in signal processing. Some of our earlier work has been included in Ullman's text on VLSI.

Algorithms and Special-Purpose Architectures for VLSI: We have developed novel architectures based on recently discovered fast algorithms to solve several basic problems in signal processing. Our approach will result in fully pipelined bit serial architectures which require no control units. We have shown that the aera is about the minimum possible and the overall delay is within an optimal order of magnitude. An essential ingredient of these implementations is the use of digit online adder and multiplier cells. Several chips have been fabricated for the DFT processor. Other type of architectures we

considered uses serial memories (such as those appearing in magnetic disks, magnetic bubble, charge coupled devices, and even VLSI shift registers) that have a high information density and low cost. We have developed optimal algorithms for sorting, computing the discrete Fourier transform and matrix operations.On the other hand, optimal algorithms for several graph problems were obtained by one of our students (S. Hambrusch).

Theory of Computation: Although not a main focus of research, the techniques used in some of our proofs yielded excellent results in nearby areas of theoretical computer science. For example, arguments used for information transfer (Kolmogorov complexity) gave powerful lower bounds on the time required for certain on-line computations. Similarly,very sharp lower bounds have been obtained for certain probabilistic space-bounded computations and restricted ways of computing the permanent.

CAD Tools: A new approach for compiling logic has been developed by Ja'Ja' and his students. The standard approach is usually based mostly on using PLA's and sometimes Weinberger Arrays. Our method tries to exploit all the symmetries inherent in the given functions and forms a layout that is especially tailored for symmetric or partially symmetric functions. We can rigorously show that if the given functions have a reasonable degree of symmetry, then our method will be considerably better that any of the known methods. In case no symmetry is detected, some transformation are applied and the resulting functions are guaranteed to have a certain degree of symmetry. We can show that we will always end up with a layout that is at least as good as the one produced by the PLA approach. A new system SYMBL, SYMmetric Boolean Layout, has been built and we are in the process of

experimenting with it.

Larry Jones and J. Simon are in the final stages of implementing a structured circuit editor based on attribute grammars. The system will maintain dynamically properties of the circuit being designed. When a subcircuit is redesigned only the changes caused by the substitution will have to be recomputed. The selection of what to recompute and in what order is done fairly optimally by the system. The algorithms, an extension of similar techniques used for incremental grammar- based editors, are new. We believe that such systems are going to be practical, and will enable the construction of efficient "expert" editors for VLSI designs. As an illustration of the power of the formalism, it was possible to add to the sytem a version of the MOSSIMII circuit simulator with very little effort. While the implementation is very slow, it took only few days of programming to bring it up. A preliminary report of this work was given at the Principles of Programming Languages Conference this January.

In addition to the major pieces of work discussed above, several of our students have done work on VLSI design tools or designed small chips. There was work on PLA generators, Weinberger Array Generators, design of adders as well as a large number of MS papers that although not supported by the contract, would not have been possible without the initial impetus to VLSI design at Penn State given by the contract.

Parallel Computation: Much research effort has been expanded into mapping algorithms designed for not realistic general purpose computers into models that can in fact be realized, either with present technology, or with technol-

ogy that should be available within a decade. We mention the following results. With Y. Chang (a graduate student supported by the project) and S. Hambruch, we investigated the feasibility of mapping parallel algorithms with given submodules into systolic arrays. Unfortunately we showed that except in very simple cases such attempts are bound to fail: even the problem of deciding whether a given module is feasible is already NP-complete. Another major result, obtained recently by Y Chang and J Simon, concerns routing of messages on the hypercube. We show that it is possible to pipeline routing instances efficiently. More precisely, it has been known that it is possible to route probabilistically on an n-dimensional hypercube in time O(n). We show that this is true even if one starts a new routing instance every c units of time. More precisely, there are constants c and d such that is a new batch of messages appears at times ic for i=0,1,2,.... then the messages will reach their destination by time ic+dn with overwhelming probability. It was not known previously that n batches could be routed in less than $O(n^2)$ time, nor that the probabilistic scheme could be repeated indefinitely without serious degradation. Since several hypercube multicomputers have been built recently, such schemes have more than academic interest.

Fault-Tolerant Distributed Computation: Massively parallel computers will have failing components. Our research has dealt with the problem in two important ways:

a) the reduced hardware architecture proposed by Ja'Ja' and Owens is well suited for graceful degradation in the presence of certain classes of processor failure.

b) Very recent work by Berman and Simon deals with clock failures. We

show that there is only a constant factor slowdown if one uses a self-timed circuit to simulate a fully synchronous one. Since self-timed circuits have no global clock, and the result remains true under fairly strong modes of local clock skew (like no assumptions on nearby clock ratios), the rather surprising result (after all slow processors could delay each other and such delays could cascade intolerably) may have practical implications for clocking disciplines for WSI processors.

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S. Wu, Ph.D. expected 1986.

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