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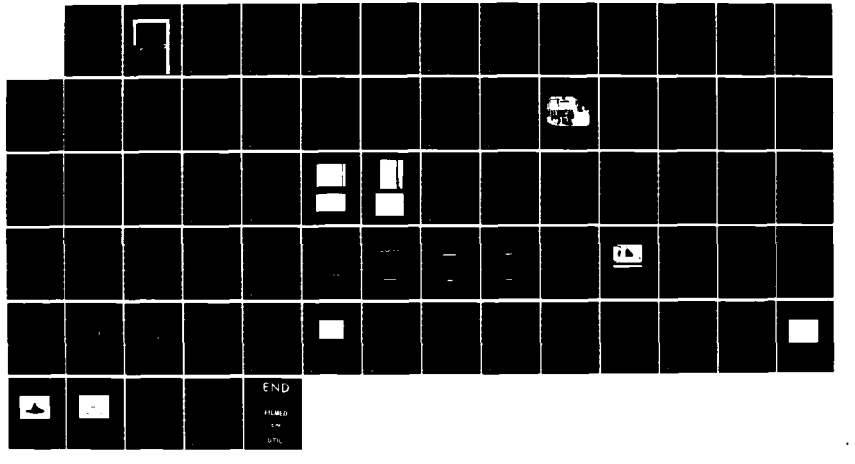

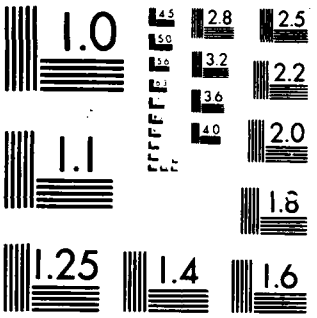

X-BAND GaAs ISIS IMPATTs

JULY 1985

FINAL REPORT

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SECTION 1
INTRODUCTION

1.0 PROGRAM OBJECTIVES

The underlying purpose of this nine month program was to demonstrate the feasibility of synergistic power in Gallium Arsenide Integrated Series IMPATT Structures (ISIS). In order to demonstrate such a feasibility, the program entailed the following:

Task 1.

(a) Designing of appropriate doping profiles for GaAs X-band ISIS diodes.
(b) Growing Integrated Series IMPATT Structures using Vapor Phase Epitaxy (VPE),
(c) Characterizing the doping profiles of the ISIS wafers.

Task 2.

(a) Processing ISIS wafers grown by VPE into single mesa diodes with integral heat sinks.
(b) Processing ISIS wafers grown by Molecular Beam Epitaxy (to be provided by NRL) into single mesa diodes with integral heat sinks.
(c) Assembling diodes of (a) and (b) into standard packages compatible with coaxial mounts.

Task 3.

Evaluate the DC and RF results for (MBE and VPE) ISIS diodes.

Upon completion of the above, it was agreed that a total of twenty-five ISIS diodes (10 VPE and 15 MBE) would be delivered. The deliverable items, fabricated at M/A-COM, should exhibit the following characteristics:

Peak Output Power : 10 Watts (at 10 percent Duty Cycle; 1 μs pulse width).

Operating Frequency : 10 GHz

Conversion Efficiency: 15-18 percent

1.1 BACKGROUND

For several years, the desired objective of the X-band GaAs IMPATT-diode development has been to increase their efficiency and power output capabilities. This objective has been sought in response to the need for reliable, high power IMPATT modules which are to be used as replacements for beacon transponder magnetrons and for use in systems such as weather radars and active missile seekers. For the applications mentioned above, several IMPATT diodes are circuit and/or device combined so as to yield high power modules. However, as the number of diodes is increased, circuit complexity and combiner losses impose limitations on the power level that can be achieved. In order to alleviate this situation, it is necessary to improve on the performance of the individual devices.

Theoretical studies of GaAs double-drift IMPATT diodes have predicted their superiority over single-drift devices. However, state-of-the-art laboratory results of the former devices have shown them to exhibit a conversion efficiency much lower than the theoretical value. While high output powers have been achieved from laboratory x-band GaAs double-drift diodes, reports have seldomly addressed the issue of their large scale-uniform production which would be required for power combining applications. Due to limited information, it is speculated that the large scale production problems and improvement in device performance are associated with material growth and characterization techniques. First, the reproducible growth of P-type GaAs layers with precisely controlled doping profiles is very difficult, thereby resulting in poor yields. Second, the characterization of double-drift structures is complex. Uncertainty of the doping profile near the crucial avalanche region

results in unreliable evaluation data. This uncertainty makes it difficult to correlate device performance with material parameters.

Based on the dilemma outlined above, we embarked on the development of a novel Integrated Series IMPATT Structure (ISIS) device which consists of two single-drift Read type IMPATTS epitaxially grown in series. While the ISIS device eliminates the use of low doped P-type epitaxial technology, as required by x-band double-drift IMPATTS, it offers the same output power potential as a double-drift diode. Furthermore, since the need for low doped P-type technology is eliminated, ISIS diodes can be produced with a much higher yield due to the well-established N-type epitaxial techniques.

1.2 SUMMARY OF TASK ACHIEVEMENTS AND PROBLEM AREAS

In order to achieve the objective of this program, much emphasis was given to (a) the design of an appropriate ISIS doping profile, (b) the preparation of such a structure using halide vapor phase epitaxy, and (c) the evaluation of the individual layers within the ISIS epitaxial wafers.

An appropriate high-low (HI-LO) ISIS doping profile was chosen to satisfy the power requirements for this contract. The design profile was acquired using a computer simulation program in conjunction with our knowledge and experience of HI-LO single-drift IMPATT diodes. Specific design considerations addressed issues such as unequal operating junction temperatures and injection of minority carriers across the tunnel junction in the ISIS diode.

In an attempt to verify our disign model and the ISIS concept, individual HI-LO IMPATT chips were physically stacked in ODS-275 packages. The RF results from the physically stacked chips were very successful and confirmed this ISIS concept as well as our design model. These results, including a discussion of the design considerations, are given in Section 2.

Some problems were encountered as the program proceeded towards

material preparation of the ISIS diodes using vapor phase epitaxy. They were observed while examining cleaved cross sections of the ISIS wafer in a scanning electron microscope. The problems were later identified with the diffusion of zinc atoms from the sandwiched P^{++} layer into the first grown active layer. Appropriate VPE growth techniques were successfully devised so as to eliminate this problem in subsequent ISIS growth runs.

Due to the complexity of the HI-LO ISIS doping profile and the presence of two junctions, conventional IMPATT characterization techniques were extended so as to evaluate the multi-layer epitaxial structure. In addition to the conventional characterization methods, an automatic electrochemical system (Post Office Profiler) was used to evaluate the doping density of the sandwiched N^{++} layer. Prior to the use of the Post Office profiler it was not possible to evaluate the doping of this layer and, hence, assess the extent of compensation caused by P^{++} memory effect. In our VPE system, we were routinely able to grow the sandwiched N^{++} buffer layer with a carrier concentration of $2.5X10^{18}/cm^3$ after depositing a highly doped P^{++} contact. These results as well as others on epitaxial growth and characterization techniques are presented in Section 3.

Processing of ISIS epitaxial wafers followed the routine steps used in the fabrication of X-band IMPATT devices. No problems were encountered as the VPE ISIS wafers were processed into single mesa plated heat sink chips. The latter were ribbon bonded into our OSD-275 packages and evaluated for their RF characteristics. Descriptions of the processing and assembly techniques are presented in Section 4.

Based on our evaluations, we were able to achieve the following DC and RF test results from one of our VPE ISIS wafers:

Zero bias capacitance = 57 pF
Breakdown voltage = 106 volts
Operating voltage = 120 volts

Operating current	= 1.5 amps
Peak output power	= 16 watts (at 10 percent Duty Cycle; 1μs Pulse width).
Conversion efficiency	= 8.7 percent
Operating frequency	= 9.406 GHz

At the end of this contract a total of twenty-five hermetically sealed VPE ISIS diodes, with test data similar to those given above, were delivered to the Navy. A more detailed presentation of the DC and RF test results is given in Section 5.

SECTION 2
ISIS DESIGN

2.0 DESIGN CONSIDERATIONS

The general nature of the ISIS is shown schematically in Figure 2.1. In essence, Figure 2.1 can be considered as two series connected single-drift IMPATT structures. Separating the two drift (active) regions is a P^{++} N^{++} junction. The avalanche regions are located at the interface of the P^{++}/N active layers. When processed and assembled, the ISIS chip is mounted epi down into the package (see Figure 2.2). In this case, the last grown P^{++}/N junction (or bottom diode in package) is positioned closer to the heat sink than the first grown junction (or top diode). During operation, the diode situated closer to the heat sink will dissipate the generated heat faster than the top diode. Consequently, the junction temperature of the top diode is hotter than that of the bottom diode.

Based on the thermal analysis of an ISIS chip thermo-compression bonded to a semi-infinite heat sink (package), the junction temperature of the top diode was estimated to be 35°C hotter than the bottom diode. For the analysis a chip diameter of 18 mils was chosen and copper was used as a semi-infinite heat sink. The operating junction temperature of the bottom diode was chosen to be 200°C. This value is consistent with those routinely encountered in our pulsed X-band single-drift IMPATT diodes.

As a consequence of the situation described, special consideration must be given to the design of the top diode. If, for example, both diodes are designed with the same doping profile, lattice scattering in the top diode will be greater, causing the fraction of carriers that reach high enough energy for multiplication to decrease. As a result, the oscillation frequency and output power of the top diode will be lower than that of the bottom diode. Therefore, the two diodes will be mis-matched and the overall performance of the ISIS diode will degrade. In order to remedy this mis-match between the

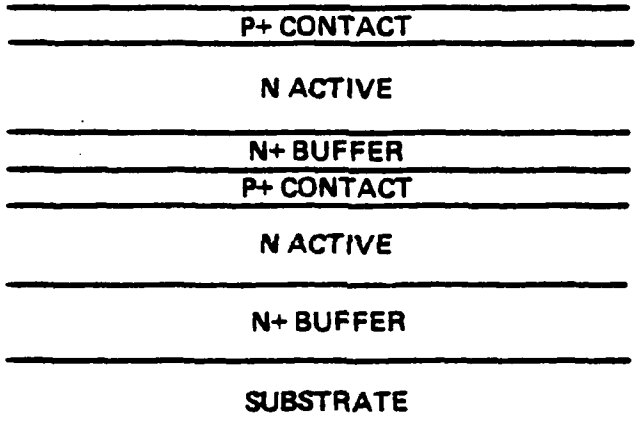

FIGURE 2.1 CROSS-SECTION OF AN ISIS EPITAXIAL WAFER

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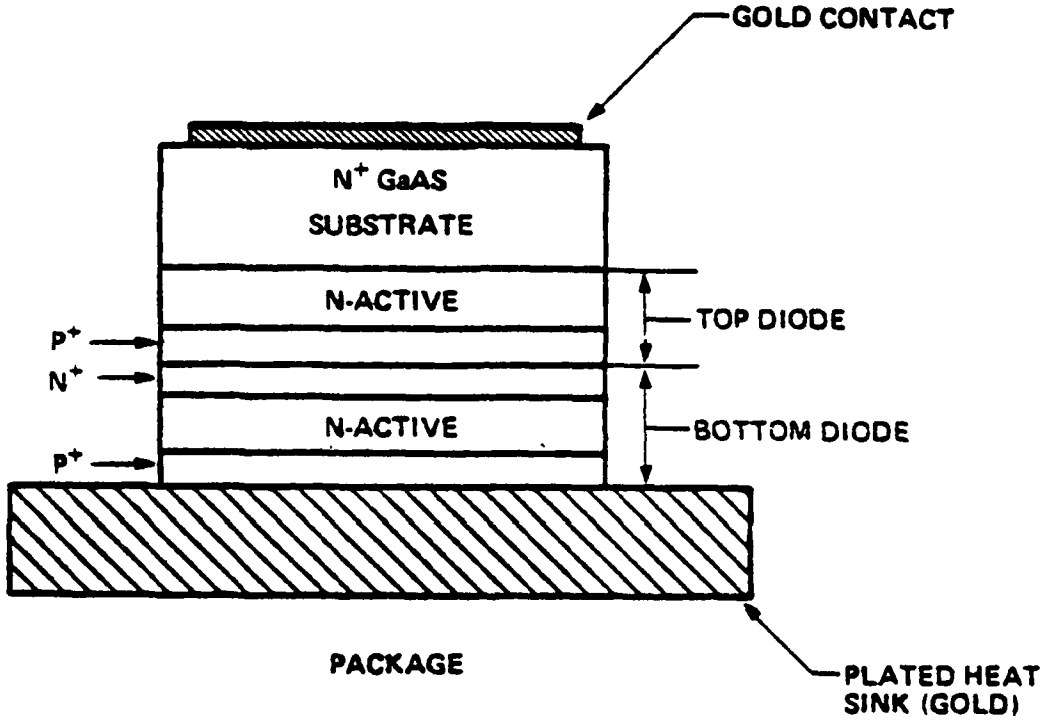

FIGURE 2.2 PLATED HEAT SINK ISIS DIODE MOUNTED EPI DOWN IN PACKAGE.

two diodes, the doping profile of the top diode was adjusted so as to compensate for its higher junction temperature.

The modelling of the top device was simplified after establishing the appropriate doping profile for the bottom diode. The structure shown in Figure 2.3 is one of our X-band single-drift IMPATT designs that is capable of generating 15 watts of peak output power with a DC to RF conversion efficiency of 18 percent. This design was selected to represent the bottom diode, operating at a junction temperature of 200°C. By incorporating the information of Figure 2.3 into a design routine program, the doping profile of the top diode was generated after using a junction temperature of 235°C as an input parameter. The resulting structure of the top diode, as simulated by the computer program, is shown in Figure 2.4.

When the ISIS diode is reverse biased during operation, the sandwiched P^{++} N^{++} junction (see Figure 2.2) becomes forward biased. Because of this bias configuration, electrons from the N^{++} layer are injected into the P^{++} contact of the top diode. Similarly, holes from the P^{++} contact of the top diode are injected into the N^{++} buffer of the bottom diode. If the N^{++} and P^{++} layers are very thin and low doped, these injected carriers will diffuse and enter the active region of the two single-drift structures composing the ISIS diode.

The phenomenon described above will degrade the efficiency of the ISIS diode. This can be explained. Electrons injected into the P^{++} layer (from the N^{++} buffer) will diffuse out at the critical moment to flood the avalanche region (of the top diode) which should be depleted of carriers. The out-diffusion of electrons provides an enormous saturation current which reduces the phase delay associated with the avalanche process in the top diode. As a result, the efficiency of the device is reduced.

To suppress the level of injected minority carriers, it is necessary to increase the thickness and carrier density of the N^{++} and P^{++} layers. Calculations have shown that with a 4μm thick P^{++} layer,

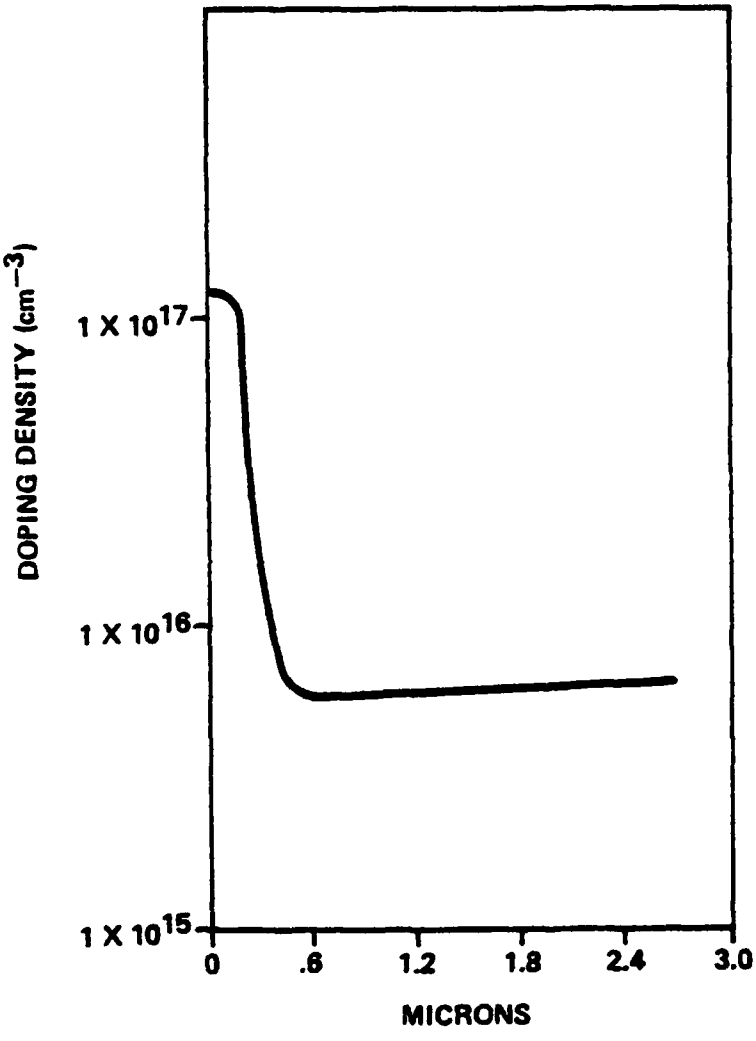

FIGURE 2.3 HI-LO DOPING PROFILE FOR BOTTOM DIODES OF ISIS. JUNCTION TEMPERATURE = 200°C.

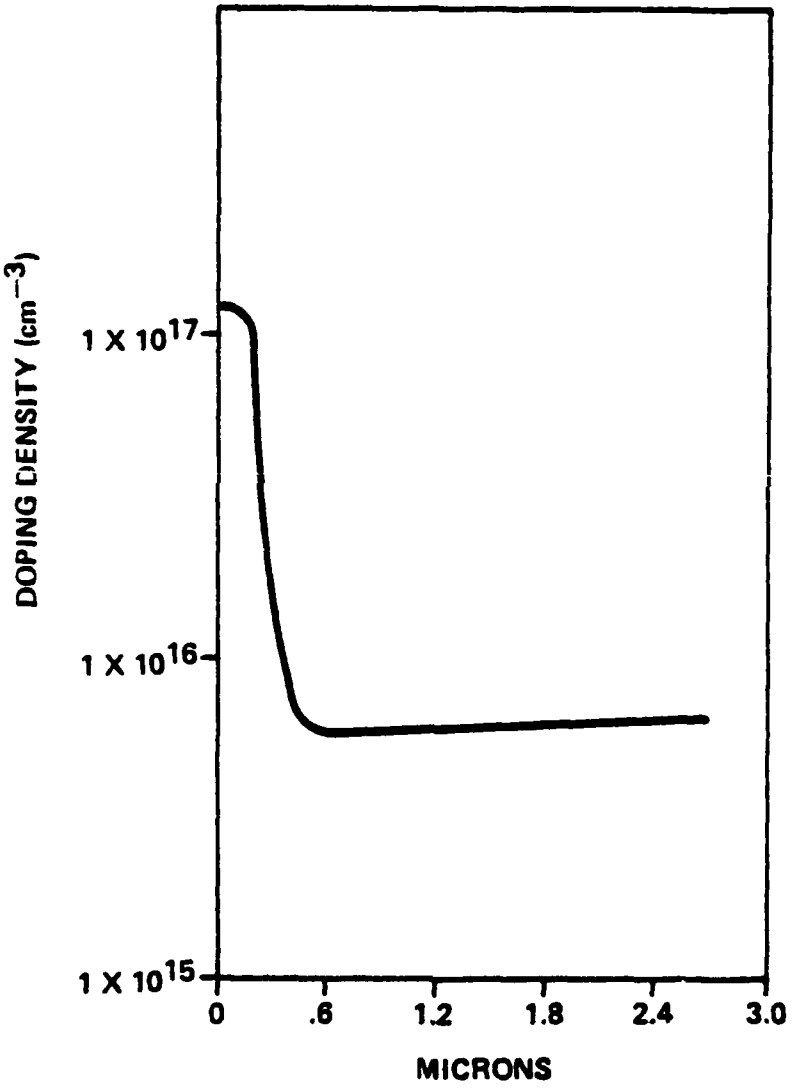

FIGURE 2.4 HI-LO DOPING PROFILE FOR TOP DIODE OF ISIS. JUNCTION TEMPERATURE = 235°C.

TABLE 2.1: RF RESULTS OF X-BAND STACKED CHIPS (PW=1μs, DUTY CYCLE=10%).

Diode#	V_B(TOP)/V_B(BOTTOM) [VOLTS]	C_o [pF]	V_{op} [VOLTS]	I_{op} [AMPS]	PEAK POWER [WATTS]	η [%]
1	32/48	74.1	108	1.5	20.0	12.0
2	38/49	74.0	108	1.1	20.5	17.3
3	38/49	74.8	108	1.1	20.0	16.8
4	35/48	75.1	110	1.8	28.0	14.0
5	32/48	73.0	108	1.4	23.0	15.2
6	48/48	73.0	120	0.66	8.0	10.0

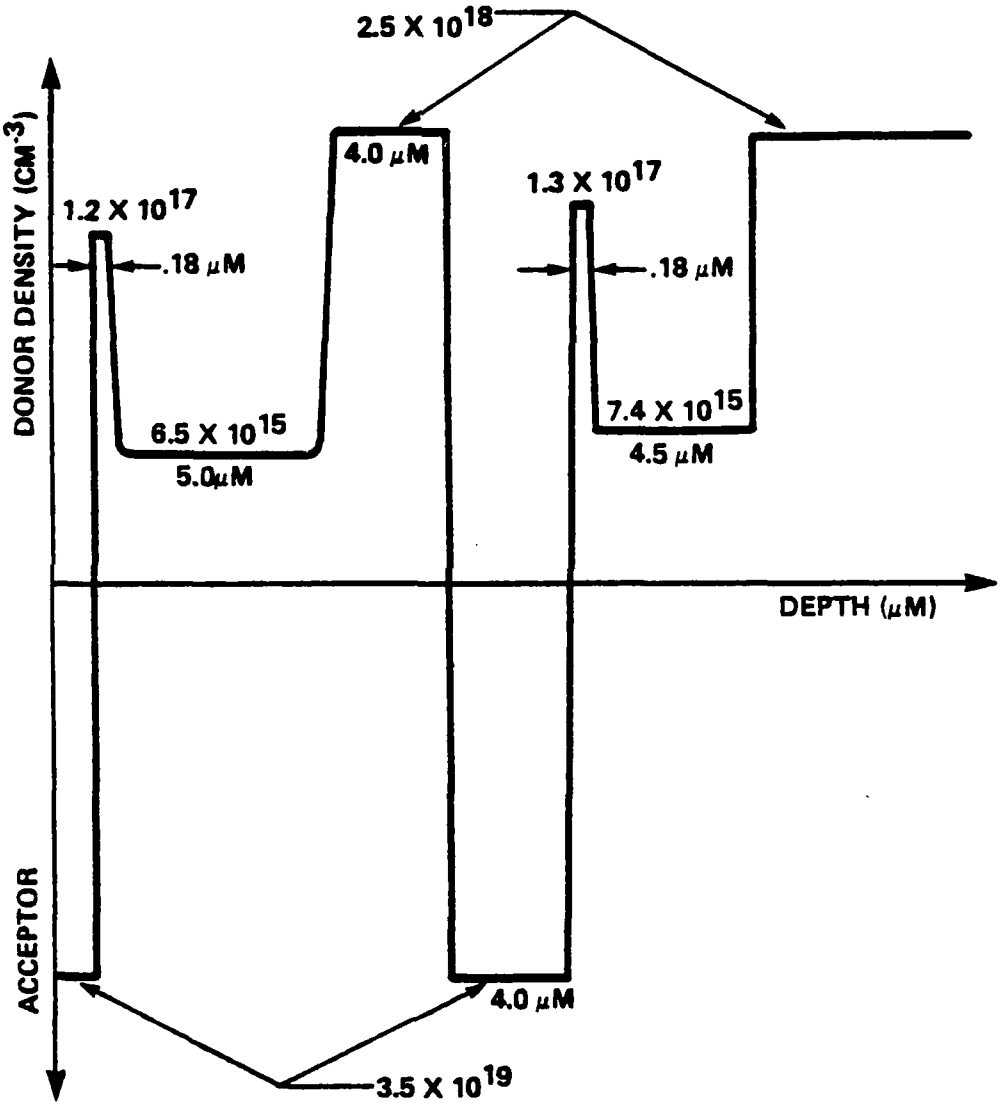

FIGURE 2.5 DESIGN PROFILE FOR X-BAND HI-LO ISIS

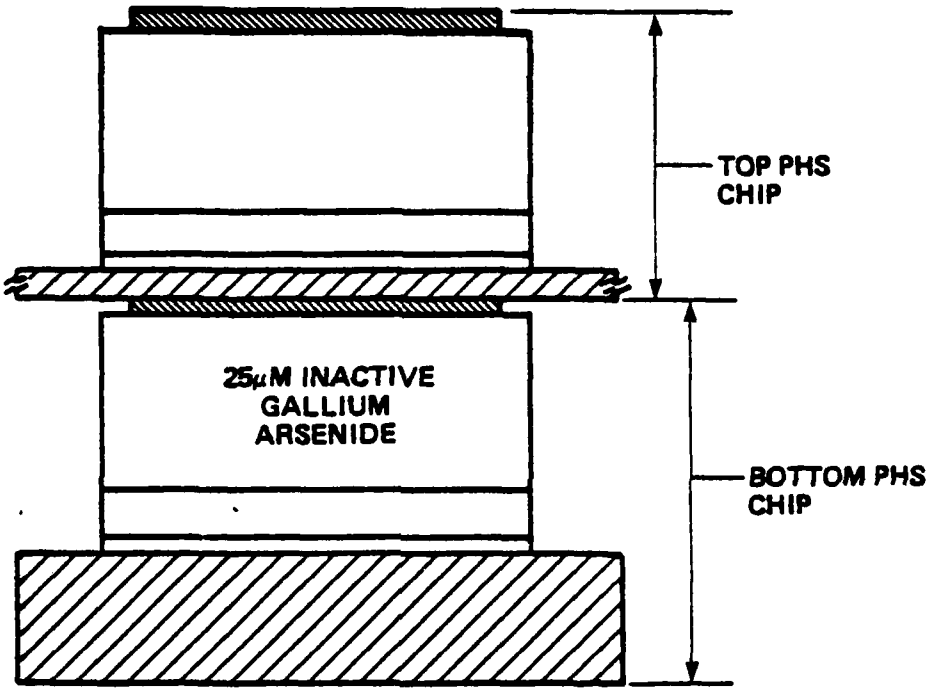

FIGURE 2.6 CONFIGURATION OF PHYSICALLY STACKED CHIPS

SECTION 3
VAPOR PHASE EPITAXY

3.0 INTRODUCTION

This section describes the growth of X-band gallium arsenide Integrated Series IMPATT Structures (ISIS) using the $AsCl_3$-GaAs-H_2 horizontal system. The systems and techniques used for ISIS growth are outlined below. Also, the techniques used to characterize X-band ISIS wafers are discussed.

3.1 $AsCl_3$-GaAs-H_2 SYSTEM (GENERAL)

In the open tube $AsCl_3$-GaAs-H_2 chemical vapor transport system, hydrogen is bubbled through $AsCl_3$ which is maintained at a constant temperature. As hydrogen and $AsCl_3$ vapor enter the upstream side of the reactor tube, the following reaction occurs:

$$AsCl_3+3/2H_2 \rightleftharpoons 1/4\ As_4+3HCl \qquad (3.1)$$

The created HCl gas reacts with an undoped GaAs source that is maintained at approximately 800°C. Here,

$$GaAs+HCl \rightleftharpoons GaCl+1/4\ As_4 \qquad (3.2)$$

The above reaction is driven from left to right causing the decomposition of GaAs at 800°C. A seed, or GaAs wafer, is positioned downstream of the source and is maintained at 700°C. At the seed location, reaction (3.2) is driven in the opposite direction, causing the deposition of GaAs on a wafer that is positioned on a carriage. In summary, this VPE process involves the transport of GaAs from a source, where it is formed, to a GaAs wafer, on which it is deposited in a vapor form.

3.2 VPE SYSTEM

The main features of the VPE system used for this program to grow X-Band ISIS epitaxial material are as follows:

(i) A 4" diameter reactor tube positioned in a 6-zone furnace.

(ii) A multi-channel (tier) seed carriage.

(iii) Separate N and P dopant networks.

(iv) Two $AsCl_3$ bubblers maintained at a constant temperature by means of circulator baths.

(v) An HP 1000 computer system for automatic control.

(vi) An electronic console to interface the HP 1000 with the VPE system. Features include automatic/manual control of all growth parameters.

(vii) A Pd-diffused hydrogen purifier to supply the VPE system with high purity hydrogen.

Some of the above features are pictured in Figure 3.1. A schematic of the reactor tube is shown in Figure 3.2. The tube consists of three inlets. The 1st inlet is connected to the $AsCl_3$ growth bubbler and is used to transport hydrogen and $AsCl_3$ vapor necessary for the source reaction. The 2nd inlet is connected to the N-dopant network and allows a flow of silane (SiH_4) to enter the reactor when growing N-type layers. For in-situ etching prior to epitaxial growth, the 2nd inlet is also used to transport $AsCl_3$ from the etch bubbler. The 3rd inlet is located further downstream of the 2nd inlet and is used as a conduit for dimethylzinc (DMZ) when growing P^{++} contact layers.

The furnace that accommodates the 4" diameter tube consists of six

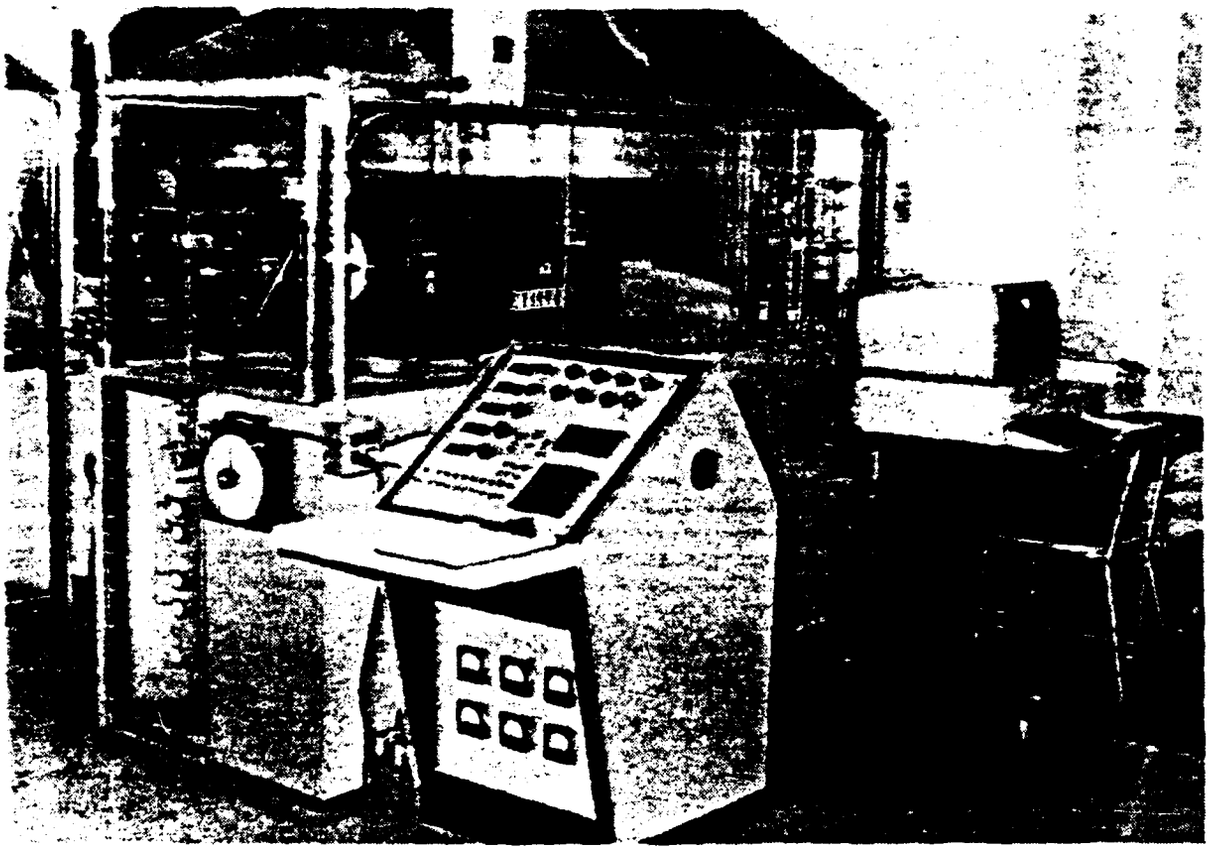

FIGURE 3.1 LARGE BORE (4" DIA.) COMPUTER CONTROLLED DOUBLE-DRIFT IMPATT REACTOR.

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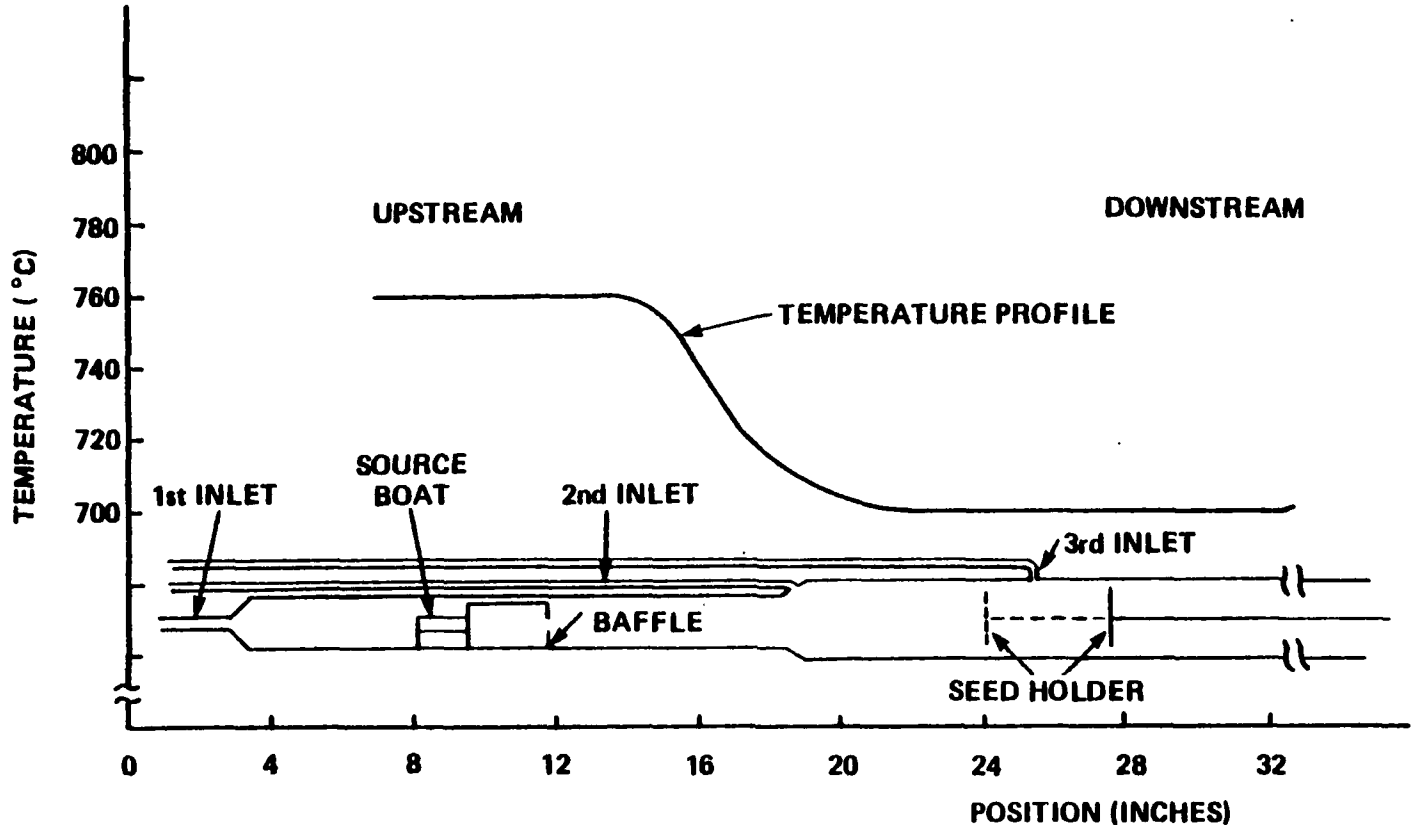

FIGURE 3.2 SCHEMATIC OF 4" DIAMETER REACTOR TUBE POSITIONED WITH RESPECT TO TEMPERATURE PROFILE.

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zones with each zone independently controlled by a temperature controller and SCR power supply. Twenty-three thermocouples are positioned along the length of the furnace with six of them being control thermocouples. The others are used for measuring temperature along the furnace. With a total heated length of 36 inches, the furnace was profiled to yield a 6" constant temperature source zone (760°C) and a 12" flat deposition zone (700°C).

The location of the source boat within the reactor tube is shown in Figure 3.2. Adjacent to the source boat is a quartz baffle which allows for thorough mixing of the components resulting from the source reaction. During the growth of N-type layers, the seed carriage is positioned between the 2nd and 3rd inlets. Subsequently, the carriage is moved into a region downstream of the 3rd inlet in preparation for the growth of the P^{++} contact layer.

A schematic of the plumbing arrangement is shown in Figure 3.3. This arrangement consists of mass flow controllers, normally opened and closed valves, and $AsCl_3$ bubblers. The upper section of the flow diagram in Figure 3.4 that includes MFC 1,2, and 3 is a representation of the P-dopant network. A separate N-dopant network is also represented and includes MFC 4,5, and 6. The N and P dopant networks are assembled separately so as to avoid the cross contamination of impurities when growing P-N junctions.

The N-dopant network is configured so as to allow for the growth of N-type layers with a wide range of carrier concentration. For example, when growing highly doped ($>2X10^{18}/cm^3$) N-type layers, such as buffer layers, a high concentration of silane (80ppm in H_2) bypasses MFC4 and enters the 2nd inlet of the reactor via MFC6 (see Figure 3.4). For this dilution bypass procedure, the configuration of valves 2 and 3 in Figure 3.4 are reversed instantaneously. For moderately doped (10^{15} - $10^{17}/cm^3$) N-type layers, silane is diluted with hydrogen. In this case, MFC4 controls the amount of the concentrated silane that enters the dilution

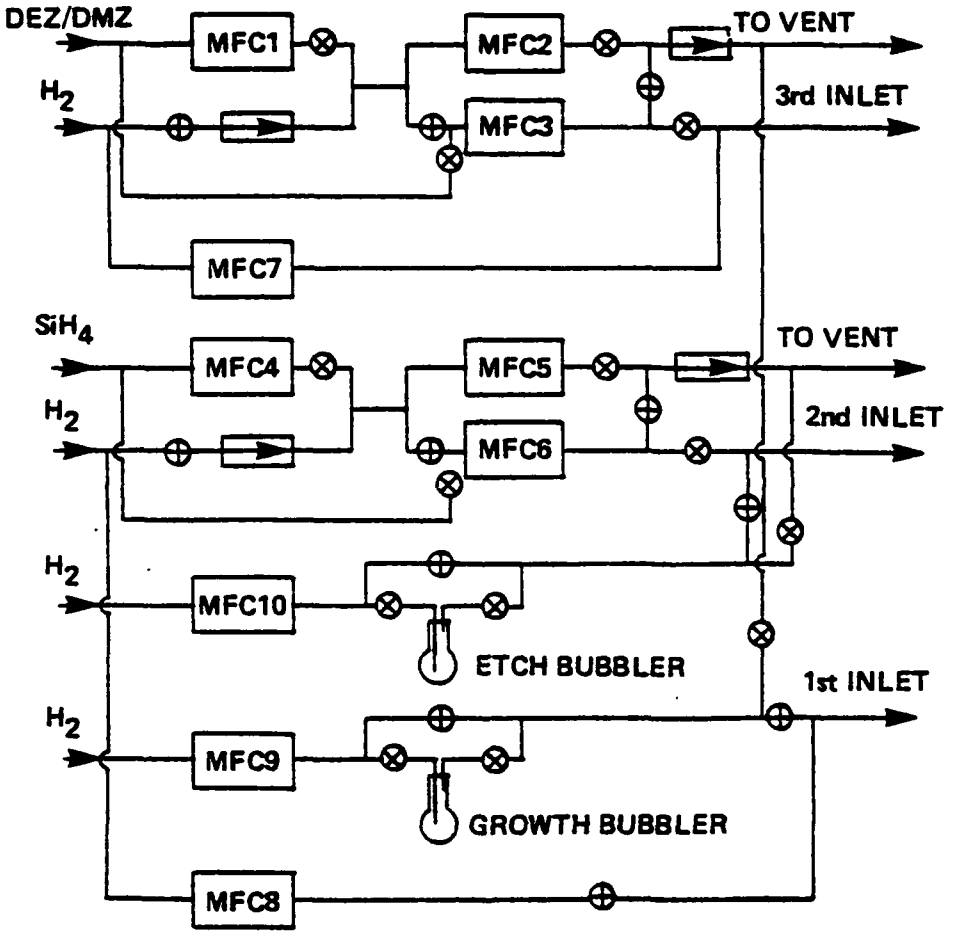

FIGURE 3.3 GAS FLOW CONTROL FOR LARGE BORE DOUBLE-DRIFT REACTOR.

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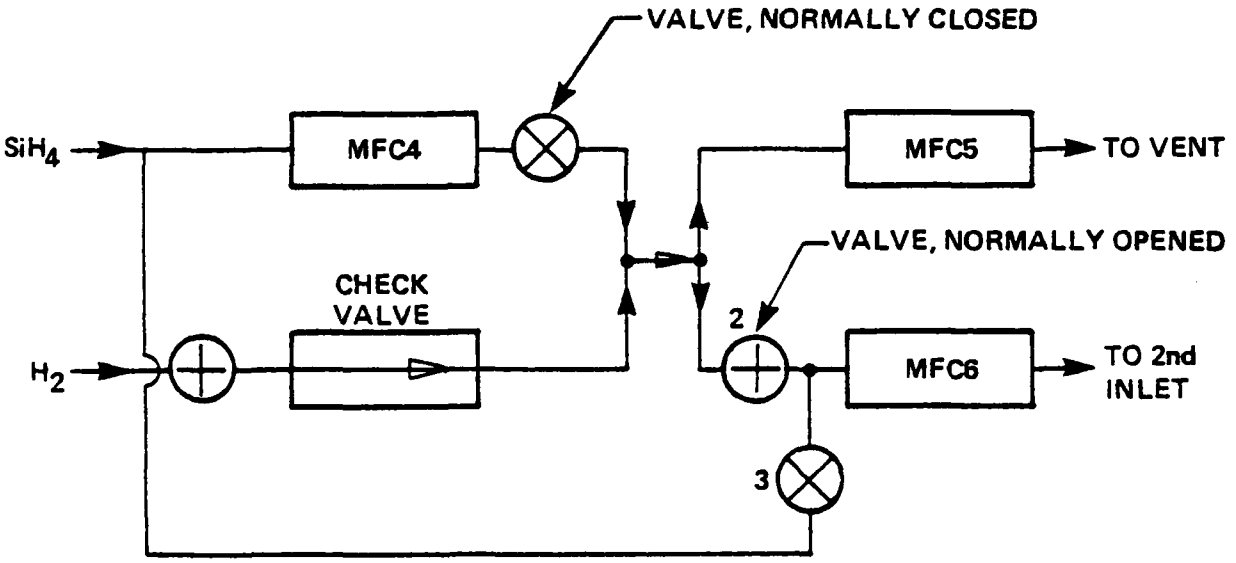

FIGURE 3.4 GAS FLOW CONTROL FOR DOPANT DILUTION SYSTEM.

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The important advantage of the computer controlled epitaxial system is that it ensures reproducibility of growth runs. Furthermore, sharp doping transitions are achieved since mass flow controllers are instantaneously reset in synchronization with valve switching during phase transition.

3.4 EPITAXIAL GROWTH PROCEDURE

Substrates used for this program to produce X-Band Integrated Series IMPATT Structures were Si doped N^{++} GaAs, grown by the horizontal Bridgman technique. They were oriented 2° off the (100) towards the (110) plane with a resistivity of <0.002 ohm-cm. The measured etch pit density on these D-shaped substrates was approximately 5000/cm^2. The substrates were lapped and chemically polished to a final thickness of 17 mils.

Prior to epitaxial growth, the substrates were etched in 5:1:1 (H_2SO_4:H_2O:H_2O_2), rinsed in DI water, and cleaned in acetone and alcohol. Once cleaned, the substrate was loaded into the multi-tier seed carriage and the latter was positioned in the appropriate growth zone.

Before attempting to grow the entire X-band ISIS (P^{++}-N^{+}-N-N^{++}-P^{++}-N^{+}-N--N^{++}) in a single growth run, it was necessary to develop growth techniques through several stages, simulating growth parameters for each section of the structure. The evolutionary stages were as follows:

(a) The growth of a N^{++} buffer with a carrier concentration of $2.5X10^{18}/cm^3$.

(b) The sequential growth of a N^{++} buffer/N-active structure.

(c) The sequential growth of a N^{++} buffer/N-active/N^{+} avalanche structure.

(d) The growth of a P^{++} contact layer with a carrier concentration $1X10^{19}/cm^3$.

(e) The sequential growth of an N^{++}-N-$N^{+}P^{++}$ structure.

The predictable growth of HI-LO (N^{+}-N) doping profiles require an

understanding of the relationship between injected silane concentration (ppm) and the resulting epilayer carrier concentration (cm^{-3}). This relationship was determined by performing an N-type calibration growth run. For such a growth run, several layers were deposited sequentially on an N^{++} substrate. During the growth of each layer a controlled amount of silane was injected into the reactor.

The multi-layer structure resulting from the N-type calibration growth run was characterized by the conventional differential capacitance-voltage method using a mercury probe. Access to each of the N-layers was made possible by using a 3:1:1 (H_2SO_4:H_2O:H_2O_2) etch. Since the injected concentration of SiH_4 was computed for each of the layers, it was possible to empirically determine the dependence of SiH_4 concentration (ppm) on the doping density of the epilayer. As shown in Figure 3.5, it was possible to grow N-type layers with donor densities ranging from $2X10^{15}/cm^3$ to $2.5X10^{18}/cm^3$.

Using dimethylzinc (DMZ) as the P-type dopant source, epitaxial layers were grown on semi-insulating GaAs substrates. The electrical properties of the P-type layers were evaluated by Hall Van der Pauw measurements. Based on the results from these measurements, we were able to grow P^{++} contact layers having a carrier concentration of $1X10^{19}/cm^3$ with a room temperature mobility of $78cm^2/V\text{-sec}$. These results were achieved by injecting approximately 200 ppm of DMZ while growing the P^{++} material.

3.5 GROWTH OF X-BAND HI-LO ISIS

The HI-LO ISIS profile of Figure 2.5 consists of eight distinct layers, namely, N^{++} buffer, LO-N, HI-N, P^{++} contact, N^{++} buffer, LO-N, HI-N, and P^{++} contact. The growth of these layers was done sequentially in the order listed above. The preprogrammed steps used for the sequential growth of the eight layers are listed in Table 3.1. In order to realize sharp doping transitions, additional steps were incorporated in the automatic growth schedule.

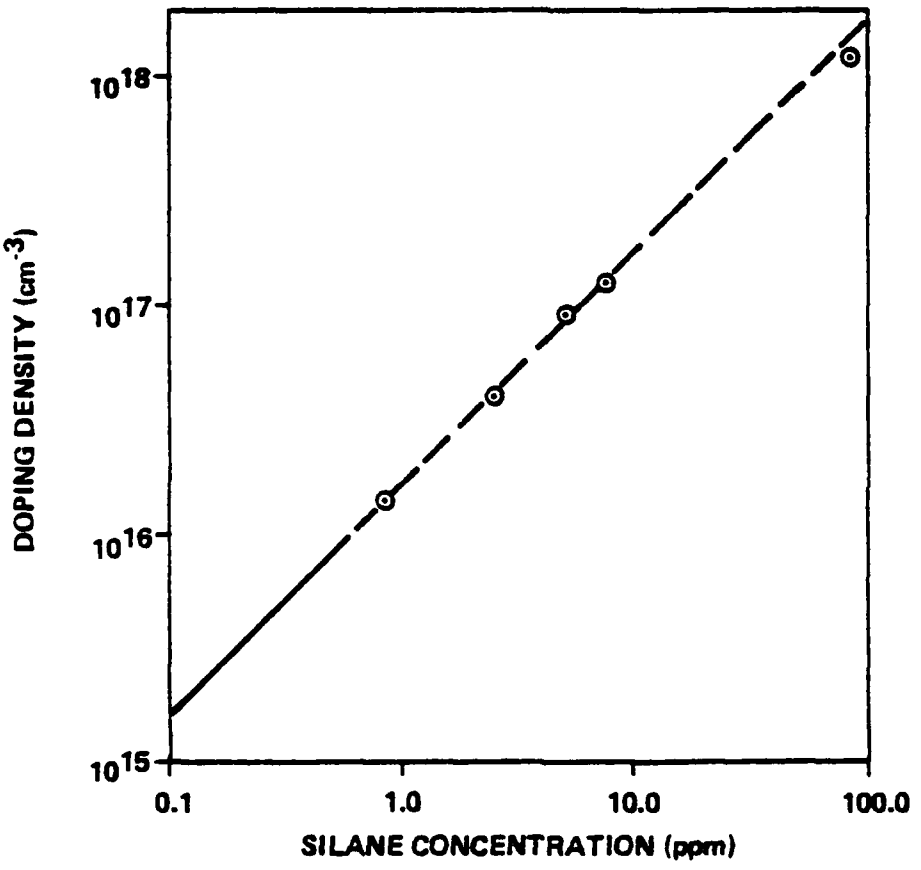

FIGURE 3.5 DONOR DENSITY (cm^{-3}) VERSUS INJECTED SILANE CONCENTRATION (ppm).

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Some of these steps included in-situ etch back, purge, and dope-up. The purpose of the first two steps was basically to remove residual dopant gases, while the third was used to condition the reactor tube at the doping level required by the subsequent layer.

Subsequent to the separate N and P type simulated growth runs, attempts were made to integrate their calibrated growth parameters so as to achieve an ISIS epitaxial wafer. After loading a pre-cleaned N^{++} substrate into the VPE reactor, the HP 1000 system was engaged for automatic control of the entire growth procedure, as listed in Table 3.1. Following the initial phase, the $AsCl_3$ etch bubbler was switched on so as to vapor etch (in-situ etch) the substrate prior to epitaxial growth.

The third sequence involved the growth of a 2-3um thick N^{++} buffer having a carrier concentration of $2\text{-}3X10^{18}/cm^3$. This high doping density was achieved by directing concentrated silane (80 ppm) into the reactor via the bypass dilution network (see Figure 3.5). During the growth of the N^{++} buffer layer, the dilution network was activated, with MFC4, and 5 set at the values required for the subsequent growth of the LO-N active layer.

At the appropriate time for the LO-N layer growth, the established flow in the dilution network was exchanged with that used for the N^{++} buffer growth. The advantage of this approach was to minimize the interface width between the N^{++} buffer and the LO-N layer. To further improve the doping transition between these layers, an in-situ etch back of the N^{++} buffer layer was employed.

After growing the first HI-LO portion of the ISIS profile, a large flow of hydrogen was admitted into the tube, thereby purging it of residual silane. Before growing the P^{++} contact layer, DMZ was allowed into the tube so as to condition the region downstream of the 3rd inlet. At the termination of the P-dope-up phase, the seed carriage was pulled into the doped region and the growth bubbler switched on. The growth of the P^{++} contact layer was followed by a hydrogen purge phase to continue the second half of the ISIS

profile. The seed carriage was pushed into the N-growth region and the above steps were repeated. Finally, the system was purged and the wafer unloaded for characterization.

Chronologically, a simplified flat profile ISIS was initially chosen (prior to growing the design HI-LO ISIS profile) so as to develop and establish the growth techniques described above. A flat profile ISIS was chosen due to the simplicity associated with its characterization. The results achieved from these test runs revealed that a major portion of the first grown layer was compensated. At first, the idea of a compensated layer was not obvious, as C-V step etching techniques were used to evaluate the epi layers. While this characterization technique was able to reveal the entire doping profile of the second grown active layer, it only uncovered a fraction of the first grown active.

The extent of compensation was readily determined after viewing a cleaved cross-section of the ISIS epitaxial material with the aid of a scanning electron microscope (see Figure 3.6). The compensation of the active layer was thought to be caused by zinc diffusion from the sandwiched P^{++} layer. The degree of zinc diffusion was found to be dependent on the concentration of dimethylzinc injected into the reactor tube during the growth of the P^{++} layer. A reduction of this concentration minimized the degree of compensation, but at the expense of the P^{++} acceptor density.

In order to remedy the problem of zinc diffusion and maintain a very high acceptor density in the P^{++} layer (as required by the ISIS design), other growth techniques were explored. A successful approach which was implemented involved a hydrogen purge phase after growing the highly doped P-type layer. The results achieved after using this technique showed no signs of zinc diffusion (see Figure 3.7). With a purge phase prior to growing the N^{++} buffer layer, it is speculated that zinc atoms which are absorbed onto surfaces out-diffuse into the gas stream rather than diffuse into the GaAs crystal. For earlier growth runs where compensation was observed, the N^{++} buffer was deposited immediately after growing the P^{++}

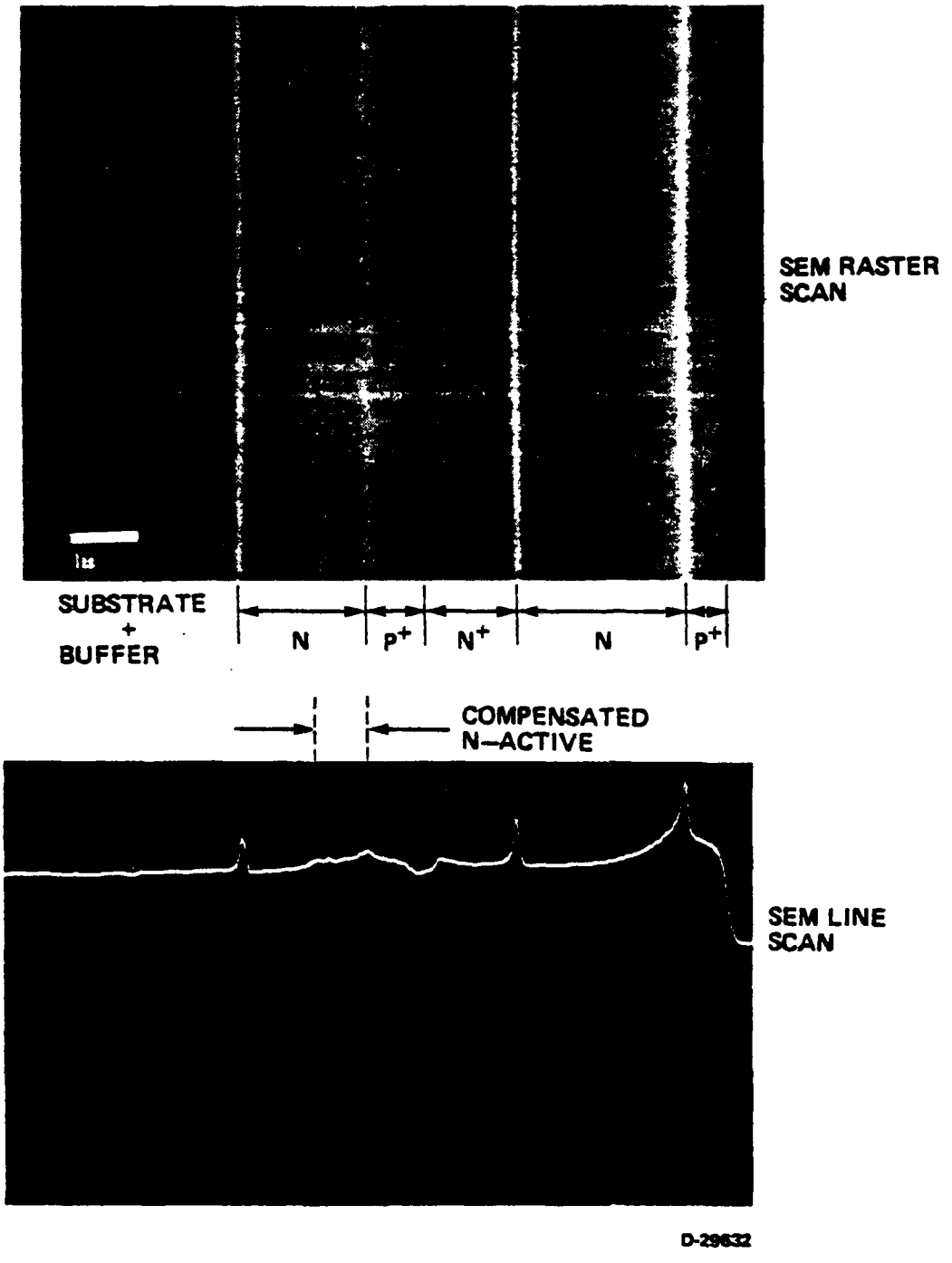


FIGURE 3.6 CLEAVED CROSS-SECTION OF ISIS SHOWING COMPENSATED REGION OF FIRST GROWN N–ACTIVE LAYER.

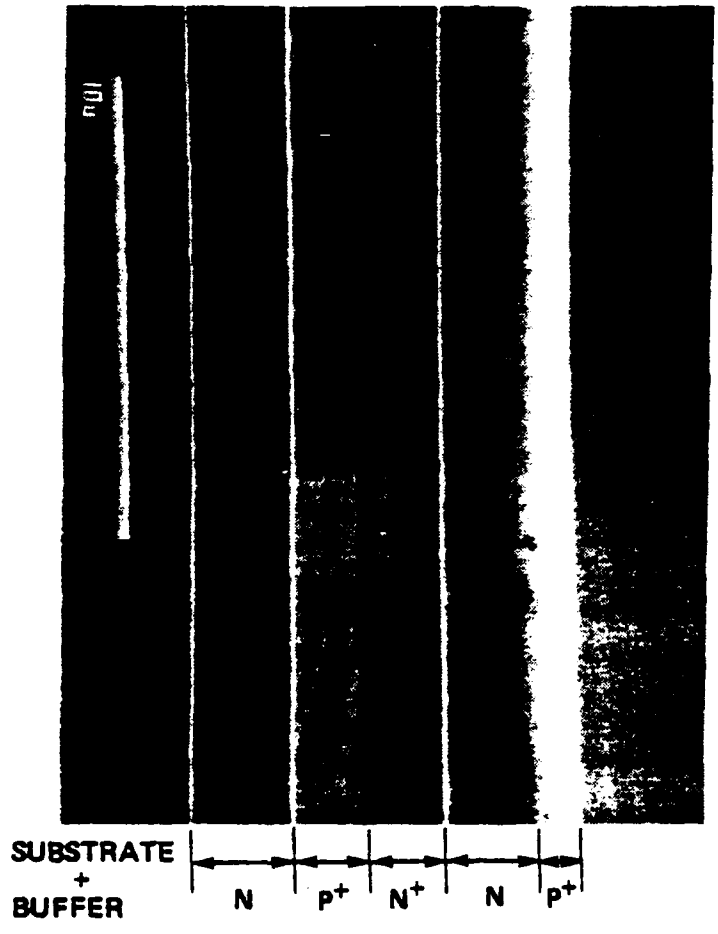


FIGURE 3.7 CLEAVED CROSS-SECTION OF ISIS. NO COMPENSATION OF FIRST GROWN N–ACTIVE LAYER.

layer. The former layer was apparently acting as a "cap" to contain the zinc atoms and further promote its diffusion.

After solving the zinc diffusion problem as described above, VPE growth runs were made to produce the design structure shown in Figure 2.5. The characterization techniques used to evaluate the HI-LO ISIS doping profiles are discussed below.

3.6 CHARACTERIZATION OF ISIS WAFERS

The characterization of epitaxial material is an integral part of the epitaxial growth process. A knowledge of the epitaxial doping profile enables the establishment of a feedback loop which constantly updates the functional characteristics of the growth system. Based on the acquired information, growth parameters and techniques can be tailored to meet the specifications of the subsequent doping profile. Additionally, epilayer characterization is essential for selecting material to be submitted for device fabrication.

The evaluation of a HI-LO ISIS doping profile is not as straight-forward as that of a flat profile ISIS. For the former case, the difficulty is due to a sub-micron (0.18 microns thick) HI-N layer situated adjacent to each of the P^{++} contact layers as shown in Figure 2.5. With the conventional C-V step etching technique (in which atomic layers are chemically removed at the end of each C-V profiling step), it is very difficult to accurately determine the position of the HI-N layer. Nevertheless, the doping level of the HI-N layer can be determined with the conventional technique.

To accurately determine the doping profile of a HI-LO ISIS, we developed a scheme in which mesas were defined to various heights on an evaluation piece cleaved from the epitaxial wafer. Figure 3.8 (a) and 3.8 (b) show the mesa definition used for evaluating the doping profile of the 2nd and 1st grown diodes, respectively. In Figure 3.8 (c), the mesas were defined to a height that was equivalent to the total thickness of the epitaxial layers. With this configuration, the composite characteristic of the two diodes was evaluated.

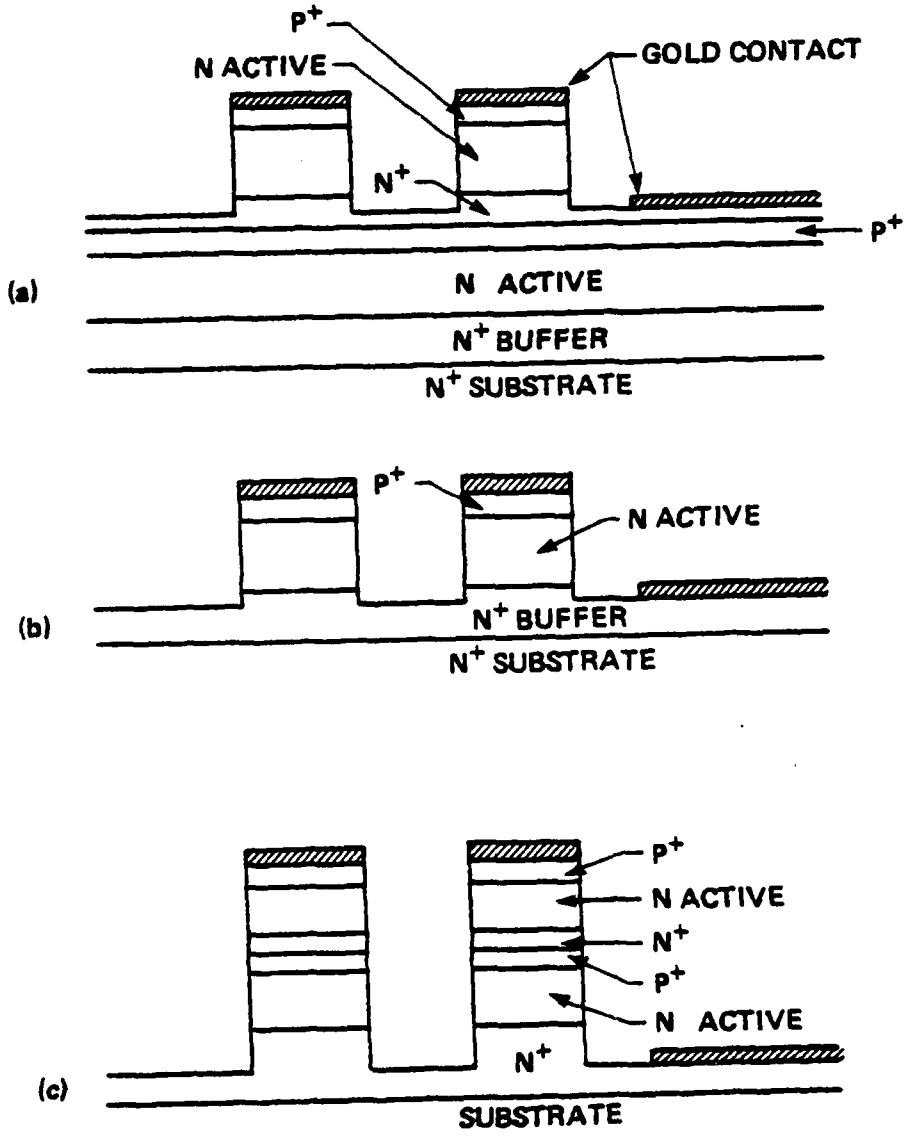


FIGURE 3.8 DEFINITION OF MESAS ON ISIS EVALUATION SAMPLES

D-29461

The structures of Figure 3.8 were accomplished by the standard photoresist procedures. Mesa isolation was provided by removing GaAs material with a 5:1:1 (sulphuric acid: water:Hydrogen peroxide) etch. In order to prepare the sample according to Figure 3.8 (b), the 2nd grown device was chemically removed in the 5:1:1 etch before the mesas were defined. The etch rate of the 5:1:1 solution was determined to be 3.0 microns/minute, at room temperature.

The specification of mesa height for each sample required a knowledge of epilayer thickness. The latter was acquired by staining cleaved cross-sections with the following formulation:

36ml DI:12 ml NH_4OH

50ml DI:1.0g $K_3Fe(CN)_6$

mixed in a 2:1 ratio before use. The thickness of the individual layers was evaluated with the aid of an optical/SEM microscope. With the thickness results and the etch rate of the 5:1:1 solution, it was possible to fabricate the mesa structures of Figure 3.8.

In addition to the evaluation techniques mentioned above, an automatic electrochemical profiler was used to characterize the sandwiched N^{++} buffer layer in the ISIS wafer. With conventional C-V measurements it is not always possible to have an entire depth profile without resorting to the tedious step etching techniques. By using the automatic profiler, which incorporated electrochemical dissolution with simultaneous differential C-V measurements, it was possible to achieve the entire depth profile of the N^{++} buffer layer. To simplify this measurement technique, the last grown P^{++} contact and part of the second grown active layer of a VPE ISIS were chemically removed in a 5:1:1 etch solution. The resulting doping profile is shown in Figure 3.9 and portrays two important features: (a) A highly doped N^{++} buffer layer ($2.5X10^{18}/cm^3$) deposited after growing a highly doped P^{++} contact layer. Such a highly doped sandwiched N^{++} buffer layer is an indication that no (or minimum) memory effect was experienced after growing the highly doped

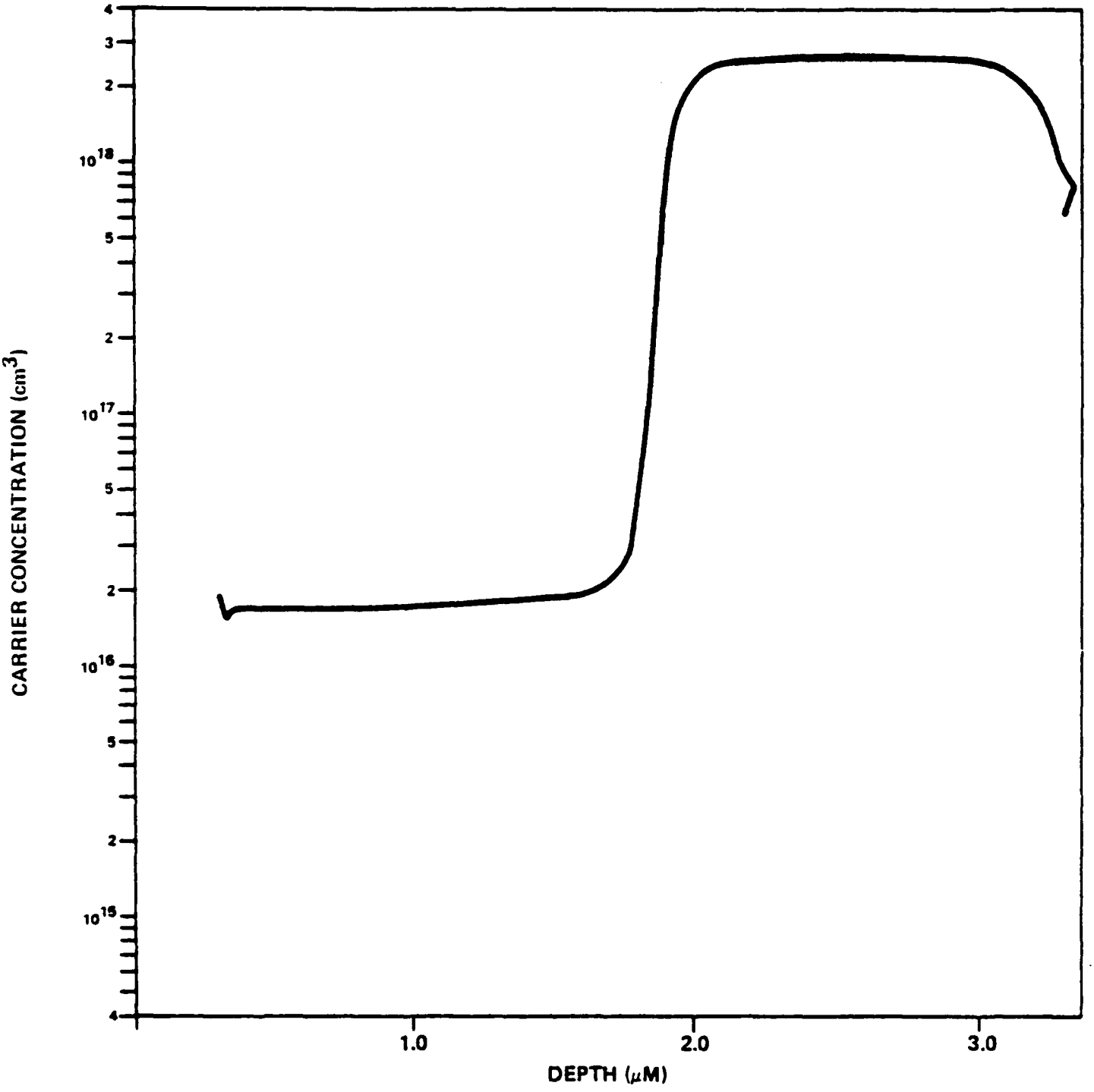


FIGURE 3.9 POLARON (N-W) PLOT OF SECOND GROWN N-ACTIVE/N^{++} BUFFER INTERFACE

P^{++} contact layer. (b) A sharp doping transition between the N^{++} buffer and the active layer. These are some of the features that can be expected from our VPE-halide system.

SECTION 4
DEVICE FABRICATION

4.0 PROCESSING

Subsequent to growth and characterization of VPE ISIS wafers, appropriate epitaxial slices were submitted to the processing laboratory. There, the slices were processed into discrete single mesa plated heat sink (PHS) devices. The steps involved in the processing of the slices are summarized in Table 4.1 and Figure 4.1. Additionally, a description of each step is presented in the following paragraphs.

In order to ascertain the usable surface area and ensure slice traceability, the incoming ISIS slices were visually inspected and photographed for surface defects (such as pits, stains, hazes, hazes, cleaves, etc.) The above information was noted on a traveller which accompanied each slice. Process specifications such as epitaxial metallization, mesa height and diameter were also appended to each traveller.

Following a thorough solvent cleaning procedure, each ISIS slice was mounted into an E-beam evaporator so as to metallize the epitaxial side of the slice. The metallization scheme involved the co-evaporation of 750Å of gold and 100Å of zinc to form an ohmic contact on the P^{++} layer. A two micron thick protective layer of gold was then electroplated over the gold-zinc metallization (see Figure 4.1 (b)). To achieve a reliable ohmic contact, the slice was alloyed at 435°C for 8 minutes in an atmosphere of pure hydrogen.

To minimize the series resistance in the final device, the original 17 mil thick N^{+} GaAs substrate of the ISIS slices was reduced to a final mesa height of 30 microns. The reduction of the substrate thickness was achieved by, first, mechanically lapping it to a thickness of 175 microns (see Figure 4.1 (c)) using a 5.5 micron aluminum grit suspended in oil. While the thickness value at the end of this step was not critical, it is essential to establish a very flat surface (within + 0.1 mil variation).

OPERATION SEQUENCE

INCOMING WAFER INSPECTION
LOT DOCUMENTATION
WAFER PREPARATION (PRE-METALLIZATION CLEANING)
EPITAXIAL LAYER METALLIZATION
METALLIZATION ADHERENCE TEST
PROTECTIVE PLATING
GaAs FLAT LAP
WAFER CLEANING (PRE-PLATING CLEAN)
HEAT SINK PLATING
WAFER CLEANING
SUBSTRATE THIN LAP
WAFER CLEANING (PRE-POLISH CLEAN)
POLISH ETCH 1
PHOTO STEP #1 (STRESS RELIEF GRID)
ETCH #2 (GRID ETCH)
REMOVE RESIST
ETCH #3 (SUBSTRATE TAILOR ETCH)
WAFER CLEAN (PRE-TOP CONTACT CLEANING)
TOP CONTACT METALLIZATION
PHOTO STEP #2
ETCH TOP CONTACT
STRIP RESIST
ETCH #4 (REMOVE EXCESS BACK CONTACT METAL)
PHOTO STEP #3 (MESA MASK)
ETCH STEP #5 (ETCH MESA)
STRIP RESIST
EVALUATION AND TAILOR ELECTRICAL SPECIFICATIONS
MECHANICAL INSPECTION
SEPARATE CHIPS

D-21620

TABLE 4.1 PHS PULSED IMPATT PROCESS FLOW CHART.

FIGURE 4.1 (a). ISIS EPITAXIAL WAFER

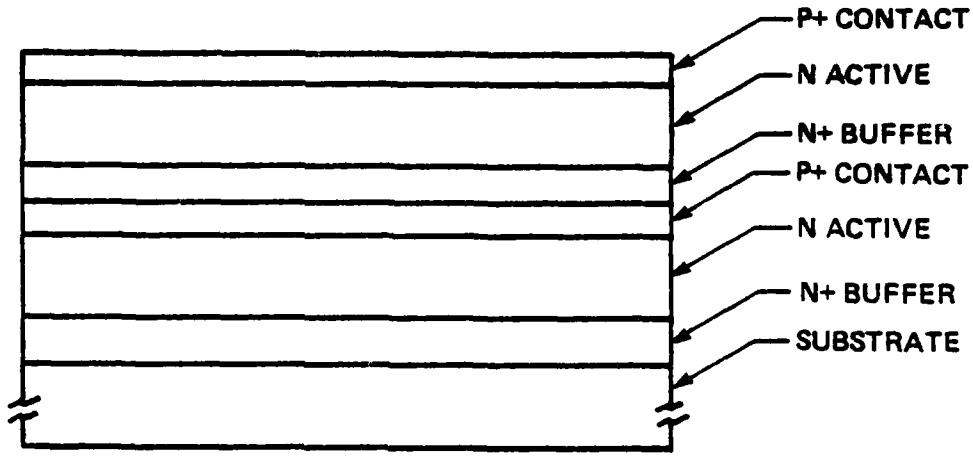


FIGURE 4.1 (b). OHMIC P-TYPE METALLIZATION AND PLATING

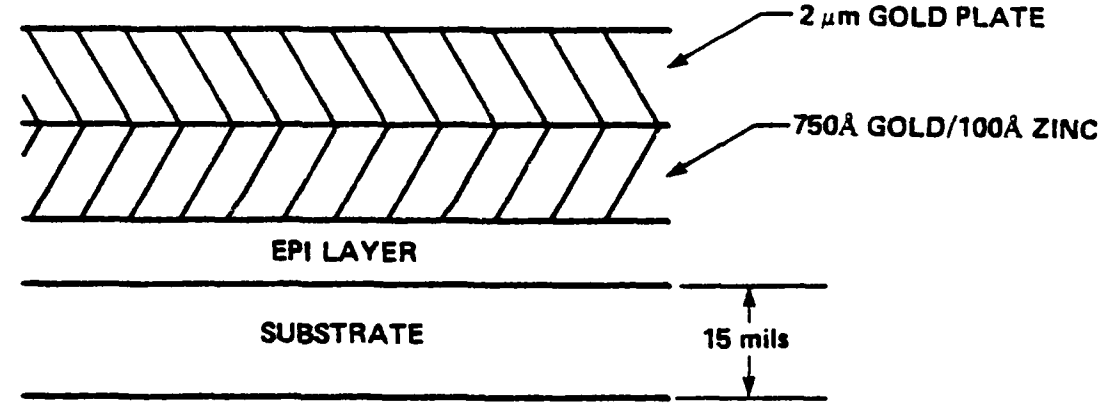


FIGURE 4.1 STEPS IN THE PLATED HEAT SINK PROCESS.

FIGURE 4.1 (c). SUBSTRATE FLAT LAP.

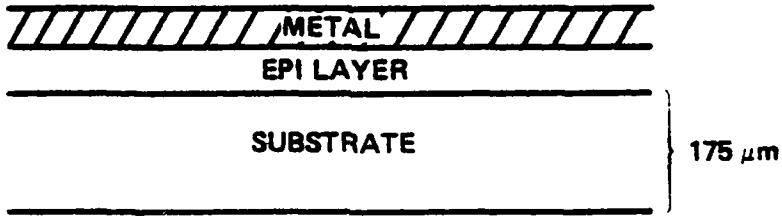


FIGURE 4.1 (d). GOLD HEAT SINK PLATING.

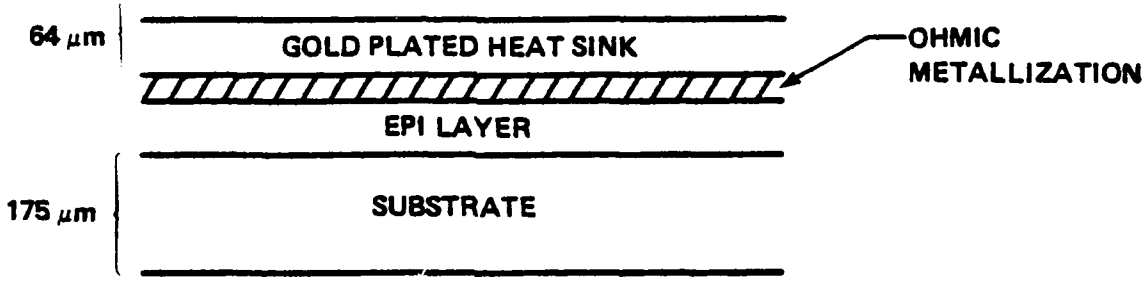


FIGURE 4.1 STEPS IN THE PLATED HEAT SINK PROCESS.

This serves as a reference plane for future lapping operations. The substrate thickness was reduced further during processing as described below.

For reliable operation, the junction temperature of the ISIS diode was kept as low as possible. In order to maintain a safe junction temperature (<250°C) and at the same time achieve the maximum RF output power, it was necessary that the dissipated heat in the diode be removed efficiently. In order to accomplish this, a 64 micron thick layer of gold was electrolytically plated on the epitaxial side of the ISIS slice (see Figure 4.1 (d)) at an average rate of 4.5 microns/hour. To obtain optimum thermal conductivity, conditions were established so as to yield a heat sink with high density and a small grain size. The desired properties were accomplished by initially using a low plating current density and then gradually increasing it to a maximum of $2.5mA/cm^2$.

After plating the heat sink, the edges of the slice were trimmed to remove any build-up of gold that could induce stress into the slice or hinder future lapping operations. Using the flatness from the original GaAs flat lap step as a reference plane, the PHS was also flat lapped (with a 9.5 micron aluminum grit suspended in oil) in order to maintain parallelism (within 0.0001") between the two surfaces (see Figure 4.1(e)). It should be noted that errors relating to parallelism will result in non-uniformity in the GaAs mesa height. Thus, the PHS acts as a reference plane for subsequent thinning operation.

Thin lapping was accomplished by mounting the PHS side of the ISIS slice onto a stainless steel block. With a 5.5 micron aluminum grit the GaAs substrate was reduced to a thickness of approximately 1.0 mil greater than the desired mesa height. The extra 1.0 mil of GaAs material was chemically polished in an agitated solution of 3:1:1 (H_2SO_4:H_2O:H_2O_2) in order to remove any embedded lapping compound and to prepare the surface of the slice for the back contact metallization (see Figure 4.1 (f)).

FIGURE 4.1 (e). GOLD LAP

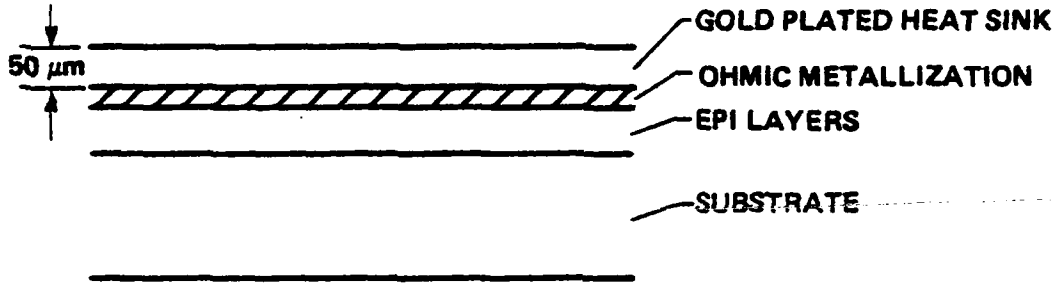


FIGURE 4.1 (f). GaAs SUBSTRATE LAP AND POLISH ETCH.

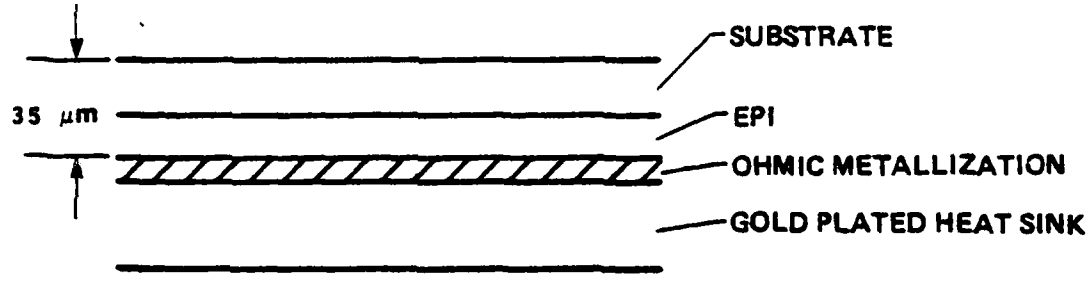


FIGURE 4.1 STEPS IN THE PLATED HEAT SINK PROCESS.

In order to relieve any stress due to the flexing of the gold PHS, a matrix of 0.002" lines on 0.030" centers were exposed on the polished GaAs using standard photoresist procedures. The exposed pattern was then etched through the GaAs material to the gold-zinc metallization of the P^{++} epitaxial layer as shown in Figure 4.1 (g).

After a thorough solvent cleaning procedure, the ISIS slice was placed into an E-beam evaporator in preparation for an N-type ohmic contact metallization. 1000Å of gold and 300Å of germanium were simultaneously evaporated so as to achieve an 88% gold/12% germanium mixture by weight. Subsequently, 200Å of nickel and 2000Å of gold were respectively deposited on the gold-germanium layer as shown in Figure 4.1 (h).

To ensure an adequate bonding surface for the top electrical ribbon connection, it was necessary to electroplate a layer of soft gold onto the back contact metallization. In order to perform this procedure, it was necessary to sputter a 3000Å layer of gold (see Figure 4.1 (i)). Sputtering, rather than E-beam evaporation, produced a sidewall coverage of the mesas which aided in the plating process via electrical continuity across the slice. After plating a 5 micron layer of protective gold, the sample was alloyed at 400°C for 8 minutes so as to form a reliable ohmic contact to the N^+ substrate. After alloying the N^+ contact metallization, the slice was electroplated with a 2 micron layer of soft gold for ribbon bonding.

Back contact definition was accomplished by exposing and developing an array of circular photoresist pattern on the center of the square GaAs grids (see Figure 4.1 (j)). With the resist acting as a mask, excess gold was removed using a C-35 gold etch solution as shown in Figure 4.1 (k). Before removing the excess photoresist, the mesas were tailor etched to give the desired zero bias capacitance (Figure 4.1 (l)). Metal overhang was reduced using standard photolithographic techniques (see Figure 4.1 (m) and (n)).

The slice was cleaned and probed for reverse voltage breakdown and zero bias capacitance values. This information as well as the number and size

FIGURE 4.1 (g). STRESS-RELIEF GRID ETCH

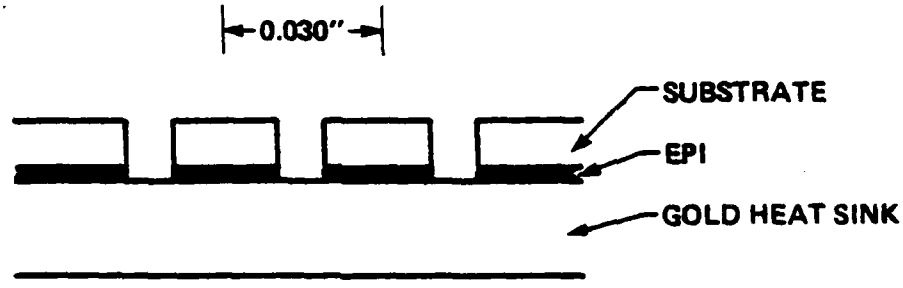


FIGURE 4.1 (h). Au/Ge/Ni/Au METALLIZATION

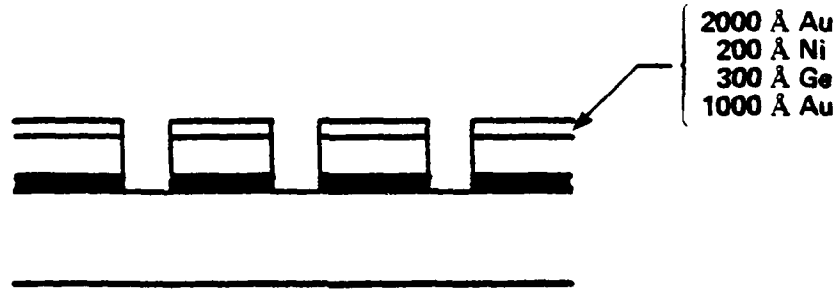


FIGURE 4.1 STEPS IN THE PLATED HEAT SINK PROCESS.

FIGURE 4.1 (i). SPUTTER/PLATE GOLD

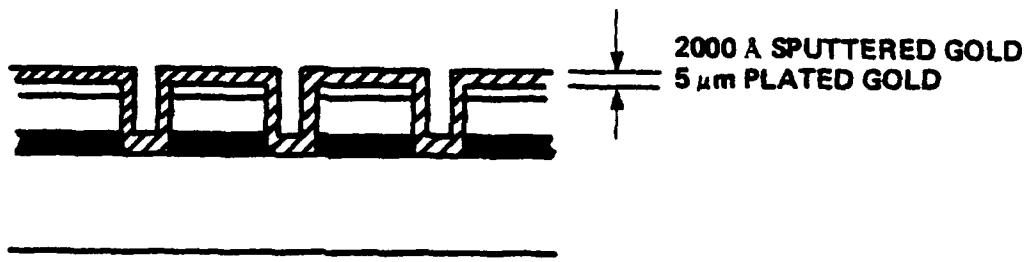


FIGURE 4.1 (j). CONTACT PHOTO

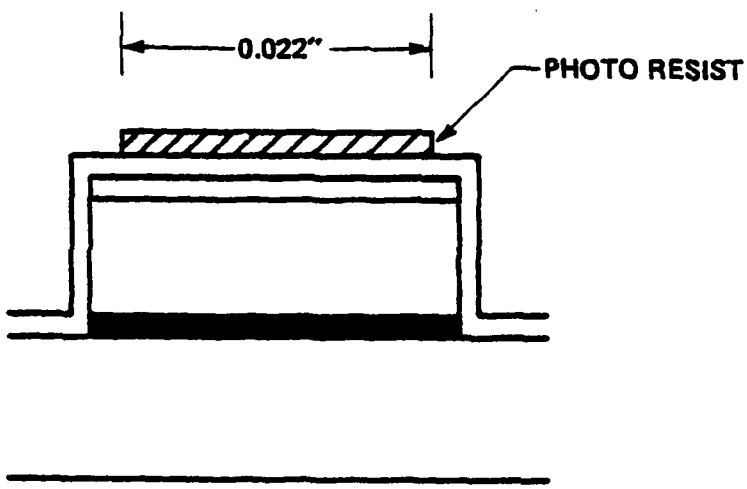


FIGURE 4.1 STEPS IN THE PLATED HEAT SINK PROCESS.

FIGURE 4.1 (k). GOLD ETCH

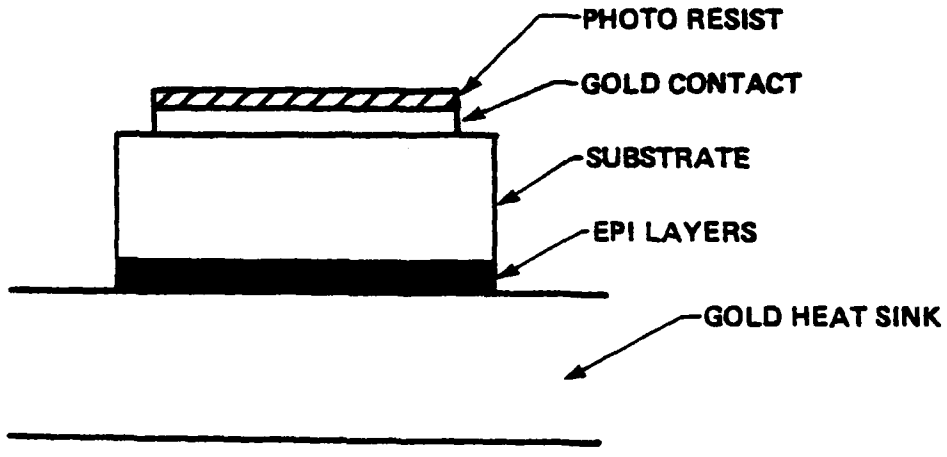


FIGURE 4.1 (l). MESA ETCH

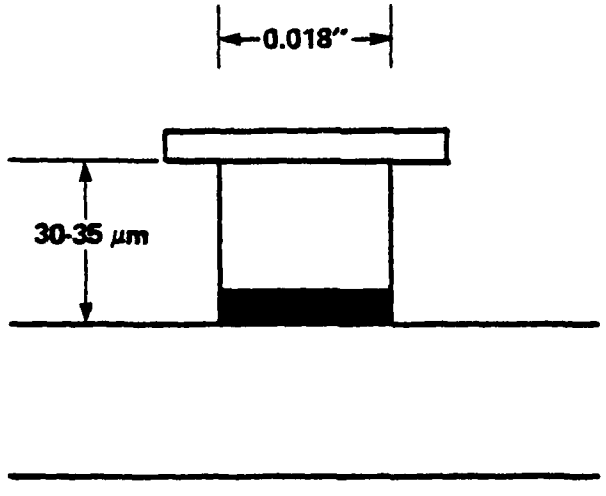


FIGURE 4.1 STEPS IN THE PLATED HEAT SINK PROCESS.

FIGURE 4.1 (m). CUTBACK PHOTO

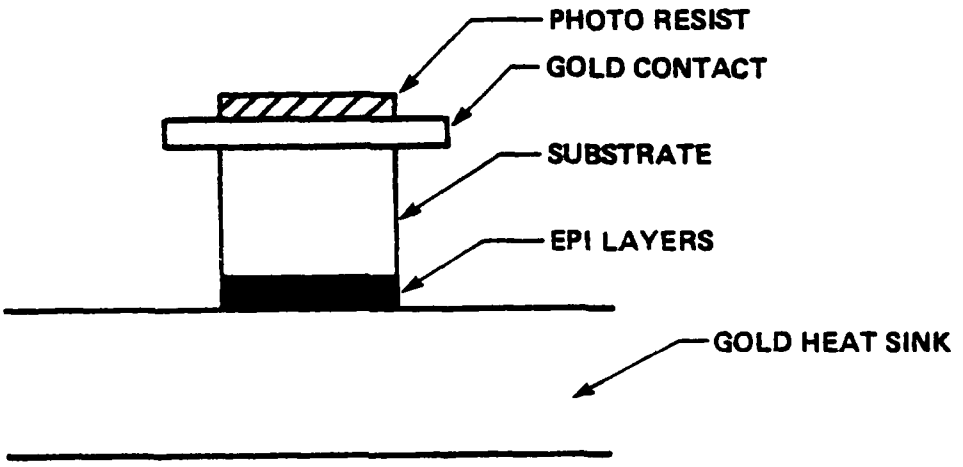


FIGURE 4.1 (n). ETCH GOLD OVERHANG

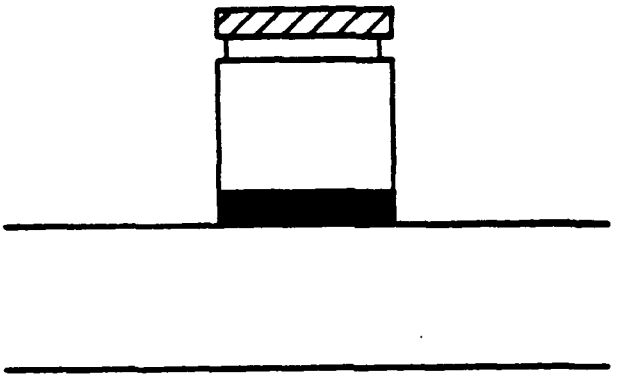


FIGURE 4.1 STEPS IN THE PLATED HEAT SINK PROCESS.

of the diodes was added to the traveller which was kept for future reference. The ISIS slice was then delivered to the assembly laboratory, ready to be diced, packaged, and tested. An example of a typcial ISIS chip, as delivered to the assembly laboratory, is shown in the SEM photomicrograph of Figure 4.2.

4.1 Diode Assembly

4.1.1 Introduction

Two major problems in bonding plated heat sink IMPATT chips are: (i) maintaining enough pressure on the chip during heating in order to insure the thinnest possible solder layer, and (ii) creating an atmosphere which is conducive to optimum solder wetting without the use of flux. By resolving these problems, it is possible to secure a reliable bond between the chip and its package, and the packaged device can exhibit the lowest possible thermal resistance.

4.1.2 Die Bonding

The package used for this work is shown in Figure 4.3. In order to bond a PHS ISIS chip to its package, a gold-tin solder perform is placed into the package which is being held in a heater stage at a temperature of 250°C. The ISIS chip is then drawn by vacuum into a conventional tungsten-carbide collect and placed over the solder. A stream of heated forming gas (80% nitrogen, 20% hydrogen) is directed at the bond area via a heater nozzle behind the die collet. Pressure is applied and held until the solder has been melted and displaced by the chip. The hot gas is then shut off in order to allow the solder to solidify. Provided that the package and solder are clean, temperatures are controlled, and appropriate bonding collet pressures are maintained, reliable performance can be expected from this bond.

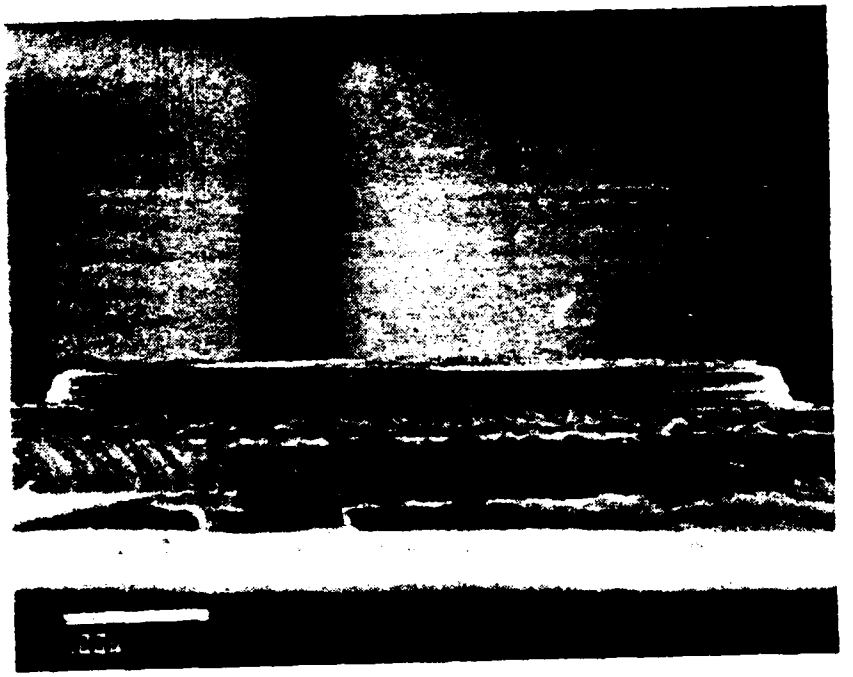
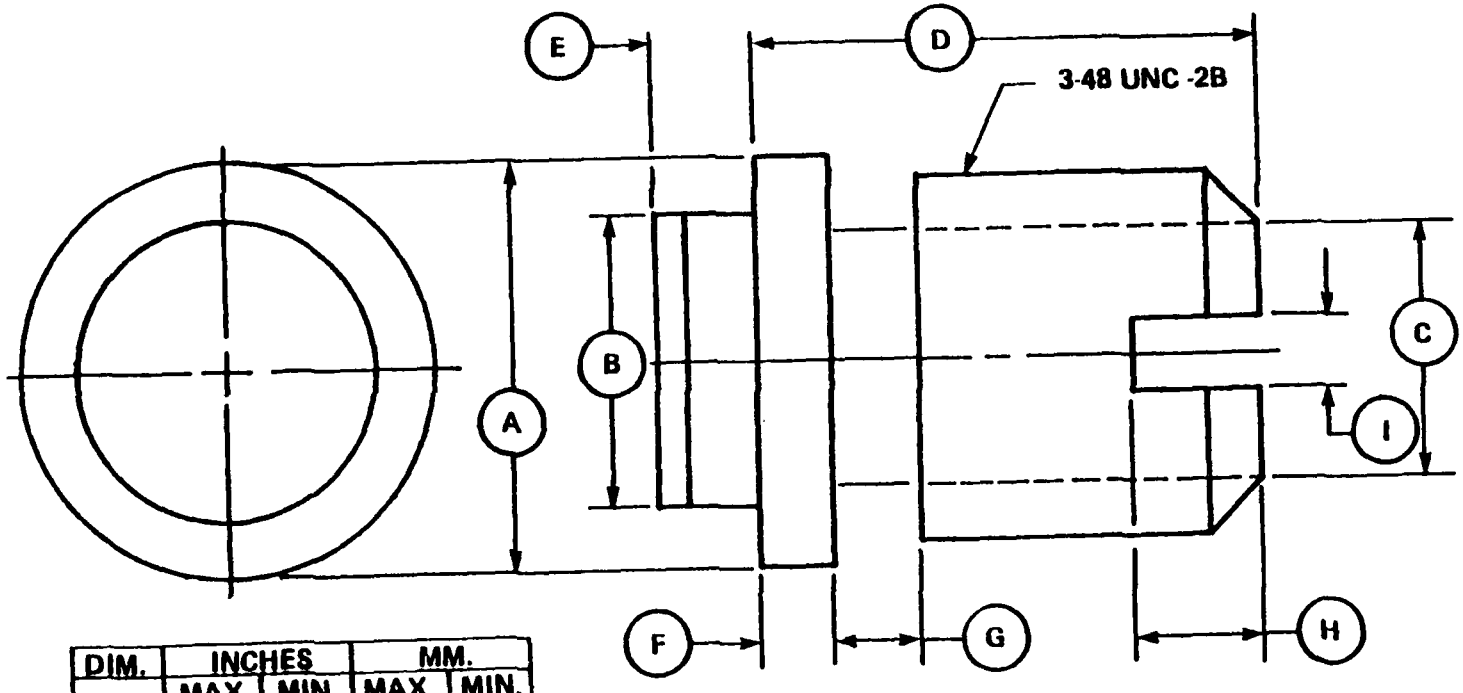


FIGURE 4.2 SEM PICTURE OF A PLATED HEAT SINK ISIS DIODE.



DIM.	INCHES		MM.	
	MAX.	MIN.	MAX.	MIN.
A	.118	.113	3.00	2.87
B	.084	.076	2.13	1.93
C	.072	.068	1.83	1.73
D	.146	.138	3.71	3.51
E	.034	.026	.86	.66
F	.022	.018	.56	.46
G	.020		.51	
H	.045	.025	.114	.64
I	.025	.015	.64	.38

FIGURE 4.3 SCHEMATIC OF THE PACKAGE USED FOR ISIS DIODES.

D-23747

4.1.3 Wire Bonding

Following die bonding, the ISIS chips are cleaned and prepared for visual inspection. The chips are inspected for several quality criteria which include cracked mesa, metallization voids or defects in geometry, and incomplete solder wetting. To minimize parasitic inductance, two gold ribbons (0.005" X 0.010") are cross-strapped to the ISIS chip. The ribbons are thermocompression bonded to the ohmic contact pad located on the substrate side of the chip.

4.1.4 Device In-Package Etch

Subsequent to ribbon bonding, the combined device and package capacitance, as well as the device breakdown voltage, are evaluated. At this point, poor I-V characteristics may be observed as a result of junction damage that may have occurred during fabrication. To restore good diode behavior, the junction of the packaged device is in-situ etched using a 2:1:1 (H_2SO_4:H_2O:H_2O_2) solution. After in-package etching, the device is (i) stabilized in a prolonged DI water rinse, (ii) boiled in isopropyl alcohol, and (iii) baked for one hour at 150°C in forming gas.

4.1.5 Capping

Devices with appropriate DC characteristics are capped using a gold-tin solder preform and a gold plated copper lid. For an experimental device, a temporary lid is placed on the package. After preliminary RF evaluations, the temporary lid can be removed in order to further reduce the device diameter by an in-situ etch.

SECTION 5
DEVICE EVALUATION

5.0 AUTOMATED DC TESTING

After device fabrication, the resulting diodes are evaluated for their DC characteristics. The DC parameters of interest include: (i) reverse and forward breakdown voltages, (ii) zero bias capacitance, and (iii) capacitance and leakage current at 80 percent of breakdown. At M/A-COM, the above parameters are measured using an automated test system as shown in the block diagram of Figure 5.1. The processor is a HP2112 minicomputer with software features which include open and short circuit detection and automatic polarity determination.

In addition to the parameters mentioned above, the automated DC test system is capable of generating capacitance-versus-voltage (C-V), doping versus depth (N-W), and electrical field versus depth (E-W) profiles of the diode under test. As mentioned in Section 3, the mesa configurations of Figure 3.8 (a) and (b) were respectively used to evaluate the second and first grown IMPATT diodes within the ISIS. The composite ISIS profile was determined by using the configuration of Figure 3.8 (c).

Examples of C-V, N-W, E-W plots generated by the automated test system for ISIS wafer #170 are presented in Figure 5.2. The characteristics of the second grown IMPATT diode in wafer #170 are shown in Figure 5.2(a). Its breakdown voltage on the test kit was given as 51.5 volts. This value was independently verified on a curve-tracer. Plots similar to Figure 5.2(a) are given in Figure 5.2(b) for the case of the first grown IMPATT device in wafer #170. Its breakdown voltage of 59 volts was also verified on an I-V curve tracer. The composite profiles of wafer #170 are given in Figure 5.2(c). Its I-V characteristic gave a reverse breakdown voltage of 110 volts (see Figure 5.2(d)).

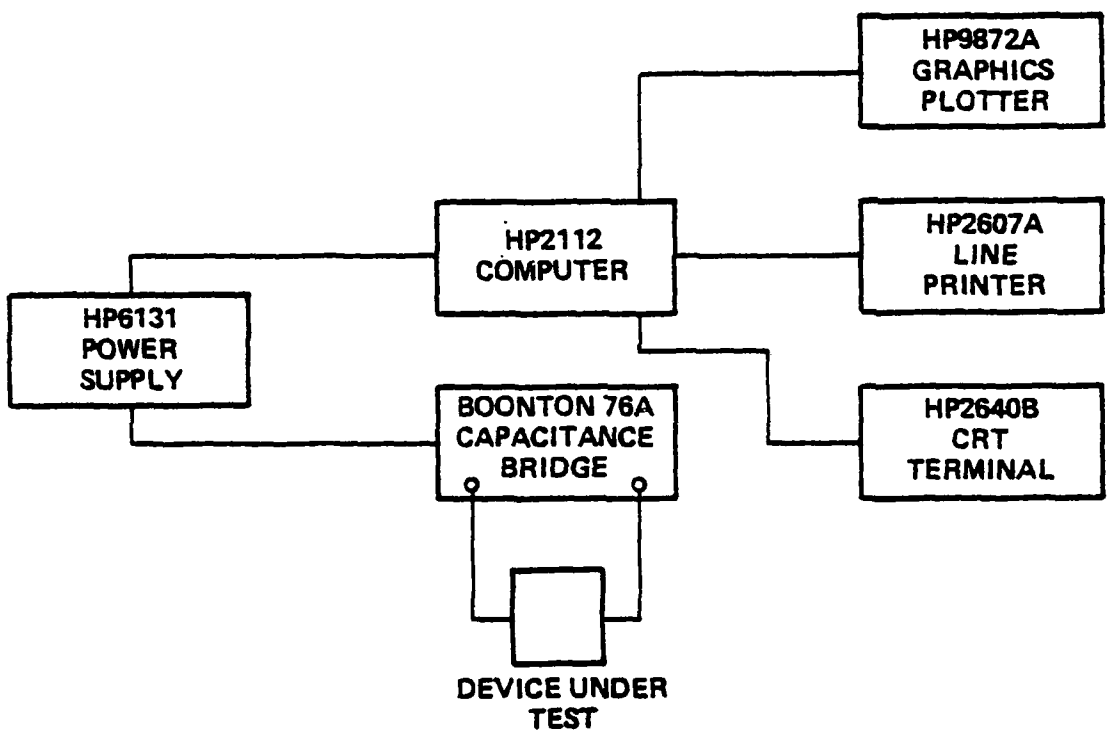


FIGURE 5.1 AUTOMATIC DOPING PROFILE MEASUREMENT SYSTEM.

D-17306

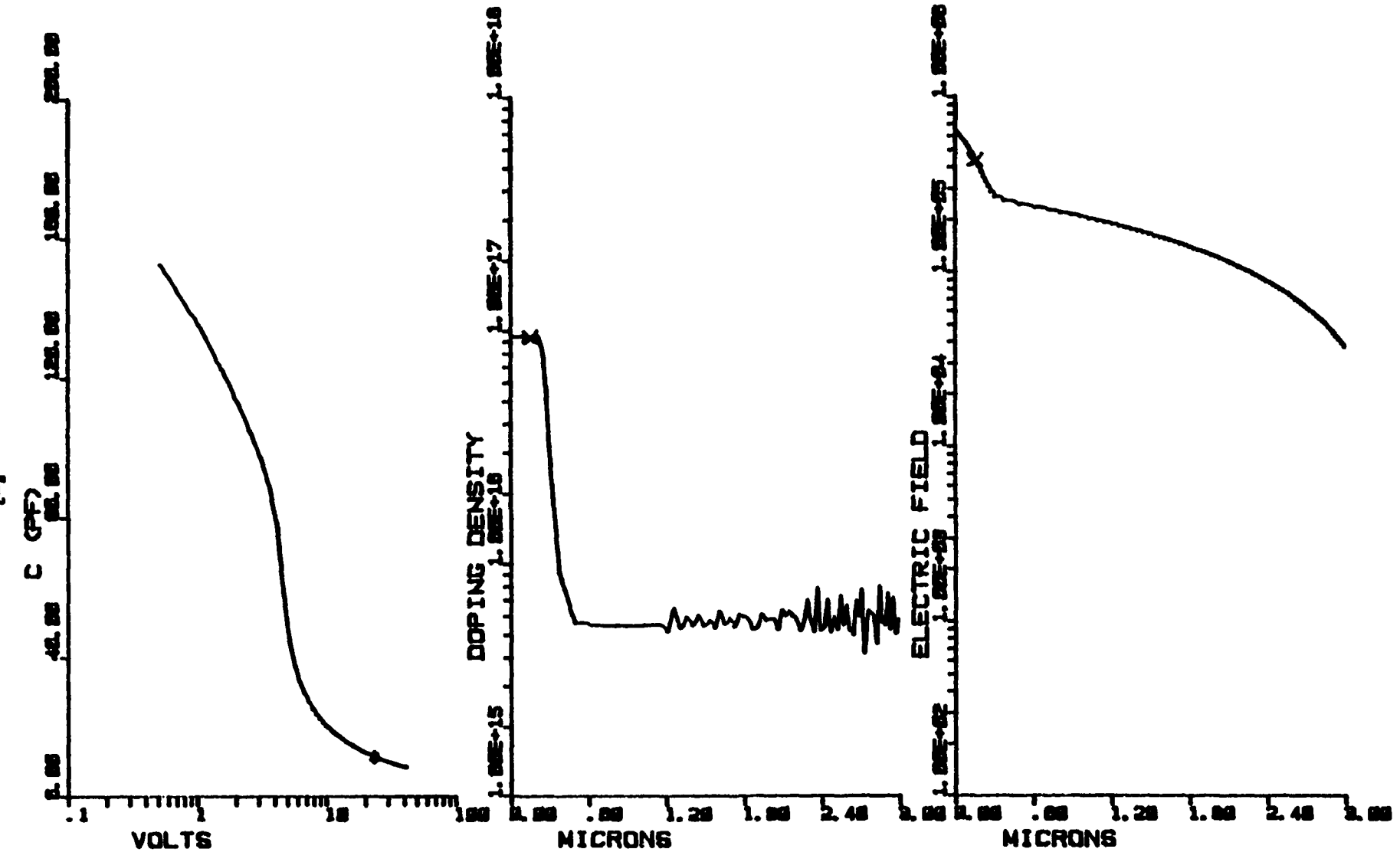


FIGURE 5.2(a): C-V, N-W, and E-W plots for second grown IMPATT diode in ISIS wafer #170. V_b = 51.5 volts.

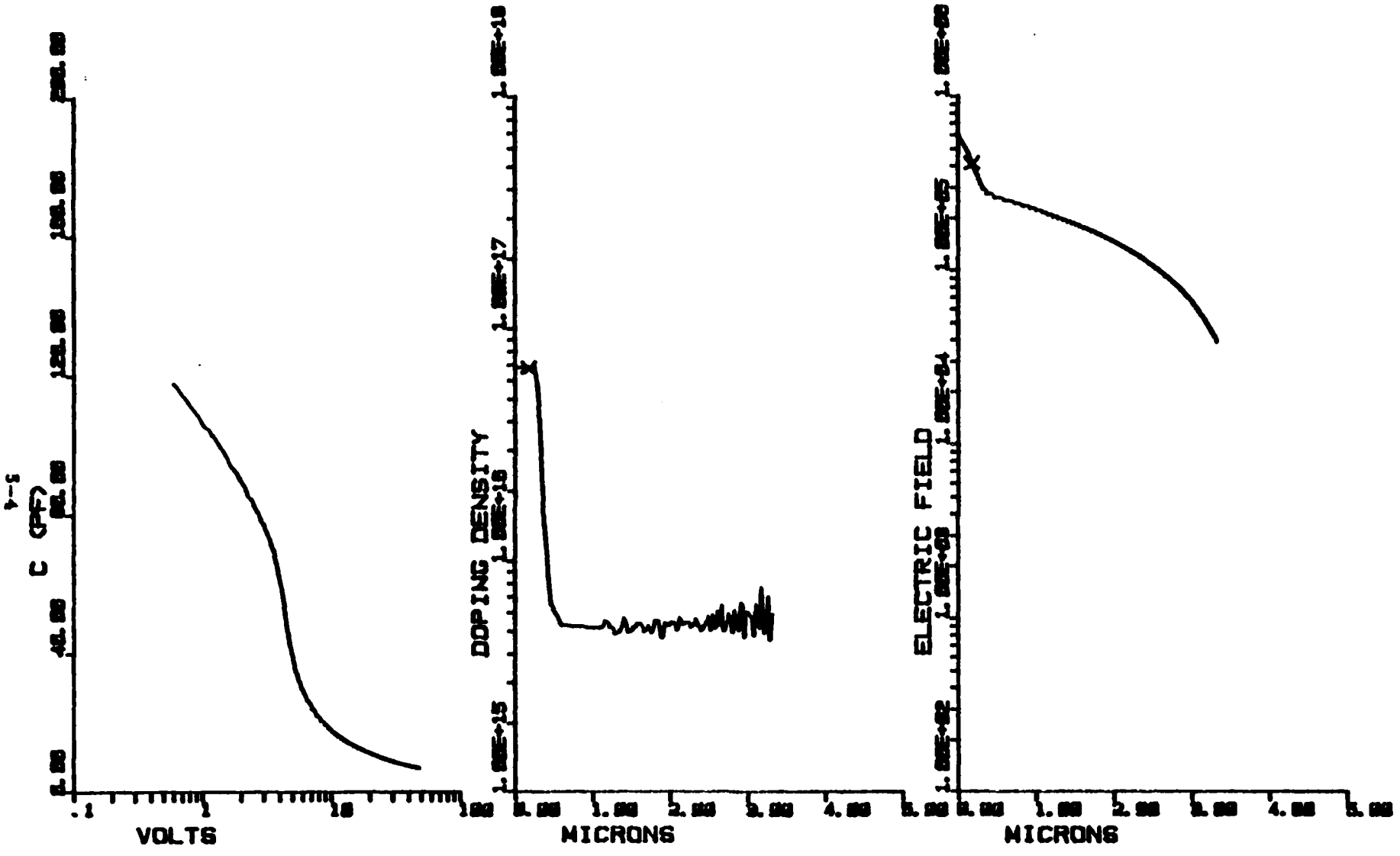


FIGURE 5.2(b): C-V, N-W, and E-W plots for first grown IMPATT diode in ISIS wafer #170. V_b = 59 volts.

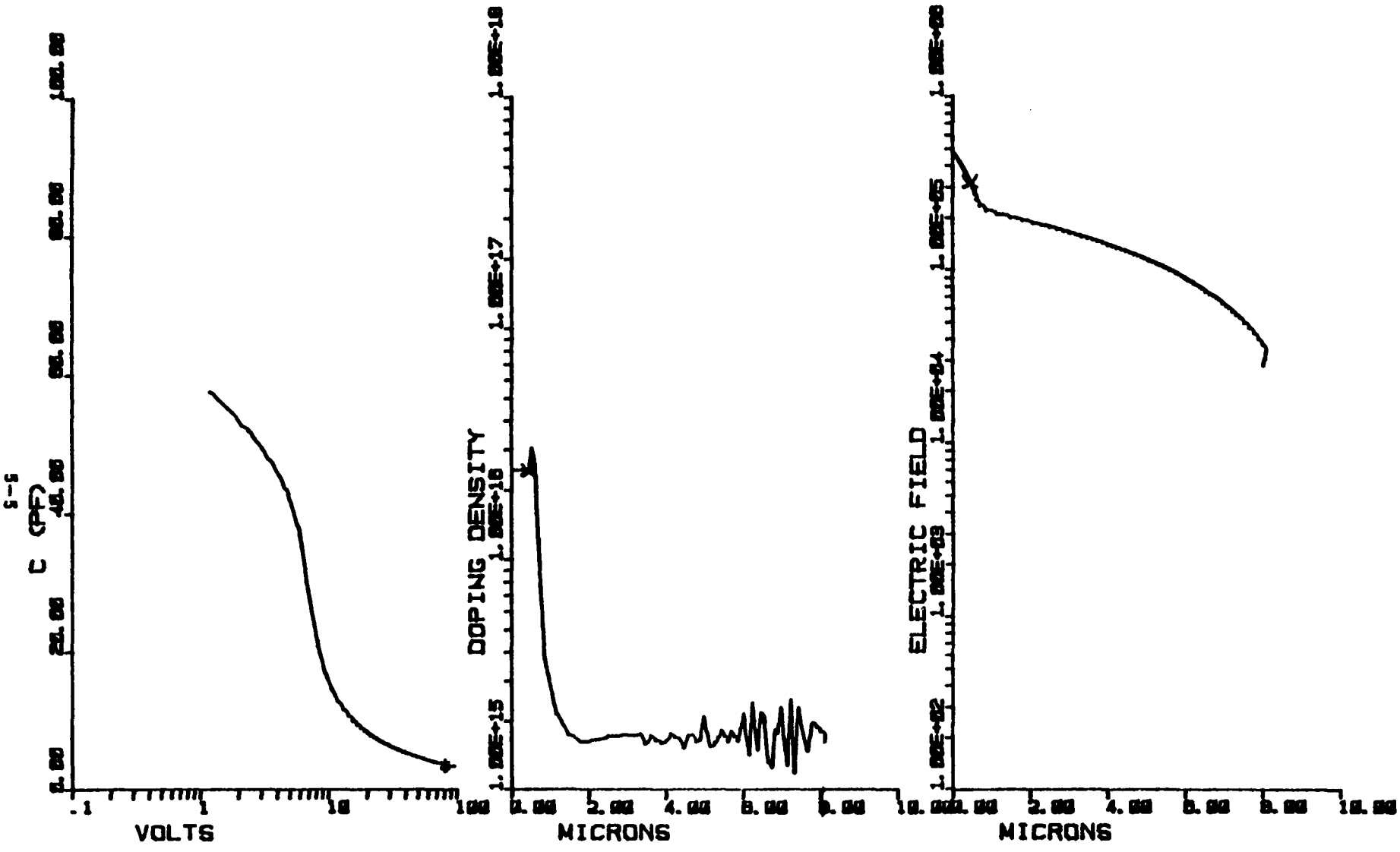


FIGURE 5.2(c): Composite characteristics for ISIS wafer #170.

As expected, the reverse breakdown voltage of the composite ISIS profile is in close agreement with the total breakdown voltage observed for the profiles shown in Figures 5.2(a) and (b). The forward voltage of 3.8 volts @ 1mA for the ISIS device is shown in Figure 5.2(e). This value of forward voltage accounts for two forward biased junctions (1.1 volts each), as well as a reverse biased $P^{++}N^{++}$ junction (V_R = 1.6 volts). The small contribution of V_R reflects the desired high doping of the $P^{++}N^{++}$ junction that separates the two IMPATT devices in the ISIS.

Of the several VPE HI-LO ISIS growth runs, two wafers gave diodes that exhibited good RF performance. The epitaxial characteristics of the two ISIS wafers are given in Table 5.1.

5.1 Thermal Resistance Measurement

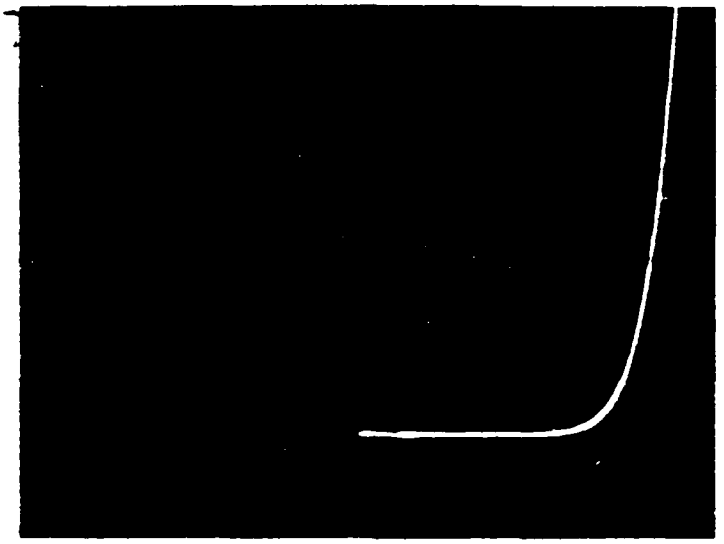
The technique used in measuring the thermal resistance of an IMPATT diode is based on the temperature dependence of its breakdown voltage, i.e.,

$$V_b(T_j) = K_T(T_j - T_c) + V_{BO} \qquad (5.1)$$

where:

T_j= junction temperature, °C
T_c= case temperature, °C
V_{BO}= breakdown voltage at $T_j = T_c$
K_T= temperature coefficient of breakdown voltage, V/C°.

The circuit used to measure the thermal resistance of an IMPATT diode is shown in Figure 5.3. The diode is placed in a test fixture and biased at the operating point. Diode oscillations are suppressed by the use of a graphite load material in the test fixture. A negative-going pulse of 500 nanoseconds duration is introduced across the diode and the amplitude adjusted until the diode peak current equals the DC current. The pulse



H: 1volt/div.
V: ·2mA/div.

FIGURE 5.2(e): Forward I-V characteristic for ISIS wafer #170.

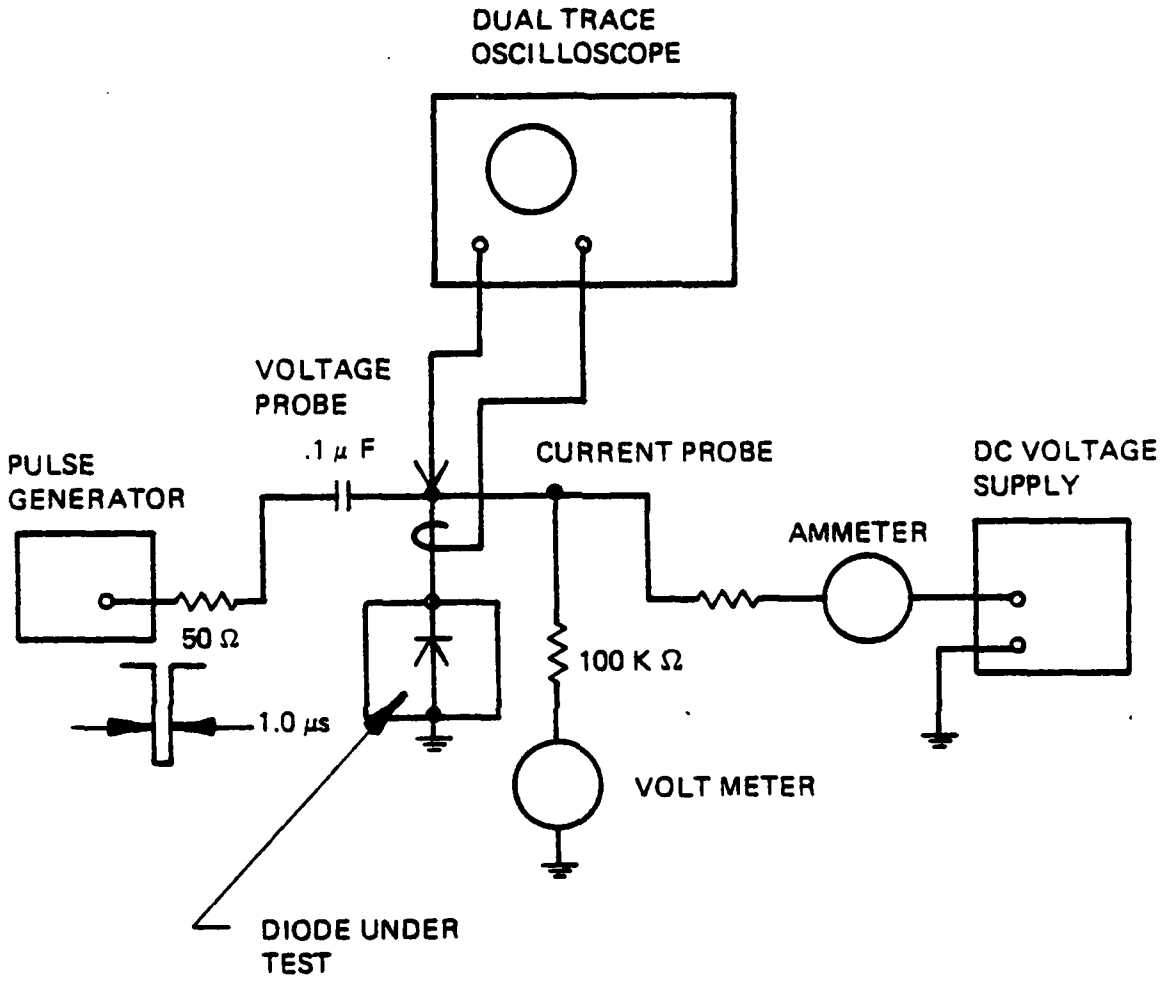
TABLE 5.1: DOPING AND THICKNESS RESULTS FOR TWO VPE HI-LO ISIS WAFERS.

1) Wafer #170

Layer	Doping Density(cm^{-3})	Thickness (μm)
P^{++} contact	$\geq 1X10^{19}$	1.0
N-high	$9.7X10^{16}$	0.17
N-low	$6.1X10^{15}$	5.5
N^{++} buffer	$2.5X10^{18}$	3.0
P^{++} layer	$\geq 1X10^{19}$	4.0
N-high	$6.9X10^{16}$	0.21
N-low	$5.6X10^{15}$	5.0
N^{++} buffer	$2.5X10^{18}$	3.5

2) Wafer #183

Layer	Doping Density(cm^{-3})	Thickness (μm)
P^{++} contact	$\geq 1X10^{19}$	1.0
N-high	$8.9X10^{16}$	0.21
N-low	$6.0X10^{15}$	5.6
N^{++} buffer	$2.5X10^{18}$	4.5
P^{++} layer	$\geq 1X10^{19}$	4.5
N-high	$8.3X10^{16}$	0.21
N-low	$5.7X10^{15}$	5.6
N^{++} buffer	$2.5X10^{18}$	3.5



$$\theta_J = \left[\frac{V_B - V_{BO}}{K_T} + T_{co} - T_C\right] \frac{1}{V_{DC}\, I_{DC}}$$

FIGURE 5.3 EQUIPMENT USED IN IMPATT THERMAL RESISTANCE MEASUREMENT.

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voltage required at the diode is then subtracted from the applied DC voltage in order to give a breakdown voltage value, measured with the junction at normal operating temperature. Because the pulse duration is much less than the chip thermal time constant, negligible cooling occurs.

Using equation (5.1), the junction temperature, and thus, the thermal resistance of the device may be calculated if K_T is known. The temperature coefficient of breakdown voltage may be measured by removing the DC bias and applying external heat to the diode, while observing the pulsed breakdown voltage. In practice, the breakdown voltage is measured as a function of T_C for a few sample diodes from a given wafer and K_T determined from a best fit line drawn on a V_b versus T_C plot. Case temperatures of 100, 150, and 200°C are used. The value of K_T obtained is then used to characterize the thermal resistance of other diodes from the wafer. The equation used to determine the thermal resistance of an IMPATT diode is given in Figure 5.3.

5.2 RF Evaluation

IMPATT diodes are characterized by a low value of negative resistance. The RF test fixtures, therefore, have certain requirements for gallium arsenide IMPATT diodes. The test circuit must transform the waveguide or coaxial line impedance (usually about 300 ohms in a waveguide or 50 ohms in a coaxial cavity) to the diode impedance, with a minimum of circuit loss. The test fixture must be able to resonate the device at the correct frequency. Finally, the test fixture should have the capability of easily adjusting both resistance and reactance to match the appropriate device impedance.

RF testing is carried out using the equipment shown in the block diagram of Figure 5.4. The device under test (mounted in a coaxial test cavity) is connected to a power detector through a tuner, isolator, and precision attenuator. Directional couplers are used to supply signals to a spectrum analyzer and diode detector. Pulsed bias is supplied from a Cober Type 604 pulse amplifier driven by a HP-214A pulse generator.

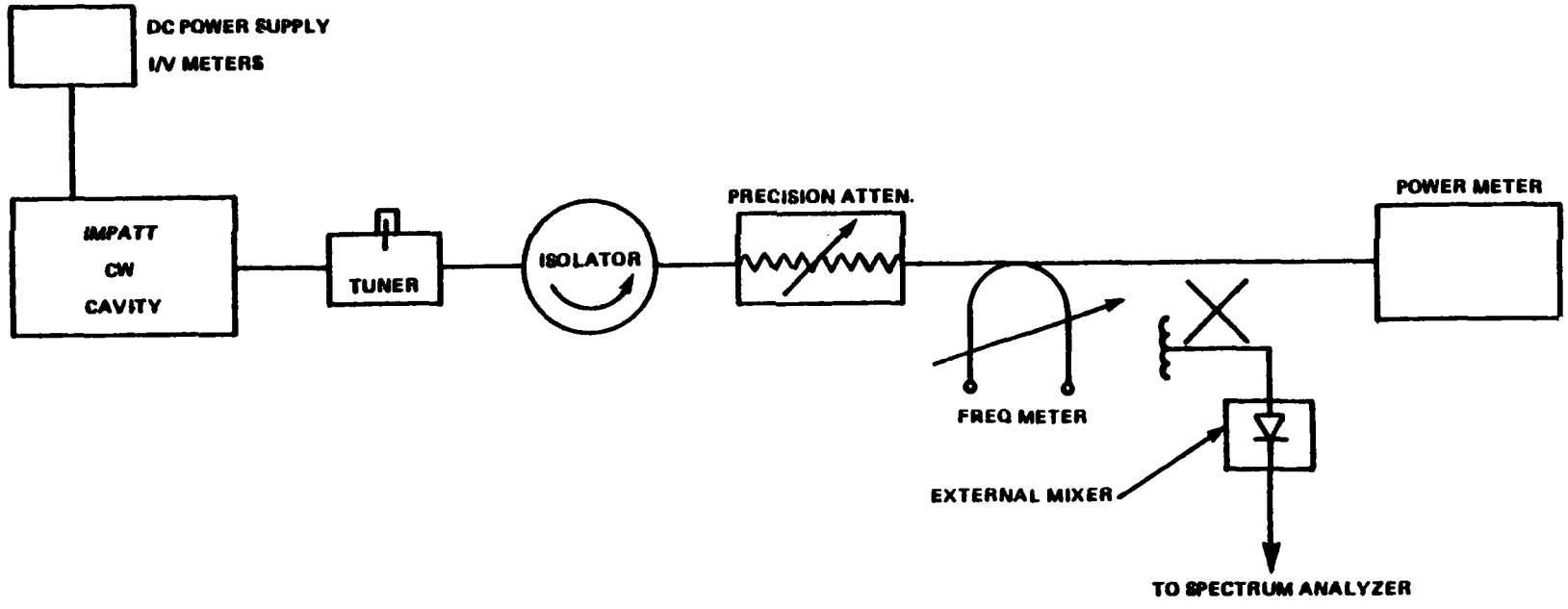

FIGURE 5.4 RF TEST SET-UP.

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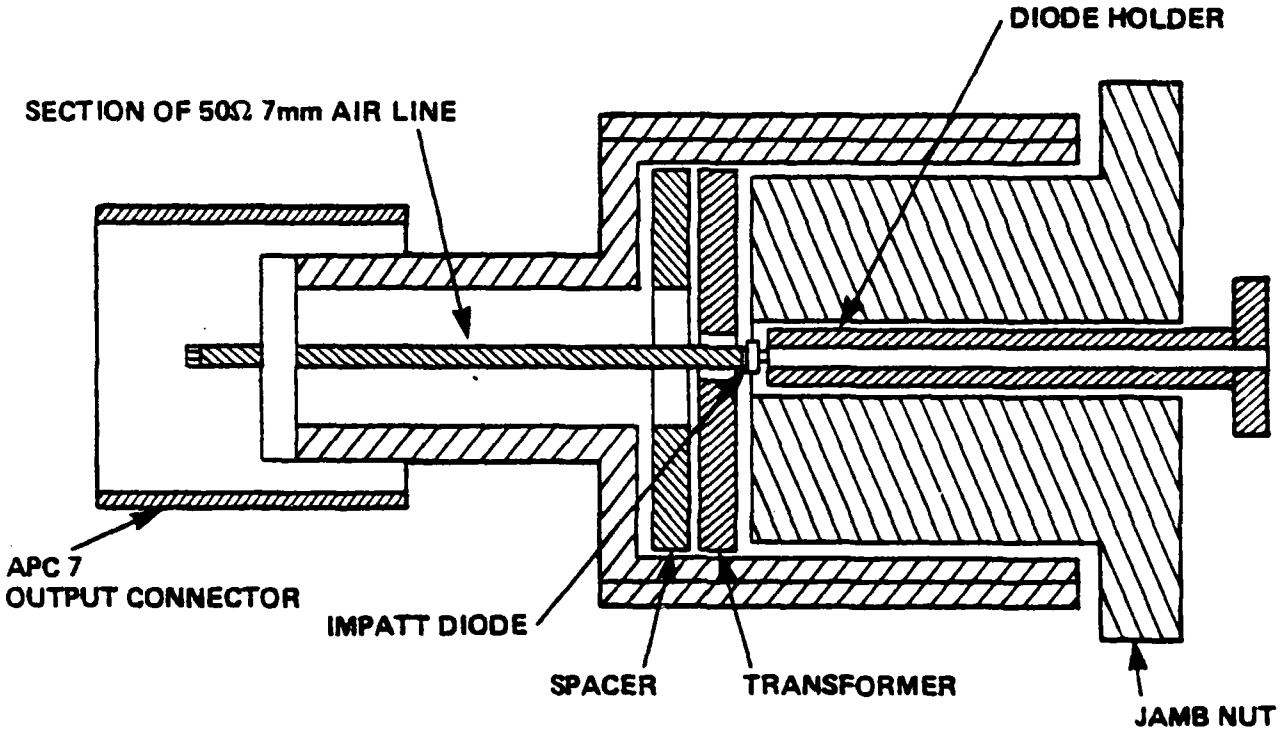

FIGURE 5.5 COAXIAL CAVITY IMPATT TEST FIXTURE.

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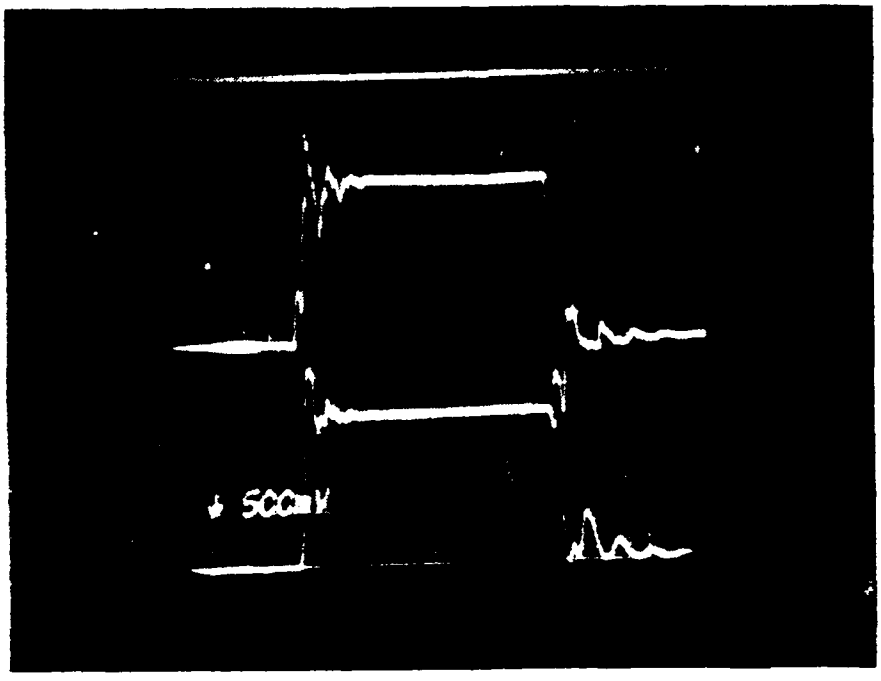
TABLE 5.3: DC AND RF TEST DATA FOR THE 1ST LOT OF ISIS DIODES (WAFER #183) DELIVERED TO NRL.

Device No.	V_B	C_o	Peak Power	F_{op}	V_{op}	I_{op}	η	θ	S/N
	[Volts]	[pF]	[Watts]	[GHZ]	[Volts]	[Amps]	[%]	[°C/W]	
1	108	57.9	16.24	9.272	120	1.55	8.73	6.1	0145
2	106	53.3	16.24	9.308	122	1.55	8.59	5.7	0145
3	108	58.6	16.24	9.282	120	1.55	8.73	6.3	0145
4	108	58.4	16.24	9.305	122	1.60	8.32	5.9	0145
5	108	52.9	16.24	9.583	122	1.50	8.87	6.2	0145
6	108	58.6	16.24	9.282	120	1.55	8.73	5.9	0145
7	108	57.6	16.24	9.304	120	1.55	8.73	6.0	0145
8	105	58.1	16.24	9.292	120	1.55	8.73	6.2	0145
9	107	56.3	16.24	9.305	122	1.55	8.59	5.4	0145
10	108	56.5	16.24	9.292	122	1.60	8.32	6.1	0146
11	108	57.3	16.24	9.292	120	1.60	8.46	5.6	0146
12	108	56.1	16.50	9.308	122	1.60	8.45	5.3	0146
13	108	56.0	16.50	9.292	120	1.60	8.59	6.3	0146
14	108	58.8	16.00	9.292	120	1.50	8.89	5.9	0146
15	108	58.2	16.00	9.305	122	1.55	8.46	5.6	0146

TABLE 5.4: DC AND RF TEST DATA FOR THE 2ND LOT OF ISIS DIODES (WAFER #183) DELIVERED TO NRL.

Device No.	V_B	C_o	Peak Power	F_{op}	V_{op}	I_{op}	η	θ	S/N
	[Volts]	[pF]	[Watts]	[GHz]	[Volts]	[Amps]	[%]	[°C/W]	
1	108.0	50.5	17.98	9.572	120.0	1.50	9.99	6.1	10061
2	106.0	56.3	15.66	9.566	125.0	1.50	8.35	6.1	10062
3	103.0	59.0	15.66	9.486	118.0	1.50	8.85	5.4	10063
4	107.0	60.3	16.59	9.487	115.0	1.50	9.62	5.7	10064
5	106.0	59.5	15.08	9.506	115.0	1.45	9.04	5.2	10065
6	100.0	56.9	14.50	9.600	120.0	1.50	8.06	6.2	10066
7	104.0	58.1	14.50	9.537	115.0	1.50	8.41	5.9	10067
8	104.0	59.8	15.66	9.530	115.0	1.50	9.08	5.8	10068
9	106.0	50.9	15.66	9.582	120.0	1.50	8.70	6.3	10069
10	106.0	53.4	15.66	9.580	120.0	1.50	8.70	7.3	10070



PW = 1μs DUTY = 10%

FIGURE 5.6. TYPICAL OPERATING VOLTAGE AND CURRENT WAVEFORMS FOR ISIS DIODES FROM WAFER NO. 183.

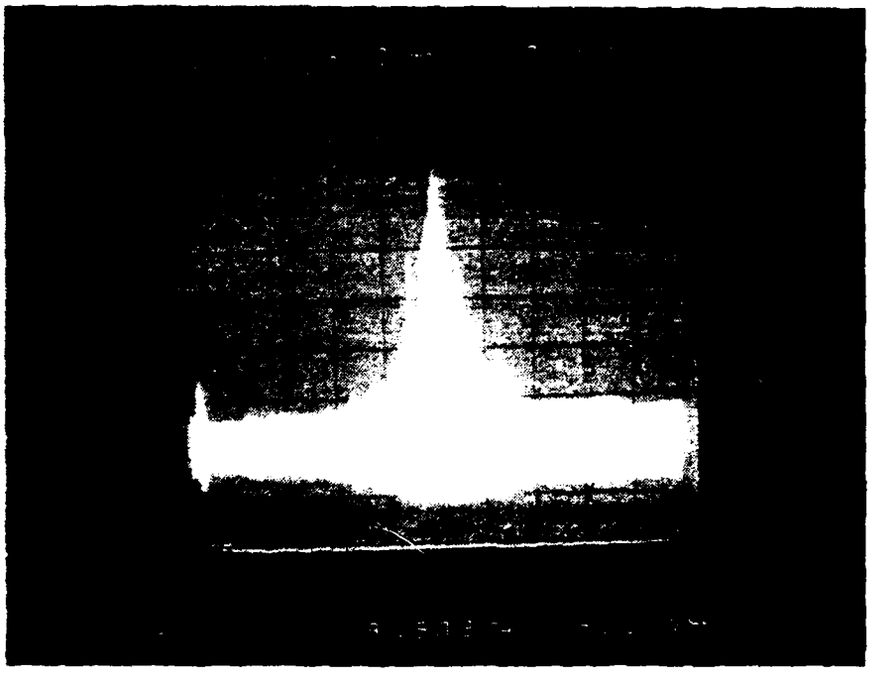


FIGURE 5.7 TYPICAL FREQUENCY SPECTRUM FOR A FREE RUNNING ISIS DIODE IN A COAXIAL CAVITY.

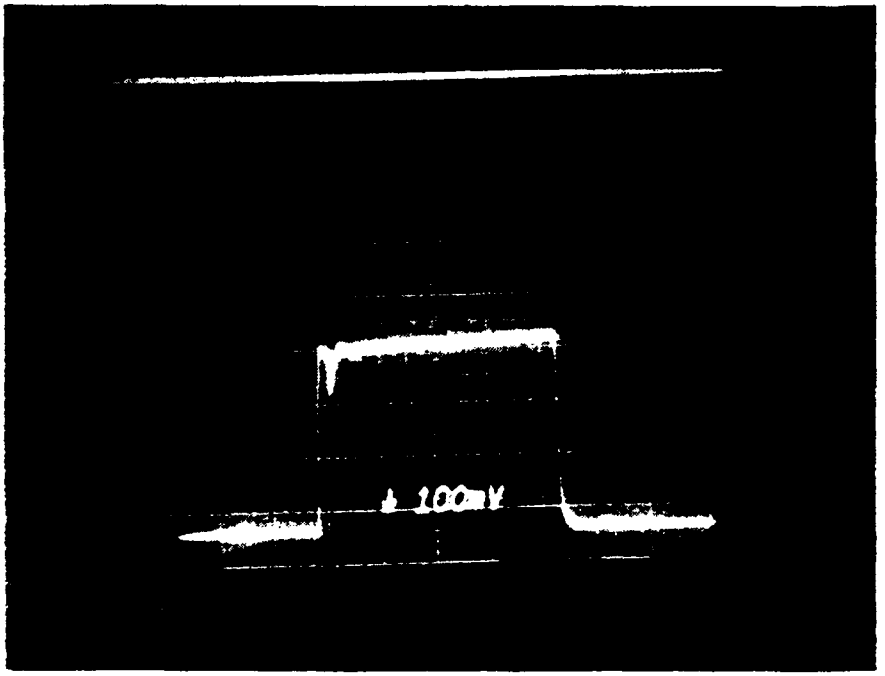


FIGURE 5.8 DETECTED RF WAVEFORM FOR A TYPICAL ISIS DIODE.

SECTION 6
CONCLUSIONS AND RECOMMENDATIONS

The significant accomplishment under this program is the development of an Integrated Series IMPATT Structure capable of generating 16 watts of peak power at 9.4 GHz. To achieve this result, major emphasis was given to (a) device design and demonstration of the ISIS concept using physically stacked single-drift IMPATT chips, (b) material preparation using halide-VPE techniques, and (c) characterization of ISIS epitaxial material.

As discussed in Section 2, design considerations addressed two critical aspects of the ISIS device, namely: (a) injection of minority carriers across the tunnel junction that separates the two single-drift IMPATT diodes and (b) the operating junction temperature of the IMPATT device that is further away from the heat sink. To minimize the extent of minority carrier injection into the two IMPATT diodes, the sandwiched P^{++} and N^{++} layers were each designed to be 4 microns thick with $N_A=3.5X10^{19}/cm^3$ and $N_D=2.5X10^{18}/cm^3$, respectively. The anticipated higher junction temperature for the device located further away from the heat sink was accounted for by designing its doping profile such that its breakdown voltage was less than that of the other IMPATT device in the ISIS.

With the design considerations mentioned above, several halide-VPE growth experiments were aimed at producing the desired HI-LO ISIS doping profile. Of the several attempts, two epitaxial wafers gave devices that exhibited very encouraging RF test data. While the results were very encouraging, they were not as good as those reported in our studies concerning physically stacked single-drift IMPATT chips. It is concluded here that the reasons for not achieving comparable "stacked-chip" results is due to (a) the mis-match of the IMPATT diodes in our VPE ISIS devices. For the results given in Tables 5.2 through 5.4, the breakdown voltage of the 1st grown device was greater than that of the 2nd.

This is the opposite of the design model and was not anticipated in the VPE growth runs. (b) The actual doping profile for the two IMPATTS in ISIS wafers #170 and #183 was different from their respective design parameters. (c) The speculation that the tunnel junction separating the two IMPATTS may not be adequate. The calculations used for the design of the P^{++} and N^{++} layers were based on material parameters ($\tau_{N,P}$ and $\mu_{N,P}$) which may not be accurate, since they were extrapolated from published data.

Based on the above conclusions, it is recommended that further work should be directed in the following areas:

(a) Now that the epitaxial growth and characterization techniques have been developed, more iterations of growth runs should be performed to achieve the desired HI-LO ISIS doping profile.

(b) To address the speculation concerning the tunnel junction, growth experiments should be performed whereby the P^{++} and N^{++} sandwiched layers are doped to the extent that their solid solubility limit is approached.

(c) The ISIS concept should also be attempted for devices operating at higher frequencies. At higher frequencies, where the layer thicknesses are much less that those required at X-band, an ISIS design profile should be easier to achieve since there will be less constraints placed on the epitaxial growth system.

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