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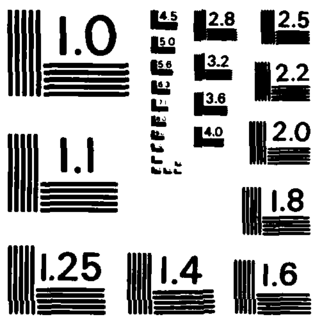
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VLSI Memo No. 85-259 September 1985

Contract N00014-85-K-0213

MASTIF - A Workstation Approach to Fabrication Process Design*

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ABSTRACT

The design of a fabrication process increasingly necessitates the availability and use of a variety of tools, including process and device simulation, analysis, and synthesis aids. The MASTIF workstation (MIT Analysis and Simulation Tools for IC Fabrication) is a menu and window oriented program written in C and Fortran which provides a methodology and uniform software structure for the connection of process and device design tools. MASTIF currently includes a facility for incremental development and version management of a process description, management mechanisms for definition of physical cross sections deriving from the overall process description, and an interactive graphics interface and data interchange for process and device simulators (SUPREM-III and MINIMOS). With MASTIF, the user can effectively develop and evaluate a fabrication process via a single integrated workstation.

*To be presented at the International Conference on Computer-Aided Design, Santa Clara, California, November 18-21, 1985. This work was supported in part by DARPA contract no. N00014-85K-0213 and by a National Science Foundation Graduate Fellowship.

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PRELIMINARY DRAFT
This paper is to be presented at ICCAD-85.

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Abstract

The design of a fabrication process increasingly necessitates the availability and use of a variety of tools, including process and device simulation, analysis, and synthesis aids. The MASTIF workstation (MIT Analysis and Simulation Tools for IC Fabrication) is a menu and window oriented program written in C and Fortran which provides a methodology and uniform software structure for the connection of process and device design tools. MASTIF currently includes a facility for incremental development and version management of a process description, management mechanisms for definition of physical cross sections deriving from the overall process description, and an interactive graphics interface and data interchange for process and device simulators (SUPREM-III and MINIMOS). With MASTIF, the user can effectively develop and evaluate a fabrication process via a single integrated workstation.

Motivation

Spurred by the increasing complexity of VLSI design, many CAD tools have been developed to provide help in successive phases of design, from system specification through circuit realization to mask layout. Many of these design tasks can be accomplished on integrated workstations, where tools for capture and synthesis are accompanied by verification and simulation programs.

The design of the fabrication process, on the other hand, is a task which suffers from a lack of similar computer assistance. Process simulators such as SUPREM [1] and SUPRA [2] have been developed to model the fabrication process; simulators such as MINIMOS [3] also exist for the evaluation of semiconductor devices. Few integrated systems exist which provide both simulation and synthesis tools in the domain of device and process design [4]. Such an integrated workstation is needed to meet a number of particular process design needs.

Requirements for a Process Design System

As with each of the other IC design phases, a process design system is needed to provide aid in roughly two categories: simulation and synthesis. This section will examine these two aspects in turn. The role, utilization, and requirements of CAD tools in process simulation are discussed below:

1. ROLE OF PROCESS SIMULATION: A process simulator transforms a starting representation of the wafer structure (or initial wafer state) into a final representation under the influence of a specified wafer treatment. By performing successive simulation steps to model the actual sequence of fabrication operations, one, two, or (eventually) even three dimensional models of a a device or wafer structure can be constructed. Thus, SUPREM-III provides material and impurity concentration information for one-dimensional cross-sections, while SAMPLE [5] calculates two-dimensional geometric effects resulting from lithographic, deposition, and etching process steps.

2. USE OF PROCESS SIMULATORS: The structure produced by process simulators is useful only so far as means are also available for the analysis and evaluation of the structure with respect to formal or informal goals. Some analysis capabilities, such as sheet resistance or junction depth calculations, are usually built into process simulators.

3. PROCESS SIMULATION REQUIREMENTS

a. Common Interface: An interface between the process engineer and the multitude of simulators is important for two reasons. First, the variety of simulation protocols or languages makes use tedious; a translation from a single description of the process to the particulars of each simulator is needed. Secondly, a unique description of the process is important in order to guarantee that the various simulators create consistent structural information.

b. Computation: Process simulation is driven by complex and often incompletely understood physics. As such, process simulation is a computationally intensive and time consuming task. Mechanisms for reducing the amount of simulation during process development are needed.

c. Device Simulation: Often very sophisticated analysis of the wafer structure is needed. A model of a whole device structure constructed from process simulation results is usually evaluated using device simulators. For example, the threshold voltage for an MOS device or a response to specified bias conditions may be the measure of "success" for a particular process. Adequate process analysis thus requires a good interface between device and process simulators.

The requirements for process "capture" or synthesis can be summarized as follows:

1. *PROCESS REPRESENTATION:* The goal of process synthesis is to produce a fabrication process which meets a set of goals. Clearly, some representation of the process is required. This process specification must be powerful enough to construct structure representations using a variety of process simulators, but must be independent of any particular simulator.

2. STRUCTURE REPRESENTATION: A uniform representation of device or wafer structures would be useful as a common interchange between different process simulators, analysis tools, device simulators, and graphic display packages. In the absence of such an interchange format, explicit interfaces must be developed where needed.

3. DESIGN MANAGEMENT: Just as in circuit design, a great need for documentation and version management exists in the design of a process. Version control is particularly complicated in process design. The engineer must not only compare the effects of different process parameter choices, but it must also examine the effects of a choice in several different regions or cross-sections of the physical structure. That is, the system must manage structures that change with process modifications, spatial position, and simulation time.

4. AUTOMATIC SYNTHESIS: The creation of a fabrication process is currently a highly intuitive and complex task. The physical structure depends on process parameters in a very nonlinear manner, and the tradeoffs to be managed are ill-defined. These characteristics make it difficult both for engineers to develop processes and for researchers to develop expert systems.

The MASTIF Process Design Workstation

The MASTIF workstation is a first attempt at meeting the requirements for process design outlined above. The current capabilities of MASTIF will be summarized; tools that have been developed or incorporated into the workstation will be described. This will be followed by a discussion of the implementation of MASTIF, with emphasis on mechanisms for extending the system to include additional tools.

1. MASTIF CAPABILITIES: an integrated workstation approach to process design has been adopted. The user interacts with a single graphics screen via a tablet and keyboard; a variety of menus and windows can be displayed simultaneously. The basic user modules in MASTIF are summarized in Figure 1.

A Process Description Window gives the engineer the ability to interactively create and edit a fabrication Process Description. This description is independent of any particular process simulator, and includes constructs for version management.

A Cross Section Summary Window allows the engineer to specify a number of one or two dimensional regions or cross sections for both process and device simulation. Masking or layout information is incorporated here. This window is also responsible for maintaining consistency between the Process Description Window and the various Process Simulation Windows.

A number of different Process Simulation Windows can be used simultaneously. Given the global Process Description and masking information for a specified cross section, a SUPREM One-Dimensional window can be created and updated automatically. From the menu in this window, the user can direct background simulation of particular steps, as well as interactively produce plots or calculations of steps in the process. Currently, only SUPREM-III simulations are available; eventually both one and two-dimensional simulators will be incorporated.

A Device Simulation Window can also be generated, given the cross section and process simulation information. The user may direct and evaluate MINIMOS simulations from the menu of this window. The results of simulations may also be examined graphically through a MIDAS window. This subsystem consists of a general purpose MINIMOS plotting module and an interactive Focused Ion Beam simulation subsystem.

2. MASTIF IMPLEMENTATION: Mastif is implemented in C and Fortran, and currently runs on a multi-user VAX 11/750 under VMS. An AED 767 color graphics display terminal with tablet and mouse and a keyboard completes the hardware. The MFB graphics package [6] has been used to achieve some degree of device independence. Several modules have been written to support the user windows described above.

A simple syntax generation and parsing subsystem provides the capability for programmers to write new "syntaxes" using a parameter specification grammar (similar to the grammar used in SUPREM-III). Examples of syntaxes which are expressed by MASTIF using this grammar include the Process Description, the SUPREM-III input language, the Cross Section summary, and the MINIMOS input language. Once a syntax is specified, text files may be read by MASTIF, expressed and manipulated either graphically or textually by window handlers, and rewritten as text files for storage purposes.

A menu handling subsystem provides for the generation and use of simple menus. These menus are associated with each window, and may be either permanent or "pop-up" in format. Special purpose menus (such as a color selection menu) can also be generated.

A Main Menu and Command Area are included. Information and prompts may be issued, and textual inputs accepted from the window. A Browsing Window allows the user to examine system files.

A Background Job Handling system manages the executions of SUPREM and MINIMOS jobs. In order to maintain modularity and extensibility of the system, MASTIF has adopted a methodology for inclusion of simulation tools whereby all simulators are maintained in a stand-alone form. MASTIF will generate the input files, manage execution, and access results of simulators in a manner that does not require modification of the simulation programs themselves.

Evaluation of MASTIF

MASTIF has so far been useful in a number of ways. At the very least, the SUPREM Cross Section Windows provide a powerful, interactive user interface to the SUPREM-III simulator. Secondly, the ability to create a Process Description and maintain simulation consistency in multiple regions of the wafer in the face of an evolving process is quite useful. Moreover, the availability of a Process

Description is advantageous in that it may interface quite well with process recipe generation programs.

In an effort to maintain the interactive and extensible nature of MASTIF, we have found that MASTIF becomes file intensive. Intermediate SUPREM simulation results are now stored as the binary data files normally produced by SUPREM. All interfaces, both with regard to input file generation and to wafer structure exchange, have been written explicitly. A profile or wafer interchange format for the storage and exchange of wafer and device structure information is currently under consideration.

A workstation approach, stress upon a uniform, interactive interface between tools, MASTIF, and the engineer, and the availability of a base of MASTIF subsystems make it possible to add tools to MASTIF as they are developed. As additional process and device simulation and analysis tools are integrated into the system, it is expected that MASTIF will become a powerful system for the design of semiconductor devices and fabrication processes.

Acknowledgements

This material is based upon work supported by DARPA contract N00014-85K-0213. The work of D. Boning was supported in part by a National Science Foundation Graduate Fellowship. The contributions of J. Jacobs, T. Tung, and R. Lowther are gratefullly acknowledged.

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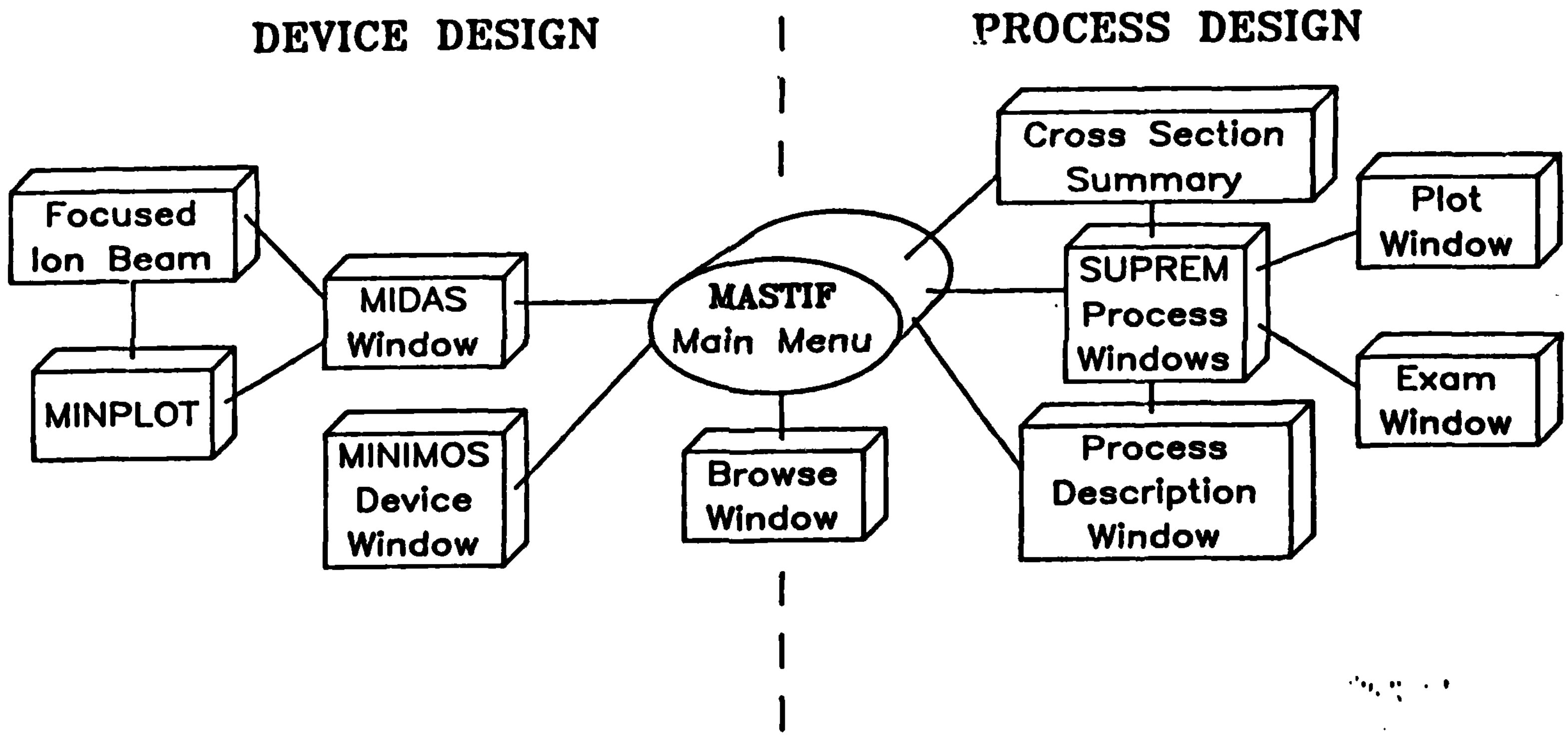
List of Figures

Figure 1. MASTIF User Windows


DEVICE DESIGN
PROCESS DESIGN
Focused Ion Beam
MINPLOT
MIDAS Window
MINIMOS Device Window
MASTIF Main Menu
Browse Window
Cross Section Summary
SUPREM Process Windows
Process Description Window
Plot Window
Exam Window

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