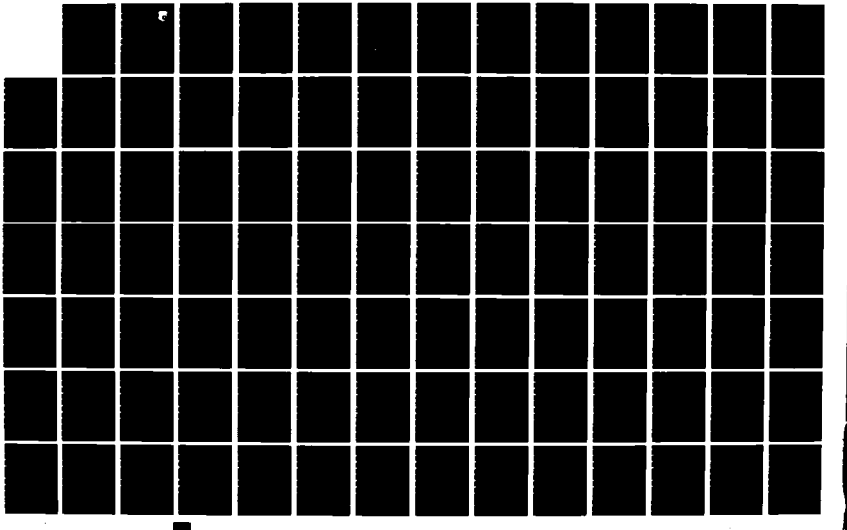
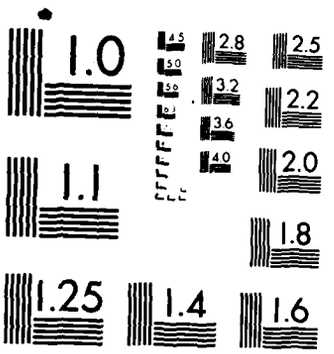
AD-A162 360 ADVANCED INVERTER TECHNOLOGY(U) MARTIN MARIETTA 1/2
AEROSPACE DENVER COLO ENGINEERING DEPT
C R GRIESBACH ET AL OCT 85 MCR-85-613 AFWAL-TR-85-2065
UNCLASSIFIED F33615-82-C-2239 F/G 10/2 NL





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AFWAL-TR-85-2065

ADVANCED INVERTER TECHNOLOGY

AD-A162 360

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P.O. Box 179
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October 1985

Final Report for Period October 1982–October 1985

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This report has been revised by the Office of Public Affairs (ASD/PA) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

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AD-A168 350

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; Distribution unlimited.
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) MCR-85-613	5. MONITORING ORGANIZATION REPORT NUMBER(S) AFWAL-TR-85-2065
6a. NAME OF PERFORMING ORGANIZATION Martin Marietta 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION Aero Propulsion Laboratory (AFWAL/POOC)
6c. ADDRESS (City, State and ZIP Code) P. O. Box 179 Denver, CO 80201	7b. ADDRESS (City, State and ZIP Code) Air Force Wright Aeronautical Laboratories Wright-Patterson Air Force Base, OH 45433
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Same as 7a 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F33615-82-C-2239
8c. ADDRESS (City, State and ZIP Code) Same as 7b	10. SOURCE OF FUNDING NOS.

PROGRAM ELEMENT NO.	PROJECT NO.	TASK NO.	WORK UNIT NO.
62203F	3145	32	72

11. TITLE (Include Security Classification) Advanced Inverter Technology (U)	
12. PERSONAL AUTHOR(S) C. R. Griesbach and R. L. Moser	
13a. TYPE OF REPORT Final Report	13b. TIME COVERED FROM Oct 82 TO Oct 85
14. DATE OF REPORT (Yr., Mo., Day) 85 October	15. PAGE COUNT 174
16. SUPPLEMENTARY NOTATION	

17. COSATI CODES		
FIELD	GROUP	SUB. GR.
09	05	———
10	02	———

18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
Control Architecture, Gate Control (SCR), Converter Control, Generalized SRI Control and Converter Protection, Protection, (cont.)

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This report gives the results of all Program tasks for the Advanced Inverter Technology Program. APL has three existing series resonant inverter-based power converters.

Power	Topology
10 kW	dc/dc ½ Bridge
5 kW	ac/dc Full Bridge
200 kW	DC/DC Dual Full Bridge

The control and protection circuits are different for the three units. The purpose of this program was to produce a control and protection architecture and functional circuits that would work with all three power stage topologies. The requirements for the three existing power stages were determined. The three existing control and protection circuits were analyzed. An IC technology study was performed to determine the optimum (cont)

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT. ☐ DTIC USERS ☐	21. ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE NUMBER (Include Area Code)	22c. OFFICE SYMBOL
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DD FORM 1473, 83 APR EDITION OF 1 JAN 73 IS OBSOLETE.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

18. SUBJECT TERMS (Continued)

Power Converter
Series Resonant Inverter Control

20. ABSTRACT (Continued)

technology and fabrication method for SRI control and protection circuits. A control and protection architecture utilizing common functional circuits that would work with the three existing topologies was developed and block diagrams drawn. The functional tasks were partitioned into five custom parts. The requirements for the custom parts were described. A study was performed to assess the potential present and future functions for a microprocessor in a series resonant inverter. A packaging and thermal study was performed to investigate the problems associated with space deployment of a 200-kW series resonant inverter.

FOREWORD

This Martin Marietta Denver Aerospace Interim Report covers the work accomplished on Contract F33615-82-C-2239 for the period of October 1982 to October 1985.

This contract was being performed for the Aero Propulsion Laboratory, Air Force Wright Aeronautical Laboratories, Air Force Systems Command, Wright-Patterson AFB, Ohio. The program is under the technical direction of Rene Thibodeaux, AFWAL/POOC-1.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

LIST OF TABLES (concluded)

ACRONYMS AND ABBREVIATIONS

A	Anode
ac	Alternating Current
AFWAL/RCA	Air Force Wright Aeronautical Lab/Radio Corporation of America
AIT	Advanced Inverter Technology
ALU	Arithmetic Logic Unit
AND	Logic "and" function.
APL	Aero Propulsion Laboratory
AST DIC	Analog Signal to Discrete Time Interval Converter
BB	Breadboard
BBS	Back-Bias Sensor
CCM	Continuous Conduction Mode
CU	Control Unit
CMOS	Complimentary Metal Oxide Semiconductor
CMOS/SOS	CMOS/Silicon on Sapphire
CRM	Center for Radiation Hard Microelectronics, Sandia National Laboratories
CT	Current Transformer
CTA	Current Transformer "A"
CTB	Current Transformer "B"
CU	Control Unit
dc	Direct Current
DCM	Discontinuous Conduction Mode
DI	Dielectric Isolation
ECL	Emitter-Coupled Logic
FF	flip-flop
FPG	Firing Pulse Generator
G	Gate
GFP	Government-furnished Property
GPU	General Processing Unit
GTO	Gate-assisted Turn Off
GUA	Gate Universal Array
HCC	Housekeeping Circuit Card
IC	Integrated Circuit
IG	Gate Current
I^2L	Integrated Injection Logic
K	Cathode of SCR
kHz	Kilohertz
kW	Kilowatts
LED	Light Emitting Diode
LSI	Large-scale Integration
LSTTL	Low-power Schottky Transistor Transistor Logic

mA	Milliamp
ms	millisecond
MHz	megahertz
μs	Microsecond
MOS	Metal Oxide Semiconductor
MSI	Medium-scale Integration
mV	Millivolt
mW	Milliwatt
NMOS	Negative Metal Oxide Semiconductor
ns	Nanosecond
NTIS	National Technical Information Service
OR	Operations Requirement
OVP	Overvoltage Protection
Pa-cm	PASCAL--Centimeter
PMOS	Positive Metal Oxide Semiconductor
PU	Protection Unit
rad (Si)	Radiation Silicon
RFT	Request for Transition
RMS	Reliability Measurement System
ROM	Read Only Memory
SCR	Silicon-Controlled Rectifier
SFT	Safe for Transition
Si	System International
SIT	Software Integration Test
SOS	Silicon on Sapphire
SRFO	Sub-Resonant Frequency Operation
SRI	Series-Resonant-Inverter
SSI	Small-Scale Integration
TQ	SCR Reverse Recovery Time
TPU	Three-Phase Unit
TTL	Transistor-Transistor Logic
UPS	Uninterruptible Power Source
VCC	Voltage, Collector-Collector
Vdc	Volts Direct Current
WPAFB	Wright Patterson Air Force Base

1.0 BACKGROUND

1.1 INTRODUCTION

Several different series-resonant-inverter (SRI) based converters have been developed for the Aero Propulsion Laboratory (APL) of Wright Patterson Air Force Base (WPAFB) over the years. The control and protection circuits for these converters varied and were built of discrete components. This program was established to simplify and standardize the control and protection circuitry and to use modern integrated circuit (IC) technology to reduce the converter's size.

This final report covers the work accomplished during the period from October 1982 to October 1985.

1.2 OBJECTIVES

The primary objective of this program is to develop a standardized control and protection circuit that will work with any SRI-based converter; a hybrid implementation version of the control and protection circuitry will be produced. The secondary objective is to identify potential problem areas associated with using the existing 200-kW dual full-bridge SRI in space.

1.3 SCOPE

The scope of this program is limited to control and protection circuitry for an SRI-based converter including analysis of the operation of the control and protection circuitry for the three existing APL converters. It includes recommending approaches to reduce the size and complexity of the control and protection circuitry through IC technology. The program includes design, fabrication, and test of a breadboard and a prototype of the standard control and protection circuitry. Operation of the standard control and protection circuitry will be demonstrated with the three existing APL power stages.

1.4 PHASE I TASKS AND SUMMARY OF KEY RESULTS

1.4.1 Converter Requirements Definition

The objective of this task was to define the requirements and interfaces for the three specified APL converters. The converter requirements for the three specified APL converters have been collected in a

requirements document. The electrical inputs and outputs, as well as details of the interfaces between the controller and the three power stages, have been incorporated in this document. The primary objective of this program was to develop a set of standardized control and protection modules that can be configured to control any SRI topology. The controllers provide a voltage regulator output characteristic that operates from 10% of rated load to rated load. Input and output overvoltage protection is provided and the control and protection units operate with an output transformer or a short for testing.

1.4.2 Control and Protection Analysis

The objective of this task was to analyze the implementation and requirements for the control and protection circuits for the three existing SRI-based converters. The 5-kW ac-dc and 10-kW dc-to-dc units were government-furnished property (GFP) to Martin Marietta at Denver. Analysis and operation of these units, as well as analysis of the 200-kW dc-to-dc unit which remained at WPAFB, revealed unique requirements and previously unknown details of control and protection circuit operation. In addition, electrical schematics were prepared for the complete 10-kW unit, all the control boards of the 200-kW unit, and selected parts of the 5-kW unit. Through this a detailed understanding of the operation and performance requirements for the control and protection circuits has resulted.

Analysis of the 5-kW ac-dc unit revealed two unique requirements. Back-bias sensors (BBS) for this unit must tolerate ac voltage and not saturate. There is also a requirement for the protection unit to prevent simultaneous conduction of series SCRs during phase transition. Analysis of the 10-kW dc-to-dc unit uncovered an unreported inversion in the control integrator and an unreported use of the resonant capacitor voltage in the control and protection implementation. A detailed understanding of the operation and requirements for control and protection was acquired from analyzing and operating the 10-kW dc-to-dc unit. Analysis of the 200-kW dc-to-dc unit revealed a nonresetting integrator in the controller.

1.4.3 IC Technology Study

The objective of this study was to identify process and fabrication IC technologies for implementing the control and protection circuits. For the near term, it is practical to design for 10^5 rad (Si). Test data are available to substantiate this level of radiation tolerance and parts are available from manufacturers. If the background level is greater than this, local shielding must be used to reduce the piece-part radiation level to 10^5 rad (Si). The following recommendations are made for the control and protection circuits: (1) digital circuits should be CD40XX series CMOS (2) IC operational amplifiers and voltage comparators should be bipolar monolithic LM108s and LM111s (3) the digital design constraints of the Sandia Center for Radiation-Hardened Microelectronics (CRM) should be followed (4) hybrid circuit technology should be used for the firing pulse generator (FPG), BBS, protection unit (PU), and three-phase unit and (5) discrete circuits should be used for the control circuit.

1.4.4 Functional Design

In the functional design task, all of the required functions of the control and protection circuits were identified, duplicate functions were identified and removed, the identified functions were partitioned to logical groupings of functional circuits, all signals associated with each circuit were identified, and block diagrams of the control and protection circuits that interface with each of the three existing APL power stages were developed.

1.4.5 Custom Part Specifications

The objective of this task was to define the custom part specifications. The control and protection functions were partitioned into five areas and custom part specifications were written for the following five parts:

1) Back-bias sensor (BBS),
2) Firing pulse generator (FPG),
3) Protection unit (PU),
4) Three-phase unit (TPU), and
5) Control unit (CU).

The custom parts specifications have a narrative description of the requirements, both top-level and detail requirements, a block diagram, a circuit schematic, power requirements, and a parts list.

1.4.6 Microprocessor Study

There were two purposes for the microprocessor study. The first was to consider using a microprocessor to reconfigure the control and protection circuitry for the three existing power stages. The second was to identify tasks that could be performed by a microprocessor on future SRIs.

The study concluded that a microprocessor is not appropriate to reconfigure the controller to the three existing APL power stages because the reconfiguration can simply be performed by a three-position rotary switch. If a microprocessor were used, an uninterruptible power source (UPS) would be required, and a microprocessor malfunction could cause unknown damage to a power stage. It was also determined that a microprocessor was too slow for use as an embedded controller. The control and protection functions can be performed much faster by dedicated analog and digital circuits.

However, several candidate microprocessor functions for future SRIs were identified. These functions can be performed either by a local microprocessor in the SRI or by a central microprocessor in the electrical power subsystem. These candidate functions are:

1) Data acquisition;
2) Limit checking;
3) Self-protection;
4) Monitor key parameters;

5) Efficiency calculation;
6) State of health monitoring;
7) Peak power tracking with solar array.

1.4.7 Thermal Study

The purpose of the thermal study was to provide a first-order assessment of the magnitude of the problems associated with space deployment of the 200-kW SRI. From this study it was determined that the SCR-diode pair effectively sets the radiator temperature. The most likely radiator temperature would be constrained at about 57°C when power semiconductor junction temperatures are at 125°C maximum. To limit the SCR temperatures, heat pipes are recommended. Under ideal conditions to keep a radiator at 57°C, the radiator area would be 150 ft^2 to reject 8 kW thermal from the 200-kW SRI. This study assumed ideal conditions. For systems not under ideal conditions, the radiator area would be significantly larger.

1.4.8 Packaging Study

The general packaging problems associated with space deployment of the 200-kW SRI were addressed. The study was limited to the low-voltage power stage only; the high-voltage output transformer, rectifiers, and capacitor were excluded. The study, which assumed ideal conditions, revealed no insurmountable packaging problems with space deployment of the 200-kW SRI. The projected weight of a 200-kW converter unit (including the power electronics, thermal control, and radiator) was 339 lb for a specific weight of 1.7 lb/kW. For a system with nonideal conditions, the specific weight will be significantly higher.

1.5 PHASE II TASKS AND SUMMARY OF KEY RESULTS

1.5.1 Detailed Design

The objective of this task was preparation of detailed design drawings for circuits used in the generalized control and protection for each of the functional blocks identified in the Phase I study. Maximum use of breadboard circuits allowed design optimization of custom parts. The designs were tested over varied line input conditions, at fixed output voltage, over a 10:1 load range, and over a temperature range of -40 to +85 degrees C. Breadboard tests were completed before finalizing the designs for hybrid microcircuit fabrication.

1.5.2 Fabrication of Hybrid Microcircuit Prototypes

Designs developed under the breadboard fabrication test and evaluation task were adopted to microcircuit hybrid designs. Chip components were used to directly replace IC and discrete capacitor and semiconductor components which were used on breadboards. Resistors were replaced in the hybrids by silk-screened resistive ink, where appropriate, and with

chip components, where required. Layouts of individual hybrid circuitry were optimized for circuit performance. Packaging arrangement was based on use of existing hardware. Packaging tailored to specific application is possible by modifying existing assembly designs.

Components used in the prototype demonstration hybrids follow the recommendations outlined in the Phase I study and those described in section 1.4.3 of this report. The intent of the Phase II fabrication task is the demonstration of functioning control architecture. Commercially available components were substituted for radiation hardened and MIL screened components where practical.

1.5.3 Test Plan

Functional test procedures have been developed as a common baseline for screening various design approaches. They ensure that the selected approach meets design goals, and they provide a means of testing performance of the custom parts as individual circuit functional blocks when fabricated and throughout unit life. A functional test procedure was written for each of the three Aero Propulsion Laboratory (APL) power converters to evaluate operation as complete control units configured with breadboard functional blocks or prototype hybrid circuit functional blocks.

1.5.4 Control System Test

Two of the three APL power stages and a scale model of the 200 kW power stages were operated and functionally tested in accordance with the test procedures outlined in paragraph 1.5.3. Several conditions were monitored during tests and are as follows:

1) Line input voltage and current,
2) Resonant current waveform,
3) Control circuit logic timing,
4) Output voltage and current,
5) Component stress voltage and currents.

During evaluation of individual functional circuit blocks, design goals were compared with measured results. Circuit modifications were made to optimize circuitry to meet or exceed design criteria where possible. In testing each of the functional circuit blocks, consideration is given to operation up to 100 kHz resonant circuit frequency. For all functional blocks, the capabilities and limitations of each circuit are identified.

1.6 PHASE III TASKS AND SUMMARY OF KEY RESULTS

1.6.1 Acceptance Test Procedure

The objective of this task was the development of an acceptance test procedure for the integration and test of the standardized control system for each of the three APL SRI power converters listed in paragraph 2.1.2. A unique card cage assembly is used for each of these power

converters. Functional blocks are implemented on individual plug cards for modularity and ease of testing. Each may be moved from one card cage to another with no modifications or jumper changes.

The acceptance test procedures were written for each of the three APL power converters. Each procedure lists support requirements, special considerations, test operations, and an appendix of supporting tables and figures. Support requirements include test equipment, materials, documents, and facilities required to properly perform the tests. Special considerations are listed for cautions and warnings, definitions, list of acronyms, and other necessary information vital to properly administer the tests. Test operations are listed in logical sequence with consideration to least risk to hardware and personnel. Where applicable, prerequisites to running tests are listed. The appendix of supporting tables and figures includes diagrams showing proper connection of test equipment, hardware under test, and facilities power. Tables for acceptance testing are included along with blank tables which may be used to record data taken at subsequent tests.

1.6.2 Demonstration at AFWAL APL

Two of the APL SRI power converters were tested at Martin Marietta Denver Aerospace, the 10 kW half bridge dc-to-dc and the 5 kW three phase ac-to-dc. These two converters were retested at APL to ensure proper operation after shipment from Denver to WPAFB. The 200 kW dc-to-dc unit requires input power of 600 Vdc at 370 amps and a 200 kW load bank and was tested at APL where facilities are available to run the full power test.

2.0 PHASE I STUDY TASKS

2.1 CONVERTER REQUIREMENTS DEFINITION

2.1.1 Top-Level Requirements

The standard control and protection circuitry will perform the functions necessary to start, operate, regulate, protect, and shut down an SRI-based converter. The controller is required to work with any SRI-based converter topology, and with either ac-dc or dc-to-dc and protection circuitry will perform the functions necessary to start, operate, regulate, protect, and shut down an SRI-based converter. The controller is required to work with any SRI-based converter topology, and with either ac-dc or dc-to-dc converters. The controller will mechanize a voltage regulator function.

2.1.2 Target SRI-Based Converters

The standard controller will be designed to work with the following three existing APL SRI-based converters. By reconfiguring one controller design it will be able to operate each of the three converters.

Table 2.1-1 describes the three existing APL SRI-based converters. Simplified schematics of the power stages for these devices are shown in Figures 2.1-1 through 2.1-3 (Ref 1, 2, and 3).

Table 2.1-1 SRI Power Converter Characteristics

Type	Power	V (In)	V (Out)	Topology
ac-dc	5 kW	208 Vdc 3-Phase	20 kV dc	3-Phase ac Full Bridge
dc-to-dc	10 kW	600 Vdc Max	10 kV dc	1/2 Bridge
dc-to-dc	200 kW	600 Vdc Max	25 kV dc	Twin Full Bridge

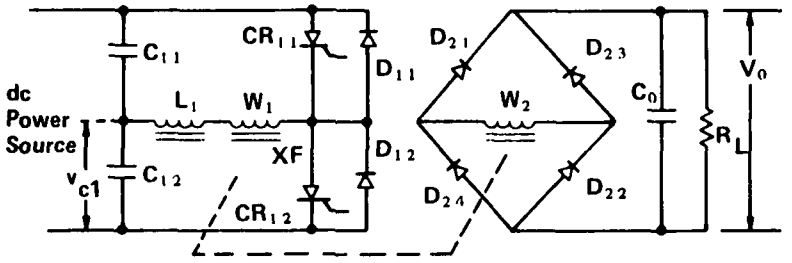


Figure 2.1-1 Half-Bridge SRI-Based Converter–10-kW dc-dc

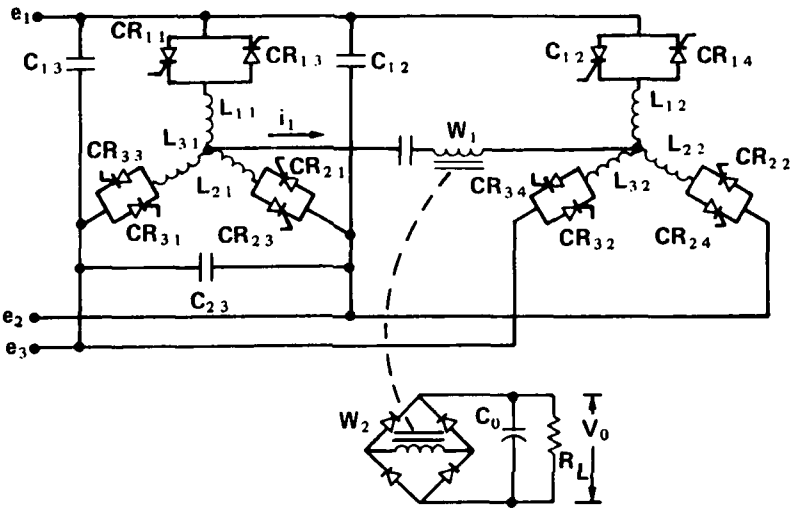


Figure 2.1-2 Three-Phase ac-dc/SRI-Based Converter–5 kW ac-dc

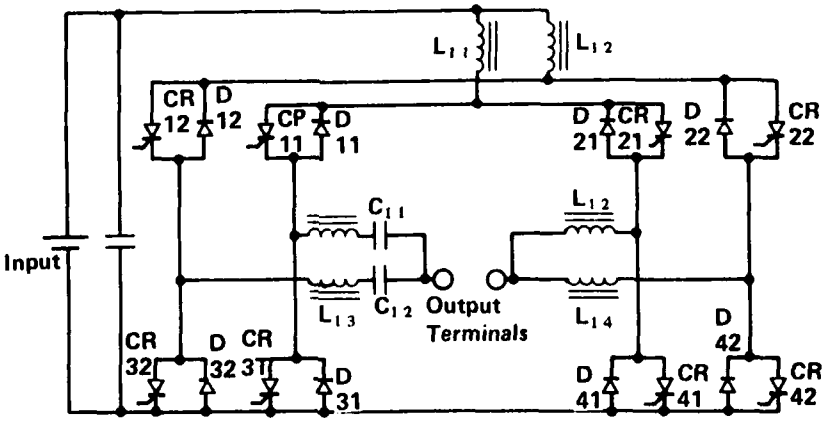


Figure 2.1-3 200-kW dc-dc, Dual, Full-Bridge SRI

2.1.3 Operating Frequencies

The internal resonant frequency of the three converters is 10 kHz. The controller was designed considering internal resonant frequencies up to 100 kHz.

The input of the 5-kW ac-dc converter is three-phase 60 Hz, sine wave. The controller was designed considering an input frequency up to 2.5 kHz.

2.1.4 Output Characteristic

The controller provides a current-limited voltage regulator output characteristic for the SRI power stage. The voltage regulator operates from 10% of full rated load to full rated load.

2.1.5 Environmental Requirements

2.1.5.1 Temperature Requirements--The control and protection circuitry was designed to work within specification in the temperature range of -40 to 85°C.

2.1.5.2 Radiation Requirements--The control and protection circuitry was designed with piece parts that will withstand 10^5 rads (Si). Local shielding will be required to ensure that the electronic piece part dose rate does not exceed 10^5. Although not required to be built with radiation-hard piece parts, the prototype control and protection circuitry was designed with piece parts that have radiationhard equivalents.

2.2 CONTROL AND PROTECTION ANALYSIS

The objectives of the control and protection analysis were to review the control and protection approaches in each of the three existing APL SRI-based converters, to determine which control and protection functions are necessary (both essential and nonduplicate), and to develop an architecture tnat can be used with all three existing topologies (half bridge dc-to-dc, full bridge ac-dc, and dual bridge dc-to-dc).

The three existing APL SRI were analyzed. Table 2.2-1 summarizes the control and protection tasks.

Table 2.2-1 Summary of Control and Protection Tasks

o Detection of SCR Reverse Bias
o Firing Pulse Generation
o Output Voltage and Current Control
o Protection from Catastrophic Failure
o Start-Up
o Phase Control (Three-Phase ac-dc Unit)

The fundamental protection problem arises from the basic topology of all three power stages: half bridge, full bridge, or twin full bridge. In any bridge configuration, two SCRs are in series across the source. If for any reason one SCR is triggered on while the other is conducting, the SCRs may be destroyed by short-circuit current from the source. The fundamental protection function is to ensure that one SCR is off before the other is triggered on. Directly related to this function is accurate sensing of the SCR state. Sensing of the SCR state involves determining whether the anode-to-cathode voltage is forward or reverse-biased. Every SCR has a reverse recovery time (TQ). After an SCR has been forward-biased and conducting, it must be reverse-biased for a time not less than TQ before it recovers its ability to block forward voltage. The protection function, then, includes sensing the SCR reverse bias and inhibiting SCR triggering until the TQ requirement has been met.

A specific control function is associated with generation of the firing pulse to trigger the SCRs on. Specific functions are also associated with controlling the output voltage and current. These include a fast loop for cycle-by-cycle control of the current and a slower loop for voltage control.

Specific functions are also required to start the SRI. The protection circuitry required to ensure two series SCRs are never fired at the same time complicates the task of the start-up circuitry. The start-up function includes using the polarity of the resonant capacitor voltage to determine which SCR to fire first. Because of unbalanced leakage in the SCRs, the initial resonant capacitor voltage can be of either polarity. The initial SCR fired will be chosen so the resonant capacitor voltage adds to the source voltage. In addition, the start-up circuitry overrides the protection circuitry for one cycle to allow the power stage to start. The start-up circuitry also provides a clock signal to initialize the three-phase control unit.

The three-phase control unit requires additional functions to determine when an input phase transition has taken place, to determine when the proper back-bias signals have been received based on the phase pair, and to give SCR fire commands based on the phase pair. The three-phase unit must generate SCR fire commands for two discrete modes: first, when the SCR functions as an SCR, and second, when the SCR functions as a diode.

2.2.1 Previous Approaches

Analysis of the three existing SRI control circuits revealed the following approaches were used to implement control and protection.

It was found that distributed rather than centralized logic was used which resulted in more complicated interfaces between functional circuits. Representative areas in which distributed logic functions were found are:

1) The 10-kW dc-to-dc BBS hold-off circuit,

2) The three-phase configuration BBS antisaturation circuit,

3) The 200-kW dc-to-dc configuration firing pulse generator inhibit circuit.

It was found that functions had been duplicated. In the 10 kW dc-to-dc configuration, there were double-sided start circuits, multiple "FIRE" prevention circuits to inhibit toggle action, and duplicate means of preventing overvoltage.

It was also found that there were multiple circuit designs to perform the same functional task in different topologies. There were also different circuit designs for the firing pulse generator for the 5 kW ac-dc and 200 kW dc-to-dc configurations.

It was also found that discrete logic had been used rather than integrated circuit logic.

2.2.2 Criteria for Partitioning of Functional Tasks

The object of the partitioning task was to simplify the architecture, produce simple, logical interfaces, remove duplicated functions, and ensure that general-purpose functions are defined that can be used in all configurations (except functions that are unique to the ac-dc unit).

2.2.3 New Architecture and Functional Units

The new architectural approach is based on:

1) Centralized logic;
2) Functions identified as necessary and nonduplicate;
3) Circuits capable of performing their functions in all topologies;
4) Use of IC technology.

Using the partitioning criteria, the control and protection tasks have been grouped into the five functional circuits:

1) Back-bias sensor;
2) Firing pulse generator;
3) Protection unit (includes start-up function);
4) Three-phase unit;
5) Control unit.

2.2.4 Results of Existing SRI-Based Converter Evaluations

Table 2.2-2 summarizes the results of the 10-kW converter evaluation. Two items in the converter design were found that had not been pointed out in the open literature. First was an inversion in the controller integrator and second was the use of the resonant capacitor voltage as an input to the protection circuit. These discoveries aided in a detailed understanding of the 10-kW unit operation that could be extended directly to the 5-kW and 200-kW units.

Table 2.2-2 Results of 10-kW Converter Evaluation

Observation	Significance
Inversion in Controller Integrator	This inversion not shown in open literature; addition to practical knowledge.
Use of Resonant Capacitor Voltage Protection Circuit	Never shown in open literature; additional knowledge.
Detailed Understanding of 10 kW Unit	Understanding directly applicable to 5-kW and 200-kW units.

Table 2.2-3 summarizes the results of the evaluation of the 5-kW ac-dc and 200 kW dc-to-dc units.

Table 2.2-3 Results of 5-kW and 200-kW Evaluations

5 kW ac-dc
- Established unique Requirements for 3-Phase Back-Bias Sensor
- Prepared Electrical Drawings for Selected Cards
- Developed Selected Back Plane Wiring Information
200 kW dc-dc
- Determined that controller Uses an Apparent Nonresetting Integrator
- Developed Electrical Schematics for All Cards

2.3 IC TECHNOLOGY STUDY

The purpose of this study was to identify IC process and fabrication technologies for the control and protection circuits. Although the goal was to identify technologies that were compatible with wide use and high production rates, only prototype quantities will be produced for this contract.

Another general study guideline was to consider the possibility and difficulty of radiation-hardening the chosen process technology. Although there was no requirement for the prototypes to be radiation hard, the ability to implement the prototype designs in a radiation-hard technology was considered.

The IC technology study consisted of a survey of process technology (bipolar or MOS), a survey of fabrication technology (custom ICs, commercially available ICs, gate arrays, and hybrids), a discussion of the options for each functional circuit, and recommendations for the process and fabrication technology for each of the functional circuits.

2.3.1 Process Technology--Digital

For digital circuits, the IC process technology can be divided into two categories, bipolar and MOS, with the subdivisions as in Table 2.3-1.

The most common bipolar processes are Transistor-Transistor Logic (TTL), including TTL-LS (low-power Schottky), and ECL. Emitter Coupled Logic (ECL) is a superfast technology and has excellent radiation resistance. On the negative side it consumes high power, requires multiple bias voltages, and has limited family availability. Its very high speed also requires special care in layout and interconnection design. A prominent use for ECL has been in such large mainframe computers as the CRAY series of supercomputers. The AIT series resonant inverters operating up to 100 kHz will not require the speed that ECL provides, such as toggle frequencies in the hundreds of MHz region. ECL is not considered a candidate for AIT. TTL has been the leader in small and medium-scale integration (SSI and MSI) although in recent years it has fallen behind in the trend toward large-scale integration (LSI) because of thermal limitations in high-density microcircuits. TTL-LS represents an improvement in bipolar technology to make it more competitive with the MOS technologies. It has much lower power dissipation than TTL while maintaining relatively good speed and radiation resistance.

Table 2.3-1 Comparison of Integrated Circuit Processes

Integrated Circuit Process	Power Consumption	Speed	Family Availability	Radiation Hardness
Bipolar				
- TTL	Poor	Very Good	Excellent	Very Good
- TTL-LS	Good	Good	Good	Good
- ECL	Very Poor	Excellent	Poor	Excellent
- I^2	Programmable	Programmable	Poor	Good
MOS				
- NMOS	Poor	Excellent	Poor	
- PMOS	Good	Poor	Good	
- CMOS	Very Good	Good		
- CMOS/SOS	Very Good	Good	Poor	Very Good
- CMOS/BULK	Very Good	Poor	Poor	Very Good

The TTL processes yield 5-V parts. The noise margin for 5-V TTL is approximately 0.4 V or 8% of VCC. Conservative design practice prefers noise margins larger than the 0.4 V available from 5-V TTL.

I^2L is still expensive and lacks sufficient industry interest (sources of supply) to be considered a strong candidate for the AIT program. Another criticism that has been leveled at I^2L is a lack of standardization as there are large variations from manufacturer to manufacturer.

The generic MOS processes are NMOS, PMOS, and CMOS. NMOS is currently the most popular MOS process although it has a narrow range of operating temperatures, poor radiation resistance, and requires high power. Many sources of supply and a great variety of device types have combined to force its cost to the lowest levels. NMOS is used in many of the microprocessors for such personal computers as the 6502 microprocessor in the Apple 2 Plus.

PMOS has lower power dissipation and better radiation resistance than NMOS but few sources of supply and limited device selection. Its development has been stifled by the development of CMOS.

CMOS represents a near-perfect process technology in many ways. Its quiescent power dissipation is near zero, and its dynamic dissipation increases primarily because of parasitic capacitance loading. Noise immunity is very high (30 percent of supply voltage for both high and low states) and switching noise generation very low relative to TTL and ECL. A particular advantage of CMOS for the AIT program is that it can combine both analog and digital functions. Digitally controlled analog transmission gates are available that can operate with input and output voltages between zero and a full power supply voltage level. These gates are highly useful in systems where analog multiplexing and ac-to-dc conversion functions are required.

An advantage of CMOS is that it is available in a variety of operating voltages, up to 15 V. By going to 15-V CMOS, a noise immunity of up to 5 V can be obtained. This is 12.5 times the noise immunity of 5-V TTL.

Any process technology selected for AIT should be compatible with space application. This means radiation resistance. The Space Division has established near-term goals for microelectronics radiation tolerance for five-year missions of $5x10^4$ rad (Si) minimum in general and $1x10^5$ rad (Si) for enhanced survivability missions. The long-term goal is 1x10 rad (Si). Unhardened CMOS is good to about 10^4 rad (Si). To overcome this limitation, serious development activities are underway in two areas--CMOS/SOS and CMOS/Bulk. Referring to the substrate, SOS indicates silicon-on-sapphire and Bulk indicates silicon substrate base material. The physics of the Bulk technology are well understood and its capabilities and producibility have been demonstrated by the CRM. Although material problems have plagued CMOS/SOS, it continues to receive heavy emphasis.

Sandia's Bulk technology process has been used to fabricate radiation-tolerant parts since the middle 1970s, first with a metal gate process and subsequently with self-aligned polysilicon gates. They have consistently demonstrated total dose tolerance in the 10^5 rad (Si) to 10^6 rad (Si) range. They have also demonstrated upset levels greater than 10^8 rad/S. They have fabricated tens of thousands of these hardened parts that have also functioned over the full range of normally specified environments. Many of the parts were subjected to full Class S screening and quality assurance procedures.

Appendix A gives further information about radiation-hard microprocessor chip sets.

2.3.2 Process Technology--Linear

The basic process technology for linear ICs is bipolar monolithic. Two sources were used to gather information about radiation-hard linear ICs--first the CRM at Sandia National Laboratories, and second, the Parts Technology group at Martin Marietta Denver Aerospace.

At the time of this survey, CRM did not have any radiation-hard linear circuits in production (operational amplifiers or comparators). CRM anticipates some operational amplifiers in production within two years, but they have no comparators scheduled (Ref 4). Therefore CRM is not a source of radiation-hard linear circuits for the prototype phase of the AIT program.

The Parts Technology group at Martin Marietta is responsible for selecting parts for the radiation-hard circuits to be produced in the near term. They have surveyed commercial manufacturers and compiled a list of linear IC, digital IC, transistor, and passive component producers who have published data demonstrating radiation hardness. It was concluded that fabrication of radiation-hard electronics using commercially available components in the near term will require the following guidelines. Electronic piece parts that can be produced in the near term are considered acceptable for use with appropriate derating at 10^5 rad (Si) total dose. If the background dose is higher than this level, local shielding should be used to reduce the total dose at the piece part of 10^5 rad (Si).

Table 2.3-2 summarizes linear piece parts demonstrating acceptable radiation hardness to 10^5 rad (Si).

Table 2.3-2 Linear ICs with Demonstrated Radiation Hardness to 10^5 rad (Si)

Generic P/N	Manufacturer	MIL-M-38510	Description	Hardness Status
LM101A	NSC	10103	Op amp	Acceptable
LM103	NSC	None	Ref Diode	Acceptable
LM105	AMD	None	Adj Volt Reg	Acceptable
LM108A	AMD	10104	Op Amp	Acceptable
LM111A	AMD	10304	Comparator	Acceptable
LM113	NSC	None	Ref Diode	Acceptable
LM124	AMD	11005	Quad Op Amp	Acceptable
OP-15	PMI	None	Bi Fet Op Amp	Acceptable
Ref-02	PMI	None	+5 Volt Reg	Acceptable

Discrete bipolar transistors are subject to beta degradation and saturation caused by ionizing radiation. The radiation can cause an increase in photocurrents that appear as an increase in collector-to-base leakage, causing the transistor to saturate. Low-frequency bipolar transistors are more radiation-sensitive than high-frequency transistors. Therefore, a suggested radiation hardening guideline is to choose transistors with as high a cutoff frequency as possible.

2.3.3 SCR Radiation Discussion

An SCR is a four-layer bistable switch that depends on a p-n-p-n structure for regenerative feedback. When the SCR loop gain is less than 1, it is off. When its loop gain is made greater than 1, it is switched on. It is normally turned on by injecting current into the gate. The photocurrents caused by ionizing radiation can produce an apparent gate current increase. If the photocurrents induce gate current exceeding the turn-on threshold, the SCR will be turned on by radiation. A general rule is that the dose rate required to turn a SCR on is proportional to the gate current required to turn on the SCR. The higher the gate current required to turn on the SCR, the higher the dose rate threshold for turn-on. At the present time, radiation-tolerant flight-type SCRs have not been identified.

2.3.4 Fabrication Technology

Table 2.3-3 summarizes the candidate fabrication technologies. The most desirable technology for the control and protection circuits is custom IC. Custom IC will yield the lowest unit cost per circuit and will hasten the wide acceptance and use of the SRI. The fabrication technology characteristics show that they differ in initial cost, development time, time to produce the first prototype, and lot size for economic production. Custom ICs have the highest initial cost, longest development time and the highest lot size for economic production, but the lowest unit cost. Custom ICs may require from $0.1M to $1.0M for initial cost and require up to a year for delivery of prototypes.

Table 2.3-3 Candidate Fabrication Technologies Compared

Candidate	Initial Cost	Development Time	Reliability	3-Phase Controller	All Other Control Circuits
Custom IC	Highest	Highest	Highest	Yes	Yes
Gate Array	Lower	Lower	High	Yes	No
Hybrid	Lower	Lower	Lower Than Gate Array	Yes	Yes
Discrete	Lowest	Lowest	High	Yes	Yes

A candidate technology for the three-phase controller is a gate array because the three-phase controller is primarily digital. Gate arrays are not a candidate for any other AIT control circuit. Commercial gate arrays from silicon foundries have been estimated to have an 8- to 12-week turnaround time (from design input to delivery of prototype chips) with a cost of $10k to $30k.

The fabrication technology compatible with the low-production scenario for the prototypes in this contract is hybrid circuits. Hybrid circuit technology is a candidate fabrication technology for all control and protection circuits.

A hybrid circuit fabrication of the three-phase controller is compatible with radiation hardening. The prototype will be built with commercial 4000-series CMOS chips that are not radiation-hard but do have radiation-hard equivalents to 10^6 rad (Si). The three-phase controller can be made radiation-hard by substituting the radiation-hard chips from RCA for the commercial 4000-series chips. The linear ICs from Table 2.3-2 that have radiation-hard equivalents will be used for prototype fabrication.

2.3.5 Options

Table 2.3-4 summarizes the options for the three-phase unit. There are no theoretical problems with implementing the three-phase controller by a commercial CMOS gate array. The controller will require approximately 100 gates, which is pedestrian. Mask-programmable gate arrays are capable of speeds up to 10 MHz. A maximum frequency of 2.5 kHz for the three-phase unit and a maximum of 0.1 MHz for the resonant frequency is required. The most practical option for the three-phase unit is considered to be hybrid circuit technology because of the availability of radiation hard 4000-series CMOS.

Table 2.3-4 Three-Phase Controller Options

Option	Can Design Be Built with Radiation-Hard Parts?	Comment
1) Use Gate Array from Conklin Chip Set	Yes	Not practical; hardened gate array not in production at Sandia.
2) Commercial CMOS Gate Array from a Silicon Foundry	Qualified Yes	By using CRM radiation-hard design constraints and only cells available from CRM Library, there would be minimum effort to fabricate in GUA array at CRM.
3) Hybrid Circuit	Yes	Prototype with 4000-series CMOS; substitute radiation-hard 4000-series CMOS for later builds; no additional design required for radiation hardening.

Table 2.3-5 summarizes the options for the FPG, BBS, control unit, and protection unit. Commercial linear arrays are not considered strong candidates because of the lack of radiation-hardened versions of the linear arrays. There are only digital gate arrays, no linear arrays, in the Conklin chip set that is being radiation hardened by CRM. Hybrid circuits are the most practical option for the prototype fabrication.

Table 2.3-5 Options for FPG, BBS, Control Unit, and Protection Unit

Option	Can Design Be Built with Radiation-Hard Parts?	Comment
1) Commercial Linear Array	No	Theoretically a possibility, but the number of linear arrays is very small compared to digital gate arrays.
2) Hybrids	Yes	Hybrid fabrication most practical for the prototype production quantities envisioned; suggest design be done using LM108 and LM111 parts that have radiation-hardened equivalents.

2.3.6 Recommendations

The recommendations for the fabrication and IC technologies for the circuits are summarized in Table 2.3-6. Hybrid circuits are recommended for the firing pulse generator, back-bias sensor, protection unit, and the three-phase unit. Discrete ICs are recommended for the control unit because the many external components required to customize the control circuit to the particular SRI negate any advantage in hybridizing the control circuit at this time. For digital circuits, RCA 4000-series commercial CMOS is recommended for the prototypes. Radiation-hard equivalents of the 4000-series CMOS can be used for later builds to produce radiation-hard circuits. We recommend the prototypes be built with commercial equivalents of the demonstrated radiation-hard linear circuits from Table 2.3-2.

Table 2.3-6 IC Technology and Fabrication Recommendations

Unit	Fabrication Technology	IC Technology
Three-Phase	Hybrid	RCA 4000-series CMSOS for prototype; substitute radiation-hardened RCA 4000-series for flight.
FPG, BBS, Protection	Hybrid	Monolithic bipolar, LM108 and LM111 for linear, digital same as three-phase.
Control	Discrete	Monolithic, LM108, LM111, and OP-15.

2.4 FUNCTIONAL DESIGN

2.4.1 Objectives

The objectives of the functional design task were to:

1) Identify the functional elements;
2) Generate system block diagrams for each of the three existing APL SRI topologies;
3) Generate functional requirements for each functional block;
4) Perform a functional design for each functional block to the block diagram and schematic level.

This section describes the system-level block diagrams. Conceptual design of the functional blocks will be discussed in Section 2.5 (custom part specifications).

2.4.2 Partitioning

The control and protection functions were partitioned into the following five areas:

1) Back-bias sensor;
2) Firing pulse generator;
3) Protection unit;
4) Three-phase unit;
5) Control unit;

2.4.3 10-kW dc/dc Block Diagram

Figure 2.4-1 is a block diagram of the control and protection circuit configuration for the 10-kW dc-to-dc converter. The features of the

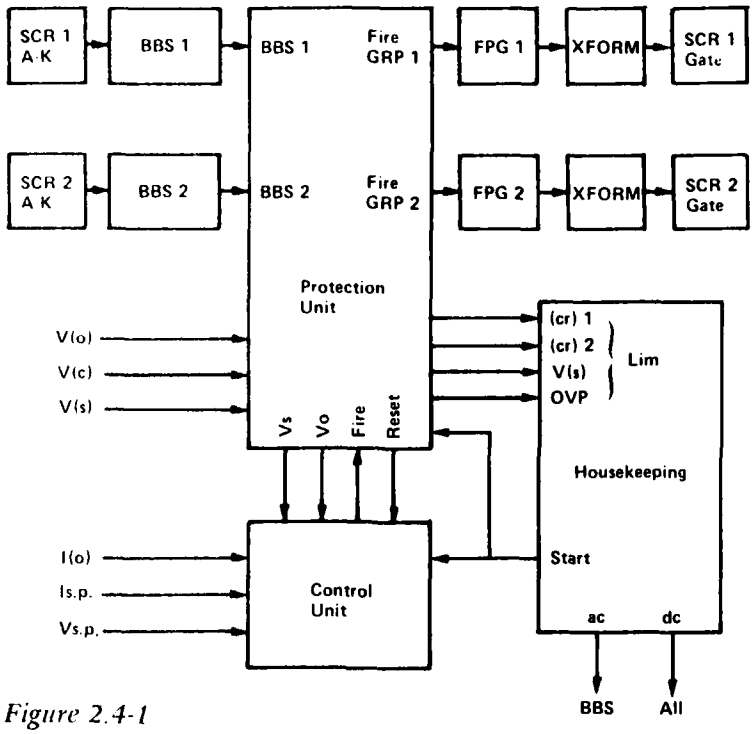


Figure 2.4-1

10-kW dc-dc Simplified Functional Block Diagram

power stage are that it is a half bridge with two SCRs, two BBSs, and two FPGs. There is one control unit, one protection unit, and one housekeeping power supply. The start function is shown as a separate block to highlight it, but it is functionally incorporated in the protection unit. The housekeeping supply includes a debounce circuit for the logic start signal configurations. The feedback parameters used for control are the resonant current and the output voltage.

2.4.4 5-kW ac-dc Block Diagram

Figure 2.4-2 is a block diagram of the control and protection circuit configuration for the 5 kW ac-dc converter. The significant features of the 5-kW ac-dc configuration are that each of the 12 SCRs functions as an SCR 1/3 of the time, a diode 1/3 of the time, and is inactive 1/3 of the time. There are six phase pairs within 360 electrical degrees. The phase pairs must be sensed, and while the system is operating within a phase pair, the system equivalent circuit is that of a full-bridge SRI-based converter.

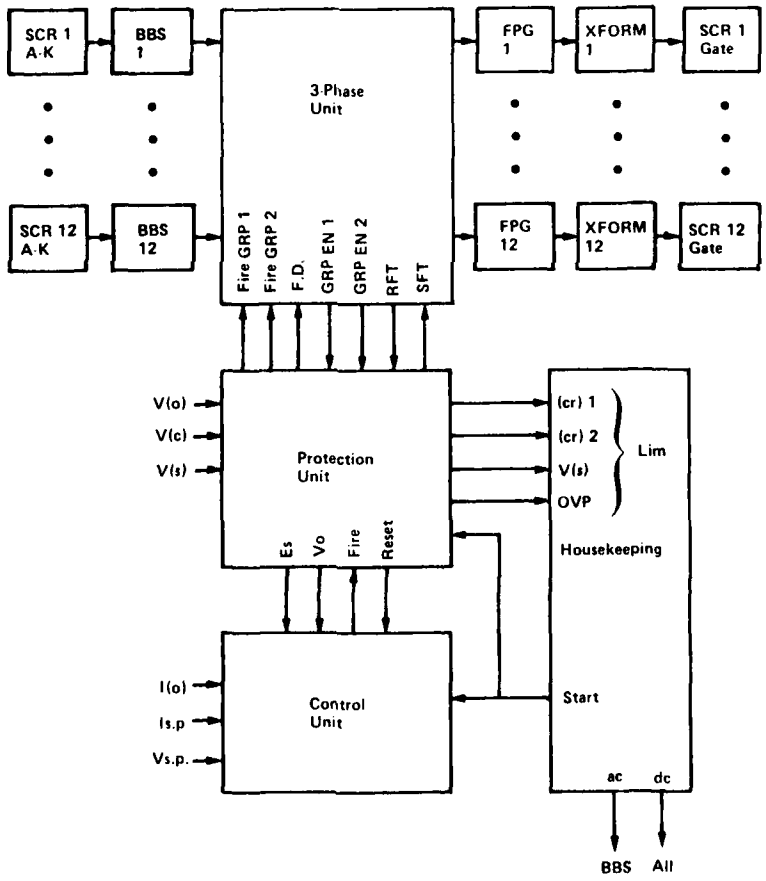


Figure 2.4-2
5kW Three Phase ac-dc Simplified Functional Block Diagram

The control and protection circuit includes 12 BBSs and 12 FPGs, one for each of the 12 SCRs. The three neutral to phase voltages are inputs to the three-phase unit where they are used to determine the instantaneous operational phase pair. The RFT signal is generated in the three-phase unit and sent to the protection unit. When the protection unit determines it is safe to go from one phase pair to another, it responds by sending a SFT signal to the three-phase unit. The feedback parameters used for control are the resonant current and output voltage.

2.4.5 200 kW dc/dc Block Diagram

Figure 2.4-3 is a block diagram of the control and protection circuit configuration for the 200-kW dc-dc converter. The significant features of the power stage topology are that there are twin full bridges, eight SCRs, and each SCR is provided with an antiparallel diode. The SCRs function as SCRs only. They do not have to function as diodes as in the three-phase configuration. Each SCR is used, at most, 50% of the time.

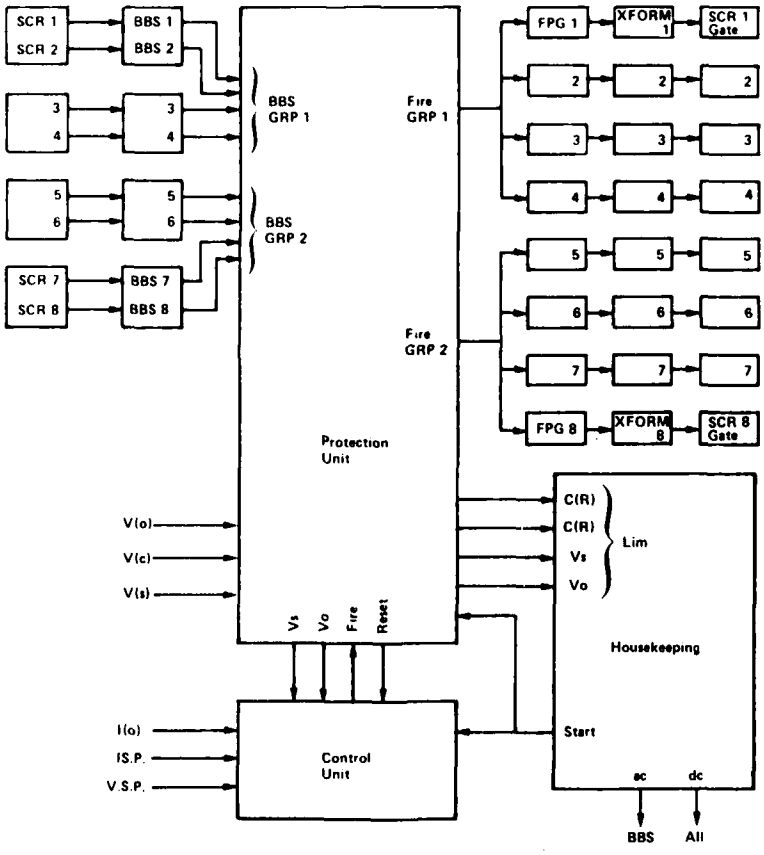


Figure 2.4-3 200 kW dc-dc Simplified Functional Block Diagram

Significant features of the control and protection circuit are the eight BBSs and eight FPGs. Because there are two full bridges for one direction of resonant current two SCRs must be fired for each bridge, or a total of four for the two bridges. The four SCRs associated with the same direction of resonant current are fired from the same protection unit signal. The firing pulse generators are all referenced to

signal ground. The SCR gate and cathode circuit are isolated from signal ground with a transformer. The resonant current and the output voltage are the feedback variables for control.

2.5 CUSTOM PART SPECIFICATIONS

There are five functional elements: (a) firing pulse generator, (b) back-bias sensor, (c) protection unit (d) three-phase unit, and (e) control unit. The detail requirements are described in the following subsections.

Four of the five functional circuits have been implemented as hybrid custom parts. The control function is implemented using small scale integrated circuits to facilitate circuit modifications. A unique control function is not optimal for all power converter applications.

2.5.1 Firing Pulse Generator

2.5.1.1 Background--The three SRI power stages all use SCRs as the power-switching device. The fundamental interface requirements for an SCR gate circuit are the open-circuit voltage, the equivalent series resistance, and the pulse width. A survey of modern large SCRs revealed that they all have approximately the same gate turn-on requirements. The modern SCRs all have amplifying gates. The gate current at turn-on is specified as 150 mA and the voltage as 3 V. Turn-on times are typically 3.5 microseconds maximum. Figure 2.5.1-1 shows typical SCR turn-on delay time as a function of gate current. The figure shows that a gate current of 0.5 amp produces a delay time of 1 microsecond. Gate currents larger than 0.5 amp provide only marginal reductions in the delay time. The rise time of the current should be less than one microsecond.

Another factor that influences the required open-circuit voltage for the SCR gate drive circuit is the time rate of change of current (di/dt) that must be supported while the SCR is turning on. If the maximum specified di/dt is called for, an open-circuit voltage of up to 15 V can be required (Ref 5). From an analysis of existing SRI converters it is apparent that they have been designed for a low di/dt during SCR turn-on. For example, the 200-kW dc-dc unit has a maximum di/dt of 6 amps per microsecond. This is much less than the 100-amp per microsecond the SCR is rated for. When the circuit of the 200-kW FPG was analyzed, we found that the open-circuit voltage was 6 V. In the 200-kW FPG, there was no intentional series resistance. Only the parasitic resistance in the circuit was used to limit the gate current.

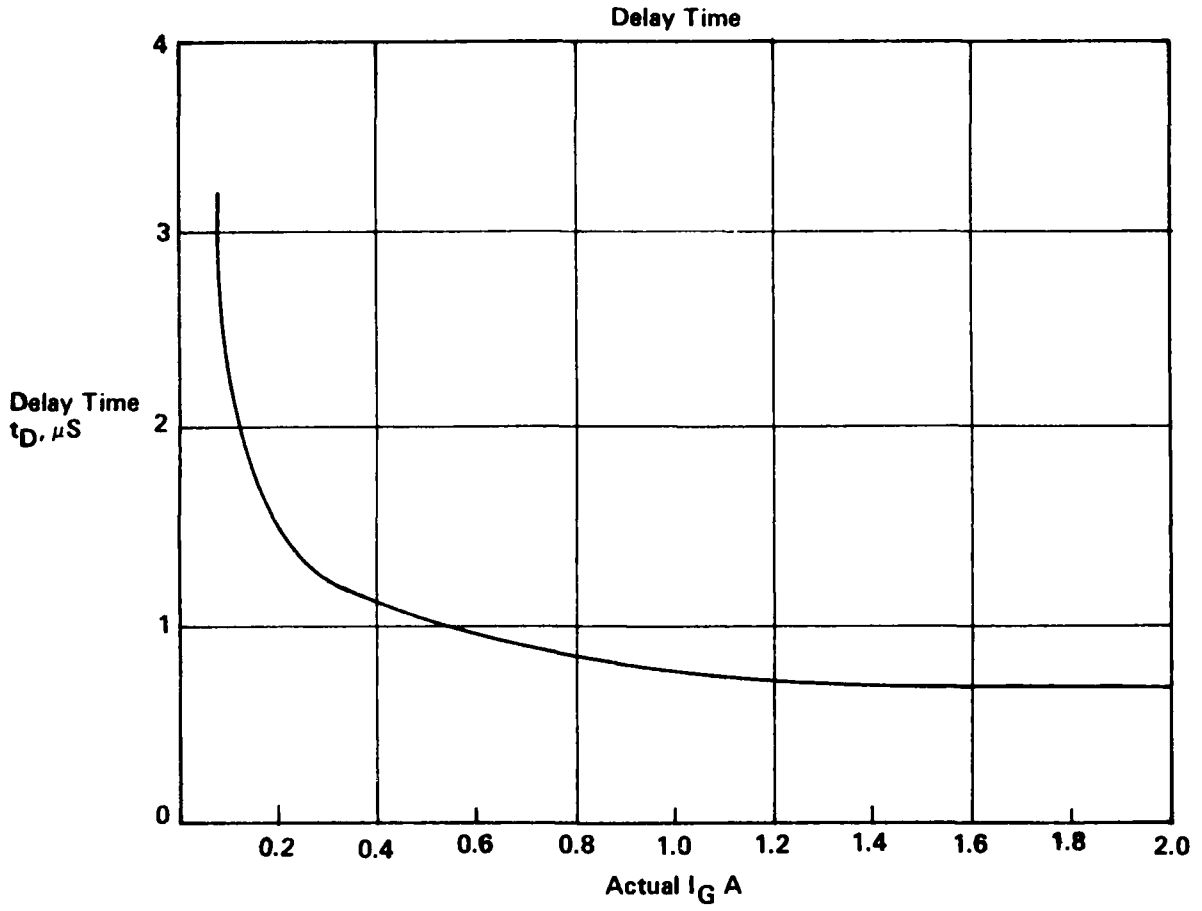


Figure 2.5.1-1 Typical SCR Turn-On Characteristics

Figure 2.5.1-2 shows an idealized representation of the FPG current waveform. There are six adjustable parameters: four current levels (IP1, IP2, Idc1 and Idc2), and two pulsewidths (TP1 and TP2).

A discussion of the FPG characteristics for the power switch drive combinations shown in Figure 2.5.1-3 follows. The SCR direct drive requires a current pulse from the FPG for SCR turn-on but no sustaining current to hold the SCR on. A gate-assisted turn-off (GTO) SCR will require a current pulse for minimum turnoff time. For driving a bipolar transistor with proportional drive, the FPG must supply both turn-on and turn-off pulses. The proportional feedback will supply the base current to hold the bipolar transistor on. Because bipolar direct drive requires the FPG to supply all of the base current while the transistor is conducting, it is not practical for large SRI-based converters.

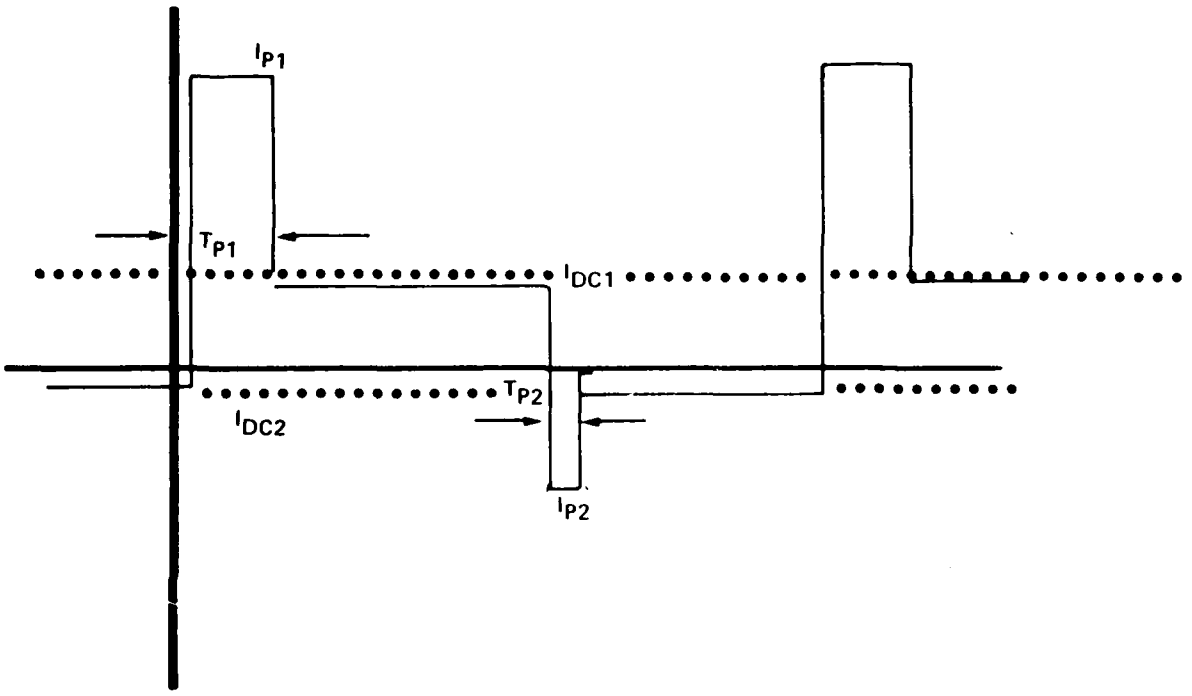


Figure 2.5.1-2 FPG Current Waveforms

A MOSFET requires only gate voltage for continuous conduction. The FPG must supply an initial turn-on current pulse to charge the gate capacitance and a sustaining current to maintain voltage on the gate clamp. For turn-off the FPG must supply a negative current pulse to discharge the gate capacitance and a sustaining current to maintain the reverse voltage clamp.

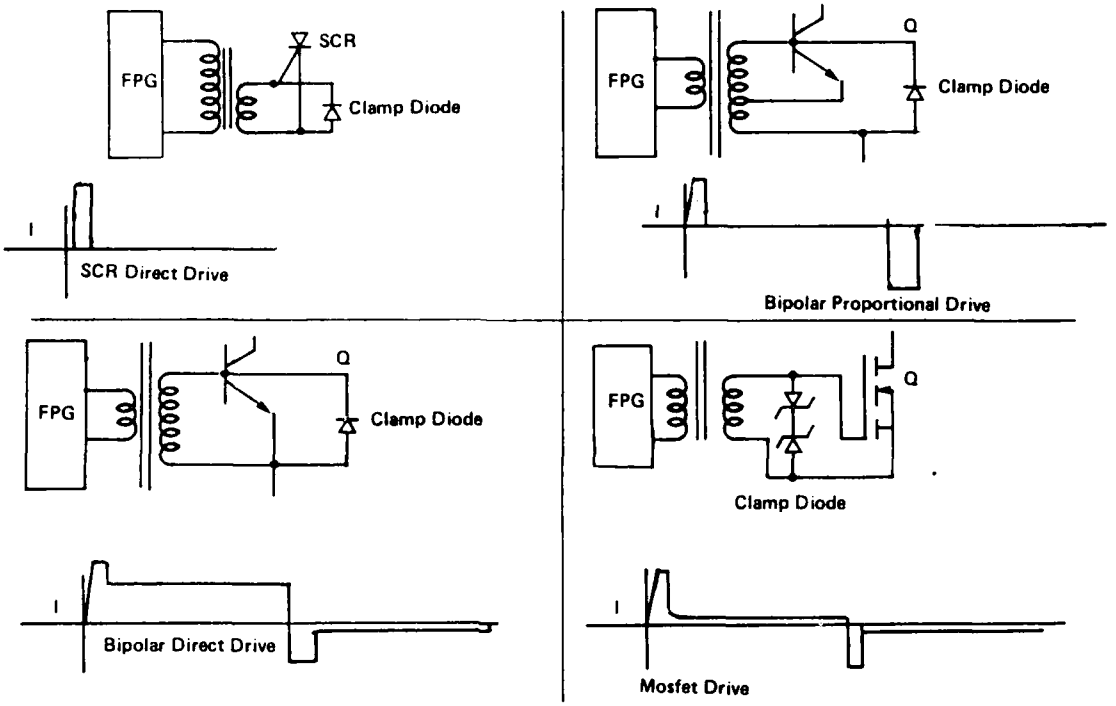


Figure 2.5.1-3 Possible Drive Combinations

An investigation was made to determine the compatibility of requirements for the SCR drive and bipolar transistor drive. From tests of the 5-kW ac-dc and 10-kW dc-dc breadboards, it was found that actual firing pulse generator requirements could be met by an open-circuit voltage of 9 V, a peak current of 1.5 amps, and a pulsewidth of 4 microseconds. In Ref 6, Robson and Hancock described the development of base drives for SRI using the bipolar transistors D60T and D70T. In their paper, they list the following as turn-on pulse requirements for proportional drive.

Transistors	Pulse Amplitude, A	Pulse Width, ms
D60T	12	15
D70T	30	10

From these considerations, it does not appear a single firing pulse generator could be optimum for both an SCR and a bipolar proportional drive. A circuit that is designed for a 1.5-amp SCR pulse will be too small for the bipolar drive. If the firing pulse generator is designed to supply either 12- or 30-amp pulses for bipolar drive, the circuit will be greatly overdesigned if used with an SCR. During the detailed design phase, attempts were made to reconcile the conflicting requirements of an SCR and bipolar transistor proportional drive for a single drive circuit.

2.5.1.2 Requirements--As a minimum, the firing pulse generator must function with the three existing SCR power stages. The firing pulse generator must have the following characteristics:

1) Open-circuit voltage--15 V,

2) Peak current--2 amps,

3) Pulsewidth--To 10 microseconds where these parameters can be made smaller by changing circuit components.

This set of requirements will allow the same SCR gate firing circuit to meet the requirements for the three existing APL converters and also provide lower gate voltages and currents for minimum gate circuit dissipation and maximum efficiency.

2.5.1.3 Block Diagram--Figure 2.5.1-4 is a block diagram of the SCR FPG with transformer isolation. The transformer provides isolation between signal ground and the SCR gate and cathode.

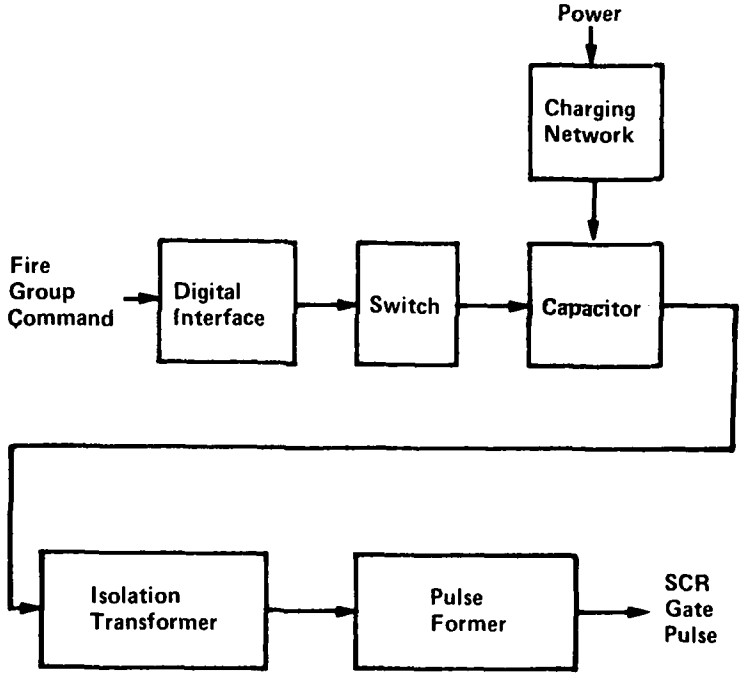


Figure 2.5.1-4 FPG Block Diagram

2.5.1.4 Circuit Diagram--Figure 2.5.1-5 shows a circuit diagram for the capacitor discharge FPG. The components inside the dashed lines are those to be incorporated in a hybrid circuit. The switch is composed of Q1, Q2, and Q3. Energy storage capacitor C1 is charged through R2, and T1 is the isolation transformer. The pulse characteristics can be controlled by varying C1, the turns ratio of T1, or by varying R3.

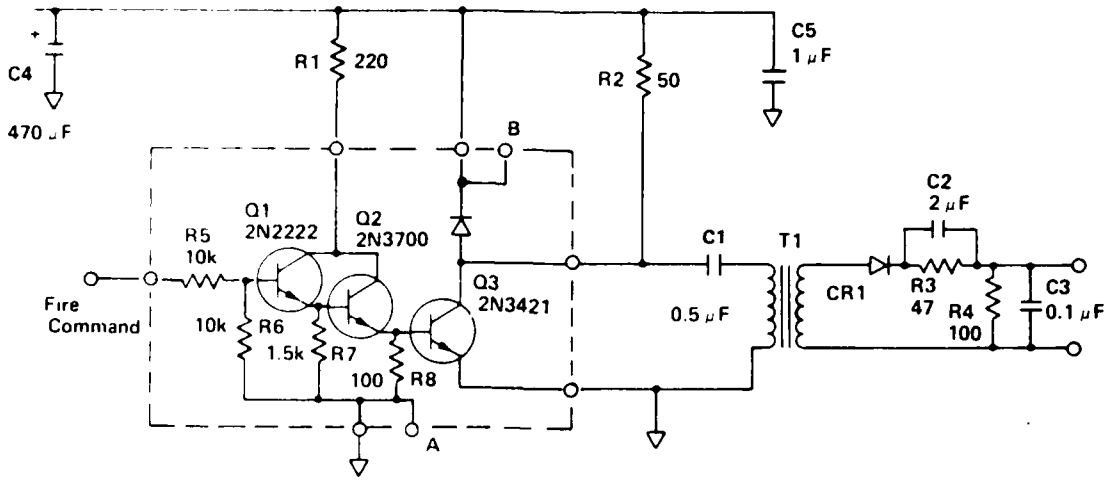


Figure 2.5.1-5 FPG Schematic

2.5.1.5 Power--The FPG shall be provided with 15 V, ±10%. The fire command to the FPG shall be a positive true signal from the 15-V CMOS.

2.5.1.6 Parts List--The parts list is summarized in Table 2.5.1-1.

Table 2.5.1-1 FPG Parts List

Reference Designator	Description	PN
Q3	NPN Transistor	2N3421
Q2	NPN Transistor	2N3700
Q1	NPN Transistor	2N2222
T1	Core	846T250-3C8

2.5.2 Back-Bias Sensor

2.5.2.1 Background--In all of the topologies for the three SRI-based inverters, there is an SCR with an antiparallel diode to provide soft commutation of the SCR. There is only one diode drop of reverse voltage across the SCR when the SCR is to turn off. The fundamental BBS problem is to sense one diode drop in the 600-V common mode and have the BBS survive the 600-V common mode.

A characteristic of all SCRs is that after the SCR is forward-biased, it must remain reverse-biased for a time equal to the reverse recovery time (TQ) before it can block forward voltage. Therefore to ensure the SCR will be recovered and able to block forward voltage, it is necessary to sense when the SCR is reverse-biased, then wait TQ seconds before triggering the opposing SCR that would forward-bias the off SCR. The BBS sensor will sense SCR back-bias. The delay to assure SCR recovery will be provided in the protection unit.

2.5.2.2 Requirements--Table 2.5.2-1 summarizes the derived requirements for the back-bias sensor. A single design will be capable of sensing either positive or negative voltage with respect to BBS common. Each BBS will have an isolated power supply. The BBS must be able to sense one diode drop reverse voltage on one-half cycle and not be damaged by up to 600-V forward voltage on the next half-cycle.

Table 2.5.2-1 Back-Bias Sensor Requirements

- Back-Bias Voltage, -0.1 to -1.0 V
- Differential Mode Voltage of 600 V Square Wave across the Inputs
- Output Compatible with CMOS Logic Family
- Maximum Signal Delay to be Kept under 1 microsecond
- A Single Design Capable of Sensing Positive or Negative Reverse Bias Voltage with Respect to BBS Common
- Isolated Power Supply

The logic output of the BBS as a function of the SCR anode-to-cathode voltage is tabulated.

SCR Anode to Cathode Voltage	Logic Output of BBS
+ (Forward-Biased)	0
- (Reverse-Biased)	1

2.5.2.3 Block Diagram--Figure 2.5.2-1 shows a block diagram of the BBS. The significant features are that the comparator and associated components are in a hybrid; a square wave oscillator and transformer are used to supply isolated power to the two comparators, an optocoupler is used for signal isolation, and a level translator circuit interfaces the 5V optocoupler with the 15V CMOS. The isolation transformer, optoisolator, and level translator will be external to the hybrid. The optoisolator is not compatible with hybrid design because it must withstand 600-V and hybrid packages are only normally good for 50V from pin to pin. Also of significance is that the returns of the two BBSs are fully isolated because in the 200-kW unit SCRs that have anodes electrically connected have separate anode sense leads brought out for the BBS.

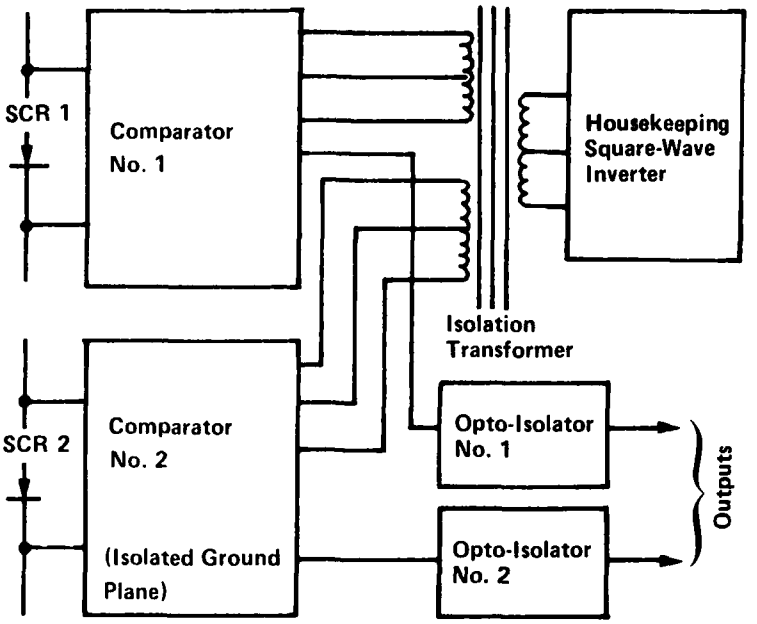


Figure 2.5.2-1 BBS Block Diagram

2.5.2.4 Circuit Schematic--Figure 2.5.2-2 shows a circuit schematic of the back-bias sensor comparator. R1 will be external to the hybrid because it will have 600 V across it and dissipate up to 1 W. R1, along with CR1 and CR2, protect the comparator inputs from 600 V. To sense either a positive or negative voltage with respect to return, point A as well as the inverting and noninverting comparator inputs must be brought out of the circuit for external connection. For a negative sensor, point A is connected to the noninverting input.

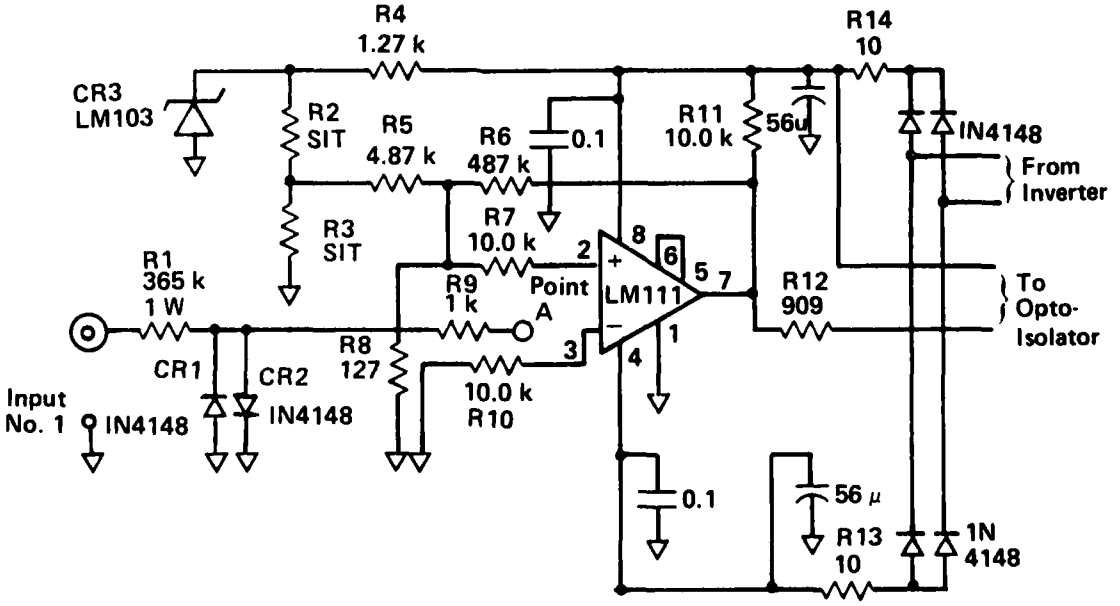


Figure 2.5.2-2 BBS Schematic of One Comparator

For a positive sensor, point A is connected to the inverting input. A stable voltage reference is provided by voltage divider R2 and R3 and the regulator diode CR3. Positive feedback and hysteresis is provided by R6 and R8. R12 is used to limit the current to the photodiode.

2.5.2.5 Power--The BBS is supplied with transformer-isolated ac power. The ac power source is square wave, 25 kHz ±10%, and 15 V ±10% peak-to-peak.

2.5.2.6 Parts List--Table 2.5.2-2 summarizes the BBS parts.

Table 2.5.2-2 BBS Parts List

Description	PN
Comparator	LM111
Optoisolator	6N134
Transformer Core	2616P-L00-3B7

2.5.3 Protection Unit

2.5.3.1 Background--All of the SRI topologies require two series switches to be placed across the source. Should these switches be turned on at the same time, they would be destroyed. One of the primary requirements for the protection unit is to prevent simultaneous conduction of these SCRs. The power switches are divided into two groups that are alternatively toggled during inverter operation. The protection unit must provide this toggle function between groups of power switches. It includes limit checking and control integrator inhibit for the resonant capacitor voltages, source voltage, and output voltage.

The protection unit must work with both a dc-dc and ac-dc converter. To add the ac-dc compatibility to the dc-dc protection unit, two additional handshake signals are required. An RFT signal will be generated in the three-phase unit. The protection unit will respond to this by ensuring that all SCRs are off, all SCRs that were used as diodes have stopped conducting, and the resonant current has decayed to zero. Then, the protection unit will issue a SFT to the three-phase unit and the SRI will be restarted.

The initial start function is also included in the protection unit. When in the off state but with control power applied, the initial conditions of all flip-flops are controlled. When power is applied to the power stage, the polarity of the resonant capacitor will vary depending on switch leakage. The polarity of the resonant capacitor voltage will be used to select the initial set of SCRs to be turned on. The set of SCRs will be selected so the resonant capacitor voltage adds to the source voltage. This is done to ensure maximum resonant current on the initial pulse. When the start signal is received, the protection unit will issue a SFT to the three-phase unit, delay, and then clock a fire command. After this one initial fire pulse, the normal operation commences.

2.5.3.2 Requirements--Table 2.5.3-1 gives the top-level functional requirements for the protection unit.

Table 2.5.3-1 Protection Circuit Top-Level Requirements

- After Group 1 SCRs are fired, a back bias signal from Group 1 shall exist for t seconds before Group 2 shall be enabled to fire.
- The SCRs shall be divided into two groups and shall be fired alternately.
- RFT (Request for Transition)--When this signal from the three-phase controller is true, it shall inhibit SCR fire commands.
- SFT (Safe for Transition)--This is generated in the protection unit in response to an RFT from the three-phase controller. Once RFT is true and there are no SCR fire commands, the protection unit shall look for a 1-0 transition on the back-bias sensors, delay t seconds, and send a SFT high true to the three-phase controller.
- Resonant capacitor or input voltage out of limits shall inhibit the Fire Group 1 and 2 SCR signals.
- The output voltage out of limit shall inhibit the integrator in the control circuit.
- When not connected, there shall be a minimum of 1 meg ohm at 2 V common mode between input and signal return and 1 meg ohm at 2 V common mode between output and signal return at dc.

As shown in the block diagram of Figure 2.5.3-1, the protection unit is partitioned into three functional areas: (1) SCR fire generator and digital protection (2) start circuit and (3) analog protection.

The functional requirements for each area are described.

2.5.3.2.1 SCR Fire Generator and Digital Protection--This circuit will generate alternate SCR fire signals; fire GRP1 SCR, Fire GRP2 SCR, and then repeat. The logic expression for fire SCRs is

$$\text{Fire GRP 1 SCR} = (\overline{\text{FIRE}}).(\overline{\text{ANALOG PROTECT}}).(\text{TOGGLE FF})$$

$$\text{Fire GRP 2 SCR} = (\overline{\text{FIRE}}).(\overline{\text{ANALOG PROTECT}}).(\overline{\text{TOGGLE FF}})$$

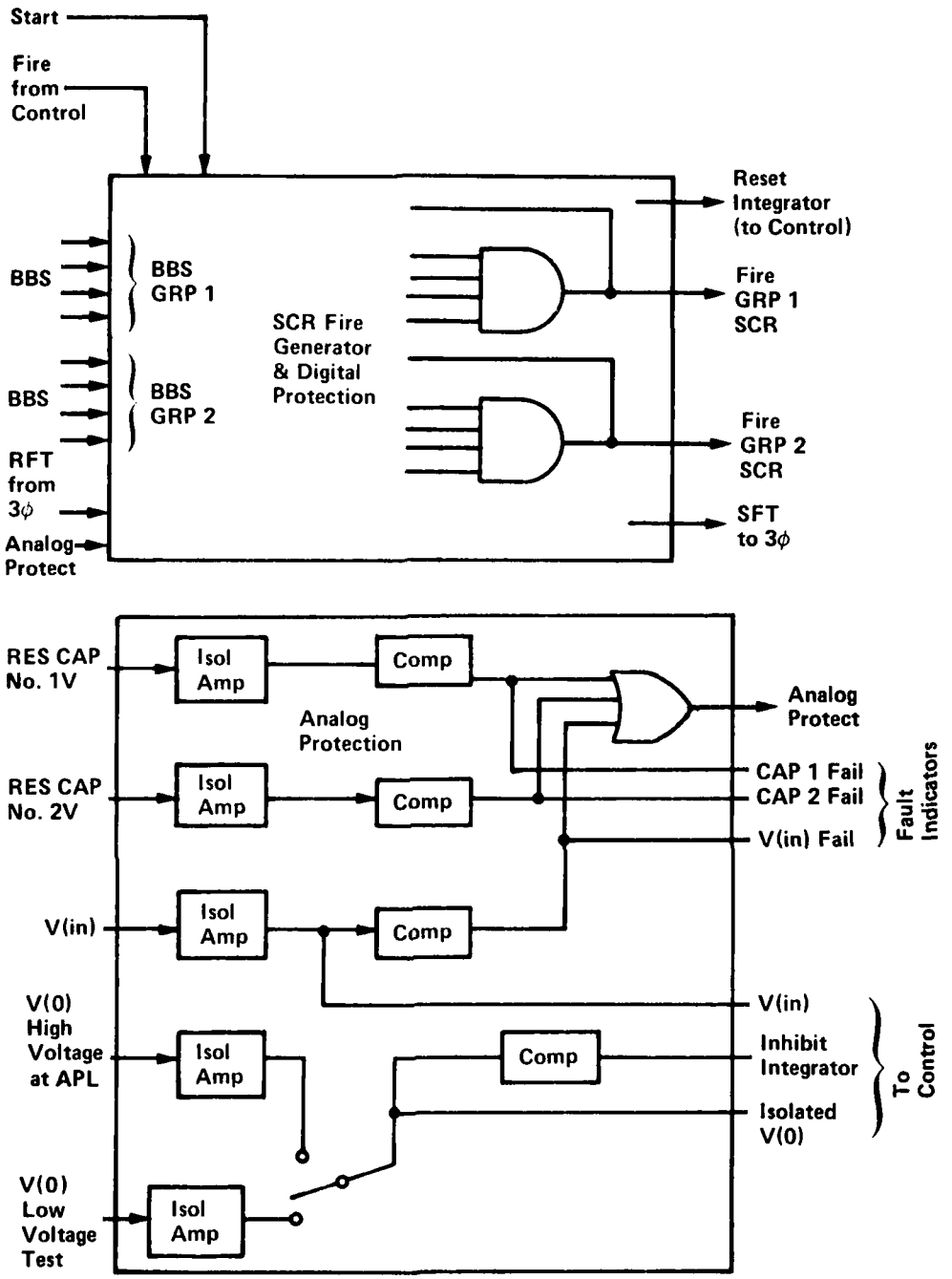


Figure 2.5.3-1 Protection-Simplified Block Diagram

After a fire command has been issued, the circuit will check to see that a valid back bias signal has been received from the last fired group of SCRs. For example, if GRP 1 was last fired, there will be a valid back bias signal from GRP 1 BBS before GRP 2 SCRs can be fired. The back bias signal will exist for TQ seconds before it is considered valid.

The following is a description of the requirements for responding to RFT and generating SFT when the protection unit is used in the three-phase system. When RFT is true, the fire flip flop will not issue a fire signal. The system will wait until both Fire GRP 1 SCR and Fire GRP 2 SCR signals are false, and then it will look for a back-bias to forward-bias transition on BBS 1 or BBS 2. When it finds the back-to-forward bias transition, the circuit will send a SFT to the three-phase unit.

2.5.3.2.2 Start Circuit Requirements--An external OFF/RUN switch with debounce circuits will be provided. The following requirements for a start sequence are established:

1) Main power disconnected;
2) RUN/OFF switch to OFF;
3) Bias supply to ON; external pause to ensure bias supply output in steady state;
4) Main power connected;
5) RUN/OFF switch to RUN.

Three sets of requirements must be addressed: (1) OFF requirements, (2) RUN requirements, and (3) STOP requirements.

2.5.3.2.3 OFF Requirements--Under the constraints that main power must be disconnected, RUN/OFF to OFF, and then the bias supplies are turned on, the following requirements are established:

1) START will be false;
2) Hold the following flip-flops in the reset state;
    a) Start flip-flop;
    b) Memory latch;
    c) Fire flip-flop;

Holding START false ensures that no Fire GRP 1 or 2 SCR signal can be issued. Holding the three flip-flops (FFs) in reset for an OFF switch command ensures they are in the proper initial state when a RUN command is received.

2.5.3.2.4 RUN Requirements--The proper initial states were established during the OFF state by resetting the Start FF, Memory Latch, and Fire FF. When the RUN/OFF switch goes to RUN, the following sequence will occur:

1) Remove reset to Start FF, Memory Latch, and Fire FF;
2) Use a one shot to provide a pulse to SFT;
3) Use the 1-0 edge of SFT to clock the Start FF;
4) The Start FF will set the Fire FF.

The start circuit will only pulse one group of SCRs, GRP 1 or GRP 2. The initial group of SCRs to be turned on will be chosen based on the polarity of the resonant capacitor. The SCRs will be chosen so the resonant capacitor voltage adds to the source voltage. When either Fire Group 1 or 2 SCRs is True, the Start FF will be reset to remove the set command to the Fire FF. The start circuit will have no further effect on the system after one group of SCRs has been fired once.

2.5.3.2.5 STOP Requirements--The STOP requirement provides for safe turn-off of the power stage by the RUN/OFF switch while main power is connected.

The STOP requirements are satisfied for all three power units. For the two dc/dc units, when the RUN/OFF switch goes to OFF, the Fire Group 1 and 2 SCR signals are held false. The commutating diodes provide a path for the resonant current. For use with the three-phase units, when the RUN/OFF switch goes to OFF, the Fire Group 1 and 2 SCR commands are inhibited. In the three-phase unit, the SCRs that are to be used as diodes are controlled only by the V12, V13, V23, and BBS signals. Thus, the commutating diode function will be provided even though the Fire signal is driven false.

2.5.3.2.6 Analog Protection Requirements--Table 2.5.3-2 identifies the analog input signal names and characteristics for each of the three power units. There are different analog inputs for the three different power units. In all cases, the resonant capacitor voltage can have a common-mode voltage equal to the source voltage. The resonant capacitors all have a maximum operating voltage limit. This protection limit must be set lower than the nameplate rating. When the protection limit is exceeded, the capacitor will be protected by inhibiting SCR fire commands. Because the resonant capacitor voltage can swing both plus and minus, a window comparator will be required.

Source voltage is to be sensed, compared to a positive limit only, and the SCR fire commands stopped if the input limit is exceeded.

Table 2.5.3-2 Analog Inputs to Protection from the Three Power Units

Power Unit	Inputs	Common-Mode Voltage	Limits	Ground Reference
10 kW dc-dc 1/2 Bridge	Resonant Cap V	600 V	±750 V	Input
	V(IN) dc	2 V	−700 V	Input
	E(OUT) Flight	2 V	5 V + TBD	Output
	E(OUT) Test	250 V	350 V	Input
5 kW ac-dc Full Bridge	Resonant Cap V	300 V	±600 V	Input
	V(IN) Rectified Three-Phase	2 V	−200 V	Input
	E(OUT) Flight	2 V	7 V	Output
	E(OUT) Test	250 V	350 V	Input
200 kW dc-dc Twin Full Bridge	Bridge 1 Resonant Cap V	600 V	±750 V	Input
	Bridge 2 Resonant Cap V	600 V	±750 V	Input
	V(IN)	2 V	700 V	Input
	E(OUT) Flight	2 V	7 V	Output
	E(OUT) Test	600 V	650 V	Input

For each of the three power units, E(OUT) is available in two configurations. In the flight configuration, there will be an isolation transformer between input and output. The sensed output voltage will be 5 V for full scale. The isolation requirements are 1 megohm at 2 V common mode at dc. When used, it is required that the power return, signal return, and output return all be connected to a single-point ground. When the sensed output voltage exceeds a limit, the integrator in the control unit is inhibited. A configuration used for test only, has no output transformer for the power stage. The primary of the output transformer is replaced by a diode bridge, filter capacitor, and resistive load.

2.5.3.3 Block Diagram--Figure 2.5.3-1 is a simplified block diagram of the protection unit. All input and output signals for the protection unit are identified in the figure. All logic signals are positive true. The start signal will be externally debounced.

2.5.3.4 Schematic Diagram--Figure 2.5.3-2 is a schematic diagram for the protection unit.

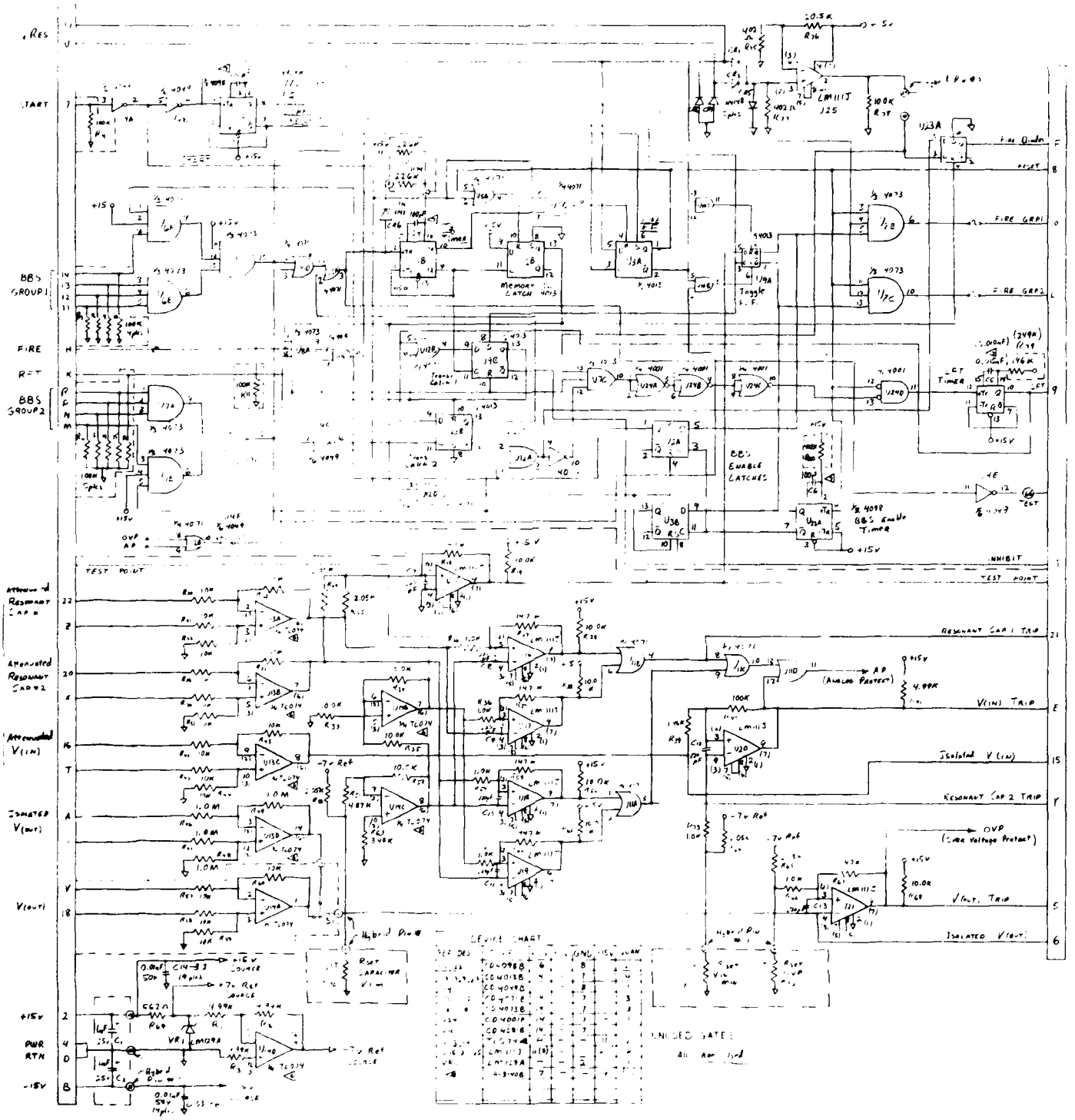


Figure 2.5.3-2 Protection Unit Schematic

2.5.3.5 Power Requirements--The protection unit will be supplied with + and -15 V ± 10%. The power dissipation will be less than 0.5 W.

2.5.3.6 Parts List--Table 2.5.3-3 gives the parts list.

Table 2.5.3-3 Protection Units Parts List

Reference Designator	Part Number	Description
U1,22	CD4098B	Dual Monostable Multivibrator
U2,3,9,23	CD4013B	Dual D-Type Latch
U4	CD4049B	Hex Inverter
U5,11,12	CD4071B	Quad 2-Input OR
U6, U7, U8	CD4073BE	Triple 3 Input AND
U24	CD4001B	Quad 2-Input NOR
U10	CD4081B	Quad 2-Input AND
U13,14	OP-15*	BiFet Op Amp
U15-21,25	LM111J	Comparator
VR1	LM129A	Voltage Reference

*Substituted with RCA CA-3140B in hybrid microcircuit.

2.5.4 Three-Phase Unit

2.5.4.1 Background--Figure 2.5.4-1 shows the topology of the existing three-phase power stage. There are six pairs of oppositely connected SCRs, or a total of 12 SCRs. A representation of the input three-phase, sinusoidal waveforms is at the top of Figure 2.5.4-2 (Ref 7). A simplified explanation of the three-phase unit's requirements follows. It is necessary to select the phase pair that has the largest positive difference. In 360 electrical degrees, there will be six phase pairs. Each phase pair will be 60 electrical degrees long, or last 2.8 ms for a 60-Hz input. When the power stage is within the time period of a phase pair, it uses only four SCR pairs and operates as a conventional full-bridge SRI. This is illustrated in Figure 2.5.4-3.

As the phase pairs change, the selection of four out of the six SCR pairs changes. Each SCR not used 1/3 of the time, is used as an SCR for another 1/3 of the time, and is used as a diode for 1/3 of the time.

2.5.4.2 Requirements

2.5.4.2.1 Logic Requirements--Table 2.5.4-1 summarizes the high-level requirements for the three-phase unit.

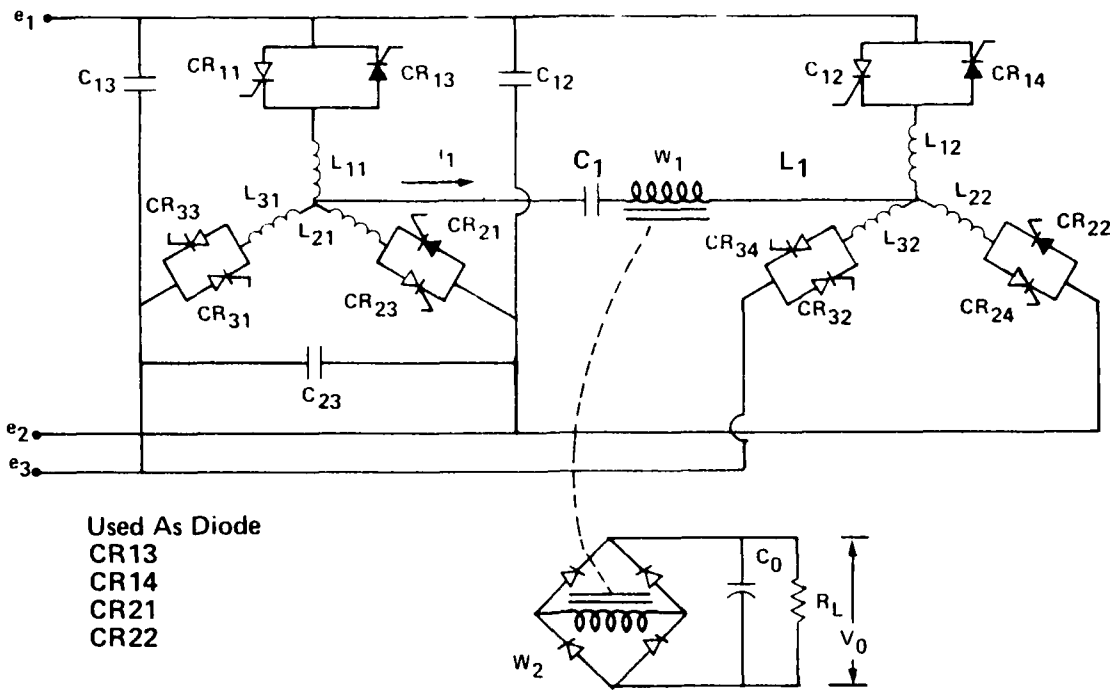


Figure 2.5.4-1 Three-Phase ac-dc SRI-Based Converter, 5 kW ac-dc

Table 2.5.4-1 Three-Phase Unit Top-Level Requirements

- Determine phase pair. - Determine the proper back-bias states based on the phase pair. - Generate 12 SCR fire signals based on the phase pair and a fire group 1 or 2 SCR signal from the protection unit (when the SCR is used as an SCR). - Generate 12 SCR fire signals based on the phase pair and the back-bias states (when the SCR is used as a diode).

The logic requirements for the three-phase unit are derived from the topology of the existing three-phase unit and the three-phase signal diagram. Figure 2.5.4-2 (Ref 7) shows the three-phase signals where el, e2, and e3 are the three-phase inputs. V12, V13, and V23 determine whether a particular phase is positive or negative with respect to another phase voltage and each is positive for 180 out of 360 electrical degrees. The Phi 1-2 to Phi 3-2 pick the instantaneous phase pair with the maximum positive difference. Each of the six Phis is true for 60 out of 360 electrical degrees.

Figure 2.5.4-1 shows the topology of the existing APL three-phase power stage. Figure 2.5.4-3 shows the eight SCRs that are active for Phi 1-2.

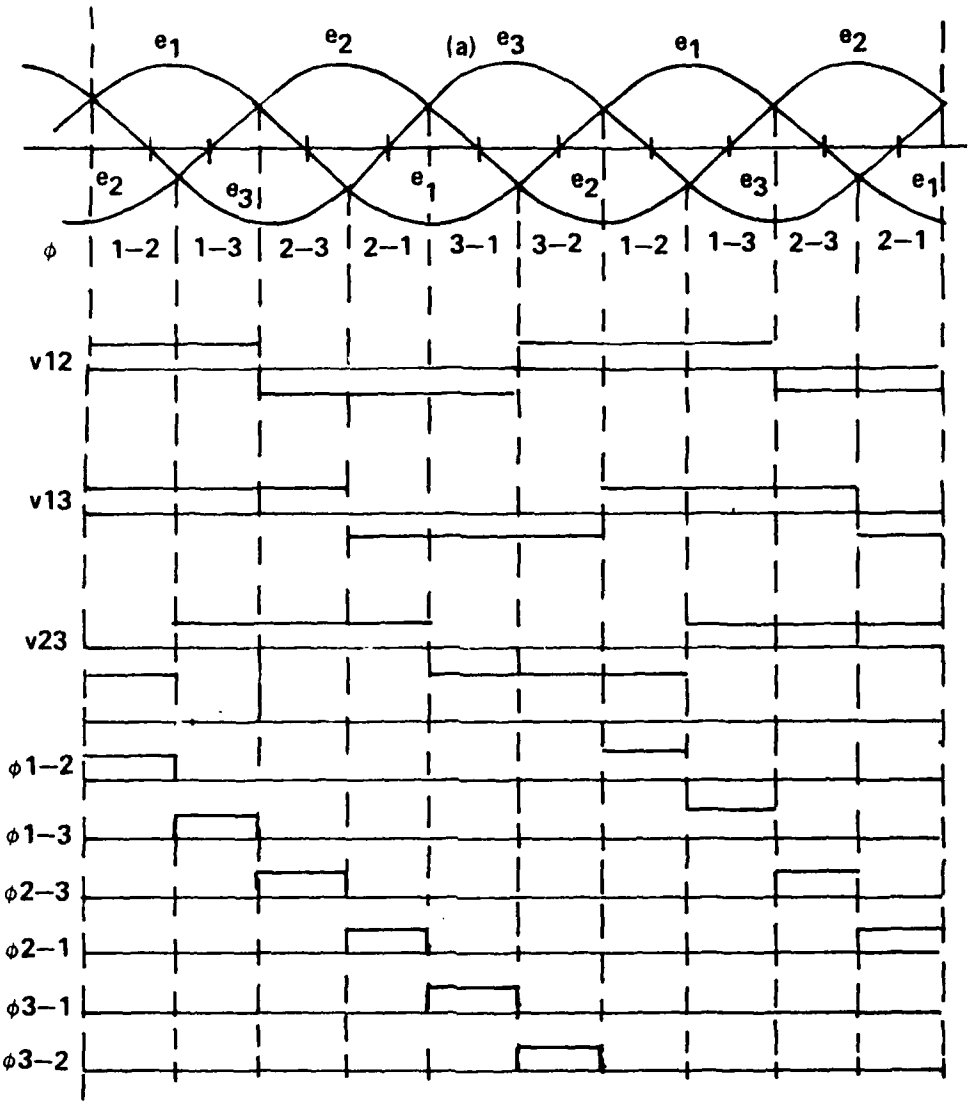


Figure 2.5.4-2 Three-Phase Signals from Schwartz (Ref 7)

The SCRs used as diodes in Phi 1-2 have been highlighted in black. Four SCRs are not used in Phi 1-2. Five more schematics similar to Figure 2.5.4-3 could be drawn and the active devices identified to function as an SCR or a diode. Using Figure 2.5.4-2 for Phi 1-2 and five similar figures for the other five phase pairs, one can derive the use of each SCR by phase pair. Each SCR is identified by designator and function (SCR or diode) in each of the six phase pairs in Table 2.5.4-2. In the table, S represents use as an SCR and D represents use as a diode. While Phi 1-2 exists for 60 electrical degrees, the unit functions as a full-bridge SRI. For resonant current of one direction, SCR11 and SCR24 function as SCRs and SCR13 and SCR22 are used as their antiparallel diodes. For resonant current of the opposite polarity, SCR23 and SCR12 are used as SCRs and SCR21 and SCR14 are used as anti-parallel diodes.

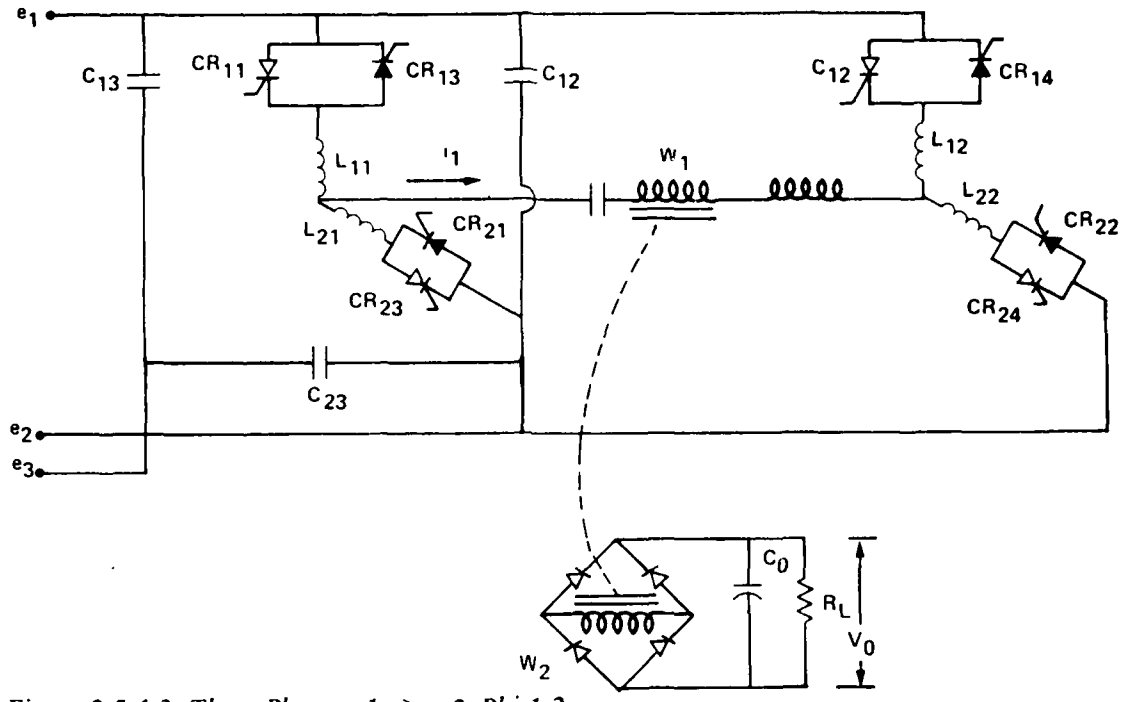


Figure 2.5.4-3 Three-Phase, e1 > e2, Phi 1-2

The logic signal requirements derivation is now reduced to defining the logic equations for:

1) V12, V13, and V23;
2) RFT;
3) Generate six Phi XY from V12, V13, and V23;
4) Group 1 and Group 2 Enable (back-bias check);
5) 12 SCR commands (both as SCR and diode).

2.5.4.2.2 V12, V13, and V23 Generator--The generator is shown in Figure 2.5.4-4. Comparators U1, U2, and U3 are used to generate V12, V13, and V23 from the phase voltages. The logic for V12, V13, and V23 is tabulated:

Phase Voltages	V(iJ)
e1 e2	V12 High
e1 e2	V12 Low
e1 e3	V13 High
e1 e3	V13 Low
e2 e3	V23 High
e2 e3	V23 Low

Table 2.5.4-2 SCR Identified by Phi and Use (SCR or Diode)

ϕ	SCRs									
	11	13	21	23	31	33	12	14	22	24	32	34
1-2	S	D								S		
			D	S			S	D	D			
1-3	S	D									D	S
					D	S	S	D				
2-3			S	D							D	S
					D	S			S	D		
2-1			S	D			D	S				
	D	S							S	D		
3-1					S	D	D	S				
	D	S									S	D
3-2					S	D			D	S		
			D	S							S	D

The three flip-flops *U4*, *U5*, and *U6* are used to hold the three states, clock them, and generate the inverse states.

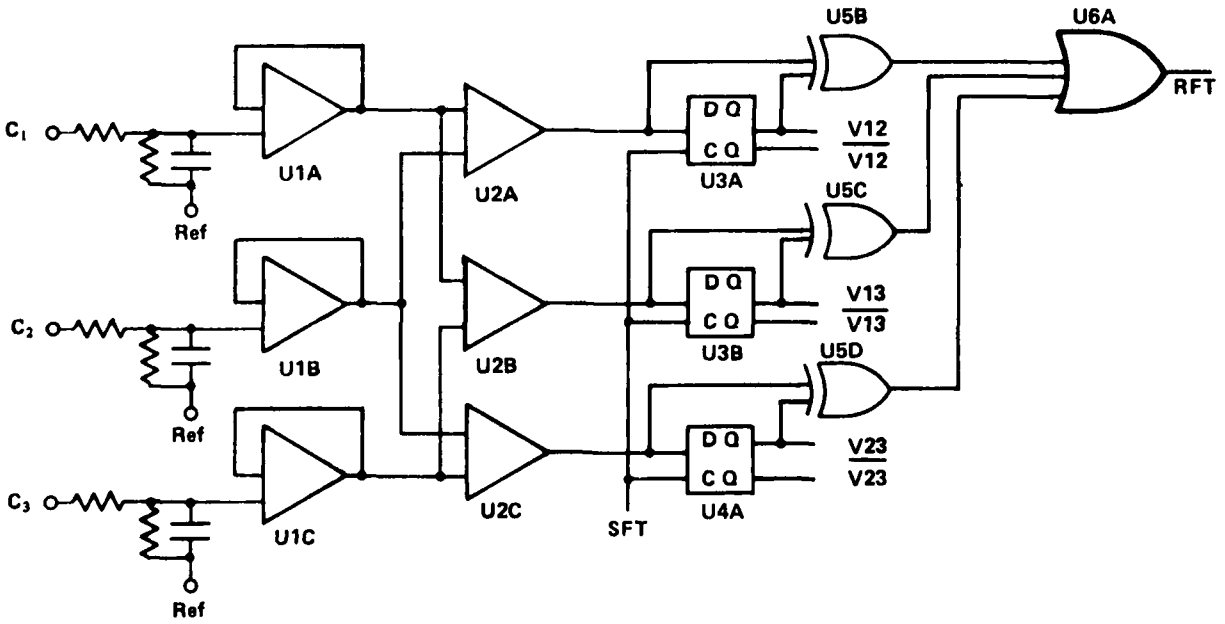


Figure 2.5.4-4 VXY and RFT Generator

2.5.4.2.3 RFT Generator--Figure 2.5.4-4 is a simplified schematic of the RFT generator. The generator comprises the three D flip-flops (U3A, U3B, and U4A) the three EXCLUSIVE OR gates, U5B, U5C, and U5D and the NOR gate U6A. It is necessary to generate an RFT (Request for transition) signal whenever a D flip-flop input is different from its Q output. The expression for RFT is a logic equation. The logic symbolism used is tabulated.

Description	Logic Symbol
Logical OR	+
Logical AND	·
Exclusive OR	+
Logic Variable	A
NOT A	$\overline{A}$
N^{th} D FF Input	ND
N^{th} D FF Q Output	NQ
N^{th} D FF Q NOT Output	$\overline{NQ}$

The logic equation for RFT is;
RFT = (4D + 4Q) + (5D + 5Q) + (6D + 6Q).

RFT is an input to the protection circuit. The protection circuit requirements to generate a SFT (safe for transition) signal are:

1) Inhibit any SCRs from firing;
2) Allow SCRs used as diodes to fire;
3) Wait until SCRs used as diodes have stopped conducting (no backbias signals exist);
4) Delay for TQ to allow SCR used as diode to recover blocking capability.

The SFT signal from the protection circuit will be used to clock the three D flip-flops.

2.5.4.2.4 Phi XY Generator--The six Phi ij logic equations can be written directly from the three-phase signal chart in Figure 2.5.4-2. Table 2.5.4-3 shows the six logic equations for the Phi ij. Table 2.5.4-4 shows the definitions of the Group 1 and 2 SCRs.

Table 2.5.4-3 Logic Equations for Phi 12 to 32

$$PH1\ 12 = V12.\overline{V13}.V23$$

$$PH1\ 13 = V12.V13.V23$$

$$PH1\ 23 = \overline{V12}.V13.V23$$

$$PH1\ 21 = \overline{V12}.\overline{V13}.V23$$

$$PH1\ 31 = \overline{V12}.\overline{V13}.\overline{V23}$$

$$PH1\ 32 = V12.\overline{V13}.\overline{V23}$$

Table 2.5.4-4 Definition of Group 1 and 2 SCRs

Group 1 SCRs	Group 2 SCRs
SCR11	SCR23
SCR24	SCR12
SCR34	SCR33
SCR21	SCR22
SCR14	SCR13
SCR31	SCR32

2.5.4.2.5 Group 1 Enable and Group 2 Enable--Group 1 Enable and Group 2 Enable are generated in the three phase unit and sent to the protection unit. For operating the SRI, there are two groups of SCRs. They are fired alternately. Before Group 1 SCR can be fired, it is necessary to ensure all of the Group 2 SCRs are off (back-biased). Also, before a Group 2 SCR can be fired, it is necessary to ensure all Group 1 SCRs are back-biased.

The logic equations for GRP 1 Enable and GRP 2 Enable can be written by inspection from Table 2.5.4-2.

The definition of Group 1 and Group 2 SCR depends on the Phi ij.

From Table 2.5.4-2, before SCR23 and SCR12 can be fired as SCRs, there must be back bias signals for SCR11 and SCR24. In all the phases, the top pair used as SCRs is called Group 1 and the bottom pair Group 2. By inspection from Table 2.5.4-2:

BBS Grp 1 =(Phi 12)·(BBS 11)·(BBS 24)+(Phi 13)·(BBS 11)·(BBS 34)
+(Phi 21)·(BBS 14)·(BBS 24)+(Phi 23)·(BBS 21)·(BBS 34)
+(Phi 31)·(BBS 31)·(BBS 14)+(Phi 32)·(BBS 31)·(BBS 24)

BBS Grp 1 =(Phi 12)·(BBS 12)·(BBS 23)+(Phi 13)·(BBS 12)·(BBS 33)
+(Phi 21)·(BBS 22)·(BBS 13)+(Phi 23)·(BBS 22)·(BBS 33)
+(Phi 31)·(BBS 32)·(BBS 13)+(Phi 32)·(BBS 32)·(BBS 23)

GRP 1 EN is of the AND/OR logic form.

The implementation is shown in Figure 2.5.4-6.

2.5.4.2.6 SCR Fire Commands--The logic equations can be written directly from Table 2.5.4-2. Because there are 12 SCRs, 12 logic equations are required. Firing the SCR when it functions as both an SCR and as an antiparallel diode must be accounted for. For example, SCR11 is used as an SCR in Phi 12 and Phi 13, and is used as a diode in Phi 21 and Phi 31. Fire Group 1 and Fire Group 2 are generated in the protection unit and are inputs to the three phase unit.

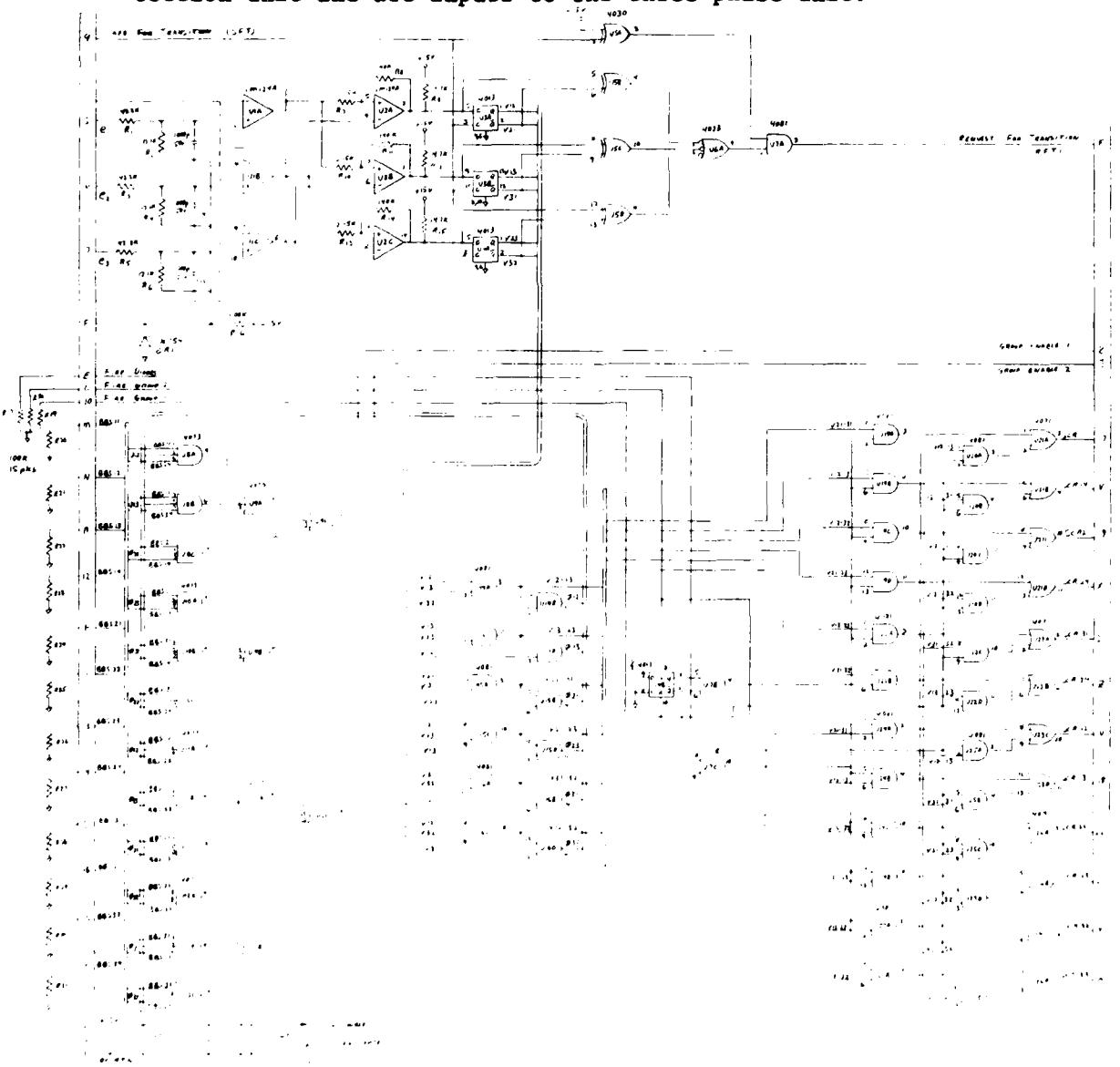


Figure 2.5.4-5 Three-Phase Unit Schematic

Table 2.5.4-5 shows all 12 fire SCR logic equations.

Table 2.5.4-5 Fire Logic Equations

SCR		Derivation	Diode		Derivation
11	=	FG2.V12.V13	13	=	FG2.V12.V13.Iz
12	=	FG1.V12.V13	14	=	FG1.V12.V13.Iz
13	=	FG1.V21.V31	11	=	FG1.V21.V31.Iz
14	=	FG2.V21.V31	12	=	FG2.V21.V31.Iz
21	=	FG2.V21.V23	23	=	FG2.V21.V23.Iz
22	=	FG1.V21.V23	24	=	FG1.V21.V23.Iz
23	=	FG1.V12.V32	21	=	FG1.V12.V32.Iz
24	=	FG2.V12.V32	22	=	FG2.V12.V32.Iz
31	=	FG2.V31.V32	33	=	FG2.V31.V32.Iz
32	=	FG1.V31.V32	34	=	FG1.V31.V32.Iz
33	=	FG1.V13.V23	31	=	FG1.V13.V23.Iz
34	=	FG2.V13.V23	32	=	FG2.V13.V23.Iz

2.5.4.3 Power Requirements--The circuit requires only +15V $\pm$ 10%. The power dissipation is less than 0.5 W.

2.5.4.4 Block Diagram--Figure 2.5.4-6 is a block diagram of the three-phase unit. All of the input and output signals for the three-phase unit are shown. All logic signals are positive true and are compatible with CMOS powered from 15-V.

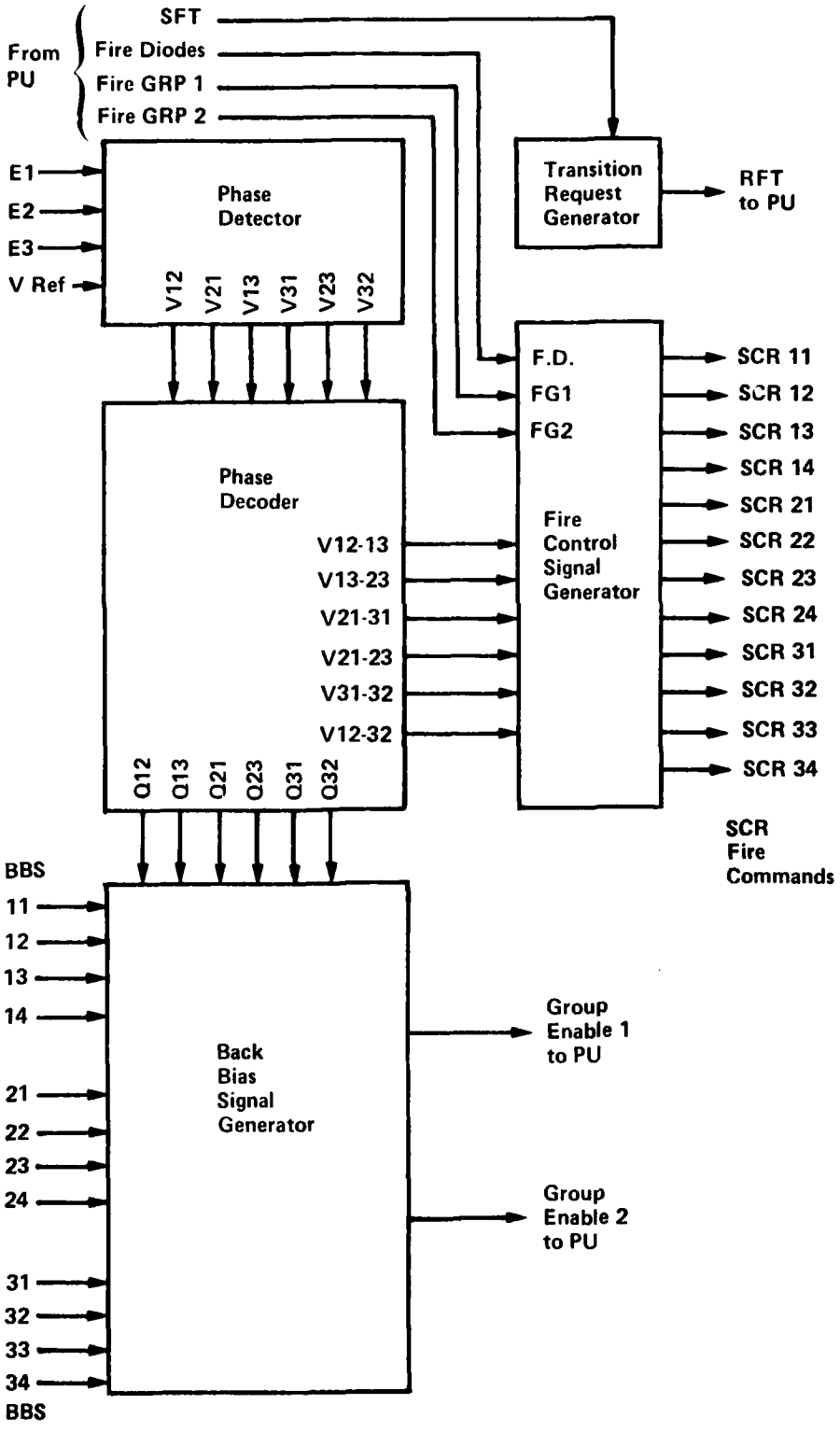


Figure 2.5.4-6 Three-Phase Unit Block Diagram

2.5.4.5 Schematic Diagram--A schematic diagram of the three-phase unit is shown in Figure 2.5.4-6.

2.5.4.6 Parts List--The parts list is shown in Table 2.5.4-6.

Table 2.5.4-6 Three-Phase Unit Parts List

Reference Designator	Part Number	Description
U1	LM124A	Quad Op Amp
U2	LM139A	Quad Comparator
U3,4	CD4013B	Dual D-type Latch
U5	CD4030B	Quad Exclusive OR
U6	CD4023B	Quad NAND
U7,14,15,16,19 20,24,25,27	CD4081B	Quad 2-input AND
U8,10,11,13	CD4073B	Triple 3-input AND
U9,12	CD4075B	Triple 3-input OR
U21,23,26	CD4071B	Quad 2-input OR

2.5.5 Control Unit

2.5.5.1 Background--The control unit requirements for the three existing APL converters were established. The 10-kW dc-dc unit had a current control loop, but not a voltage control loop. The 5kW ac-dc unit had both a voltage and a current control loop. The 200-kW unit had a current control loop.

For a general control unit applicable to a wide range of SRI topologies, it is necessary to implement both a fast current control loop and a slower voltage control loop. The two feedback variables are the resonant current and the output voltage. The basic control in the three units consists of integrating a portion of the rectified resonant current, comparing the integrator output to a reference, and sending an SCR fire signal when the integrator output exceeds the reference. In the 10 kW unit, only the diode portion of the resonant current is integrated. The basic relations among the rectified resonant current, reset, integrator output, and fire command--are shown in Figure 2.5.5-1.

In Figure 2.5.5-1, only the diode portion of the resonant current is integrated. When the integrator output exceeds the reference, a fire command to the protection unit is issued. When the protection unit declares that it is safe to fire the SCRs, it first fires the SCRs and generates a reset to the integrator. The fire signal must be latched in the protection unit. From the figure it is apparent that the resonant current cannot be integrated directly; an increase in diode current causes a decrease in the SCR firing angle that results in a larger resonant current. The simplest stable current control loop is one where the resonant current is subtracted from a reference and the difference is integrated.

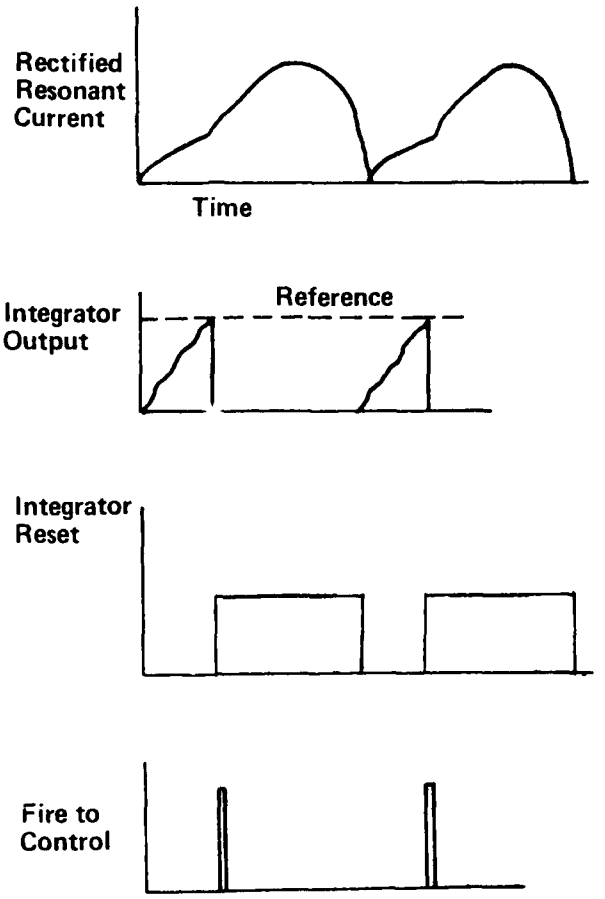


Figure 2.5.5-1 Control Unit Waveform

One additional function is incorporated: an integrator inhibit function. Integrator inhibit is used to hold the integrator and stop it from integrating. This function effectively removes the input to the integrator but does not reset it. Phase transition is used as the parameter to control integrator inhibit. When a phase transition logic transfer is in progress the integrator is inhibited.

2.5.5.2 Requirements--The feedback variables are current and the output voltage. The resonant current is rectified in the control unit and there is both a current and a voltage control loop. The output voltage is compared with a reference and the error voltage integrated in the first integrator. This integrator time constant is several half periods of 10 kHz. The difference between the output of the first integrator and the resonant current is the input to the second integrator. The time constant of the second integrator is determined from the breadboard and is expected to be close to a half period of 10-kHz. The output of the second integrator is compared with a reference and when the reference is exceeded, a fire command is issued. Two positive true logic commands are incorporated in the control unit. The reset signal resets the second integrator to a known voltage. The inhibit command will remove the input to the integrator. All interface signals are compatible with 15-V CMOS.

2.5.5.3 Block Diagram--Figure 2.5.5-2 is a block diagram of the control unit. This block diagram mechanizes the requirements described in the previous section. A significant feature of this implementation is the second integrator, which is discussed next.

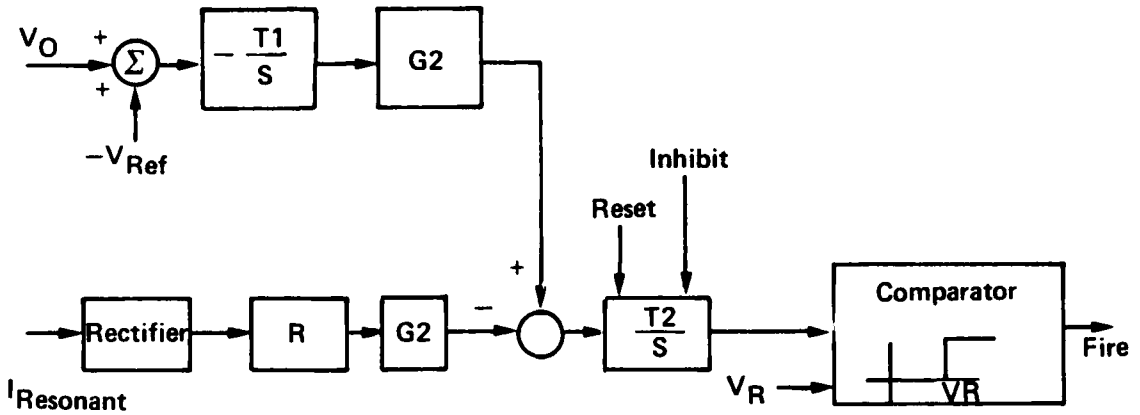


Figure 2.5.5-2 Control Unit Block Diagram

The output of the integrator is compared with reference voltage Two, and a fire SCR command is issued when the reference is exceeded. The following comments about the form of the integrator output are pertinent. First, when the system is initially turned on, e(out) and the resonant current are both zero. Because the reference voltage Two is not zero, the output of integrator Two will rapidly go to the reference level and a fire command will be generated. In the steady-state, an increase in the resonant current results in the integrator taking longer to reach the reference level Two where a fire command is issued. Similarly, a decrease in e(out) will increase the SCR firing angle. The system is stable on a cycle-by-cycle basis.

2.5.5.4 Circuit Diagram--A control unit circuit schematic is shown in Figure 2.5.5-3.

2.5.5.5 Power--The control unit is supplied with $\pm$ 15V $\pm$ 10%. The +15V is the same as is used for the 15-V CMOS logic in the protection unit.

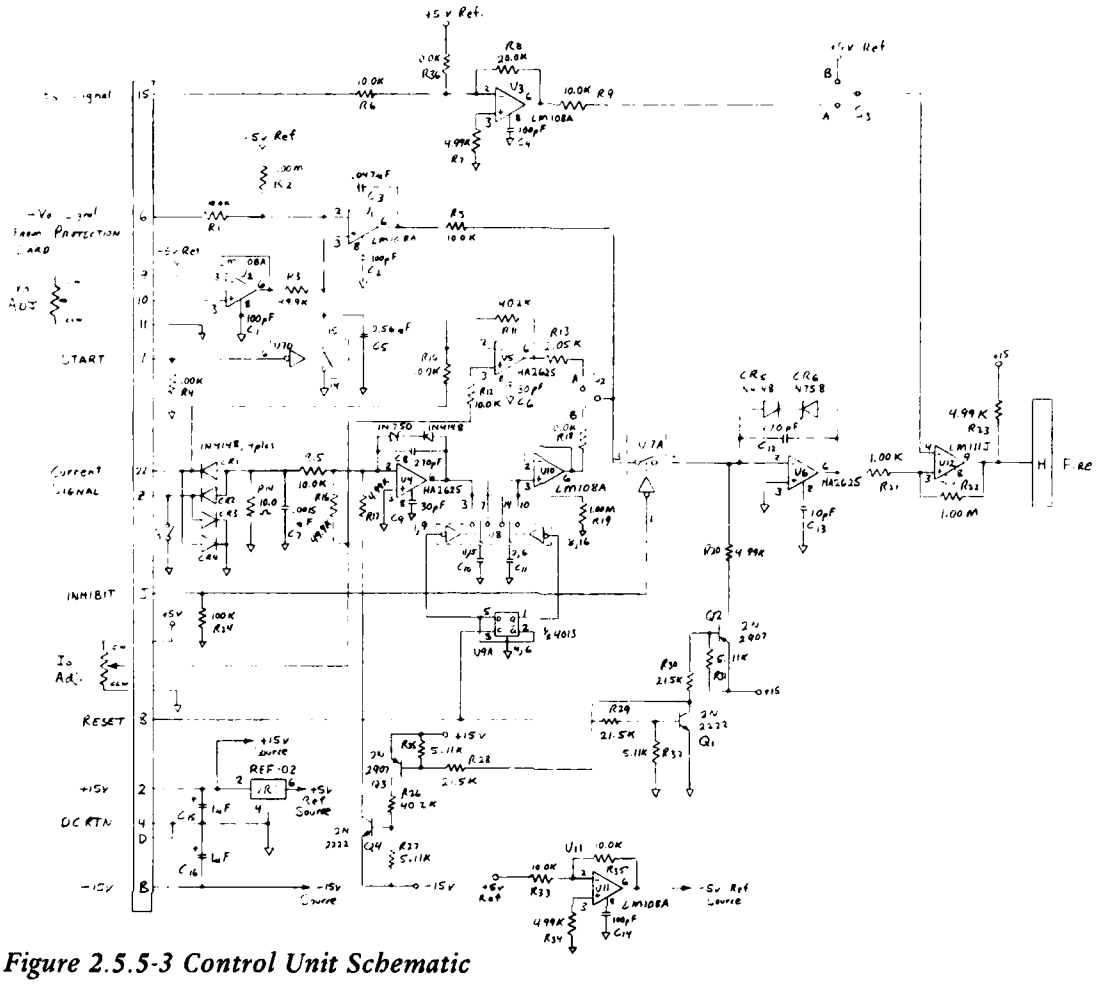


Figure 2.5.5-3 Control Unit Schematic

2.5.5.6 Parts List--Table 2.5.5-1 is a parts list.

Table 2.5.5-1 Control Unit Parts List

Reference Designator	Part Type Number	Description
U1,2,3,10,11	LM108A	Op Amp
U12	LM111J	Comparator
U4,5,6	HA2625	High Speed Op Amp
U7,8	SW-03	Quad Analog Switch
U9	CD4013B	Dual D-type Latch

2.6 MICROPROCESSOR STUDY

2.6.1 Study Guidelines

The first reason to consider a microprocessor was to make it easier to reconfigure the controller for operation with the three existing power sections. The second was to identify candidate tasks for a microprocessor in future SRI-based converters.

2.6.2 Microprocessor Reconfiguration Study

A study was performed to identify how a microprocessor could be used to reconfigure the controller to make it easier to use with the three existing APL power sections. The block diagrams of the controller for each of the power stages were inspected, and the most complex controller was for the three-phase ac-dc unit. The following scenario was used for the study. The most complex controller, the 5-kW ac-dc, would be fabricated first. There would be one controller panel for BNC cable interfaces. When configurations were changed, cables from the controller BNC cable interface to a different power unit would be changed. For the microprocessor to reconfigure the control system, analog switches or relays would have to be added along with interface circuits. The switches could be used to change interconnections among the controller blocks to connect the three-phase controller for the ac-dc unit or to disconnect it for dc-dc control. The switches could also be used to change the following gains:

1) Differential amplifiers for resonant capacitor voltages;

2) Resonant current transformer amplifiers;

3) Source voltage;

4) Output voltage amplifier.

The operator could give one command to the microprocessor to change the switches from one configuration to the next. This is the only function for the microprocessor. The microprocessor would not operate again until the next time the operator wanted to run the controller with a different power unit. This same function however could be performed by a three-position rotary switch and does not warrant the use of a microprocessor for the following reasons:

1) There is no advantage for a microprocessor in configuring a controller. If switches or relays were used for gain and configuration change, the control would be more simply done with the switch rather than a microprocessor;

2) A microprocessor would add unnecessary complexity to verify the position of the switches;

3) A microprocessor could add unreliability because of transient phenomena that could reconfigure the controller while the power stage was running; this would have a potentially disastrous impact on the power stage;

4) A microprocessor would require an UPS to remove facility power transients.

2.6.3 Microprocessor Functions for Future SRI

The purpose of this study was to also identify areas of applying microprocessors in future SRI-based converters.

The methodology for performing this study was to identify failure modes and effects, a measurements list and microprocessor functions.

Table 2.6-1 (Ref 8) summarizes the major failure modes and effects in an SRI. A major failure mode is a shorted SCR. When an SCR shorts, there will be a short across the source the next time its companion SCR fires. This type of fault will normally be cleared by an input fuse opening. The failures fall into three classes:

1) No output;

2) High or low output voltage;

3) SRI overheats.

Table 2.6-1 Series-Resonant Inverter Failure Modes and Effects

Failure Mode	Cause	Effect
Power SCR Short	SCR Fail, Control Failure, Fuse Fail	No Output
Power SCR Open	Control or SCR Fail	No Output
Commutation Diode Shorted	Diode Fail, Fuse Fail	No Output
Load Short	Load Fail	No Output Power, SRI Not Harmed by Short
V(OUT) High	Control Fail, OV Protection Fail	Damage Loads
No Output V	Multiple Component, Wire Open	No Power Output
Degraded Efficiency	Filter Cap ESR Increase	Assembly Overheats
Resonant Caps Fail on Overvoltage	Lack of Redundancy, Lack of Margin	No Output
V(OUT) Low	Control Failure	Insufficient P(OUT)

External failures can also affect the SRI. On the input side, the source voltage can go high or low making it impossible for the SRI to perform its required function. On the output side, the external loads can fail to low impedance, the output may be overloaded by the system incorrectly connecting an excessive number of loads, or the load bus may open.

A candidate measurements list is shown in Table 2.6-2

Table 2.6-2 Measurements List

Parameter
V(IN)
I(IN)
V(OUT)
I(OUT)
V(Res Cap 1)
V(Res Cap 2)
Temp 1 to Temp N
Resonant Frequency

The measurements include the terminal voltages and currents, resonant capacitor voltages, internal temperatures, and the resonant frequency.

Table 2.6-3 lists the candidate microprocessor functions. The microprocessor is used for automated data acquisition, limit checking, self protection by shutting down when limits are exceeded, state of health monitoring and status reporting, diagnosis and correction of output low voltage conditions, and peak power tracking with a solar array.

A significant microprocessor function is to automate data acquisition and limit checking. By periodically taking the data and comparing them to limits, the SRI state of health can be determined. Measurement of key internal temperatures will be a significant input to state-of-health determination. Efficiency is also a key indicator of state of health. The microprocessor is well-suited to efficiency calculation and limit checking. In general, efficiency will be a function of terminal conditions. As a major problem with power systems in spacecraft in the past has been a paucity of information about real-time failures, one strong automation candidate is failure monitoring and reporting. For example, there can be multiple reasons for low-output voltage. The input voltage may be low, the SRI may have a control failure, or the output may be overloaded. The microprocessor can therefore be used to diagnose the problem and take corrective action. It can be used to check the input for normal values, remove loads on a priority basis and check the output after each removal, or finally diagnose the fault as an internal SRI failure.

Table 2.6-3 Microprocessor Functions For Future SRI

- Data acquisition;
- Perform limit checks on all measurements;
- Self protection by automatic shut down on limit check failure;
- Monitor V(IN), V(OUT), and I(OUT) to sense shorted load; automatically turn SRI off to allow shorted load to be removed or recovered; microprocessor to hold SRI off, then automatically try to restart;
- Monitor key internal temperatures;
- Periodically calculate efficiency and compare to limits; if efficiency is below limits, the microprocessor can report to an operator or the next higher level computer, and system executive can elect to place low efficiency unit on standby and activate back up unit;
- Maintain measurements before and after a shutdown; report reason for shut down along with pre shutdown data to next higher level;
- Maintain a state of health status word for SRI;
- Monitor and report status of input fuse;
- Diagnose reason for low output voltages;
- Perform peak power tracking when power source is a solar array.

2.7 PACKAGING STUDY

In evaluating the 200-kW series-resonant inverter (SRI) design for space-based applications, the packaging design objectives remain essentially the same as in airborne applications; namely, efficient use of materials to minimize weight and volume impact, long-term reliability under all anticipated environments and a design that is producible and maintainable at reasonable cost.

The major differences in design approach result from the environmental factors. The launch and deployment dynamic loads associated with spacecraft missions are generally much more severe than airborne. Random vibration levels for launch are typically in the 10- to 20-grms range for large electronic equipment. The ambient pressure range, lack of gravity effects, and available thermal control methods associated with space operation are even more significant factors influencing the packaging of spaceborne electronics.

To achieve a reliable, efficient design requires a thorough understanding of the environmental effects on the equipment plus a comprehensive knowledge of circuit elements, materials and processes to be employed in packaging the SRI. Figure 2.7-1 shows the twin full-bridge power circuit evaluated for spaceborne packaging considerations.

The main packaging issues are thermal control, high-voltage protection, structural design, EMI control and power distribution and interconnection.

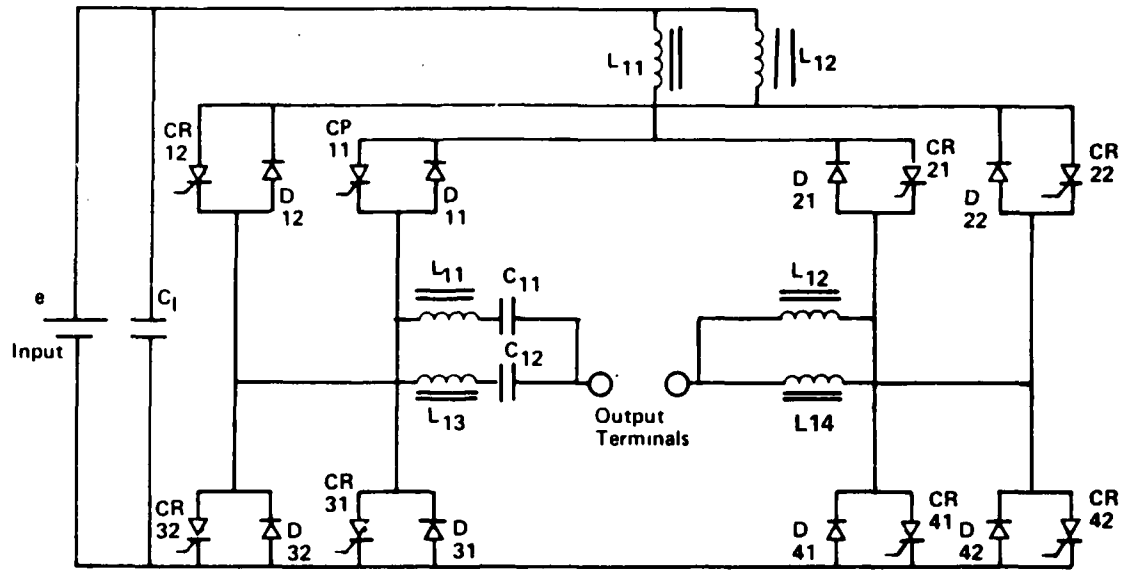


Figure 2.7-1 Power Stage Schematic—200-kW Twin Full-Bridge SRI

Table 2.7-1 lists the operational parameters assumed as representative of future space missions for the SRI.

Table 2.7-1 200-kW dc-dc Operational Parameters

Input Voltage	-	200 to 400 Vdc
Output Voltage, Frequency	-	250 V, 10 kHz
Output Power	-	200 kW Max
Power Dissipation	-	8000 W Max
Peak Voltage Stress	-	1000 V at the Series Capacitors
Operating Environmental Pressure	-	P 10^{-4} torr, or P 600 torr
Gravity Environment	-	1-g Prelaunch, Zero-g Postlaunch

2.7.1 Thermal Control

The concentrated heat loads dissipated in eight thyristor-diode pairs present a major challenge to the designer. For space operation, thermal conduction paths must be provided to transfer the heat generated from localized sources to a spacecraft radiator designed to efficiently reject thermal energy to deep space. Alternative systems may be used at the spacecraft level to utilize this waste heat in a thermal engine or to absorb thermal energy in an open-loop system, such as a boiler, with vapor ejected to space.

Several methods might also be devised for transporting heat energy from the SRI-localized sources to the spacecraft sink. The heat transfer analysis performed on the 200-kW inverter considered the use of heat pipes as the most efficient and effective method of heat transfer for this application. Heat pipes have been operated successfully as high-conductance devices in spacecraft since 1967. Recent space applications include Skylab, ATS-6 and the STS (space telescope system) scheduled for launch in 1986. Properly designed, heat pipes are considered a highly efficient, reliable method for heat transfer in space operations. The heat pipe uses a boiling-condensing thermal cycle with a small amount of vaporizable fluid contained in a closed tubular structure. Capillary forces pump the fluid to the evaporator where it absorbs heat and vaporizes. The vapor flows along the tube to the condenser section because of a slight pressure difference in that section where heat is rejected through condensation. The process is essentially isothermal except for temperature gradients through the heat pipe structure at the evaporator and condenser sections.

An alternative thermal control system for the SRI heat sources are active cooling loops. A suitable fluid used as a coolant, circulates by electrical pumping to transfer heat loads to the spacecraft sink. The Space Shuttle and Spacelab systems use active coolant loops and cold plates for thermal management of electronic components.

For either passive heat pipes or active coolant loops, thermal impedance must be minimized at mechanical interfaces for concentrated heat loads. For the SRI, maximum thermal flux density occurs at the thyristor contacts, which is estimated to be 26 W/cm^2. High contact forces and materials to enhance the effective contact area are required to produce acceptable thermal conductions. Similar techniques are required at cold plate interfaces for all major dissipators to maintain effective thermal control.

The 16 SRI power diodes and thyristors may be grouped in a 4x4 array with each device clamped to a common, electrically isolated cold plate base. The eight diode-thyristor pairs are electrically bused together on the cold plate base side using three separate conduction plates according to interconnection requirements of the circuit as shown in the schematic Figure 2.7-1. A similar arrangement is provided on the opposite side of the thyristor-diode pairs, with four groups of two pairs each connected electrically. Cold plates are attached to each thyristor-diode pair on the top side. Th s provides cooling from both sides of the disc-shaped semiconductors and facilitates assembly, test, and repair. This configuration would allow parallel arrays of heat pipes to be attached or embedded in the cold plates, each handling approximately 150 W, assuming four heat pipes per thyristor-diode pair.

The alternative active-coolant-loop scheme may be used in the same manner using suitably designed cold plates attached to coolant loops.

Associated inductors and capacitor banks designed for cold plate mounting may be supported on the cold plate base adjacent to or integrated with the semiconductor array. Additional heat pipes or coolant loops

will be required to accommodate the heat load associated with the inductors. The use of multiple heat pipes or coolant loops allows some redundancy without seriously complicating the design.

A dielectric thermal interface material such as fiberglass-reinforced silicon rubber sheet with beryllia or alumina filler is recommended as a candidate material for an interface between the semiconductors and aluminum cold plates.

The cold plates should be designed as an integral extension of the heat pipes or coolant loops to avoid an additional mechanical interface. This will provide a quasi-isothermal cold plate to reduce concentrated hotspots and improve the efficiency of the thermal control system.

Heat pipes have also been successfully integrated into power inductors and transformers to provide efficient thermal conduction paths and eliminate hot spots. In these cases the heat pipes have finned extensions that perform a structural function or act as electrostatic shields and are designed and fabricated into the magnetic assembly. The heat pipes extend from the assembly and are routed to appropriate cold plates or radiator surfaces.

Testing heat pipes in a gravity environment requires the heat pipes be reasonably horizontal to prevent gravity from influencing their capillary pumping ability. This can be accomplished by carefully routing heat pipe elements during design, limiting the array to a single plane, or by ensuring that departures from the plane are designed for a gravity assist during capillary pumping. This is important because inadequate return of condensate to the evaporator section will result in reduced thermal capacity or complete shutdown of the system.

2.7.2 Structural Design

Maximum efficiency will be achieved through using the cold plate component mounting base as the major structural element, with component inertial loads being carried through the cold plate directly to spacecraft supporting structural members. A lightweight vented enclosure designed for EMI control and protection from handling and debris will complete the housing.

Suitable enclosure construction may include formed aluminum sheet-metal covers, aluminum honeycomb constructions, or fiber-reinforced composite enclosures with foil metallization for EMI shielding. The secondary structures required to support the power control electronics and other low dissipating circuits, internal wiring, connectors, and shielding may be machined from aluminum stock and designed for structural continuity to the support base.

The component mounting cold plate with integral heat pipe elements can be considered an efficient plate structure because of its high specific stiffness, similar to corrugated construction. The relatively thick base sections required for thermal conduction can provide structural support to transmit loads to the spacecraft attachment points.

2.7.3 Spacecraft Integration

The obvious choice location for spacecraft mounting of the SRI to minimize weight and facilitate installation and ground testing is centrally on a dedicated radiator panel with the heat pipes routed in a planar array and connected to the radiator elements. In effect, the radiator elements become an extension of the inverter cold plate with heat pipes distributing the thermal load to produce a quasi-isothermal radiating surface.

System efficiency may be further improved by providing dedicated radiator panel elements to handle the heat load from the series inductors because they may be operated at roughly 80°C higher temperatures than the semiconductors. This will allow higher radiator flux densities with some associated weight savings.

For systems employing active cooling loops to remove heat from SRI components, the proximity of the SRI to the radiators is not a major consideration.

2.7.4 High-Voltage Considerations

To achieve reliable operation under widely varying conditions of ground testing and long-term space environments, the numerous factors influencing voltage breakdown in the SRI must be carefully considered. Provision must be made for controlling cracks and voids in insulation to avoid degradation and failure of insulation from partial discharges (Ref 9). The breakdown voltage of a uniform field gap in a gas can be plotted to relate the voltage to the product of gas pressure times the gap length. This is known as Paschen's law. Paschen's law has a minimum breakdown voltage for the critical pressure-spacing product. At 400 Hz the minimum breakdown for air is 327 V peak at the critical pressure spacing product (Ref 10). This voltage is called the corona inception voltage. The spacing and operating pressure must be controlled to ensure the corona inception voltage will not be exceeded (Ref 11). For air, the gas pressure electrode spacing product is 1 Pa-Cm (PASCAL-centimeter). For any pressure spacing product equal to 1 Pa-cm for a voltage of 327 V peak or greater, a glow discharge may occur. Although a glow discharge is not sufficient to cause breakdown, it can initiate the following breakdown sequence:

1) Glow discharge;

2) The glow discharge will slightly heat the surface causing further outgassing;

3) Particulates on the surface will induce surface tracking and eventual breakdown.

With the inverter operating voltages ranging up to 400 Vdc at the input and peak voltage stress of 1 kV at the series capacitors, it is apparent that appropriate high-voltage design practices must be used to prevent destructive corona and arc-overs.

The SRI is expected to operate outside of the corona region, i.e., at pressures close to atmospheric or in the hard vacuum of space at less than 10^{-4} torr. This simplifies the packaging design by allowing for a fully vented packaging approach while using the dielectric properties of air on earth or hard vacuum in space to avoid the electrical failures from voltage breakdown.

The vented design is also the lightest and least costly approach because the alternatives are for void-free dielectric encapsulation with grounded conductive outer surfaces to control voltage stress or to design and maintain a pressurized enclosure with dielectric fluids or gases as the insulating media. Both of these alternative approaches are necessarily more complicated and result in a significant weight increase over the vented packaging approach.

Other considerations for high voltage operation include:

1) Applying the usual electrode spacing rules for voltage breakdown in air;

2) Selecting dielectric solid materials for encapsulants, and adhesives, insulator bushings, standoffs, wire insulation, and thermal interface dielectrics that have been qualified as low-outgassing materials suitable for sustained operation at 200°C;

3) Eliminate or shield all sharp edges on protrusions from conducting surfaces to reduce electrical field stress (screw threads and wire ends are common sources of breakdown so rounded terminal and solder joint configuration should be used);

4) Considering nickel plate over aluminum or copper conducting hardware to maximize the voltage breakdown level;

5) Positive venting design techniques, including provisions for venting wire bundles, jacketed wire, connectors, stud-mounted parts that tend to entrap air in the clearance spaces, enclosed compartments and the overall housing, because unless specific venting measures are taken throughout the assembly, the desired low-pressure operating region may be unattainable within reasonable time limits;

6) Separate low voltage control circuitry from the high-voltage elements using appropriate electrostatic shielding techniques;

7) Applying void-free conformal coating on exposed high-voltage conductor surfaces wherever practical to reduce the possibility of surface breakdown from contaminants and electrical assembly debris;

8) In using insulation materials, the thickness should keep the maximum voltage stress from exceeding 10% of the actual breakdown voltage (this derating factor is used to account for material properties degradation under long-term voltage stress plus aging effects).

The packaging considerations for high-voltage design stated above are basic for high reliability in the design. Additional factors to consider are to be found in recent NASA and DOD guideline publications on spacecraft high voltage equipment design.

2.7.5 Connectors

Conventional multiwire connectors may be used for control and monitor circuits at the SRI interface but are not advisable for the main power input/output interfaces because of the current density and high voltage considerations. Standard MIL-SPEC connectors are designed with environmentally sealed plug and receptacle elements that entrap air and, in space vacuum, will eventually reach critical pressure causing corona breakdown.

A simpler approach would be to use threaded insulated terminals, sized to handle the current load and fitted with corona suppression caps or cap nuts.

2.7.6 Size and Weight

Using preliminary design data and assumptions on the packaging approach to be used, a size and weight estimate was performed. The results are presented in Table 2.7-2 and represent an estimate considered achievable with present technology for a space-based 200-kW inverter.

Table 2.7-2 Size and Weight Estimates

Components	Weight, kg	Remarks
Thyristor and Diodes	3.6	Vendor Data
Input Filter Capacitors	3.6	Estimate Including Supporting Bracketry
Series Capacitors	1.5	Estimate Including Brackets
Series Inductors	9.0	Assumes Integral Heat Pipe Cooling
dv/dt Coils	5.0	Estimate Without Heat Pipes
Control and Monitor Circuits	2.0	Estimate
Conductors and Connectors	3.7	Assumes Aluminum Plate and Rod Busing for High-Current Conductors
Subtotal, Electronics	28.4 kg	(62.6 lbs)
Base Structure	11.4	Assumes 50% Solid Structure with Integral Heat Pipes or Coolant Loops
Enclosure	3.6	
Miscellaneous Fasteners	1.3	
Subtotal, Structure	16.3 kg	(35.9 lb)
Radiator	85.0	Assumes 13.9 m^2 (150 ft^2) at 6.1 kg/m^2 (1.25 lb/ft^2)
Heat Pipes	24.0	Assumes 44 heat pipes at 20 mm diameter and 1.3 m mean length. Includes 3.4 kg for associated cold plates not covered elsewhere. Heat pipe sp. wt. = 0.36 kg/m
Subtotal, Thermal Control	109.0 kg	(240 lb)
TOTAL SRI SYSTEM WEIGHT	153.7 kg	(339 lb)
Specific Weight at 200 kW	1.7 lb/kW	
Size Estimate		
SRI Assembly	15x46x71 cm (6x18x28 in.)	
Radiator	13.9 m^2 (150 ft^2)	

2.8 THERMAL STUDY

The 200-kW dc-dc dual-bridge SRI was studied. The study was limited to the power components and excluded the high-voltage transformer, high-voltage capacitor, and output rectifiers. A 100% duty cycle was assumed. Cold plate requirements at semiconductor interfaces and heat pipes for heat transport were considered.

The power dissipated during operation must be transported away from the electronics and the maximum internal and junction temperatures must be controlled. The ultimate heat sink is deep space and the thermal energy will be transferred to it by radiation. The following assumptions were made:

1) A radiator with high emissivity, E greater than 0.95;

2) The view factor to space is 1.0;

3) Max allowable semiconductor junction temperature is 125°C.

Each diode thyristor pair is estimated to dissipate 625 W. A study was performed to find the radiator area as a function of radiator power dissipation and temperature. The results of this study are shown in Figure 2.8-1. The figure shows that as the radiator temperature increases, for constant power dissipation, the radiator area decreases.

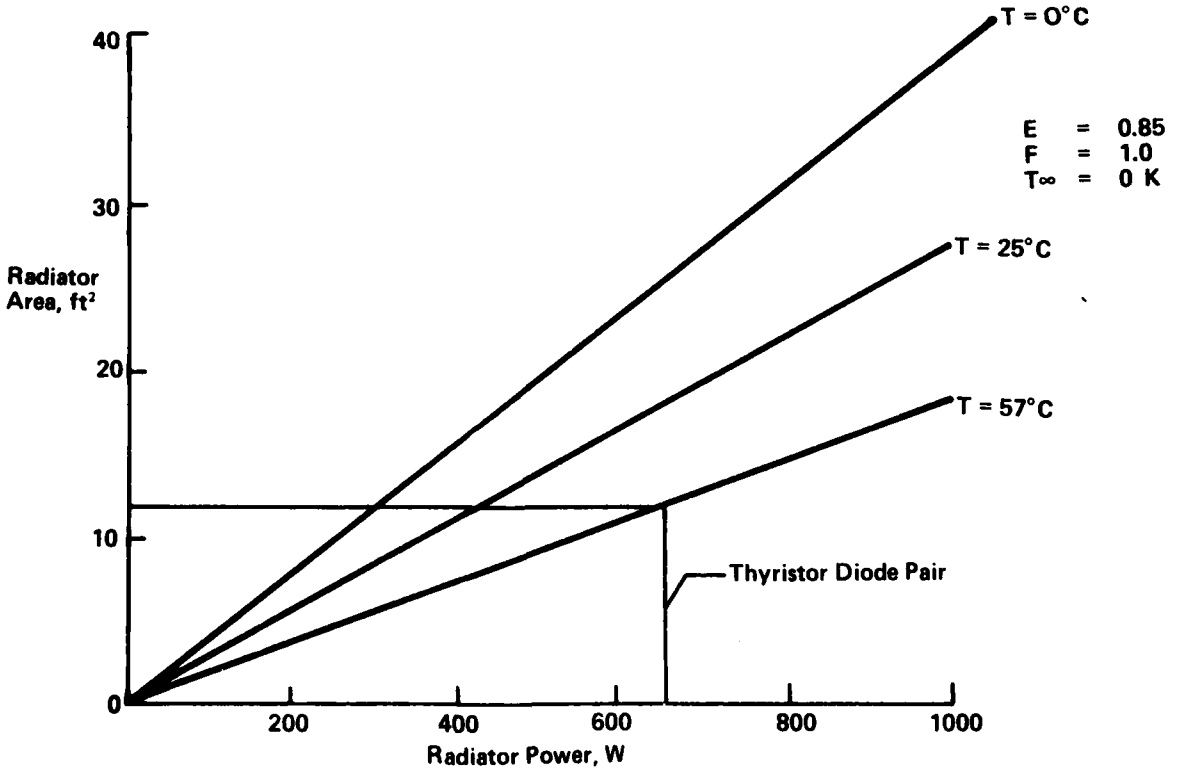


Figure 2.8-1 Radiator Area as a Function of Power Dissipation and Radiator Temperature.

Assuming the maximum allowable junction temperature to be 125°C, a typical thermal gradient between the thyristor and radiator is calculated to be 68°C, so the radiator temperature is 125 - 68 = 57°C.

For a thyristor diode pair dissipating 625 W and the radiator at 57°C then, approximately 12 ft^2 of radiator area are required as the figure shows.

The major power dissipators are the thyristor diode pairs--eight pairs, 625 W/pair, or 5000 W total for the eight pairs. Thermal gradients and weight can be minimized by the use of heat pipes. To illustrate the weight savings of using a heat pipe as compared to a solid aluminum conductor, the weight of an aluminum conductor transferring 300 W with a 30°C gradient was calculated and compared to the weight of a heat pipe. Figure 2.8-2 shows the results. For a 30-in. length, the solid aluminum conductor would weigh 200 lbs compared to 3 lb for a heat pipe.

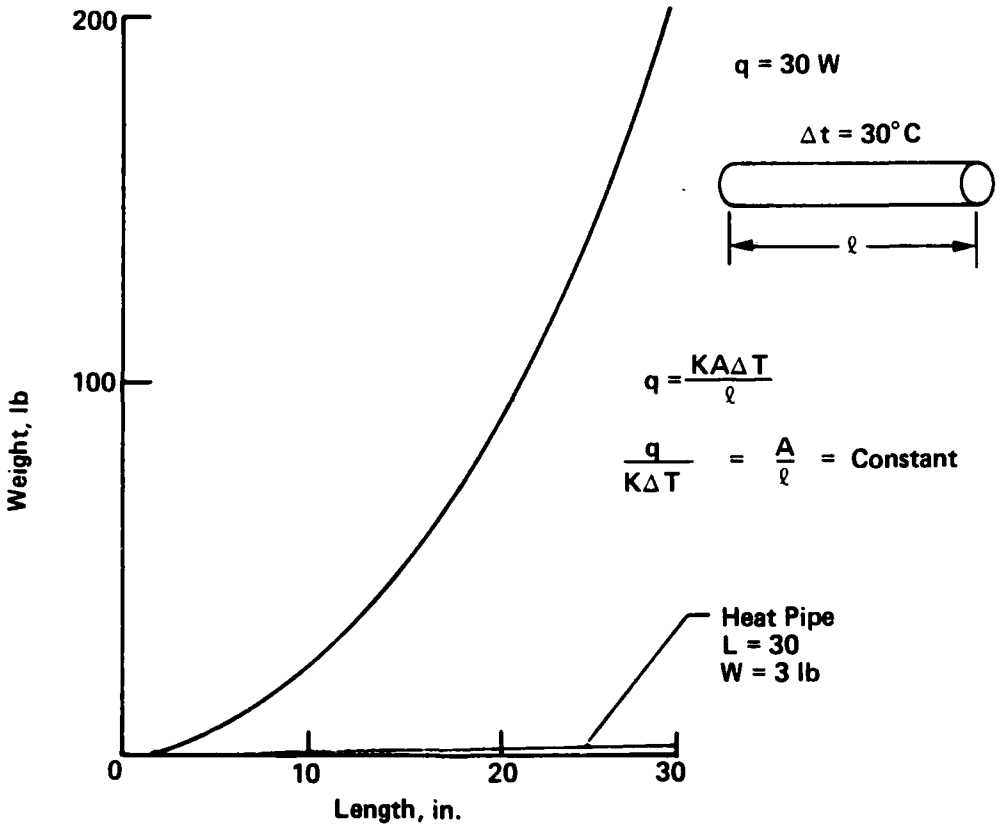


Figure 2.8-2 Aluminum Conductor and Heat Pipe Weights As Function of Length

Figure 2.8-3 shows the thermal configuration of the SCR diode pair. The SCR and diode are connected by the two cold plates. Both sides of the SCR diode pair must be electrically insulated from the heat pipes.

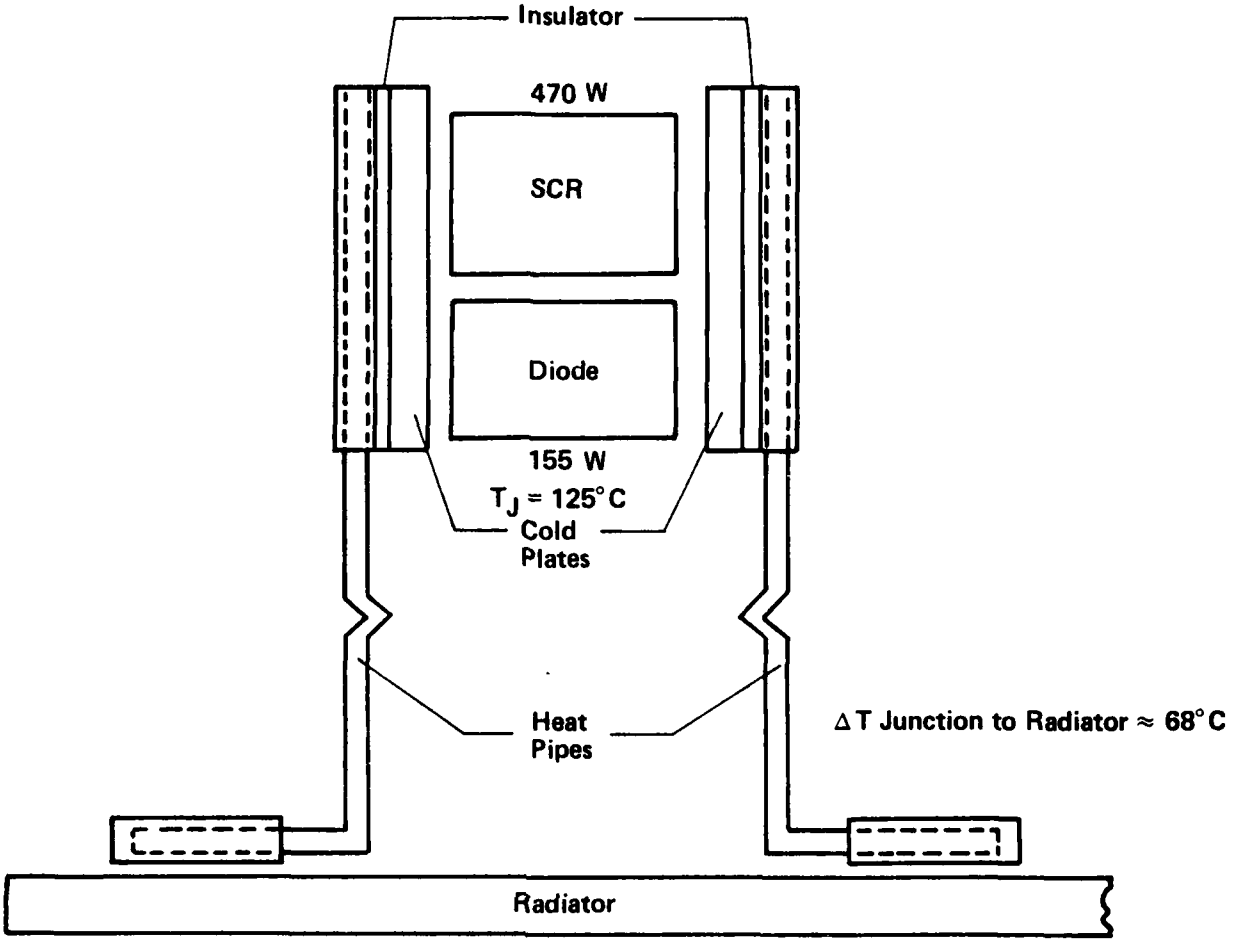


Figure 2.8-3 SCR Diode Thermal Configuration

A parametric study was performed to investigate the relation between radiator temperature, radiator area, and the number of heat pipes for one SCR diode pair. Figure 2.8-4 shows the results. If two heat pipes per pair were used, then the radiator would be at 57°C and each pair would require approximately 12 ft^2 of radiator area. At the other extreme, if nine heat pipes per SCR diode pair were used, or the SCR diode pair were mounted on the radiator, the radiator would be at 87°C and each pair would require approximately 8.3 ft^2 of radiator.

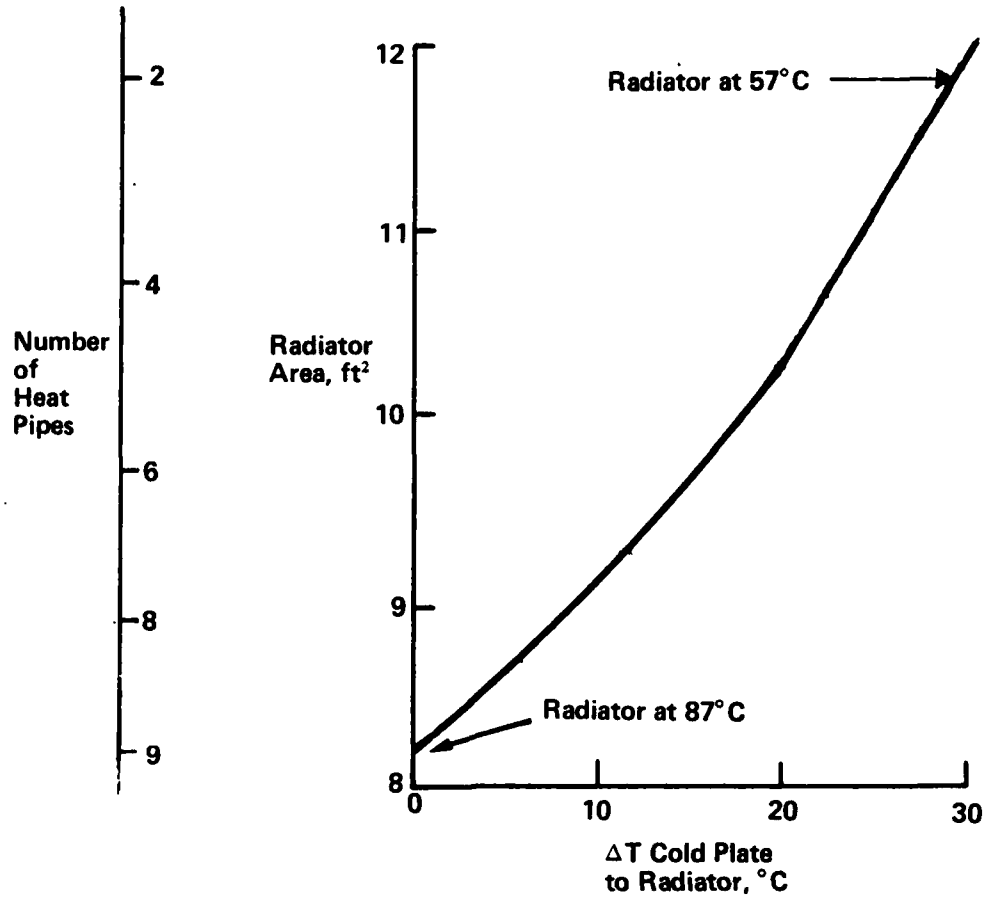


Figure 2.8-4 SCR Diode Thermal Parametric Study

In conclusion, the thermal analysis in this study examined individual parts and determined what is required to maintain the parts within their respective temperature limits.

On a system level the design could be optimized by using several different cold plates in the spacecraft. The different plates should operate at different temperatures and also some plates should be made of electrically nonconductive material. For proper thermal management, the parts should be mounted on the various plates according to their temperature limits and their electrical isolation requirements.

The study showed that for ideal conditions, 150 ft^2 of radiator area would be required to dissipate 8 kW thermal. As one goes from ideal to a real set of conditions, the required radiator area would be expected to increase.

The analysis also shows that a potential way to reduce the radiator size and spacecraft weight is by using heat pipes to transfer the heat from the cold plates to the radiator. The number of heat pipes per plate should be determined by the desired temperature of cold plate and by the reliability of the heat pipes.

3.0 PHASE II FABRICATION AND TEST TASKS

3.1 DETAILED DESIGN

Each of the functional blocks has been designed in accordance with functional design criteria outlined in section 2.4 and custom part specifications detailed in section 2.5. In addition, the following design rules were established to maintain compatibility between the functional blocks to provide maximum flexibility in configuring existing and future SRI topologies; 1) compatible with 15V CMOS logic, 2) good power supply isolation, 3) high input noise immunity, 4) minimum number of interconnects between functional blocks.

3.1.1 Firing Pulse Generator

3.1.1.1 Background--Results of the study to reconcile conflicting requirements of SCR gate drive, MOSFET gate drive, and bipolar transistor proportional drive indicated that a single circuit designed for all three functions could not be optimized for any one drive. Ref. paragraph 2.5.1.1. The final design criteria is based on driving SCRs with provision for driving transistors with additional circuitry that are external to the hybrid package. Schematics are shown for possible interface circuits which could drive MOSFET and bipolar transistors. Actual interface circuitry will be dependent on the particular power devices chosen and these circuits are presented as examples of typical arrangements.

3.1.1.2 Detailed Design--The FPG hybrid is a quad solid state power switch with integral protection diode and uncommitted emitter and collector terminals for flexibility in designing output circuitry. Up to four FPG inputs may be driven directly from a single 15V CMOS logic gate. The FPG is used to drive amplifying gate SCRs for the AIT SRI controllers. Circuit components which are external to the hybrid must be chosen for each particular SRI design, since di/dt, dv/dt, and other SCR device characteristics dictate pulse generator design.

Design for the FPG circuit card is as follows. Resistor R1 was selected to limit base drive current to output switch Q3. Resistor R2 is sized to charge capacitor C1 within the minimum idle time of the SCR, or 50 microseconds. C1 has been selected to supply a minimum of 30 microjoules of gate energy in each firing pulse. The transformer isolates logic common from the resonant voltage which may swing 700 or 800 V p-to-p. The windings are spaced a minimum of 0.13 in. apart to provide high voltage withstand capability and have small interwinding capacitance. Leakage inductance is relatively high due to the winding configuration, but the resonant frequency of primary leakage inductance with C1 is sufficiently high to provide adequate rise time for the gate firing pulse. Rise time for the firing pulse for the AIT SRI controllers is 1 microsecond to 15 V open circuit seconding voltage. Total "front-stop" time is 3 microseconds and "back porch" is maintained through the resonant power half cycle, or 47 microseconds. Rectifier CR1 is required to block flyback voltage produced by the isolation transformer from the SCR gate terminal. Resistor R3 and capacitor C2 sharpen the leading edge of the firing pulse to about 300

nanoseconds when firing Westinghouse T507 type SCR devices which exhibit a turn-on voltage of 4 to 5 V. Turn-on is about 400 to 500 nanoseconds when firing GE C149M15 SCRs. Components C3 and R4 reduce source impedance at the gate so that reapplied voltage dv/dt may be increased and snubbing loss reduced.

3.1.1.3 Circuit Schematic--Firing Pulse Generator

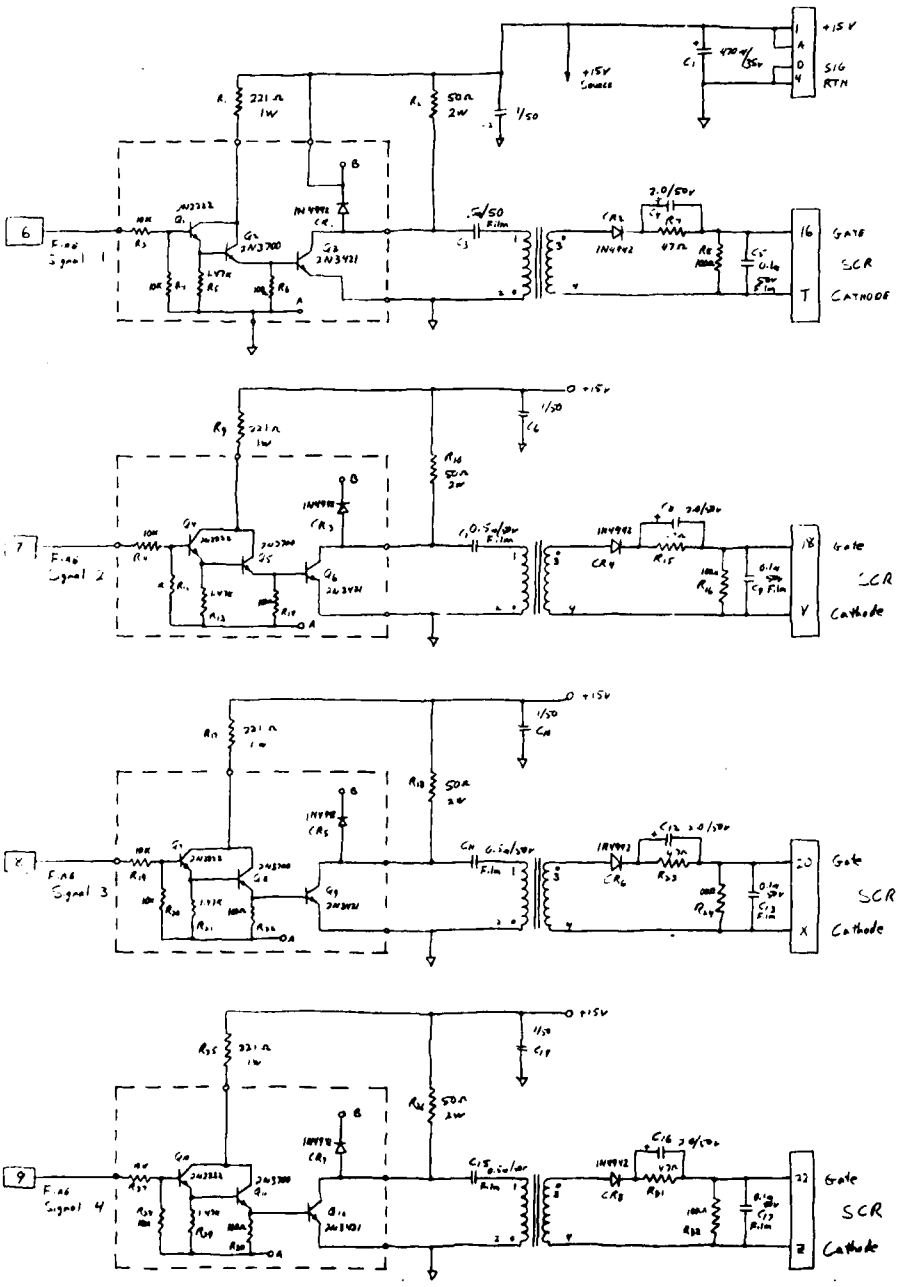


Figure 3.1.1-1 Firing Pulse Generator Schematic

3.1.1.4 Theory of Operation--One quad FPG hybrid is used on each FPG circuit card. The 200 kW twin full bridge SRI controller uses two of these cards, the 5 kW ac-to-dc converter uses three cards and the 10 kW half bridge SRI uses two sections of one FPG. The fire command line is held low during charge of the energy limiting capacitor and is derived from BBS timing by the protection circuit. A "true" fire command, generated by the protection card is used to produce the sharp leading pulse. Total pulse width is determined by pulse forming components C1 and T1 and the SCR gate characteristics. The power switch is held on during the entire conduction period of the SCR.

3.1.1.5 Device Ratings--Device ratings conform to manufacturers data sheet specifications, except for the following:

1) Q1, Q2, Q3 power dissipation derating is 0.3;

2) Q3 peak collector current is 3.0 amps;

3) Total hybrid dissipation is 680 mW.

3.1.1.6 Application Information--The FPG hybrid may be used to drive SCRs with minimal interface circuitry which is comprised of energy limiting components and pulse forming components. These components must be chosen for the particular application and device type. Data for designing these two networks are available from manufacturers of power SCRs, with Westinghouse and GE data used for the AIT program. Drive of MOSFET transistors may also be accomplished with minimal interface components. The simple interface shown in the following paragraphs uses only passive components, while tighter control of rise and fall rates may require more sophisticated designs. Interface to high power bipolar transistors such as the D60T and D7ST generally will require rather sophisticated circuitry.

SCR Drive--Resistor R1 is selected to limit maximum base drive current to the 2N3421 output switch. The FPG is configured in the AIT SRI controllers for a capacitive discharge forward transfer pulse generator. Resistor R2 is selected to fully charge C1 within 1/2 cycle of the resonant frequency. Faster charging may be accomplished by an active constant current charge device, if required. C1 is chosen to limit gate energy transferred to the SCR. Some of the energy is dissipated by the gate pulse forming components, C2, C3, R3, R4, CR1 and the isolation transformer and must be accounted for.

Pulse forming is controlled by C1, C2, C3, T1, R3, and R4. C1 and T1 leakage inductance form a resonant circuit that may limit the pulse rise time. Isolation transformer flyback current is blocked from the SCR gate by CR1 and returned to the supply by the hybrid internal diode. Resistor R4 and capacitor C3 are used to lower gate input impedance for increased dV/dt capability. These components reduce the pulse rise time and so components C2 and R3 are added to recover the leading edge. The rise time of the pulse leading edge has a strong effect on di/dt capability of the SCR and manufacturer's data should be consulted before component calculations are made.

MOSFET Drive--The power MOSFET transistor is a charge driven device and switching times should be controlled by the drive circuit since the device cannot inherently provide this control. The rise time should be controlled in an SRI to eliminate the possibility of simultaneous conduction of the series connected power switches. Simultaneous conduction would result in excessive power dissipation and possible damage of the MOSFET transistors. Current spikes also could produce unwanted ringing, EMI, and control difficulties. The rise time of the MOSFET also should be longer than the reverse recovery time of the output rectifiers so that primary current is continuously coupled to the load to reduce production of noise.

Additional current rate of rise limiting may be provided by the series resonant tank circuit. Parasitics in the power circuit, however, may negate benefits that would be expected from the resonant current characteristic, due to ringing caused by wiring reactance and transformer and inductor self-oscillation. Saturating inductors placed very close to drain or source terminals of the MOSFETs may also help to control rise time switching transients.

During turn-off, energy stored in wiring stray inductance will cause voltage spikes with amplitudes directly dependant on turn-off time. A snubber may be required to limit the magnitude of the voltage spikes. Power dissipated may be minimized by a fast turn-off time. A properly designed MOSFET drive circuit should provide controlled turn-on time and a very fast turn-off time. Maximum efficiency of a MOSFET SRI may be realized with proper coordination of switching time control between the power circuit, snubbing, and drive circuits.

3.1.1.3 Block Diagram--Figure 3.1.1-2 is a block diagram of the FPG with interface circuitry to a power MOSFET. The transformer provides isolation between logic ground and the high voltage power circuit.

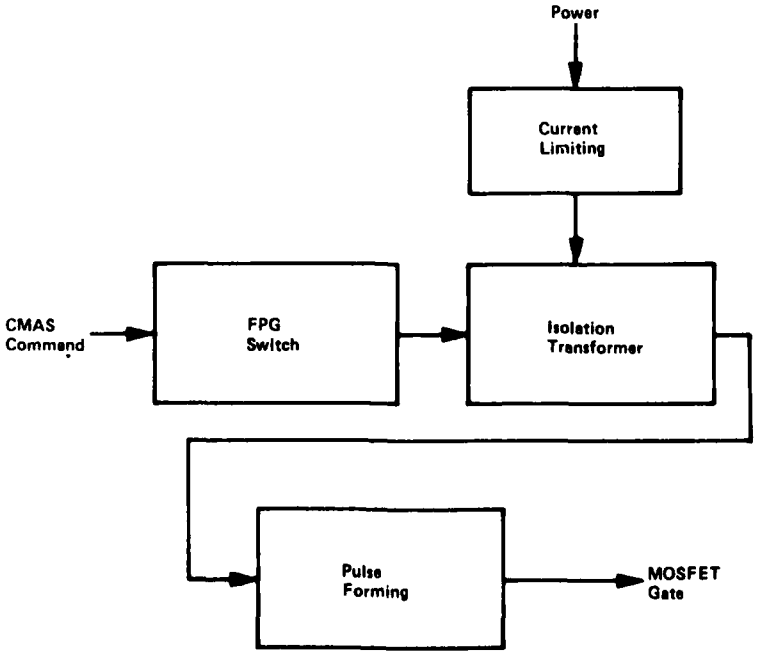


Figure 3.1.1-2 FPG/MOSFET Drive Block Diagram

3.1.1.4 Circuit Diagram--Figure 3.1.1-3 shows a circuit diagram for a simple MOSFET drive using the AIT FPG to supply gate drive charge current. The circuit provides a controlled rate of rise by linearly increasing gate voltage. The rise time is determined by constant current drive from the isolation transformer charging the parallel combination of the external gate capacitor, C and transistor input gate capacitance. The relatively large C will also minimize the effects of variations of Cgs and feedback from Cdg. The zener provides gate overvoltage protection from drive, stray inductance, and Cdg feedback from the drain.

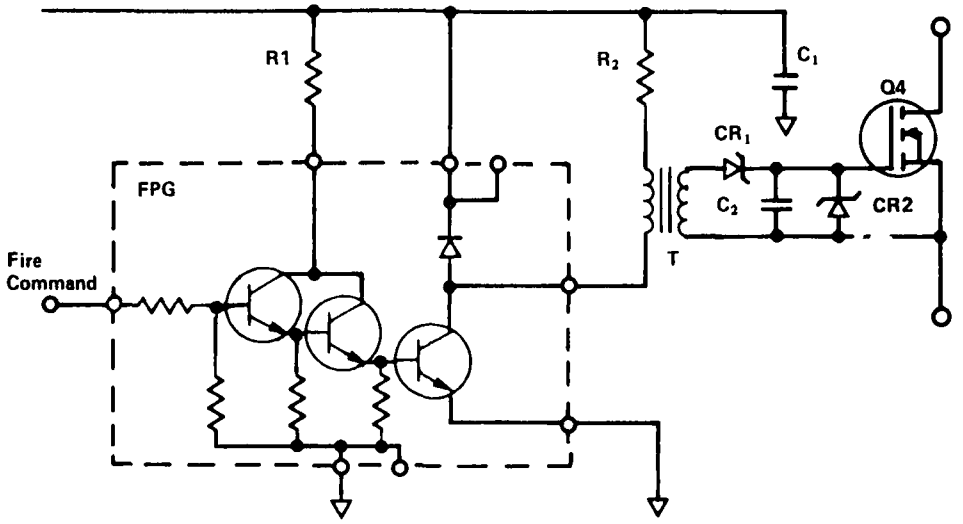


Figure 3.1.1-3 MOSFET Drive Schematic

3.1.1.5 Parts List--The parts used for the MOSFET drive circuit are summarized in Table 3.1.1-1.

Table 3.1.1-1 FPG/MOSFET Drive Circuit Parts List

Reference Designator	Description	Part Number
CR1, CR2	Zener Diode, 15V	1N4469
U1	FPG Hybrid	850AT400001
T1	Drive Transformer	2213P-600-3B7
Q4	MOSFET	2N6765

3.1.1.6 Bipolar Transistor Drive--The bipolar transistor is a current driven device and this drive current must be continuously supplied during the entire conduction period. The SCR drive requires only a start pulse which must last 1 to 5 microseconds and likewise, the MOSFET drive is required for only a short duration to charge the gate capacitor. Average power to drive SCRs and MOSFETs is an order of magnitude, or more lower than that required for a bipolar transistor driving an equivalent load. The drive circuitry is also more complex. Base drive interface circuitry must provide three functions:

1) Turn-on current pulse,

2) Proportional feedback base current drive, and

3) Turn-off pulse.

The interface circuitry necessary to drive a high current bipolar transistor such as the D60T must provide high base current drive to start conduction and must also supply a continuous holding current to the base during the entire conduction period. Additionally, a high-current turn-off pulse must be provided to sweep the base-emitter charge from the device to ensure collector turn-off before forward voltage is re-applied.

Design of a base drive circuit to interface the FPG hybrid to a D60T transistor was not attempted during this program. Requirements have been identified and a block diagram of circuit functions is shown. In Ref. 6, Robson and Hancock developed base drive circuits for the SRI using D60T and D7ST transistors. In their report, turn-on pulse requirements for proportional drive are listed.

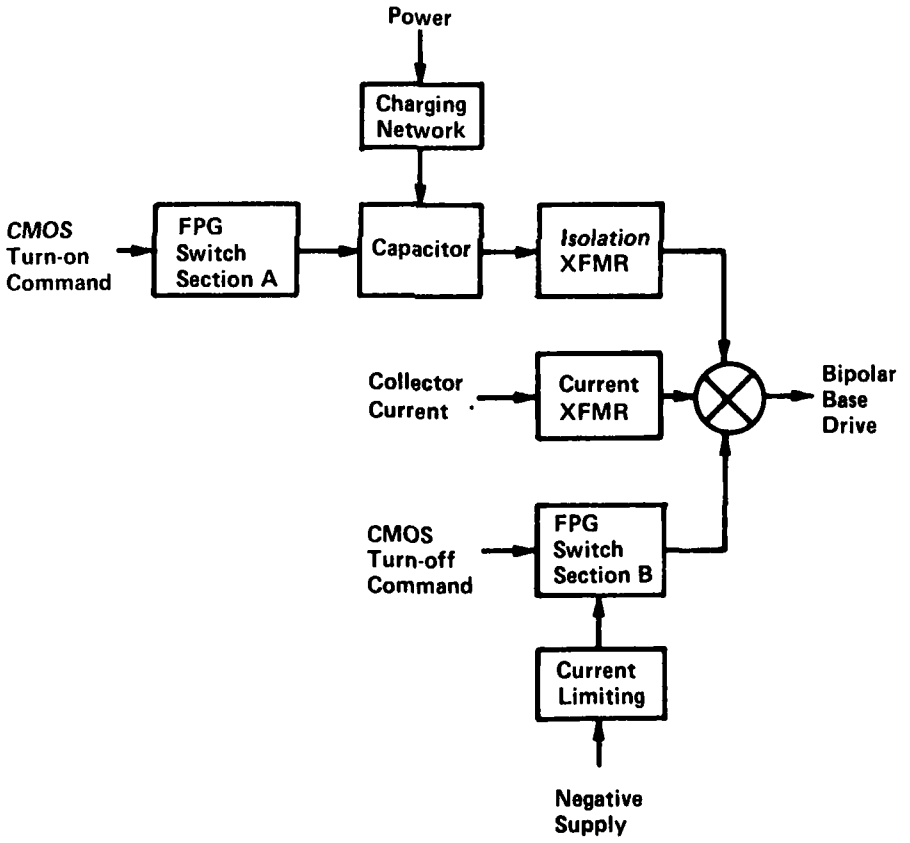


Figure 3.1.1-4 FPG/Bipolar Transistor Base Drive Block Diagram

3.1.1.7 Performance Data--Switching time is less than 300 ns, which should make this device useful for SRI application to 100-kHz. Device dissipation should be calculated to determine thermal capability of the packaging.

3.1.1.8 Packaging--The hybrid package chosen for the quad FPG is oversized to allow much larger thermal dissipation than is required for the AIT controllers. This was done as a conservative measure based on possible test circuit overstress. Increased packaging density for flight hardware could be accomplished from existing photographic artwork.

3.1.2 Back Bias Sensor

3.1.2.1 Background--For the three SRI converter topologies under study, SCR reverse bias detection provides a critical timing function to the control and protection circuits. Back bias is necessary to ensure sufficient SCR recovery time (Tq) before reapplication of forward voltage. Failure to meet the Tq requirement will cause a bus short and possible damage to the power converter. Sensing zero anode current flow is insufficient to determine device recovery. Recovery time is guaranteed only when reverse voltage is applied to the SCR. The BBS output is true only when reverse bias exists above a presettable threshold voltage.

3.1.2.2 Detailed Design--Baseline design requirements are listed in section 2.5.2.2. One requirement was changed after functional testing was begun. Threshold voltage range was expanded from -0.2 -0.4 to -0.1 -1.0 V. It was discovered that a lower threshold voltage reduced the circuit delay time when resonant circuit input-to-output voltage q approaches unity. This condition exists at full power output and low line voltage input, an operating point which requires minimum control angle (maximum switching frequency) to sustain full output voltage. Increasing the BBS threshold level to 1 V appeared to be an advantage in controlling the 5 kW three-phase ac-to-dc converter, since SCRs are used as antiparallel diodes and have initial forward voltage drop of about 5 V. SCRs turn on much slower than conventional diodes and this allows the resonant circuit to run in an unclamped mode for 1 to 2 microseconds. In this unclamped mode, the SCR snubbers provide the only damping for power circuit parasitic ringing and noise. A threshold level of 0.5 V provided an optimum compromise between delay response and noise immunity. The control unit provided reliable control for all SRI power stages when detection level was set to approximately 0.25 V.

3.1.2.3 Circuit Schematic--Figure 3.1.2-1 shows the schematic of the back bias hybrid. Rsit and Rattn are external to the hybrid and are selected for particular device application by the designer. Three jumper points are used to select either positive or negative voltage with respect to return. Section 3.1.2.6 explains use of these application functions.

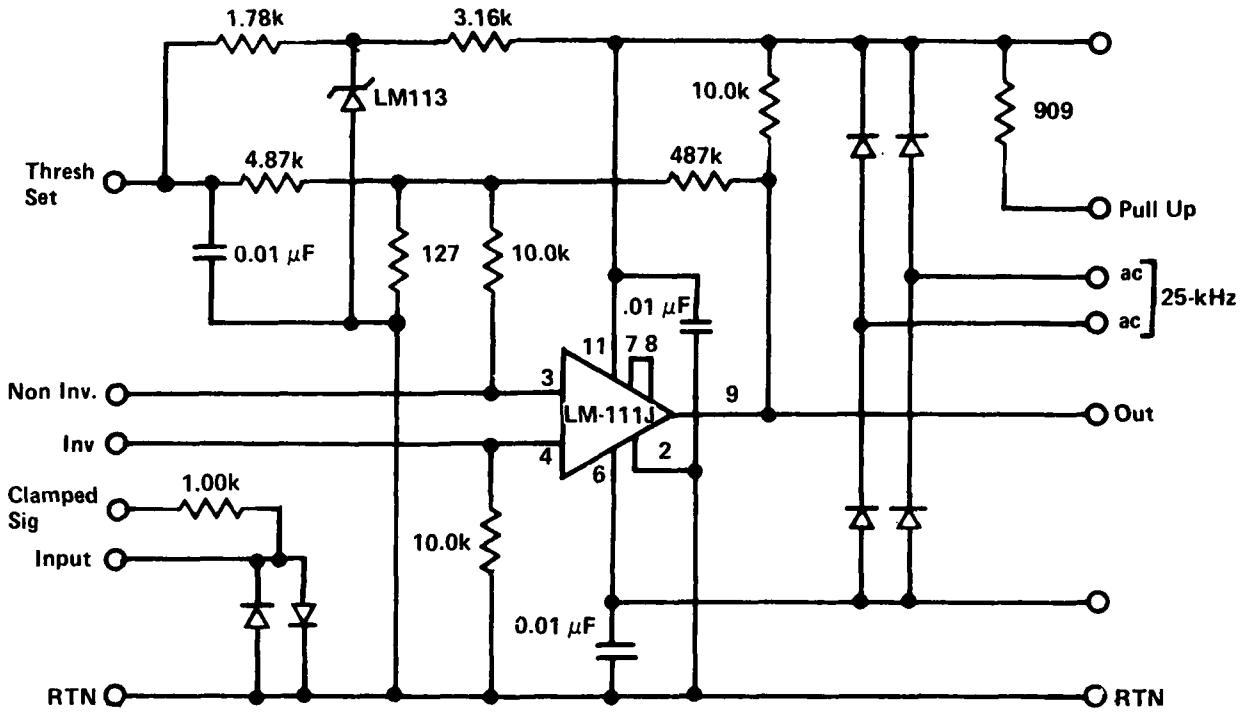


Figure 3.1.2-1 BBS Hybrid Schematic

3.1.2.4 Theory of Operation--Theory of operation is explained for the BBS circuit card, which includes all circuitry in the BBS hybrid, range setting components, the 25-kHz ac isolation transformer, the output circuit optocoupler, and logic level shifters.

SCR reverse bias is detected by connecting the BBS input lines to the Anode and Cathode of the SCR. The BBS return must be connected to either the positive or negative supply, which is the anode of the positive SCR and the cathode of the negative SCR. Voltage across each pair of SCRs is attenuated by R1 and R20. The input of the hybrid is protected from high power circuit voltages by back-to-back clamping diodes. The attenuated voltage is applied to either the inverting or the noninverting input of an LM111 high speed comparator by selection of jumper A. This voltage is compared to a stable reference which is derived from an LM113 band gaμ precision reference chip. Back bias voltage that exceed the threshold magnitude will cause the comparator output to turn on. Output current from the comparator is limited by a 909 ohm resistor and used to drive the input to a 6N134 dual high speed optocoupler. The five volt output signal from the optocoupler is converted to CMOS logic by a constant-current, two-stage level shifter.

The two BBS circuits are electrically separated by a potential equal to the supply voltage. These functional elements are isolated from the housekeeping power supply by 25-kHz transformers. High frequency ac power is produced by a housekeeping power supply which is common to a control card cage and can supply power to 12 BBS hybrids. Electrical isolation from logic common is accomplished by light coupling through dual optocouplers.

A design goal of 1 microsecond total circuit delay is budgeted as follows. The LM111 comparator delay is 500 ns for 3 mV overdrive and a 10 V swing. Delay caused by the 6N134 is approximately 90 ns. Delay through the level shifter is 200 ns. Delay caused by passive components was approximated by using a computer simulation program called "ECAP". Circuit gain was flat out to 220-kHz and down 6 db at 1 Mhz. Phase remained at -180 up to 50 kHz and increased to -120 at 1.5-Mhz. Total circuit delay in applications up to 100-kHz is typically 800 ns.

3.1.2.5 Device Ratings--Input levels applied to the comparator must follow National Semiconductor data for the LM111 chip. Total average input current to hybrid pin 9 must not exceed 20 mA. Maximum voltage difference between positive and negative power section supplies must be within the ratings of the H.P. 6N134 optocouplers. Ac power applied to the isolation transformers must be 14.0 +/- 1.0 Vac p-p at a frequency of 20 kHz to 40 kHz. The square wave applied to the transformer must have a leading edge rise time of at least 100 ns so that ringing and spike noise will not become a problem as a result of diode switching time. Maximum output signal source drive current is 5 mA and maximum sink current is 20 mA.

3.1.2.6 Application Information--BBS Threshold Level - Two resistor values may be changed to set the threshold level, the threshold setting resistor which is connected to pin 4 of the hybrid and the signal input attenuation resistor which is connected to pin 9 of the hybrid. Generally the input attenuator is selected for minimum dissipation but must be sized so that maximum current input to hybrid pin 9 does not exceed 20 mA. For the 600 V dc-to-dc converters, this input current is 1.6 mA.

The simplified schematic of the comparator circuit (Fig. 3.1.2-2) is used in conjunction with the two equations listed to determine input current limiting and voltage threshold setting resistor values.

[1] Equation for Calculation of Rattn -

$$Rattn = V(supply) / I(in)$$

where:
V(supply) is the SRI power module maximum supply voltage.
I(in) is the input current to pin 9 of the hybrid.

Example:

For I(input) = 1.6 mA (Input current to pin 9)
V(supply) = 600 V (Back bias detection level)

$$Rattn = 600\ V / .0016\ A = 375{,}000\ ohms$$

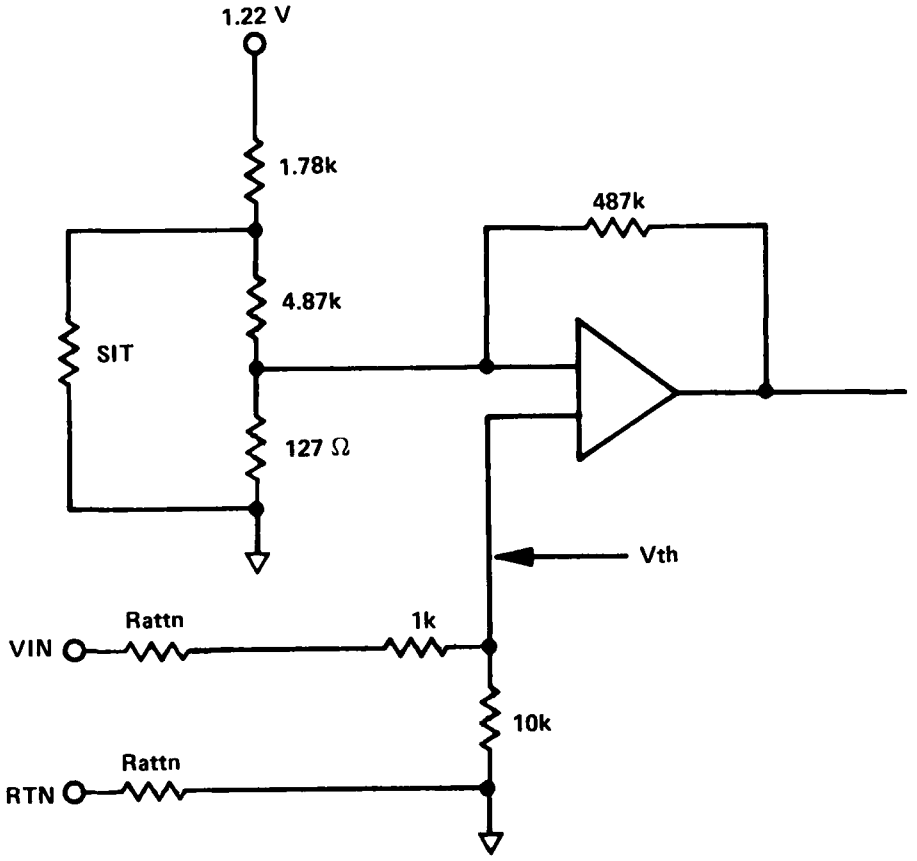


Figure 3.1.2-2 Simplified Schematic of BBS Input Circuit.

[2] Equation for Calculation of Vth

$$Vth = V(in) \times 10k / (11k + Rattn)$$

where:
Vth is the comparator threshold voltage.
V(in) is the back bias signal detection voltage.

Example:

For V(in) = 0.25 volts

$$Vth = 0.25 \times 10k / (11k + 375k) = 6.48 \text{ mV}$$

[3] Equation for Calculation of Rsit

$$Rsit = 39350 \times Vth / (.685 - 14.23 \times Vth)$$

where:
Rsit is the threshold voltage setting resistor connected between pin 4 of the BBS hybrid and ground.

Example:

$$Rsit = 39350 \times .00648 / (.685 - 14.23 \times .00648) = 430 \text{ ohms}$$

BBS Voltage Sense Polarity--For a negative sensor, point A (hybrid pin 10) is connected to the noninverting input of the comparator (pin 6) and for a positive sensor, point A is connected to the inverting input (pin 7).

Noise Reduction--A small capacitor may be connected between the inverting and noninverting pins of the comparator (pins 7 and 6, respectively) to increase noise immunity. Typical capacitor range is 100 pF to 1000 pF. Noise immunity may be improved using this method with only small additional circuit delay.

Input Connection to the Power Converter--The return line of each BBS hybrid (pin 8) must be connected to either the positive or negative supply of the power section. If the BBS return line is connected to an active SCR terminal, the BBS will be toggled at the SRI switching frequency and normal BBS operation will be lost. The active terminal from the SRI power converter section must be connected to the attenuation resistor which is wired in series with hybrid pin 9.

3.1.2.7 Performance Data--Maximum switching frequency of the SRI is dependent on delay in detecting SCR reverse bias voltage. The three converters under study are switched at a maximum 10-kHz and SCR recovery time is 10 microseconds. Total circuit delays in the BBS, PU, TPU, and FPG must total less than 10 microseconds for control to be successful. A program goal of 1 microsecond total delay time in the BBS circuitry became a design requirement for 100-kHz operation. Functional testing was run to 100-kHz using a 1-kW scale model SRI. Since the SCR power switch could not be expected to operate at this

frequency, the power stage was driven by a wide band power amplifier. Figure 3.1.2-3 is an oscillograph of the BBS output waveforms. Input wiring and protection circuit loading was not changed for this test.

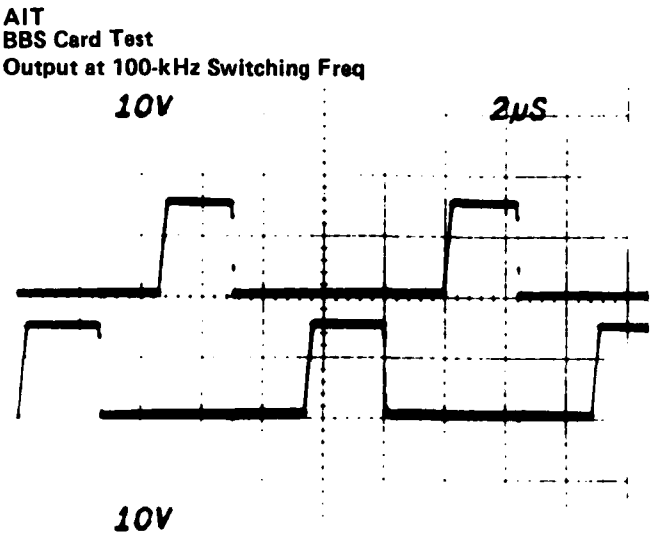


Figure 3.1.2-3 Oscillograph of the BBS Output Waveforms.

3.1.2.8 Packaging--Packaging area density of the BBS hybrid is approximately 25% and volumetric density is less than 10%. The BBS microcircuitry could be repackaged in a much smaller footprint and lower profile package for flight use, using existing designs. Further reduction in packaging volume could be realized by replacing screened resistors with chip components.

3.1.3 Protection Unit

3.1.3.1 Background--The protection unit (PU) is divided into three logical sections, analog protection, digital timing, and start function. The function of each is described as follows.

Analog Protection--monitors line input voltage, converter output voltage, and capacitor voltage of both resonant capacitors. It also generates a status signal for the front panel fault displays, and isolates the output voltage analog signal which is used by the control circuit.

Digital Timing--prevents simultaneous conduction of series connected power switches, provides timing to maintain power converter oscillation, and provides handshake interface with the control unit and three phase unit.

Start Function--provides initialization of digital logic and generates a fire pulse to initiate power oscillation. The start function is integrated into the digital timing circuit.

Some new issues were encountered in preliminary functional testing and additional requirements were added to the original top-level requirements outlined in the phase I study task. These requirements are:

1) The converter must not shut down due to a missing BBS pulse.

2) Transients on the BBS signals must not interfere with normal digital control timing.

3) Three phase transition must not occur due to power line transients.

4) SCRs used as diodes in the three phase ac-to-dc converter must be fired at or before zero current crossing to prevent excessive power dissipation in snubber circuits.

These requirements are discussed under detailed design, section 3.1.3.4.

3.1.3.2 Theory of Operation--The protection unit hybrid is physically divided into two sections, the analog protection unit and the digital timing section. The two physical protection unit sections are logically interconnected by three interface signals, analog protect, OVP, and resonant capacitor polarity status. Each logical section will be discussed separately.

Analog Protection--The analog protection circuitry provides continuous monitoring of these four parameters and generates status signals for output "overvoltage protection" and "analog protection." A third output from the analog protection circuit is a resonant capacitor status signal which is used by the digital timing circuit to ensure start up. When power is applied to the SRI output stage, SCR leakage current may charge the resonant capacitors. The status output is true for positive capacitor charge and false (low) for negative capacitor charge. The correct SCR(s) is (are) fired to compliment resonant capacitor charge.

Refer to the Protection Unit simplified block diagram in Figure 2.5.3-1. Inputs for resonant capacitor voltage, line input voltage, and output voltage are isolated from the power circuit by differential input amplifiers and compared with preset voltage references. Out-of-limit conditions generate a protection signal which interrupts operation of the power converter and produces a trip signal to drive front panel displays. There are two isolation amplifiers for output voltage. One is contained in the protection hybrid and is designed to interface with an external signal conditioning amplifier. Two of the APL power converters produce several kV dc and have integral high voltage attenuation networks and signal amplifiers. The PU internal isolation amplifier is designed to interface with an external amplifier and provides unity gain common-mode isolation. When low voltage output is monitored, the PU circuit card external amplifier is used.

Power converter output voltage is monitored by a unity gain differential buffer which removes common mode noise from the long lines which connect the output voltage amplifier in the power section to the control card cage. The isolated output voltage signal is routed to the control circuit card for feedback control.

Four trip signals generated by the analog protection circuit are resonant capacitor 1 and 2 trip (overvoltage), line input voltage trip (insufficient voltage to run SRI), and output voltage trip (overvoltage). These signals are routed to display drivers on the housekeeping card.

Digital Timing Circuit--The digital timing circuit is in the inverter feedback control loop and forms an integral part of the control circuitry. Functionally, the control loop is arranged as shown in the block diagram of Figure 3.1.3-1. The analog section of the protection functional block cannot be considered as part of the control loop since it has no control effect during normal converter operation.

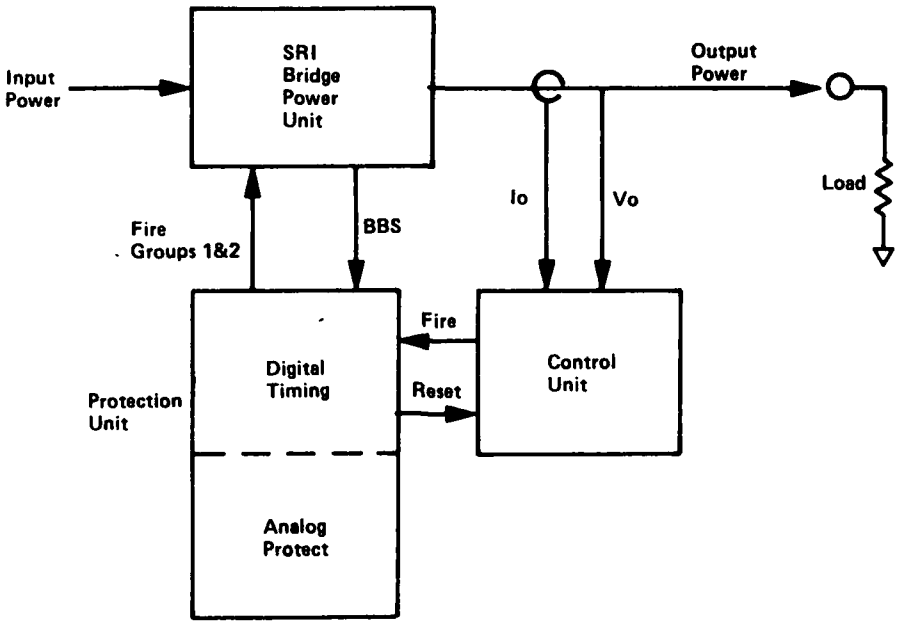


Figure 3.1.3-1 Control Loop Block Diagram.

The digital timing section of the protection unit is enclosed in the power converter feedback control loop. This portion of the PU provides the following functions:

1) Protection from simultaneous conduction of power switches,

2) Component stress limiting based on analog protection status,

3) Handshakes with the control circuit, and

4) Provides a converter start function.

Additional requirements for the ac-to-dc converter are:

1) Three Phase Unit (TPU) handshaking, and

2) Generated diode timing signal.

Protection from simultaneous conduction is provided on a half-cycle basis. A power switch cannot be fired until four conditions are met. First, all power switches must be recovered to a forward blocking state. Second, analog protection status must indicate that monitored circuit voltages are within limits. Third, a "fire" signal from the control circuit must be present. The fourth condition applies only to the ac-to-dc converter and is based on a handshake status signal from

the Three Phase Unit (TPU), request for transition. Power switch operation is interrupted during logical transition of three phase decoding logic.

Several methods have been employed to provide protection for the SRI power section and to ensure continuous, uninterrupted converter operation. First, component stress is actively limited. Input, output, and resonant components are monitored continuously for voltage and action is taken by the digital timing section within 1/2 cycle to limit the component stress and is implemented as follows. OVP and analog protect inputs from the analog protection section are applied to the digital timing section and if either of these signals is true, the fire command signal from the control card is interrupted until the fault clears.

Control circuit handshaking is provided to ensure coordination between logical circuits which appear in the closed feedback loop. Three signals provide this handshaking function. Two signals are directly enclosed in the control feedback loop, RESET and FIRE. The third sigma, INHIBIT, is used only during three phase ac-to-dc operation.

Normal closed-loop handshaking between the PU and Control Unit (CU) functions as follows; A fire command is produced by the control circuit when additional power is required from the converter. The PU will allow power switches to fire when the fire command is true, recovery is sensed, and analog circuits are within limits. When the PU generates a fire group command, a RESET signal is sent to the CU to reset the control angle integrator. At the end of the power half cycle, reset becomes false and the control angle integrator will begin generation of a control angle for the next half cycle.

Start sequence timing is included to initiate closed loop oscillation after power is first applied and for restart after protection shutdown or manual stop. When power is applied to the power converter control circuits, all logic is reset. During normal operation, logic is clocked by back bias signals from the power section. The start function sets up logic and initiates the first fire group signal. When used for the ac-to-dc converter, an additional signal is produced which initializes three phase logic before a fire group signal is produced.

Ac-to-dc converter operation--Two PU functions are required which are unique to three phase operation, handshaking with the TPU and timing the firing of SCRs used as diodes. Handshaking is accomplished with two control signals, Request For Transition (RFT) and Safe For Transition (SFT). RFT is generated by the TPU when a phase pair change is detected and is used by the PU to interrupt firing of power switches. At the end of a power half cycle and resonant current has dropped to zero, SFT is generated by the PU and is a signal to the TPU that logic may be safely changed to enable groups of SCR pairs. Tq microseconds after the SFT is generated, firing of power switches may resume.

The three phase ac-to-dc converter uses SCRs alternately as power switches and as diodes. Once a group of SCRs have been fired to produce a resonant half cycle, reflected resonant current which is produced at the end of the half cycle must be returned to the power supply. This current must have a low impedance path in order to prevent potentially destructive voltage from damaging components. SCRs are fired as diodes to provide this current path back to the power source. Timing for the two modes is different and is based on unique circuit conditions. Power switch timing is based on SCR recovery and a fire command from the control unit. Diode timing is based on change of sign of resonant current.

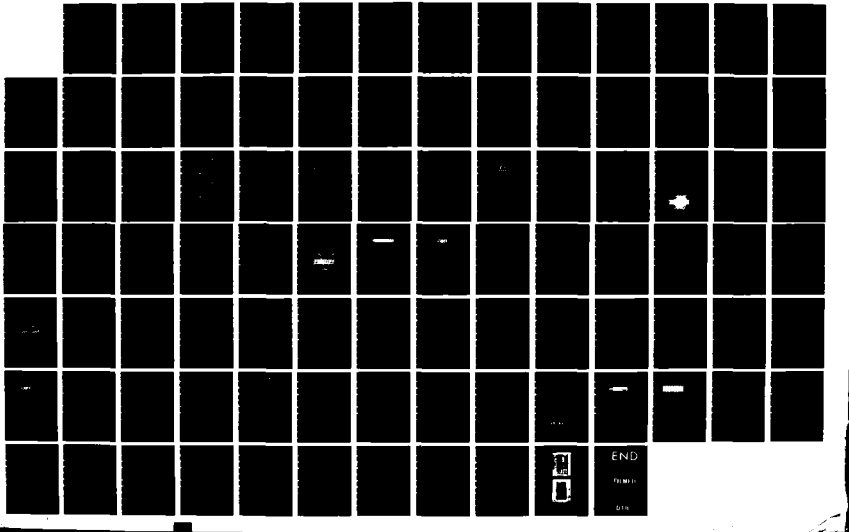
3.1.3.3 Circuit Schematic--Figure 2.5.3-2 shows the final schematic of the protection unit. All components within the dashed lines are external to the hybrid. Several of these external components are not required for a flight unit and are included here to protect hybrid circuits in a plug-card environment. The 100 k ohm input resistors are included on the plug cards to reduce the input impedance of CMOS gates to attenuate noise picked up in card cage wiring. Also, the outboard isolation amplifier is used for bench test of low voltage converters and would not be needed in a flight type design.

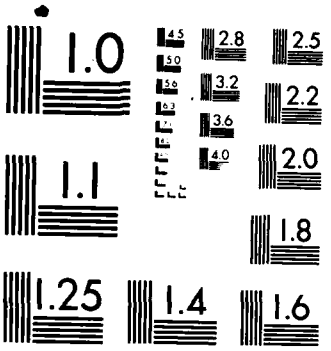
3.1.3.4 Detailed Design--Each of the two logical sections of the PU will be discussed. The design of the start circuit function is discussed separately but is integrated into the hardware design of the digital timing circuit.

Analog Protection Circuit--Analog input signals for resonant capacitor voltage, line input voltage, and output voltage are isolated from logic ground by unity gain differential buffer amplifiers, U13A-D. The two input amplifiers for resonant capacitor voltage and the line input voltage amplifier rely on high value input attenuator resistors in series with inputs to provide ground isolation from the power section. The voltage output amplifier operates with a low voltage signal from an isolation amplifier located in the power section and therefore is designed with 1 Meg ohm input resistors, R46-49, to supply ground isolation.

Resonant capacitors are continuously monitored for voltage within limits set by dual positive and negative window comparators, U16 to U19. The plus and minus voltage limits are set by a single SIT resistor, R70, which sets the outputs of a complementary tracking voltage reference, implemented by U14B and U14C. The four section window comparator is logically OR'ed by U11 so that an overvoltage of either sign on either of the two capacitors will produce an analog protection signal. The protection signal will remain true only during an actual overvoltage condition and can exist for a fraction of the power cycle. Capacitor voltage is 90 degrees out-of-phase with resonant current and an overvoltage signal can be only produced during resonant current zero crossover. Resonant capacitor analog protection has the result of delaying power switch firing until the capacitor voltage is within limit.

AD-A162 360 ADVANCED INVERTER TECHNOLOGY(U) MARTIN MARIETTA 2/2
AEROSPACE DENVER COLO ENGINEERING DEPT
C R GRIESBACH ET AL OCT 85 MCR-85-613 AFWAL-TR-85-2065
UNCLASSIFIED F33615-82-C-2239 F/G 10/2 NL





Line input voltage is tested for sufficient voltage to operate the power converter, by U20. Line voltage must be larger than output voltage plus circuit losses in order to successfully operate an SRI converter. If this condition is not met input-to-output voltage "q" approaches unity and resonant current and voltage becomes theoretically unbounded with operation in an undefined operating mode. Line input voltage is compared by U20 with a reference which is set by a single SIT resistor, R71. The value of the resistor is determined from equation [8]. Insufficient line input voltage causes U21 to produce a V(in) trip signal and an analog protection signal which interrupts firing of SCRs.

Converter output voltage is tested for overvoltage by a single-sided comparator, U21. Threshold voltage is set by the OVP SIT resistor, R72. The value of the resistor is determined by using equation [9]. Outputs for "V(out) trip" to actuate a fault display and for "OVP" are produced. The OVP signal interrupts firing of power switches until the output recovers within limit.

All comparators in the analog protection section are high speed LM111 chips. To provide clean switching and freedom from oscillations, five design methods are used:

1) The hybrid substate and base of the metal package are used as a ground plane.

2) Input pins are guard-banded.

3) 220pF capacitors, C7-13, are connected between inverting and non-inverting input connections and are located very close to each comparator to prevent small differential mode noise from falsely triggering inputs.

4) Unused offset adjustment pins 5 and 6 are tied together to prevent coupling output signals to input circuits.

5) 100 mV of positive feedback is used to force each amplifier quickly out of linear operation. Input voltage sag occurs during power converter operation. This line input voltage transient caused triggering of the V(in) analog protection. The input voltage comparator, U20, hysteresis level was increased from 100 mV to 300 mV to prevent power converter "short cycling." All reference voltages are derived from a single source, VR1, an LM129A precision voltage reference chip. The positive reference is buffered and inverted to provide a tracking negative 6.9 volts reference source, U14D.

Digital Timing Circuit--Circuit operation for dc-to-dc power conversion is discussed first while operations unique to ac-to-dc operation is discussed at the end of this section. A timing diagram for the digital timing circuit is included in Figure 3.1.3-2.

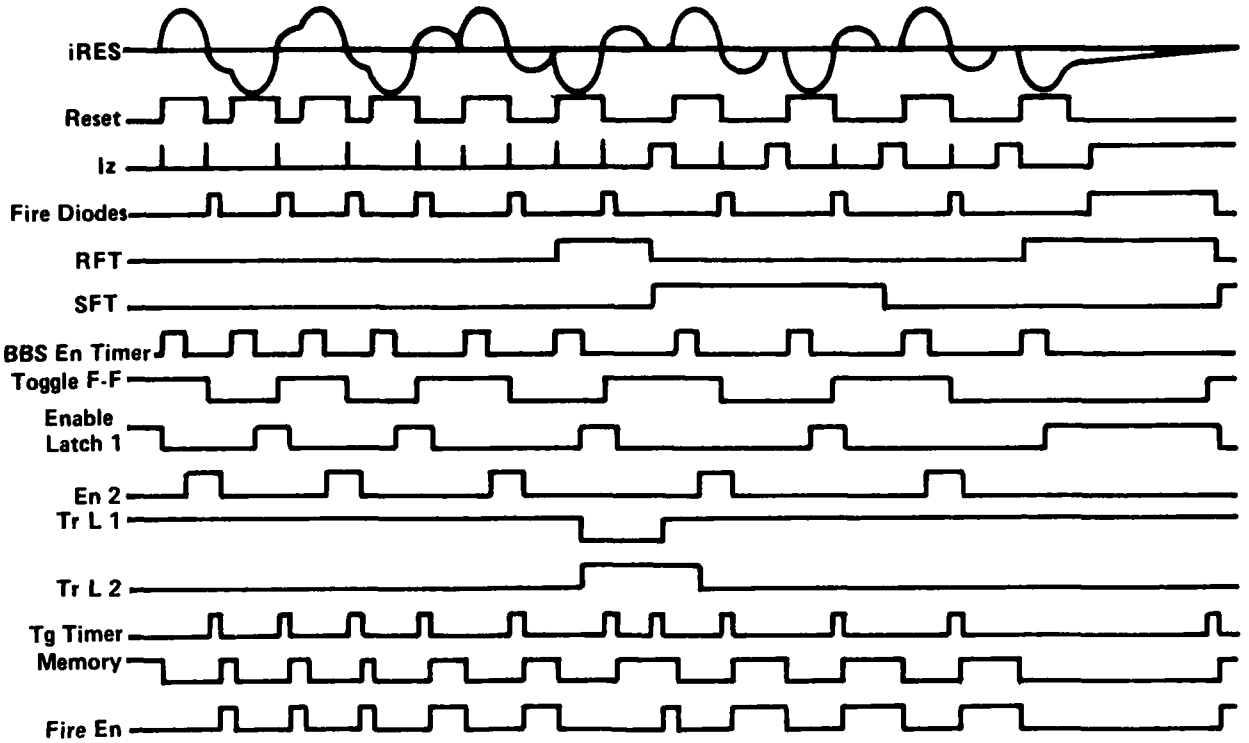


Figure 3.1.3-2 Protection Unit Logic Timing Diagram

Back bias sensor signals are logically OR'ed by U6, U7A, U7B, U10A, and U5D. Unused BBS inputs must be tied high and this is accomplished in the 10 kW and 5 kW card cages by hard wiring on the PU card edge connector. The 200 kW SRI uses all 8 BBS inputs, while the 10 kW half bridge and 5 kW ac-to-dc use only two of the BBS inputs. The twelve BBS signals used by the 5 kW three phase converter are combined into two signals by the Three Phase Unit (TPU) and are named group 1 enable and group 2 enable.

When all required BBS signals are true, the recovery timer, U1B, a CMOS 4098 monostable multivibrator, is started. This timer has three modes, two for normal circuit timing and one used in the three phase ac-to-dc converter only, which is discussed in a later paragraph. The two operating modes for normal operation are normal recovery and delayed recovery. Continuous true BBS for the entire recovery period is defined as normal recovery. Discontinuous true BBS will result in extended recovery time. SCR recovery requirements are based on a discussion with Joe Rockot of Westinghouse (Ref. 5). An SCR must have reverse bias to facilitate recovery to a blocking state but this reverse bias is often discontinuous in the SRI power stage due to resonant current parasitic oscillation. The timing components of the recovery timer, are C4, R6 and R74. The leading edge of the BBS signal triggers U1B. In normal recovery time operation, the BBS signal remains true and timing is determined by equation [4].

[4] Equation 3.1.3.3. $T = 1/2 \times C4 \times \left| \frac{R6 \times R74}{R6 + R74} \right|$

When the BBS signal is false during a portion of the recovery time, CR6 becomes reversed biased and timing capacitor is charged through R6 only and the time constant is established by the equation T = 1/2 x C4 x R6. R6 may be eliminated for some applications and is included on the prototype controller so that operation with input-to-output voltage "q" approaching unity could be studied. Note that "q" near unity will produce a very narrow BBS signal which is of shorter duration than SCR recovery time.

After recovery time-out, the memory latch, U2B is set, enabling a fire signal to pass AND gate, U8A. AND gate U10C is used for ac-to-dc operation only. If a fire signal is present at card input H, this signal will set the Fire Flip Flop (FFF), U3A and one of the two fire group signals is set high. The Q output of the FFF produces the RESET signal which is used to time integration of the resonant current on the control card. Fire group 1 or fire group 2 is generated dependant on the state of the Toggle Flip Flop (TFF), U9A. The TFF state is clocked into the SET and RESET inputs by the Q bar output of the FFF and are derived from the BBS signals. A BBS group 2 signal causes the TFF to set up to fire group 1 SCRs while a BBS group 1 signal sets up the TFF to fire group 2 SCRs.

Noise transients are present on the BBS signal lines due primarily to parasitic oscillation of resonant current in the power section. These transients could interfere with normal oscillator timing and appear as ripple and noise on the output voltage. These transients are therefore removed from logic timing with two enable latches, U2A and U3B, which allow only valid BBS signals to trigger the recovery timer. This is accomplished by two BBS enable signals which cause the BBS group 1 and group 2 input gates to pass information only during the appropriate portion of the cycle. Refer to the PU timing diagram line X. Proper clock timing for the BBS enable latches is provided by the BBS enable timer, U22A.

Three phase logic handshaking is provided by integrated circuits U25, U24, U23, U22B, U12A, U12B, U10C, U9B, U7C, U4C, and U4D. Two functions are performed by these circuits, handshaking with the Three Phase Unit (TPU) and generation of a "Fire Diodes" signal. Handshake interconnection with the TPU prevents simultaneous conduction of power switches while logic on the TPU is transferring from one phase pair to the next and is implemented as follows; The TPU begins transition logic by sensing a requirement to change selection of which four of the six pairs of power switches are enabled, and generates a Request For Transition (RFT) signal. The RFT signal is received at the PU by U4C, U9B, and U7C. Firing of power switches is prevented by U9B which is held in reset while the RFT signal is true, thus preventing a Fire signal from passing AND gate U10C and setting the FFF, U3A. When resonant current has returned to zero after an antiparallel "diode" conduction half cycle, the PU generates a Safe For Transition (SFT) signal. The SFT signal is an instruction to the TPU circuit to transfer phase logic.

Generation of the SFT is accomplished as follows; Zero resonant current exists under two conditions, at the end of a power switch half-cycle and at the end of an antiparallel "diode" half-cycle. The later exists at zero current and when BBS inputs are disabled. Note that a power switch must be fired to start the BBS timer, U22A and will enable one of the BBS inputs. This function is implemented by U12A which detects a BBS enable, U4D which inverts the absence of BBS to a true logic level to enable AND gate U7C. The other two inputs to U7C are zero current and RFT. The output of U7C and a low reset signal are inputs to AND gate U24D. The output of U24D triggers U22B which produces the SFT signal. The series gates U24A, U24B, and U24C provide delay to prevent timing conflict with fire signal timing. A one-shot is used for the SFT to prevent logic transition "chatter" which could be caused by power line sag and interruption of the RFT signal. Time-out of the SFT one-shot is determined by components C5 and R79. For the 60 Hz 5 kW SRI, phase pairs exist for an average time of 1/(60 Hz X 6 phase pairs) = 2.78 ms. The time period selected for the SFT one shot is approximately 1.2 ms. The formula for calculating time period based on charging components is taken from the RCA CMOS data book and is presented in equation [5]. By calculation, the time period is 1.47 ms and by measurement is 1.2 ms. The timing capacitor was measured on an HP model 4262A RCL bridge and found to be within 1% of rated value. The timing resistor was measured using a 4 1/2 digit multimeter and found to be within rated tolerance of 1%.

[5] $T = 1/2\ RC$

While the TPU logic is undergoing phase pair transition, the PU must delay firing a power switch. The Tq timer provides this delay. The output of U22B produces the SFT signal which also sets up a low data input to U23B and a high data input to U9B. When logic TPU transition is complete, the RFT signal goes low. A transition of the RFT from high to low is inverted by U4C and provides a clock signal to U23B. The true output of U23B triggers the Tq timer through U5A. After Tq time-out, U1B Q bar output transfers high the true SFT signal at the data input of U9B is clocked to the output. The true output of U9B holds U23B in reset to prevent interruption of normal converter operation, its feedback to its data input to hold Q output high, and enables AND gate U10C to pass a fire command from the control circuit input (U8A output) to the FFF, U3A.

SCRs are fired as diodes by timing provided from the PU circuit. It was determined during functional testing that firing SCRs at or just before zero current crossing reduced power dissipated in the snubber networks. The BBS cannot produce a signal at zero resonant current crossing since back bias voltage is produced a finite amount of time after resonant current reverses polarity. The BBS propagation time produces additional delay after resonant current zero crossing.

The Fire Diodes signal is generated by a zero current detector comprised of U25 and U23A. Resonant current at card pins 17 and U is rectified by CR1-CR4. CR5 clamps the rectified output at one diode drop. Threshold of the LM111 comparator, U25, is set by R75 and R76 and is approximately 0.27 V which translates to R77 burden resistor current of 0.67 mA.

Three current transformers are available in the APL 5 kW three phase SRI to provide input current to the Fire Diodes signal generator. These transformers have unique turns ratios. The transformer connected to the power section front panel jacks CTA is 1000:1, the CT connected to jack CTB is 250:1 and the CT connected to CTC is 100:1. These allow selecting detection current at 670 mA, 168 mA, or 67 mA. Intermediate values of threshold current may be selected by connecting a second burden resistor in parallel with PU card input pins 17 and U. The formula for calculating fire diode signal timing is based on resonant current and threshold current. Equation [6] may be used to calculate timing.

[6] $T = SIN^{-1}\ [Idet/(Idet \times Ires(pk)) \times 2.78X10^{-7} + 6 \times 10^{-7}]$

where Idet = threshold current and Ires(pk) = peak resonant current

Start Circuit--The start circuit performs two functions. While the stop signal is false (low), PU logic is reset. Start signal transition from low to high triggers the start one shot, U1A and removes reset from the Memory Latch, U2B, the Fire Flip Flop, U3A, and both BBS Enable Latches, U2A and U3B. The pulse duration of the start one shot is set by components C3 and R5 and the approximate pulse time may be calculated by equation [5].

The AIT breadboard PU uses a 2 microsecond start pulse, set by the internal 100 pF capacitor, C3, and an external 49.9 k ohm resistor, R5. The leading edge of the start pulse clocks the Toggle Flip Flop (TFF), U3A, state to the correct power switch fire group based on sign of the resonant capacitor voltage. The power switch group is selected which compliments capacitor charge so that generation of the first power pulse is guaranteed. The trailing edge of the start pulse clocks a true data signal through the Fire Flip Flop (FFF), U3A.

Oscillation is sustained by closed loop operation. At completion of the first resonant power pulse, back bias is detected by the PU and logic is set up in preparation for the next resonant power half cycle. Closed loop operation is then self-sustained.

3.1.3.5 Device Ratings--Inputs to the hybrid analog section must not exceed 15 V in either polarity. Operating temperature range is -40° to 85° C. and performance has been tested over this range. Output signals are consistent with B series CMOS specifications. Input power is +15 Vdc and -15 Vdc with a $\pm$1 Vdc tolerance. Ripple and noise must remain within the $\pm$1 V tolerance limit.

3.1.3.6 Application Information--Seven select in test (SIT) resistor values may be changed to tailor the PU for specific application and their use is described in the following subparagraphs by function.

Start Timer--Resistor R5 may be changed to vary the start pulse width. Refer to equation [4]. The internal capacitor value is 100 pF $\pm$ 10%. The equation will produce approximate pulse time and actual value may vary $\pm$ 50% from calculated value. The pulse width is required to allow set-up time for logic circuits and the selected value

of 2 microseconds is designed to accommodate 20 CMOS B-series gate delays. Other application of the PU may require change of logic set-up time.

Tq Timer--Resistors R6 and R74 are used to charge internal timing capacitor C4. R6 is included to allow operation in a marginal operating mode and should be included in the circuit for lab study only. This resistor enables the SRI to continue operation when input to output voltage ratio (q) approaches unity. Under some circumstances, SCR recovery cannot be guaranteed when this condition exists and an example is discussed in section 3.2.7. Resistor R74 can charge the timing capacitor only during a true BBS condition. When R6 is open, the BBS signal must exist for the entire recovery time to enable the converter to continue uninterrupted operation.

Proper calculation of maximum power switch recovery time is necessary to prevent simultaneous conduction of power devices. Manufacturer's published data may need to be factored for application in an SRI converter. General Electric has published a recommendation for SCR recovery time approximation when an antiparallel diode is used, stated as follows: "Turn-off time measurements have shown that SCR turn-off times with diode are 20-to-50% longer than tq with reverse voltage" (Ref 13). Reverse voltage must be at least 50 V to meet tq with reverse voltage applied, per GE specifications.

SCR recovery is accomplished by two methods, sweeping the space charge from the junction with reverse current, and recombination of pos- itive and negative charges which can occur when forward current has ceased. Reverse voltage assists in sweeping the space charge, but a high-efficiency diode placed across the SCR will limit current sweeping to a minimal amount. Recombination time is the worst case recovery time for an SCR, provided that forward current has ceased. Recombination time for any particular device should be available from the manufacturer.

Once proper device maximum recovery time is determined, Tq Timer pulse width may be calculated. Loop delay time should be subtracted from the calculated Tq to arrive at Tq Timer pulse width. The loop delay includes 900 ns BBS circuit delay, 3 gates x 100 ns propagation delay and 6 gates with 30 ns propagation delay in the PU circuit, and 300 ns delay in the FPG, for total control circuit loop delay of 1.7 microseconds.

Example: SCR reverse recovery time is specified to be 15 microseconds with reverse voltage applied. With antiparallel diode, this increases to 15 X 1.5 = 22.5 microseconds. Tq timer pulse width is therefore 22.5 microseconds minus loop delay of 1.7 microseconds, or 20.8 microseconds.

BBS Enable Timer--The BBS enable timer, U22A maximum pulse width must be less than the power section resonant half period in order to enable the appropriate BBS input gate before resonant current reverses direction. There is no absolute minimum time for the BBS timer pulse width, but it should be of sufficient length to mask transients which are produced after an SCR is fired. One quarter period was selected for the

AIT breadboard, or 25 microseconds. Pulse width is calculated from equation [4]. The charge capacitor, C6, is contained in the hybrid and is 100 pF. Resistor R80 is changed to alter the BBS Enable Timer pulse width.

SFT Timer (Three Phase Only)--The SFT Timer pulse width is selected to mask line input voltage fluctuation that is caused by loading of the SRI. Line voltage drop on the phase pair which is loaded will recover when an RFT is generated and power switching within that phase pair ceases. Phase pair selection could revert back to the last pair unless prevented by the SFT pulse. The effect of line source impedance and associated line drop has been measured. Approximately 500 microseconds were required for the line voltage to recover when the SRI was operated at maximum power output. The SFT Timer pulse was set at 1.2 ms as a safe point between the 0.5 ms minimum required and the 2.78 ms phase pair interval. Line frequency other than 60 Hz would require recalculation of SFT pulse width. The charge capacitor, C5, is internal to the hybrid and is 0.015 microfarads. For the AIT breadboard, the charge resistor, R79, is 196 k ohms to produce a 1.2 ms pulse width. Equation [4] is used to determine the value of R79. For 2500 Hz line frequency, phase pairs exist for 66.7 microseconds and the value of R79 would be 3.3 k ohms to produce a 25 microsecond SFT pulse width.

Resonant Capacitor Stress Voltage Limit--Resonant capacitor voltage is tested with dual window comparators. The positive and negative reference voltages for these comparators is generated by U14B and U14C from a single source, U14D. A single resistor, R70, is selected to set the capacitor voltage limit for both capacitors for both the positive and negative limits. Equation [7] is used to calculate the value of R70.

[7] Resonant Capacitor Voltage Limit Resistor

$$R70 = \frac{487\ Vth}{3.45 - 0.343\ Vth} \qquad \text{where } Vth = \frac{10}{10 + Rattn}\ Vcap$$

Example: Given Vlim = 1000 V pk-pk.
and Rattn(vcres) = 1.5 M ohms
then Vth = 6.62 V

R70 = 2734 ohms

Minimum Line Input Voltage--An attempt to start an SRI when line input voltage in insufficient to overcome circuit losses and forward bias the output rectifiers results in an undefined operating mode. Operation in this mode may generate voltages that could overstress power section components and protection must be provided for this. This protection function is implemented by comparator U20. Threshold level of this comparator is set by SIT resistor, R71. Equation [8] may be used to calculate the value of R71.

[8] Minimum Line Input Voltage Setting Resistor

$$R71 = \frac{2050 \times Vth}{6.9 - Vth} \quad \text{where} \quad Vth = \frac{10 \times Vs}{10 + Rattn}$$

Example: Given Vline = 500 Vdc
and Rattn(vin) = 750 k ohms

Vth = 5.882 R71 = 11,845

Output Overvoltage Protection--Output voltage is compared with a reverence voltage which is set by resistor R72. Power switching is interrupted when output voltage exceeds this limit. The value of R72 is calculated from equation [9].

[9] Output OVP Resistor

$$R72 = \frac{2050 \times Vth}{6.9 - Vth}$$

$$\text{where } Vth = \frac{10}{10 + Rattn} Vo$$

Example: Given Vout(lim) = 210 Vdc
and Rattn(vo) = 500 k ohms

Vth = 2.47 R72 = 1143 ohms

3.1.3.7 Performance Information--Maximum switching frequency is a function of total circuit delay time and the speed of the power switches. Total circuit delay of the PU hybrid when included in an SRI control loop, is 500 ns. If it is assumed that control loop delay in circuit elements other than the PU is an additional 500 ns and minimum control angle to prevent component overstress for a practical SRI power converter is approximately 40°, then the maximum switching frequency capability of the PU is found as follows;

1) Minimum control angle = 40°
2) Minimum control time = 40/180 x 1/2F = 0.111/F = 1 microsecond
3) F(max) = 0.111/1 microseconds = 111-kHz

The maximum switching frequency of a very high power dc-to-dc SRI converter is limited by currently available power switches. State of the art in high power bipolar transistors is the D60T, which could be switched at 40-kHz in a high power SRI converter. Current technology in high power SCRs is 10 microseconds recovery time which limits maximum switching frequency to about 10-kHz. High power Gate Turn Off (GTO) thyristors exhibit recovery times approaching 3 microseconds. A low power MOSFET converter has been demonstrated to 1.5 Mhz (ref 3.1.3-1) but a high power, high voltage MOSFET device has not been identified.

Future application of high power SRI converters may enable high switching frequency when power devices are available for this purpose. The PU circuit delay time may be reduced by implementing logic circuits with high speed gates. A change from standard CMOS devices to High speed CMOS (HCMOS) or TTL logic could increase the switching frequency limit to about 300-kHz.

See Reference 3.1.3-1: Redl, R., B. Molnar and N. Sokal. "Class-E Resonant Regulated dc-to-dc Power Converters: Analysis of Operation and Experimental Results at 1.5 MHz," PESC Conference Proceedings, 1983.

3.1.3.8 Packaging--The PU hybrid is physically separated into two sections within a single hybrid container. The sections are divided between analog and digital circuit functions.

Further optimization of the packaging could be accomplished with one or a combination of the following methods;

1) Single section op amps and comparators could be replaced with quad section devices, provided radiation hard parts could be identified.

2) Chip resistors could replace screen printed resistors.

3) The single layer circuit substrate could be replaced with a multilayer substrate to reduce surface area consumed by wiring runs.

4) Protection circuitry for a dc-to-dc converter could be implemented without the extra circuits required for three phase handshaking and SCR diode timing.

3.1.4 Three Phase Unit

3.1.4.1 Background--Two TPU test breadboard cards were fabricated and tested. The first test card was designed and tested to the requirements outlined in program Phase I and listed in paragraph 2.5.4.2 of this report. The test circuit operated satisfactorily when operating the APL 5 kW ac-to-dc converter at low power. Three issues were raised as a result of testing;

1) Delay caused by the BBS circuit caused SCRs used as diodes to fire 2.3 microseconds after resonant current had reversed direction. Snubbing circuits were required to carry resonant current for the BBS and FPG delay time plus turn on time of the SCRs. Energy delivered to the snubbing circuits is dissipated as heat and converter efficiency is penalized. A perfect, zero-delay BBS could reduce the SCR timing error to TPU propagation delay time plus FPG circuit delay plus SCR turn-on time, or approximately 1.5 microseconds. A goal of reducing diode turn on delay to 1 microsecond was established.

2) Noise sensitivity of the BBS circuits had been improved substantially during functional test and redesign, but no method was found to guarantee noise-free BBS signals. Some concern with TPU logic errors caused by noisy BBS signals was raised. Note that BBS signal noise was an issue with PU functional test and circuit redesign of the PU was required to eliminate BBS noise from protection logic. Ref. paragraphs 3.1.3.1 and 3.1.3.4 (Digital Timing Circuit).

3) Phase transition is based on selection of the two power source legs which have the greatest magnitude voltage difference. No current is used from the third power source leg. Some voltage drop is experienced on the two circuit legs which supply current to the SRI converter. During phase transition, input current is interrupted while logic is transferred and line voltage on the last selected phase pair recovers. A variable voltage transformer was used to source the three phase SRI during functional testing. The magnitude of the recovery was quite large due to the high source impedance of the variable transformers. The large change in line voltage during phase transition caused instability of the phase transition logic. Two methods were developed to eliminate this problem, improved hysteresis and limiting the time interval at which phase transition was allowed to occur.

These three issues resulted in the decision to reconfigure TPU top level requirements. The new requirements are summarized in Table 3.1.4-1.

Table 3.1.4-1 Three Phase Unit Top-Level Requirements (Revised from Table 2.5.4-1)

- Determine phase pair.
- Limit occurrence of phase pair selection
- Determine proper back bias states and generate two group enable signals for the PU logic.
- Generate coordinated fire signals for each SCR based on phase pair selection and SCR mode (power switch or diode).
- Base diode SCR timing on an anticipate signal from the PU.

All of the information in the following paragraphs in this section will refer to the TPU hybrid circuit which is based on the above top level requirements.

3.1.4.2 Theory of Operation--The Three Phase Unit is logically divided into four sections:

1) Phase detection,

2) Phase decoding,

3) Back bias signal group generation, and

4) SCR fire control.

Each will be discussed separately in the following paragraphs.

Phase Detection--Phase voltages are attenuated by three resistor dividers and isolated from magnitude comparators U2A, U2B, and U2C by unity gain buffers, U1A, U1B, and U1C. Three signals are produced by the magnitude comparators, e1-e2, e1-e3 and e2-e3. These three signals are latched by the SFT signal and six output produced, the three signals from the magnitude comparators with three complementary signals, summarized in Table 3.1.4-2.

Table 3.1.4-2

Phase Voltage	Designation
e1-e2	V12
e2-e1	V21
e1-e3	V13
e3-e1	V31
e2-e3	V23
e3-e2	V32

Phase detector states must not cause logic changes of state during SRI power stage conduction. Handshaking signals which coordinate phase detection logic with Protection Unit logic interface with the phase decoder section of the TPU. A change in state of a decoded phase pair signal causes generation of a Request For Transition (RFT) signal. Decoded phase signals are latched into the Phase Decoder by a clock signal which is the Safe For Transition (SFT) signal from the PU.

Phase Decoding--The six phase voltage signals generated by the phase detector are decoded into two logical groups with six signals each. The first group of signals provides logical selection of back bias control group signals and are designated as Phi signals. The second group provides logical selection for SCR fire control and are designated as voltage pair signals, i.e. V12.V13. The twelve outputs from the phase decoder are summarized in Table 3.1.4-3.

Table 3.1.4-3.

Phase Pair	Derivation	Voltage Pair Signals
12	V12.V13.V32	V12.V13
13	V12.V13.V23	V13.V23
21	V21.V23.V31	V21.V31
23	V21.V23.V13	V21.V23
31	V31.V32.V21	V31.V32
32	V31.V32.V12	V12.V32

Back Bias Signal Group Generator--Back bias signals from the twelve SCRs are logically combined into two back bias group signals. Two groups of SCRs are fired alternately in normal SRI power converter operation. Before Group 1 SCRs may be safely fired, it is necessary to ensure that all of the SCRs in Group 2 have recovered and before Group 2 SCRs may be fired, it is necessary to ensure that all Group 1 SCRs

have recovered. Back bias is used to start the recovery timer in the PU. Logical selection of the proper SCRs which must be checked for back bias is the function of the back bias signal group generator. Logical representation of the two BBS groups are shown in equations [10] and [11].

[10] BBS Group 1 = (Phi 12).(BBS 11).(BBS 24)+(Phi 13).(BBS 11).(BBS 34)
+ (Phi 21).(BBS 14).(BBS 24)+(Phi 23).(BBS 21).(BBS 34)
+ (Phi 31).(BBS 31).(BBS 14)+(Phi 32).(BBS 31).(BBS 24)

[11] BBS Group 2 = (Phi 12).(BBS 12).(BBS 23)+(Phi 13).(BBS 12).(BBS 33)
+ (Phi 21).(BBS 22).(BBS 13)+(Phi 23).(BBS 22).(BBS 33)
+ (Phi 31).(BBS 32).(BBS 13)+(Phi 32).(BBS 32).(BBS 23)

Fire Control Signal Generator--Nine inputs are combined to generate fire signals for each of the twelve SCRs. Six of the inputs are phase pair voltage signals generated by the phase decoder. Two inputs are used to time firing SCRs as primary power switches and are the fire group 1 and Fire Group 2 signals generated by the PU circuit. One signal is used to time firing SCRs as diodes and is the Fire Diodes signal that is generated by the PU. The Fire Diodes signal is synchronized to the correct fire group by an R-S flip flop which is toggled from the two fire group signals. Logical functioning of this circuit is summarized in Table 3.1.4-4. Logic equations are listed in Table 3.1.4-5.

Table 3.1.4-4 Fire Control Logic Summary

	Fire Group 1		Fire Group 2	
Signal	SCR	Diode	SCR	Diode
V12.V13	12	14	11	13
V21.V23	22	24	21	23
V31.V32	32	34	31	33
V21.V31	13	11	14	12
V12.V32	23	21	24	22
V13.V23	33	31	34	32

Table 3.1.4-5 Fire Control Logic Equations

SCR		Derivation	Diode		Derivation
11	=	FG2.V12.V13	13	=	FG2.V12.V13.Iz
12	=	FG1.V12.V13	14	=	FG1.V12.V13.Iz
13	=	FG1.V21.V31	11	=	FG1.V21.V31.Iz
14	=	FG2.V21.V31	12	=	FG2.V21.V31.Iz
21	=	FG2.V21.V23	23	=	FG2.V21.V23.Iz
22	=	FG1.V21.V23	24	=	FG1.V21.V23.Iz
23	=	FG1.V12.V32	21	=	FG1.V12.V32.Iz
24	=	FG2.V12.V32	22	=	FG2.V12.V32.Iz
31	=	FG2.V31.V32	33	=	FG2.V31.V32.Iz
32	=	FG1.V31.V32	34	=	FG1.V31.V32.Iz
33	=	FG1.V13.V23	31	=	FG1.V13.V23.Iz
34	=	FG2.V13.V23	32	=	FG2.V13.V23.Iz

3.1.4.3 Detailed Design--Design for each of four physical circuits used to implement each of four logic functions listed in the theory of operation section are explained independently.

Phase Detector--The phase decoder performs five functions:

1) Buffering of input attenuators,

2) Phase voltage magnitude comparison,

3) Decoded phase pair signal latching,

4) Phase transition detection, and

5) Generation of the RFT signal.

Input Buffering--Implementation of these functions is as follows. The high voltage line inputs are attenuated by resistor dividers R1-R2, R3-R4, and R5-R6. Capacitors C13, C14, and C15 attenuate high frequency transients from the inputs. Additional attenuation of the line voltage is provided by external resistors which are wired in series with PU card connector pins 5, 6, and 7. These are located off-board due to considerations for power dissipation and high voltage dielectric isolation. The buffer amplifiers, U1A, U1B, and U1C are three sections of an LM124 quad op amp. The amplifiers provide a low impedance source for each magnitude comparator in order to minimize hysteresis network cross-talk.

Magnitude Comparison--The magnitude comparators, U2A, U2B, and U2C are three sections of an LM139 quad comparator. Pull up resistors are provided for the open-collector outputs to pull the CMOS latch inputs to a high state. Hysteresis is set by positive feedback resistor networks R7-R8, R10-R11, and R13-R14. Hysteresis overdrive is approximately 50 to 100 mV, depending on input voltage level. This amount of input overdrive provides fast comparator switching and freedom from oscillation.

Phase Pair Latching--Phase pair latches, U3A, U3B, and U4A are implemented with dual D-type 4013 CMOS and are used to prevent logic transitions during SRI power stage conduction. Changes in phase control logic may only be clocked into the latches by the safe for transition signal from the PU.

Phase Transition Detection--Phase transition is detected by U5, U6A, and U7A. Three exclusive OR gates are wired respectively to one input and one output pin of each of the three phase detector latches. A mismatch of input-to-output state can occur only as result of a relative magnitude change between phase pairs. This condition will cause a low state at one of the X-OR outputs. The X-OR outputs are OR'ed together by U6A.

RFT Signal Generation--An RFT signal may be generated only when the SFT signal is low and a phase transition exists. This function is performed by U5A and U7A. A phase transition condition is detected by OR'ing the outputs of the X-OR gates U5B,C, and D. The RFT signal is present at the output of U6A but must be enabled to the output pin of the TPU hybrid by U7A. While the SFT signal is high, RFT is inhibited.

Phase Decoder--The logic required for phase pair decoding is summarized in Table 3.1.4-3 and implemented with CMOS 4081 quad two-input AND gates, U14, U15, and U16.

Back Bias Signal Group Generator--Phase decoder logic summarized in equations [10] and [11] is implemented by CMOS 4073 triple three-input AND gates U8, U10, U11, and U13 and 4075 triple three-input OR gates U9 and U12.

Fire Control Signal Generator--Two functions are provided by the fire control circuit:

1) Routing Fire Group 1 and Fire Group 2 signals to the correct SCRs, and
2) Coordinating the Fire Diode signal to the correct SCRs, based on phase pair selection and fire cycle timing.

Both functions are implemented by identical circuitry. The equations in Table 3.1.4.4 describe these logic functions. SCRs used as power switches are controlled by 4081 CMOS quad two-input AND gates U19, U22A, U22B, U24, U27A, and U27B. SCRs used as diodes are controlled by logic gates U20, U22C, U22D, U25, U27C, and U27D. Diode and SCR functions are combined by 4071 CMOS quad two-input OR gates, U21, U23, and U26.

Fire group selection of SCRs used as power switches is accomplished by the PU circuit. Control group selection of SCRs used as diodes is implemented by an R-S flip flop, U4B and two-input AND gates U7B and U7C. A true Fire Group 1 signal resets the diode group selector flip flop to select Group 2 diodes, (U4B Q bar output true). A true Fire Group 2 signal sets the diode group selector flip flop to select Group 1 diodes (U4B Q output true).

3.1.4.4 Circuit Schematic--A schematic of the TPU is shown in Figure 2.5.4-5. The same schematic applies to the breadboard card, the prototype card, and the hybrid microcircuit. All components shown on the schematic are used on the breadboard card. Components used on the hybrid card are divided between discrete and hybrid components. Components which are external to the hybrid are contained within dashed lines and to the left of the input card edge connector terminal block. These components were intentionally deleted from the hybrid circuit design. The input attenuator may require modification for different applications. The fifteen 100 k ohm resistors attached to the input connector block are used as terminators for card cage wiring and would be unnecessary for flight hardware.

3.1.4.5 Device Ratings--Supply voltage is 15 Vdc +/- 10%. Total power dissipation is 220 mW typical and 450 mW maximum. Signal input voltage and current limits must conform to B-series CMOS ratings. Signal input current must not exceed 1 mA on any pin.

3.1.4.6 Application Information--There are no SIT resistor values required to operate the TPU. The line voltage input attenuator must be designed for each specific application and must produce the correct signal level for proper operation of the phase detector. The magnitude of the line input voltage signals is 10 V p-p maximum and 2 V p-p minimum. The TPU is designed to operate from a single 15 V supply. Single-supply operation is possible by using the 6.8 Vdc reference to offset the incoming phase voltage signals.

3.1.4.7 Performance Information--The maximum operating frequency of the TPU circuit is determined on a basis of maximum SRI switching frequency and three phase line input frequency. Maximum switching frequency which may be supported by the TPU is based on maximum circuit delay time and is found by summing maximum propagation delays through the critical circuit path. These gates are in series with closed loop control and total delay is listed for each:

Device	Delay (rise + propagation)
CD4073B	45
CD4075B	45
CD4075B	45
CD4081B	45
CD4071B	45
total	225 ns

The calculated speed of the TPU is consistent with SRI switching frequency up to 100-kHz.

Maximum line input frequency is limited only by the bandwidth of the LM124 input amplifiers and the the LM139 comparators. The specified large signal unity gain frequency response of a National LM124 is 10 kHz for a 10 V p-p output swing.

Both the switching frequency and line frequency limits may be increased by implementing the same circuit design with higher speed components. The circuit delay may be reduced to allow operating the TPU in an SRI converter with switching frequency higher than 100-kHz. This may be accomplished by replacing standard B-series CMOS devices with High speed CMOS (HCMOS) or TTL devices. This change would reduce critical path circuit delay to 50 ns so that the TPU could be used in an SRI operating at a switching frequency of 400-kHz.

Line input frequency may be improved with wide bandwidth input amplifiers. The only practical limit for line input frequency is approximately 10% of resonant frequency. Radiation hardened operational amplifiers are available which can achieve unity gain power bandwidth to several hundred kilohertz.

3.1.4.8 Packaging--The TPU hybrid is packaged in a 1.25 X 2.40 in. dual in-line flatpack. Most of the internal real estate is covered with printed wiring. Some reduction of outline dimensions is possible by using a multilayer substrate. An estimate from the Martin Marietta Denver Aerospace microcircuits lab suggests that the TPU could be optimally packaged in a 1.25 in. square flat-pack. The TPU circuitry is readily applicable to gate array implementation if production quantities could justify the high development and packaging cost. Ref. paragraph 2.3.4 of this report.

3.1.5 Control Unit

3.1.5.1 Background--A general control unit applicable to a broad range of SRI-based converters must meet requirements for accurate output voltage control, current control, and line voltage compensation. These requirements may be met with a control scheme based on the Analog Signal to Discrete Time Interval Converter (ASDTIC) control circuit patented by Dr. F. C. Schwarz. Some implementation difficulties and control range limitations were discovered in functional testing of the ASDTIC circuit and these will be addressed in detail. The range limitation of the ASDTIC control circuit is a consideration when an output transformer is included in the SRI output stage resonant circuit. The practical control range limit is 2:1.

Another control circuit was designed during AIT program work. It overcomes the range limitation of the ASDTIC circuit described above. The control scheme uses three separate control parameters, output voltage, output current, and line voltage. This method of control is widely used in Pulse Width Modulated (PWM) dc-to-dc power converters.

The control difficulties with ASDTIC control identified early in Phase II functional testing caused difficulty in testing other functional circuits. In order to quickly overcome the control issues and proceed with testing of functional elements which were to be hybridized, a simple voltage control card was designed, fabricated, and tested. No difficulties have been identified with voltage control.

The two existing control circuits, single mode voltage control and three parameter control, will be discussed in the paragraphs following in this section. The three parameter control card may be configured for an ASDTIC control circuit. Test results for the two control unit cards and for an ASDTIC control unit will be presented in section 3.2.5.

3.1.5.2 Theory of Operation--Theory of operation for the two existing control unit breadboard cards is discussed. Both of these circuits are directly compatible with the three control card cages designed to operate the three APL, SRI converters.

Voltage Control Unit Breadboard--Output voltage is used as the control parameter. Reference the schematic of the voltage control card, Figure 3.1.5-3. Control voltage is an isolated and inverted signal from the PU circuit. This negative signal is integrated and compared against a negative reference by a single amplifier stage, U1. The resultant

error signal is applied to the control angle integrator, U2. The control angle integrator is reset during SCR conduction by a reset signal generated by the PU circuit. Each half cycle of converter operation, a unique control angle is generated by U2 in response to error voltage produced by U1. The output slope of the control angle integrator is compared with a positive reference. When the integration slope reaches the reference voltage, a fire signal is produced.

Control is accomplished as follows. An increase in output voltage reduces the magnitude of a negative error voltage which in turn causes slower integration of the control angle integrator and a larger control angle (decreased switching frequency). Conversely, a decrease in output voltage increases the magnitude of a negative error voltage which produces a faster integration time and a shorter control angle (increased switching frequency). The system is stable on a cycle-by-cycle basis.

Three Parameter Control Unit--Output voltage, output current, and line voltage are used as the three control parameters. Output voltage is controlled by a low bandwidth control loop, output current is controlled by a wide bandwidth control loop, and line voltage compensation is accomplished on a cycle-by-cycle basis. Reference block diagram, Figure 3.1.5-1. The basic control is based on integrating an error signal produced by comparing output voltage against a reference, and summing this error signal with an integrated current feedback signal, and integrating this sum to produce a slope based on error magnitude. This slope is compared with a reference voltage which may be switched to one of two sources, a fixed reference or a reference that is proportional to source voltage.

The use of source voltage derived reference provides feedforward compensation. This control technique is used to improve audio susceptibility and line ripple rejection.

Current feedback may be derived from one of two sources, resonant current excess, or output current. Resonant current feedback is the current control method discussed by the inventor, Dr. F. Schwarz. Reference section 2.5.5 of this report. Excess resonant current is that portion of resonant current which is not damped (consumed) by load resistance and equates to "diode" current. The diode referred to here and in section 2.5.5 is the anti-parallel diode which is placed across each SCR power switch. The integral of diode current is proportional to input-to-output voltage ratio "q" and load resistance. Mathematical equations which describe these relationships may be found in appendix B. The comparator output is the fire signal which is sent to the PU circuit to cause the next power half-cycle to begin.

3.1.5.3 Detailed Design

Voltage Control Unit--A negative voltage signal which is proportional to output voltage is received from the PU card. This signal is compared with a negative reference to produce an error voltage which increases in amplitude as output voltage decreases. In this the control angle is decreased with an increase in converter output load. The error voltage comparator, U1 is a TI TL081 op amp. The reference for the comparator is produced by an adjustment control located on the

reference based on relative setting, and output voltage may be regulated to any value between zero and maximum. The -4.7 V reference is produced from the -15 V input source by a 1N750 zener diode, CR3. The error amplifier is stabilized by capacitor C1, which provides integrator response. Unity gain crossover occurs at 340 Hz. Direct current gain is equal to the open loop gain of the op amp, or approximately 94 db, thus providing accurate steady-state voltage regulation.

Output error is converted to a control angle by the control angle integrator, U2. The output of the error amp is converted to a current source which is an analog of output voltage error, by resistor R3. This error current is used to charge integrator capacitor C2. The output slope of the control angle integrator, U2, a TL081 op amp, is a positive going ramp. Rate of change of this ramp is controlled by the magnitude of the error current. Larger error current reduces charge time, whereas smaller error current increases charge time. Control angle is a function of integration time with a finite minimum which is designed to be less than SCR recovery time. The practical maximum control angle is limited only by the maximum input current of U2, and may be shown to exceed 1 million resonant cycles. The control angle integrator is reset each half cycle by the reset signal from the PU. The reset signal is unidirectionally coupled to the integrator input pin through CR2. Reset current is set by R5 at approximately 0.7 mA. Reset is limited to -0.6 V by CR1.

The output ramp of the control angle integrator is compared against a precision +5 V reference by comparator U3, an LM311. Positive feedback is applied to this stage by resistors R6 and R7, to prevent unwanted oscillation. Hysteresis level set by the resistor combination is approximately 10 mV. U3 pins 5 and 6 are tied together to prevent oscillations due to radiated pickup from output wires. The 5 V reference is derived from the +15 V power source by a REF-02 precision integrated circuit voltage reference.

Three Parameter Control Unit--Control tasks are divided among the ICs as shown in Table 3.1.5-1.

Table 3.1.5-1 Control Tasks

Device	Function
U1	Error voltage amplifier.
U2	Reference voltage buffer, voltage amp.
U3	Line voltage feedforward amp.
U4	Feedback current integrator.
U5	Output current scaling amp.
U6	Control angle integrator.
U7A	Control inhibit switch.
U7D	Soft start switch.
U8, 9, 10	Bilateral current reference sample and store.
U11	Negative voltage reference amp.
U12	Fire signal comparator.
VR1	+5.0 Vdc precision reference.

Functions are described in detail. The output voltage error amp, U1, is an LM108A with integrator response. The negative voltage signal from the PU card is compared with a negative reference to produce an error voltage that becomes more negative as output voltage decreases. Control angle is decreased with an increase in converter output load. The reference for the comparator is produced by an adjustment control located on the front panel of each control card cage. The control divides the -5.0 V reference based on relative setting, and output voltage may be regulated to any value between zero and maximum. The -5.0 V reference is produced by inverting amplifier, U11, from the +5.0 V precision reference, VR1, a PMI REF-02. The error amplifier is compensated by capacitor C1, and exhibits unity gain crossover at 340 Hz. Direct current gain is equal to the open loop gain of the op amp, or approximately 94 db, which provides accurate steady-state voltage regulation.

The reference voltage buffer, U2, an LM-108A Op Amp, is used to isolate the control potentiometer from the control circuitry. The buffer could be compensated to attenuate noise pickup from front panel and card cage wiring. The buffer also provides a low impedance source for the active stages to decouple external wiring from control circuit compensation networks.

Line Voltage Feedforward Amp--U3, an LM-108A Op Amp, generates an output voltage which is proportional to line voltage. This voltage may be used as the output comparator reference voltage. This function is selected by switch S3, position A. A change in line voltage will immediately change the threshold point of the output comparator, shown graphically in Figure 3.1.5-1. This function may be shown to be accurate by a computer program written to calculate control angle based on source voltage and load. A single printout from the program, for four steps in line input voltage, is shown in Table 3.1.5-2.

Current feedback may be derived from one of two sources, output current or resonant current. Choice of current feedback mode is selected by switches S1, and S2. Switch S3 is used to select line voltage feedforward compensation and should be used with output current feedback control. The current scaling amp U5, a Harris type HA-2625 Op Amp, conditions the output current signal from a current sense resistor which is placed in series with the load. Gain is set by resistors R10 and R11 to 32 db to increase the low level signal from the output current shunt from 50 mV to 2 V. At peak output current, the signal to the control integrator, U6, is 1 mA. Power converter output current is set by a control located on the front panel of each control card cage. Output set point may be adjusted from zero to maximum current by this control.

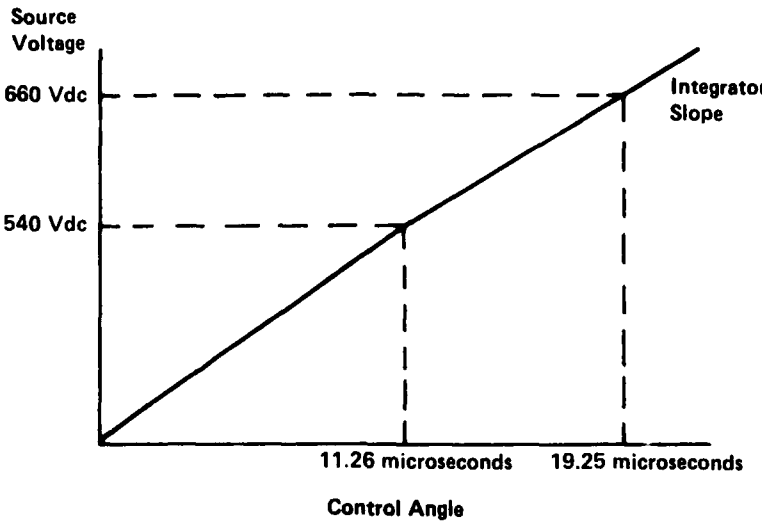


Figure 3.1.5-1 Graphical Representation of Voltage Feed Forward Control.

Table 3.1.5-2 Program for calculating SRI control.

Maximum Input Voltage = 660
Minimum Input Voltage = 540
Output Voltage = 500
Output Current = 400 amps
Output Power = 200000 watts
Resonant Capacitor = 7 Mfd
Resonant Inductor = 15.5 MicroHenries
Resonant Frequency = 15279.4 Hertz
Circuit Impedance = 1.48805 ohms

Step	Vs	Vo/Vs (q)	Alpha	Beta (deg)	Tc (Microsecond)	Fs	Irms	Idave	Ipk	Vcpk
1	540.0	0.926	62.1	172.7	11.287	11715	486.776	7.340	785.127	1208.300
2	570.0	0.877	74.8	170.2	13.598	11225	498.922	12.387	815.630	1283.690
3	600.0	0.833	86.4	168.9	15.700	10773	496.851	16.819	832.062	1338.150
4	630.0	0.794	96.5	168.3	17.548	10386	496.747	20.808	844.736	1387.010
5	660.0	0.758	105.7	168.1	19.208	10048	496.738	24.447	855.967	1433.720

Control from resonant current provides inherent line voltage compensation, improved dynamic load regulation, and good output voltage regulation. Resonant current is sensed by a current transformer located in the SRI power section resonant circuit. The current signal is rectified by CR1,2,3,4, is attenuated by R14 and R15, and is offset by current from the output current adjustment control which is located on the front panel of the control card cage. Current offset is produced by division of the +5 V reference signal by this output current adjustment control and limited by R16 to 100 microamps.

The diode portion of the resonant current signal is integrated by U4, an HA2625 op amp. Integration takes place during diode conduction of the resonant cycle. Integration is stopped when a RESET signal is produced. The integrator is reset from this signal by transistor Q4. Transistor Q3 is used to shift the logic level from +15 V to -15 V. The series connected diodes in the feedback loop of the current integrator provide active limiting of the output voltage swing during reset, to about +6.3 V.

The reciprocal of the integral of diode current is directly proportional to load and line conditions and is therefore an excellent control parameter. This control signal is produced from the preceding power switch resonant half cycle and is of opposite sign. This control signal, if used to generate the control angle for the next power half cycle, will amplify any unbalance in the SRI power stage. This inherent instability may be overcome by half-cycle delay of the resonant current feedback signal. This is implemented with a bilateral sample and hold circuit comprised of U8, U9, and U10. The quad precision analog switch, U8 is a PMI SW-03. It is configured as a DPDT switch for the two flying capacitors, C10 and C11. The two capacitors transfer the current signal to a buffer amp, U10, an LM108A during each half cycle. The MOSFET switches are driven from two complementary signals which are produced from the RESET signal by a CMOS 4013 D-type flip-flop, U9A. Delay through Q1, Q3, and Q4 is sufficient to allow charge transfer to/from the flying capacitors C10 and C11 before reset is begun.

The current feedback signal is summed at the inverting input of the control angle integrator, U6. The selection of resonant current or output current feedback is made with switch S2. With steady-state current feedback, the operating point of the control circuit is determined by the voltage feedback error amp, U1. Instantaneous changes in output current will cause immediate change in control operating point and therefore rapid correction to load changes. Instantaneous changes in load will cause a change in diode current on the following half cycle. This change will be delayed an additional half cycle by the control circuit and control operating point will be effected after a one-cycle delay.

The control integrator is reset by transistor Q2 from the RESET signal. Q1 is used as a level shifter and Q2 as a power switch. Reset time is controlled by resistor R20 and is determined from equation [12].

[12] Control integrator reset time.

$$T = Vcap \times C12 / Icharge$$

where:

$$Icharge = 15V / 4.99 \text{ kohms} = 3 \text{ mA}$$

and $$Vcap = 10 + 0.6 = 10.6 \text{ V}$$

and $$C12 = 470 \text{ pF}$$

therefore: $$T = 10.6 \text{ V} \times 470\text{pF} / .003 \text{ A} = 1.66 \text{ microseconds}$$

Reset time is actually slightly longer due to slew rate limiting of the op amp.

The control angle integrator produces a very linear ramp with slope determined from capacitor charge current. Control angle may be calculated from equation [12] using appropriate values for Vcap and I-charge. Vcap is determined as the magnitude difference between reset voltage and reference voltage. I-charge is dependent on the sum of error current from the voltage error amp, U1 and feedback current from either U5 or U10. Limits of the control angle integrator are tabulated in Table 3.1.5-3.

Table 3.1.5-3 Table of control angle integrator limits.

Charge current	Time (V-C/I)	Control Angle (degrees)
1 mA	7.33 microsecond	26
1 nA	7.33 seconds	26,395,200

The final entry for Table 3.1.5-3 corresponds to the performance limit of the control angle integrator. This value is based on input leakage current of the op amp. In practice, the maximum control time is only about 0.1 s. An attempt to produce longer closed loop control time causes latching of the error amp.

The output of the control angle integrator is compared with a reference by the fire signal comparator, U12, an LM111J comparator. Hysteresis is provided to prevent oscillation of the output signal due to stray coupling of output-to-input. The level is set by resistor network, R21 and R22 at 10 mV. This level of overdrive produces an output slew rate of about 50 V/microseconds which provides a clean, sharp leading edge for the logic circuits.

Positive and negative reference voltages are produced from one precision reference IC, VR1, a PMI REF-02. The negative reference is produced by inverting the positive reference by U11, an LM-108A op amp. The positive reference is used for current signal scaling and may be used for the fire signal comparator threshold level. The inverted voltage is used as a reference for the voltage error amplifier, U1.

A soft start circuit is implemented to limit inrush current to the SRI power stage. The soft start components are U7, C5, R2, and R3. When the STOP/RUN switch on the control card cage is set to "STOP" the start signal is low. The start signal is applied to U7D input pin 16. A low at this input closes switch section "D" and shunts the reference voltage produced by U2 to ground. Resistor R2 sums a small negative current to the inverting input of U1 so that offset errors from U2 will be removed.

When the STOP/RUN switch is placed in the "RUN" position, the start signal is high true. Analog switch U7D opens and the reference voltage buffer amp begins to charge C5 through R3. One time constant of the RC is 28 ms. Components C5 and R3 may be changed for different time constants. Larger values of C5 may require some series resistance to protect the analog switch. Reference the applications section, 3.1.5.7.

3.1.5.4 Circuit Schematics--Two control unit schematics are shown. The single-mode voltage control unit schematic is shown in Figure 3.1.5-2 and the three-mode control unit schematic is shown in Figure 3.1.5-3.

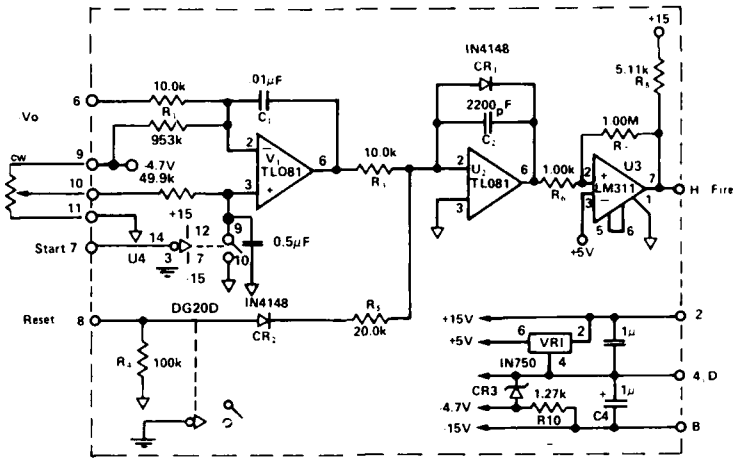


Figure 3.1.5-2 Voltage Control Unit Schematic.

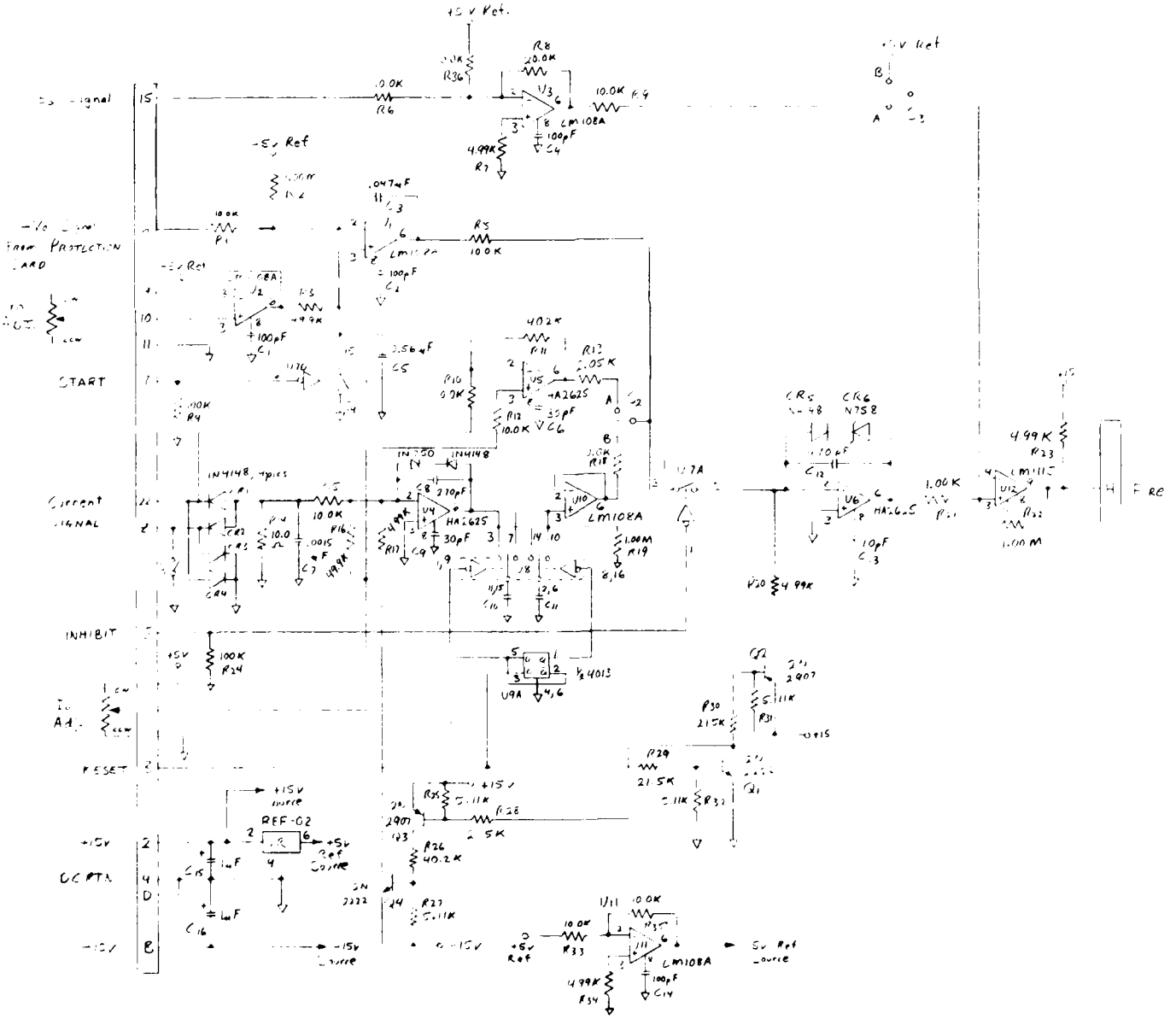


Figure 3.1.5-3 Control Unit Schematic

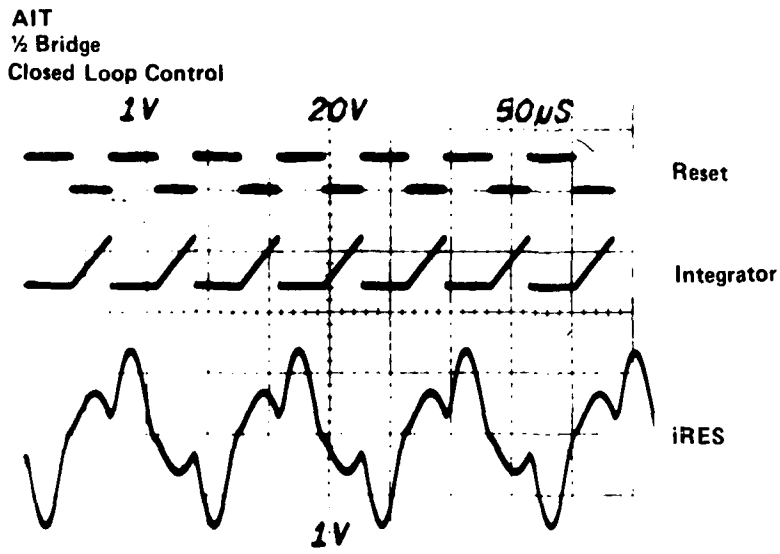


Figure 3.1.5-4 CU/PU Handshake Signals and Resonant Current

3.1.5.5 Timing Diagram--A timing diagram for operation of handshaking with the PU and for operation of the resonant current bilateral sample and store circuit is shown (Fig. 3.1.5-4).

3.1.5.6 Parts List

Voltage Control Unit:

Ref/Des	Device	Description
CR1,CR2	1N4148	Signal Diode
CR3	1N750	4.7 V Zener Diode
U1,U2	TL081	High speed op Amp
U3	LM111A	Comparator
VR1	REF-02	Precision 5 V Reference

Three Parameter Control Unit:

Ref/Des	Device	Description
CR1,2,3,4,5,8	1N4148	Signal Diode
CR6	1N758	10 V Zener Diode
CR7	1N750	4.7 V Zener Diode
U1,2,3,10,11	LM108A	Op Amp
U4,5,6	HA2625	High Speed op Amp
U7,8	SW-03	Quad CMOS Analog Switch
U9	CD4013B	Dual CMOS D Latch
U12	LM111J	Comparator
VR1	REF-02	Precision 5 V Reference

3.1.5.7 Application Information--Both control units have been tested with the three APL SRI power stages and the two Martin Marietta Denver Aerospace scale model breadboard of the 200 kW Twin Bridge power stage. Changes to the circuits may be required for new applications. Future applications study is beyond the scope of the AIT program.

3.1.5.8 Performance Data--The maximum performance for each of the control circuits is based on the ability of the unit to produce a correct control angle in less time than the power switch recovery. For the APL and Martin Marietta Denver Aerospace breadboard SRI power stages, minimum SCR recovery time is 15 microseconds. Table 3.1.5-3 shows that a minimum control time of 7.33 microseconds is possible with the circuit as designed. Both control units are designed with similar hardware and have nearly the same circuit delay time. The three mode control is slightly slower and only this circuit will be considered for performance calculation.

Maximum switch frequency of an SRI is based on power switch recovery time. This time is also the maximum time that may be allowed for the control circuit to generate a control angle. Control circuit delay is based on the critical path delay through U6 and U12, as shown in Table 3.1.5-4.

Table 3.1.5-4. Control circuit delay.

Device	Ref/Des	Delay time (ns)
HA-2625	U6	50 ns
LM-111J	U12	250 ns
	total	300 ns

Based on a minimum required control angle of 40 degrees, and a maximum Tq of 300 ns, maximum SRI operating frequency based on the delay limitation of the control unit is approximated as follows:

$$Fs(max) = 1 / (2x(40+180/40)x300ns) = 303\text{-kHz}$$

3.1.6 Housekeeping Circuit Card

3.1.6.1 Background--Functions were needed for the engineering prototype control units which are not required for flight hardware. These functions and the BBS 20-kHz ac power source are implemented on the Housekeeping Circuit Card (HCC). This is a plug card which may be moved between the three control card cages with no circuit changes required.

3.1.6.2 Theory of Operation--Three functions are implemented on the HCC, a 10 W ac power source for the BBS isolation transformers, a quad switch debounce circuit, and a quad fault latch/ display driver circuit. Each is described separately.

Ac Power Source--The ac power source is a square wave oscillator which is overload and short circuit protected. The frequency of oscillation is generated by a CMOS type 4536 programmable timer. This device allows frequency change in binary steps which may be changed by jumper selection of input programming pins. The output of the timer is isolated by a CMOS 4049 buffer from two complementary Darlington output switches, Q3-Q4 and Q5-Q6. The output is capacitor coupled to the load by C8.

Output overload protection is provided by sampling power source current. As this current approaches a preset limit, the oscillator output is disabled. The power source is self-resetting. After a short time interval, the oscillator will attempt to drive the load. Excessive source current will again shut down the oscillator if the load fault still exists. The oscillator will continue to run in this fashion indefinitely. Average power dissipated in the output stage remains well within the capability of the devices.

Switch Debounce Circuit--A mechanical switch does not provide a clean transition between states. A condition referred to as "teasing" exists for a few milliseconds while electrical contact is formed. When used to generate a logic source for electronic logic circuits, a mechanical switch produces several high-to-low transients before a continuous logic state exists. Latches are used on the HCC to remove the switch teasing and bounce and produce clean logic states. Two of four available debounce circuits are used, one for STOP/RUN and one for fault clearing.

Fault Latch--Four faults may be detected by the PU card, resonant capacitor overvoltage on either of two capacitors, source voltage out of limits, and output overvoltage. These signals are latched on the HCC by two dual D-type latches. The outputs of the latches are used to drive transistors which amplify current to drive LED displays. The display lamps are located on the front panel of each control card cage.

3.1.6.3 Detailed Design--Each of the three circuits are discussed.

Power Oscillator--The frequency of oscillation is determined by clock frequency and binary division of the CMOS 4536 programmable timer, U1. The clock frequency is set by RC components R14 and C5. Frequency of oscillation is determined by equation [13].

[13] Power oscillator frequency.

$$F = 1 / (2.3 \times R14 \times C5) = 1 / (2.3 \times 26.7k \times 100pF)$$
$$= 162,840 \text{ Hz}$$

Output frequency is determined by division of the clock, set by programming pins 9,10,11,12 and 6. A division of 8 has been selected by wiring pins 6 and 10 high for an output frequency of 20.4-kHz.

The output of the oscillator is split into two signals to drive the complementary output switches. Two unidirectional delay circuits are used to prevent simultaneous conduction of output switches. The delay times of these circuits are longer than the recovery times of the output transistors. The two delayed signals are current amplified by parallel stages of a CMOS type 4049 hex buffer, U2. The complementary outputs from the buffer drive darlington output stages Q3-Q4 and Q5-Q6. Diodes CR2 and CR3 prevent reverse overvoltage at the output transistors.

Overload protection is provided by sampling power source current from the 15 V supply. A current shunt, R6, develops a voltage proportional to drive current. This voltage is used to charge capacitor C4 through R5 and CR1. Overcurrent quickly charges C5 and Q1 is biased on. Hysteresis is provided by Q2 to prevent oscillation. The collector of Q1 produces a true logic state during overcurrent that is used to reset the oscillator, U1. When overcurrent is no longer present, C5 discharges slowly through R1 and R4, Q1 turns off and the oscillator is enabled.

When a continuous output overload (or short) exists, the power oscillator operates in a burst mode of short duty cycle. Average dissipation is maintained well below device ratings by the small duty cycle.

Switch Debounce Circuit--Switch inputs are debounced by four D-type latches. Each switch is a DPST type. One switch pole sets a latch and one pole resets a latch. The four latches are built from two dual CMOS type CD4013B D-type latches. R17 through R24 are pull-down resistors so that gate inputs are committed to a logic state while switch contacts are in flight.

Fault Latch Circuit--Fault trip signals produced on the PU card are used to clock the inputs of D-type CMOS CD4013B latches. Instantaneous faults are thus held by the latches until a reset signal is received. All four latches are reset simultaneously by a reset signal from the clear switch. This switch is located on the front panel of each control card cage. One LED display is used to indicate each of the four fault conditions. The Q output of each fault latch is current amplified by a 2N2222 transistor. The base of the output transistors are current driven at 0.5 mA through 25-kohm resistors R30, 32, 34, and 36. Current delivered to the display LED's are limited to approximately 10 mA by series connected resistors R31, 33, 35, and 37. The four LED cathodes are tied together on the front panel and returned to dc common.

3.1.6.4 Circuit Schematic--Figure 3.1.6-1 shows a schematic for the HCC. The BBS power oscillator section components are U1, U2, Q1, 2, 3, 4, 5, 6, CR1, 2, 3, C4, 5, 6, 7, 8, and R1-12. The switch debounce circuit components are U3, U4 and R17-24. The fault latch and display driver section components are U5, U6, R30-37, and Q7-Q10.

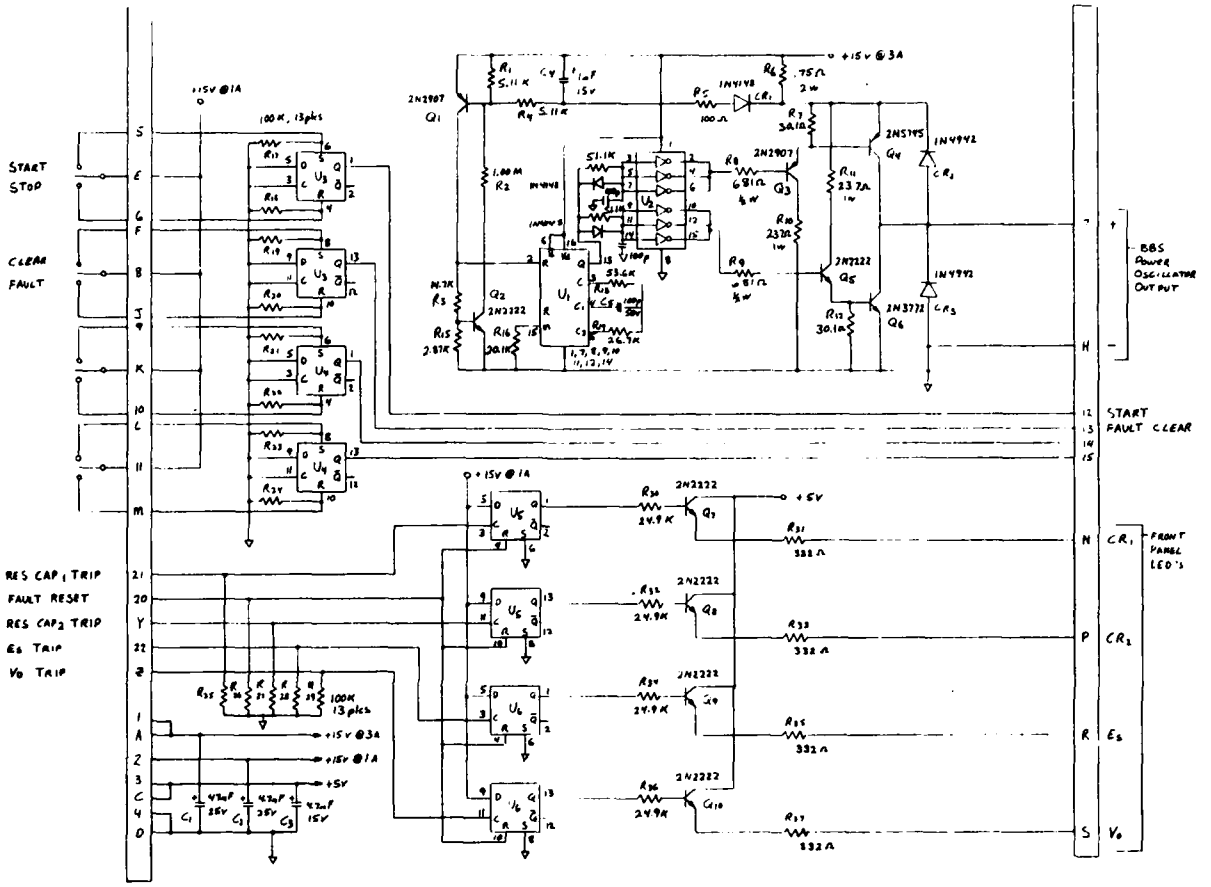


Figure 3.1.6-1 Housekeeping Circuit Card Schematic

3.2 BREADBOARD DEVELOPMENT TESTING

Developmental testing was conducted in Phase II work in order to optimize the generalized control functional circuits. The results of this test activity is summarized in the following paragraphs for each of the five common functional blocks and for both of the APL SRI power converters tested at Martin Marietta Denver Aerospace. Discussion of testing activity includes test results from two scale model SRI converters built at Martin Marietta Denver Aerospace. Temperature tests were run on the four functional blocks which were hybridized. Results of temperature tests are given in section 3.2.3.

3.2.1 Breadboard Circuit Testing of Functional Blocks

Testing of each of the five functional blocks identified in the generalized control system is summarized. Four of the five functional blocks are hybridized. All developmental testing was accomplished on discrete and integrated circuit component breadboards rather than with the hybrids. Functional testing of hybrids was conducted to assure conformance to specifications which were established for the breadboard circuits. Results of hybrid circuit functional testing is summarized in Section 4 which covers program Phase III work.

3.2.1.1 Firing Pulse Gererator Developmental Test--Test criteria for the Firing Pulse Generator (FPG) was established from SCR gate firing requirements outlined in Phase I and found in section 2.5.1.2 of this report. Gate firing pulse characteristics for the 5 kW and 10 kW APL SRI converters was measured. These data were used as a baseline for evaluating breadboard circuit FPG performance.

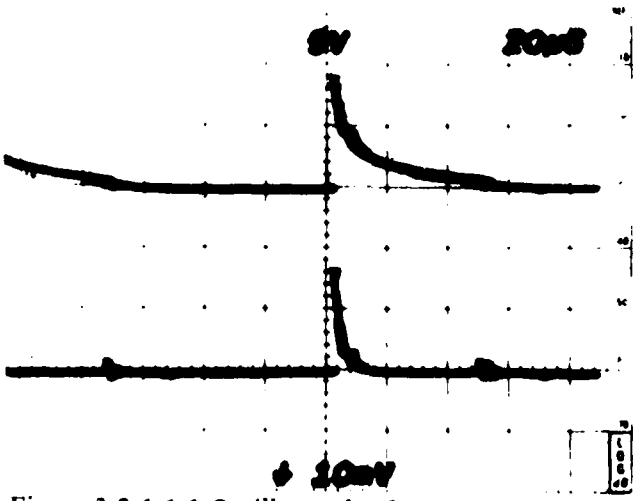


Figure 3.2.1.1-1 Oscillograph of SCR Gate Pulse – 5 kW ac-to-dc SRI.

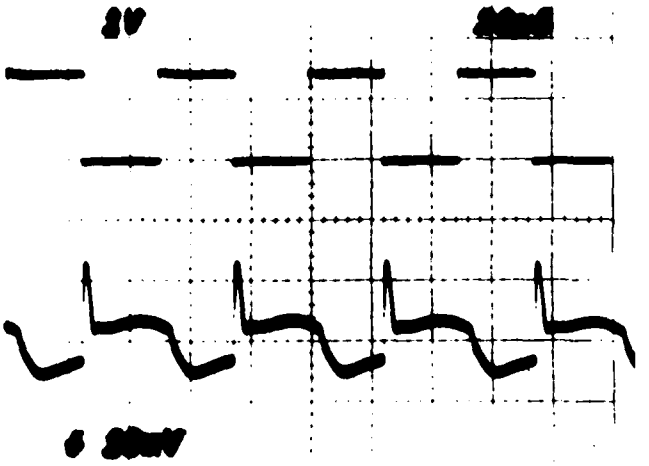


Figure 3.2.1.1-2 Oscillograph of FPG Output Pulse.

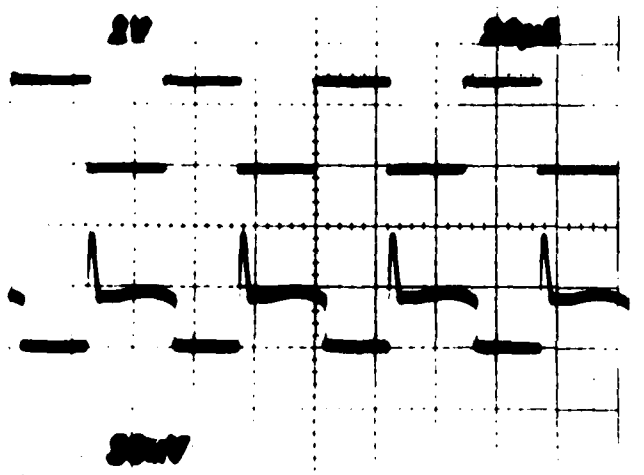


Figure 3.2.1.1-3 Oscillograph of FPG Internal Waveforms.

FPG pulse output waveforms shown in figures 3.2.1.1-2 and 3.2.1.1-3 were generated while driving Westinghouse type T507 SCR gates. These SCRs were used in the 5 kW dc-to-dc scale model converters. Loaded output peak voltage is a function of gate firing threshold voltage and varies among different SCRs within the same type.

Open circuit voltage produced by the FPG and shown in figure 3.2.1.1-4 exceeds 15 V peak, which is the maximum requirement for amplifying gate SCRs.

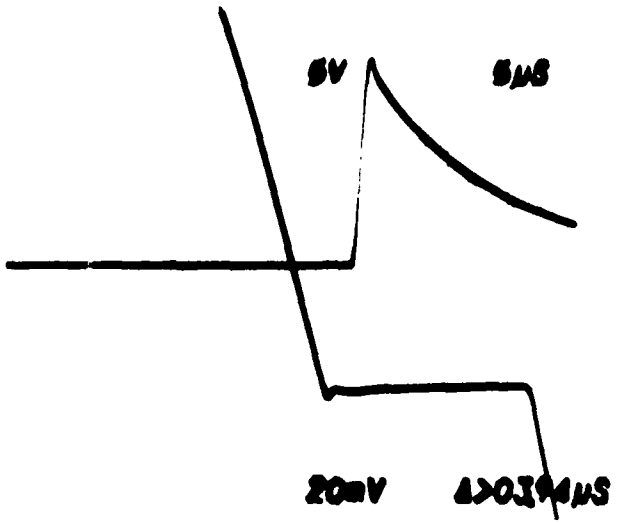


Figure 3.2.1.1-4 Oscillograph of FPG Open Circuit Pulse Output.

The FPG circuit has been demonstrated to meet the requirements for amplifying gate SCRs. Pulse quality is within the guidelines published by GE and Westinghouse for amplifying gate thyristors. Pulse output was measured to be 15 V open circuit. Peak gate current was measured at approximately 1.0 amp while firing a Westinghouse T507 type SCR, Pulse current greater than one amp did not decrease turn-on time. Pulse output to 3 amps peak at 15 V has been demonstrated. Current and voltage pulse waveforms are programmed outside the hybrid.

Testing has shown that input to output rise time delay is approximately 200 ns. This is adequate for SRI converters using SCRs or MOSFETS operating at switching frequency to 100-kHz.

3.2.1.2 Back Bias Sensor Developmental Test--The back bias sensor is tasked to measure reverse bias voltage across an SCR. The reverse bias voltage is limited to a single diode forward voltage drop because of the antiparallel diode wired in reverse across the SCR. The BBS must measure a signal as small as 50 mV in the reverse direction and block 600 Vdc in the forward direction.

Figure 3.2.1.2-1 depicts the BBS input signal in the upper trace and resonant current in the lower trace. The upper trace is a waveform of an SCR in an SRI power converter operating from a 100 Vdc source. Forward voltage is above and off the oscilloscope screen. Shown is the diode forward voltage drop which occurs during reflected resonant current flow.

Figure 3.2.1.2-1 depicts the BBS signal input, upper trace and associated resonant current, lower trace.

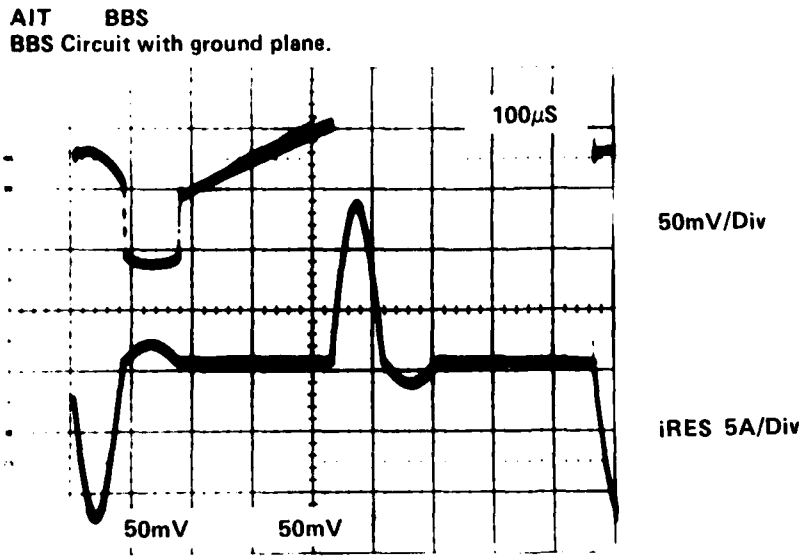


Figure 3.2.1.2-1 BBS Input Signal, Upper Trace and Associated Resonant Current, Lower Trace.

Clean BBS signals are required for cyclical stability of the SRI converter. Four improvements were made to the original BBS circuit design to reduce noise susceptibility:

1) A ground plane was added.
2) A capacitor was added between the input pins of the voltage comparator.
3) Compensation pins are shorted together to prevent stray coupling to the output wiring from these unused inputs.
4) Physical layout of the circuit components was arranged to minimize stray coupling of output to input.

Figure 3.2.1.2-2 depicts the BBS signal before it is applied to the optical isolator.

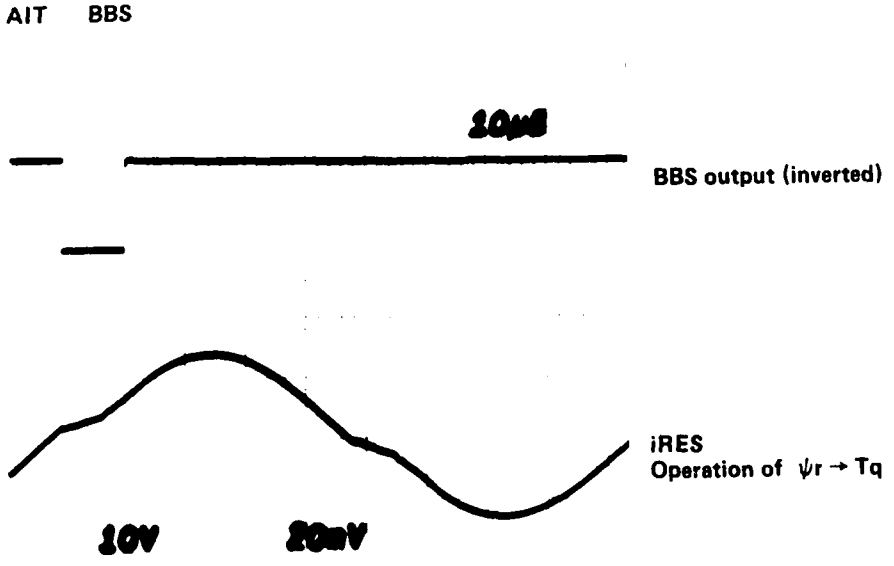


Figure 3.2.1.2-2 The BBS Signal Before it is Applied to the Optical Isolator.

Figure 3.2.1.2-3 depicts the BBS signal output at the circuit card edge connector. The leading edge of the BBS signal provides oscillator timing in conjunction with the PU circuit.

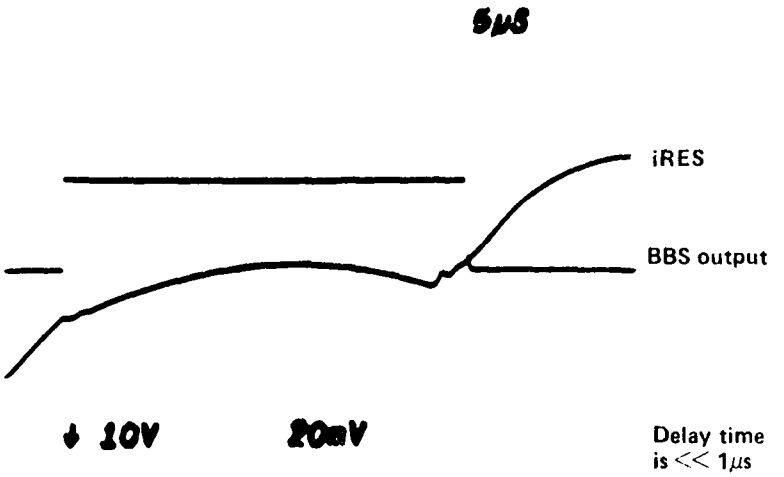


Figure 3.2.1.2-3 The BBS Signal Output at the Circuit Card Edge Connector.

The first test of the BBS circuit produced an excessive delay, which was inadequate for 100-kHz operation. The delay was traced to two causes, output optocoupler circuit delay and input comparator delay which was caused by high back bias threshold level. The delay was reduced to 800 ns with the addition of an active pullup current source for the output of the optocoupler and reduction of the threshold level of the input comparator.

One additional observation was made during testing of the breadboard BBS circuit. When used in conjunction with the three phase converter, it was found that a signal derived from back bias cannot be used efficiently for firing SCRs as diodes. It was determined that a BBS circuit, even if designed with no delay, cannot deliver a properly timed signal because of the inherent delay in back bias voltage.

The back bias delay is caused by snubber networks. Since SCRs require about 1 microsecond to turn on, they must be fired before the snubbers have stopped conducting current so that they may take over current conduction. SCRs fired from a BBS signal will allow the resonant circuit to open while the SCRs are turning on. This allows reversal of resonant circuit voltage which interferes with the BBS signal and an unstable condition results. SCR timing for the three phase converter is derived from a zero current detector so that BBS delay does not degrade three phase converter performance.

Figure 3.2.1.2-4 depicts BBS signal delay. It is clearly seen that diode back bias voltage lags zero current crossing by 1 to 2 microseconds.

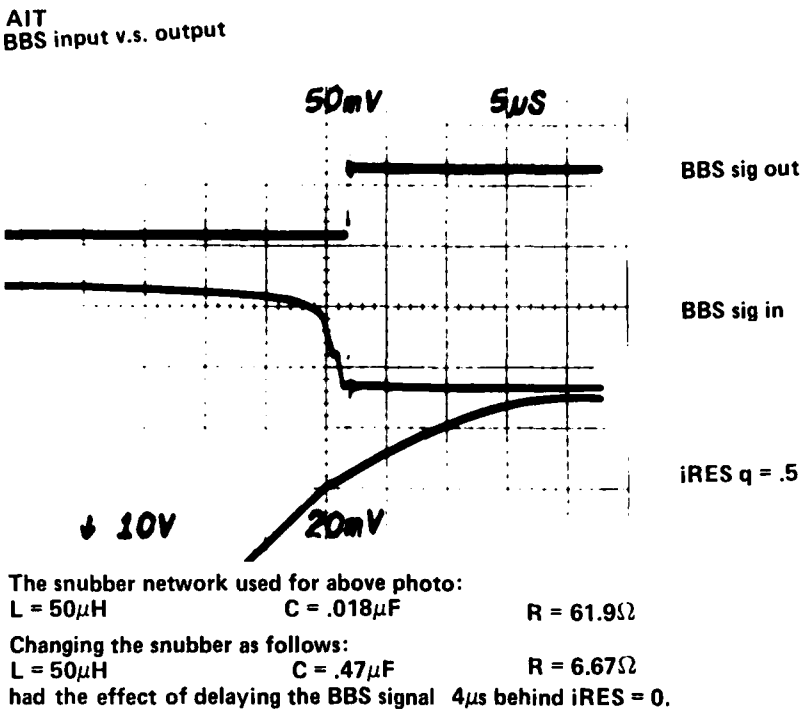


Figure 3.2.1.2-4 BBS Signal Delay.

One of the protection functions required to prevent failure of an SRI power converter eliminates the possibility of operation when input-to-output voltage ratio (voltage ratio "q") approaches unity. Unity "q" represents undefined operation. In practice, operation in this mode is equivalent to operation in an open load at maximum switch frequency. Component stress ratings are quickly exceeded.

The BBS function can serve to eliminate the possibility of power converter oscillation at unity voltage "q". When this condition exists, reflected resonant current (diode current) is equal to zero and a BBS signal is not produced. Operational test to ensure proper BBS circuit function was run at "q" nearly equal to unity. Diode current was nearly unmeasurable.

Figure 3.2.1.2-5 depicts BBS output during SRI operation at nearly unity voltage "q". Resonant current is included to illustrate the magnitude of diode current. Further reduction of voltage "q" caused the BBS output to disappear and converter oscillation to cease.

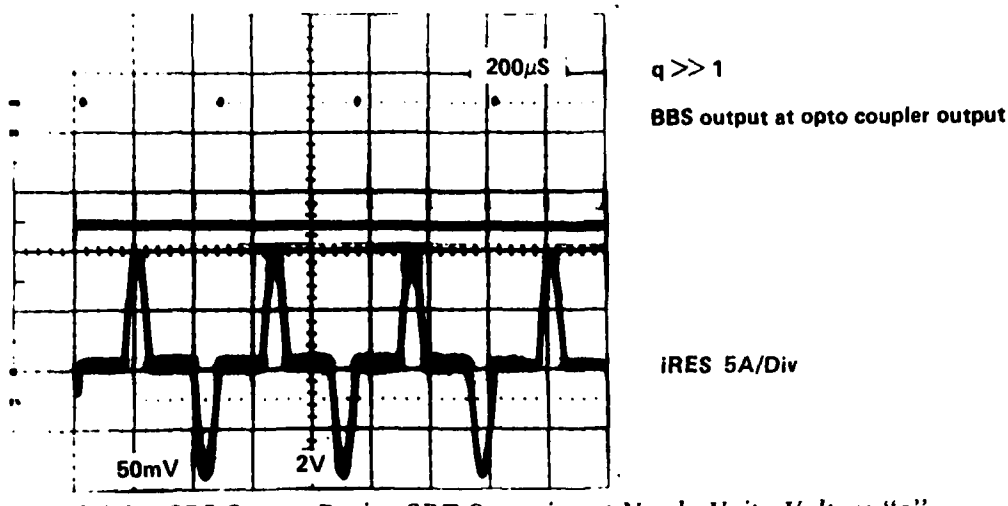


Figure 3.2.1.2-5 BBS Output During SRT Operation at Nearly Unity Voltage "q".

The BBS input-to-output delay of 0.8 microseconds meets the design goal of 1 microsecond. Operation of the comparator up to 100-kHz is shown by an oscillograph photo in figure 3.2.1.2-6.

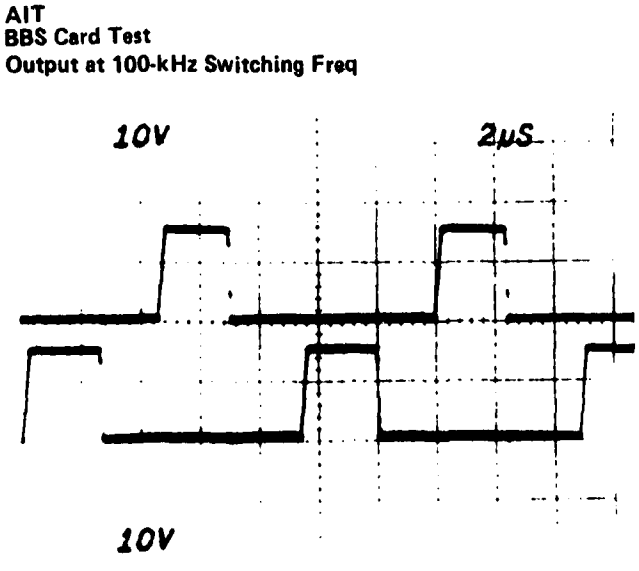


Figure 3.2.1.2-6 BBS Operation at 100-kHz.

3.2.1.3 Protection Unit Developmental Test--The Protection Unit is tasked to provide two functions, protection from component overstress and power oscillator timing. These tasks have been separated into two separate sections of the PU circuit hybrid, Analog Protection and Digital Timing. Each section was tested separately and are presented in different sections.

The Digital Timing section functional requirements are somewhat different for dc-to-dc and 3 phase ac-to-dc converter operation. These different requirements are addressed in section 3.1.3.2 of this report. Test data and timing diagram photographs are presented separately.

3.2.1.3.1 Analog Protection Tests--The following circuit functions were tested:

1) Resonant capacitor overvoltage trip.
2) Source voltage trip.
3) Output voltage buffer amplifier.
4) Output voltage (OVP) trip.
5) Analog protection logic.
6) Start pulse sign logic.

Fault trip signals and logic signals were tested for proper logic states and found to be as designed.

The input amplifiers were tested for gain, common-mode rejection, and bandwidth. Results of gain and common-mode rejection tests are listed in table 3.2.1.3-1. Bandwidth was measured to 10-kHz and found to be flat to within 1 db. Detailed data was not collected for PU amplifier bandwidth.

Table 3.2.1.3-1 Analog Protection Gain Tests

	---- Amplitude ----		
Amplifier	Input	Output	Deviation (%)
Res. Cap 1	10.000 V	10.013	0.13
Res. Cap 2	10.000 V	9.989	0.11
V source	10.000 V	10.102	1.02
V output	10.000 V	10.059	0.59

Table 3.2.1.3-2 Analog Protection Common-Mode Rejection

	---- Amplitude ----		
Amplifier	Input	Output	Rejection (db)
Res. Cap 1	1.50 V p-p	10 mV	43.5 db
Res. Cap 2	1.50 V p-p	12 mV	41.9
V source	1.50 V p-p	11 mV	42.7
V output	1.50 V p-p	18 mV	38.4

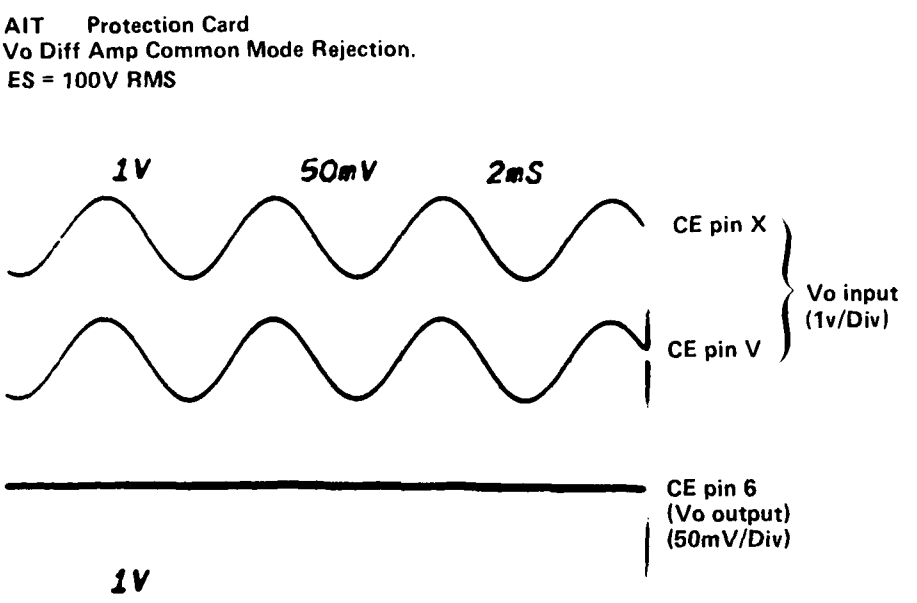


Figure 3.2.1.3-1 Analog Protection Common-Mode Rejection.

3.2.1.3.2 Digital Timing Tests--The following circuit functions were tested:

1) Start function,
2) Converter protection shutdown,
3) Fire Group Generator,
4) Tq Timer,
5) Control Unit handshaking (Fire / Reset),
6) Three Phase Unit handshaking (RFT / SFT), and
7) Fire Diodes signal generator.

Logic timing for PU normal operation in the half-bridge dc-to-dc converter is shown in figure 3.2.1.3-2.

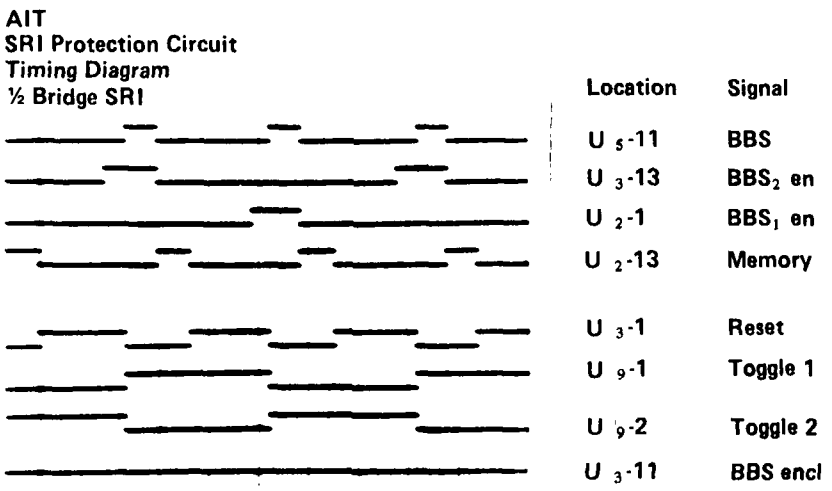


Figure 3.2.1.3-2 PU Logic Timing Diagram, dc-to-dc.

Logic timing for PU normal operation while operating in the APL three phase-to-dc 5 kW converter is shown in photo 3.2.1.3-3. Figures 3.2.1.3-4 and -5 show resonant current waveforms taken concurrently with the timing diagram photograph. Input and output conditions during the test are as follows:

V source = 208 V RMS Three Phase
V out = 204 Vdc
Rload = 8.3 ohms

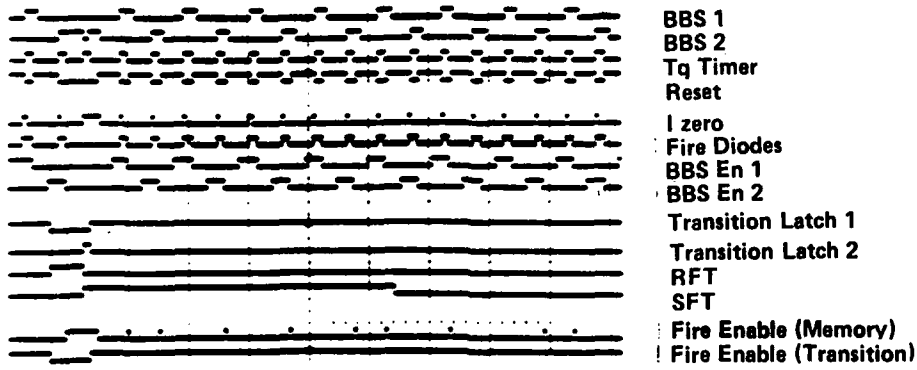


Figure 3.2.1.3-3 PU Logic Timing Diagram, Three Phase ac-to-dc.

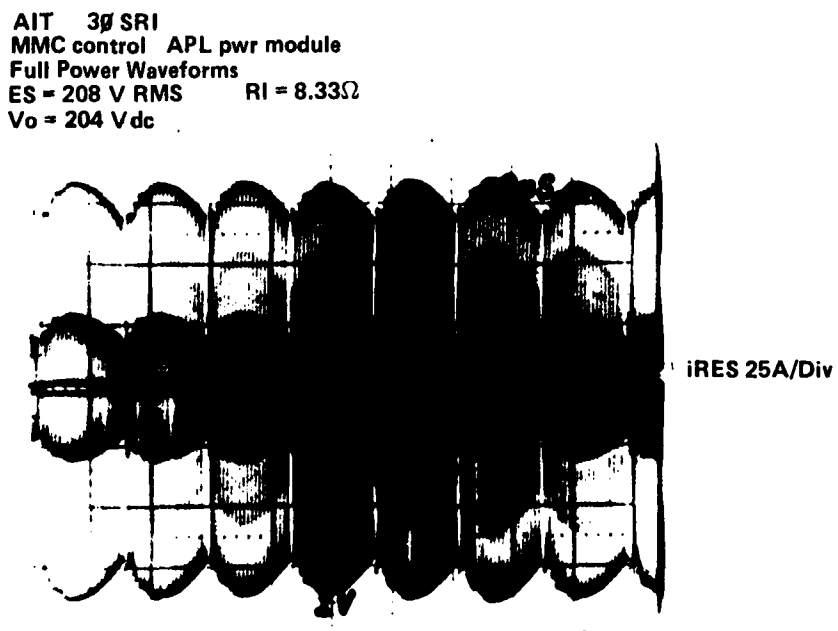


Figure 3.2.1.3-4,5 PU Resonant Current Waveform

A major issue was resolved during functional testing of the PU circuit. This issue occurs during three phase operation only and involves firing of SCRs as diodes. Timing of SCRs used as diodes was conceptually derived from one of two sources, BBS signal or a zero current signal. Architechturally, derivation of SCR diode timing from BBS signals is more desirable, easier to implement, and offers an overall simpler solution.

During test of the APL three phase ac-to-dc SRI, it was found that SCR timing derived from BBS signals caused excessive SCR snubber dissipation. In order to optimize SRI power converter efficiency, an architectural change was made to fire SCRs used as diodes from timing derived from resonant current.

Figure 3.2.1.3-6 shows the BBS signal in the upper trace, resonant current in the center trace, and the "Fire Diodes" signal in the lower trace. The resonant current waveform was produced from BBS signal derived timing for firing SCRs as diodes.

The following photographs were taken while operating the APL 5 kW ac-to-dc converter from a dc source. Input and output conditions during the test are as follows:

V source = 120 V RMS Three Phase
V out = 100 Vdc
Rload = 6.25 ohms

Operation of the three phase converter on a single phase pair using a dc voltage source produced stable, distorsion-free oscilloscope photographs. This technique was used extensively during functional testing of the PU circuit.

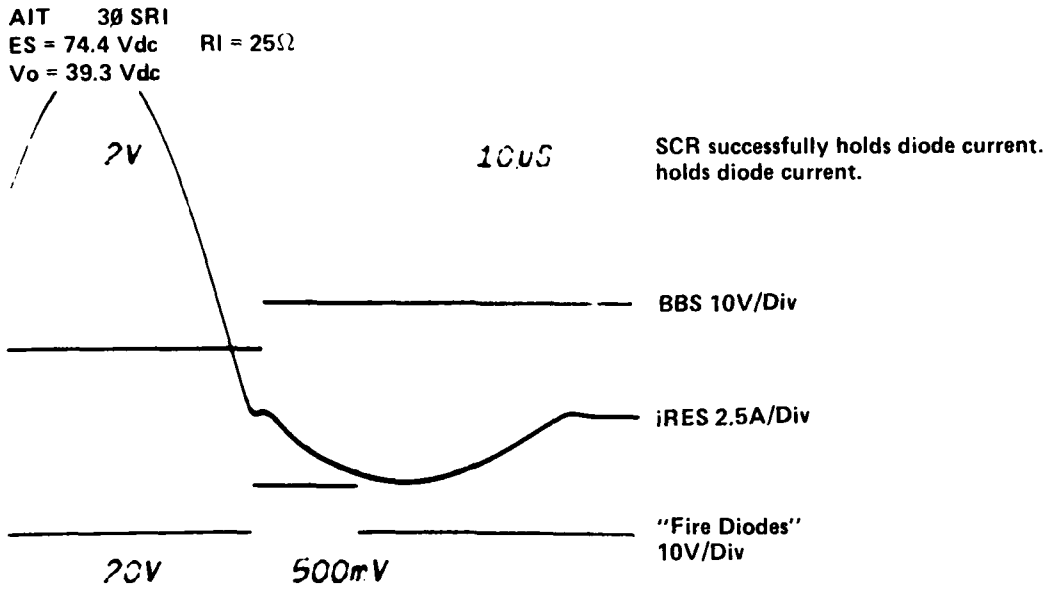


Figure 3.2.1.3-6 Signal Timing for SCRs Used as Diodes.

Timing of SCRs used as diodes is derived from resonant current amplitude in the existing design of the AIT control architecture. A photograph which compares the BBS signal and "Fire Diodes" signal to resonant current is shown in figure 3.2.1.3-7.

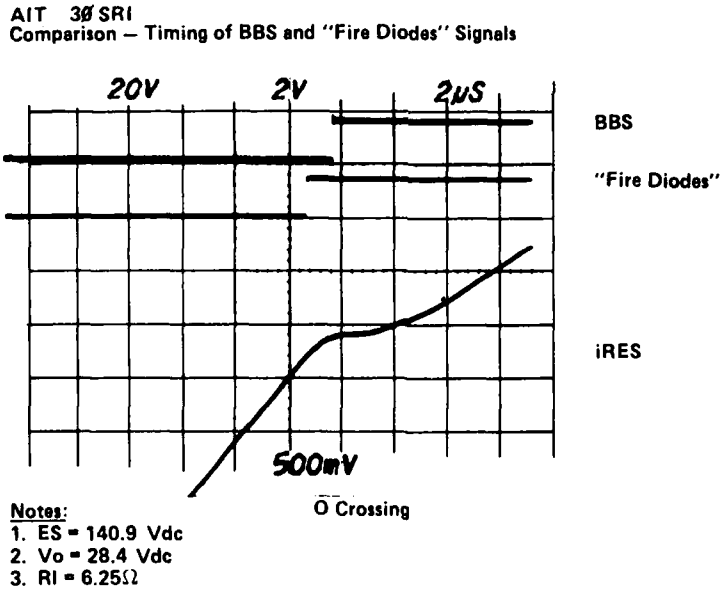


Figure 3.2.1.3-7 Signal Timing for SCRs Used as Diodes, Resonant Current Derived.

Figure 3.2.1.3-8 shows construction of the "Fire Diodes" signal used in the existing three phase architecture. The upper trace is the resonant current input which is applied to a current magnitude comparator. The second trace from the top is the output signal from the current magnitude detector. The third trace is the derived "Fire Diodes" signal after conditioning by the PU circuit. The bottom trace shows resonant current for reference.

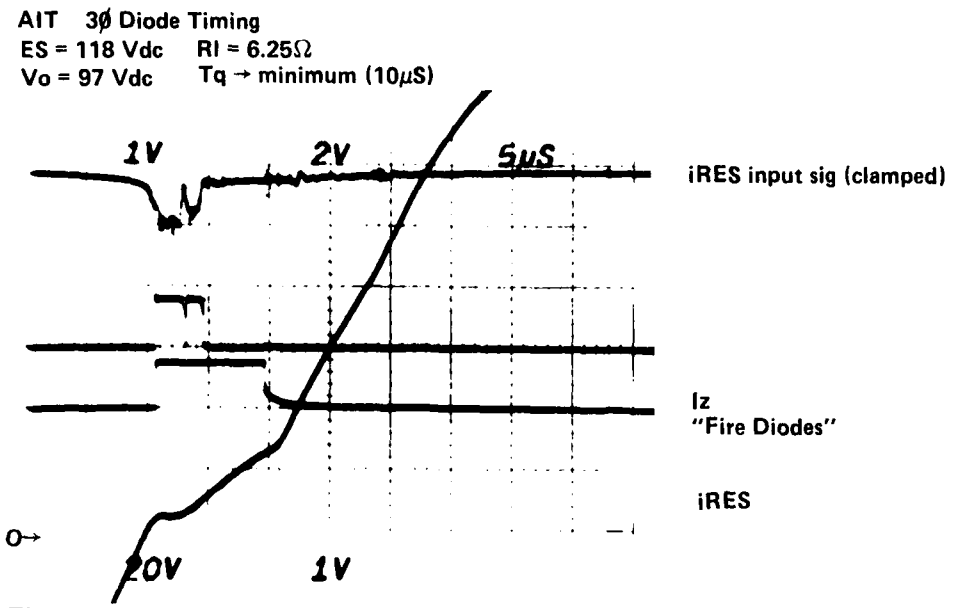


Figure 3.2.1.3-8 Derivation of the "Fire Diodes" Signal.

3.2.1.4 Three Phase Unit Developmental Test--The TPU is tasked to provide a logic function for selection of SCR pairs based on line input phase pairs. Functional testing was conducted to verify correct circuit operation before attempting to operate the APL 5 kW three phase ac-to-dc converter.

Functional testing was divided into three categories:

1) Static test,
2) Open loop dynamic test, and
3) Closed loop dynamic test.

Each of the three tests are discussed and results presented.

TPU Static Test--Static functional test of the AIT TPU is divided into 5 sections:

1) Voltage reference test,
2) Three Phase Decoder operation,
3) Group Enable signal generation,
4) SCR fire signal generation, and
5) Diode fire signal generation.

Test results are found in table 3.2.1.4-1.

Table 3.2.1.4-1 TPU Static Test Summary

Item	Test	Condition	Result	Go	No-Go
1.	Voltage Ref.	6.80 V	6.976		
2.	3 Decoder	V12			
		V21			
		V13			
		V31			
		V23			
		V32			
3.	Group Enable	Phi 12	Group 1		
		Phi 13	Group 2		
		Phi 21	Group 1		
		Phi 23	Group 2		
		Phi 31	Group 1		
		Phi 32	Group 2		
		Output	SCR	Diode	
4.	SCR Fire Signal	11			
		12			
		13			
		14			
		21			
		22			
		23			
		24			
		31			
		32			
		33			
		34			

Signal conditions during the group enable and fire signal tests are summarized in tables 3.2.1.4-2 and -3.

Table 3.2.1.4-2 TPU Group Enable Static Test Signal Table

TPU Card Pin	"True" Fire BBS	Group Enable Output Ø12 12	Ø13 12	Ø21 12	Ø23 12	Ø31 12	Ø32 12
M	11	10	10				
N	12	01	01				
11	13			01		01	
12	14			10		10	
P	21			10	10		
R	22			01	01		
13	23	01				01	
14	24	10				10	
S	31				10	10	
16	32				01	01	
15	33		01	01			
T	34		10	10			

8 Group Enable 1
J Group Enable 2

Table 3.2.1.4-3 TPU SCR/DIODE Static Test Signal Table

TPU Card Pin	SCR	SFT	PHI	SCRs e_1	e_2	e_3	F_D	FG1	FG2	PHI	Diodes e_1	e_2	e_3	F_D	FG1	FG2
17	11	∫	12	+	−	0	0	1	0	21	−	+	0	1	0	∫
U	12		12	+	−	0	0	0	1	21	−	+	0	1	∫	0
18	13		21	−	+	0	0	0	1	12	+	−	0	1	∫	0
V	14		21	−	+	0	0	1	0	12	+	−	0	1	0	∫
19	21	∫	23	0	+	−	0	1	0	32	0	−	+	1	0	∫
22	22		23	0	+	−	0	0	1	32	0	−	+	1	∫	0
20	23		32	0	−	+	0	0	1	23	0	+	−	1	∫	0
X	24		32	0	−	+	0	1	0	23	0	+	−	1	0	∫
21	31	∫	31	−	0	+	0	1	0	13	+	0	−	1	0	∫
Y	32		31	−	0	+	0	0	1	13	+	0	−	1	∫	0
W	33		13	+	0	−	0	0	1	31	−	0	+	1	∫	0
Z	34		13	+	0	−	0	1	0	31	−	0	+	1	0	∫

e_1, e_2, e_3 Symbols
+ = 1
− = 0

0 = Open
∫ = Diode Output

Goes True on Low to High Transition

Open Loop Dynamic Tests--Functional testing of the AIT TPU breadboard card was facilitated through parallel sharing of logic signals from the existing APL three phase ac-to-dc control unit. Fourty-eight BNC-type "T" connectors allowed signals generated from the APL SRI power module to be routed to the existing APL control unit and to the AIT control unit under development.

The SRI power module was run under closed loop control from the APL discrete component control unit. All control and feedback signals were input to the AIT control unit under test. The following four photographs were taken from AIT control unit logic signals which were derived from inputs from the operating SRI power module.

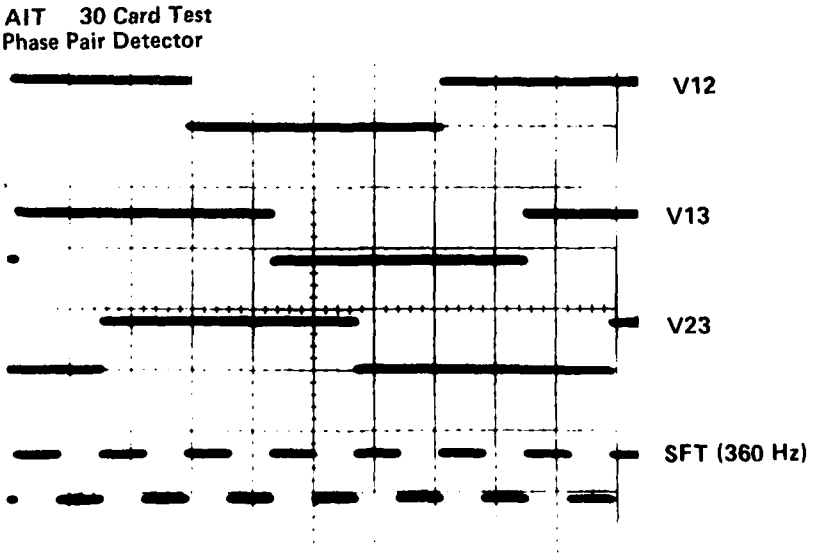


Figure 3.2.1.4-1 Phase Pair Detector Signals and SFT.

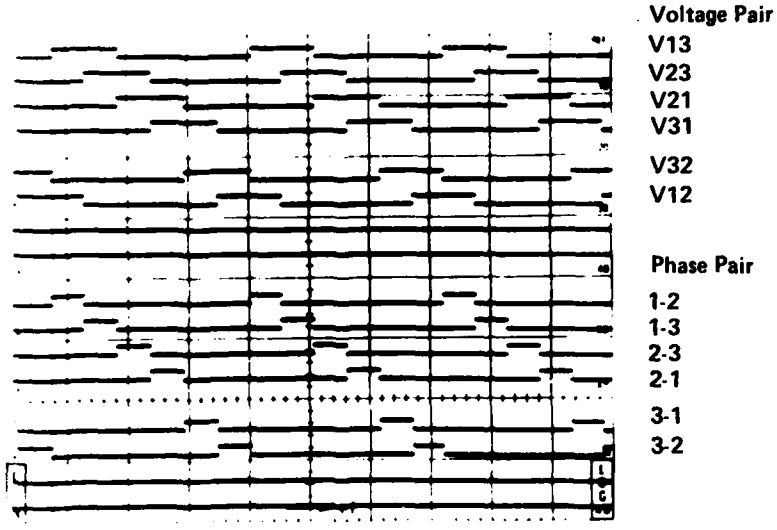


Figure 3.2.1.4-2 Phase Pair Decoder Signals.

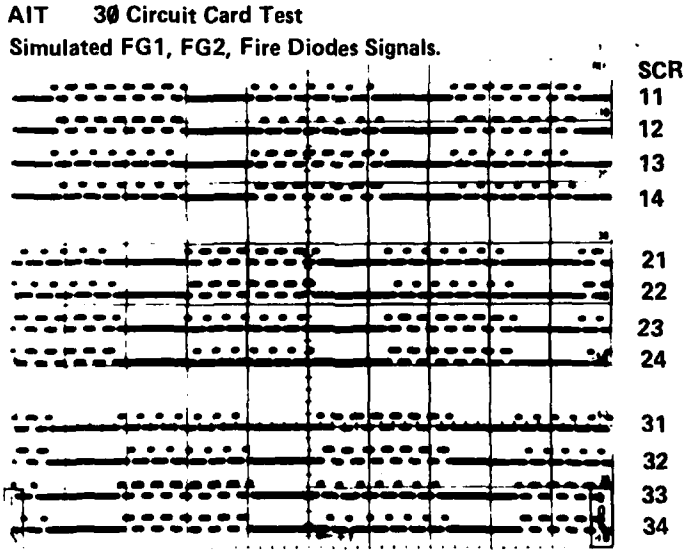
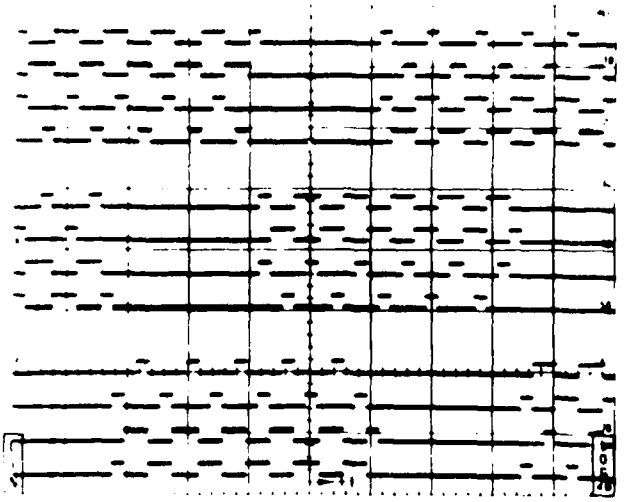


Figure 3.2.1.4-3 SCR Fire Signals, For all Six Phase Pairs.



Same as above photo.

Test Conditions

Fs = 2 kHz

60Hz 30
line input

Simulated fire signals
from test tool.

Figure 3.2.1.4-4 SCR Fire Signals, Detail.

Closed Loop Dynamic Tests--Logic was verified with TPU static and open loop tests before control was attempted using the AIT controller for a closed loop test.

The TPU was functionally tested in successive logical increments to minimize risk of damage to the SPL SRI power stage due to a logic signal error. The TPU breadboard circuit was verified on each phase pair using dc source voltage before three phase source voltage operation was attempted. Handshaking signals used to detect and transition logic during voltage source phase changes was generated from a signal synthesizer.

After functional testing was conducted on all six phase pairs using dc input, three phase testing was begun. Some interesting results were obtained and are summarized as follows:

1) Large distorsion of the line input occurred.
2) Ratcheting of phase transition logic occurred.
3) Phase pairs were misselected due to line transients.

Two photos of line input distorsion while operating the APL SRI are shown in Figures 3.2.1.4-5 and 6.

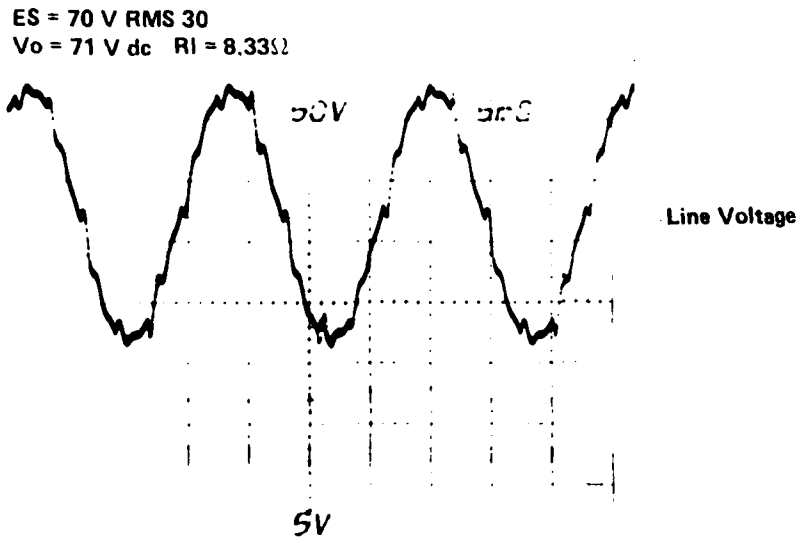


Figure 3.2.1.4-5 Line Input Distortion.

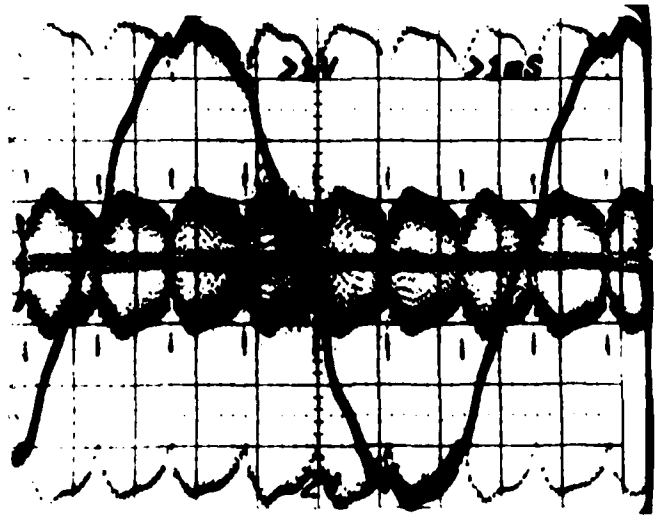


Figure 3.2.1.4-6 Line Input Distortion.

The line voltage fluctuations occurred when the power stage idled during phase transition. Several microseconds are required for resonant current commutation to zero. Power switches are not enabled until current has returned to zero. Phase transition logic toggled as a result of line distorsion.

Figure 3.2.1.4-7 shows a normal waveform of resonant current when phase selection is correct. Increased power converter demand caused larger line input transients which in turn caused ratcheting of phase decoder logic. Figure 3.2.1.4-8 shows the resonant current waveform when phase logic is incorrectly selected.

ES = 208 V RMS 3ø
Vo = 104 Vdc RI = 8.33Ω

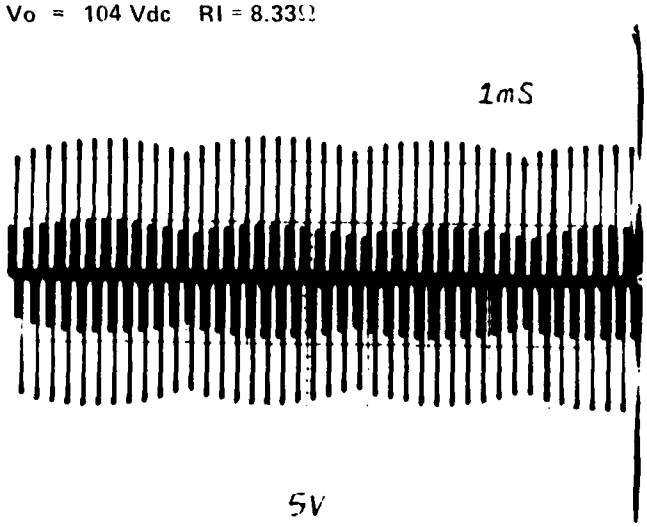


Figure 3.2.1.4-7 Resonant Current at 1300W Output.

AIT 3ø SRI
High Power Current Waveforms
ES = 186 V RMS 3ø
Vo = 150 Vdc RI = 8.33Ω

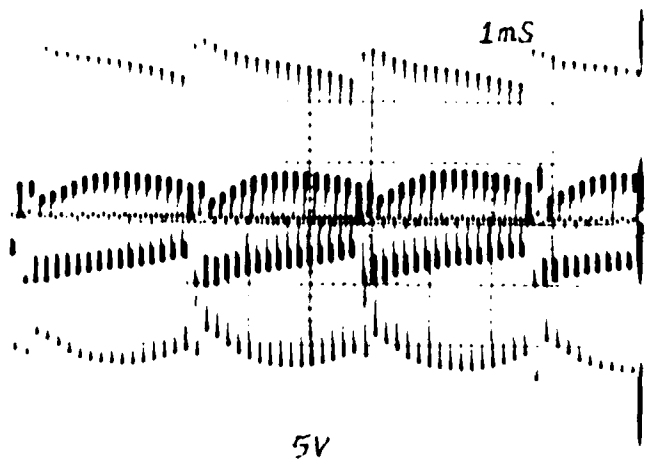


Figure 3.2.1.4-8 Resonant Current at 2700W Output.

The condition was easily corrected with the addition of increased hysteresis. The increased hysteresis required adding line voltage input buffer amplifiers to the TPU circuit. These additions are incorporated in the hybrid circuit design.

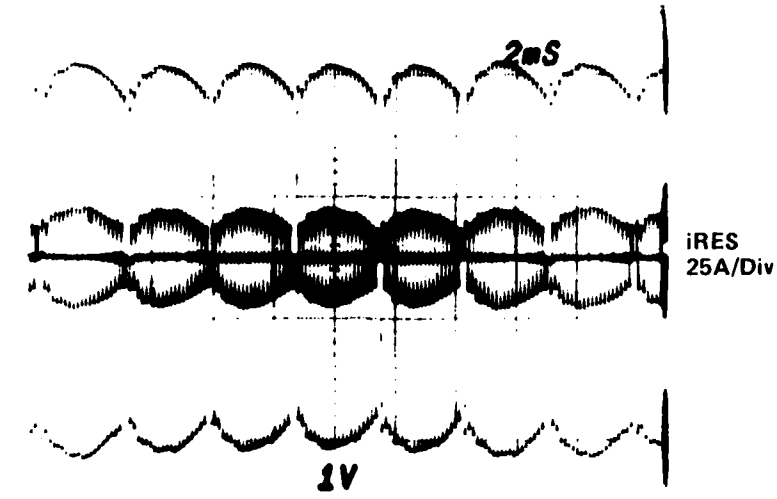


Figure 3.2.1.4-9 Resonant Current at 5000-W Output.

Testing of the APL three phase SRI was accomplished over a line input voltage range of 50 Vac to 240 Vac three phase. A three section variable transformer produced a division of the 208 Vac line source. The output impedance of this device caused increased line transients during phase transitions. The amplitude of the transients precluded using a increased hysteresis on the TPU to prevent misselection of phase pairs.

This difficulty was overcome by disabling the RFT signal for several resonant cycles immediately following a phase transition. Results of this circuit improvement are shown in Figures 3.2.1.4-10 and 11.

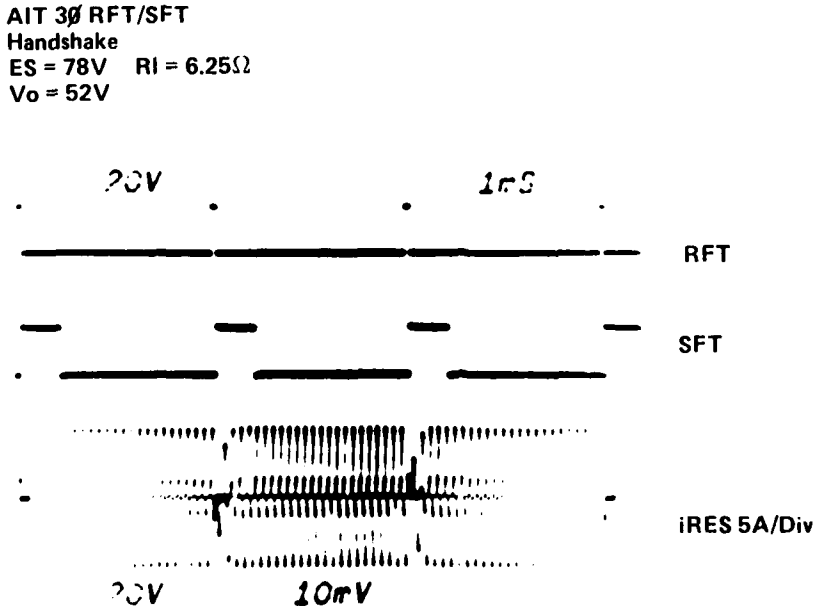


Figure 3.2.1.4-10 Phase Transition Handshaking Logic Signal Four Phase Transitions.

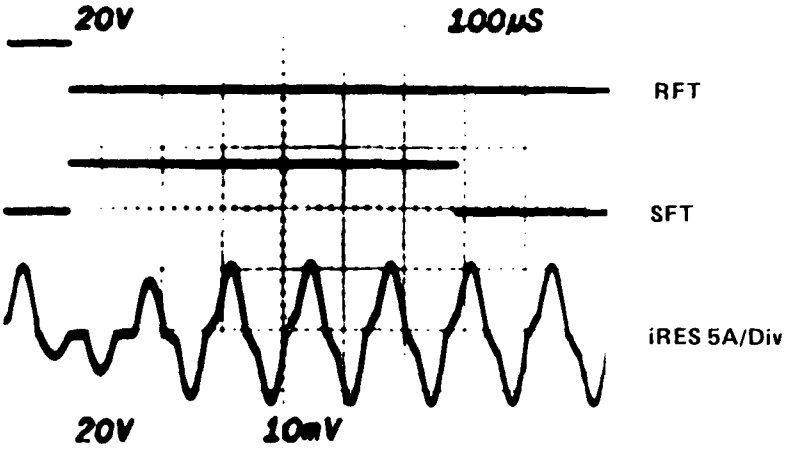


Figure 3.2.1.4-11 Phase Transition Handshaking Logic Signal, Detail of a Single Phase Transition.

3.2.5 Control Unit Developmental Test

The CU is tasked to generate a fire signal in response to load conditions. Functional testing was conducted for two purposes, first to determine an acceptable control technique which would be adaptable to all three APL SRI power converters, and second to test performance of this control technique with the two dc-to-dc converters and the ac-to-dc converter.

Control Loop Tests--A control technique was desired which would provide the following control functions over a 10:1 load range and ± 15% of nominal line voltage change:

1) Steady-state voltage regulation of ± 5%
2) Current-mode control
3) Transient response to dynamic load changes up to 1 kHz.

Output voltage, resonant current, output current, and source voltage were tested as control parameters. These are discussed in the following sections which describe control tests. Control tests are further subdivided into three areas of concern:

1) Voltage Control and CU Timing,
2) Current-mode Control, and
3) Control with an Output Transformer.

Voltage Control and CU Timing--Closed loop tests were attempted only after verification of the voltage control circuit. Control unit functions were verified by driving the half-bridge SRI from a frequency synthesizer to establish oscillation of the power converter. Voltages, timing and operating states were verified.

When the control loop was closed, voltage regulation was immediately established. Figure 3.2.5-1 shows CU timing.

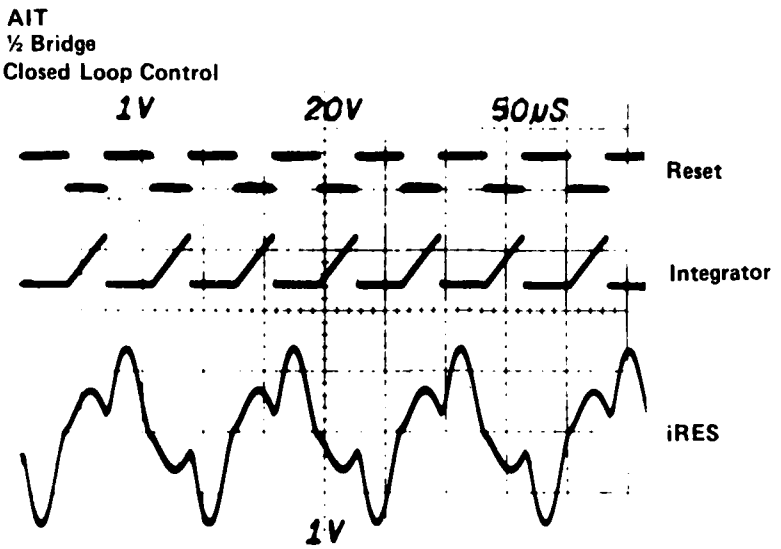


Figure 3.2.5-1 CU/PU Handshake Signals and Resonant Current.

Current-Mode Control--Perhaps the first mechanization of current-mode control was invented and patented by F.C. Schwartz (4). This control technique is referred to as Analog Signal to Discrete Time Interval Conversion (ASDTIC). The first current-mode control tests conducted on the AIT program used an implementation of the Schwartz design.

There are several advantages to the ASDTIC current-mode control method:

1) Transient response to load changes occur on a cycle-by-cycle basis.
2) Source voltage compensation is provided inherently. Separate feed-forward control is not required.
3) The feedback signal is easy to obtain.

F.C. Schwartz described use of resonant current as a input parameter for the ASDTIC control circuit. Resonant current which flows during antiparallel diode conduction equates to residual resonant current which was undamped by load resistance. The integral of this residual current is proportional to load resistance, switching frequency, and the ratio of source to load voltage.

Tests were conducted to measure the relationship of diode current to load current. A half bridge SRI was run under the following conditions:

1) Source voltage = 100 Vdc
2) Output voltage = 15.0 Vdc
3) Load = ACME PSL-1000 Electronic Load

The ACME electronic load box was connected as a constant voltage, variable current sink by wiring a zener diode between the load and control input. The SRI was driven from a frequency synthesizer over the range of 5 to 10-kHz. The diode current integral remained constant over the entire frequency range.

The results of this test are shown in figures 3.2.5-2 and -3.

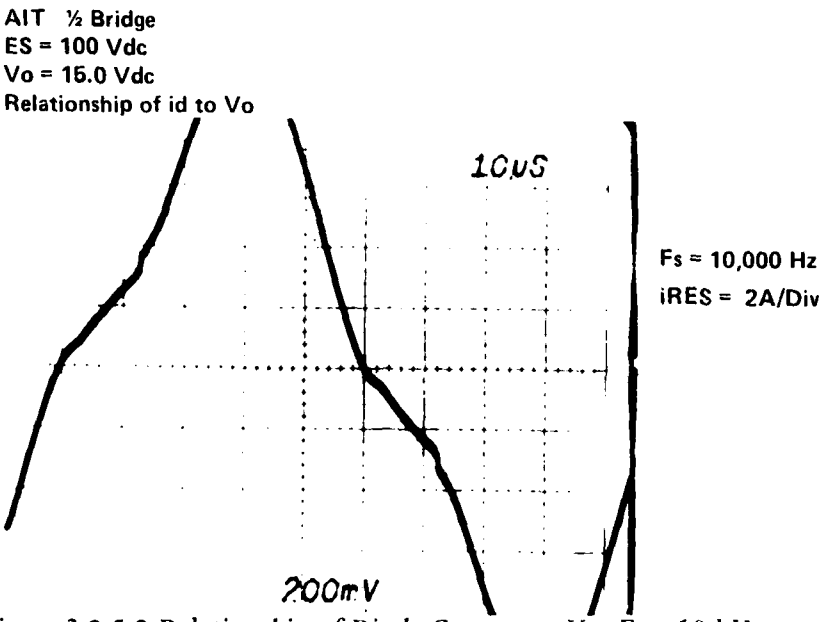


Figure 3.2.5-2 Relationship of Diode Current to Vo, Fs = 10-kHz

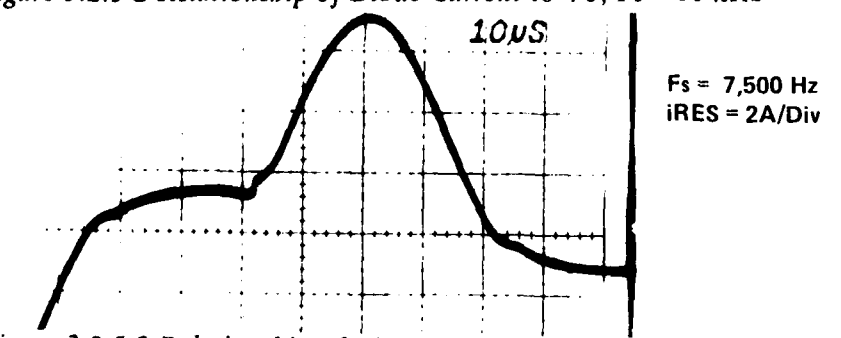
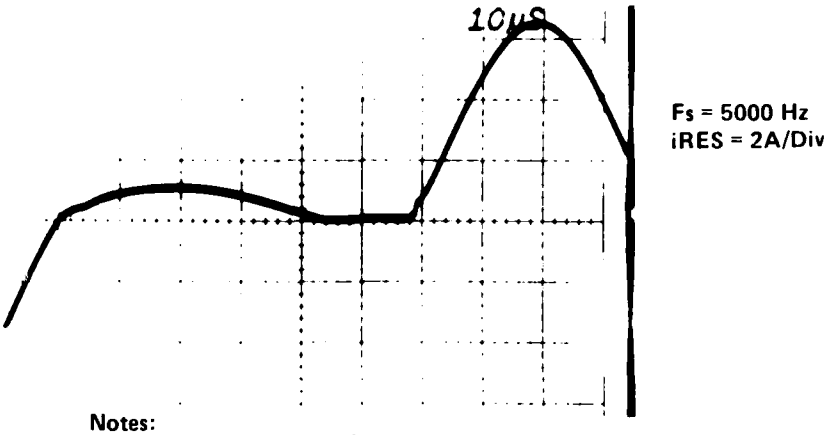


Figure 3.2.5-3 Relationship of Diode Current to Vo, Fs = 7.5 kHz



Notes:
1. Loaded with Acme PS² L-1000, "R" mode.
2. Load adjusted for Vo = 15.0 VDC.

Figure 3.2.5-4 Relationship of Diode Current to Vo, Fs = 5-kHz

Closed loop tests were performed using an ASDTIC current control circuit. The advantage of this control method is readily apparent from review of test data. This data is presented in table 3.2.5-1. Vref is the output signal from the diode current integrator.

Table 3.2.5-1 ASDTIC Control Circuit Test, Line Regulation

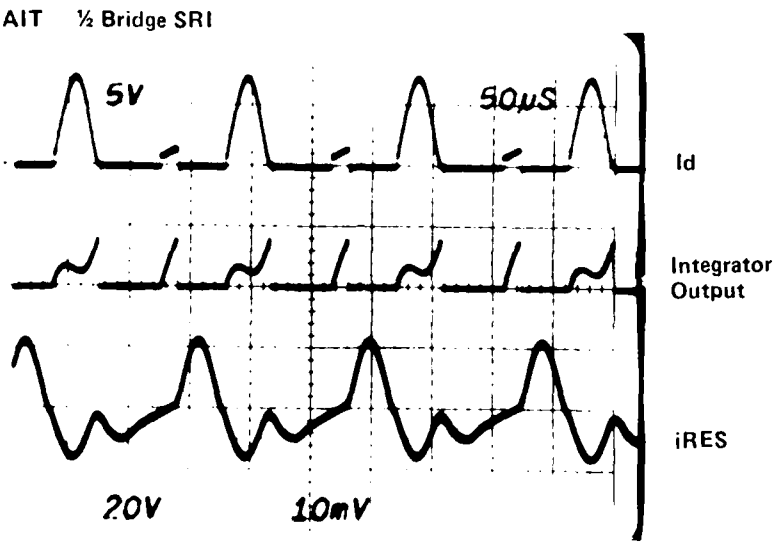
Run	V source	V output	V ref	Load = 2.70 ohms
1	120	19.97	0.39	
2	140	20.02	1.08	
3	160	20.05	1.78	
4	180	20.06	2.49	
5	200	20.05	3.06	
6	220	20.03	3.68	
7	240	20.02	4.16	

Two significant issues were identified during test of the ASDTIC current-mode control circuit:

1) An inherent instability occurred in the CCM operating mode.
2) The control range is limited to Continuous Conduction Mode (CCM) with transformer-coupled output.

The inherent instability results from timing Fire Group 1 SCRs from current feedback produced by Fire Group 2 SCRs. A more complex implementation of the current control was required. Figure 3.2.5-5 shows the resultant distorsion.

The issue raised with operating the SRI with an output transformer using ASDTIC resonant current-mode control will be discussed.



Notes:
1. This condition does not occur in discontinuous mode.
2. As Fs > Fo/2; nonsymmetry of Id begins to occur.
3. Above waveforms were the maximum instability that could be sustained without converter shut-down by the protection circuit.

Figure 3.2.5-5 Instability of Current Feedback Loop.

Notes:

1) This condition occurs in continuous conduction mode only.

2) Nonsymmetry of the resonant current waveform occurs for switching frequency greater than 1/2 resonant frequency.

3) The above waveforms were produced at maximum distorsion which could be sustained without converter shut-down by the protection circuit.

The instability was traced to the method used for implementation of the current feedback signal. It was discovered that a half-cycle delay of the resonant current feedback signal solved the instability issue. The half-cycle delay was implemented in the existing AIT control unit breadboard card by using a bilateral sample and store circuit. Reference section 3.1.5.3.

Control With Transformer-Coupled Output--Practical application of SRI converters generally requires voltage conversion which is accomplished by the use of a step-up or step-down output transformer. During light load, the output bridge rectifier/filter circuit is electrically disconnected from the SRI power stage due to insufficient tank circuit voltage. The secondary is uncoupled from the transformer, and the primary magnetizing inductance appears in series with the resonant tank. Resonant frequency is then determined by the sum of resonant inductor inductance and output transformer primary magnetizing inductance and the resonant capacitor capacitance.

This phenomena, normally called subresonant frequency operation (SRFO), has been observed by others, including Stuart of the University of Toledo (Ref. 14) and Robson of Hughes (Ref. 15). Operation of an SRI converter with transformer-coupled output presents a control difficulty for the ASDTIC resonant current-mode control circuit. This is intuitively apparent by observation of the resonant current waveform during light load.

Figure 3.2.5-6 shows the resonant current waveform during SRFO. The lower trace is resonant current. The half period of SRFO is approximately an order of magnitude longer than the normal resonant half period. The upper trace was included to show that current was not delivered to the load during SRFO, indicated by the sign of output filter capacitor voltage time rate-of-change.

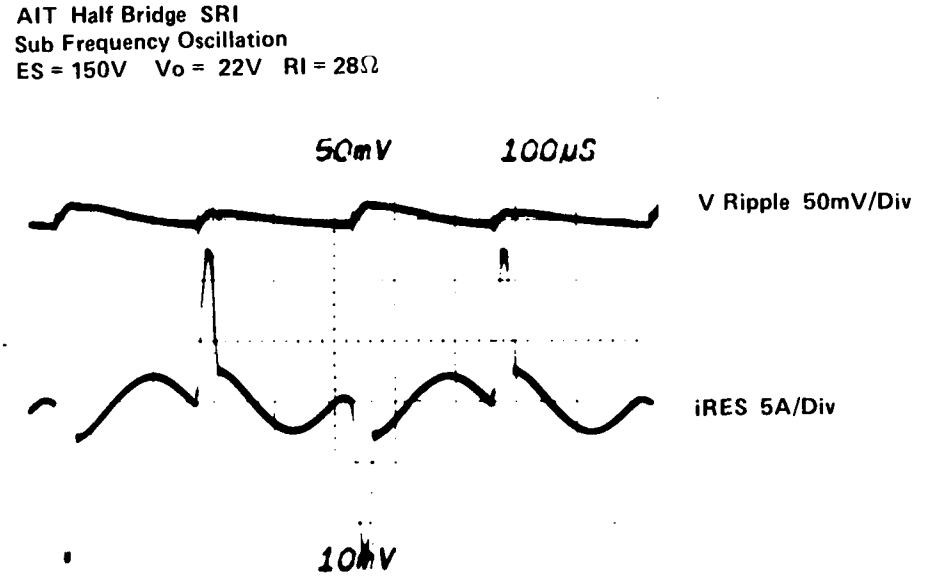


Figure 3.2.5-6 Sub-Resonant Frequency Operation.

The relationship between the integral of diode current and output voltage which was measured and data presented in table 3.2.5-1, does not exist during subresonant frequency operation. The control range of the ASDTIC resonant current-mode control was measured using the half-bridge SRI power module. Results are presented in table 3.2.5-2.

Table 3.2.5-2 Control Range--ASDTIC Resonant Current-Mode Control

Test Conditions:

Source Voltage = 150 Vdc
Load Voltage = 22 Vdc
Output Transformer Turns Ratio = 1.9:1 (Np/Ns)

RUN	Rload	output
1	0.75 ohms	645 W
2	1.51	321
3	1.71	283

Note:

The APL half bridge SRI is designed to deliver full power from a 600 Vdc source. At 150 Vdc reduced voltage input, maximum switching frequency will produce about 650-W output.

An alternate circuit for implementation of current-mode control was designed, fabricated and tested. This method is based current control from the output transformer secondary current. The feedback signal is monitored ahead of the full wave bridge rectifier and is sinusoidal so that I/O isolation is simplified. A toroidal current transformer is used to detect and isolate transformer secondary current.

Figure 3.2.5-7 shows transient response to a 10% to 100% load step. Test conditions are as follows:

V source = 150 Vdc
V output = 24 Vdc
Load = 2.7 ohms / 27.7 ohms

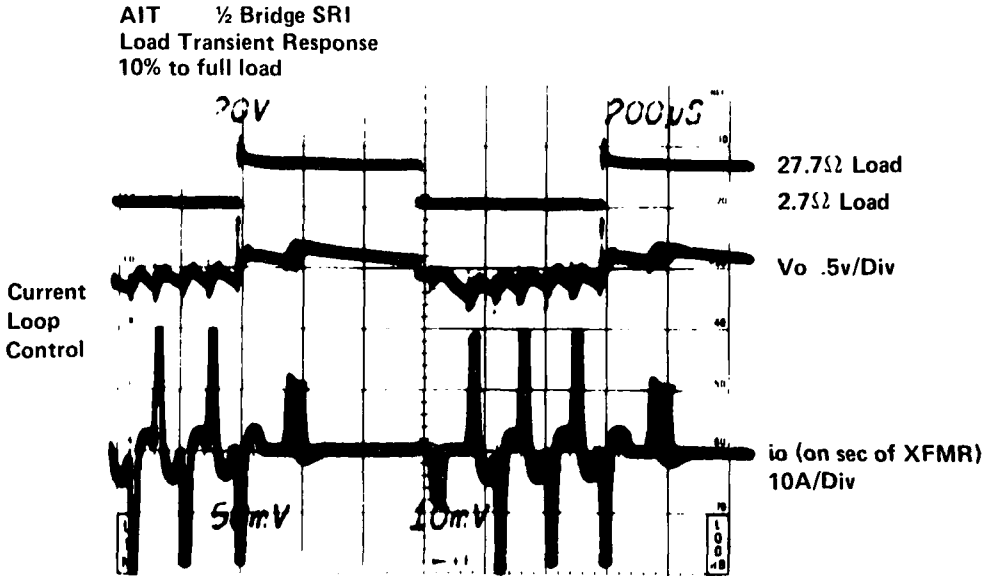


Figure 3.2.5-7 SRI Load Transient Response, Current Mode Control.

Results indicate that an SRI with resonant frequency of only 10-kHz may provide adequate transient response to a load step from minimum to maximum load, with less than 2% output voltage variation.

Performance Tests--Performance testing was conducted for steady state regulation, load transient response, and closed-loop stability. Results are presented in the following tables.

Test	Figure
Regulation (dc-to-dc)	Table 3.2.5-3
Regulation (ac-to-dc)	Tables 3.2.5-4,5
Load Transient Response	Figure 3.2.5-7
Closed-Loop Stability	Figures 3.2.5-8,9

Table 3.2.5-3 dc Test Data

Load (ohms)	VS (Vdc)	Vo (Vdc)
50.0	80.6	51.0
25.0	80.6	50.7
12.5	80.6	50.3
8.33	80.6	50.0
6.25	80.6	49.9
50.0	120	81.3
25.0	120	81.1
12.5	120	80.6
8.33	120	80.3
6.25	120	80.2
50.0	150	101.6
25.0	150	101.4
12.5	150	100.9
8.33	150	100.6
6.25	150	100.5

Table 3.2.5-4 ac Test Data

Load (ohms	Es (Vac)	Vo (Vdc)
50.0	100	80.6
15.0	100	80.4
12.5	100	79.9
6.25	100	79.4
50.0	150	131.7
25.0	150	131.4
12.5	150	130.8
6.25	150	130.4
50.0	200	149.8
25.0	200	149.6
12.5	200	148.9
6.25	200	148.6

Table 3.2.5-5 Regulation, ac-to-dc SRI Converter, Voltage Control

Line Voltage (ac RMS)	Load Voltage (dc)	Load (ohms)
170.8	190.00	8.33
179.9	200.32	8.33
187.7	200.39	8.33
199.9	200.44	8.33
208.6	200.45	8.33
219.8	200.45	8.33
230.0	200.50	8.33
240.2	200.50	8.33
189.6	200.40	12.51
198.5	200.40	12.51
208.9	200.44	12.51
219.3	200.45	12.51
229.6	200.47	12.51
239.8	200.46	12.51

Figure 3.2.5-8 Closed-Loop Stability, dc-to-dc SRI Converter, Half Power Output

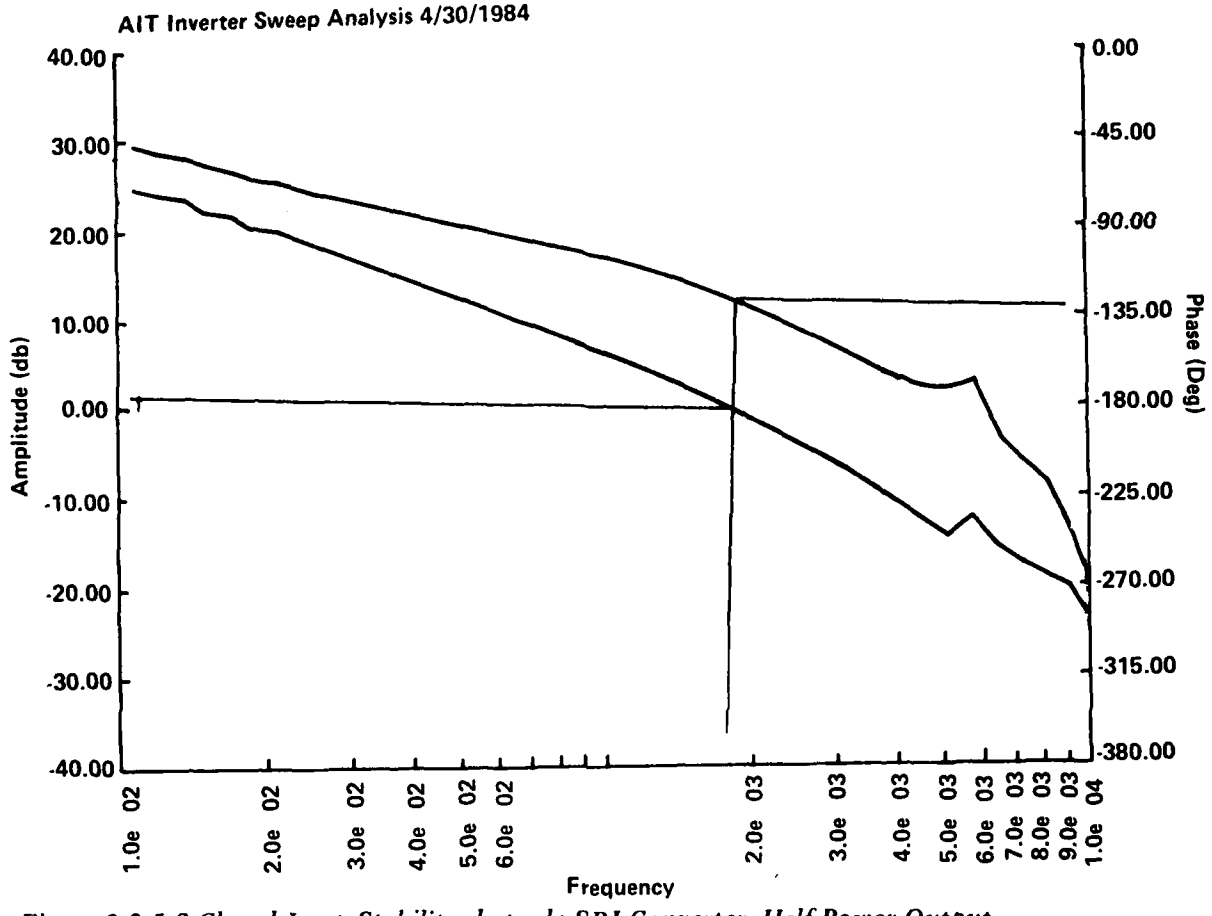


Figure 3.2.5-8 Closed-Loop Stability dc-to-dc SRI Converter, Half Power Output.

Figure 3.2.5-9 Closed-Loop Stability, dc-to-dc SRI Converter, Full Power Output

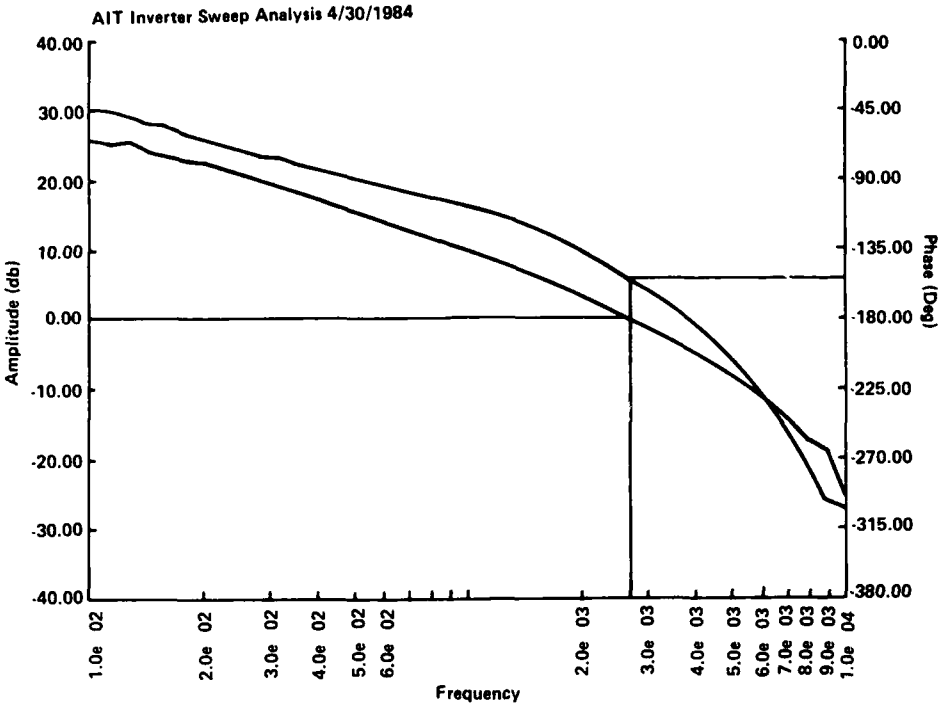


Figure 3.2.5-9 Closed-Loop Stability, dc-to-dc SRI Converter, Full Power Output

3.3 SYSTEM LEVEL DEVELOPMENTAL FUNCTIONAL TEST

System level testing was performed on three SRI power converters. Card cage controllers were connected to their associated SRI power modules. Tests for each of the SRI power converters were distributed into three tasks, static test, dynamic open loop functional test, and closed loop performance test.

Static Test--The following static tests were conducted on each controller card cage.

1) Point-to-point wiring test,
2) Hypot dielectric insulation test, and
3) Signal path test.

Hypot testing was conducted at 600 Vac RMS between wires and terminals connected to the SRI power module and the controller card cage chassis. Wiring and insulators which did not pass were replaced.

Signal paths between functional breadboard cards and between the controller card cage and the power module were verified before an attempt was made to run the SRIs from the ATI controllers.

A summary of functional and performance testing is presented for each of the following converters.

Power Converter	Section
10 kW Half Bridge	3.3.1
5 kW Three Phase	3.3.2
200 kW Scale Model	3.3.3

3.3.1 10 kW Half Bridge SRI Integrated Functional Test

Figure 3.3.1-1 is a wiring diagram for the 10 kW SRI power conditioner using the control architecture developed under the program.

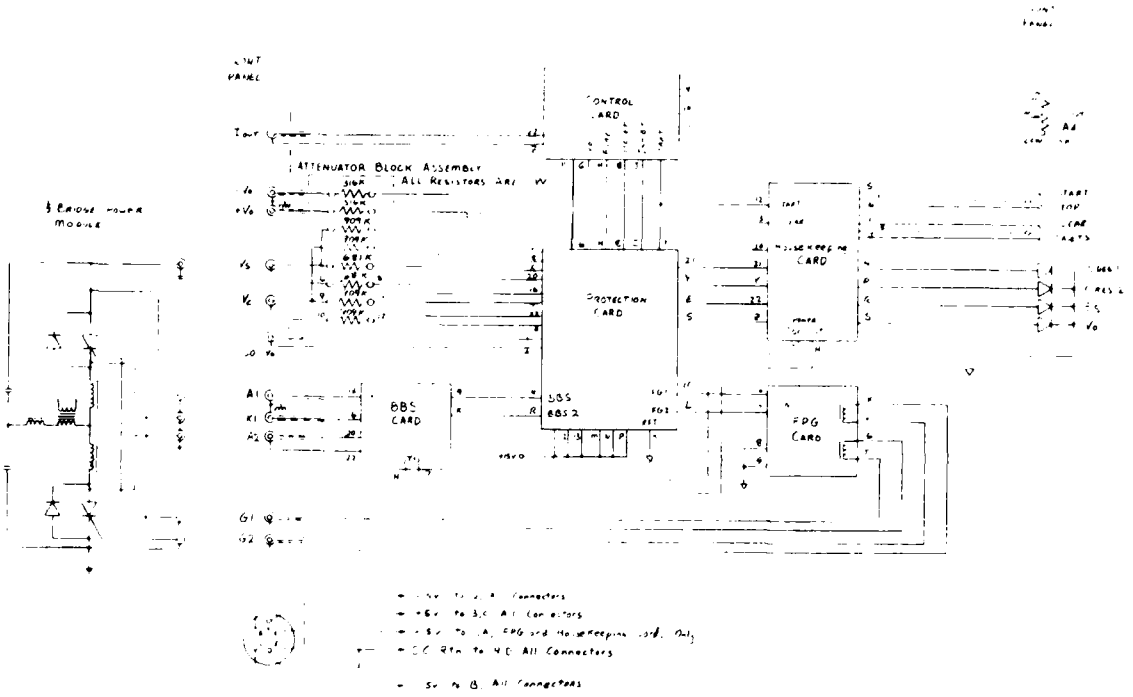


Figure 3.3.1-1 10-kW SRI Wiring Diagram

Functional testing involved verification of signal quality and proper timing of SCR fire signals. These tests were run by open-loop control of the converter. Data was collected during the open loop tests and is presented in table 3.3.1-1.

Table 3.3.1-1 Open Loop Test of the Half-Bridge SRI

Test Conditions:

V source = 230 Vdc
Load = 6.1 ohms

Output Power (Watts)	Vref	Vout	Iout	Frequency
2 mW	0.10	0.105	0.018	37 Hz
43 mW	0.50	0.508	0.085	176
159 mW	1.00	0.983	0.162	338
876 mW	2.30	2.30	0.381	797
4.06 W	5.00	5.01	0.811	1710
16. W	10.00	10.00	1.656	3500
65.9 W	20.00	19.99	3.295	7065
264 W	40.00	39.99	6.600	14139
1035 W	80.00	80.03	12.93	21206

Note:

Listed frequency is pulse frequency which is twice the switch frequency.

Closed loop functional testing was run to verify normal operation of all functional elements. An oscillograph of CU / PU handshake signals is presented in figure 3.3.1-2.

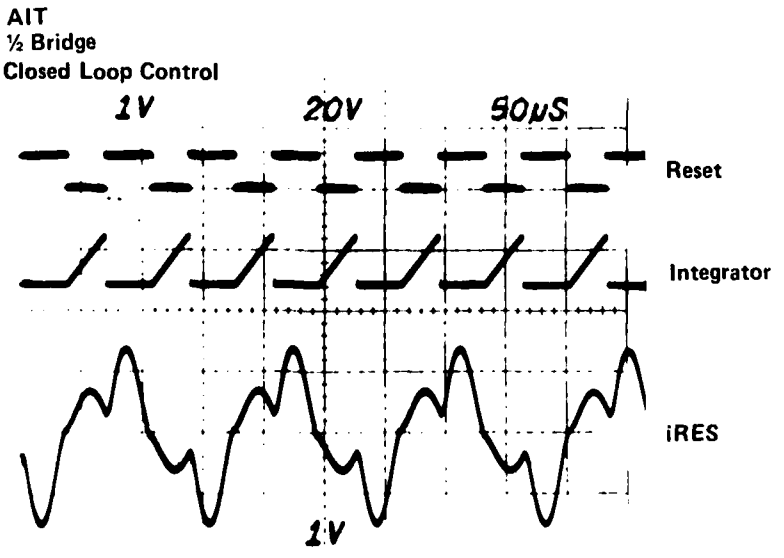


Figure 3.3.1-2 CU/PU Handshake Signals and Resonant Current.

Operation of the Protection Unit function was verified during open loop tests. Figure 3.3.1-3 shows timing signals produced on the PU breadboard during these tests.

Test Conditions:

V source = 200 Vdc
V output = 80 Vdc
Frequency = 7150 Hz

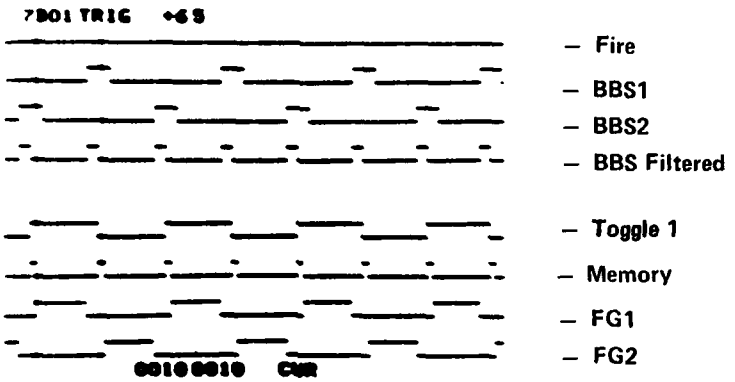


Figure 3.3.1-3 10-kW APL SRI Logic Timing, PU Circuit

Performance tests were run to verify control function over the specified 10:1 load range and + 15% of nominal line voltage range. Data are presented in tables 3.3.1-2,3. Test conditions are as follows:

V source = 498 Vdc
V output = 225 Vdc
Load = 6.25 ohms to 75 ohms

Table 3.3.1-2 Performance Test Data Summary, Half Bridge SRI, Load Regulation

RUN	LOAD (ohms)	Voutput	output (watts)
1	75	225.0	675
2	50	224.8	1011
3	25	224.4	2014
4	12.5	223.9	4010
5	8.33	223.3	5986
6	6.25	222.9	7950

Note:

Testing to rated 10 kW output was not achieved because the largest dc power source available for this test was limited to 500 Vdc output. Required output voltage for this power conditioner to achieve full power is 250 Vdc and requires a minimum line input voltage of 550 Vdc.

Table 3.3.1-3 Performance Test Data Summary, Half Bridge SRI, Line Regulation

Load = 8.33 ohms

RUN	Vsource	Voutput
1	350.2	150.0
2	374.9	150.1
3	400.1	150.1
4	424.8	150.1
5	449.9	150.1
6	474.7	150.0
7	498.5	150.0

The resonant current waveform was photographed during testing and is shown in Figure 3.3.1-4. Test conditions are:

V source = 498 Vdc
V output = 150 Vdc
Load = 8.33 ohms

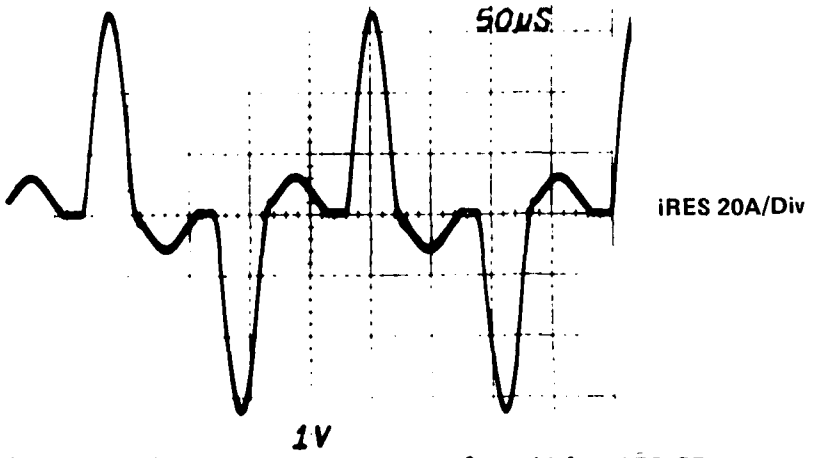


Figure 3.3.1-4 Resonant Current Waveform 10-kW APL SRI.

3.3.2 5 kW Three Phase SRI Integrated Functional Test

Figure 3.3.2-1 is a wiring diagram of the 5 kW Three Phase SRI power conditioner using the control architecture developed under the program.

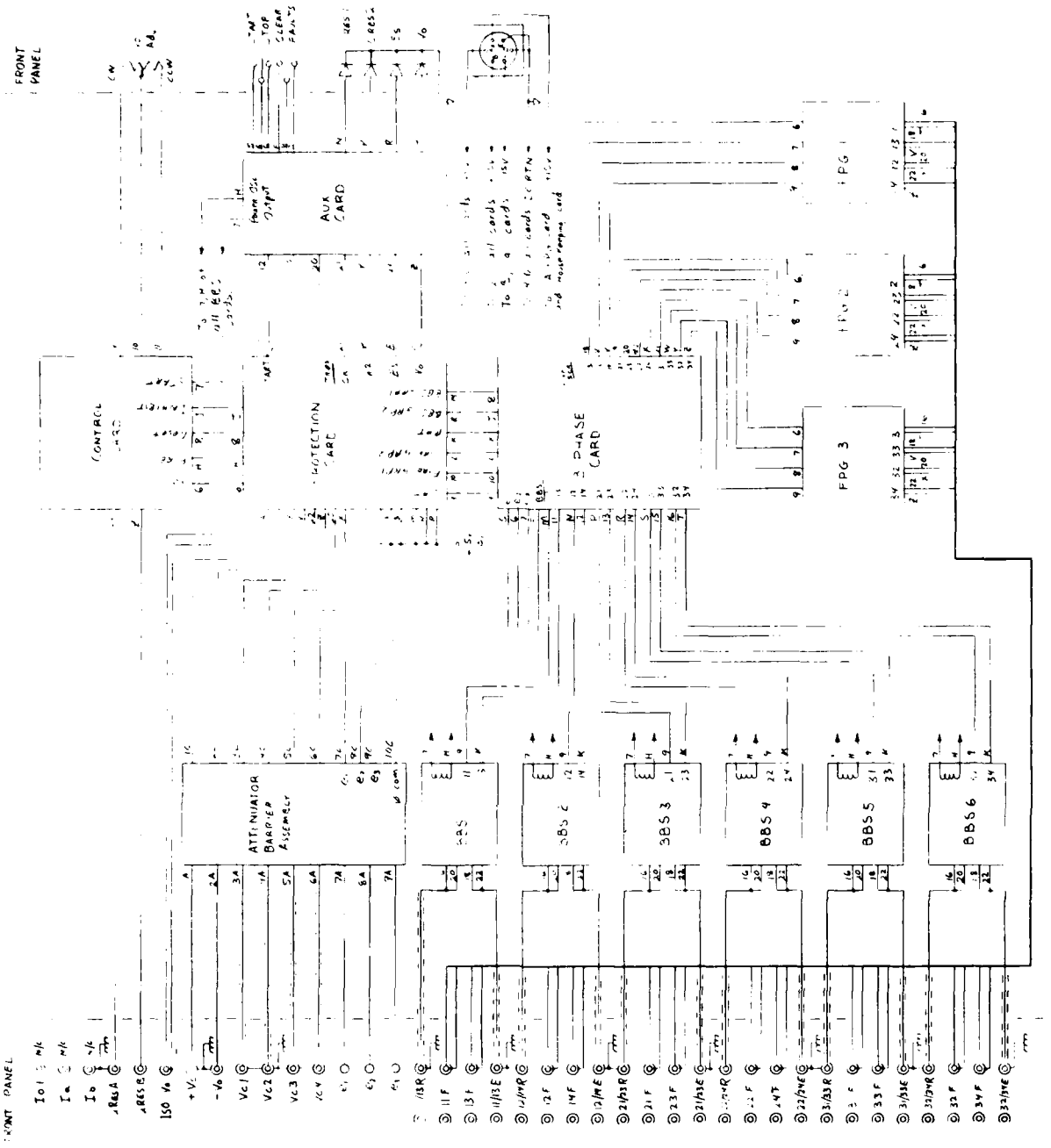


Figure 3.3.2-1 5 kW SRI Wiring Diagram

Functional testing involved operation of the SRI power module from the APL discrete component controller. The AIT controller was wired in parallel using "T" type BNC connectors to verify signal paths and logic circuits before an attempt was made to operate the SRI power module from the AIT controller developed under the program.

Open loop tests were run using a dc voltage source so that each of six phase pairs could be verified individually before three phase ac operation was attempted. Open loop oscillation was sustained using a frequency synthesizer which drove a "T" flip-flop circuit to produce fire signals. The fire signals were injected directly into the Firing Pulse Generators.

The following signals were measured during open loop tests and table 3.3.2-1 lists photographs of the measurements:

1) Quality of SCR BBS signals.
2) Timing of SCR BBS signals.
3) Amplitude of the three resonant current transformer signals.
4) Resonant current distorsion with transformer-coupled load.

Table 3.3.2-1 Static Test Photos, 5 kW SRI

Signal	Figure Number
SCR/BBS Waveform	3.3.2-2
BBS Waveform Detail	3.3.2-3
BBS Signal Timing	3.3.2-4
Current Transformers	3.3.2-5
Transformer-Coupled Output Waveform	3.3.2-6

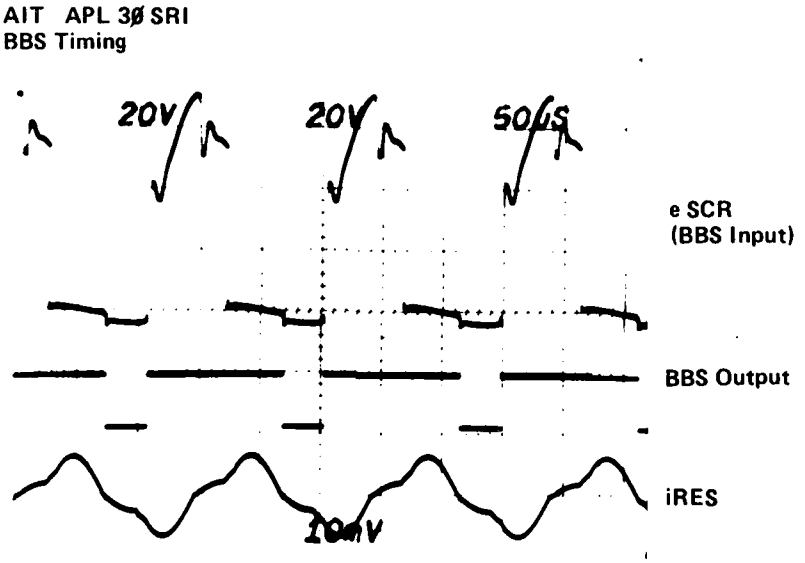


Figure 3.3.2-2 SCR, BBS and Resonant Current Waveforms, 5 kW SRI.

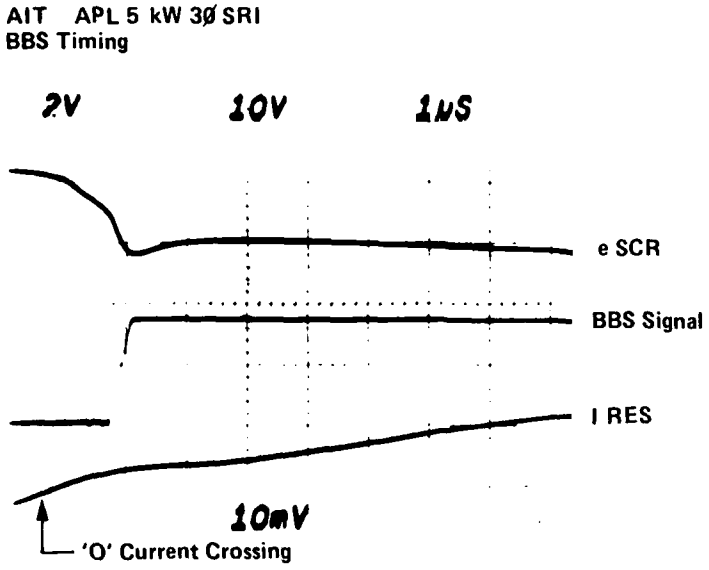


Figure 3.3.2-3 SCR Voltage, BBS Signal, and Resonant Current, 5 kW SRI, Detail.

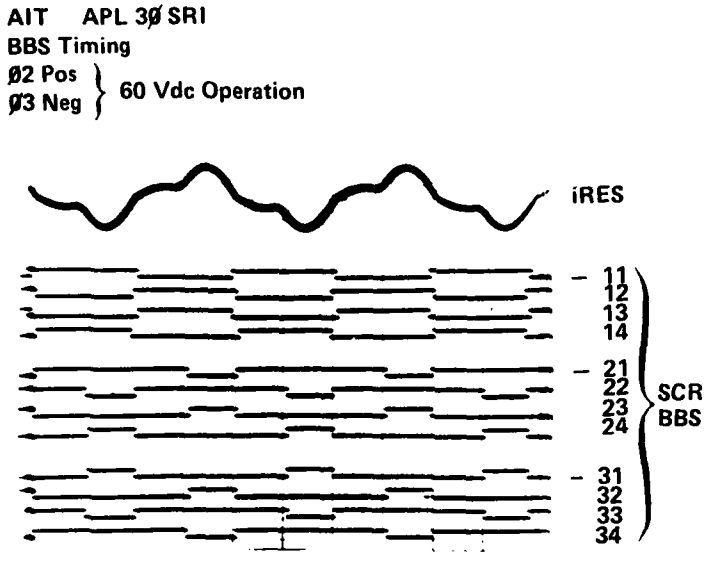
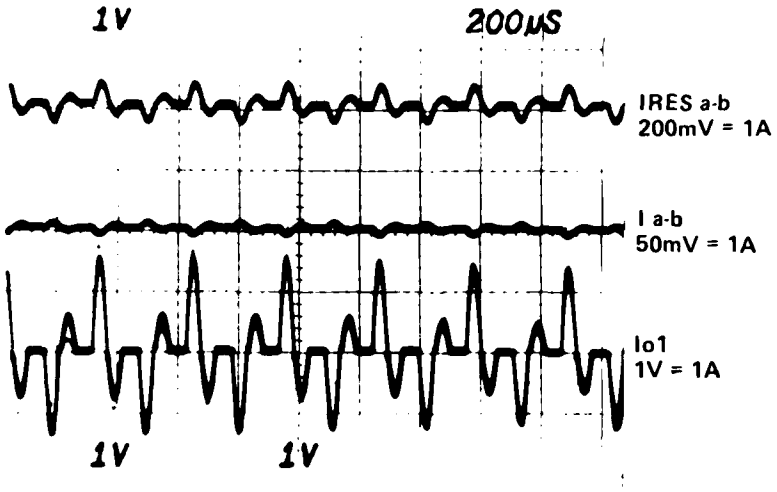


Figure 3.3.2-4 BBS Signal Timing, for 12 SCRs 5 kW SRI.



1. All current SFMR's have 50Ω burden resistors.

2. Turns ratios

IRES a to b	50Ω/.2V = 250
I a to b	50Ω/.05V = 1000
Io1	50Ω/1V = 50

Figure 3.3.2-5 Amplitude Comparison of the Three Resonant Current Transformers, 5-kW SRI

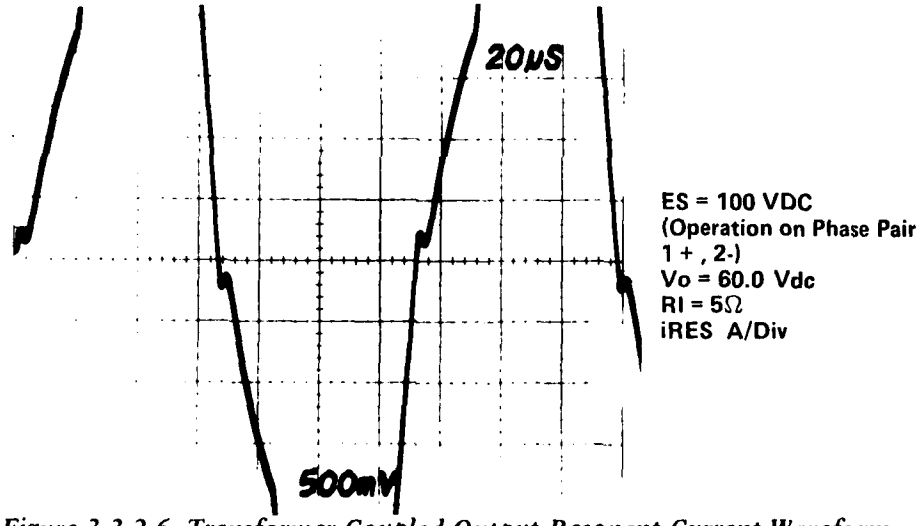


Figure 3.3.2-6 Transformer-Coupled Output Resonant Current Waveform.

Closed loop tests were run for verification of normal operation of all functional elements. Each of the six phase pairs was verified individually using a 60 Vdc source. Once all phase combinations had been verified, closed loop operation from three phase ac input was run. Table 3.3.2-2 lists all six phase pairs with associated voltage input signs.

Table 3.2.2-2 Phase Pair Assignments

Phase Pair Pair	Line Input		
	e1	e2	e3
V12	+	-	0
V13	+	0	-
V23	0	+	-
V21	-	+	0
V31	-	0	+
V32	0	-	+

Figures 3.3.2-7 and 8 are timing diagrams of BBS signals with 60 Vdc input applied to phase pairs V13 and V23, respectively.

AIT APL 3Ø SRI (5 kW)
BBS Timing
01 Pos } 60 Vdc Operation
03 Neg }

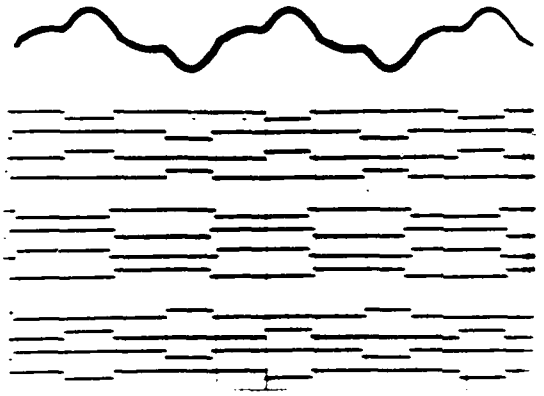
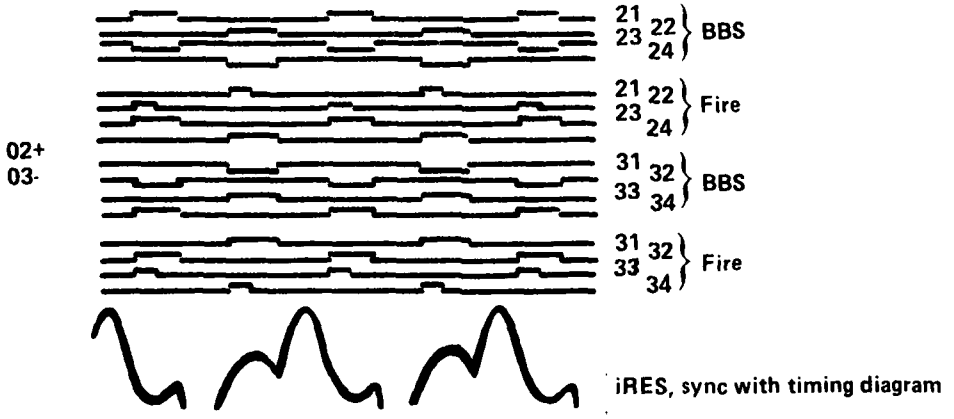


Figure 3.3.2-7 BBS Timing Diagram, Phase 1-3.

AIT 3Ø Controller
EX = 60 V Vo = 16 V
Logic Timing



Notes:
1. Short fire pulses are SCR mode.
2. Long fire pulses are diode mode
3. Length of SCR fire pulses set by a CD4098 dual one shot, to facilitate functional test of the TPU.

Figure 3.3.2-8 BBS Timing Diagram, Phase 2-3.

Verification of three phase operation is shown in figures of resonant current during phase transition and a timing diagram of PU logic which occurred during phase transition; figures 3.3.2-9 and 10.

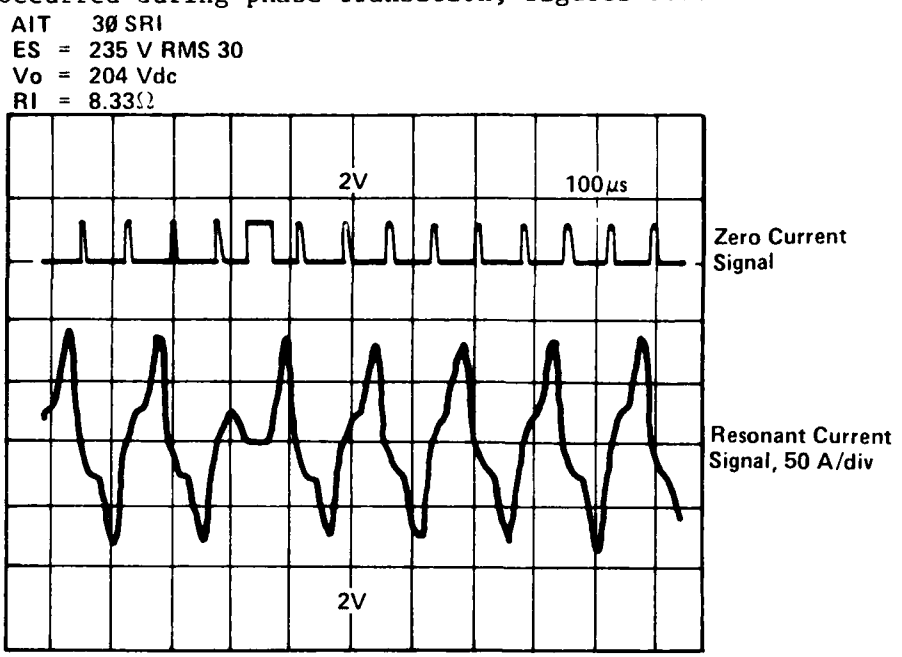


Figure 3.3.2-9 Resonant Current During Phase Transition, 5 kW SRI.

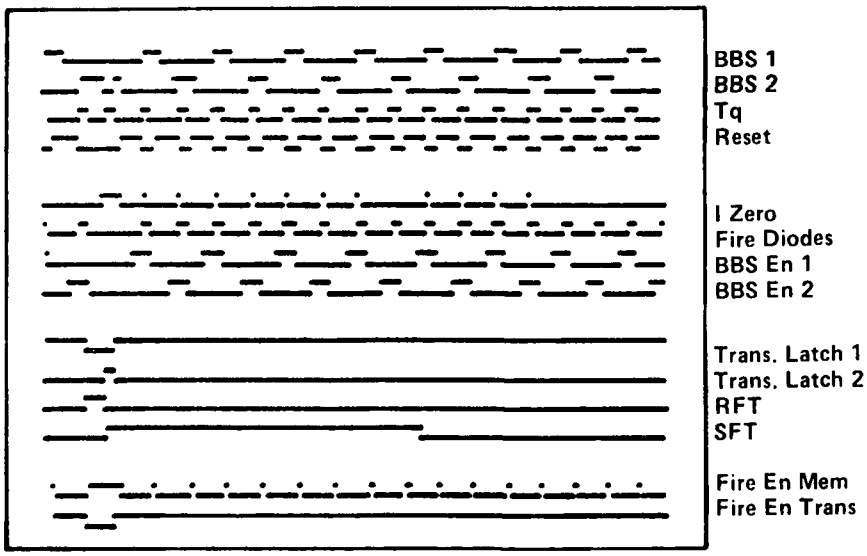


Figure 3.3.2-10 Timing Diagram of PU Logic During Phase Transition.

An envelope of resonant current is shown for all six phase pairs in figure 3.3.2-11. Operating conditions are:

V source = 208 Vdc
V output = 200 Vdc
Load = 8.33 ohms

Test Conditions:
ES = 208 V RMS RI = 6.25Ω
Vo = 177 Vdc

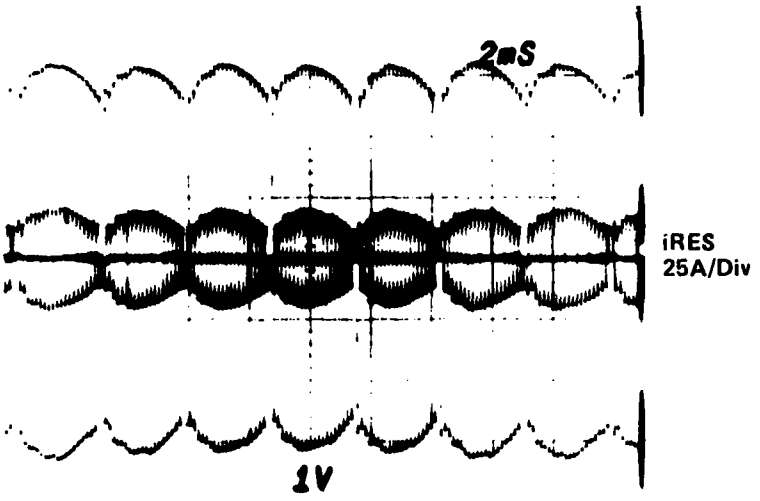


Figure 3.3.2-11 Envelope of Resonant Current Over Six Phase Pairs

Performance tests were run to verify control function over the specified 1:1 load range and ± 15% of nominal line voltage range. Data are presented in tables 3.3.2-2,3, and 4.

Table 3.3.2-3 Performance Test Data Summary, 5 kW Three Phase SRI, ac Operation

Es RMS (Vac)	*Voutput at Indicated Load (Vdc)*			
	6.25	12.5	25.0	50.0
100	79.4	79.9	80.4	80.6
150	130.4	130.8	131.4	131.7
200	148.6	148.9	149.6	149.8

Table 3.3.2-4 Performance Test Data Summary, 5 kW Three Phase SRI, dc Operation

Es (Vdc)	Voutput at Indicated Load (Vdc)				
	6.25	8.33	6.25	25.0	50.0
80.6	49.9	50.0	50.3	50.7	51.0
120.4	(1)	(1)	99.4	99.9	100.2
120.0	80.2	80.3	80.6	81.1	81.3
150.0	100.4	100.6	100.9	101.4	101.6

Note:

Test indicated by (1) opened the 10 A line fuse. Voltage output was reduced to 80 Vdc and tests were successfully run.

Table 3.3.2-5 Line Regulation Data Summary, 5 kW Three Phase SRI

Line Voltage (ac RMS)	Load Voltage (dc)	Load (ohms)
170.8	190.00	8.33
179.9	200.32	8.33
187.7	200.39	8.33
199.9	200.44	8.33
208.6	200.45	8.33
219.8	200.45	8.33
230.0	200.50	8.33
240.2	200.50	8.33
189.6	200.40	12.51
198.5	200.40	12.51
208.9	200.44	12.51
219.3	200.45	12.51
229.6	200.47	12.51
239.8	200.46	12.51

3.3.3 200 Kw Scale Model SRI Integrated Functional Test

A 4 kW scale model of the APL 200 kW Twin Full Bridge SRI was constructed to demonstrate operation of the AIT controller. Developmental testing of the AIT twin full bridge controller was accomplished with a scale model rather than the full scale converter for two reasons. First, 200 kW electrical power at 600 Vdc is not available in the Power Conditioning Lab at Martin Marietta Denver Aerospace and second, there is high uncertainty and risk associated with operating unverified hardware.

The scale model is designed to parallel electrical characteristics of the full scale converter. Important operating characteristics signal levels, and interconnections are designed to closely match the 200 kW converter. The purpose of verification tests was proof of operation in order to reduce the risk associated with initial operation of the 200 kW SRI.

Static testing was limited to "ring-out" of signal lines since all breadboard hardware had previously been verified in two existing SRI power converters.

Open loop tests were run to verify power circuit operation. Figure 3.3.3-1 is a schematic diagram of the 5 kW Scale Module Twin Full Bridge SRI. Figure 3.3.3-2 is a wiring diagram of the associated controller.

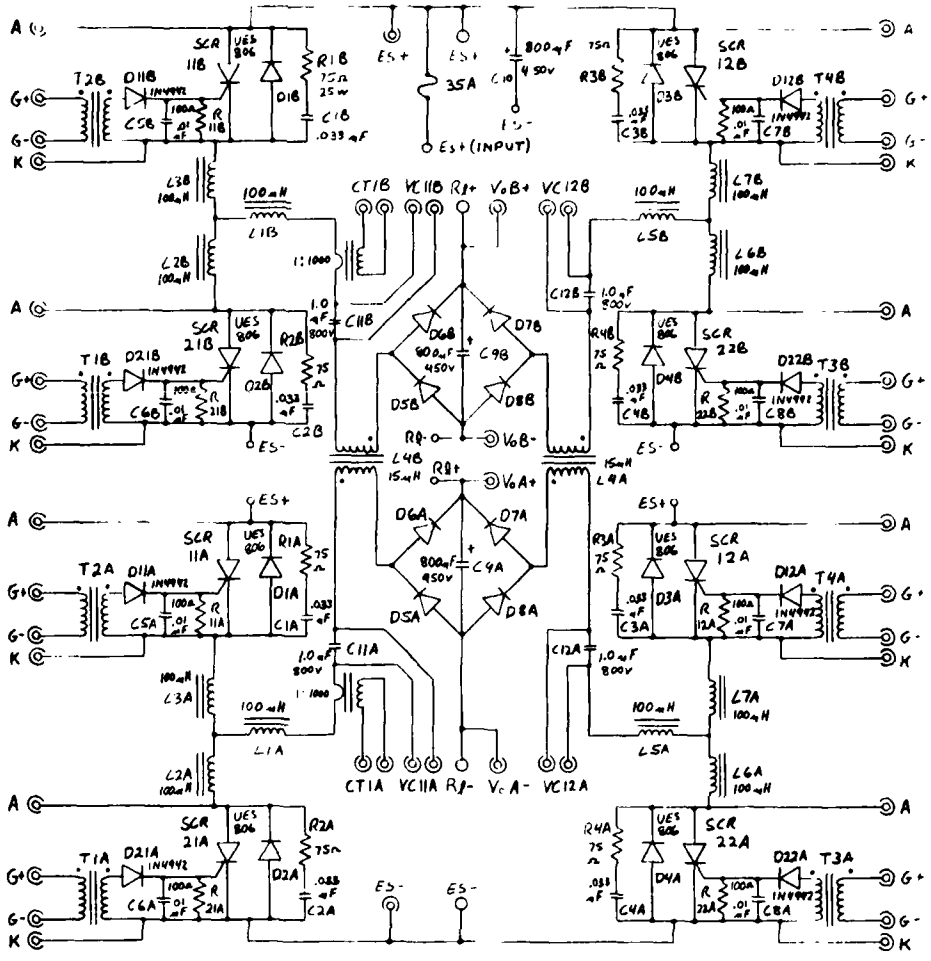


Figure 3.3.3-1 Schematic Diagram, Twin Full Bridge SRI Scale Model.

Figures 3.3.3-3, 4, 5, and 6 show voltage waveforms in the power module during full power operation. Test conditions are:

V source = 250 Vdc
V output = 191.5 Vdc
Load = 8.33 ohms
Vo ripple = 0.58 Vrms
Control Time = 16 microseconds

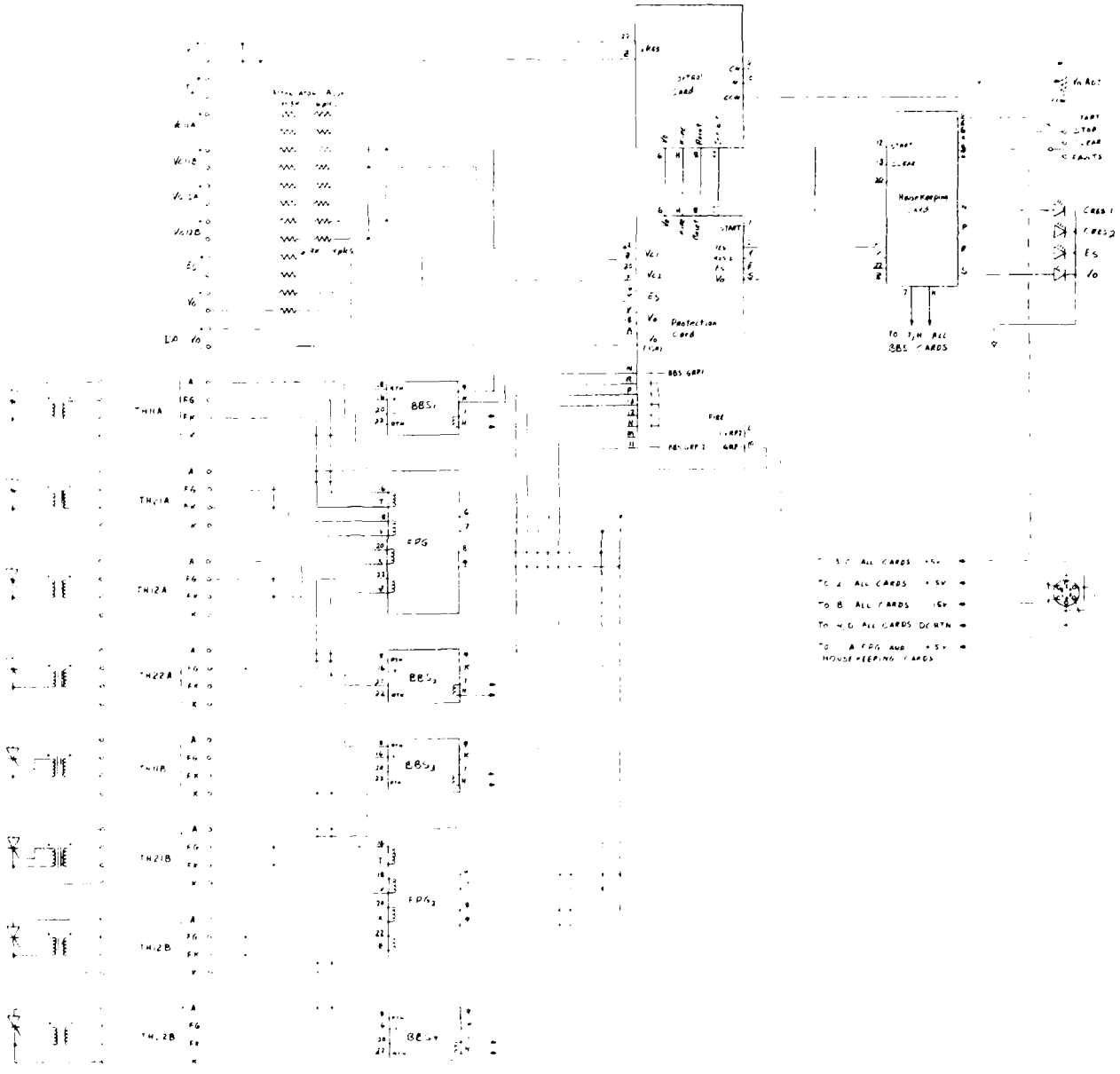
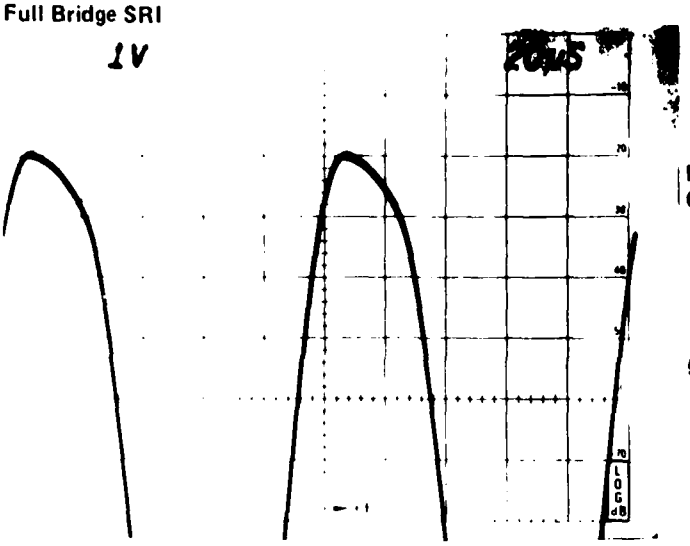


Figure 3.3.3-2 Twin Bridge SRI Wiring Diagram

Power Module Tests
Full Bridge SRI



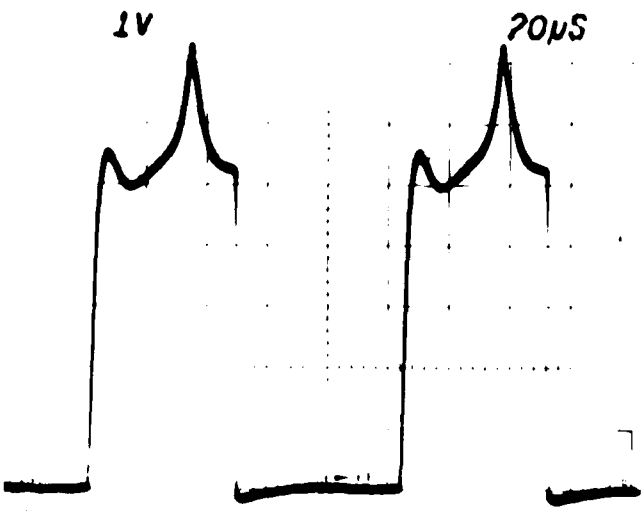
Peak Voltage Across
C11A Approx 310vP

50v Per Div

1. Full Power Tests
   (Es) = 250VDL
   (Ψr) = 16MS
   (RI) = 8.33Ω
   (VO) = 191.5 Vdc Po = 4402 Watts
   (VO Ripple) = .5575 VRMS
   (VO Cap Ripple) = A .2450 VRMS
   B .4500 VRMS

Voltage Across 1μf Caps 11A) = 241.27 VRMS
12A) = 246.96 VRMS
11B) = 239.06 VRMS
12B) = 228.92 VRMS

Figure 3.3.3-3 Full Power Test, 200-kW Model, Resonant Capacitator Voltage.



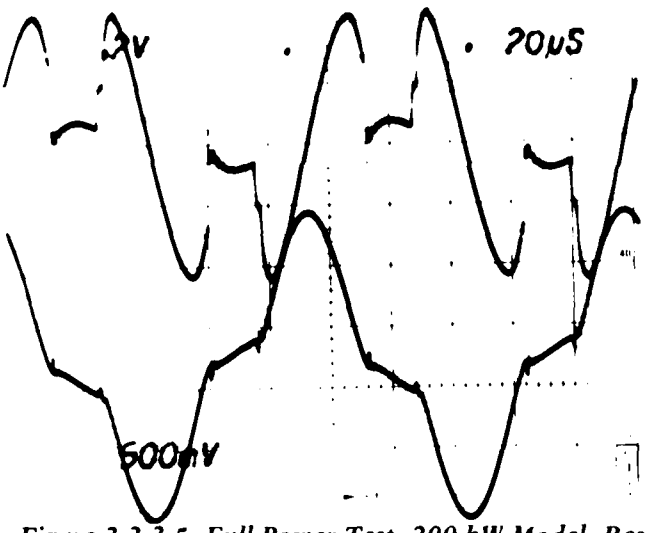
Voltage Across SCR
SCR11A = 137.35 VRMS
SCR12A = 137.69 VRMS
SCR22A = 137.73 VRMS
SCR21A = 137.15 VRMS
SCR11B = 138.22 VRMS
SCR12B = 138.04 VRMS
SCR22B = 137.79 VRMS
SCR21B = 138.15 VRMS

Voltage Across SCR11A

50v Per Div

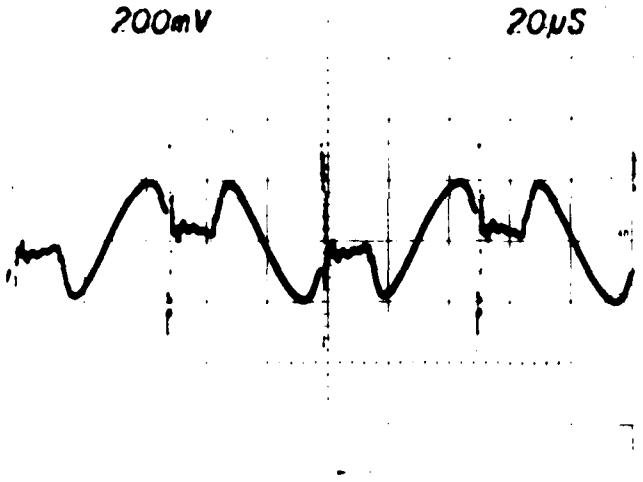
- Ov

Figure 3.3.3-4 Full Power Test, 200-kW Model, SCR Voltage.



Voltage Across Resonant Inductors
L1A = 127.93 VRMS
L1B = 130.49 VRMS
L5A = 127.91 VRMS
L5B = 133,19 VRMS

Figure 3.3.3-5 Full Power Test, 200-kW Model, Resonant Inductor Voltage.



Voltage Across L4A (S)

10v Per Div

0v

Figure 3.3.3-6 Full Power Test, 200-kW Model, Dual (Matching) Inductor Voltage.

There was no attempt to match components of the two parallel connected converter halves. Matching inductors are included in the design of the 200 kW Twin Full Bridge and were also designed into the scale model. The matching inductors force resonant current sharing between the two SRI full bridge halves, and also help match the half-periods of the resonant current sines.

Tables of measured voltages for components in both halves of the twin bridge are presented in tables 3.3.3-5,6, and 7. A table of matching inductor voltage difference between the two full bridge halves is presented in table 3.3.3-8.

Table 3.3.3-6 Voltage Measurements, Resonant Inductors

L1A = 127.93 VRMS
L1B = 130.49 VRMS
L2A = 127.91 VRMS
L2B = 133.19 VRMS

Table 3.3.3-7 Voltage Measurements, SCRs

SCR11A = 137.35 VRMS
SCR12A = 137.69 VRMS
SCR22A = 137.73 VRMS
SCR21A = 137.15 VRMS
SCR11B = 138.22 VRMS
SCR12B = 138.04 VRMS
SCR22B = 137.79 VRMS
SCR21B = 138.15 VRMS

Table 3.3.3-8 Voltage Measurements, Resonant Capacitors

C11A = 241.27 VRMS
C12A = 246.96 VRMS
C11B = 239.06 VRMS
C12A = 228.92 VRMS

Table 3.3.3-9 Voltage Measurements, Dual Inductors

L4A:	Primary = 6.820 VRMS
	Secondary = 6.030 VRMS
L4B:	Primary = 6.691 VRMS
	Secondary = 6.226 VRMS

3.4 TEMPERATURE TESTS

Tests were run on each of the four breadboard circuits to determine temperature stability and correct component and circuit design related deficiencies before release of 100% engineering input to the Microcircuits Development Lab. The criteria for test and results are listed for each of the four functional elements which were implemented as microcircuit hybrids.

3.4.1 Firing Pulse Generator Temperature Test

Test criteria, acceptable tolerances and test results are listed in tables 3.4.1-1, 3.4.1-2, and 3.4.1-3 respectively.

Table 3.4.1-1 Test Criteria for the FPG Breadboard Circuit Card.

- Operating temperature range is -40°C to +85°C.
- The FPG must operate within listed tolerances over the entire operating temperature range.
- Storage temperature range is -55°C to +125°C.
- The FPG must operate within listed tolerances after storage for 1 hour at the listed temperature extremes.

Table 3.4.1-2 Test tolerances for the FPG breadboard circuit card.

- Peak open circuit gate pulse amplitude must remain greater than Vcc -1, or 14 V. - The FPG must not fail to produce a pulse. - Pulse energy delivered to the SCR gate must remain within 20% of nominal value.

Table 3.4.1-3 Test Data Summary for the FPG Breadboard Circuit Card.

Deg (C)	q(Vo/Es)	Fs(Hz)	Vo.c.(p-p)	Eo(joules)
-40	0.757	7340	14.7	4.3 uj
-20	0.756	7341	14.7	4.3 uj
0	0.756	7341	14.7	4.3 uj
20	0.755	7341	14.7	4.3 uj
40	0.756	7341	14.7	4.3 uj
60	0.757	7341	14.7	4.2 uj
85	0.757	7340	14.7	4.2 uj

Notes:

1) Firing pulse waveforms were monitored during the test. No discernable change in waveshape was evident at any time during the test.

2) Failure to fire would cause converter shutdown. This condition did not occur at any time during the temperature test.

3.4.2 Back Bias Sensor Temperature Test

Test criteria, acceptable tolerances and test results are listed in tables 3.4.2-1, 3.4.2-2, and 3.4.2-3 respectively.

Table 3.4.2-1 Test Criteria for the BBS Breadboard Circuit Card.

- Operating temperature range is -40°C to +85°C. - The BBS must operate within listed tolerances over the entire operating temperature range. - Storage temperature range is -55°C to +125°C. - The BBS must operate within listed tolerances after storage for 1 hour at the listed temperature extremes.

Table 3.4.2-2 Test Tolerances for the BBS Breadboard Circuit Card.

- Delay time change must be less than 100 nanoseconds over the operating temperature range. At 15 microseconds control time, maximum frequency shift must be less than 0.67%. - The BBS must not fail to produce a signal.

Table 3.4.2-3 Test Data Summary for the BBS Breadboard Circuit Card.

Deg (C)	Es(Vdc)	Vo(Vdc)	Fs(Hz)
-40	94.0	100.4	7336
-20	94.2	100.6	7336
0	94.1	100.5	7336
20	93.8	100.2	7335
40	94.0	100.4	7336
60	94.0	100.4	7336
85	94.4	100.8	7337

Notes:

1) Switch frequency was set to maximum by adjusting the output voltage reference to maximum.

2) Source voltage was set to a constant value so that change of input-to-output voltage ratio would cause shift of output voltage.

3) Stability of the BBS circuit may be measured by change in delay time. Since the BBS delay will affect total control time delay, instability will show up as shift of switch frequency. At 7336 Hz, maximum allowable temperature-dependant frequency shift is 0.67% of the switch frequency or 49 Hz at 7336 Hz.

4) Failure of the BBS to produce one output pulse would cause power converter shutdown. The converter did not shut down at any time during temperature testing.

3.4.3 Protection Unit Temperature Test

Test criteria, acceptable tolerances and test results are listed in tables 3.4.3-1, 3.4.3-2, and 3.4.3-3 respectively.

Table 3.4.3-1 Test Criteria for the PU Breadboard Circuit Card.

- Operating temperature range is -40°C to +85°C.
- The PU must operate within listed tolerances over the entire operating temperature range.
- Storage temperature range is -55°C to +125°C.
- The PU must operate within listed tolerances after storage for 1 hour at the listed temperature extremes.

Table 3.4.3-2 TEST Tolerances for the PU Breadboard Circuit Card.

- Delay time may not change more than 10% over the operating temperature range. At 15 microseconds control time, maximum desired shift in control time is 1.5 microseconds.
- The PU must not fail to produce a signal. The power converter must continue to run over the entire temperature range.

Table 3.4.3-3 Test Data Summary for the PU Breadboard Circuit Card.

Deg (C)	Es(Vdc)	Vo(Vdc)	Tq(microseconds)
-40	60.95	53.19	17 microseconds
-20	60.89	53.15	17
0	60.87	53.01	17
20	60.21	52.87	18
40	60.30	52.55	19
60	60.25	52.50	19
85	60.23	52.50	19

Notes:

1) Switch frequency was set to maximum by adjusting the output voltage reference to maximum.

2) Source voltage was set to a constant value so that a change of input-to-output voltage ratio would cause a shift of output voltage.

3) Stability of the PU circuit may be measured by a change in delay time. Since the PU delay will affect total control time delay, an instability will show up as a shift output voltage. The maximum allowable temperature dependant output voltage shift is 5%.

Test Summary--During temperature testing, the PU failed to produce proper handshake signals with the TPU circuit. The problem is shown in figure 3.4.3-1 as power converter failure to oscillate. This problem was traced to a change in pulse width of the SFT timer on the PU card. The timing capacitor used was found to suffer from a large change in capacitance below -20°C. The capacitor was changed and the temperature test rerun. Figure 3.4.3-2 shows that oscillator stability is maintained.

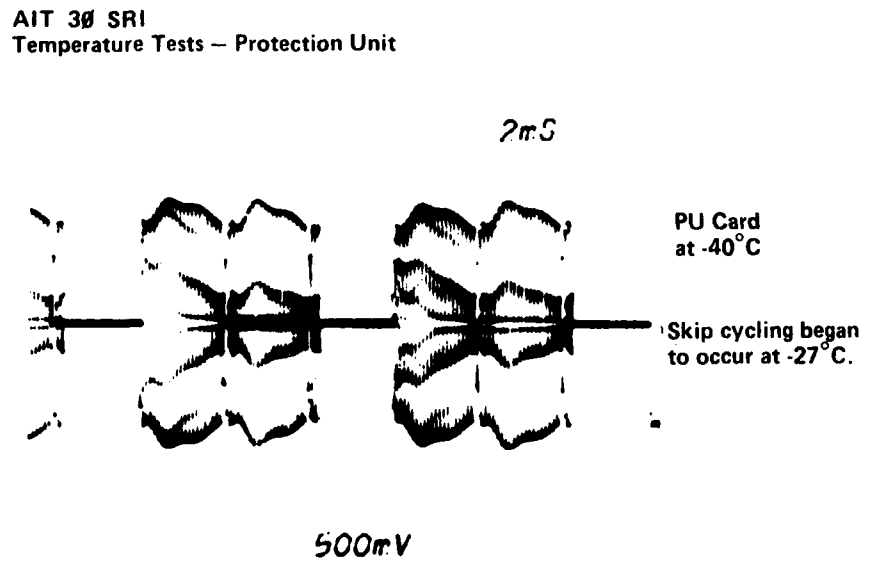


Figure 3.4.3-1 Envelope of Resonant Current at -40° (Unstable Timing Capacitor).

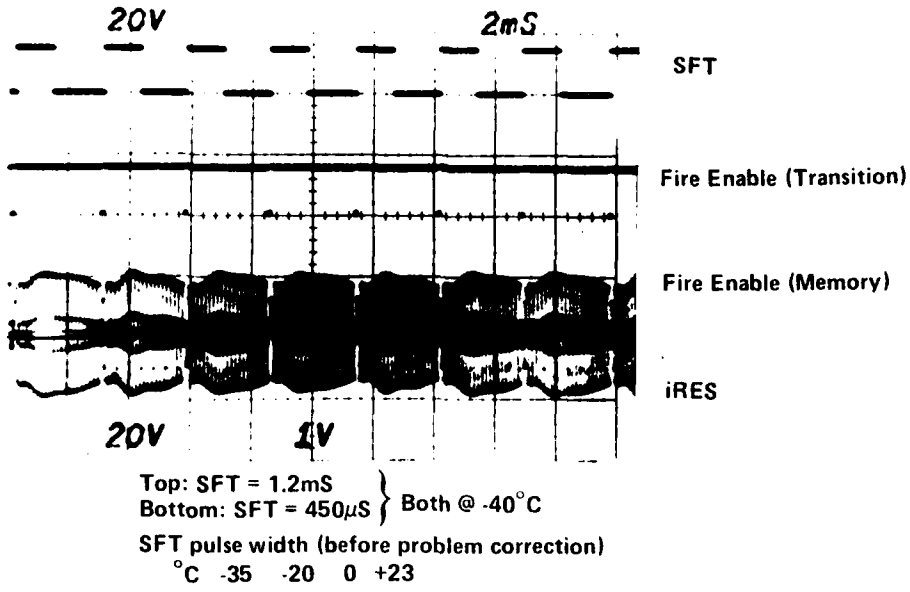


Figure 3.4.3-2 Envelope of Resonant Current, SFT Signal and Fire Enable Signal at -40° C.

3.4.4 Three Phase Unit Temperature Test

Test criteria, acceptable tolerances and test results are listed in table 3.4.4-1, figure 3.4.4-1, and table 3.4.4-3 respectively.

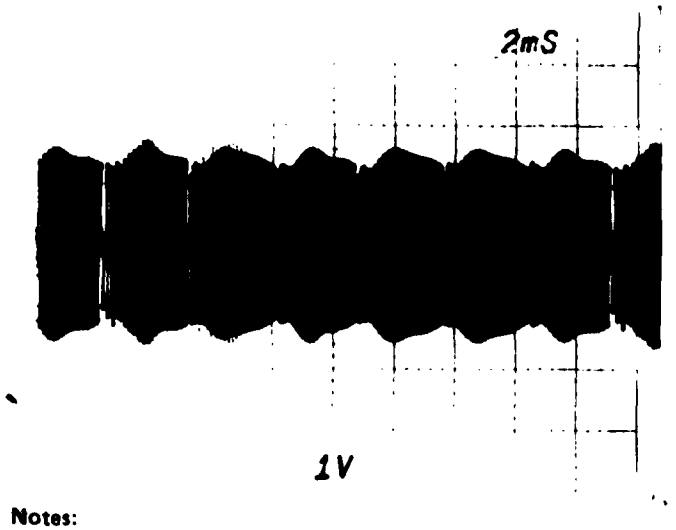
Table 3.4.4-1 Test Criteria for the TPU Breadboard Circuit Card.

- Operation temperature range is -40°C to +85°C. - The TPU must operate within listed tolerances over the entire operating temperature range. - Storage temperature range is -55°C to +125°C. - The TPU must operate within listed tolerances after storage for 1 hour at the listed temperature extremes.

Table 3.4.4-2 Test Tolerances for the TPU Breadboard Circuit Card.

- The SRI power converter must produce constant output voltage over the operating temperature range. - The TPU must properly select SCRs for all six phase pairs over the operating temperature range.

AIT Breadboard Circuit Temp Test
Three Phase Unit (TPU)



iRES 25A/Div

Photo taken -40°C.

Notes:
1. ES = 100 v RMS 30
   Vo = 100 VDC RI = 8.33Ω
2. Gaps in iRES during some phase transitions was shown to be a result of 60Hz pickup in the wiring to exist when the TPU is installed in the card cage.
3. At all temperatures between -40°C and +85°C output voltage and resonant current waveforms remained constant.

Figure 3.4.4-1 Envelope of Resonant Current During Temperature Test.

Notes:

1) Test conditions -
   Esource = 100 VRMS, Three Phase
   Voutput = 100 Vdc
   Load = 8.33 ohms

2) Gaps in the resonant current during some phase transitions were shown to be a result of 60 Hz pickup in the interface wiring to the test chamber and is not temperature dependent. This condition does not exist when the TPU is installed in the controller card cage.

3) At all temperatures over the full operating range, output voltage and resonant current waveforms remained constant.

Test Summary--There are no RC timing circuits in the TPU design. Logic is designed so that propagation delays cannot effect circuit function. The only predicted failure mode that is possible is failure of the TPU to properly select correct SCRs based on phase pairs. Figure 3.4.4-2 clearly shows proper selection of SCRs for all phase pairs. The envelope of resonant current remained identical over the full operating temperature range.

4.0 PHASE III DEMONSTRATION TESTS

Testing was conducted in Phase III in order to establish a performance baseline for each of the three SRI controllers. The baseline data may be used to verify system performance during subsequent operation. The results of acceptance test activity is summarized in the following paragraphs for the three Protection and Control Units. Discussion of testing activity includes test results for three different SRI converters.

4.1 SYSTEM INTEGRATION

Discrete component breadboard circuit plugcards were removed from each of the three card cage controllers. Hybrid circuit plugcards were designed to be pin-for-pin compatible with the discrete component plugcards. These hybrid circuit plugcards were integrated into each card cage controller and performance tested with each of the three demonstration SRI power stages.

4.2 ACCEPTANCE TEST PROCEDURES

There are three typed acceptance test procedures, one for each of the following control and protection configurations:

Power Converter	Procedure Number
- 10 kW dc/dc	850AT110000-0P12
- 5 kW ac/dc	850AT100000-0P12
-200 kW dc/dc	850AT120000-0P12

The acceptance test procedures are defined by Martin Marietta Standard Procedure number 101.1, Test Procedures and Performance. The standard test procedure format used is shown below:

1.0 Scope
2.0 Support Requirements
3.0 Special Considerations
4.0 Test Operations
5.0 Securing
6.0 Figures
7.0 Tables

4.3 ACCEPTANCE TESTING

The following schedule was used to establish acceptance testing and test results are referenced:

10 kW Acceptance Test--A demonstration test was performed to Acceptance Test Procedure number 850AT110000-0P12 at Martin Marietta Denver. Test results are summarized in Tables 4.3-1 and 4.3-2.

Table 4.3-1 Supply Voltages and Signal Test Values, 10kW SRI

OUTPUT	.....MEASUREMENT POINT..... SIGNAL POINT	REFERENCE	SPEC	DATA
Supply Power	Card Edge Pin 2	+15.0 VDC	14.7/ 15.3	+15.06
Supply Power	Card Edge Pin 3,C	+ 5.0 VDC	4.90/ 5.10	+ 5.05
Supply Power	Card Edge Pin 1,A	+15.0 VDC	14.7/ 15.3	+15.01
Supply Power	Card Edge Pin B	-15.0 VDC	-15.3/-14.7	-15.01
Housekeeping Power	BBS Card Edge Pins 7 to H	14 V p-p	13.0/ 15.0	14.5
		25 Khz	20.0/ 30.0	24.9

Table 4.3-2 Regulation Test Data, 10kW SRI

TEST 1--LOAD REGULATION

Source Voltage

Ref. 300 Act. 300.2

RUN		Load Resistance	Output Voltage
1	Ref.	6.25	100
	Act.	6.22	100.6
2	Ref.	25.0	100
	Act.	25.0	100.2
3	Ref.	62.5	100
	Act.	62.04	100.2

TEST 2--LINE REGULATION

Load Resistance

Ref. 6.25 Act. 6.22

RUN		Source Voltage	Output Voltage
1	Ref.	270	100
	Act.	269.9	100.2
2	Ref.	300	100
	Act.	300	100.2
3	Ref.	330	100
	Act.	330.5	100.2

5 kW Acceptance Test--A demonstration test was performed to Acceptance Test Procedure number 850AT100000-0P12 at martin Marietta Denver. Test results are summarized in Tables 4.3-3 and 4.3-4.

Table 4.3-3 Supply Voltages and Signal Test Values, 5kW SRI

OUTPUT	.....MEASUREMENT POINT..... SIGNAL POINT	REFERENCE	SPEC	DATA
Supply Power	Card Edge Pin 2	+15.0 VDC	14.7/ 15.3	+15.07
Supply Power	Card Edge Pin 3,C	+ 5.0 VDC	4.90/ 5.10	+ 5.05
Supply Power	Card Edge Pin 1,A	+15.0 VDC	14.7/ 15.3	+15.02
Supply Power	Card Edge Pin B	-15.0 VDC	-15.3/-14.7	-15.00
Housekeeping Power	BBS Card Edge Pins 7 to H	14 V p-p	13.0/ 15.0	14.5
		25 Khz	20.0/ 30.0	24.9

Table 4.3-4 Regulation Test Data

TEST 1--LOAD REGULATION

Source Voltage

Ref. 208 Act. 208.2

RUN		Load Resistance	Output Voltage
1	Ref.	8.3	200
	Act.	8.26	200.4
2	Ref.	25.0	200
	Act.	24.98	200.7
3	Ref.	75.0	200
	Act.	74.44	200.8

TEST 2--LINE REGULATION

Load Resistance

Beginning of Test

End of Test

Ref. 8.3 Act. 8.30 8.12

RUN		Source Voltage	Output Voltage
1	Ref.	187	200
	Act.	186.4	200.2
2	Ref.	208	200
	Act.	208.2	200.3
3	Ref.	229	200
	Act.	229.0	200.4

200 kW Acceptance Test--A demonstration test of the control and protection circuitry was performed with the scale model of the APL 200 kW power stage to Acceptance Test Procedure number 850AT120000-0P12 at Martin Marietta Denver. Test results are summarized in Tables 4.3-5 and 4.3-6.

Table 4.3-5 Supply Voltages and Signal Test Values, 200kW Scale Model

	.....MEASUREMENT POINT.....			
OUTPUT	SIGNAL POINT	REFERENCE	SPEC	DATA
Supply Power	Card Edge Pin 2	+15.0 VDC	14.7/ 15.3	+15.02
Supply Power	Card Edge Pin 3,C	+ 5.0 VDC	4.90/ 5.10	+ 5.02
Supply Power	Card Edge Pin 1,A	+15.0 VDC	14.7/ 15.3	+14.98
Supply Power	Card Edge Pin B	-15.0 VDC	-15.3/-14.7	-15.03
Housekeeping Power	BBS Card Edge Pins 7 to H	14 V p-p	13.0/ 15.0	15.0
		25 Khz	20.0/ 30.0	24.3

Table 4.3-6 Regulation Test Data, 200kW Scale Model

Note: Voltages reduced because D.C. power source used for test could not provide sufficient power to run original test.

TEST 1--LOAD REGULATION

Source Voltage

Ref. 225 Act. 225.0

RUN		Load Resistance	Output Voltage
1	Ref.	8.33	150
	Act.	8.5	150.94
2	Ref.	25.0	150
	Act.	25.4	150.19
3	Ref.	75.0	150
	Act.	76.0	150.27

TEST 2--LINE REGULATION

	Load Resistance		Beginning of Test	End of Test
Ref.	8.33	Act.	8.4	8.12

RUN		Source Voltage	Output Voltage
1	Ref.	200	150
	Act.	200.3	150.84
2	Ref.	225	150
	Act.	225.15	150.98
3	Ref.	250	150
	Act.	250.24	151.06

Demonstration at APL--The control and protection circuitry is scheduled for demonstration with all three APL power stages at APL. Test results were not available at the time this final report was printed.

5.0 RECOMMENDATIONS

From the IC technology study, we recommend that the prototype circuits for the back-bias sensor, firing pulse generator, protection unit, and three-phase unit be fabricated with hybrid circuit technology because these circuits have wide application and few external components. We also recommend that the prototype circuit for the control unit be fabricated from discrete components at this time because of the many external components required to customize it to a given power stage topology.

We recommend that CMOS be used for digital circuits because of the low power dissipation, high noise immunity, and availability of radiation-hard equivalents. LM108s and LM111s are recommended for operational amplifiers and comparators because they will meet the electrical requirements of the program and are widely available in both commercial and radiation-hard versions.

The three block diagrams made in the functional design task show the recommended connections of the functional circuits for control and protection of the three SRI power units. The control and protection tasks were grouped into five custom circuits. These custom circuits can be configured to work with all three SRI power units. The five recommended custom circuits are:

1) Back-bias sensors,
2) Firing pulse generator,
3) Protection unit,
4) Three-phase unit, and
5) Control unit.

From the microprocessor study, we recommend that a microprocessor not be incorporated in the present system to reconfigure the prototypes to the different power stages because this is an unproductive use of a microprocessor and would add unnecessary complications. Recommendations are made in the body of the report, however, on possible functions for a microprocessor in a future SRI-based converter.

6.0 LIST OF REFERENCES

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APPENDIX A--RADIATION-HARD MICROPROCESSOR CHIP SETS

Under Mr. Conklin, the Air Force Avionics Lab has played a leading role in pursuing space-qualified development of CMOS/SOS technology. Their work has resulted in what is commonly referred to as the Conklin chip set, or the AFWAL/RCA chip set.

Six device types were of interest in the AFWAL/RCA chip set. Table A-1 summarizes these device types. Three of the device types merit special explanation. The TCS 129 general processing unit (GPU) forms the foundation for the entire chip set. It is an 8-bit-wide ALU slice that can be cascaded to form an arbitrarily wide data word. In addition to shift and complement operations, the GPU can perform ADD, NAND, and OR operations. The TCS 196 is an 8x8-bit two's complement multiplier that can be cascaded to form an NxN multiplier without the use of external logic. This was done by providing partial product logic and signals on the device. The TCS 093 gate universal array (GUA) is used to bind the other devices in the chip set to form a complete system. This large-scale integration (LSI) device eliminates the need for medium-scale integrated (MSI) and small-scale integrated (SSI) circuits. GUAs are fixed regular patterns of transistors and routing paths. By defining the transistor interconnections, GUAs are customized with logic in much the same way read-only memory (ROM) is customized with data.

Table A-1 AFWAL/RCA CMOS/SOS Microprocessor Chip Set

GPU TCS 129 - General processing unit - 8-bit parallel slice - Concatenatable - Fully static - 125-ns register add	MUL TCS 196 - 8x8-bit multiplier - Expandable - Completely asynchronous - Latched-input operands
RAM TCS 246 - Random-access memory - 4k x 1-bit organization - 125-ns access time - Read-only memory - Fully static 4096 bits - Mask-programmable - 100-ns cycle time	GUA TCS 093 - Gate universal array -Customized logic - 632 gate-level complexity - 64 pads - Proven cell library - 100-mHz high-speed divider - 452,300, and 182 GUAs also available
	2910 Controllers TCS 158 - Microprogram controller - Functional equivalent to Am2910

The AFWAL/RCA chip set has been implemented in SOS by RCA and by the Center for Radiation-Hardened Microelectronics (CRM) at Sandia Laboratories in their CMOS bulk process.

The AFWAL/RCA chip set has an 8-bit-wide slice architecture. The bit slice architecture requires a large amount of work to produce a working computer, i.e., instruction set definition, microprogramming, and control logic design and reduction to gate arrays. The word length can be 8 bits, or multiples of 8 bits (8, 16, 24, etc). This type of computer will very likely have much more computing power than will be required by a dedicated SRI computer (these are spacecraft central computers, not dedicated power converter microprocessors).

CRM has also produced a radiation-hardened version of an 8-bit microprocessor: Intel 8085 and its peripheral chips. The radiation-hardened version of an Intel 8085 is expected to be much closer to the requirements for a dedicated AIT microprocessor than the bit slice architecture of the AFWAL/RCA chip set.

Table A-2 summarizes the bulk CMOS design constraints.

Table A-2 CRM Radiation-Hard Bulk CMOS Design Constraints

- Replace N-CH Transmission Gates with Complementary Pairs
- Progressive Buffering (Fanout Less Than 4)
- Eliminate 8-Input NANDS

The CRM Sandia National Laboratories radiation-hardened CMOS microprocessor family has the SA3000 microprocessor (Intel 8085A equivalent). The family also contains hardened CMOS peripheral chips: RAM, ROM, Decoder, CMOS-TTL Level Converter, Bus Transceiver, and I/O Port. A description of the Sandia part numbers and commercial equivalents is in Table A-3. Table A-4 is a summary of the bulk CMOS characteristics.

Table A-3

Radiation-Hardened CMOS Equivalents of Intel 8085A Microprocessor and Support Chips

- SA3000 Microprocessor (Intel 8085A Equiv)
- SA3001 RAM I/O-Timer (Intel 8155/56 Equiv)
- SA3002 ROM I/O (Intel 8355 Equivalent)
- SA2998 128X8 MNOS RAM
- SA2999 2KX8 MNOS EAROM
- SA2995 3-to-8 Decoder (LS138)
- SA2996 CMOS-TTL Level Converter (Noninverting CD40116)
- SA2997 Bus Transceiver (NSC82PC08)
- SA3025 I/O Port (8212)

Table A-4 Bulk CMOS Technology Characteristics

- Bulk, P-Well
- Single Guard Band
- Projection Lithography
- Dry Processing for Critical Steps
- Radiation Hardness -10^6 rads (Si)
- Gate Delay 1 to 4 ns
- 10-V Operation

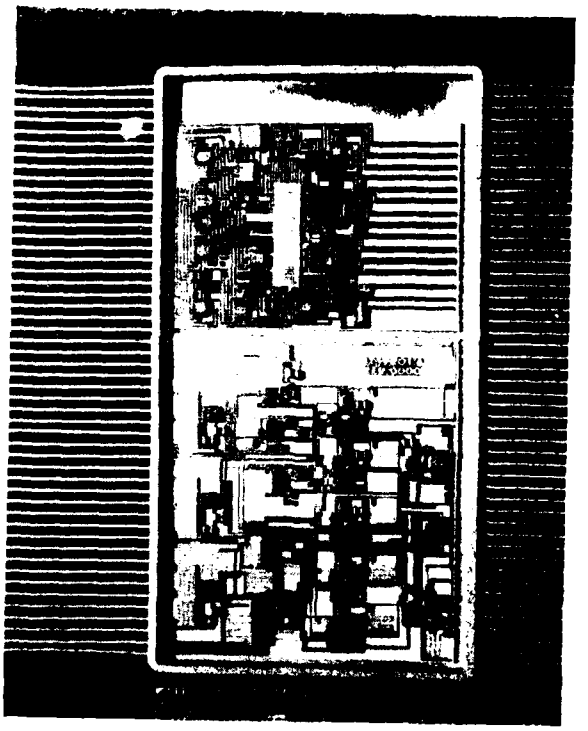
APPENDIX B LIST OF SRI EQUATIONS

Equations for Continuous Conduction Mode

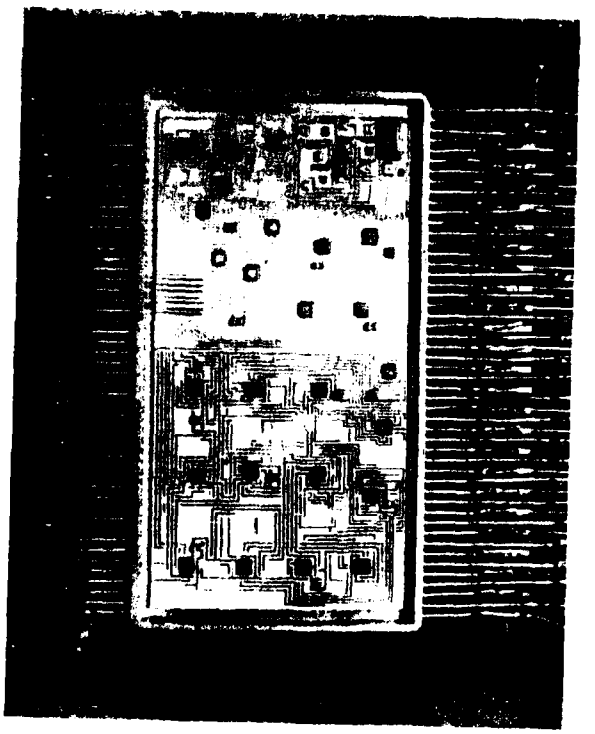
1. $q = V_o/V_s$
2. $Zo = \sqrt{L/C}$
3. α = Control Angle
4. β Power Switch Conduction Angle
5. $I_o = (V_s/Z_o)[(1 - q^2)\sin\alpha/(q - \cos\alpha)]$
6. $I_{avg} = (V_s/Z_o)[2(1 + q)(1 - \cos\alpha)/(\alpha + \beta)(q - \cos\alpha)]$
7. $I_{peak} = (V_s/Z_o)[(1 + q^2 - 2q\cos\alpha)/(q - \cos\alpha)]$
8. $$I_{rms} = \{[1/(\alpha + \beta)][I_0^2(\beta/2 + \sin2\beta/4) + [(V_{co} + V_s - V_o)/Z_o]^2(\beta/2 - \sin2\beta/4) + I_o[(V_{co} + V_s - V_o)/Z_o]\sin^2\beta + [(V_{c1} + V_s + V_o)/Z_o]^2(\alpha/2 - \sin2\alpha/4)\}^{1/2}$$
9. $I_{Qavg} = [(1 + q)/4]I_{avg}$
10. $I_{Davg} = [(1 - q)/4]I_{avg}$
11. $V_{co} = V_s[q(1 + q)(1 - \cos\alpha)/(q - \cos\alpha)]$
12. $V_{c1} = V_s[-(1 + q)(1 - \cos\alpha)/(q - \cos\alpha)]$
13. $V_{cpeak} = V_s[\pm(1 + q)(1 - \cos\alpha)/(q - \cos\alpha)]$

Equations for Discontinuous Conduction Mode

14. $I_{avg} = (V_s/Z_o)[4/(\alpha + \pi)]$
15. $I_{peak} = (V_s/Z_o)(1 + q)$
16. $I_{rms} = (V_s/Z_o)[(1 + q^2)\ \pi/(\alpha + \pi)]^{1/2}$
17. $I_{Qavg} = [(1 + q)/4]I_{avg}$
18. $I_{Davg} = [(1 - q)/4]I_{avg}$
19. $V_{co} = V_s(2q)$
20. $V_{c1} = V_s(-2)$
21. $V_{cpeak} = V_s = V_s(\pm2)$



Protection Unit Hybrid



Three Phase Unit Hybrid

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