



MICROCOPY RESOLUTION TEST CHART
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SECURITY CLASSIFICATION OF THIS PAGE

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REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION Unclassified		1b. RESTRICTIVE MARKINGS	
2a. SECURITY CLASSIFICATION AUTHORITY ---		3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited	
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A		5. MONITORING ORGANIZATION REPORT NUMBER(S) AFOSR-TR. 85-0875	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)		6a. NAME OF PERFORMING ORGANIZATION New York State CASE, Syracuse	
6b. OFFICE SYMBOL (If applicable)		7a. NAME OF MONITORING ORGANIZATION AFOSR	
6c. ADDRESS (City, State and ZIP Code) Hinds Hall, Syracuse, NY 13210		7b. ADDRESS (City, State and ZIP Code) Bldg. 410 Bolling AFB, D.C. 20332-6448	
8a. NAME OF FUNDING/SPONSORING ORGANIZATION AFOSR		8b. OFFICE SYMBOL (If applicable) NM	
8c. ADDRESS (City, State and ZIP Code) Bldg. 410 Bolling AFB, D.C. 20332-6448		9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER AFOSR-85-0065	
11. TITLE (Include Security Classification) Interim Report - Grant AFOSR-85-0065		10. SOURCE OF FUNDING NOS.	
		PROGRAM ELEMENT NO. 61102F	PROJECT NO. 2304
		TASK NO.	WORK UNIT NO.

2. PERSONAL AUTHOR(S)

Dr. Bradley J. Strait

3a. TYPE OF REPORT

Interim

13b. TIME COVERED

FROM 1 Oct 84 to 30 Jun 85

14. DATE OF REPORT (Yr., Mo., Day)

30 June 1985

15. PAGE COUNT

9

6. SUPPLEMENTARY NOTATION

7. COBATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number) Systems automation, VAX 11/780
FIELD	GROUP	SUB. GR.	
XXXXXXXXXXXX	XXXX	XXXX	

9. ABSTRACT (Continue on reverse if necessary and identify by block number)
 The DOD University Research Instrumentation grant together with cost sharing by Syracuse University and grants/ discounts from equipment manufacturers has created a sizable research facility of Syracuse, including a VAX 11/780 system, 4 AED graphics terminals, a Hewlett Packer Drafting plotter and an Imager Laser printer. Research projects being supported include "New Generation Knowledge Processing", "Concurrent Computer Architectures for Unification Operations", "Construction of a Multiprocessor Reduction Machine for the Support of Logic Programming", "Logic Programming and Knowledge Base Maintenance and An Initial Architecture for the Solution of the Partial-Match Retrieval Problem in the Context of Logic Programming".

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OCT 15 1985

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT UNCLASSIFIED/UNLIMITED <input checked="" type="checkbox"/> SAME AS RPT. <input type="checkbox"/> DTIC USERS <input type="checkbox"/>		21. ABSTRACT SECURITY CLASSIFICATION Unclassified	
22a. NAME OF RESPONSIBLE INDIVIDUAL Dr. Robert N. Buchal		22b. TELEPHONE NUMBER (Include Area Code) (202)767-4939	
		22c. OFFICE SYMBOL NM	

AD-A160 598

NEW YORK STATE CENTER FOR ADVANCED TECHNOLOGY IN
COMPUTER APPLICATIONS AND SOFTWARE ENGINEERING

INTERIM REPORT - GRANT NO. AFOSR-85-0065

Accession For	
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Unannounced	<input type="checkbox"/>
Justification	
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June 30, 1985



Submitted to:

Dr. Robert N. Buchal
AFOSR/NM
Building 410
Bolling AFB, DC 20332-6448

Submitted by:

Dr. Bradley J. Strait
Managing Director
CASE Center
Syracuse University
Syracuse, New York 13210

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INTRODUCTION

This is the Interim Report on contract AFOSR-85-0065 between the Air Force Office of Scientific Research (AFOSR) and the New York State Center for Advanced Technology in Computer Applications and Software Engineering (CASE Center) at Syracuse University. This grant program provides \$274,028 from AFOSR toward the purchase of a VAX 11/780 computer system to create a laboratory for Systems Automation Through Artificial Intelligence. Presented here are descriptions of research projects conducted through the Artificial Intelligence Consortium, a listing of the equipment and peripherals installed to date, and summaries of the research programs that are being carried out using this computer facility.

ARTIFICIAL INTELLIGENCE CONSORTIUM

One of the major research-related activities of the CASE Center over the past year included establishment of the Artificial Intelligence Consortium, sponsored by the Rome Air Development Center at a funding level of \$8 million over five years. The purposes of the Artificial Intelligence Consortium are (1) to increase basic research capabilities and activities in artificial intelligence (AI) at participating academic institutions, (2) to apply AI techniques to problems of mutual interest, and (3) to increase the research and teaching resources available for education and training of new AI researchers and practitioners, particularly at the Rome Air Development Center.

The Systems Automation Through Artificial Intelligence facility is used extensively in the Syracuse University based research projects associated with the Artificial Intelligence Consortium. Following are brief abstracts of these projects.

Project: Software and Hardware Architectures for Increasing Performance of Very Large Knowledge-Based Systems

P. Bruce Berra, Professor, Electrical & Computer Engineering

This project consists of two tasks, the first of which is to develop advanced software and hardware architectures for knowledge-based systems that are sufficient to overcome fundamental limitations in current techniques for implementing, managing, and maintaining knowledge bases. This first task is approached by seeking new software and hardware techniques to enhance the performance of systems that manage knowledge through use of logic, production rules, semantic networks, and frames. Since management of a very large knowledge base is a fundamental problem within a knowledge-based system, it is intended that this phase of the project concentrate initially on exploiting the relatively well-developed fields of database management and database machines.

The second task is a subset of the first. It consists of research leading to software and hardware architectures that support efficient logic programming.

Ways are sought to exploit inherent parallelism, eliminate processing bottlenecks, and implement unique secondary storage organizations pertinent to logic programming systems.

Project: Knowledge Base Maintenance Using Logic Programming Methodologies

Kenneth A. Bowen, Professor, Computer & Information Science

The knowledge bases used to support Air Force missions over the next decade will assist both human and automated experts to perform various tasks ranging from logistical support to C3I and intelligence analysis. In these latter two examples, the knowledge bases will be large, complex, and highly volatile. This project addresses the problem of providing basic automated machinery for the management of such knowledge bases, especially the maintenance of consistency and integrity constraints. The work is carried out from the point of view of certain logic programming systems, namely the "meta-level" systems, primarily embodied in a system called metaProlog.

EQUIPMENT

In order to establish this research facility, the following equipment has been purchased, delivered and installed:

No.	Unit Description	Cost
	Vendor: Digital Equipment Corporation	\$262,089
1	VAX 11/780 Standard System, with Fixed Disk and Controller and Magnetic Tape Drive	
1	MS780-FA 2MB (64K) ECC MOS Expansion Memory	
2	DMF32-M Communications Controllers	
1	DF100-RM Modem Enclosure	
1	DF100-PR Power Regulator	
1	DW780-AA Unibus Adaptor	
1	BA11-KU Expansion Box	
1	DD11-DK Expansion Backplane	
1	H7007-AC Surge Suppressor	
2	CK-DMF32-LDCAB Kit Multifunction GNL	
4	VT220-AA A/N Video Terminals	
4	VT22K-A Country Kits	
3	DF03-RA 300/1200 Modems	
1	DF03-RC 300/1200 Auto Call Modem	
3	DF112-AM 300/1200 Sync/Asyn Rack Mode	
1	DF112-AM Modem in a DF100-D	
1	RA81-AA 456 MB 16B Disk, 12-OV/60, NO C	

No.	Unit Description	Cost
	Vendor: Advanced Electronic Design Inc.	\$ 41,021
4	AED 767T8A6 - 767 Table Top Color Graphics Terminals	
4	AED 767M06A6 - 19" Diagonal Long Persistence Monitors	
	Vendor: RG Engineering	\$ 4,236
1	Bit Pad One, 15" x 15" with RS-232 Interface, Controller, Biasing Device, and Manual	
1	Four Button Cursor	
1	Standard Wall Mount Power Supply and 10' Interface Cable	
3	Bit Pad Two, 11" x 11" with RS-232 Interface, Controller, and Technical Reference Manual	
3	Four Button Cursors	
3	Power Supplies and Cables	
	Vendor: ATT	\$ 400
1	CPU License for UNIX System	
	Vendor: University of California - Berkeley	\$ 750
1	UNIX License	
	Vendor: Hewlett-Packard Corporation	\$ 19,977
1	7586B Option 065 Drafting Plotter	
1	7475A 6 Pen Graphics Plotter	
	Vendor: Imagen Corporation	\$ 11,266
1	Model 8/300 Laser Printer System, 512Kbytes memory	
1	Additional 512Kbytes memory for Printer	
1	Firmware Maintenance	
1	DIMP Host Software Support for Printer	
1	Additional Paper Tray for Model 8/300 Printer	
4	Print Cartridges for Printer	
	TOTAL EXPENDITURES	\$339,739

There have been some changes to the configuration of the system as outlined in the proposal to the Department of Defense. The DZ11-DP communications interfaces were replaced by DMF32 communication controllers that provide more lines of access, and the DF02-AC modems were replaced with DF112 modems, which are upgraded models. A reevaluation of the graphics needs of the system, showed that the Imagen 8/300 Laser Printer

was equivalent to the Versatec plotter for small plots and better for text output purposes, and, in combination with the smaller HP 7475 plotter, would better serve the researchers using the system.

The faculty members involved in research programs using this computing system, have formed a VAX Management Committee to oversee the operation of the facility. In addition, the CASE Center is seeking a programmer to supervise day-to-day activities.

RESEARCH PROJECTS

There are a variety of ongoing research efforts being conducted at the CASE Center that are able to make extensive use of this computing system. Following are brief descriptions of current research projects associated with the Systems Automation facility.

Project: New Generation Knowledge Processing
RADC Contract #F30602-84-K-0001

**J. Alan Robinson, University Professor and Research
Director, CASE Center**

The objective of this project is to design and implement an ultra-high-level programming system called SUPER (Syracuse University Parallel Expression Reduction). The system will consist of a programming language and a multi-processor architecture. The SUPER language will be a programming language combining certain features of the lambda calculus, the predicate calculus, and set theory, together with a collection of primitive constants sufficient to furnish the main features of LISP and of LOGIC programming. As noted above, this work is supported by the Rome Air Development Center under Contract #F30602-84-K-0001.

Coincident with the development of the SUPER language, Drs. Oldfield and Berkling are responsible for the development of a SUPER machine. The goal of the SUPER machine project is to design and construct a hardware machine which provides part of or all the basic architecture support structure for the SUPER language. Abstracts of their projects follow.

**Project: Concurrent Computer Architectures for Unification
Operations**

**John V. Oldfield, Professor of Electrical & Computer Engineering
Chairman, VAX Management Committee**

Unification is a fundamental operation of logic programming systems such as LOGLISP and PROLOG. It accounts for a large proportion of the time spent by conventional computers in executing logic programs. Thus, speedup in unification would markedly improve the performance of many computer applications, including large-scale expert systems. This project is an integral part of the SUPER LOGLISP project, a broad-ranging research effort to

extend the capabilities of logic programming by language improvements and novel software methods as well as by special architectures and hardware components. The computer architecture envisaged will exploit concurrent operation and custom VLSI circuits where appropriate. The Syracuse Unification Machine (SUM) is a prototype system intended to develop the groundwork for more ambitious schemes and yet at the same time be capable of solving realistic problems. SUM is an experimental coprocessor for an existing host computer, such as an LMI Lambda Lisp machine, and is designed to accelerate unification by means of a computer architecture that permits major functional units to operate concurrently. It incorporates several custom VLSI chips. One critical unit of SUM, the Binding Agent, has been designed. It employs a content-addressable memory in the form of an Associative Stack. A prototype chip has been designed and successfully tested. When the full-scale version is incorporated in a Binding Agent, this should result in about a hundredfold speedup over software methods. Although SUM will not lead to such dramatic acceleration in the overall unification task, the results will guide the design of future systems with more concurrency and higher chip packing densities.

This project is currently supported through the CASE Center and Dr. Oldfield has recently applied to DARPA for continuing support of the research.

**Project: Construction of a Multiprocessor Reduction Machine
for the Support of Logic Programming**

Klaus J. Berkling, Research Professor, CASE Center

The goal of this project is to construct a very high-level "new generation" architecture that will support symbolic computation in general. In particular, it will provide support for a language embodying both function programming (lambda calculus) and logic programming (predicate calculus) in a simple architecture whose main features correspond directly to those of the language itself. The meaning of expressions of the language is given by reduction rules. Computation consists of reducing a given (input) expression by methodically rewriting it according to these rules until an (output) expression is obtained. Dr. Berkling constructed a machine on these lines in Germany several years ago (the RED1 Machine) and demonstrated successfully a direct hardware realization of the fundamental beta reduction rule of the lambda calculus, which is the main rule governing pure LISP. In this project, the successor of the RED1 machine is referred to as RED2, which will extend the RED1 design in several directions.

1. Whereas RED1 was a single-processor system, performing one reduction at a time, RED2 will be a multi-processor system exploiting the fact that in general an expression contains many subexpressions ready to be rewritten independently of each other.
2. RED1 dealt only with LISP's basic function application transformation, by means of the beta-reduction rule. RED2 will also deal with Prolog's basic unification transformation, by means of new rules.

3. Whereas RED1 was a pure string-reduction system, requiring no memory addresses, RED2 will be a graph-reduction system, emphasizing the sharing of common structures through pointers.

This project is currently supported through the CASE Center. Dr. Berkling has recently applied to both DARPA and the Semiconductor Research Corporation for support for this project.

**Project: Logic Programming and Knowledge Base Maintenance
Grant # AFOSR-82-0292**

**Kenneth A. Bowen, Professor, School of Computer & Information
Science**

This project involves the exploration of questions of the logical status of some of the standard data structures involved in various artificial intelligence applications involving knowledge bases, with the greatest attention being focused on frames. It is felt that classes of concrete frames (e.g. representatives of scenes, or aircraft or ships) can both be axiomatized and also be given efficient, but still logical, implementations in some logic programming systems, specifically those providing a measure of metalevel expressiveness and inference. The basic axiomatization of object-level "frames with slots" as "entities with attributes" is possible in simple object-level logic programming systems. However, some of the more powerful aspects of frame-based reasoning utilize default filling of slots, together with "is-a" and "kind-of" hierarchies. The explicit representations of these modes of reasoning require metalevel facilities in the axiomatized logic. Study and experimentation have also been devoted to the development of efficient implementation techniques for these axiomatizations in Prolog-type languages. A technique that represents the frame as a generalized record structure embodying pointers between frames (which are not directly accessible to the logic programming system) has been developed. The difficulty in using such representation in logic programming systems lies in providing efficient access to the components in the face of dynamic change of components and the logical requirements of the basic system. Specifically, ordinary Prolog systems would represent updates by term complexes containing embedded copies of the original structure. This is done in order to provide support for exploration of logical alternatives (implemented via backtracking). The current approach causes updates to be immediately written directly to the components of the structure, and preserves information about the original state of the structure via an extension of the so-called "trail mechanism" used in Prolog implementations to reset values of variables during backtracking.

Experiments have been carried out in three areas:

1. Expression of various quasi-intelligent expert systems tasks,
2. Development of basic knowledge base systems, and
3. Exploration of reasoning systems for maintenance of knowledge bases.

Plans for the immediate future are to vigorously pursue the implementation of the designs developed to date. Once the core system is up and stabilized, work on the construction of serious example knowledge bases using the newly implemented system, and the exploration of truth maintenance over these knowledge bases, will be pursued.

The VAX 11/780 system provided through a grant from the Department of Defense, has been an essential tool in carrying this work forward. All of the compiler development has been carried out on this system since February, as well as the current work with the metaProlog simulators. Without the VAX, this work would have been severely hampered.

**Project: An Initial Architecture for the Solution of the
Partial-Match Retrieval Problem in the Context of
Logic Programming
RADC Contract #F30602-81-C-0169**

P. Bruce Berra, Professor, Electrical & Computer Engineering

One of the most rapidly growing fields of Artificial Intelligence is Expert Systems. Currently expert systems exist or are being constructed in medicine, business, engineering, and in national defense. These systems are composed of a knowledgebase that consists of rules and facts and an inference mechanism that is used to develop new information from the existing knowledgebase. The object of such systems is to capture the knowledge of experts in particular domains and make it generally available to nonexperts. The current state of the art is such that expert systems focus on narrow domains, have small knowledgebases and therefore have limited application. However, the concept of capturing the knowledge of the most learned persons in particular fields is so compelling that considerable research is being carried out to greatly extend the capabilities of these systems.

As these systems are expanded there will be increased demands on the management of the knowledgebase. The intensional database of rules will become large and will present a formidable management problem in itself. However, the major management problem will be in the access, update and control of the extensional database of facts. The number of facts that will be required by future expert systems will be in the gigabyte range and we can expect to have general extensional databases that serve multiple inference mechanisms. Current research includes the investigation of the development of new, more intelligent ways to interface with existing databases to make this vast wealth more readily available. These systems are often called intelligent database systems but they are really attempts at more general expert systems.

During the course of this effort we have concentrated on developing the necessary bridges between logic programming and relational database management. We have considered the use of concatenated and superimposed code words and their variations along with associative devices to solve the resulting partial match retrieval problems. In so doing we have tacitly assumed that there is a distinct division between the logic programming

portion and the relational database portion. However, in the future we plan to look carefully to determine if the need exists for the integration of these two entities and if so what computer architectures will yield maximum performance.

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