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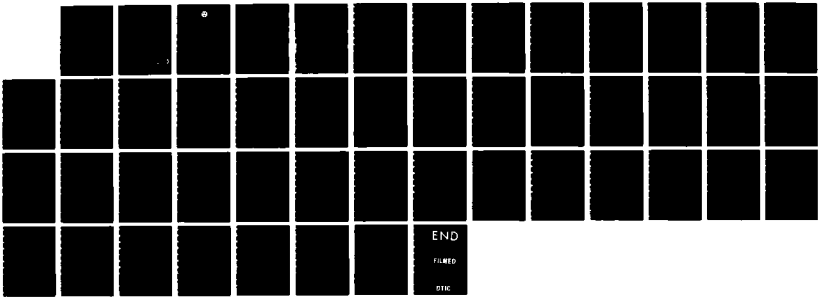

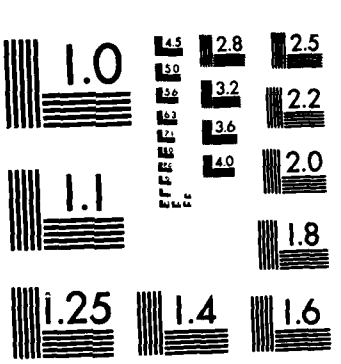

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# NOSC UNIBUS/UNIVAC INPUT/OUTPUT CONTROLLER

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19 ABSTRACT (Continue on reverse if necessary and identify by block number)

This specification describes the use of the NOSC UNIBUS/UNIVAC input/output controller with peripheral and computer input/output subsystems to be connected to a UNIBUS-type host computer via the input/output controller.

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# SECTION 1. INTRODUCTION

## 1.1. IOC DEFINITION

The NOSC-developed UNIBUS*/UNIVAC compatible Input/Output Controller (IOC) is designed to provide any host computer supporting the Digital Equipment Corp. UNIBUS configuration with an Input/Output (I/O) channel whose protocol, timing, and electrical interface specifications are compatible with standard NTDS FAST and Univac 1100 series I/O channels. In addition, true differential I/O operation is provided for use in systems where this is supported or where intercomputer grounding problems exist.

The IOC can operate when connected to either a peripheral I/O device such as a line printer or a card reader (normal mode), or the I/O channel of another computer (intercomputer mode). The mode is software selectable. By using IOCs in multiple hosts, parallel intercomputer channels may be readily established between them. Unless specifically noted otherwise, the device connected to the IOC will be referred to as the "I/O subsystem" regardless of the mode being used. The computer housing the IOC will be referred to as the "host."

Keywords: Input/Output Signals

## 1.2. SCOPE

This specification is intended to make the IOC understandable to persons who design and implement peripheral and computer I/O subsystems to be connected to a UNIBUS-type host computer via the IOC. It defines both interface characteristics and the programming and operation of the IOC from a programming point of view. All numbers are given in decimal unless indicated otherwise.

## 1.3. PHYSICAL DESCRIPTION

The IOC is contained on a single hex-high wirewrap card which may be plugged into any convenient "small peripheral" slot in the host computer that can accommodate a hex-high card. Because of the length of the wirewrap pins and the height of the IC sockets, the IOC card must have one empty slot on each side of it. Optionally, the IOC may be mounted in its own enclosure. The UNIBUS may then be brought into this enclosure using a ribbon cable and an edge connector paddle board which plugs into and occupies only one quad-high small peripheral slot.

Since the IOC is a non-processor request (NPR) device, the slot into which it is plugged must be wired to allow the non-processor grant (NPG) signal to enter the card on backplane pin CA1 and exit it on pin CB1. This is normally done by removing the UNIBUS backplane jumper wire between these pins. The IOC also issues bus requests (BRs) at the level chosen by the user. The interrupt and grant** levels are jumper selectable on the component side of the card (figure 6.3).

The card requires +5 volts at 8 amps max. and -15 volts at 1.0 amps max. which it obtains from the UNIBUS backplane. A maximum of two bus loads is presented on any signal line. Connection to the IOC I/O channel is made via one

*UNIBUS is a registered trademark of Digital Equipment Corporation.
**All figures are located in section 6.

of two pairs of 50-pin ribbon cable connectors mounted on the IOC card. One pair (X & Y) is for differential I/O and the other pair (Z & G) is for NTDS FAST I/O (figure 6.1).

## 1.4. FUNCTIONAL DESCRIPTION

Each IOC provides the host processor with one I/O channel and directs and monitors the flow of information between the I/O subsystem connected to this channel and the host memory. It performs the required addressing functions and synchronizes I/O sequences to the processor and memory timing. Figure 6.4 shows the IOC functional block relationships.

The IOC contains 1025 words of input data FIFO buffer, 1025 words of output data FIFO buffer, and 1025 words of external interrupt FIFO buffer. Transfers between the two data buffers and the host memory are performed using the Direct Memory Access (DMA) mode while all other transfers are performed under program control. All host memory transfer addresses are set up by the processor prior to the transfer itself and, thus, the Univac Externally Specified Index (ESI) mode is not supported.

A host may use as many IOCs as the physical confines of the system will accommodate, assuming that sufficient device addresses and floating vectors are available. Each IOC occupies 10 (octal) consecutive words of device address space (although only the first 6 are used) and requires 4 floating vectors. The device addresses must start at the beginning of a 10 (octal) word boundary. Similarly, the floating vectors, which are each spaced 2 words apart, must start at the beginning of another 10 (octal) word boundary. The base values (boundaries) for both device addresses and floating vectors are jumper selectable on the component side of the card (figure 6.2).

## 1.5. I/O CHANNEL TRANSFER RATES

The maximum instantaneous data transfer rate on one IOC input or output channel is 1.17 million words per second (850 nanoseconds per transfer) using the standard timing mode and 285 thousand words per second (3.5 microseconds per transfer) using NTDS FAST timing. Simultaneous input and output does not degrade these rates. They, however, apply only to output and input data transfers and external interrupts. Both forced and buffered external functions are transferred one at a time under host program control and can be considerably slower.

Note that simultaneous I/O refers only to I/O channel activity and not to UNIBUS activity. From a UNIBUS standpoint, the IOC is a half-duplex device since it has only one set of control registers.

## SECTION 2. I/O INTERFACE

### 2.1. GENERAL DESCRIPTION OF INTERFACE

The IOC/host interface consists of a set of wires with logical, electrical, and mechanical conventions established for the transmission of signals between the IOC I/O channel and the attached I/O subsystem. Each input and output cable contains the signal lines necessary to transmit 16 bits of data and 1 parity bit plus all necessary control signals. The cables each require a 50-contact, twisted-pair, female ribbon cable connector at the IOC end and connectors at the other ends as necessary to connect the I/O subsystem.

### 2.2. ELECTRICAL INTERFACE

The interface transmission system consists of differential or NTDS FAST drivers and receivers interconnected by the I/O cables. The potential difference between the host reference ground and the reference ground of any I/O subsystem connected to the IOC must not exceed plus or minus 19 volts when operating differentially. The potential difference must be 0 volts for NTDS FAST operation. The I/O subsystem must respond to the leading edge of the control signals during their transition from the "negated" to the "asserted" state. The receiving logic must be independent of the pulse width within the limits imposed by the timing relationships shown in figures 6.5 through 6.12.

The I/O cables are comprised of twisted-pair conductors with a characteristic impedance of 75-180 ohms for the pair. The maximum length of either cable should not exceed 200 feet.

### 2.3. OUTPUT SIGNAL CHARACTERISTICS

All IOC NTDS FAST output signals meet the requirements of MIL-STD-1397(SHIPS). All differential IOC output signals are capable of both sourcing and sinking 20 milliamps from 0 to 2.4 volts. A differential voltage of from 0.5 to 5.5 volts shall define a valid logic state. The waveform of any output circuit applied to any line will have a rise and fall time of between 2 and 75 nanoseconds when terminated in an impedance of 120 ohms.

### 2.4. INPUT SIGNAL CHARACTERISTICS

All NTDS FAST IOC input circuits meet the requirements of MIL-STD-1397(SHIPS). A valid differential logic state is defined by a differential voltage of between 0.5 and 5.5 volts. The maximum steady-state current drawn from a line by an IOC differential input circuit will not exceed 2.5 milliamps for a 2.5 volt differential. Input signals which are left floating are assumed by the IOC to be negated (logic 0s). All input signals should be transmitted through twisted-pair conductors. The IOC terminates all input signals with a 130-ohm resistor in series with a 0.01-microfarad capacitor.

Control logic in the I/O subsystem must be provided to re-synchronize all control signals as appropriate or required. Re-synchronization is accomplished by sensing the control signal transition from the "negated" to the "asserted" state.

## 2.5. INPUT/OUTPUT SIGNALS

Figure 6.13 shows the IOC I/O channel input and output signals and the number of pairs required per channel. The arrows show the direction of signal transmission. The I/O cable pin numbers associated with each of the signals are found in the appendix.

## 2.6. OUTPUT DATA

The 17 output data signals are used to transmit 16-bit data words with 1 parity bit. The output data signals are controlled by the IOC and the parity of the words is program selectable.

## 2.7. OUTPUT DATA ACKNOWLEDGE

The Output Data Acknowledge (ODA) control signal is asserted by the IOC after output data is stable on the output data lines.

## 2.8. EXTERNAL FUNCTION

The External Function (EF) control signal is asserted by the IOC to inform the I/O subsystem that the data on the output data lines is a function (command) word. ODA and EF are never asserted at the same time.

## 2.9. STATUS FLAG

The status flag is a non-standard user-definable control signal present in both the input and output channels. It is asserted and negated under host program control.

## 2.10. OUTPUT DATA REQUEST

The Output Data Request (ODR) control signal is asserted by the I/O subsystem and operates in the following ways:

(1) In the normal mode, ODR is asserted when the I/O subsystem is conditioned to perform an output function and can accept a word of output data (or an external function word if the ODR buffered EF mode is in use) from the IOC. The I/O subsystem holds ODR asserted until the IOC asserts ODA or EF, as appropriate.

(2) In the intercomputer mode, ODR is asserted when the I/O subsystem has accepted the output data or function word transmitted to it from the IOC. It must then be negated within the timing restrictions shown in figures 6.6 and 6.10.

## 2.11. EXTERNAL FUNCTION REQUEST

The External Function Request (EFR) control signal is used only in the EFR buffered EF mode and is asserted by the I/O subsystem when it can accept an external function word from the IOC. EFR is held asserted until EF is asserted by the IOC.

## 2.12. CLEAR INPUT PERIPHERAL AND CLEAR OUTPUT PERIPHERAL

The Clear Input Peripheral (CLR IP) and Clear Output Peripheral (CLR OP) control signals are asserted by the IOC, and upon detection, the I/O subsystem normally performs a subsystem clear and conditions itself to receive an EF from the IOC.

## 2.13. INPUT DATA

The 17 input data signals (16 data bits plus 1 parity bit) are asserted by the I/O subsystem and are used to transmit data and status words to the IOC. The parity checked by the IOC is program selectable as is the option to ignore parity entirely.

## 2.14. INPUT ACKNOWLEDGE

The Input Acknowledge (IA) control signal is asserted by the IOC and operates in two ways:

(1) In the normal mode, the IOC asserts IA after it has accepted the data transmitted from the I/O subsystem.

(2) In the intercomputer mode, IA is asserted if the IOC can accept a data or status word from the I/O subsystem. The IOC negates IA after the word transmitted from the I/O subsystem has been accepted.

## 2.15. EXTERNAL INTERRUPT

The External Interrupt (EI) control signal is asserted by the I/O subsystem when a status word is available on the input data lines. The I/O subsystem holds the EI signal asserted until the IOC asserts IA (normal mode) or for a minimum time period (intercomputer mode) as specified in figures 6.8 and 6.12. If input is enabled, the IOC will always respond to an EI with an IA, even if the EI is negated before the response.

## 2.16. INPUT DATA REQUEST

The Input Data Request (IDR) control signal is asserted by the I/O subsystem when input data is available on the input data lines. The I/O subsystem holds the IDR signal asserted until the IOC asserts IA (normal mode) or for a minimum time period (intercomputer mode) as specified in figures 6.8 and 6.12. If input is enabled, the IOC will always respond to an IDR with an IA, even if the IDR is negated before the response.

## 2.17. EXTERNAL INTERRUPT ENABLE

The External Interrupt Enable (EIE) control signal (if required by the I/O subsystem) is asserted by the IOC under program control when it can accept an interrupt from the I/O subsystem. EIE is held asserted until the IOC asserts (normal mode) or negates (intercomputer mode) IA in response to the assertion of EI. Since EIE is negated by the hardware each time an EI is acknowledged, it must be reasserted for each interrupt.

## SECTION 3. INTERFACE SIGNAL SEQUENCES

### 3.1. OUTPUT DATA TRANSFER (See figures 6.5, 6.6, 6.9, and 6.10.)

During output data transfers, one data word is transferred to the I/O subsystem from the IOC each time ODA is asserted. There are two modes of output data transfer, normal and intercomputer. Loop-back self-tests are performed using the intercomputer mode.

The sequence of events for the normal mode is as follows:

(1) The I/O subsystem asserts ODR on the output channel.

(2) The IOC detects the assertion of ODR and if the output data FIFO buffer is not empty, places the next buffer word on the output data lines. If the buffer is empty, the IOC must load more data into it from the host memory before any further output data activity can take place.

(3) The IOC asserts ODA on the output channel.

(4) To start another data transfer, the I/O subsystem must negate the existing ODR and reassert a new one. Steps 1 through 3 are repeated each time a data word is transferred.

The sequence of events for the intercomputer mode is as follows:

(1) When the IOC output data FIFO buffer has a word ready for the I/O subsystem, it places the word on the output data lines and asserts ODA regardless of the state of ODR.

(2) The I/O subsystem detects the assertion of ODA, accepts the output data, and asserts ODR (or negates and reasserts it if it was already asserted).

(3) To start another data transfer, the IOC will negate the existing ODA and reassert a new one. Steps 1 and 2 are repeated each time a data word is transferred.

### 3.2. INPUT DATA TRANSFER (See figures 6.7, 6.8, 6.11 and 6.12.)

During input data transfers, one data word is transferred from the I/O subsystem to the IOC each time IDR is asserted by the subsystem. There are two modes of input data transfer, normal and intercomputer. Loop-back self-tests are performed using the intercomputer mode.

The sequence of events for the normal mode is as follows:

(1) The I/O subsystem places the input data on the input data lines, then asserts IDR on the input channel.

(2) The IOC detects the assertion of IDR, and if the input data FIFO buffer is not full or disabled, enters the data word into the buffer. If the buffer is full or disabled, the IOC must transfer data out of

the buffer into the host memory (if full) or enable it (if disabled) before any further input data activity can take place.

(3) The IOC asserts IA on the input channel.

(4) To start another data transfer, the I/O subsystem must negate the existing IDR and reassert a new one. Steps 1 through 3 are repeated each time a data word is transferred.

The sequence of events for the intercomputer mode is as follows:

(1) When the IOC input data FIFO buffer can accept a word, the IOC asserts IA on the input channel.

(2) The I/O subsystem detects the assertion of IA, places the input data on the input data lines, and asserts IDR on the input channel for a minimum amount of time as specified in figures 6.8 and 6.12.

(3) The IOC detects the assertion of IDR and enters the new data word into the buffer.

(4) If the buffer is not yet full or disabled, the IOC negates and reasserts IA. (The final reassertion of IA can be prevented. See the explanation of the IA SYNC and NON-FIFO bits in the mode register, section 5.8.) If the buffer is full or disabled, the IOC must transfer data out of the buffer into the host memory (if full) or enable the buffer (if disabled) before IA will be toggled.

(5) Steps 1 through 4 are repeated each time a data word is transferred.

3.3. **FORCED EXTERNAL FUNCTION TRANSFER** (See figures 6.5, 6.6, 6.9, and 6.10.)

Under host program control, one or more EFs can be asserted regardless of the state of ODR or EFR. This capability is called "forcing an external function." Forced external functions may only be transferred in the normal mode. Their attempted use in the intercomputer mode will result in transfers actually being made in the ODR buffered EF mode as described in section 3.4. Loop-back self-tests are performed using the intercomputer mode.

The sequence of events for the normal mode is as follows:

(1) The host program determines when a forced EF transfer is necessary.

(2) The IOC, under program control, places the function (command) word on the output data lines, then asserts EF on the output channel.

(3) If either ODR or IDR are asserted, the I/O subsystem normally, but not necessarily, negates them. It should be noted, however, that if the I/O subsystem does choose to negate IDR (or EI) in response to assertion of the EF, the IOC will eventually respond to these signals anyway with the assertion of IA as previously mentioned in sections 2.15 and 2.16.

(7) Mode Register. An IOC or system clear clears all bits in this register to logic zeros. The bits in the mode register may be loaded in the word or byte mode. The register bits function as follows:

(a) BIT 0 - STANDARD TIMING bit: Read/write. A logic 1 makes the IOC I/O channel timing compatible with standard Univac I/O word channel timing while a logic 0 causes NTDS FAST channel timing compatibility (figures 6.5 through 6.12).

(b) BIT 1 - INTERCOMPUTER bit: Read/write. A logic 1 configures the IOC I/O channel for transactions with the I/O channel of another computer (and the loop-back self-test mode). A logic 0 configures the IOC for transactions with a non-computer I/O subsystem such as a printer or card reader.

(c) BIT 2 - BUFFERED EF bit: Read/write. A logic 1 causes all external function words to be transmitted using the buffered EF mode. A logic 0 allows all external functions to be forced.

(d) BIT 3 - USE ODR bit: Read/write. This bit is only used if the BUFFERED EF bit contains a logic 1. A logic 1 causes the ODR control signal in the output cable to be used in buffered EF sequences while a logic 0 causes the EFR control signal to be used.

(e) BIT 4 - SEGMENTED DMA bit: Read/write. A logic 1 in the SEGMENTED DMA bit allows the IOC to obtain and release the host UNIBUS as required during DMA transfers. The procurement and release of the UNIBUS are determined by the availability of data in the buffer and the selected burst count. A logic 0 prevents the release of the UNIBUS until the entire DMA block of words has been transferred.

(f) BIT 5 - EI BLOC SYNC bit: Read/write. A logic 1 in this bit causes the input data FIFO buffer to refuse input once an EI has occurred and to remain in that state until the FIFO is empty. A logic 0 does not permit EIs to affect the FIFO.

(g) BIT 6 - NON-FIFO bit: Read/write. A logic 1 causes the input data FIFO buffer to refuse input until the host processor has actually started an IOC DMA. When the DMA completes, input is again refused. A logic 0 allows input regardless of the DMA condition.

(h) BIT 7 - IA SYNC bit: Read/write. The IA SYNC bit is used only during the combination of intercomputer and NON-FIFO mode operations. A logic 1 prevents the assertion of IA (which is connected to the ODR line of the other computer) until a DMA transfer is actually started and prevents the reassertion of IA after the final word from the other computer is accepted. The typical Univac output channel will hang if this mode is used due to the absence of the terminal assertion of IA (the computer's ODR). A logic 0 during the intercomputer mode asserts IA as described in section 3.1.

DMA PARITY ERROR bit: Read only. A logic 1 indicates that a parity error was present in one or more of the words transferred (in either direction) during the most recent DMA transfer. A logic 0 indicates that all parity was correct. This bit is cleared to a logic 0 by writing a logic 1 into the GO bit.

(n) BIT 13 -

CLEAR OUTPUT PERIPHERAL bit: Write only. Writing a logic 1 causes the CLR OP control signal in the output cable to be asserted for approximately 400 nanoseconds. Writing a logic 0 has no effect.

RESPONSE TIMEOUT ERROR bit: Read only. A logic 1 indicates that a host address requested by the IOC during the most recent DMA transfer did not respond within approximately 15 microseconds and the transfer was aborted. The DMA PARITY ERROR bit should be ignored if this bit contains a logic 1. A logic 0 indicates that all host DMA addresses responded properly. This bit is cleared to a logic 0 by writing a logic 1 into the GO bit.

(o) BIT 14 -

CLEAR IOC bit: Write only. Writing a logic 1 initializes the IOC by clearing the status register to 006000 (octal), the mode register to 000000, and the memory address, word count, and inbuf count registers to 000000. It also resets all IOC internal logic, initializes the three FIFO controllers, and clears all error conditions. Writing a logic 0 has no effect.

TRANSFER TIMEOUT ERROR bit: Read only. A logic 1 indicates that during the most recent DMA transfer, the IOC attempted to maintain exclusive control of the host UNIBUS for longer than approximately 30 milliseconds and the transfer was aborted. The DMA PARITY ERROR bit should be ignored if this bit is a logic 1. A logic 0 indicates that the transfer completed in time. This bit is cleared to a logic 0 by writing a logic 1 into the GO bit.

(p) BIT 15 -

CLEAR DMA GO bit: Write only. Writing a logic 1 clears out a pending DMA transfer (clears the DMA GO bit). Writing a logic 0 has no effect.

ERROR bit: Read only. This bit is the logical OR of the DMA PARITY ERROR, the RESPONSE TIMEOUT ERROR, and the TRANSFER TIMEOUT ERROR bits and contains a logic 1 whenever any one or more of these bits contain a logic 1. This bit may be checked first by the program to ascertain if any errors have occurred during the most recent DMA transfer.

or more status words enter the EI FIFO buffer from the I/O subsystem. Writing a logic 1 into this bit will also cause the same interrupt if the buffer already contains one or more words.

(h) BIT 7 - INTR ON OUTBUF MT bit: Read/write. A logic 1 enables the IOC to generate an OUTBUF MT interrupt to the host processor each time the output data FIFO buffer is emptied by the I/O subsystem. Setting this bit to a logic 1 will not in itself cause an interrupt if the buffer is already empty. A logic 0 inhibits the interrupt.

(i) BIT 8 - DMA DONE bit: Read/write. A logic 1 read from this bit indicates that the DMA transfer has completed (successfully or unsuccessfully). Writing a logic 0 has no effect. Writing a logic 1 clears the DMA DONE bit to a logic 0.

(j) BIT 9 -

CLEAR EIBUF bit: Write only. Writing a logic 1 clears the EI FIFO buffer control logic to the "empty" state (EIBUF not ready) and negates the EIE control signal in the input cable if asserted. Writing a logic 0 has no effect.

EIBUF READY bit: Read only. A logic 1 indicates that there is a valid status word in the external interrupt register. Reading the word from the register clears this bit to a logic 0.

(k) BIT 10 -

CLEAR OUTBUF bit: Write only. Writing a logic 1 clears the output data FIFO buffer control logic to the "empty" state but will not cause an OUTBUF MT interrupt to be generated. Writing a logic 0 has no effect.

OUTBUF MT bit: Read only. A logic 1 in this bit indicates that the output data FIFO buffer is empty while a logic 0 indicates that it contains data.

(l) BIT 11 -

CLEAR INBUF bit: Write only. Writing a logic 1 clears the input data FIFO buffer control logic to the "empty" state. Writing a logic 0 has no effect.

INBUF MT bit: Read only. A logic 1 in this bit indicates that the input data FIFO buffer is empty while a logic 0 indicates that it contains data.

(m) Bit 12 -

CLEAR INPUT PERIPHERAL bit: Write only. Writing a logic 1 causes the CLR IP control signal in the input cable to be asserted for approximately 400 nanoseconds. Writing a logic 0 has no effect.

count register to the same value. An IOC or host system clear clears this register to zero.

(5) Inbuf Count Register (read/shadow write). This register is loaded under program control simultaneously with, and with the same value as, the word count register and may not be loaded apart from it. It is decremented once each time an input data word enters the input data FIFO buffer and is used to disable the FIFO during the NON-FIFO input mode. If 4096 is loaded, reading it back will yield 0, although 4096 words will still be transferred. Loading 0 has the same effect as loading 4096. If 0 or 4096 are loaded and the NON-FIFO mode is selected, the input data FIFO will be disabled to further input. Word or byte mode writes are permitted. Upon successful completion of the transfer, its contents will be 0. An IOC or host system clear clears this register to zero. This register is intended to be read only for test purposes since its contents can change non-synchronously as input data arrives at the IOC.

(6) Status Register. An IOC or host sstem clear sets bits 10 and 11 of this register to logic ones and clears all remaining bits to logic zeros. The bits in the status register may be loaded using the word or byte mode and function as follows:

(a) BIT 0 - SET DMA GO bit: Read/write. Writing a logic 1 causes the IOC to obtain host bus mastership and perform a DMA transfer under the constraints of section 5.4. It also clears the DMA DONE and the DMA PARITY ERROR bits to a logic 0. Writing a logic 0 has no effect. Reading the bit indicates whether or not a DMA is still pending (segmented DMA mode).

(b) BIT 1 - DIRECTION bit: Read/write. A logic 1 in this bit directs DMA transfers to be from the input data FIFO buffer to the host memory while a logic 0 directs transfers from the host memory to the output data FIFO buffer.

(c) BIT 2 - EXTENDED ADDRESSING 16 BIT: READ/WRITE. This bit is an extension of the memory address register.

(d) BIT 3 - EXTENDED ADDRESSING 17 bit: Read/write. This bit is an extension of the memory address register.

(e) BIT 4 - INTR ON DMA DONE bit: A logic 1 enables the IOC to generate a DMA DONE interrupt to the host processor upon completion (successful or unsuccessful) of a DMA transfer. A logic 0 inhibits the interrupt.

(f) BIT 5 - ABORT ON DMA PE bit: Read/write. A logic 1 will cause the first parity error encountered by the IOC (in a word being DMA transferred in either direction) to terminate the transfer. A logic 0 inhibits the termination.

(g) BIT 6 - INTR ON NEW EI bit: Read/write. A logic 1 enables the IOC to generate a NEW EI interrupt to the host processor when one

to 777760 (octal) in increments of 10 (octal) words (figure 6.2). The registers are located as follows:

| Register | Address (octal) |
|---|---|
| External Function/ External Interrupt | Base Address + 0 |
| Memory Address | Base Address + 2 |
| Word Count | Base Address + 4 |
| Status | Base Address + 6 |
| Mode | Base Address + 10 |
| Inbuf Count | Base Address + 12 |
| Unused | Base Address + 14-16 |

The operation of the various registers and some of their specific bits has been described in previous sections and is consolidated here as follows:

(1) External Function Register (write only). This register occupies the same address space as the external interrupt register and is accessed by writing using the word mode. Byte mode writes are ignored but no error indication is returned to the processor. The words written to this address under program control will be transmitted to the I/O subsystem as external function (command) words in accordance with the restrictions of section 3.4.

(2) External Interrupt Register (read only). This register occupies the same address space as the external function register and is accessed by reading. Words read from this address under program control come from the EI FIFO buffer and are the status words transmitted to the IOC from the I/O subsystem via the EI signal.

(3) Memory Address Register (read/write). This register is loaded under program control with the 16 low order address bits of the host memory location at which the next DMA transfer is to begin. Word or byte mode writes are permitted. Upon successful completion of a transfer, this register will contain the address following the address to/from which the last transfer was made. Bit 0 will always read back as a logic 0 since DMA transfers occur on word boundaries. An IOC or host system clear clears this register to zero.

(4) Word Count Register (read/write). This register is loaded under program control with the number of words to be transferred during the next DMA transfer (0 to 4096 words). If 4096 is loaded, reading it back will yield 0, although 4096 words will still be transferred. Loading 0 has the same effect as loading 4096. Word or byte mode writes are permitted. Upon successful completion of the transfer, its contents will be 0. Loading this register also loads the inbuf

address in the IOC. Forced external functions are not permitted in the inter-computer mode.

### 5.6. ODR BUFFERED EXTERNAL FUNCTIONS

The ODR buffered EF mode is set up by writing a logic 1 into both the BUFFERED EF and the USE ODR bits of the mode register. The EF words are then written to the EF register address in the IOC. The first EF word written after entering this mode will be transmitted to the I/O subsystem regardless of the state of ODR. Subsequent EFs will be transmitted only if ODR is asserted prior to the time each transmission is attempted and is negated after each transmission has occurred. If these conditions are not met, an EF FAIL interrupt is instead returned to the host processor indicating that the processor must retransmit the EF.

It is important to note that after the first EF word of this mode has been sent, no more output data can be transmitted using the ODR-ODA sequence until the mode is exited by having the processor clear the BUFFERED EF bit to a logic 0. This is done to ensure that output data will not be sent to an I/O subsystem which has asserted its ODR in response to the first EF and cannot actually accept output data.

### 5.7. EFR BUFFERED EXTERNAL FUNCTIONS

The EFR buffered EF mode is set up by writing a logic 1 into the BUFFERED EF bit and a logic 0 into the USE ODR bit of the mode register. The EF words are then written to the EF register address in the IOC. EFs will actually be transmitted only if EFR is asserted at the time the transmission is attempted. If a transmission is attempted but EFR is negated, an EF FAIL interrupt is instead returned to the host processor indicating that the processor must retransmit the EF.

Output data transfer using the ODR-ODA sequence can continue on an arbitrary interleaved basis during EFR buffered EF transfers and it is not necessary to exit this mode since it is passive to all other transfers.

### 5.8. IOC REGISTERS, ADDRESSES, AND BIT DESCRIPTIONS (See figure 6.15.)

The host IOC occupies 10 (octal) consecutive words of device address space and contains 6 program addressable registers. The remaining two words are unused and writing to or reading them will not affect the IOC. Each of the registers is located at a fixed offset from a starting base address. This base address is jumper selectable on the IOC card and may extend from 000000

of the final word of the Univac output buffer, to terminate the buffer and cause a Univac monitor interrupt. If the final ODR is not sent, the Univac output channel will hang.

This method, however, could cause problems for an intelligent peripheral. Since it is forced to assert ODR even though it doesn't want more data, the peripheral must be ready to accept more data anyway and hold it until it can use it. The IOC, which can be considered to be an intelligent peripheral to the Univac computer can buffer and hold the extra word if it is transmitted. It is also capable, however, of not asserting the terminal ODR if the IA SYNC mode bit is set. (The IOC IA signal is the Univac ODR signal in the intercomputer mode.) In addition, the first ODR will not be asserted to the Univac computer until the host processor actually starts its input data FIFO DMA transfer. This permits the IOC to request data only when needed but it must be assured that the other computer will allow this type of operation (such as two IOCs connected to form an intercomputer channel). It should be noted, however, that since the assertion of ODR is dependent upon the state of the DMA transfer, ODR buffered EFs will not work in this mode.

If, during a DMA transfer, a location in the host memory should fail to respond to the access request of the IOC within approximately 15 microseconds, the transfer is aborted and the RESPONSE TIMEOUT ERROR bit, the ERROR bit, and the DMA DONE bit in the status register are all set to a logic 1.

If the NO PARITY bit in the mode register and the ABORT ON DMA PE bit in the status register both contain a logic 0 at the start of the transfer, and if during the transfer a parity error in one of the words being transferred is detected by the IOC, the DMA PARITY ERROR bit and the ERROR bit in the status register are set to a logic 1 and the transfer continues to completion. However, if the ABORT ON DMA PE bit contains a logic 1 and a parity error is detected, the transfer will be aborted and the DMA PARITY ERROR bit, the ERROR bit, and the DMA DONE bit in the status register will get set to a logic 1. If the NO PARITY bit is instead set to a logic 1 in the previous discussion, only data transfers from the host memory into the IOC output data FIFO buffer will be checked for parity. Parity will be ignored completely on transfers into the host from the IOC input data FIFO buffer and EI FIFO buffer.

The host processor may determine the completion of a DMA transfer by either polling the DMA DONE bit or by setting the INTR ON DMA DONE bit in the status register to a logic 1. Setting this bit allows the IOC to generate a DMA Done interrupt to the processor whenever any event sets the DMA DONE bit to a logic 1. The processor is thereby informed that the transfer is complete. The status register, however, must be read by the processor to determine if any errors have occurred during the transfer.

### 5.5. FORCED EXTERNAL FUNCTIONS

In the normal mode, a forced EF may be sent to an I/O subsystem at any time without regard for the subsystem's ability to accept it. This is done by first assuring that the BUFFERED EF bit in the mode register is cleared to a logic 0 and then under program control writing the EF word to the EF register

be assured before the transfer is started that the input data FIFO buffer has at least as many words in it or that the output data FIFO buffer has at least enough space in it to complete the transfer.

Special DMA Mode Options

Three input mode bits in the mode register allow variations in the operation of input data transfers. These are the EI BLOCK SYNC, the NON-FIFO, and the IA SYNC bits. The three modes are described here as follows:

1. EI Block Sync Mode. This mode allows the input data FIFO to become disabled (refuse to accept any more data) when an EI is received and to remain that way until it goes empty, at which time it is re-enabled. If the FIFO is already empty when the EI is received, it remains enabled. If the segmented mode is being used, the GO condition (DMA pending) will be terminated as soon as the FIFO empties even if the DMA word counter has not reached 0. To use it in this fashion, the word counter should be loaded with some large value. When the GO condition is later terminated, the number of words actually transferred will be the difference between the initial value loaded into the word counter and its current value.

   The EI block sync mode is useful when using the IOC with peripherals which indicate the end of a block of data by sending an EI and then immediately have another block ready. Since EIs and input data are stored in separate FIFOs, lack of this mode would possibly cause confusion as to where a given block ended and where the next one began.

2. NON-FIFO Mode. In some instances it may be desirable to prevent any data from entering the input data FIFO until an IOC DMA transfer is actually started, and then to allow input to continue only for a predetermined number of words. Such an instance would be a device which supplies real time data which is continually updated. It would defeat the purpose of the data if the input data FIFO were allowed to arbitrarily fill because the data would just sit there getting old. Thus, the NON-FIFO mode will only accept data when the DMA transfer is actually started. When the number of words loaded into the word counter have been transferred, the FIFO is disabled. This mode also permits the transfer of blocks of definite length without requiring an EI from the peripheral to terminate the block.

3. IA Sync Mode. This mode has an effect only in conjunction with the simultaneous operation of the NON-FIFO mode and the intercomputer mode. As a general rule, Univac output word channels require a peripheral device to negate and reassert ODR after each word is transmitted via the Univac ODA signal, even if the peripheral has received all the words it wants. In other words, the peripheral is not allowed to count words and stop requesting when it has enough. The Univac computer actually uses the reassertion of ODR to tell it that the previous data has been accepted by the peripheral and in the case

time the IOC acquires the UNIBUS. Larger burst counts increase the possibility of the host computer generating a UNIBUS possession timeout error while smaller counts require more bus arbitration overhead.

Whatever the DMA transfer mode, if the IOC tries to maintain exclusive control of the host UNIBUS for longer than approximately 30 milliseconds, a transfer timeout will occur. This will cause the transfer to be aborted and the TRANSFER TIMEOUT ERROR bit, the ERROR bit, and the DMA DONE bit in the status register to get set to a logic 1.

**Segmented Mode DMA**

When the processor instructs the IOC to start a DMA transfer from the input data FIFO buffer into the host memory using the segmented DMA mode, the IOC does not actually obtain control of the host UNIBUS unless there is data in the buffer. When UNIBUS control is obtained, DMA transfers will occur until any one of three conditions are met. These conditions are as follows:

1. The buffer going empty, or
2. A complete burst being transferred, or
3. The total number of words specified in the word count register being transferred.

Upon detection of one or more of these conditions, the IOC releases its control of the UNIBUS. If the release occurred due to condition 1 only or conditions 1 and 2 simultaneously, the IOC re-requests UNIBUS control when it determines that the buffer has received more data. If the release was due to condition 2 only, the IOC immediately re-requests UNIBUS control. This transferring of "bursts of segments" of the required DMA block continues as long as is required to meet condition 3.

Segmented DMA transfers to the output data FIFO operate similarly except that condition 1 becomes "the buffer going full." When release due to this condition occurs, the UNIBUS will not be re-requested until the buffer has been emptied to the "half-full" point by the peripheral device.

Any remaining DMA transfers pending while in the segmented DMA mode may be canceled at any time under program control by writing a logic 1 to the CLR DMA GO bit in the status register. This termination will set the DMA DONE bit and generate a DMA DONE interrupt, if enabled. A transfer timeout can occur only if any single "segment" does not complete within approximately 30 milliseconds. The segmented DMA mode should be used to ensure minimal UNIBUS tie up when there is the possibility that the required number of words are not actually present in the input data FIFO buffer at the time the transfer is instructed to start.

**Non-Segmented Mode DMA**

As soon as the processor instructs the IOC to start any DMA transfer using the non-segmented mode, the IOC immediately obtains control of the host UNIBUS regardless of the condition of the input or output data FIFO buffers. It does not relinquish this control until the required number of words have been transferred or until a transfer timeout occurs. The burst count is internally set to "total transfer." This mode is the most efficient if it can

negated and reasserted) until the buffer has room to accept the word or is re-enabled. When the word is finally entered, IA will be asserted (or negated and reasserted) even if IDR has been negated. The I/O subsystem will, thus, be able to operate at its highest rate if it does not assert IDR until it has determined that the input data buffer has room for a new word.

The contents of the input data FIFO buffer cannot be read under program control but rather are transferred into the host memory under the control of the IOC using the Direct Memory Access (DMA) Mode. The IOC may determine if the buffer is empty by polling the INBUF MT bit in the status register. This bit will contain a logic 1 whenever the buffer is empty.

## 5.3. OUTPUT DATA

All data words transmitted to the I/O subsystem from the IOC using an ODA come from a 1025 word FIFO buffer which must be loaded from the host memory by the IOC. The output data FIFO buffer cannot be written into under program control but rather is loaded from the host memory under IOC control using the DMA mode. If the I/O subsystem asserts ODR when the buffer is empty, ODA will not be asserted until the buffer has a word to transmit. The I/O subsystem will, thus, operate at its highest rate if it does not assert ODR until it has determined that the buffer actually contains sufficient data to complete the transfer.

The host processor may determine if the output data FIFO buffer is empty in two ways:

(1) It may poll the OUTBUF MT bit in the status register. This bit will contain a logic 1 whenever the buffer is empty.

(2) If the processor sets the INTR ON OUTBUF MT bit in the status register to a logic 1, an OUTBUF MT interrupt will be sent to the processor by the IOC the next time the buffer goes empty unless it goes empty during a DMA transfer into it. In that case, the interrupt will be generated when the DMA transfer is completed if the buffer is still empty, or will be generated as soon as it goes empty if it is not. Setting the INTR ON OUTBUF MT bit with the buffer empty will not generate an interrupt.

## 5.4. GENERAL DMA TRANSFER CONSIDERATIONS

Before starting a DMA transfer, the host processor must load the IOC word count register with the number of words to be transferred, the IOC memory address register with the starting host memory location for the transfer, and the IOC status and mode registers with the appropriate control bits. Loading the IOC word count register automatically loads the IOC Inbuf count register simultaneously to the same value. There are are two program selectable DMA modes available, segmented and non-segmented. The desired mode is determined by the SEGMENTED DMA bit in the mode register.

If the segmented DMA mode is used, the burst count must be selected using the burst count selection jumper on the component side of the IOC card (figure 6.3). Either 1, 2, 4, 8, or total word bursts are available. The number selected determines the maximum number of words that will be transferred each

## SECTION 5. IOC PROGRAMMING

### 5.1. EXTERNAL INTERRUPTS

All status words transmitted to the IOC from the I/O subsystem using an EI initially enter a 1025 word FIFO buffer if the buffer is not full. IA is then asserted by the IOC (or negated and reasserted if in the intercomputer mode) indicating that the word was accepted. If, however, the buffer is full, the word will not be entered nor will IA be asserted (or negated and reasserted) until the buffer has room to accept the word. When the word is finally entered, IA will be asserted (or negated and reasserted) even if EI has been negated. The I/O subsystem will, thus, be able to operate at its highest rate if it does not assert EI until it has determined that the EI buffer has room for a new word.

When operating in the intercomputer mode with the other computer using forced external functions, the other computer is responsible for not overrunning the IOC EI FIFO buffer. The IOC cannot detect such an overrun.

The host processor may determine if an EI status word from the I/O subsystem has been accepted in two ways:

(1) Any time the EI FIFO buffer has one or more words in it and the oldest word is ready to be read under program control, the EIBUF READY bit in the status register contains a logic 1. When the host processor reads the word, the bit gets cleared to a logic 0, the word is popped out of the buffer, and within 700ns, the next buffer word becomes available for reading causing the bit to again become a logic 1. The host processor may thus poll the EIBUF READY bit to ascertain the availability of EI status words.

(2) If the processor sets the INTR ON NEW EI bit in the status register to a logic 1, the IOC will immediately generate a NEW EI interrupt to the processor if the EI FIFO buffer contains one or more words. If the buffer is empty, the interrupt will be generated when the first word is received. Since NEW EI interrupts are not queued, only one will be generated for any number of EIs arriving from the I/O subsystem prior to and during the servicing of that NEW EI interrupt. For another one to be generated, either another EI must be received after the NEW EI interrupt has been serviced or the INTR ON NEW EI bit must be negated and re-asserted with one or more words already in the EI FIFO buffer.

External interrupts are best suited for sending short messages and commands pertaining to setting up parameters for Direct Memory Access (DMA) transfers, etc.

### 5.2. INPUT DATA

All data words transmitted to the IOC from the I/O subsystem using an IDR initially enter a 1025 word FIFO buffer if the buffer is not full or disabled. IA is then asserted by the IOC (or negated and reasserted if in the intercomputer mode) indicating that the word was accepted. If, however, the buffer is full or disabled, the word will not be entered nor will IA be asserted (or

## SECTION 4. IOC I/O CHANNEL CONNECTIONS

### 4.1. NORMAL MODE CONNECTION

The normal mode is used when connecting the IOC I/O channel to a non-computer I/O subsystem such as a printer or card reader. In this mode, signals from the IOC (figure 6.13) connect to the corresponding signals in the I/O subsystem.

### 4.2. INTERCOMPUTER MODE CONNECTION

The intercomputer mode is used when the IOC is connected to the I/O channel of another computer. In this mode, the I/O cables are connected in an input-to-output fashion as shown in figure 6.14. When connected in this manner and programmed for the intercomputer mode, the IOC holds the ODR input to the other computer's output channel asserted so that the other computer can transmit output data as soon as it becomes available. No changes to the other computer are required.

### 4.3. LOOP-BACK SELF-TEST MODE CONNECTION

The loop-back self-test mode is the same as the intercomputer mode except that the IOC input channel is connected to its output channel. Section 4.2 is applicable otherwise. I/O connections for this mode are shown in figure 6.15.

The sequence of events for the normal mode is as follows:

(1) The I/O subsystem detects the assertion of EIE from the IOC (if EIE is being used), places the status word on the input data lines, and asserts EI on the input channel.

(2) The IOC detects the assertion of EI and if the EI FIFO buffer is not full, enters the status word into the buffer. If the buffer is full, the IOC must transfer status word(s) out of the buffer into the host memory before any further EI activity can take place.

(3) The IOC asserts IA on the input channel.

(4) To start another data transfer, the I/O subsystem must negate the existing EI and reassert a new one. Steps 1 through 3 are repeated each time a status word is transferred.

The sequence of events for the intercomputer mode is as follows:

(1) When the IOC EI FIFO buffer can accept a word, the IOC asserts IA (and EIE if used) on the input channel.

(2) The I/O subsystem detects the assertion of IA or EIE, places the status word on the input data lines, and asserts EI on the input channel for a minimum amount of time as specified in figures 6.8 and 6.12.

(3) The IOC detects the assertion of EI and enters the new status word into the buffer.

(4) If the buffer is not yet full, the IOC negates IA and EIE and reasserts IA (and under program control EIE). If the buffer is full, the IOC must transfer data out of the buffer into the host memory before IA will be reasserted.

(5) Steps 1 through 4 are repeated each time a status word is transferred.

(4) The I/O subsystem may respond to the forced EF by asserting its ODR, IDR, or EI signals (depending upon its condition).

(5) To start another transfer, the IOC must negate the existing EF and reassert a new one. Steps 1 through 4 are repeated each time a function word is transferred.

### 3.4. BUFFERED EXTERNAL FUNCTION TRANSFER (See figures 6.5 and 6.9.)

The host can set up pseudo-buffered external functions on the IOC output channel. They are buffered only in the sense that a request-acknowledge sequence is required for each function (command) word transferred. There is no actual buffer since the words will be transferred one at a time by the host program. There are two modes of buffered external function transfer, ODR buffered EFs and EFR buffered EFs.

The sequence of events for ODR buffered EFs is as follows:

(1) This mode is used with Univac 1100 series I/O channels and I/O peripherals. In this mode, the first EF is forced as described in section 3.3. However, successive EFs require the assertion of ODR from the I/O subsystem before EF can be asserted.

(2) The signal sequence relationship between EF and ODR during the successive EFs is the same as the relationship between ODA and ODR respectively during output data transfers.

(3) In this mode, once the transfer of the first function word of the pseudo-buffer is made, no output data words will be transferred until the ODR buffered EF mode has been terminated by the host program.

The sequence of events for EFR buffered EFs is as follows:

(1) This mode is used with NTDS I/O channels and I/O peripherals. In this mode, no EF will be asserted until EFR has been asserted. The signal sequence relationship between EF and EFR is the same as the relationship between ODA and ODR respectively during output data transfers.

(2) In this mode, output data and EF transfers may be arbitrarily interleaved since the EFR buffered EF mode does not lock out the output data FIFO buffer.

### 3.5. EXTERNAL INTERRUPT TRANSFER (See figures 6.7, 6.8, 6.11, and 6.12.)

External Interrupt (EI) is asserted by an I/O subsystem when the subsystem must interrupt the host and has a status word to present to the IOC.

There are two modes of EI transfer, normal and intercomputer. Loop-back self-tests are performed using the intercomputer mode.

(i) BIT 8 - NO PARITY bit: Read/write. A logic 1 disables the checking of parity on all transfers into the host from the IOC input data FIFO buffer and EI FIFO buffer. A logic 0 enables parity checking. Parity is always checked on data coming from the host memory into the IOC output data FIFO buffer and always generated with all words transferred into the IOC output data FIFO buffer and the external function register from the host regardless of the state of this bit.

(j) BIT 9 - ODD PARITY bit: Read/write. A logic 1 causes odd parity to be appended to all words transferred into the IOC output data FIFO buffer and the external function register from the host regardless of the state of the NO PARITY bit. It also causes each word transferred from the IOC input data FIFO buffer and the EI FIFO buffer to be checked for odd parity, within the restrictions of the NO PARITY bit. A logic 0 similarly enables even parity.

(k) BIT 10 - ENABLE OUTPUT bit: Read/write. This bit must contain a logic 1 before any output transaction with the I/O subsystem can take place. A logic 0 prevents any transactions and immediately terminates all ongoing transactions by negating ODA and EF if asserted. An ODR which remains asserted when this bit gets asserted will be honored.

(l) BIT 11 - ENABLE INPUT bit: Read/write. This bit must contain a logic 1 before any input transaction with the I/O subsystem can take place. A logic 0 prevents any transactions and immediately terminates all ongoing transactions by negating IA and EIE if asserted. An EI or IDR which remains asserted when this bit is asserted will be honored.

(m) BIT 12 -

EIE ENABLE bit: Write only. Writing a logic 1 asserts the EIE control signal in the input channel cable while writing a logic 0 negates the signal.

EIE bit: Read only. This bit reflects the state of the EIE control signal in the input cable. A logic 1 implies assertion. The EIE control signal is automatically negated each time the IOC asserts IA in response to the assertion of EI by the I/O subsystem.

(n) BIT 13 - STATUS FLAG bit: Read/write. A logic 1 in this bit sets the status flag signals in the I/O channel cables to the asserted state while a logic 0 negates them.

(o) BIT 14 - UNUSED - Reads as written.

(p) BIT 15 - UNUSED - Reads as written.

## 5.9. IOC/UNIBUS INTERRUPTS AND VECTORS

The IOC can generate up to four different types of interrupts to the host processor if the appropriate status register bits have been set up. All interrupts will occur at the same priority level which is jumper selectable on the component side of the IOC card (figure 6.3).

The floating vector produced by each interrupt occurs at a fixed offset from a starting base vector and occupies two words of vector space. The base vector is jumper selectable on the component side of the IOC card (figure 6.2) and may extend from 000000 to 000760 (octal) in increments of 10 (octal) words. The vectors are located as follows:

| Interrupt | Vector (octal) |
|---|---|
| NEW EI | Base Vector + 0 |
| DMA DONE | Base Vector + 4 |
| OUTBUF MT | Base Vector + 10 |
| EF FAIL | Base Vector + 14 |

The operation of the various interrupts has been explained in previous sections and is consolidated here as follows:

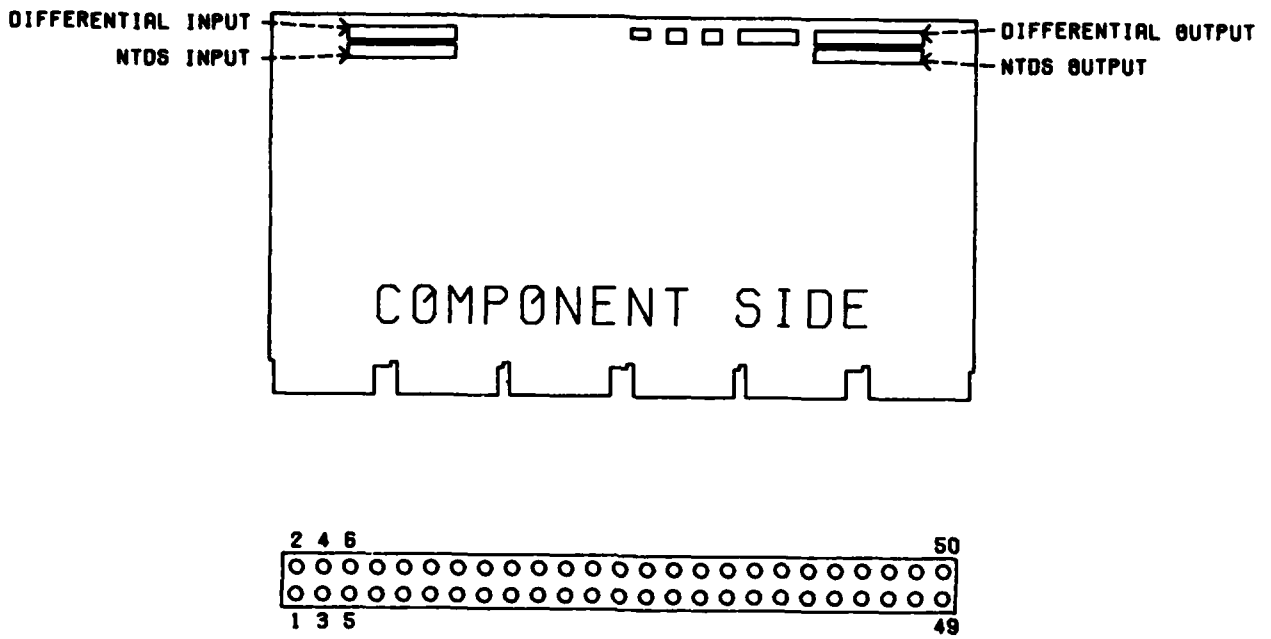
(1) New EI Interrupt. The generation of this interrupt informs the processor that a new status word has just entered the EI FIFO buffer or that the buffer already contains one or more status words.

(2) DMA Done Interrupt. This interrupt is used during host/IOC DMA transfers. The generation of this interrupt informs the processor that the current DMA transfer has completed, either successfully or with error(s).

(3) OUTBUF MT Interrupt. The generation of this interrupt informs the processor that the output data FIFO buffer has just been emptied by the I/O subsystem.

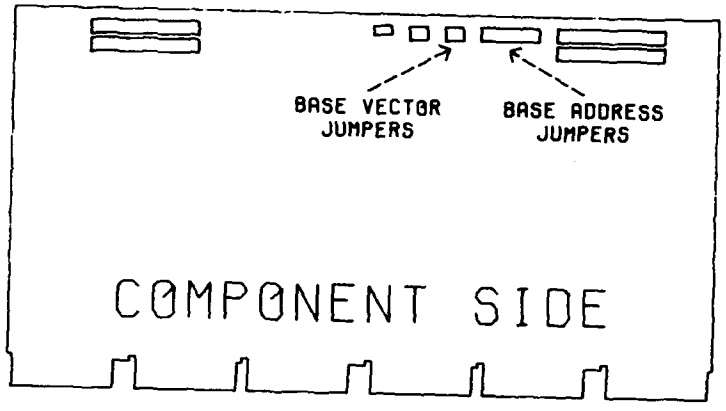
(4) EF FAIL Interrupt. This interrupt is used during buffered external function transfers. The generation of this interrupt informs the processor that the external function (command) word which it just attempted to transmit to the I/O subsystem was not actually transmitted due to the negation of ODR or EFR when the transfer was attempted.

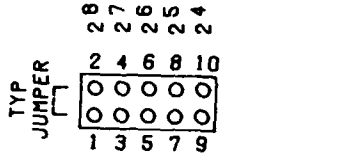
# SECTION 6. IOC FIGURES



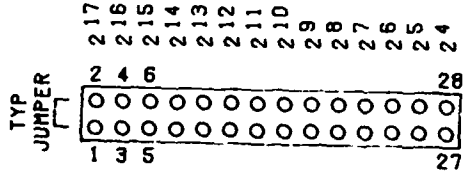

TYPICAL PIN NUMBERING FOR ALL 4 I/O CONNECTORS
(COMPONENT SIDE VIEW)

Figure 6-1. I/O connectors (I/O channel connector configuration).




BASE VECTOR JUMPERS
(COMPONENT SIDE VIEW)
JUMPER OUT = 1 JUMPER IN = 0




BASE ADDRESS JUMPERS
(COMPONENT SIDE VIEW)
JUMPER OUT = 1 JUMPER IN = 0

**Figure 6. 2. Jumper configuration (base interrupt vector and base address selection).**

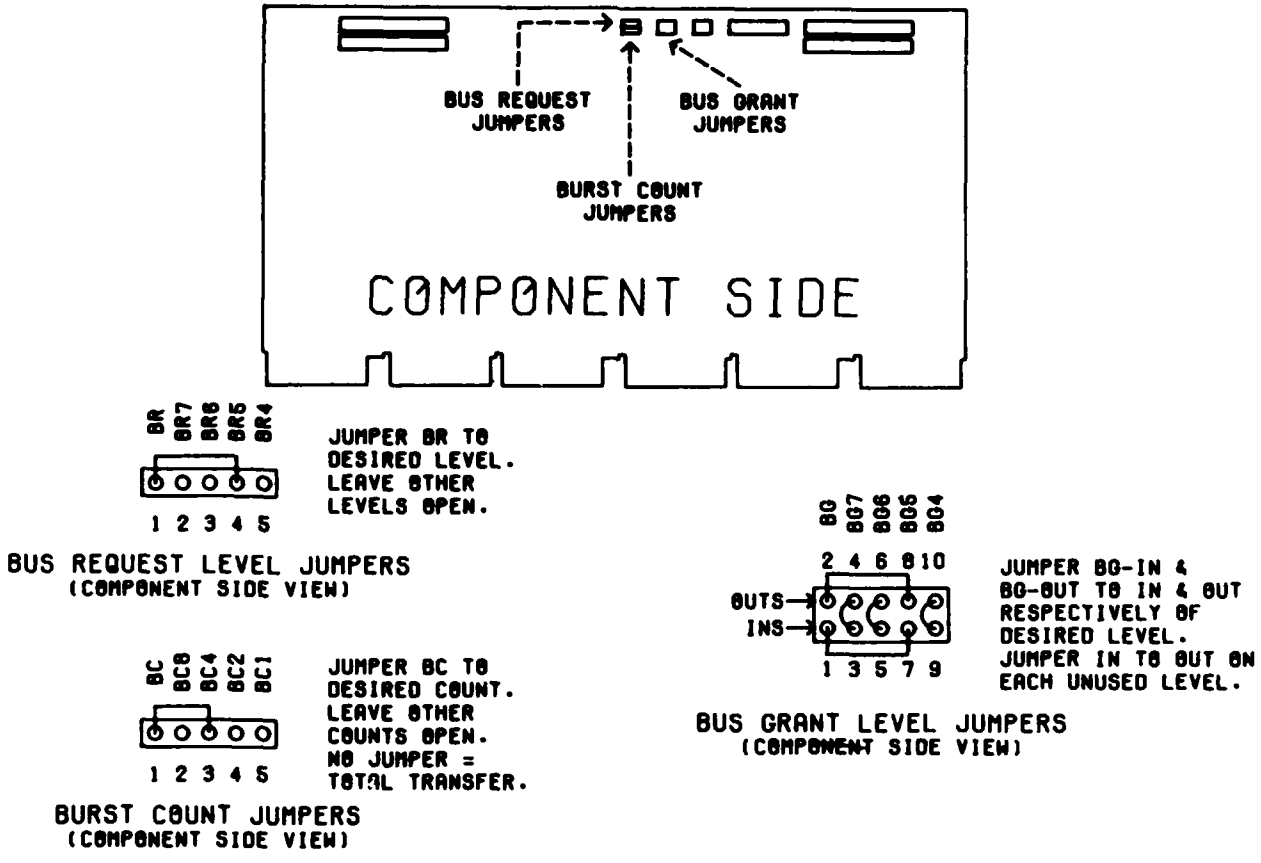



Figure 6.3. Jumper configuration (burst count and bus request/grant priority level selection).

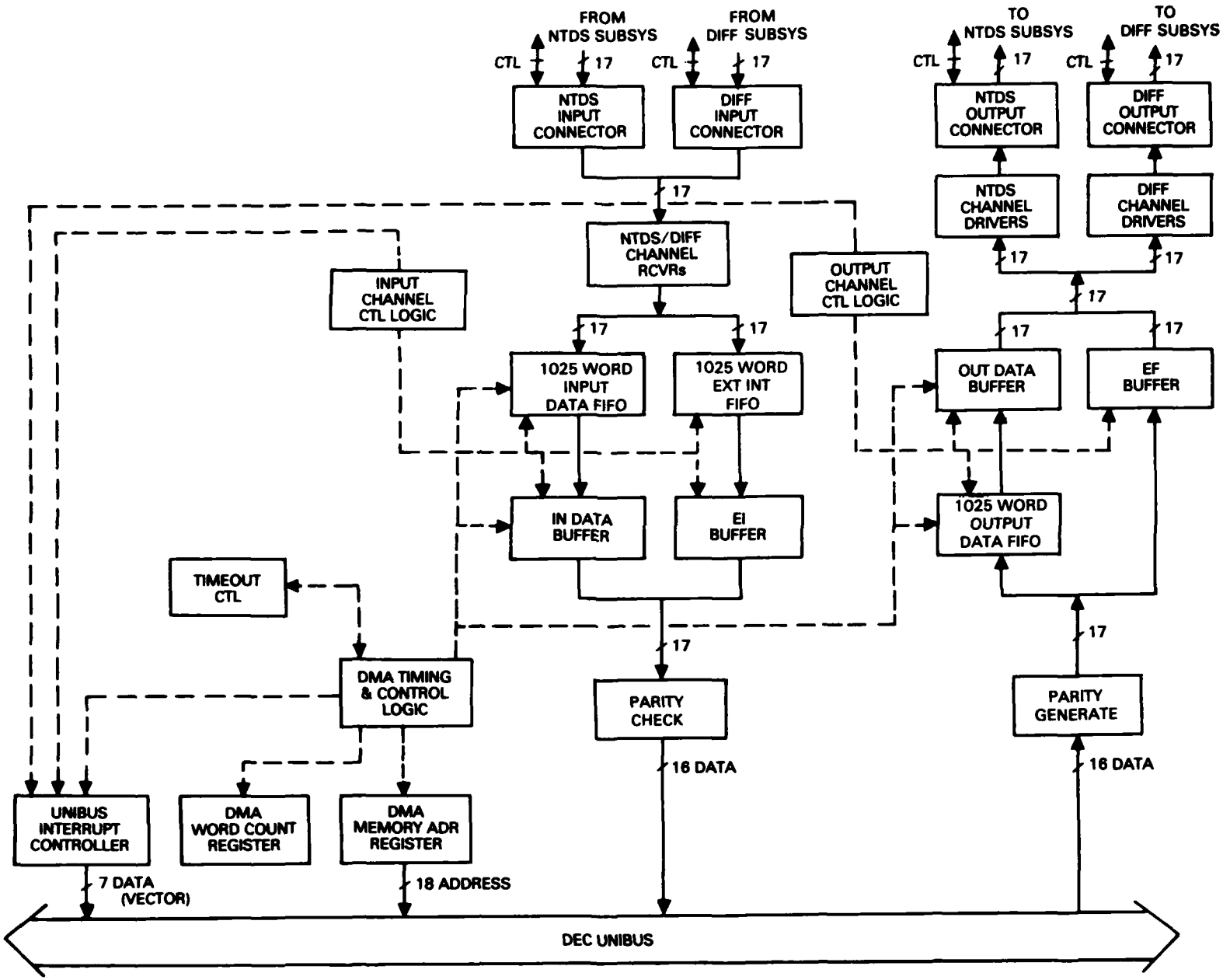
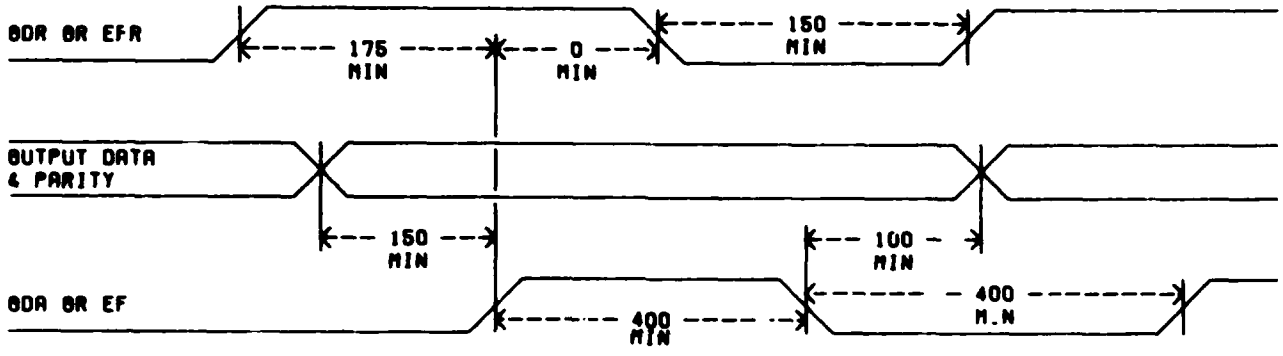


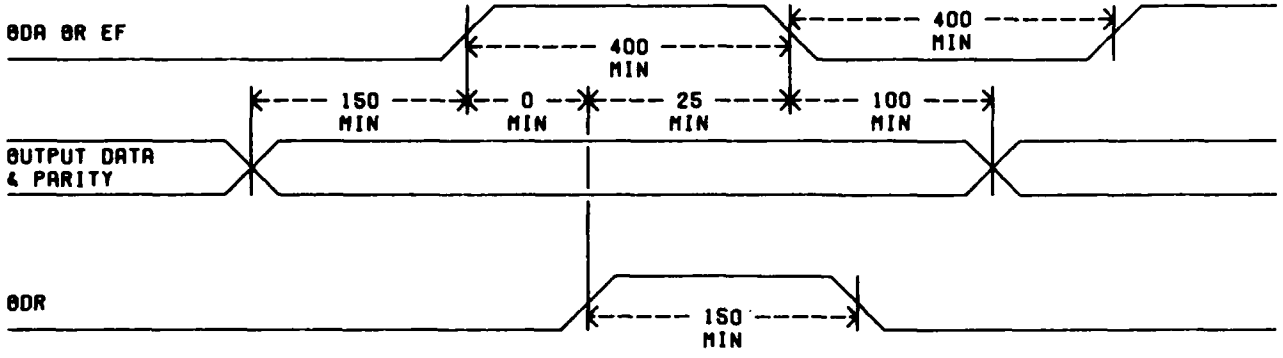

Figure 6.4. IOC functional block diagram.




NOTES:

1. ALL TIMES ARE IN NANOSECONDS.
2. HIGH = ASSERTED

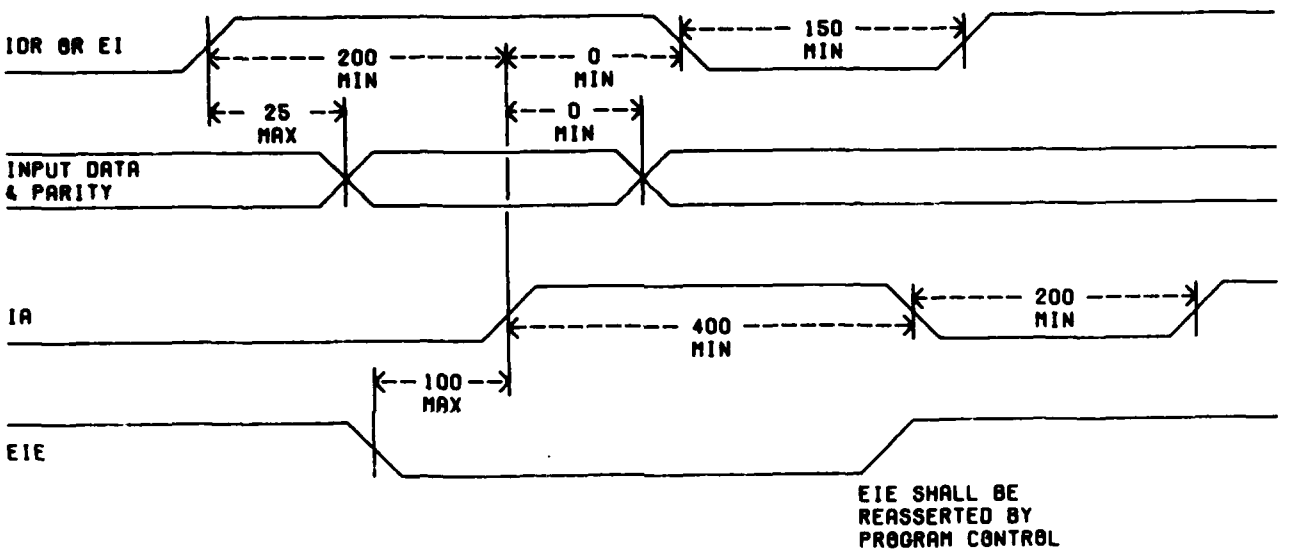
Figure 6-5. Output channel standard timing (normal mode).




NOTES:

1. ALL TIMES ARE IN NANOSECONDS.
2. HIGH = ASSERTED

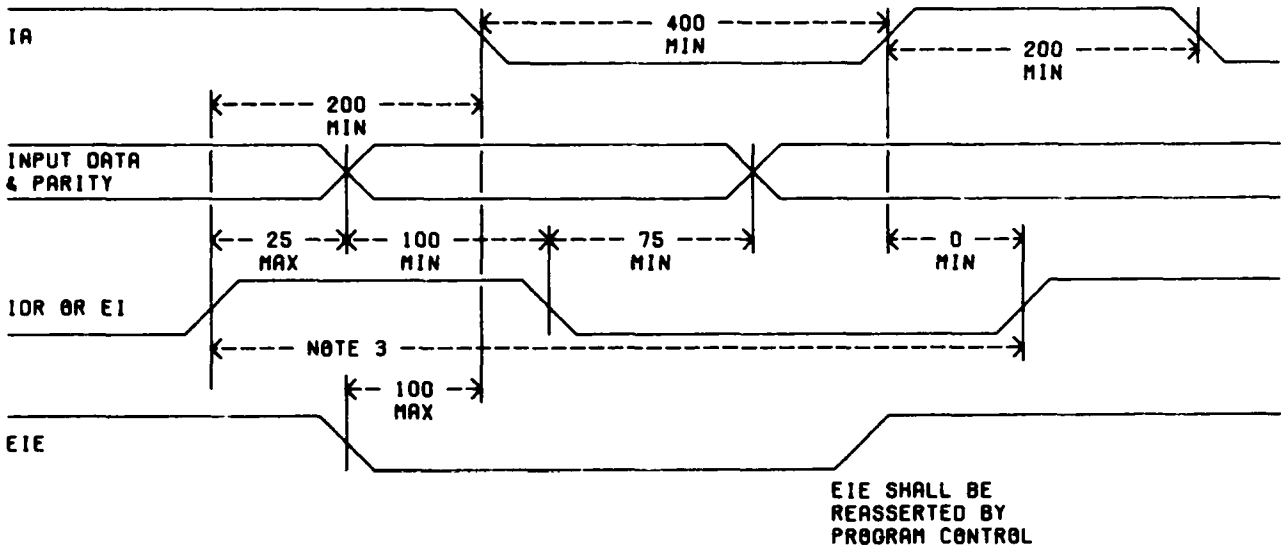
Figure 6.6. Output channel standard timing (intercomputer and loop-back self-test modes).




NOTES:

1. ALL TIMES ARE IN NANOSECONDS.
2. HIGH = ASSERTED

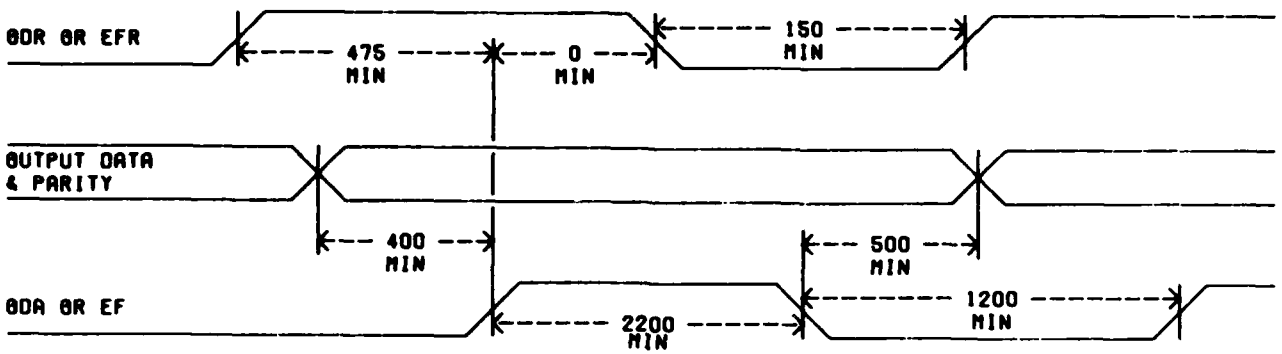
Figure 6.7. Input channel standard timing (normal mode).




NOTES:

1. ALL TIMES ARE IN NANOSECONDS.
2. HIGH = ASSERTED
3. EI MAY BE REASSERTED AFTER 1200 NANOSECONDS MINIMUM REGARDLESS OF THE STATE OF IA IF THE OTHER COMPUTER IS SENDING FORCED EXTERNAL FUNCTIONS.

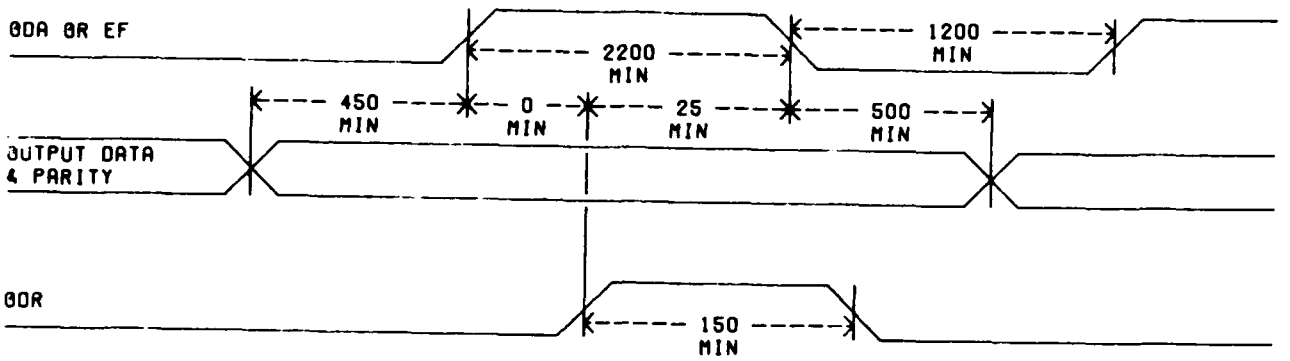
Figure 6.8. Input channel standard timing (intercomputer and loop-back self-test modes).




NOTES:

1. ALL TIMES ARE IN NANOSECONDS.
2. HIGH = ASSERTED

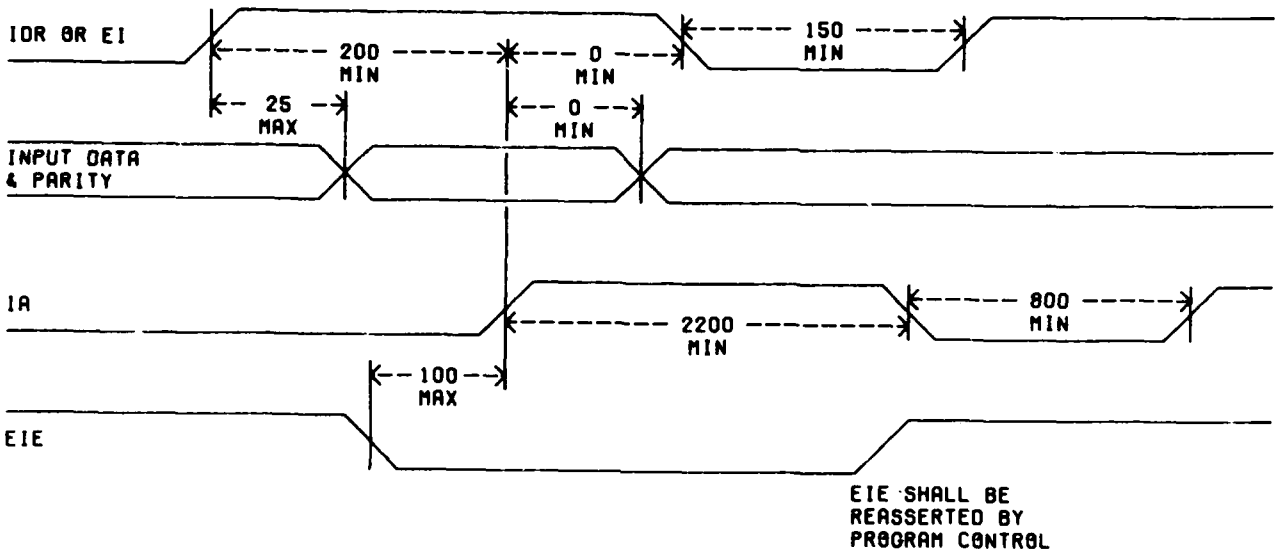
Figure 6.9. Output channel NTDS compatible timing (normal mode).




NOTES:

1. ALL TIMES ARE IN NANOSECONDS.
2. HIGH = ASSERTED

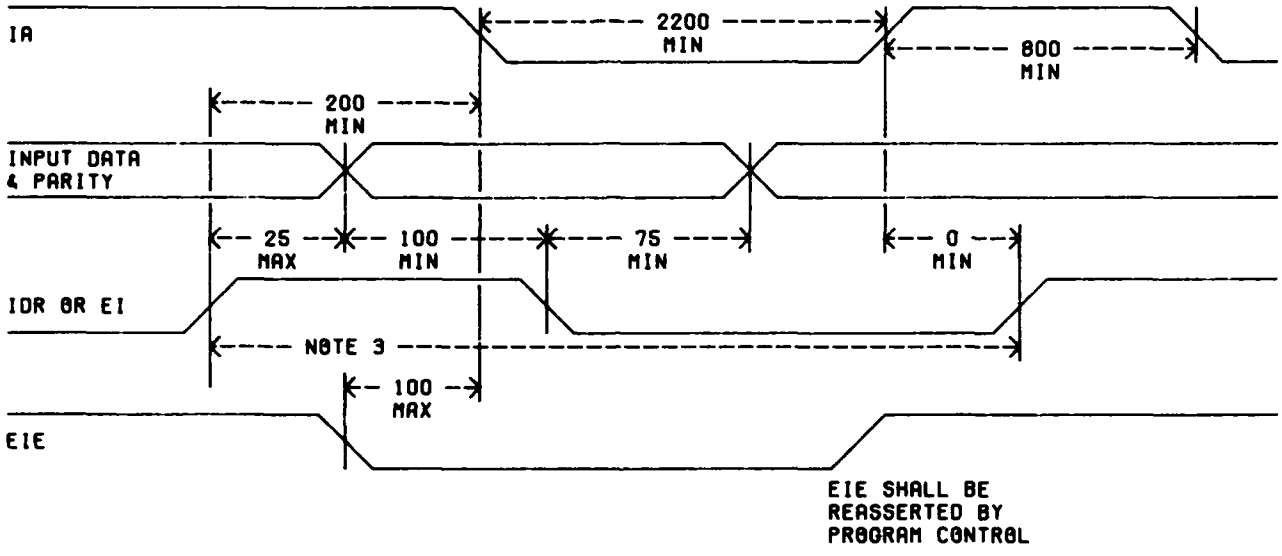
Figure 6.10. Output channel NTDS compatible timing (intercomputer and loop-back self-test modes).




NOTES:

1. ALL TIMES ARE IN NANOSECONDS.
2. HIGH = ASSERTED

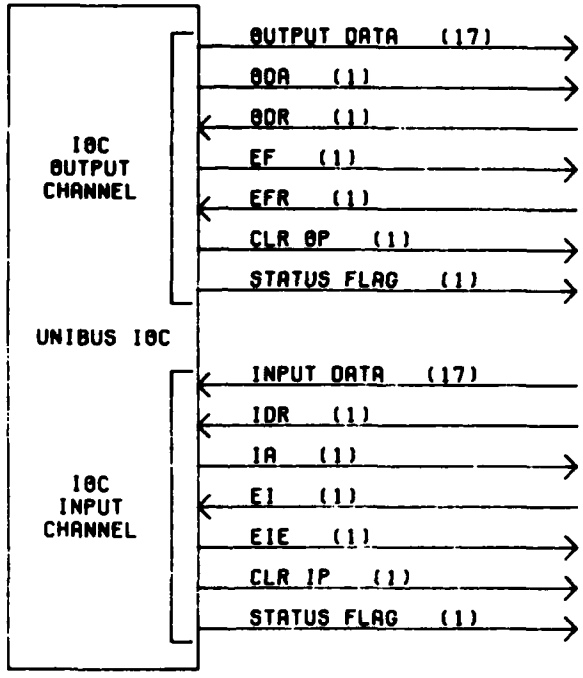
Figure 6-11. Input channel NTDS compatible timing (normal mode).




NOTES:

1. ALL TIMES ARE IN NANOSECONDS.
2. HIGH = ASSERTED
3. EI MAY BE REASSERTED AFTER 4000 NANOSECONDS MINIMUM REGARDLESS OF THE STATE OF IA IF THE OTHER COMPUTER IS SENDING FORCED EXTERNAL FUNCTIONS.

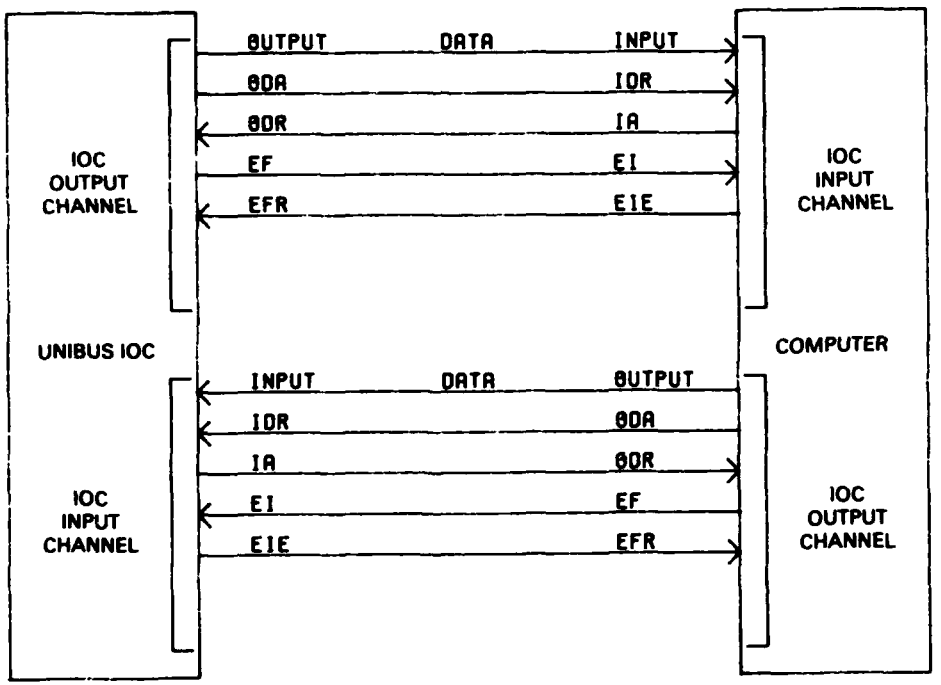
Figure 6.12. Input channel NTDS compatible timing (intercomputer and loop-back self-test modes).




NOTES:

1. THE PARITY BIT IS INCLUDED IN THE DATA.
2. THE NUMBERS IN PARENTHESES ARE THE NUMBER OF TWISTED PAIRS REQUIRED.

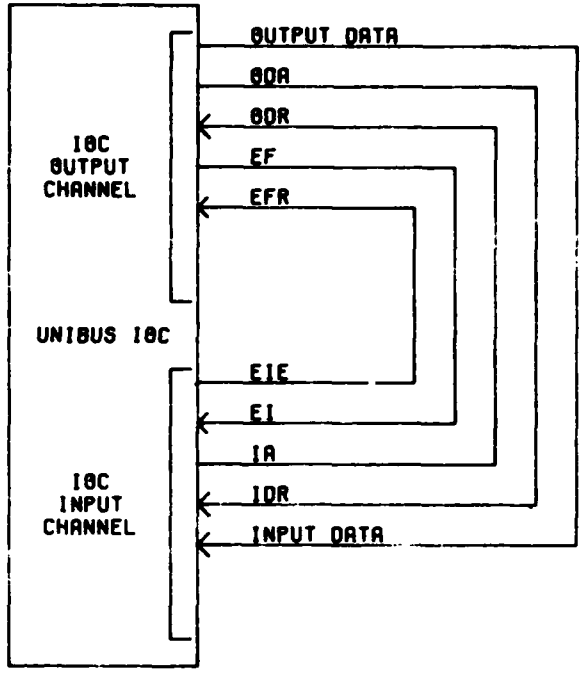
Figure 6.13. I/O channel signals.




NOTES:

1. THE PARITY BIT IS INCLUDED IN THE DATA.
2. SOME COMPUTERS DO NOT HAVE EFR OR EIE.

Figure 6.14. I/O channel intercomputer mode connections.




NOTES:

1. THE PARITY BIT IS INCLUDED IN THE DATA.

Figure 6.15. I/O channel loop-back self-test mode connections.

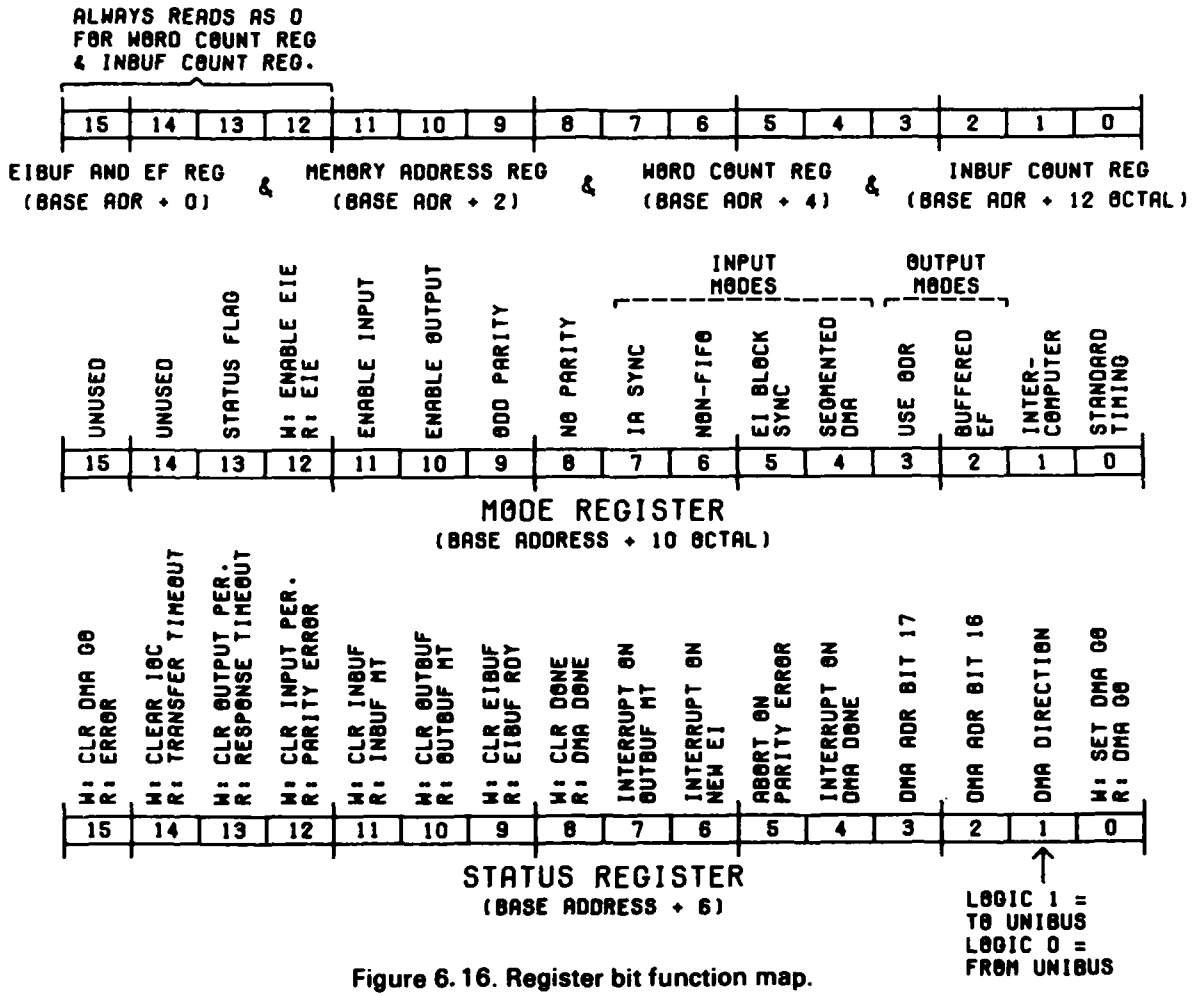



Figure 6.16. Register bit function map.

## APPENDIX. I/O CABLE PIN ASSIGNMENTS

The following pin assignments refer to the four 50-pin ribbon cable connectors on the IOC wirewrap card. For the two differential signal connectors (X & Y), the H or L following each signal name refers to the "asserted" state for control signals and the logic 1 state for data signals. For the two NTDS signal connectors (Z & G), the H refers to the asserted or logic 1 state of the single ended signal line, while the L identifies the "return" pin for that signal.

| INPUT CHANNEL CONNECTORS (X & Z) | | OUTPUT CHANNEL CONNECTORS (Y & G) | |
|---|---|---|---|
| Pin | Signal | Pin | Signal |
| 50 | IDR H | 50 | ODA H |
| 49 | IDR L | 49 | ODA L |
| 48 | IA H | 48 | ODR H |
| 47 | IA L | 47 | ODR L |
| 46 | EI H | 46 | EF H |
| 45 | EI L | 45 | EF L |
| 44 | EIE H | 44 | EFR H |
| 43 | EIE L | 43 | EFR L |
| 42 | CLR IP H | 42 | CLR OP H |
| 41 | CLR IP L | 41 | CLR OP L |
| 40 | STATUS FLAG H | 40 | STATUS FLAG H |
| 39 | STATUS FLAG L | 39 | STATUS FLAG L |
| 38 | Unused | 38 | Unused |
| 37 | Unused | 37 | Unused |
| 36 | Unused | 36 | Unused |
| 35 | Unused | 35 | Unused |
| 34 | PARITY H (IN) | 34 | PARITY H (OUT) |
| 33 | PARITY L (IN) | 33 | PARITY L (OUT) |
| 32 | DATA0 H (IN) | 32 | DATA0 H (OUT) |
| 31 | DATA0 L (IN) | 31 | DATA0 L (OUT) |
| 30 | DATA1 H (IN) | 30 | DATA1 H (OUT) |
| 29 | DATA1 L (IN) | 29 | DATA1 L (OUT) |
| 28 | DATA2 H (IN) | 28 | DATA2 H (OUT) |
| 27 | DATA2 L (IN) | 27 | DATA2 L (OUT) |

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 26 | DATA3 H (IN) | 26 | DATA3 H (OUT) |
| 25 | DATA3 L (IN) | 25 | DATA3 L (OUT) |
| 24 | DATA4 H (IN) | 24 | DATA4 H (OUT) |
| 23 | DATA4 L (IN) | 23 | DATA4 L (OUT) |
| 22 | DATA5 H (IN) | 22 | DATA5 H (OUT) |
| 21 | DATA5 L (IN) | 21 | DATA5 L (OUT) |
| 20 | DATA6 H (IN) | 20 | DATA6 H (OUT) |
| 19 | DATA6 L (IN) | 19 | DATA6 L (OUT) |
| 18 | DATA7 H (IN) | 18 | DATA7 H (OUT) |
| 17 | DATA7 L (IN) | 17 | DATA7 L (OUT) |
| 16 | DATA8 H (IN) | 16 | DATA8 H (OUT) |
| 15 | DATA8 L (IN) | 15 | DATA8 L (OUT) |
| 14 | DATA9 H (IN) | 14 | DATA9 H (OUT) |
| 13 | DATA9 L (IN) | 13 | DATA9 L (OUT) |
| 12 | DATA10 H (IN) | 12 | DATA10 H (OUT) |
| 11 | DATA10 L (IN) | 11 | DATA10 L (OUT) |
| 10 | DATA11 H (IN) | 10 | DATA11 H (OUT) |
| 9 | DATA11 L (IN) | 9 | DATA11 L (OUT) |
| 8 | DATA12 H (IN) | 8 | DATA12 H (OUT) |
| 7 | DATA12 L (IN) | 7 | DATA12 L (OUT) |
| 6 | DATA13 H (IN) | 6 | DATA13 H (OUT) |
| 5 | DATA13 L (IN) | 5 | DATA13 L (OUT) |
| 4 | DATA14 H (IN) | 4 | DATA14 H (OUT) |
| 3 | DATA14 L (IN) | 3 | DATA14 L (OUT) |
| 2 | DATA15 H (IN) | 2 | DATA15 H (OUT) |
| 1 | DATA15 L (IN) | 1 | DATA15 L (OUT) |

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