AD-A159 494 LOW CAPACITANCE E-BEAM FABRICATED BEAM LEAD SCHOTTKY BARRIER DIODES(U) UNIVERSITY COLL CORK (IRELAND) MICROELECTRONICS RESEARCH CENTER G T WRIXON JUN 85 1/1

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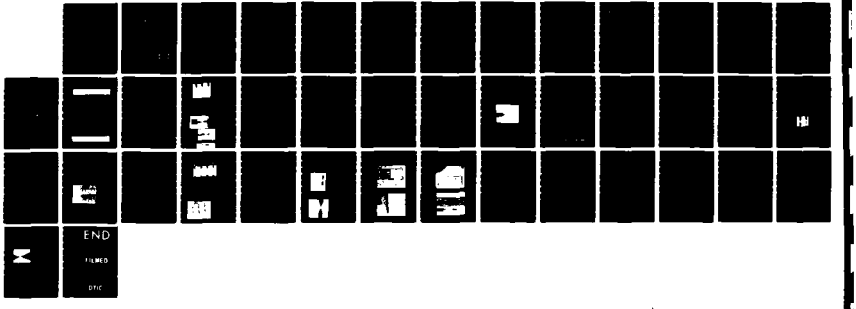

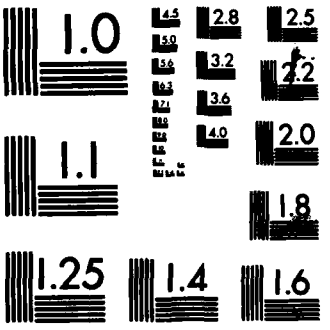

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IRELAND

LOW-CAPACITANCE E-BEAM FABRICATED BEAM LEAD SCHOTTKY BARRIER DIODES

Final Technical Report

June 1985

United States Army
European Research Office of the U.S. Army
London, England

CONTRACT NUMBER DAJA37-81-C-0261

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This is the final report in the series describing the work performed under contract No. DAJA37-81-C-0261, the object of which is to develop a process capable of fabricating low-parasitic high performance beam diodes. The diode chips use a unique physical structure which maximises overall strength and minimises the structural capacitance. In this report we present the full process which has been developed and we describe the evaluation devices which have been produced.

Keywords include:

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CONTENTS

1. INTRODUCTION

A unique method of fabricating low capacitance GaAs beam lead diodes for use in millimeter and sub-millimeter circuits has been developed. This method eliminates the mechanical fragility associated with other beam lead diode structures.

The essential technique is to minimise the overlay parasitic capacitance, by removing all the GaAs material outside a small region in the immediate location of the Schottky contact.

Previous progress reports have described many of the individual processing steps required to fabricate various features required in a beam lead diode (BLD) but did not run through this process from beginning to end in order to verify its feasibility. In addition some crucial aspects of the fabrication procedure remained untried, and some aspects needed improvement.

In this final report we describe firstly in section 2 the anode lithographic procedures and the electroplating techniques for forming the anode contact. This is perhaps the most significant step in the whole sequence from the point of view of establishing the electrical characteristics of the junction. This is followed in section 3 by a description of some changes to the ohmic contact fabrication. Section 4 includes the measurements which were made in order to verify the size of the parasitic capacitances of the beam lead diode structure. Section 5 details the processing which was done during the final laboratory phase of this work, i.e. Dec 84 through June 85.

Section 6 contains a summary of the complete fabrication process with references to the previous reports where full details are available.

Finally, Section 7 contains a brief summary and presents our conclusions.

2. Anode Definition and Plating

The object here is to define a 2um Schottky barrier diode using Mask 2. The 2um diode hole is defined on an SiO_2 layer which is then plasma etched through to the GaAs surface. The diode hole is then electroplated to make the anode contact.

The thickness of the resist is increased by reducing the spin-time and/or the r.p.m. of the photo-resist spinner. This increase in resist thickness is to protect the resist from polymerising during the SiO_2 plasma etch. If polymerising occurs on the resist it is then put into a O_2 plasma for 30-60 sec until the polymer is removed from the surface, yet leaving enough resist to continue on with the SiO_2 plasma etch.

With this new resist thickness new exposure and develop times had to be determined. Also with the thicker resist the difference between the build up at the side of the chip and the centre is not as great. Therefore the extra photolithographic stage of exposing and developing away the resist built up at the side of the chip is eliminated. (See 3rd periodic Technical Report November 1984 p. 15 subprocess 1b).

Subprocess 2a

Procedure for Cleaning Chip for Negative Resist and Exposure of Diode Pattern onto it.

Clean:	Rinse in DI for 5 minutes	(Deionised water)
	Boil in TCE	(Trichloroethylene)
	Boil in IPA	(Isopropanol)
	Boil in ACE	(Acetone)
	Boil in XYL	(Xylene)

Outgassing. Bake at 200°C for 60 min.

Let cool [in a clean air hood]

Spin On: Spin on 747 photoresist 5000 r.p.m. for 30 sec.

Bake 80°C for 20 mins

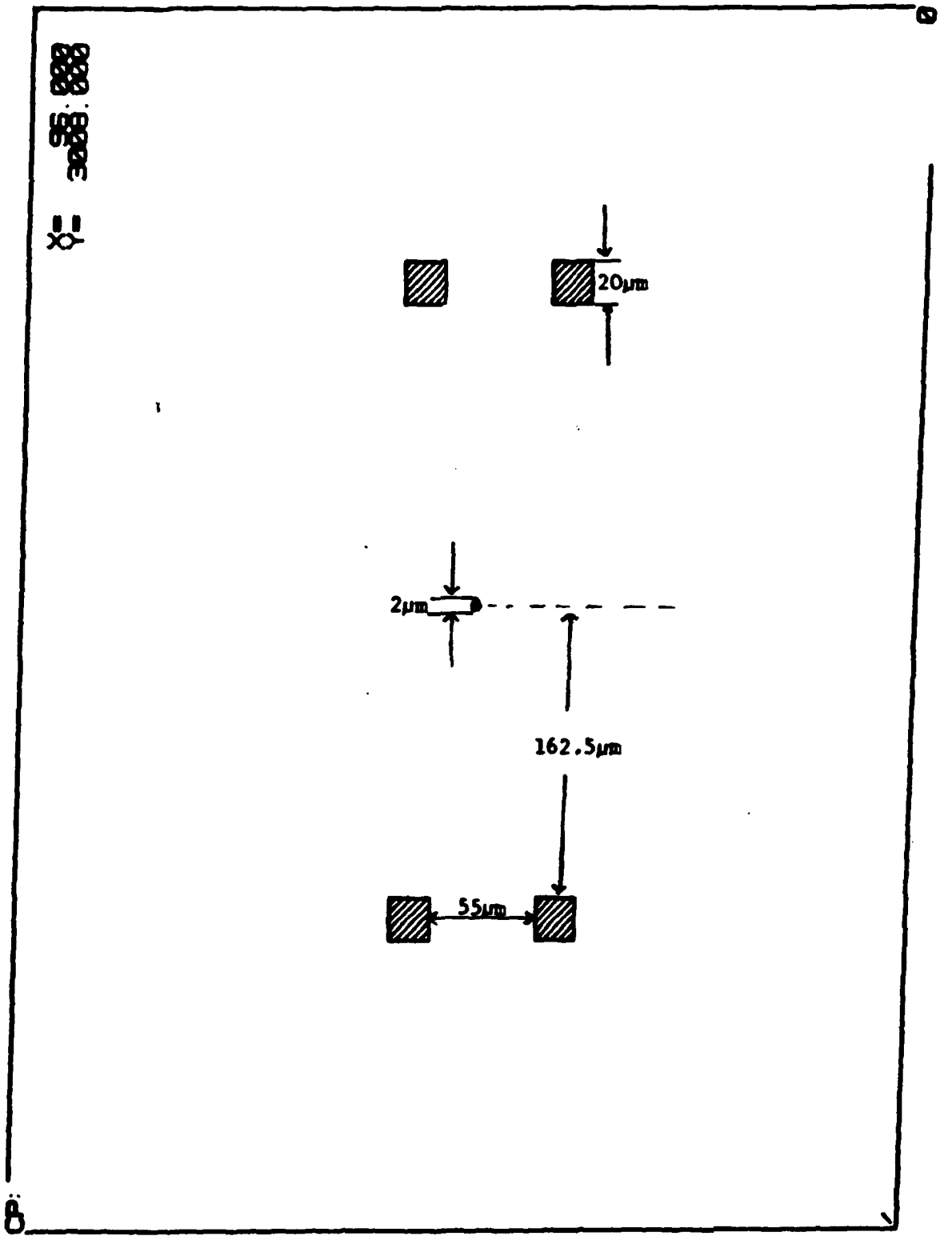
Let chip cool.

Exposure: Expose mask 2 for 2 secs. [See figure 1 and figure 1(i)]

Develop in Kodak 747 developer for 180 secs

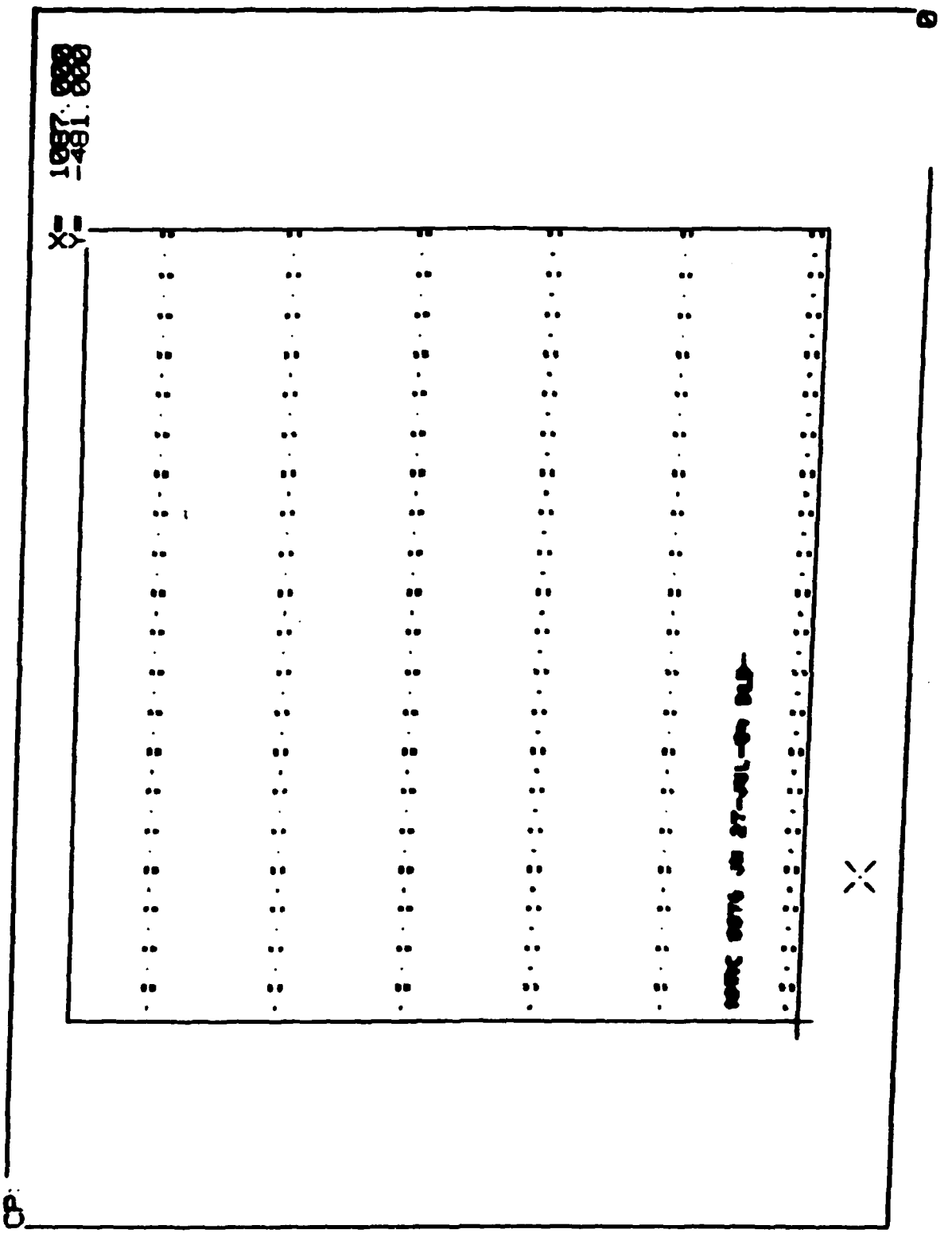
Rinse in Kodak 747 for 15 sec

Post Bake: 120°C for 30 mins.



Schottky Barrier Diode Pattern

Fig. 1



Overall View of Schottky Barrier Diode Pattern

Fig. 1(i)

Subprocess 2b

SiO_2 Plasma Etch

In this procedure etch rates must be determined for various relative concentrations of three gases:

CF_4 (tetrafluromethane)

CHF_3 (trifluromethane)

Ar (Argon)

The flow rate concentration is critical in that the formation of photoresist polymers by the plasma must be prevented.

The thickness of the SiO_2 layer used in these etch tests is 15KA, with an etch rate of 100Å/min.

Prior to the SiO_2 etch the plasma etcher was cleaned for 30 mins in an O_2 plasma created in the chamber.

The plasma etch was carried out in 10 minute intervals. This had three main purposes

(i) to check oxide colour

(ii) allow for cooling the resist

(iii) continuous check for formation of polymers

Plasma etched S.B.D. hole

Side profile schematic diagram of S.B.D.

Subprocess 2c

Pt and Au Plating

The high field pulse plating (HFFP) method is used in this process (see Subprocess 1d p. 19 3rd periodic Technical Report Nov. 1984).

The following steps were introduced in the pulse plating subprocess.

#1 Etch chip in Buffer oxide etch (BOE). This is to make sure all the SiO_2 is removed from the anode holes.

#2 Paint positive photoresist around the edge of the chip so as to reduce the plating area of the chip. Bake it then for 10 min. 90°C.

#3 Etch the GaAs surface in a Bromine methanol etch for thinning the epilayer of the GaAs. This also gives a good preplating clean of the surface.

#4 Rinse in methanol and blow dry in O.F.N. (oxygen free nigrogen).

#5 The area of GaAs to be exposed to the plating solution is calculated in mm^2.

#6 The plating time and current must also be calculated, this is determined by the anode thickness required.

#7 The face of the chip is held at the surface of the plating solution using a copper vacuum tube. The plating solution is kept at 80°C.

#8 The chip is then removed from the Pt solution and placed into the Au solution and Au plating takes place. After plating is complete the chip is rinsed in DI.

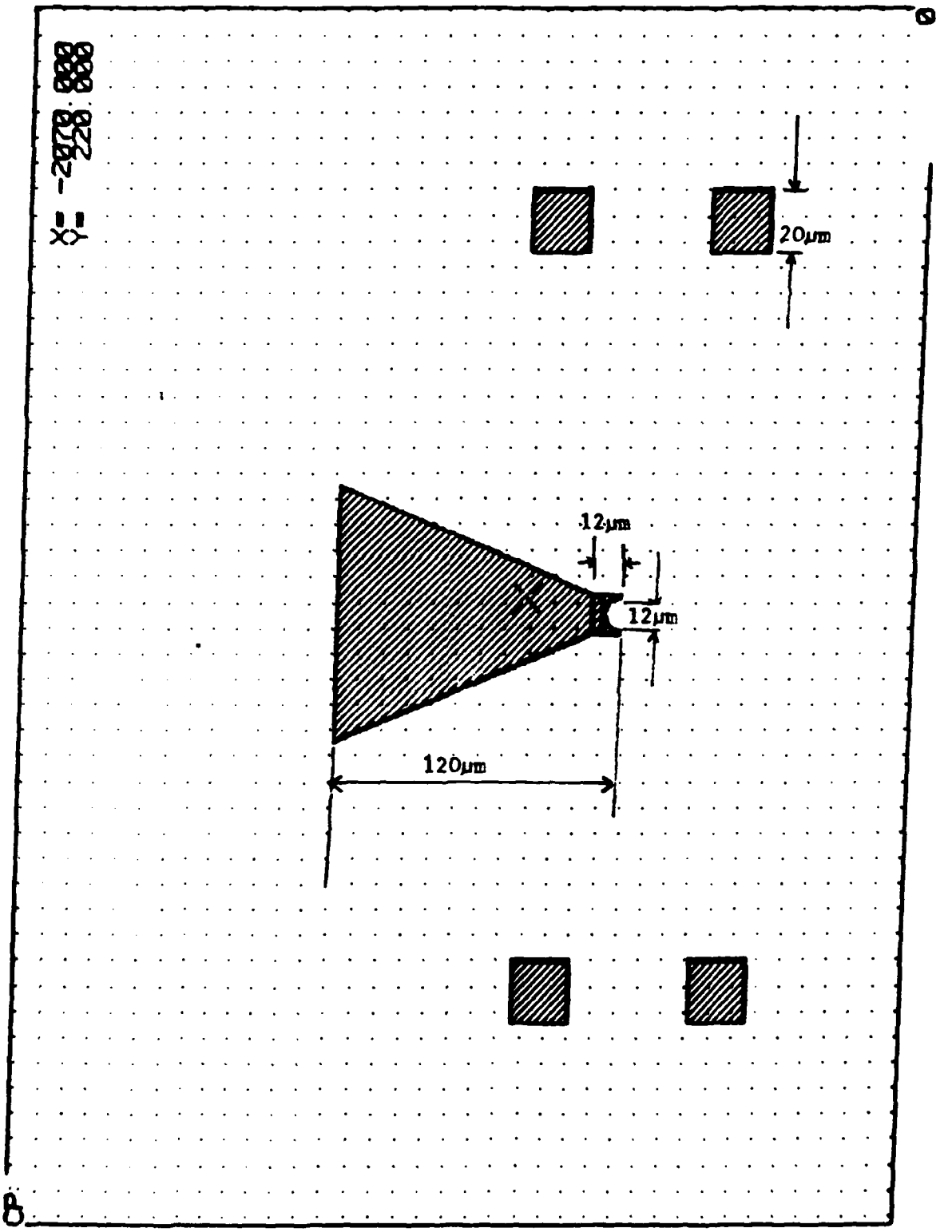
N.B. The plating solution temperatures are kept constant in a fixed temperature bath. The plating solutions are continuously stirred using magnetic stirrers.

3. Cathode Ohmic Contact Alterations

A new cathode ohmic contact mask was designed to match the alignment squares of the S.B.D. anode pattern. Figure 2 and Figure 2(i) show the new cathode ohmic contact pattern.

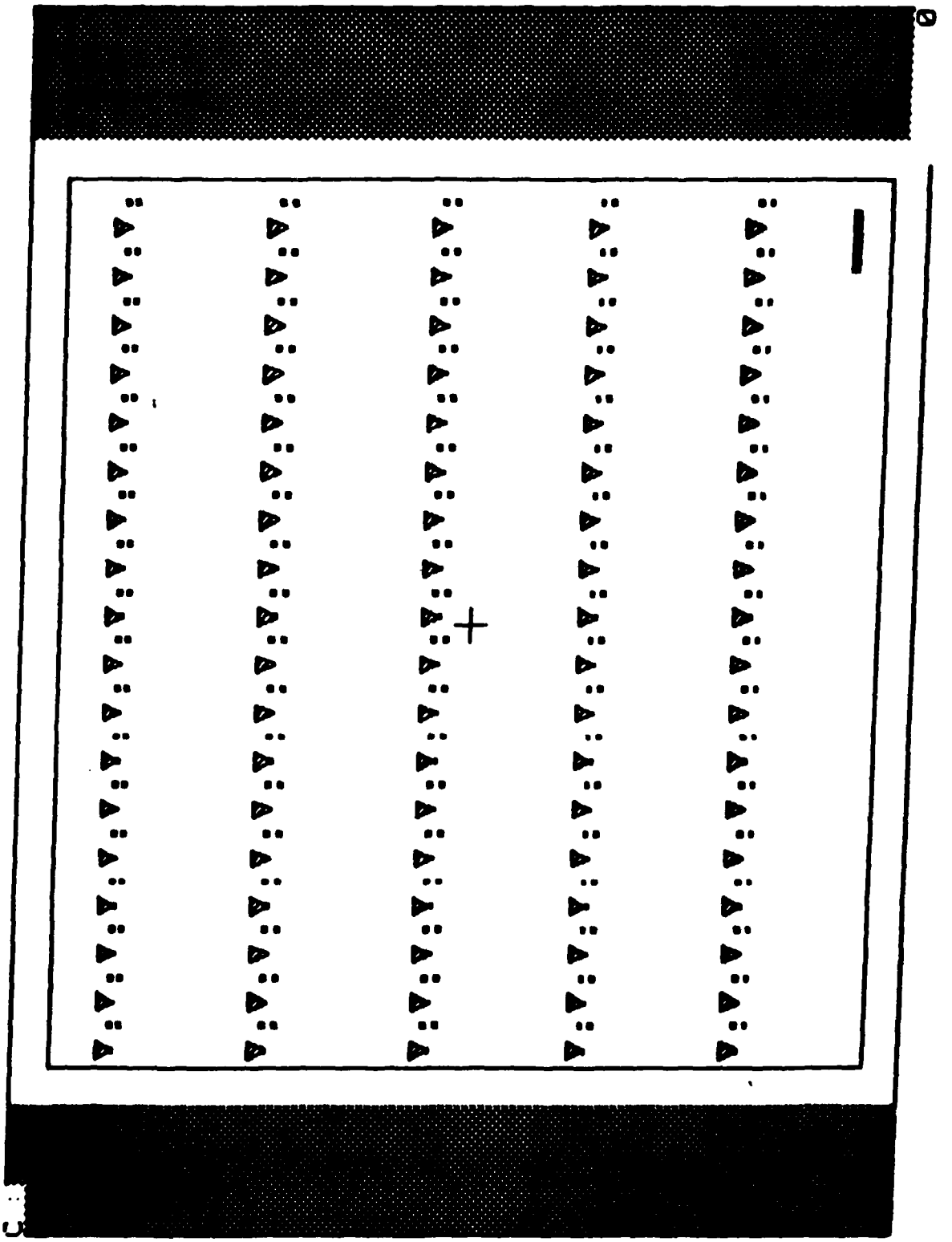
The process procedure is the same as that stated in "3rd Periodic Technical Report November 1984 - Cathode beam lead ohmic contacts, p. 15".

Subsequent to the capacitance measurements described in section 4 it is obvious that the ohmic contact mesh could be modified to provide improvements in the magnitude of the parasitic capacitance. The figures show the resulting geometry.



New Cathode Ohmic Contact Pattern

Fig. 2



Overall View of New Cathode Ohmic Contact Pattern

Fig. 2(i)

4. Parasitic Capacitance Model Testing

The capacitance testing was carried out using a 22mm x 22mm quartz slide as the substrate to test the parasitic capacitances between the beam leads. The beam lead patterns are evaporated onto the quartz slide using the beam lead metallisation mask (Mask 3).

The process is as follows:

The quartz clean:	Rinse DI
	2 boils in TCE
	Boil in ACE
	SiO_2 plasma etch 30 mins
Outgas:	Bake 200°C for 30 mins
	Let cool
Spin on:	Spin AZ21350 (positive resist) 5000 rpm 60 sec
	Bake for 30 min at 90°C
Exposure:	Soak in Chlorobenzene 1 min
	Expose to mask 3 6 secs
	Soak in chlorobenzene 7 min
	Develop 120 sec 1:4 (351 developer:DI)
	Rinse DI
Evaporation:	Load into evaporator
	Pump down to $< 10^{-6}$T
	Evaporated 500A Cr
	Evaporated 2000A Au
Lift-off:	Lift off of unwanted metal in ACE

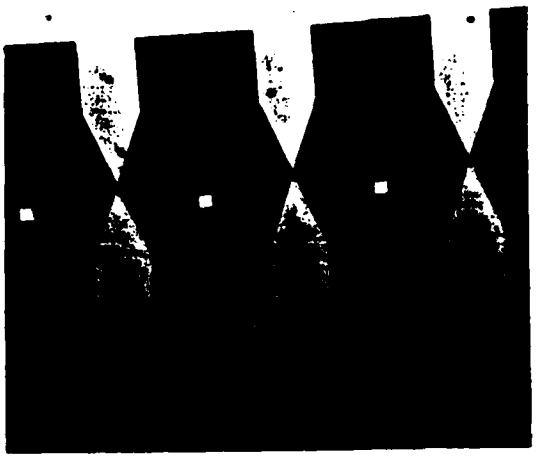
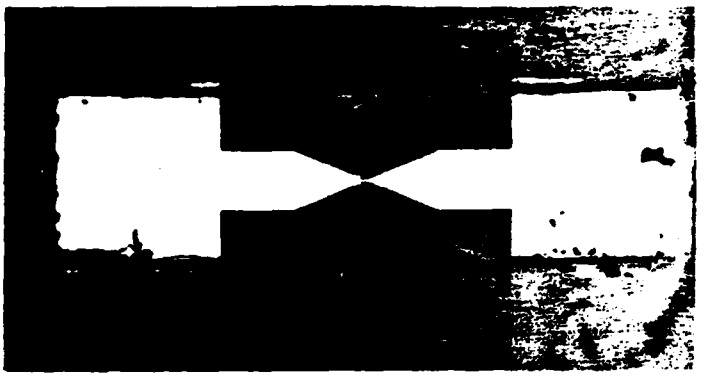


Photo 3 shows beam lead pattern after lift-off
Magnification X80

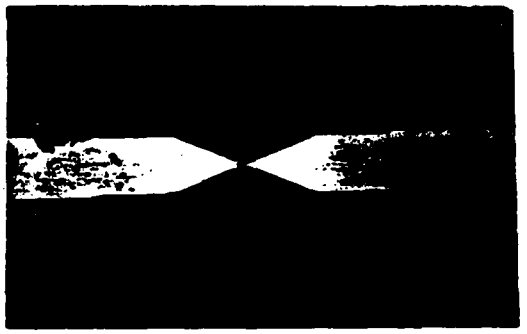
The beam leads were separated by lightly scribing the quartz and removing the metal from the neighbouring beam leads.

The beam leads themselves were cut in different lengths so as to determine the best size of beam lead by its parasitic results.

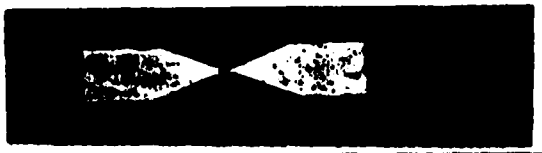
The beam lead cuts are shown in photos 3a, 3b, and 3c.



X80
Normal Cut
(Photo 3a)

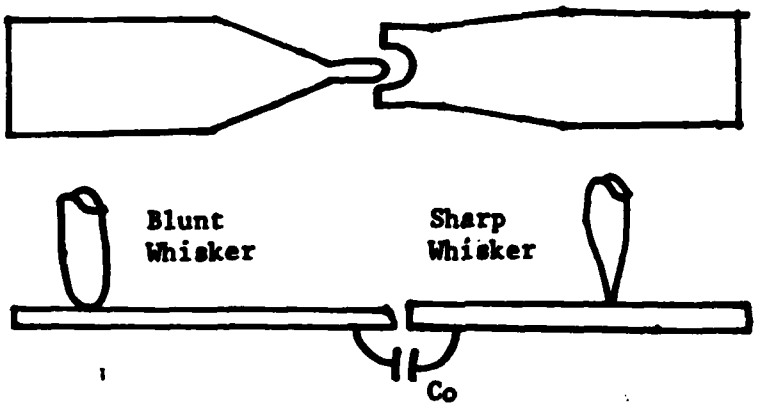


X80
Long Cut
(Photo 3b)



Modified Cut
(Photo 3c)

The beam leads were contacted by two Cu/Sn "whiskers", one blunt and one sharp. The blunt whisker being about 2um and the sharp one about 0.5um. The blunt whisker was continuously contacted to the anode beam lead, while the sharp whisker probed the other beam lead contact pad.

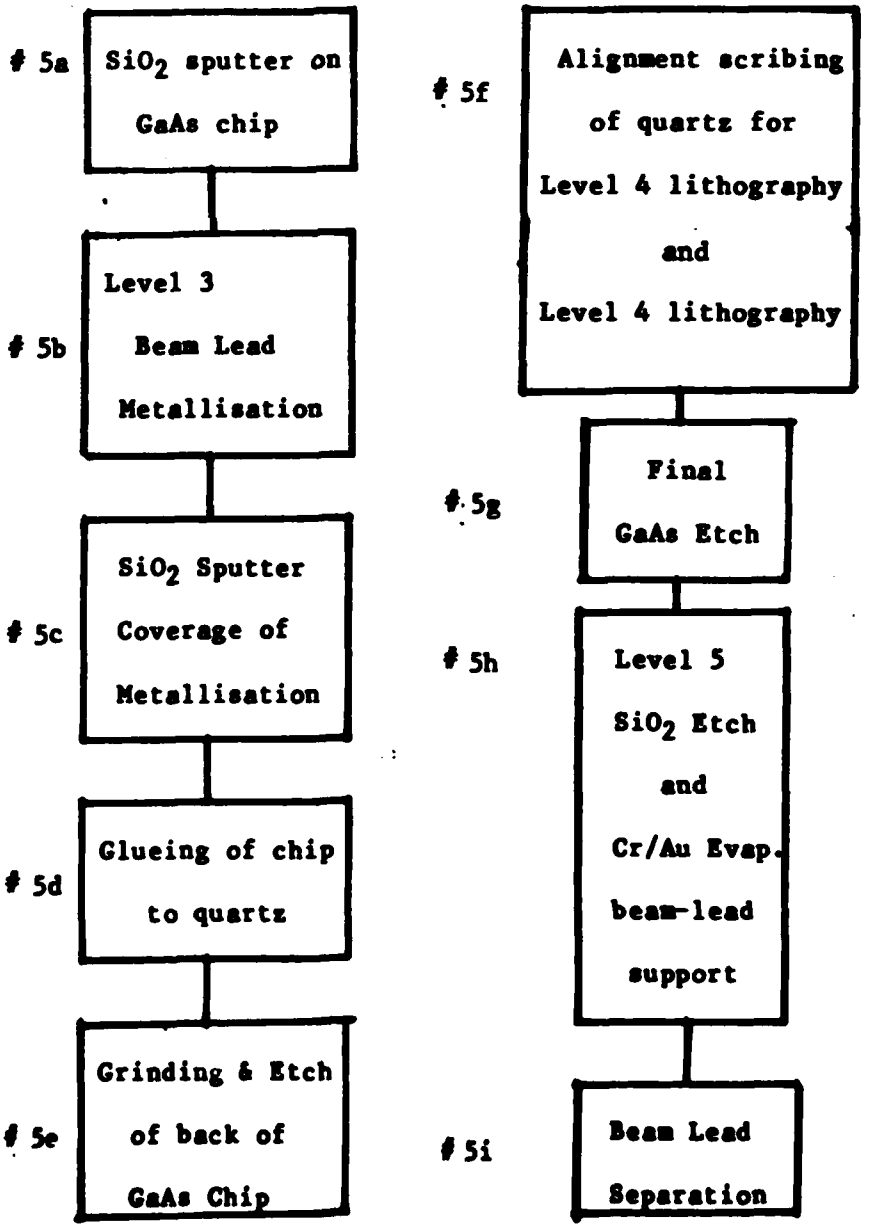


The capacitance between the beam leads were measured using a capacitance bridge. Approximately 10 readings were taken at different parts of the beam lead, being probed. The results are as follows:

Cut Type	Range of Co (fF)	Average Co (fF)
Modified	4.5 < Co < 8.5	7.57
Normal	14.3 < Co < 17.3	15.8
Long	11.8 < Co < 13.5	12.62

5. Beam Lead Diode Processing

The object of this work was to show that it is feasible to actually fabricate the beam lead structure. From the previous discussion it is possible to fabricate as far as level 3 (metallization stage). The object here is to start at level 3 and work through the process outlined below, ultimately achieving separation of fabricated beam leads.



Subprocess 5a

SiO_2 Sputter on GaAs

The process is started with five 5mm x 5mm substrates.

GaAs Clean:	Rinse and swab in DI
	Boil in TCE
	Boil in TCE
	5 min etch 1:1 Hcl:DI
	Rinse DI
Sputter Loading:	Loaded into sputterer within 5 min
	Fill liquid nitrogen
	Allow pump down to 10^{-7}T
	Sputter clean SiO_2 target 15 min
	Sputter at 300W for 1 hr 15 min

Measured the SiO_2 thickness 7.5KA

Subprocess 5b

Beam Lead Metalisation Level 3 Cr/Au Evaporation

Clean:	Rinse DI
	Boil TCE
	Boil TCE
	Boil in ACE
Out Gas:	200° for 1 hr
Level 3 Lithography:	Spin on AZ1350 positive photoresist 5000rpm 60 sec
	Bake 30 min 90°C
	Let cool
	Soak in Chlorobenzene for 1 min
	Blow dry OFN
	Expose 6 sec mask 5
	Soak in chlorobenzene for 7 min
	Blow dry OFN
	Develop in 351 developer:DI (1:4) 65 secs
	Rinse in DI
Post Bake:	90°C for 30 min
SiO_2 Etch:	Rinse DI
	15 sec in BOE
	Rinse DI
Evaporation:	Loaded into evaporator
	Pump down < 10^{-6}T
	Evaporated 500A Cr
	1000A Au

Lift off: Placed in ACE

Wait for metal to float off

Swab gently to remove any unwanted metal

Boil in ACE

Place in O_2 plasma to remove any residue

of photoresist for 1 hour

Boil in ACE

See Metal pattern after lift off in photo 4b.

X180

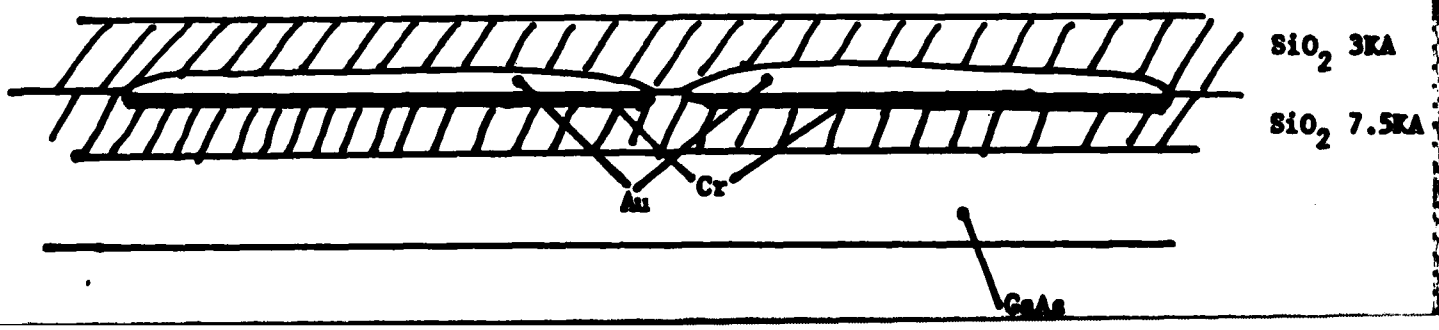
Photo 4b

Subprocess 5c

SiO_2 Sputter Coverage of Metalisation

Clean Beam-leads:	Boil DI
	Boil TCE
	Boil TCE
	Boil MeOH
Sputter:	Loaded into sputterer within 2 mins
	Fill sputterer with liquid nitrogen
	Pump down to 10^{-7}T
	Sputter clean target 200W 10 min
	Sputter chips at 100W 1hr 20 min

See figure 4c for schematic diagram of the resulting structure from the above process step.



Subprocess 5d

Glueing of Beam Leads to Quartz

Pre Glue Quartz Clean: Rinse DI

Boil TCE

Boil MeOH

US MeOH

Oxide plasma etch 20 min

Place a drop of "Loctite glass bond" onto the middle of the quartz slide. Placed SiO_2 face of beam lead onto the glue and manoeuvered it around in the glue to eliminate air bubbles between the chip face and the quartz slide. Clamp the chip down and expose to U.V. light 60 secs. See figure 4d

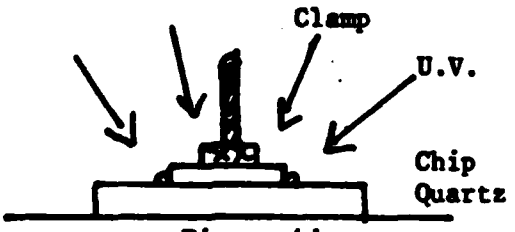


Figure 4d

The beam lead face of the chip through the quartz slide is then exposed to 60 secs UV. See figure 4d (i)

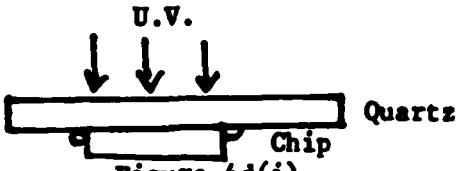


Figure 4d(i)

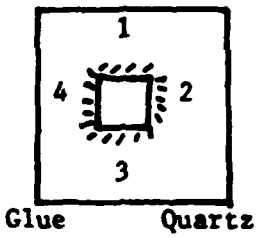
To make sure of good adhesion the beam lead chips glued to the slide are left exposed to natural U.V. for 2-3 days. (Natural U.V. meaning daylight through windows and room lights).

The glue had been previously tested against all the process solvents and acids and held up well to them all.

Subprocess 5e

Grinding the Back of GaAs

The chip on the quartz slide is then waxed down to a grinding chuck and ground down to 30-40um (See p. 26 process 4. 3rd Periodic Technical Report).



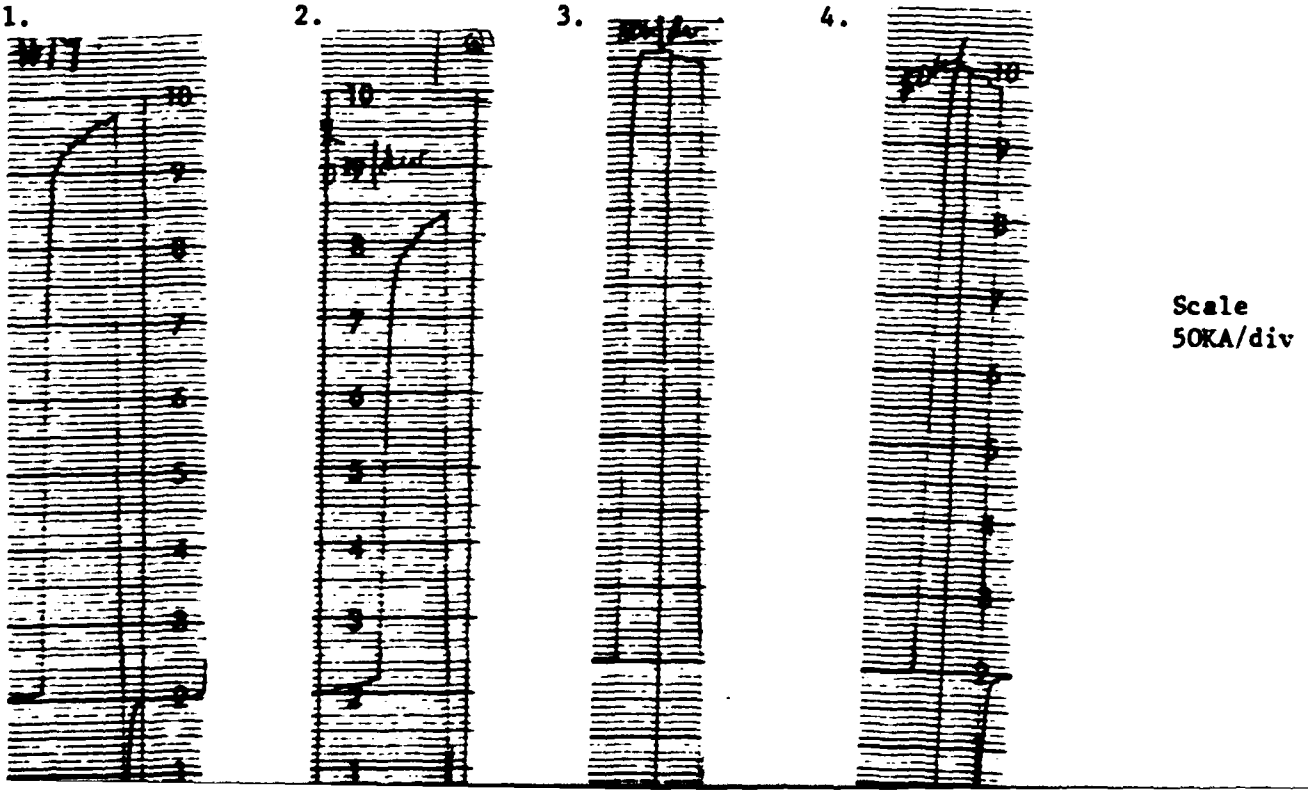
Ground Chip

1.

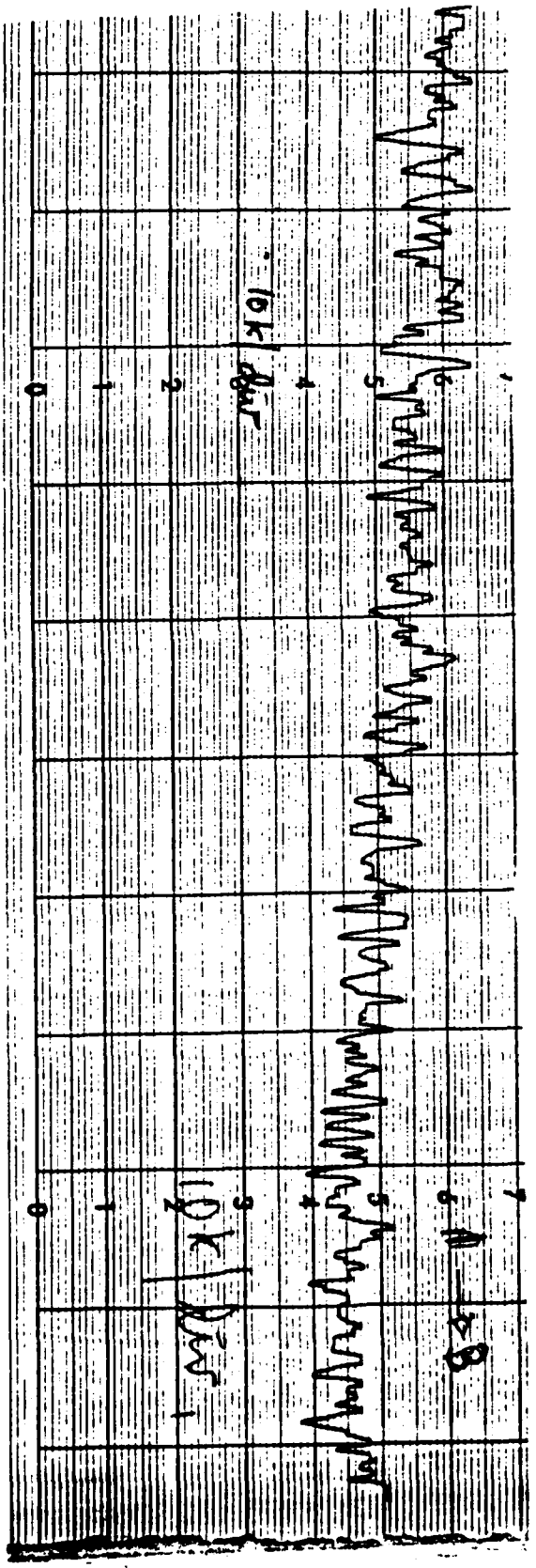
2.

3.

The above heights were measured using a Sloan Dektax profile measuring system. These profiles are shown below.



The surface profile of the ground GaAs surface was then turned using the Dektak profiler. The result was within 10um across the surface.



Dektak Profile across Chip from Position (1) to (3).

Vortex Etch

The chips are then etched down to 10um using H_2SO_4 : H_2O_2 : H_2O (3:1:1) in 1 minute vortex etch followed by a 30 sec rinse in DI.

(See page 32 3rd Periodic Technical report November 85)

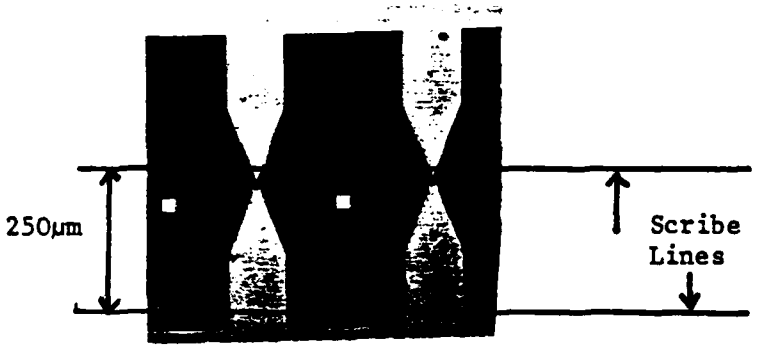
N.B. A fresh etching solution was made up for each vortex etch of a chip.

Subprocess 5f

Scribing of Beam Leads for Mask 4

Fine diamond scribe lines are scribed across the surface of the quartz.

Photo F



These 250um rectangular strips were drawn across all of the beam leads as shown in photo F)

Level 4 lithographic clean:	Short rinse DI
	Short Boil TCE
	Short Boil ACE + Rinse I pm
Out Gas:	200°C 30 min
	Let cool

Spin on: AZ1350H positive photoresist 5000rpm 60 sec

Bake 90°C 30 min

Expose mask A positive resist build up

Mask 90 secs (see 3rd Periodic Technical Report p. 16)

Develop 20 sec 1:5 (351:DI)

Rinse 20 sec DI

Expose mask IV 20 sec

Develop for 35 sec 1:5 (351:DI)

Rinse DI

Post Bake 90°C for 30 min

Before development the beam lead chip would look like this.Figure 4(i)

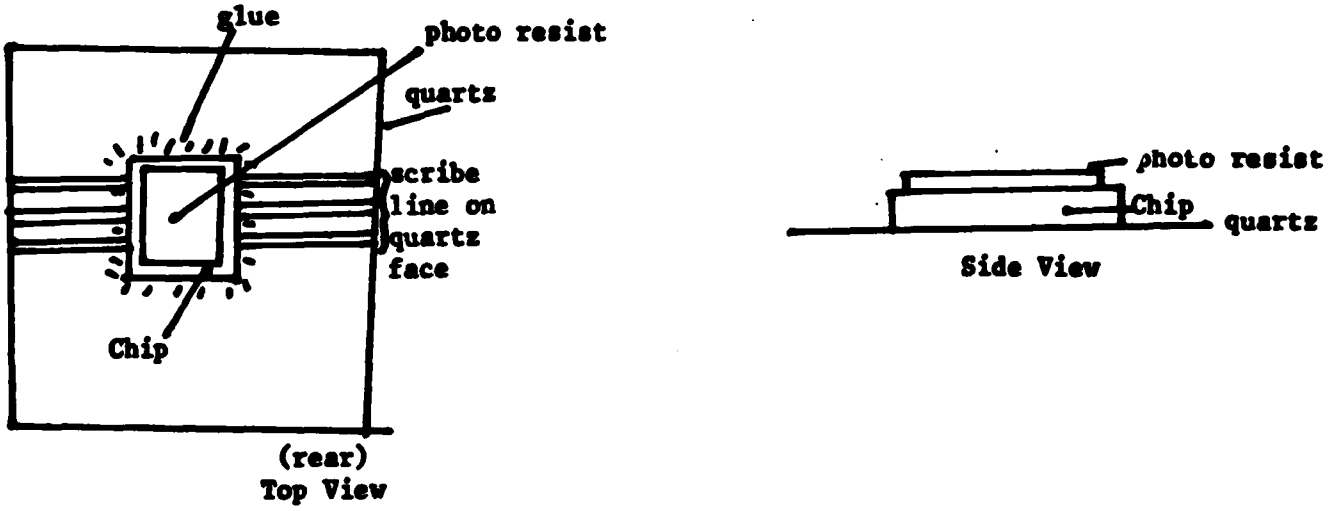
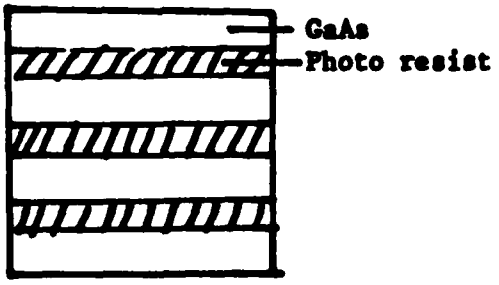


Figure 4.1

After the development we are left with strips of photoresist across the GaAs



Subprocess 5g

Final Etching of GaAs

A fresh solution aqua regia etchant is made up $Hcl:HNO_3$ (3:1).

The chip on the quartz is then immersed into the etchant for 2 minutes, taken out, rinsed in DI and examined under an optical microscope. This procedure is repeated for etch times of 75 secs., 45 secs and 30 secs until it is observed that the GaAs is removed. Except for the GaAs conducting strips beneath the photo resist. The chip id then etched in a O_2 plasma to remove the photo resist. See photo G.

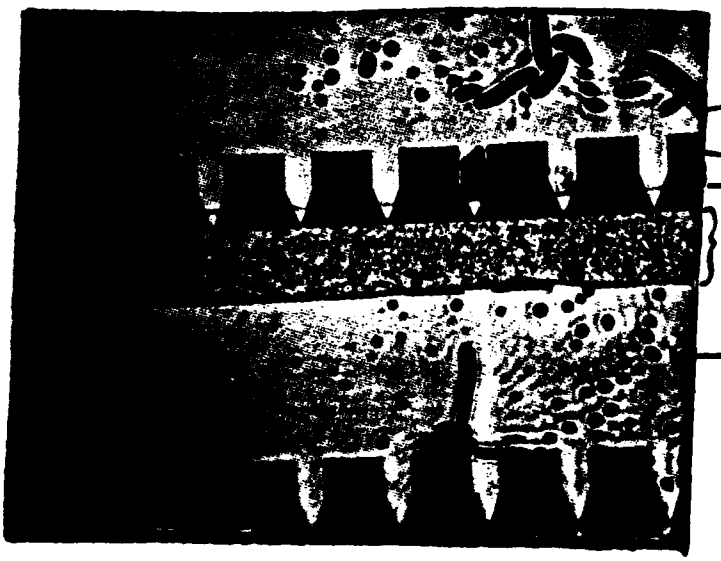
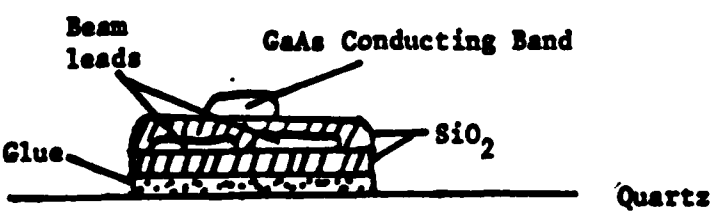


Photo G



Subprocess 5h

Oxide Etch Level 5 and Cr/Au Evaporation

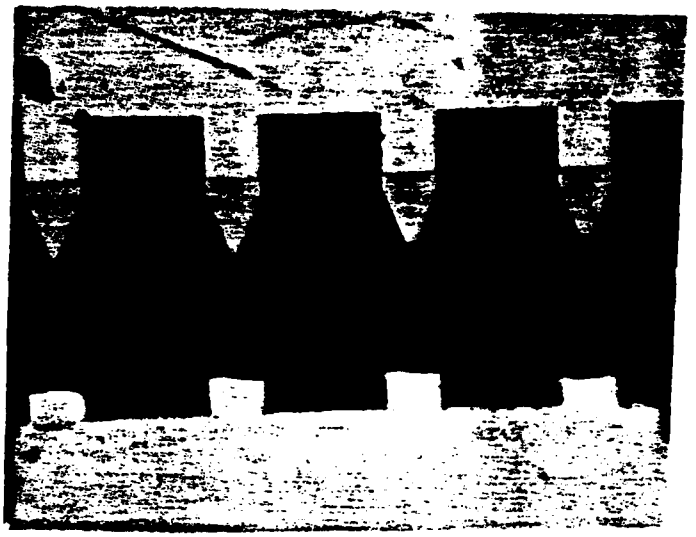
The chips were cleaned for level 5 lithography. This clean had to be very gentle because of the weaker structure of the whole beam lead structure.

Clean:	Rinse DI
	Gentle heat in TCE
	Gentle heat in IPA
	Rinse ACE
	Gentle blow dry OFN
Out Gas:	150°C 3/4hr (low temperature should improve glues strength).
	Let cool.
Spin on:	1350H for 60 sec 5000 rpm
	Expose mask A 90 sec positive
	(Photoresist build of mask)
	Develop 20 sec 1:5 (351:DI)
	Rinse 15 sec
	Expose mask 5 20 sec
	Develop 20 sec 1:5 (351:DI)
Post Bake:	Baked at 90°C for 30 min
	10 min etch BOE
	Take note that all oxide is removed down to Cr.

Photo H shows the result after the oxide etch.

X80

Photo H



Cr/Au/Oxide/Quartz

Resist/SiO_2/Quartz

Resist/SiO_2/Cr/Au

GaAs Conducting Band

Directly after the SiO_2 etch the chips are loaded into the evaporator for a Cr/Au evaporation the system is pumped down to $< 10^{-6}$T and 900A Cr and 1000A Au are evaporated. The chip is then placed in Acetone to remove excess metal. Photo H(i) shows the beam lead structure from the front through the quartz.

X80 Photo H (i)

Quartz/Glue, oxide

Quartz/Glue oxide/Au/Cr/Oxide

GaAs Conducting Strip

Quartz
Glue
Si Oxide
Au
Cr
Cr
Au

Subprocess 5i

Separation of Individual Diode Structures

The beam lead structure is waxed down level to 3 inch Si wafer as in figure i.

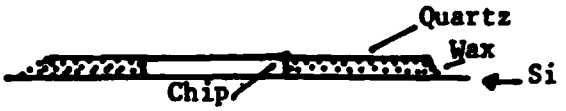


Figure i

The dicing was performed using a tempress 602 dicing saw. The Si wafer is held by vacuum to the dicing chuck. The blade used is a Tempress 12·361, typically 380µm long and 30µm thick. The quartz is cut all the way through to the Si wafer and the final cut width is approximately 40um. See cut pattern figure i(a)

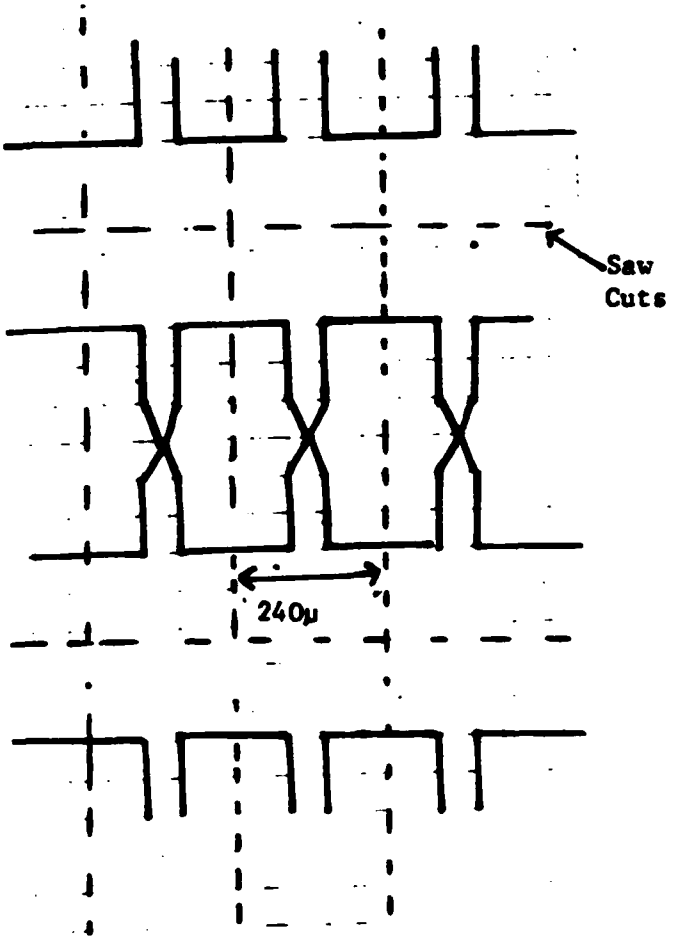
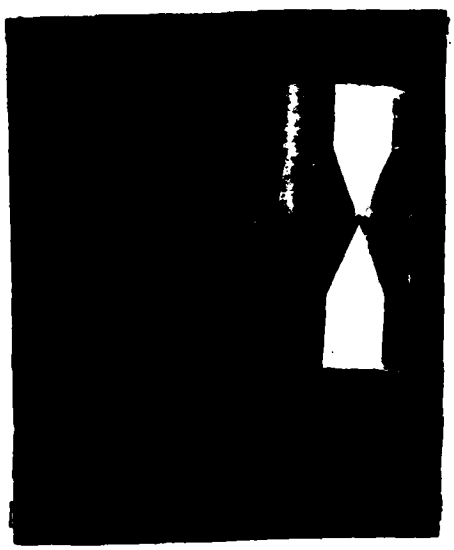


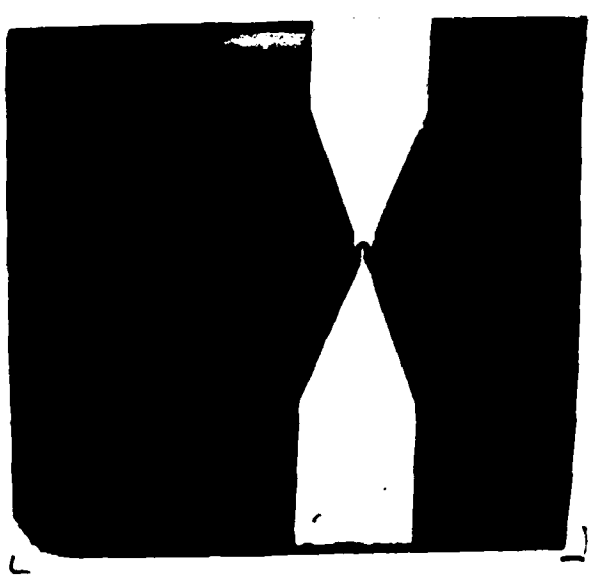
Figure i (a)

The diodes are then rinsed off the Si wafer using T.C.E. into a container of TCE and boiled then to clean away any TCE. The diodes are then filtered through filter paper and sorted using optical microscope.

Both photographs below show an individual beam lead diode structure. Both photographs are taken through the quartz face of the chip and are modified cuts.



Mag x 100

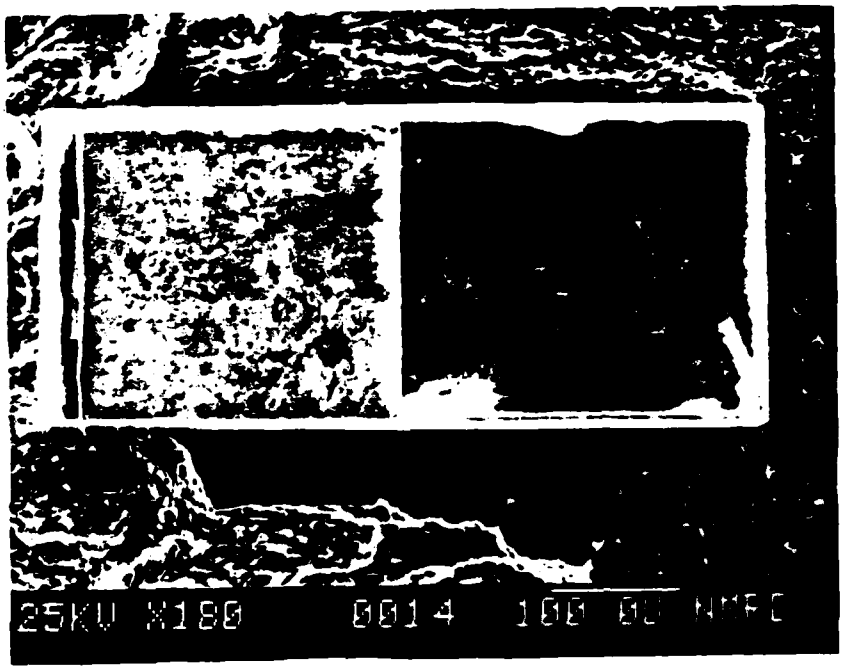


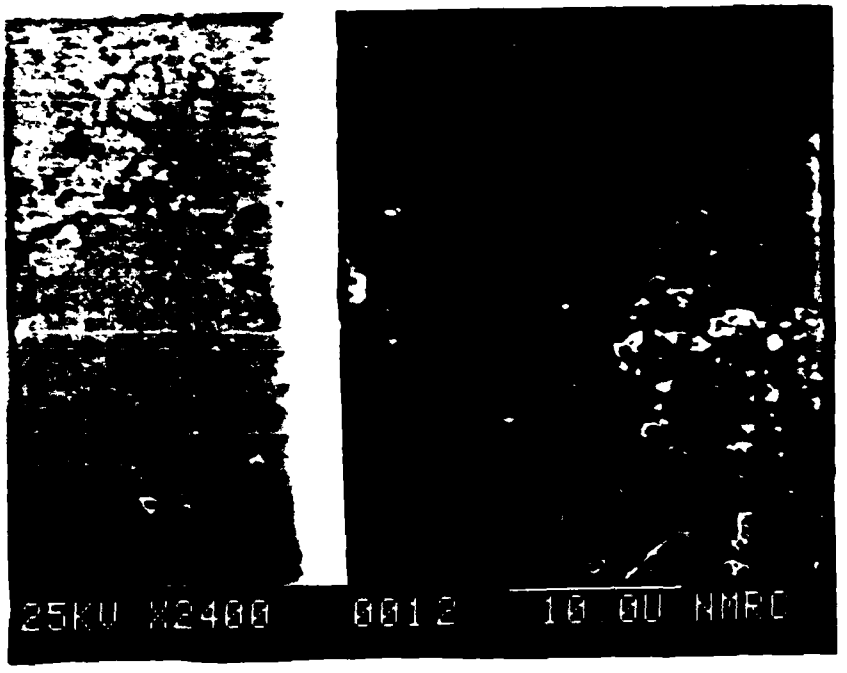
Cathode ohmic contact on GaAs, seen through SiO_2, glue and quartz.

Anode ohmic contact seen through SiO_2 and quartz.

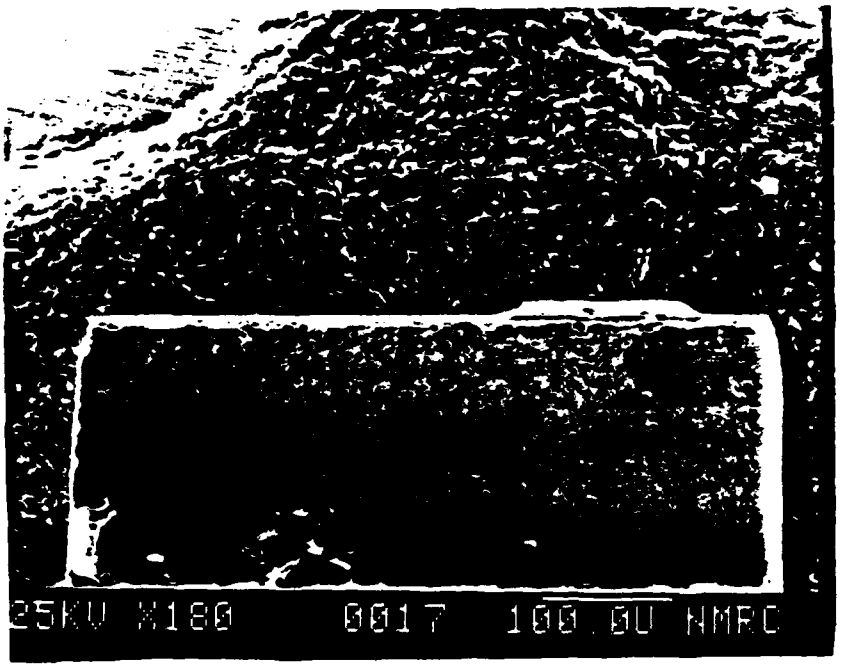
Mag x 200

The two micrographs below are of the beam lead diode structure seen from the back of the quartz. This shows the rear ohmic contact supports and the GaAs area left after grinding and etching.





The two micrographs below are of a side profile of the beam lead diode structure. The top micrograph is of an overall side profile of the chip. The bottom micrograph shows a high magnification micrograph of the GaAs, SiO_2, glue, quartz interface.



6. Summary of the Complete Fabrication Process

PROCESS STEP	TECHNICAL REPORT REF.
1. Substrate ohmic contact	3rd periodic technical report, Nov. 1984(p.14) subprocess 1(a).
2. SiO_2 sputter	Final technical report June 1985(p. 16) sub-process 5(a).
3. Cathode beam-lead ohmic contact	3rd periodic technical report, Nov. 1984(p. 15) subprocess 1(b), final technical report, June 1985(p. 9).
4. Defining Schottky diode and plating	Final technical report, June 1985(p. 3).
5. Overlay metallisation	3rd periodic technical report, Nov. 1984(p. 20), subprocess 1(e).
6. SiO_2 sputter coverage of metallization.	Final technical report, June 1985(p. 19), sub-process 5(c).
7. Glueing of beam leads to quartz	Final technical report, June 1985(p. 20), sub-section 5(d).
8. Grinding GaAs back and vortex etch.	3rd periodic technical report, Nov. 1984(p. 26), process 4. 3rd periodic technical report, Nov. 1984(p. 34) subprocess 5(a).
9. Defining GaAs conducting area	3rd periodic technical report Nov. 1984(p.34), subprocess 5(b) or final technical report, June 1985(p. 23), subprocess 5(g).
10. Final GaAs etch	3rd periodic technical report Nov. 1984(p.36), subprocess 5(d). Final technical report, June 1985(p. 25), subprocess 5g.
11. Beam lead ohmic contact	Final technical report,

7. Summary and Conclusions

In summary, the entire set of processing steps required to fabricate low capacitance beam lead diode chips has been developed and tested. The principle innovation in the structure described here is the use of a relatively thick quartz substrate to support the fragile junction in such a way as to make it mechanically strong and to minimise the excess capacitance incurred in so doing. Particular attention has been paid to verifying this particular aspect of the device and a batch of devices was fabricated in order to assess the resulting strength. This was a considerable improvement over the current state of the art in beam lead devices in that the chips could be easily manipulated for assembly and soldering purposes etc without any noticeable deterioration in the structural integrity. Photographs of these chips are shown in section 5 above.

In addition the other important attribute of the novel structure is its intrinsically low parasitic capacitance. Careful measurements have been made of this and the initially proposed structure was modified to reduce the parasitic values. The resulting structure exhibits measured capacitance values of 7.6fF in parallel with the junction.

It was not possible within the time available to make a batch of operating diodes suitable for low noise behaviour, as it was felt to be more important to implement the processing changes necessary to produce the reduction in parasitic capacitance to less than 8fF.

In conclusion we are confident that the output of this research

contract, which is in essence the list of processing steps summarised in page 33, together with the details supplied in this and the previous progress reports, has verified the feasibility of making low capacitance mechanically strong beam lead diode chips.

APPENDICES

"AN ULTRA-LOW CAPACITANCE BEAM-LEAD GaAs DIODE FOR USE IN HYBRID CIRCUITS AT MM AND SUB-MM WAVELENGTHS"

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Presented at the Ninth International Conference on Infrared and Millimeter Waves; Takarozzika, Japan, October 1984.

1984 IR & MM WAVES, TAKARAZUKA

"AN ULTRA-LOW CAPACITANCE BEAM-LEAD GaAs DIODE FOR USE IN HYBRID CIRCUITS AT mm AND SUB-mm WAVELENGTHS"

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Abstract

Minimisation of any stray parasitic components is of extreme importance if the performance capability of the active diode junction is to be fully exploited in high frequency hybrid circuits. A uniquely fabricated beam lead Schottky barrier diode with a structural parasitic capacitance of 4-5fF and a 6fF zero bias junction capacitance has been fabricated. This suggests conversion loss performance similar to that of whiskered Schottky diodes down to wavelengths approaching 1mm.

Introduction

State-of-the-art Schottky-barrier beam lead diodes have been reported in the literature to perform as favourable as whiskered diodes up to frequencies about 100 GHz, e.g. [1], [2]. Methods to define the diode active area have been either by utilizing a proton-implant isolation technique [3] or techniques involving the use of low melting point glass [4].

We have fabricated a Schottky-barrier beam lead diode by removing all the GaAs material except from a small region (30μm diameter) in the immediate location of the actual Schottky contact which defines the active diode area. This has the effect of drastically reducing the beam metallization overlay capacitance leading to a device whose capacitance is dominated by the junction capacitance. This device will therefore not suffer the conversion loss degradation observed in conventional beam lead diodes at frequencies greater than about 100 GHz.

Design Considerations

For a beam-lead diode the most critical parasitic component is the capacitance formed by the anode overlay metallization, which contacts the Schottky barrier diode and acts as a bypass capacitor across the active overlay parasitic capacitance is to remove all the GaAs material except for the location of the diode conducting area. The principal schematic of the diode assembly is shown in figure 1.

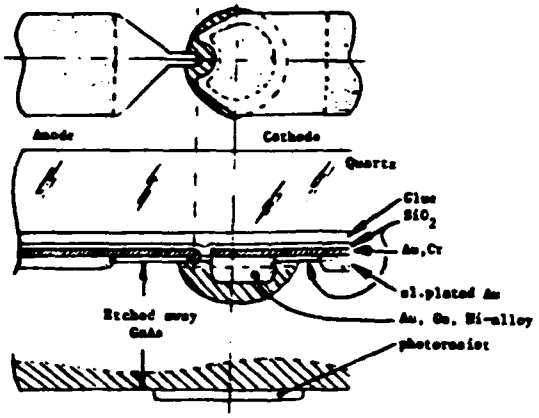

Figure 1. Principal schematic of the diode assembly.

Fabrication

The diodes were fabricated on epilayerstructure consisting of an n-type epilayer of carrier concentration $2 \times 10^{17} cm^{-3}$ on an n^+ substrate of carrier concentration $> 2 \times 10^{18} cm^{-3}$. The epilayer thickness is approximately 0.1 - 0.2μm.

After fabricating the ohmic contacts, the Schottky diodes and the overlay metallization, the "diode-side" of the chip is glued onto a quartz substrate. The "GaAs-side" of the composite quartz-GaAs chip is then ground down to a thickness of about 30μm. By means of chemical etching the GaAs layer is further reduced to approximately 10-15μm.

A mask defining the active conducting area of the diodes is aligned to the diode array. These are circular areas of 35μm diameters which coincide on the "GaAs-side" with the diodes on the "diode-side" of the chip. The excess GaAs, i.e. the 10-15μm layer of GaAs not covered by photoresist, is chemically etched away. Further etching decreases the parasitic capacitance of the diodes and reaches its minimum when the cirumferences of the GaAs dots fall tangent to the anodes of the Schottky barrier diodes.

Contact holes to the anodes and cathodes are finally opened up through the oxide and the chip assembly is sliced into individual diode chips. The glass substrate is now a carrier of the diodes to permit easy handling and good mechanical strength.

Results

The main difficulties to overcome in the fabrication were associated with grinding and uniformly etching the GaAs. Work is ongoing to refine these processes and to carry out RF measurements. Figure 2 shows the centre part of a etched GaAs beam-lead diode. The diameter of the GaAs dot is 30μm. The anode contacting finger is to the left in the microphotograph.

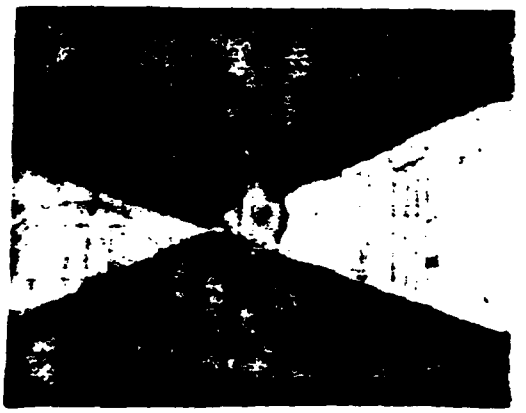

Figure 2. Centre part of an etched GaAs beam-lead diode.

Acknowledgements

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References

[1] B.J. Clifton, G.D. Alley, R.A. Murphy and I.H. Mroczkowski, "High-Performance Quasi-Optical GaAs Monolithic Mixer at 110GHz", IEEE Trans. Electron Devices, Vol. ED-28, No. 2 February 1981.

[2] S. Jamison, A. Contolatis, P. Bauhahn, J. Abrokwah, T. Peck, M. Helix and Chente Chad, "Beam-lead Schottky Barrier Planar Mixer Diodes for Millimeter Wave Applications ", IEEE Trans. MTT, Vol. MTT-25, No. 6, June 1977.

[3] R.A. Murphy, C.O. Bozler, C.C. Parker, H.R. Fetterman, P.E. Tannenwald, B.J. Clifton, J.P. Donnelly and W.T. Lindley, "Submillimeter Heterodyne Detection with Planar GaAs Schottky-Barrier Diodes", IEEE Trans. MTT, Vol. MTT-25, No. 6, June 1977.

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