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Hole Trapping in Thermal Oxides Grown under Various Oxidation Conditions Using Avalanche Injection in Poly-Silicon Gate Structures

FAIRCHILD
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Principal Investigator: Dr. Robert J. Strain
(415) 858-4451

Project Leaders: Kranti Anand
(415) 858-4457

Bruce Cairns
(415) 858-4661

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This is the final year's report of a three year project sponsored by DARPA. The main objective of this work was to study the trapping characteristics of thermally grown oxides on silicon substrates by means of avalanche injection. In this study, the substrates were n-type, <100> orientation so that only hole trapping was investigated. The gate material was LPCVD deposited polysilicon which was subsequently doped with phosphorus from a POCl3 source. A screening procedure was developed to insure that the devices measured were representative of the wafer and that they were able to survive the full test.

The main conclusions were as follows:

1) I/v data (where I is the dc current and v is the maximum value of the ac applied voltage across the device) was analyzed with respect to the theory and it was shown that the hole temperature not only depends on the substrate doping density and the electric field as

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CHAPTER 1

1.0 INTRODUCTION

1.1 This report covers the work done during the last year of a 3 year project. It begins by listing the work done in the first two years and its main conclusions (1). It will then describe the rationale for the work covered in this report which follows from the previous work. It should be pointed out that there were personnel changes between the two periods, and to some extent they reflect the change in emphasis of the project.

1.2 Summary of the First Two Years Report

The first report(1) entitled "Process Variable Dependence and Interrelationship Between Avalanche Charge Injection and Radiation Induced Carrier Trapping in Thermal Oxides," was published in April 1982. Measurements were performed on oxides grown in a variety of ways. In some cases the effect of exposure to radiation from various processes was also studied. The measurements consisted mostly of observing trapping of avalanche injected electrons and holes in these oxides. Hole trapping induced by Co60 of 1.0E6 rad (Si) radiation was also studied and compared. During radiation, the gate was biased to +10V. For details, one is referred to the report. However, a summary of its scope and findings is given below.

1.2.1 Formation of Oxides

Oxides were grown on p and n substrates of <100> and <111> orientation in dry O_2, pyrogenic steam and O_2/HCl mixture in the temperature range 800 °C to 1100 °C. For dry O_2 and steam , oxides were also grown at high pressures (up to 10 atm). Various in-situ anneals and pre and post metallization anneals were also investigated.

1.2.2 MOS Structure

All avalanche and radiation studies were done on circular dot structures of about 750 μm diameter with the back side of the wafer metallized using Al. Most measurements were done with Al gates though a few poly-gate measurements were also done.

1.2.3 Exposure to Process Related Radiation

The effect of exposure to electron beams (at doses of about 1.0E-4 Ccm^{-2} and 0.39-3.1E-2 Ccm^{-2}), laser beams and ion implant beams were examined.

1.2.4 Main Conclusions

As also seen by other workers, hole trapping is 2 to 3 orders of magnitude more efficient than electron trapping. Hence, electron trapping was carried out at J_{dc} of 1.5E-5 Acm^{-2} while hole trapping was done at J_{dc} of 4.5E-8 Acm^{-2} to

compensate for this effect. All comparisons were done on the basis of flatband voltage shift (ΔV_{FB}) after 2000 sec of trapping; the rationale being that at this time the oxide traps were reasonably close to being saturated and hence ΔV_{FB} would be a good measure of their total density. Discussion on these points are covered in chapter 3.

1.2.4.1 Hole Trapping

Dry oxides grown on <100> substrates gave the lowest trapping over the entire temperature range. Steam oxides had to be grown at temperatures below 1000^{o}C and annealed in a dry environment, e.g., Ar or N_2 to give comparable trapping levels. For oxides grown wet, at higher temperatures, Ar and N_2 anneals increased trapping. All other parameters studied, e.g., high pressure, HCl/O_2 ambient, silicon gate, low temperature H_2 anneal prior to metalization, process induced radiation, increased the trapping level. Hence, for lowest traps, one needs to keep growth temperature low and avoid H_2 bearing environments (either from steam or HCl). However, H_2 annealing is needed for reducing N_f and N_{it}. This can be done <u>after</u> metalization when no effect on trapping is seen.

1.2.4.2 Electron Trapping

For <100> substrates, either Ar or N_2 annealing was found to be necessary to give low traps with both dry O_2 and steam oxides grown at 1000^{o}C or above. High pressure O_2 and electron beam exposure also increased trapping.

1.2.4.3 Other Observations

An important observation was that there was good correlation between hole trapping due to avalanche injection and radiation induced trapping. Hence this technique could be used for monitoring the radiation sensitivity of oxides by performing electronic i.e. avalanche 'on-chip' measurements. No correlation was found between preavalanching N_f and N_{it} and post trapping ΔV_{FB}, even though it is clear that trapping changes both N_f and N_{it}.

CHAPTER 2

2.0 RATIONALE FOR THE SCOPE OF THIS REPORT

It was clear that, in the one year contract period, it would not be possible to cover all the areas that were opened up in the previous work.

Since hole trapping is several orders of magnitude more pronounced than electron trapping, it was decided to look only at the former. This is not to say that the importance of electron trapping is not recognized particularly in n channel devices. However, it should be pointed out that in short channel n MOSFETs, when the gate is operating at a lower voltage than the drain, field reversal takes place near the drain junction causing avalanche holes to be injected into the oxide. This has been found to be an important reliability consideration.

It was also decided that since all modern MOSFETs operate with poly-Si gates, this investigation would concentrate on that gate material.

It became quite clear at the very beginning of this work that there was considerable variation in the avalanche results between devices on the same wafer. Hence, a procedure was developed to ensure that the samples were representative of the population and also that they would survive the test which involves high fields within the oxide corresponding to avalanching in the substrate.

2.1 Experimental Factors Considered

A list of experimental factors that were investigated is given below:

1. Experiments were designed to develop a procedure for screening and selection of devices for testing.
2. Only poly-Si gate material was used.
3. Only hole trapping using n-type substrate of <100> orientation was investigated.
4. Effects of sacrificial oxidation prior to oxide growth on trapping were investigated.
5. Substrate doping by ion implantation and diffusion for 'on-chip'monitoring was also studied.

CHAPTER 3

3.0 AVALANCHE INJECTION AND TRAPPING (THEORY AND EXPERIMENTAL DATA)

3.1 Introduction

The purpose of this chapter is to indicate the theoretical aspects of two processes; avalanche injection of minority carriers and trapping within the oxide of a MOS structure, since this was the primary measurement vehicle employed in this study. The theoretical formulation associated with each of these processes are given indicating the concepts involved. The formulations will be used to discuss those results which illustrate the measurement itself. Comparisions among different type of oxides and substrates, which represent the main theme of this report will follow in Chapter 5. This discussion is necessary because certain anomalies were seen in the experimental data, and a realistic appraisal of them is important before comparing results for different oxides. In particular, sometimes scatter in results from device to device (usually with small physical distance between them) was seen within the same wafer. Since trapping is a time consuming measurement (typically it is done for 2000 sec for each device) rarely were more than four devices measured. Even so, it was not uncommon to find that the average values of ΔV_{FB} were smaller than the maximum variation, in spite of developing a procedure for minimizing the variation. Whenever this occured, the sample size was increased to produce greater confidence in the results. Another situation

which occured was one where the shift was minimal, i.e., usually less than Ø.1 V; these results are almost certainly not representative on the oxide.

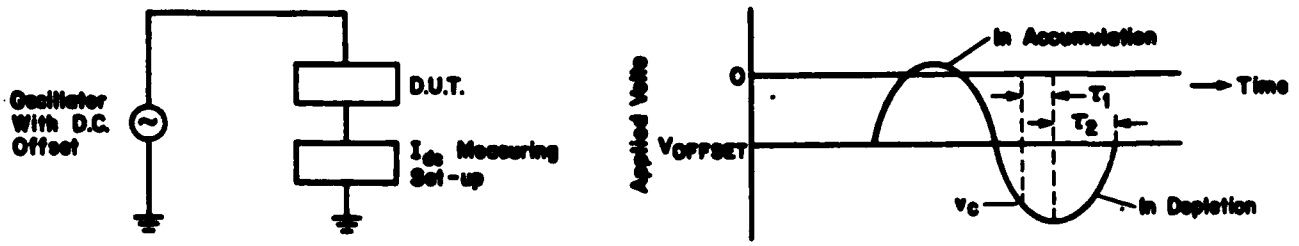
The cause of this anomaly is not yet understood. One possibility was that after avalanche sets in, only a small fraction of the holes generated, cross into the oxide. The rest collect at the SiO_2/Si interface bringing it to equilibrium. The result would be to reduce the potential drop across the semiconductor with a corresponding increase in the voltage and the field in the oxide. The increased field could allow injection of electrons from the gate which would neutralise the trapped charge. This could go on during the quarter cycle (see τ_2 in Fig. 3-1) while the field was still in the same direction. This situation could be avoided by applying a 'saw tooth' type of waveform such that once the maximum voltage was reached, the polarity reversal would be very fast.

In summary, the conclusions on the main body of this report need to be measured against a theoritical background to assist in determining accurate results.

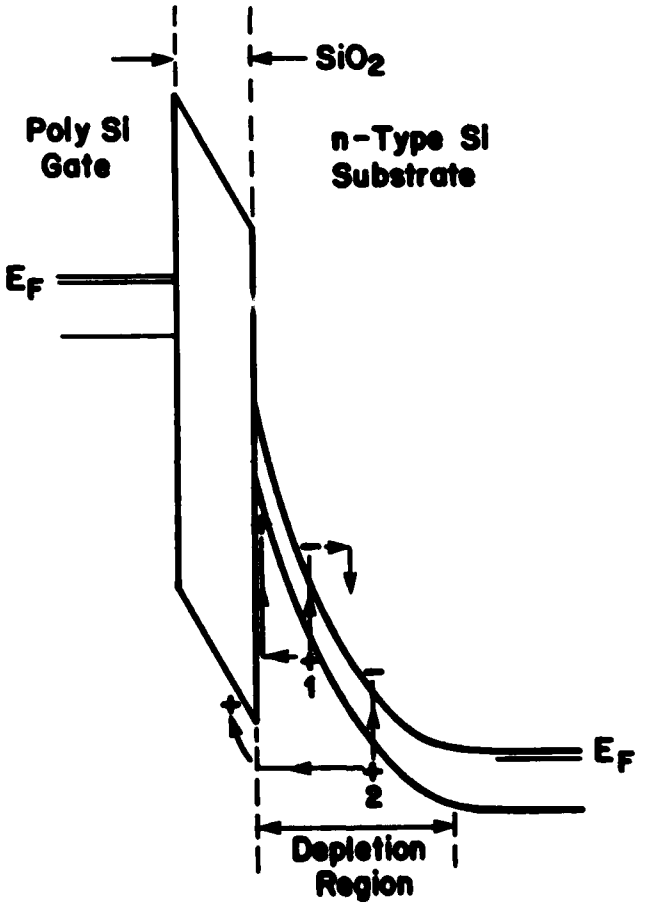
3.2 Avalanche Injection and Trapping

3.2.1 Avalanching

The experimental procedure (see Section 4.2) consisted of applying a sine wave a.c. signal of 45 kHz (period 22.2 μ sec) across the MOS device as shown in Fig. 3-1(a). The signal was continuously offset [Fig.3-1(b)] from the zero level as the peak to peak value is increased so that the peak voltage appearing



(a) (b)



(c)

Fig. 3-1 (a) The experimental set-up , (b) the applied voltage waveform and (c) the potential distribution within the device during avalanching. Hole 1 does not have enough energy to cross the barrier and hence drops to form the inversion layer. Hole 2 however does have enough energy and gets injected into the oxide to be thermalized over a short distance.

across the device when the semiconductor is in accumulation (this mostly appears across the oxide) was kept low enough to avoid oxide breakdown. In reverse bias, however, since the period for which it was applied was much smaller than the minority carrier generation life time τ_{gen}, minority carriers are not generated fast enough to maintain the semiconductor in equilibrium. Hence it goes into depletion and a substantial part of the instantaneous applied voltage v across the device would appear across the semiconductor. Above a certain value v_c, the field in the Si would be sufficiently large to take it into avalanche creating electron/hole pairs. Holes will move towards the SiO_2/Si interface. In their path from the point of generation to reaching the interface they will undergo a series of collisions reducing their kinetic energy (K.E.). However some of them (particularly those that are generated close to the interface) will reach the interface with sufficient K.E. to overcome the barrier and hence get injected into the valence band of the oxide. Since those carriers would not be in thermal equilibrium with the lattice they would be regarded as "hot". Their energy distribution at the interface is critical in determining how many will overcome the barrier ϕ_B. It is generally assumed that the distribution is Maxwellian of the form

$$f(E) = \exp. - [(E-E_o)/kT_h(\varepsilon)] \qquad 3.1$$

where T_h = 'hot' carrier temperature and depends on the instantaneous value of the field at the interface, the doping level, and the 'quality' of substrate which controls the scattering.

E_o = an adjustable energy parameter to give the correct density of electrons in the Si at the interface

The value of the hot carrier temperature T_h controls injections since the larger it is, the higher the tail of the distribution will be. Though it has not been shown, T_h also will depend on the crystal lattice (point defects etc.) since it essentially carries the information about the collective effect of scattering of the carriers through the point of origin to the SiO_2/Si interface.

These carriers will be injected during the period τ_1 in Fig. 3-1(b) which represents the time during which avalanche can be maintained. Note that it ends at the peak of the voltage cycle. This happens because as soon as avalanche sets in, only a small fraction of the generated minority carrier holes get injected into the oxide as shown in Fig 3-1(c), and the remainder begin to form the inversion layer which acts as a shield, reducing the field in the semiconductor. The avalanche field can only be maintained while the magnitude of v was increasing. In the accumulation part of the cycle no carriers are injected since this involves majority electrons which remain in thermal equilibrium with the lattice and hence do not have enough energy to overcome the barrier. The offset voltage was used to keep the oxide field low enough (less than 5E6 V/cm) so that no Fowler-Nordheim tunnelling took place. Hence during the cycle, current flowed only in the avalanche part of the cycle. It was observed and measured as the direct component I_{dc} of the total current.

3.2.2 Trapping

When hot electrons are injected into the oxide, they get thermalised over a very short distance; the scattering mean free path for thermal electrons in SiO2 is about 34 Å (2). While corresponding measurements have not been made for hot holes, 34 Å is the longest mean free path one could logically expect for hot holes. After thermalization, the holes will drift along until they get captured by traps. A trapped carrier will provide a space charge in the oxide and it will cause a shift in the flat band voltage V_{FB} of a high frequency C/V plot. It was this shift that was measured and related to the trap density. Though the mathematical modelling of the trapping process will be discussed later, there are two points that need to be made. The first is that the ΔV_{FB} is proportional to the distance of the sheet charge from the outer gate/SiO_2 interface. Hence an equal sheet charge located near the oxide/Si interface causes a bigger shift in the V_{FB} than the same charge further towards the outer surface.

The other point is that a hot carrier injected into the oxide could have a few eV of K.E. It would lose all of this energy in about 5 to 7 atomic planes. It is likely that this causes the interface to be modified ("damaged") in order to produce both fixed charge (which will be picked up as a ΔV_{FB}) and band gap states D_{it} which will show up in the quasi-static measurement. This generation process is not usually modelled in the mathematics of the trapping process which, as will be shown later,is very important.

The above concepts will now be discussed mathematically to see how they fit with the observed results.

3.3 Experimental Data Associated with Avalanching

3.3.1 Calculation of Carrier Temperature from Dynamic I/v Data

Curve 1 of Fig. 3-2a shows a typical experimental I/v characteristic of a device plotted on a semi logarithmic plot. The same data is also plotted as log I vs $\varepsilon_{ox}^{1/2}$ (curve 2) and as a linear plot of I vs ε_{ox} in Fig. 3-2b. The values of ε_{ox} were calculated using Poisson's equation for the substrate and Gauss's law at the interface. It is quite clear that there are two regimes which describe the situation. The high field (ε_{ox} > 5.7E6 V/cm) is described by a linear dependence and represents the situation in which there is strong avalanching. This situation is analysed by Nicollian and Berglund (3) and the result is given below.

$$J_{dc} = K_o (\varepsilon_{ox} - \varepsilon_B) f.S_o.\exp (-q.\phi_B/k.Tp) \qquad [3.2]$$

where K_o = the product of ϵ_o and the relative permittivity of SiO_2

ε_{ox} = the peak electric field in the oxide resulting from the a.c. signal

ε_B = field in the oxide at the onset of avalanche in the substrate

f = frequency of the applied a.c. signal

S_o = a scattering factor which is given in reference (3)

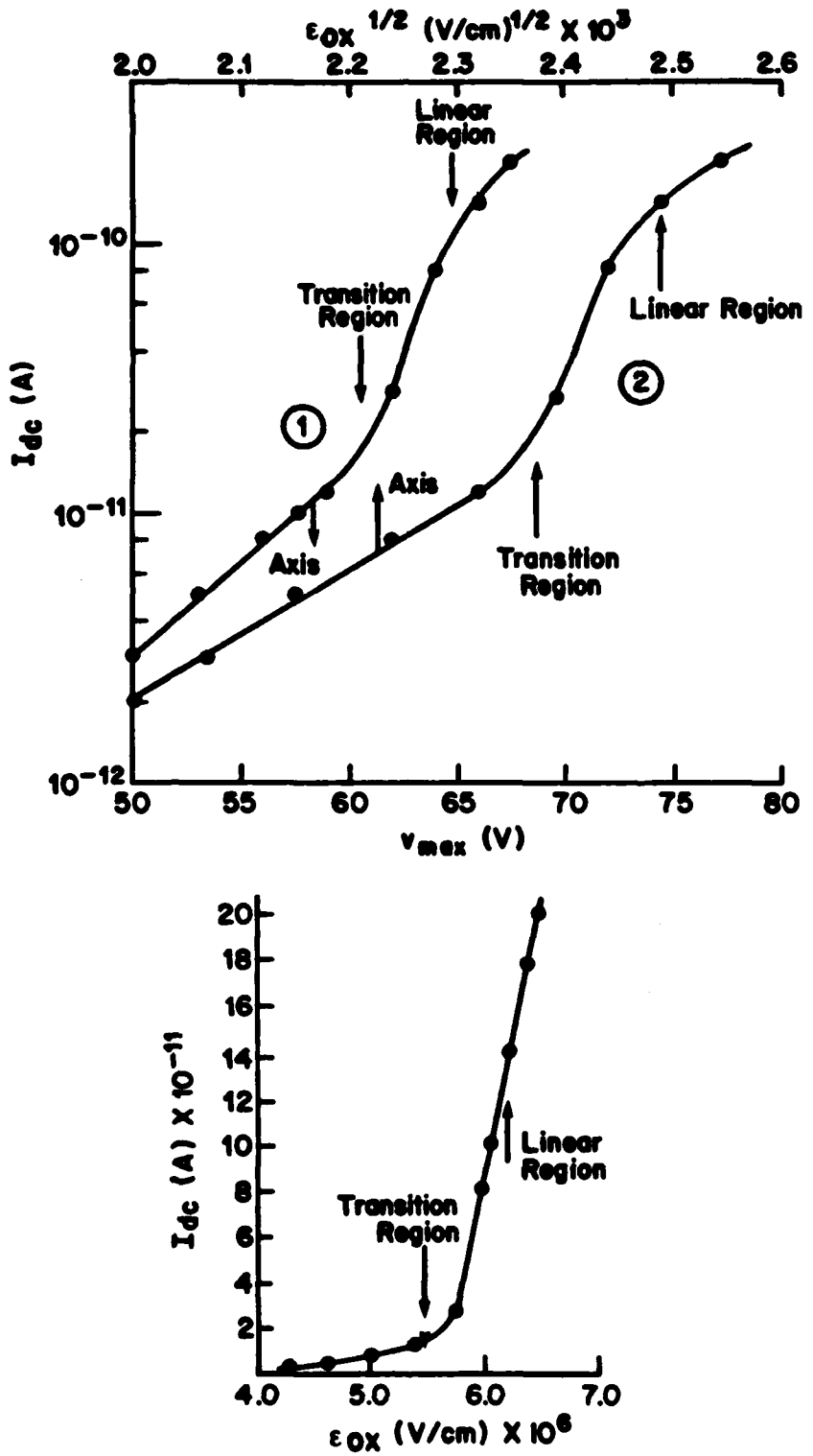


Fig. 3-2 I/v data plotted in different ways for a dot from a wafer oxidized at 1100°C in dry O_2. From these plots, hole temperature are calculated for the two avalanche regimes.

ϕ_B = the barrier height at the Si/SiO_2 interface

Tp = the carrier temperature

From the gradient of the linear portion of the plot of Fig.3-2b, a hole temperature Tp of 1710°K was calculated in comparison with about 5550°K for electrons found by Nicollian et al (3).

At low fields, i.e. below the transition regime, there is a strong field dependence seen and this is due to the low temperature of carriers which make the barrier lowering due to the field more effective in changing the injected current. It is assumed that Schottky emission during this regime describes the situation and is given by the well known relationship:

$$I_G = A\ Tp^2 \exp\left[-\left(\phi_B - \beta\ \varepsilon_{ox}^{1/2}\right)/k.\ Tp\right] \qquad [3.3]$$

where $\beta = \left(q/4\ \pi\ K_o\ \varepsilon_o\right)^{1/2}$ [3.4]

Since I_G is a strong function of the oxide field, which will vary during the cycle, it is assumed that I_G dc is approximately proportional to the instantaneous peak I_G, which will coincide with the peak of the voltage cycle. Using curve 2 of Fig. 3-2a, a hole Tp of 431°K is obtained indicating that indeed in this low field regime the holes are less hot. Ning and Yu (4) have shown in their optically induced dc measurements using MOSFET structures, that this is a valid description. The strong field dependence has also been seen by Card (5), Itsumi (6), and Nicollian et al (7) over 4 to 5 orders of magnitude though these were for electrons.

3.3.2 Effect of Substrate Doping on Avalanche Injection

In order to further confirm that the I/v characteristic is dominated by the avalanche mechanism, data is given in Fig. 3-3 for three different substrates that have been implanted with 200 keV phosphorus ions for doses that are indicated on the figure. Identical oxides of 490 Å were grown on each wafer. From the C/V data, an effective doping concentration N_D was calculated and this was used to calculate the voltage v at which the substrate surface field would reach the avalanche field(8). These points are marked ε_{crit} in the figure and it is seen that they correspond well with the voltage at which I_{dc} begins to increase.

3.3.3 I/v Variation From Dot to Dot Within the Same Wafer

One of the features observed frequently was that, in spite of a rigorous selection procedure which insured that the C_{max} and V_T of the dots within a wafer had a standard deviation σ of less than 5%, the I/v scatter was large even among closely spaced dots. Fig. 3-4 shows I/v data of 3 neighboring dots. These I/v characteristics are vastly different and this is important because (as will be shown in section 4.4.3) a very strong correlation has been found between I/v and the amount of trapping within the same batch. Hence it becomes important to see what controls I/v.

It is seen from the equations above, that there are four parameters, namely N_D, ϕ_B, X_o and Q_{SS}, which control avalanching and injection and consequently, the current I_{dc} in the device. It is important to estimate which one of these factors is likely to be responsible for the variation. The

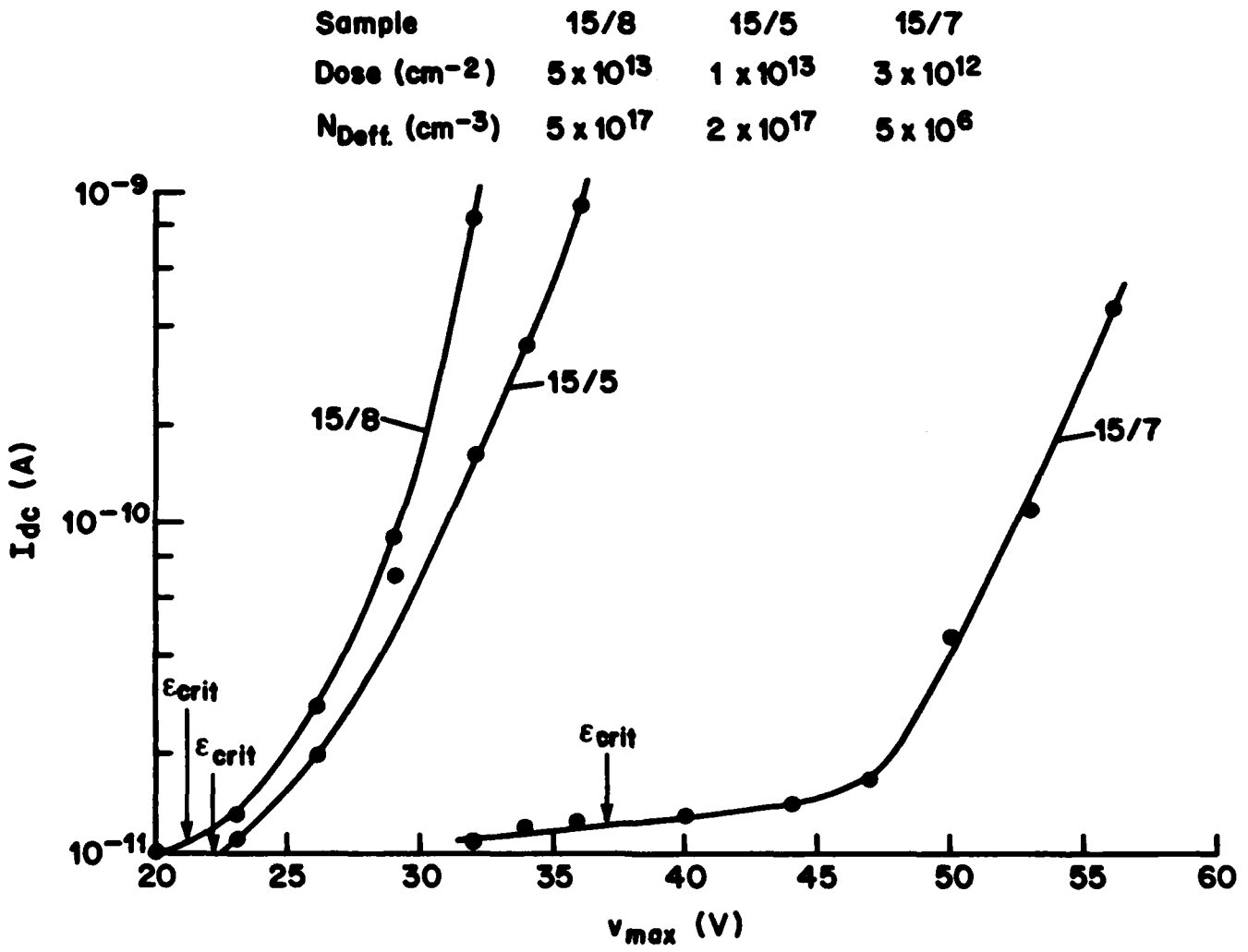


Fig. 3-3 I/v characteristics of devices on wafers implanted with different doses of P^+ ions at 200 keV. Oxide thickness was 490 Å.

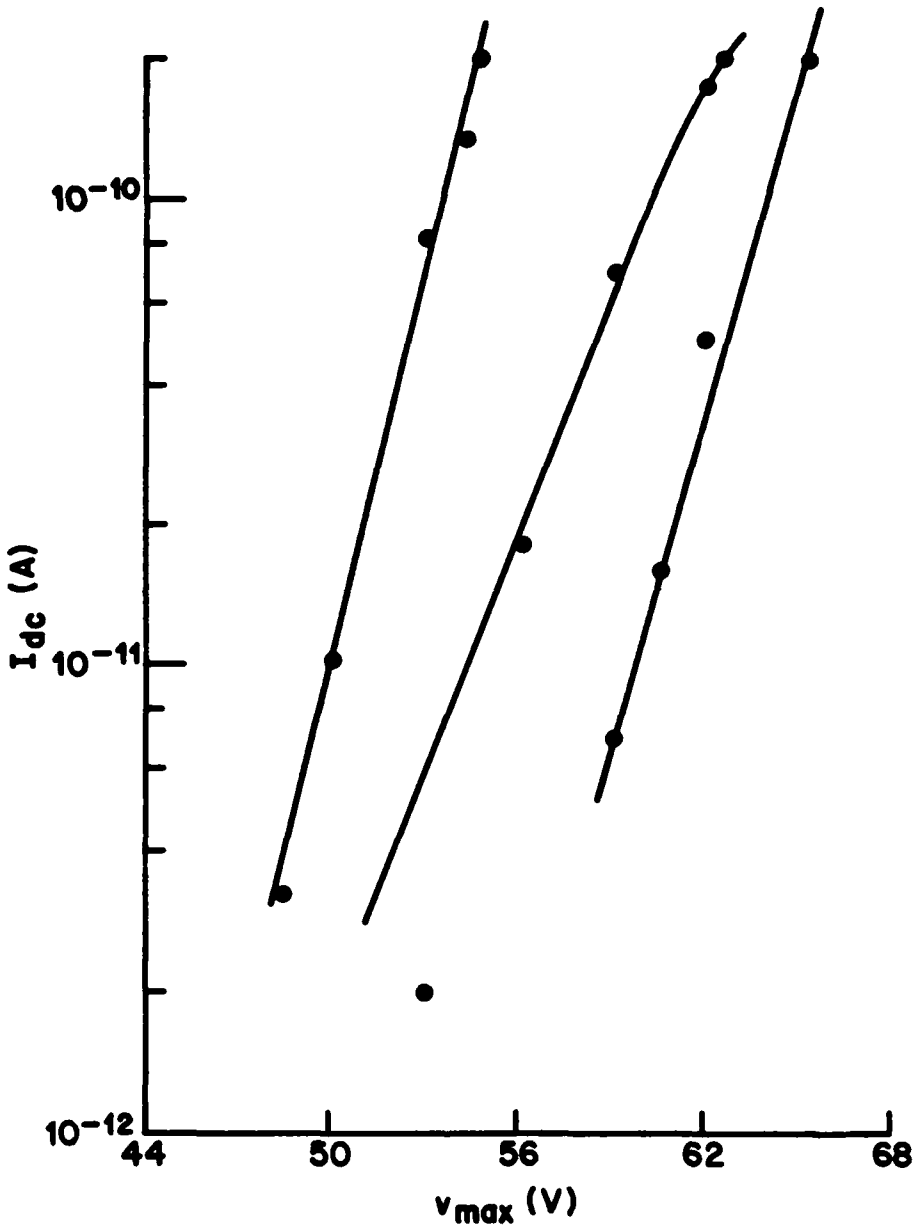


Fig. 3-4 I/v characteristics of three near neighbor devices on the same wafer (TR 104 N3)

approach used was to do a sensitivity analysis, i.e., to see if either the measured or estimated variations in the values of these parameters, could account for the variation in v at 10^{-11} Amps.

C_{max} was used to estimate the value of X_o and found to vary less than 1% among the three dots. This could not account for the approximately 10 V shift in v. Similarly it was estimated that Q_{SS} would need to be greater than 3E12 cm^{-2} before it could begin to influence the oxide field and hence v. Since at the initial stages of trapping, the measured Q_{SS} was less than 1E11 cm^{-2}, this parameter could not account for the observed scatter either.

In estimating the influence of N_D on the voltage at which avalanche would start, the relationship (8) between N_D and the field ε_{crit} was used. ε_{crit} was the field which will cause avalanching. Clearly, ε_{crit} also represents the field at which significant carrier heating takes place. If one were to assume that ε_{crit} only depends on N_D (ε_{crit} is a slowly increasing function of N_D), then one finds that, on the basis of the measured values of N_D (from C/V data), the magnitude of v comes out to be 28 V, and not 50 to 60 v as seen in Fig.3-4. Also the predicted differences among the three dots are going the opposite way from the measured values. This suggests that for these dots, the predominant influence for ε_{crit} does not come from N_D but from some other parameter associated with the substrate. It is proposed that this has to do with the carrier scattering centers which are related to the crystal quality. Qualitative explaination is that as the density of scattering

centers and/or their scattering cross-section increases, for a given N_D, ε_{crit} will also increase, since the mean free path length will go down, so the probability of an electron-hole pair production due to an impact ionization event will go down. Since v increases rapidly (roughly a square dependence) with ε_{crit}, a small localised variation in ε_{crit} due to crystal defects would account for the experimental values. Experimental evidence for this also comes from the paper by Ning and Yu (4) who measured the hot electron temperature Te vs ε_{Si} for different doping level N_A of p-type substrates. It was observed that, at high ε_{Si} and for the higher doped samples, the scatter increased. It should be pointed out that silicon substrate defects were examined under selected dots with Wright etch, but it was not possible to establish any unambiguous correlation. Therefore it is assumed that these substrate defects are at an atomic level.

Finally, it was calculated that at an estimated Tp of 1710°K, the ϕ_B would need to change by 0.35 eV to account for an order of magnitude change in I_{dc} at a given v. This seems too high a variation to be realistic, particularly among closely spaced dots.

Thus the final conclusion reached is that the variations seen in I/v are due to atomic level substrate defects which affect the ε_{crit} and Tp for a given N_D; other parameters, such as Q_{SS}, X_O, ϕ_B and N_D, are unlikely to be responsible for this scatter.

3.4 Experimental Data Associated with Trapping

In this section, the basic equations that describe the

trapping process are given with examples of how trap parameters can be extracted from experimental data. Some experimental data which throws light on the trapping process itself is also given.

3.4.1 Theory of the Trapping Process and Parameter Evaluation

As described before, the model of the trapping process is that hot carriers are injected into the oxide at the oxide/Si interface. They thermalize within a distance of about 30 Å and from then on drift along within the relevant band until they pass within the capture cross-section of a trapping site, and get captured. Notation was chosen to conform to electron capture but they are also valid for holes. This model is expressed in the following derivation. For more details refer to papers (4) and (6).

$$\frac{dnt}{dt} = \text{capture rate} - \text{detrapping rate} \qquad [3.5]$$

$$= v_{th}.\sigma.n_c(N_T - n_t) - n_t.A.\exp(-E_T/kT) \qquad [3.6]$$

where
- v_{th} = thermal velocity of the carriers.
- σ = capture cross-section of traps.
- n_c = density of conduction electrons.
- N_T = density of total traps.
- n_t = density of trapped carriers.
- A = frequency factor.It can also be thought of as the number of attempts the carrier makes to escape from the trap.
- E_T = trap depth

If it is assumed that the capturing process is very inefficient (typically less than 1% of the injected carriers are captured) and that carrier concentration is sufficiently low such that space charge can be neglected, then n_c would be uniform throughout the thickness of the oxide and

$$J_{dc} = q.n_c.v_d \qquad [3.7]$$

where v_d= drift velocity of carriers, and assumed to be the same as the thermal velocity v_{th}

Hence equation [3.5] can be written in terms of the measurable quantity J_{dc} and assuming that the traps are sufficiently deep so that the detrapping term can be neglected, equation [3.6] can be written as

$$\frac{dnt}{dt} = J.\ \sigma./(q)\ (N_T - n_t) \qquad [3.8]$$

The solution of this equation subject to the boundary condition that n_t=Ø at t=Ø, is:

$$n_t = N_T\ [1 - \exp\ (-\ \sigma.N_{inj})] \qquad [3.9]$$

where N_{inj} is the total injected charge at time t and is given by

$$N_{inj} = \int_0^t J/(q).dt \qquad [3.10]$$

However, from the experimental data point of view, equation [3.9] can be manipulated to describe an efficiency factor η , giving:

$$\eta = \frac{dnt}{dN_{inj}} = \sigma .N_T. \exp (- \sigma .N_{inj}) \qquad [3.11]$$

If it is assumed that all the n_t distributed throughout the bulk of the oxide reflects in an effective charge located at the interface then

$$n_{eff} = C_{ox}. \Delta V_{FB}/(q) \qquad [3.12]$$

Note that n_{eff} is a sheet charge whereas n_t is a volume charge concentration. As shown by Itsumi (6), it is possible to estimate experimentally whether the charge is located at the interface or uniformly within the bulk by doing measurements with different oxide thicknesses.

Therefore equation [3.11] becomes:

$$C_{ox}/(q) \frac{d\Delta V_{FB}}{dN_{inj}} = \sigma .N_T. \exp (- \sigma .N_{inj}) \qquad [3.13a]$$

Or for constant J and using equation [3.10]

$$\frac{d\Delta V_{FB}}{dt} = \sigma .N_T. J./(C_{ox}) \exp (- \sigma .J.t/q) \qquad [3.13b]$$

In trapping analysis, this is a key equation since both ΔV_{FB} and J are experimently determined. A plot of $\ln d\Delta V_{FB}/dt$ vs t allows both σ and N_T to be calculated and these two parameters characterize the trap.

At t = 0, when $n_t = 0$, and using equation [3.8] or [3.13b],

$$d\Delta V_{FB}/dt = J.\sigma.N_T/C_{ox} \qquad [3.14]$$

Since both $\frac{d\Delta V_{FB}}{dt}$ and J are experimently determined, it is possible to calculate the product $\sigma.N_T$ of the dominant trap. This product represents the overall trapping effectiveness or 'potential' of the trap, and it is an excellent parameter to characterize the trapping features of a particular oxide. It also has the advantage of being measured easily, since it is the initial gradient of the ΔV_{FB} versus t curve.

Another way of looking at $\sigma.N_T$ is to realize that its dimensions are that of L^{-1}, i.e., its reciprocal has dimensions of length. The larger the value of $\sigma.N_T$ the shorter this length, which can be thought of as the mean free path of a carrier before it is trapped. Though the value of $\sigma.N_T$ would be excellent for characterizing traps in an oxide, for the sake of consistency with the earlier report (1), ΔV_{FB} at 2000 sec was used to describe the trapping characteristics of the experimental oxides. At 2000 sec, N_{inj} is large enough such that n_t approaches its saturation value N_T, as suggested by equation [3.9]. If saturation is achieved, ΔV_{FB} should be proportional to N_T and it should also proportional to $\sigma.N_T$ or $\frac{d\Delta V_{FB}}{dt}$ at t = 0. As will be shown later in section 3.4.2, this was always found to be true for the results obtained.

It should be noted that equation [3.6] does not model the

possibility that charge states, e.g. surface or bulk oxide states could actually be created due to the impact of energetic carriers as they hit the interface and get thermalized within a few atomic planes. Work mentioned in the previous report (1) and that of Itsumi (6) have clearly shown that the measured charge is a function of I_{dc}, i.e., as I_{dc} increases, more positive charge is seen. These workers have speculated that this charge arises either because the trapping cross-section σ depends on I_{dc} or ε (which goes up with I_{dc}), or because charge flux creates Q_{ss}. On balance, the latter is favoured since an increase in D_{it} is definitely seen from quasi-static measurements.

3.4.2. Application of the Trapping Equation to Calculate Trap Density N_T and Trapping Cross-Section σ

The application of equation [3.13b] to calculate N_T and σ for a typical sample is given here. Fig. 3-5 shows results of two samples whose details are given in the caption. Sample N16/1 (3,4,5) was different from sample N16/7 (4,4,3) only in that the former substrate had a sacrificial oxidation prior to gate oxidation which was identical for both. The most significant difference is that the sacrificial sample shows two traps whereas only one is seen for the sample without sacrificial oxidation.

The product $\sigma.N_T$ was also calculated and as can be seen in Fig. 3-6, it varies monotonically with ΔV_{FB}. Each point on this graph represents a different device. As explained in section 3.4.1, this is a strong correlation. Other experiments

Calculated Data

Sample	σ_1 (cm^{-2})	N_{T1} (cm^{-3})	$\sigma_1 N_{T1}$ (cm^{-1})	σ_2 (cm^{-2})	N_{T2} (cm^{-3})	$\sigma_2 N_{T2}$ (cm^{-1})
N16/1 (3,4, 5)	5.3×10^{-15}	2.5×10^{12}	1.3×10^{-2}	1.4×10^{-15}	2.7×10^{12}	3.8×10^{-3}
N16/7 (4,4, 3)	2.5×10^{-15}	2.1×10^{12}	5.3×10^{-3}	—	—	—

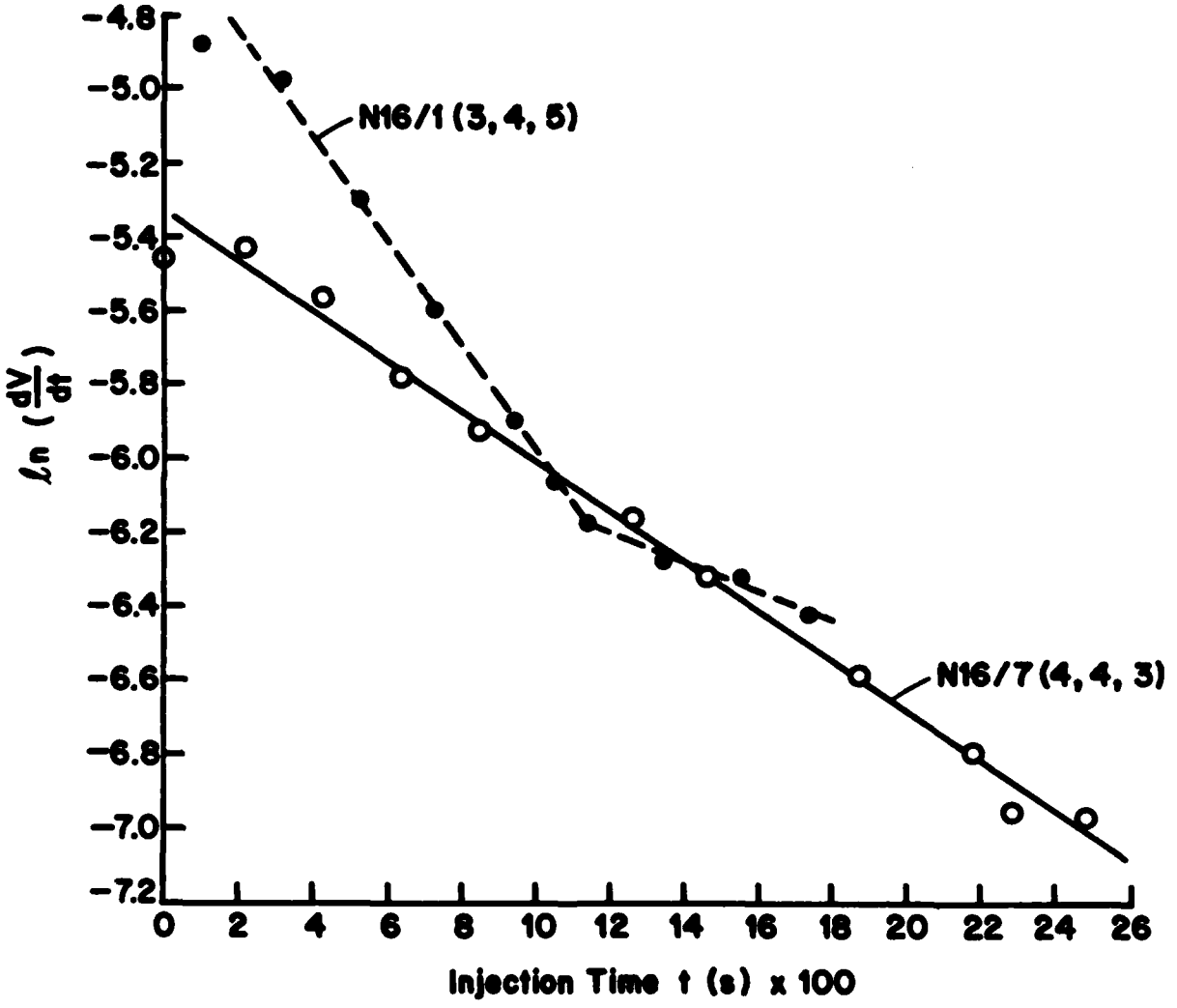


Fig. 3-5 Trapping data shown in a form that allows σ , N_T and $\sigma.N_T$ to be calculated.

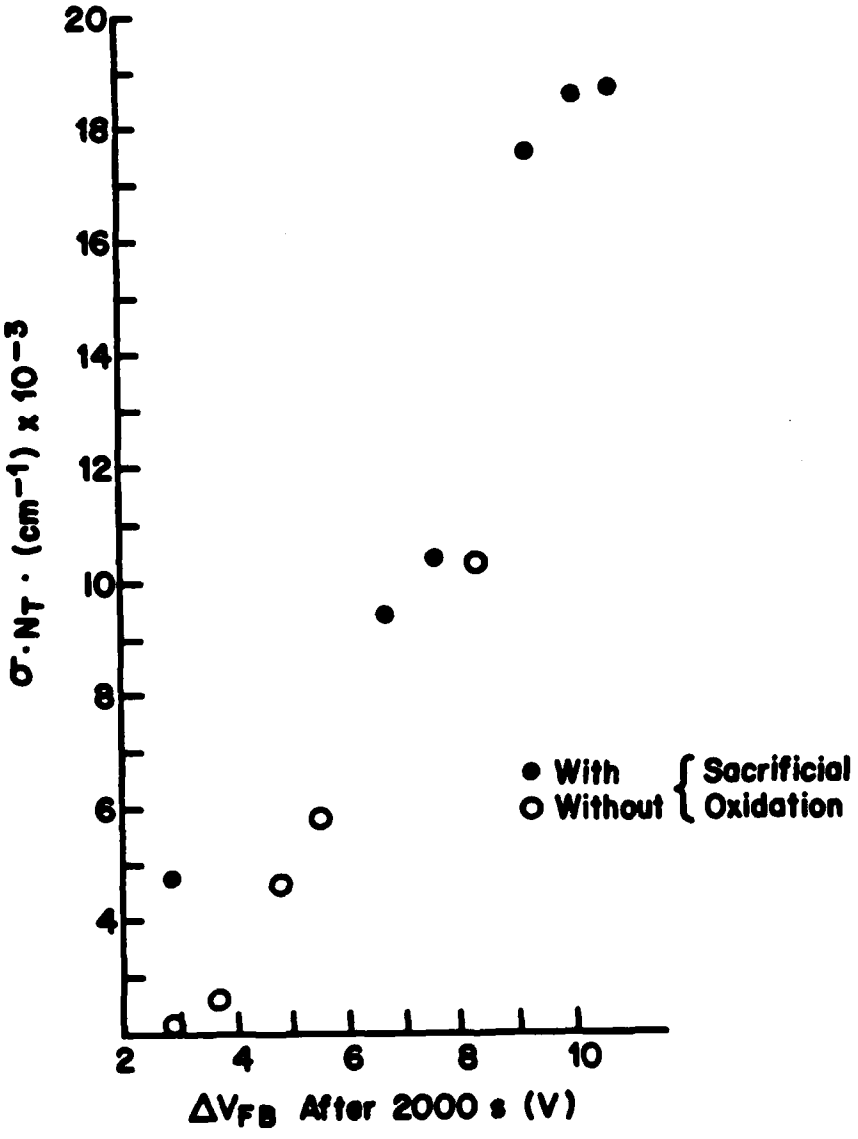


Fig. 3-6 Variation of ΔV_{FB} (2000 sec) with the parameter $\sigma.N_T$. Each point represents a particular device and data from six different wafers is given.

showed a similar correlation. Hence ΔV_{FB} (2000) will be used as a measure of $\sigma.N_T$ of an oxide which, as had been explained, represents the trapping 'potential' of the oxide.

3.4.3 Correlation Between Avalanche a.c. Voltage v and Flatband Voltage Shift ΔV_{FB} (2000 sec)

Fig. 3-7 shows the relationship between v and ΔV_{FB} for the two sets of samples. Group (a) were samples which had sacrificial oxidation and the group consists of three wafers which were oxidized at 900, 1000 and 1100°C respectively. Group (b) were oxidized under identical conditions but no sacrificial oxidation was given to the wafers prior to gate oxidation.

As can be seen, a strong correlation exists between v and ΔV_{FB}. A similar effect was seen by Itzumi (6) who found that above a certain threshold value of I_{dc}, the ΔV_{FB} became a reducing function of I_{dc}, i.e., with their electron injection, they had to account for an increased positive charge. The strong dependence of I_{dc} and v has already been mentioned in section 3.3.1. Therefore the two sets of results are consistent.

The implication of this result is very important since it suggests that at least part of the measured trap charge (as seen by ΔV_{FB}) is due to the energy of the injected charge and <u>not due</u> to the trapping characteristic of the traps within the oxide. A possible explanation is that the carriers generate positive traps whose generation kinetics depends on v (or equivalently on energy distribution of the incident carriers). Since an increase in D_{it} due to injection is seen, this

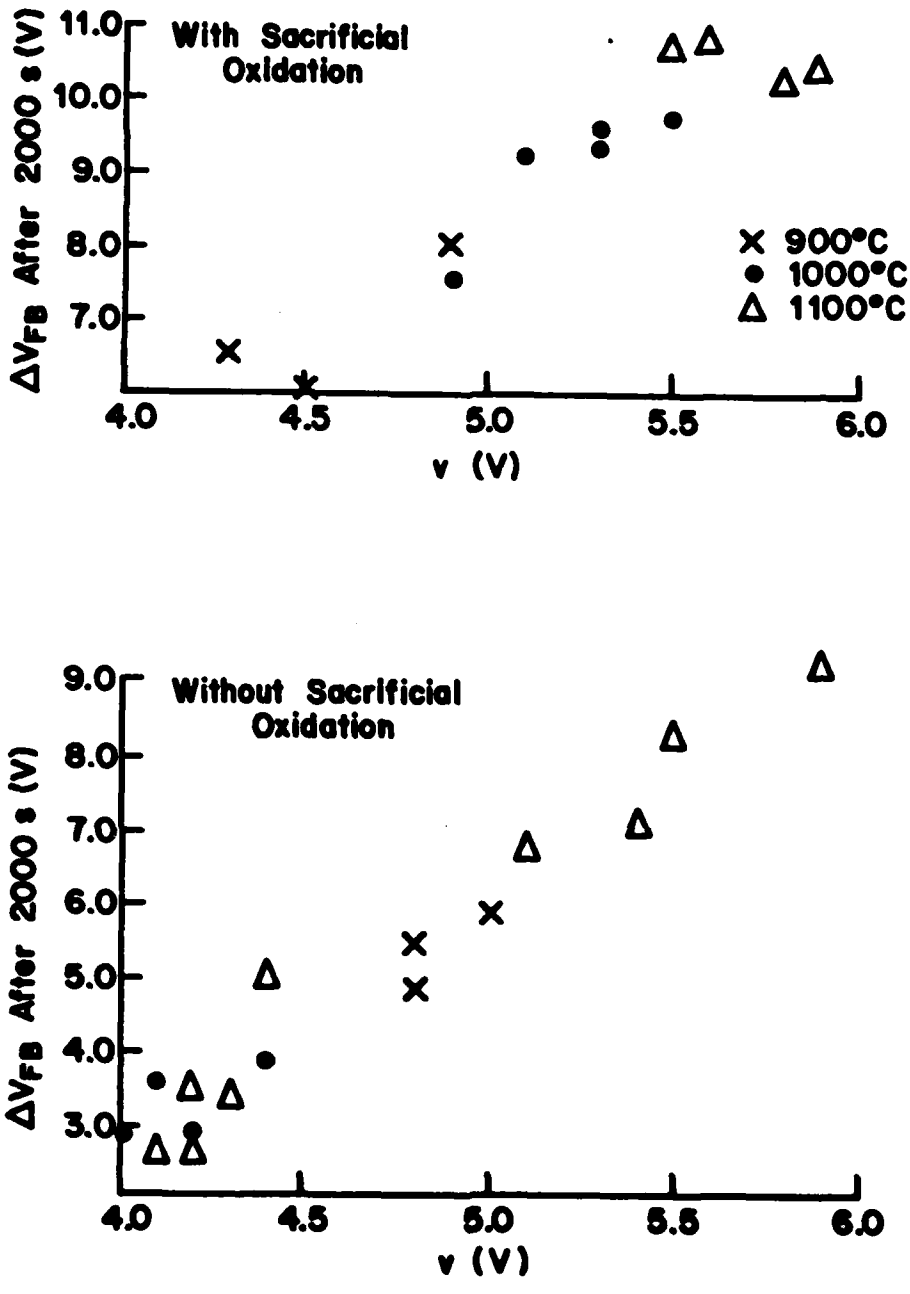


Fig. 3-7 Relationship between v (oscillator output before amplification) and ΔV_{FB} (2000 sec) shown for wafers with and without sacrificial oxidation prior to gate oxidation. Each dot on this figure represents one device and devices from wafers oxidised at different temperatures are shown.

explanation is very likely. On the other hand, since it is seen that the basic trapping equation [3.5] still applies even though it does not allow for continuous generation of traps during trapping; the only way this can be compatible is if the traps were generated rapidly, i.e., in a time small compared to the total trapping time. As will be seen later, ΔV_{FB} was found to be dependent on the growth conditions of the oxide as well as the substrate heat treatment. Hence the conclusion must be that the trap generation also depends on these variables. It should also be remembered that since the injected carriers get thermalized within a distance of about 30 Å from the SiO_2/Si interface, then the new traps must also be close to the interface.

3.5 Summary of the Chapter

In this chapter, the equations that describe the avalanching and the trapping processes were given. It was shown that for avalanching there are two regimes. One of weak and the other of strong avalanching; the former giving a lower carrier temperature than the latter. In the weak avalanche regime, the injected current I_{dc} is a very strong function of v whereas for strong avalanching the dependence is weak. It was proposed that avalanching not only depends on ε_{Si} and N_D but also on the 'scattering centers' of the carriers which depend on the crystal quality. It is the spatial variation of this parameter within wafers which explains the large scatter in I/v characteristics of dots within the same wafer which is observed quite frequently.

The trapping equation [3.13b] was seen to apply, and one

could calculate σ and N_T from it. However it is suggested that the product $\sigma.N_T$ is a good parameter which characterises the trapping `potential' of an oxide and it can be calculated from the initial $d\Delta V_{FB}/dt$ using equation [3.14]. It was then shown that $\sigma.N_T$ was strongly correlated to ΔV_{FB} (2000), and therefore the latter parameter was used to characterise the oxide as was done in the previous report.

A very significant fact has emerged in the correlation between ΔV_{FB} and v, even where there is no variation in I_{dc}. This was explained on the basis of rapid trap generation during avalanching. The trap generation would depend on the hole temperature and hence on v. Consequently, one needs to be very careful in interpreting ΔV_{FB} data, since it may be reflecting two different phenomenon , namely trapping and trap generation. In order to eliminate the trap generation mechanism, the trapping should be done at a v that is low enough that N_{inj} vs ΔV_{FB} becomes independent of I_{dc} or v.

CHAPTER-4

4.0 EXPERIMENTAL PROCEDURE

All data was taken on MOS structures with poly-Si gate circular dots of nominal diameter of 30 mils (750 μm).

4.1 Sample Preparation

Wafers were cleaned in hot sulphuric acid, acqua regia, 10:1 DI:HF acid and isopropyl alcohol followed by N_2 blow dry after a final DI water rinse. DI water rinse was given after each of the chemical treatments. The wafers were immediately oxidized in the appropriate furnace which was a hot wall resistance heated system with single wall tube. For dry oxygen, the gas was derived from liquid oxygen and for the pyrogenic steam oxidation O_2/H_2 were used, again from liquid sources.

Prior to poly-Si deposition the wafers were cleaned in acqua regia, sulphuric acid: hydrogen peroxide, followed by acqua regia and DI rinse.

A poly-Si layer of 0.6 μm thickness was deposited in a LPCVD system at 625 °C with an in-situ HCl clean prior to deposition. Pure silane was used. The layers were phosphorus doped using $POCl_3$ at 950°C. Next 0.5-1.0 μm thickness of Al-4% Cu-2% Si was deposited. The dots were then formed using photoresist (AZ 1350-J) and wet chemical etching techniques. Finally the oxide from the back was removed by wet etching while protecting the front surface using photoresist. A 0.3-0.5 μm layer of Al was

then deposited at the back for forming ohmic contacts. This was accomplished by a 20 minute anneal in 10% H_2/N_2 (forming gas) at 400 °C.

There were some experiments done for which there was a variation in the above procedure. These will be indicated at the appropriate sections in the report.

4.2 Trapping Measurements

These were done in a way which was identical to that described in the earlier report (1). Fig. 4-1 shows the experimental set up during the minority carrier charge injection into the MOS structure.

In the measurement system, the experimental configuration of Fig. 4-1 was part of a computer controlled feedback loop in which the rectified current I_{dc} was monitored every 1/3 sec and was kept at a constant level by adjusting the amplitude of the a.c. applied voltage. Every 70 sec the process was stopped and the V_{FB} recorded by taking a C/V plot on the device. The shift of V_{FB} from the original value, i.e., before the start of the trapping cycle, was recorded as a function of the total injection time. At a constant injection current, the time axis would be proportional to the injected charge. A typical result is shown in Fig. 4-2.

4.3 Selection of Devices: A Screening Procedure

There were two concerns when the trapping measurements were

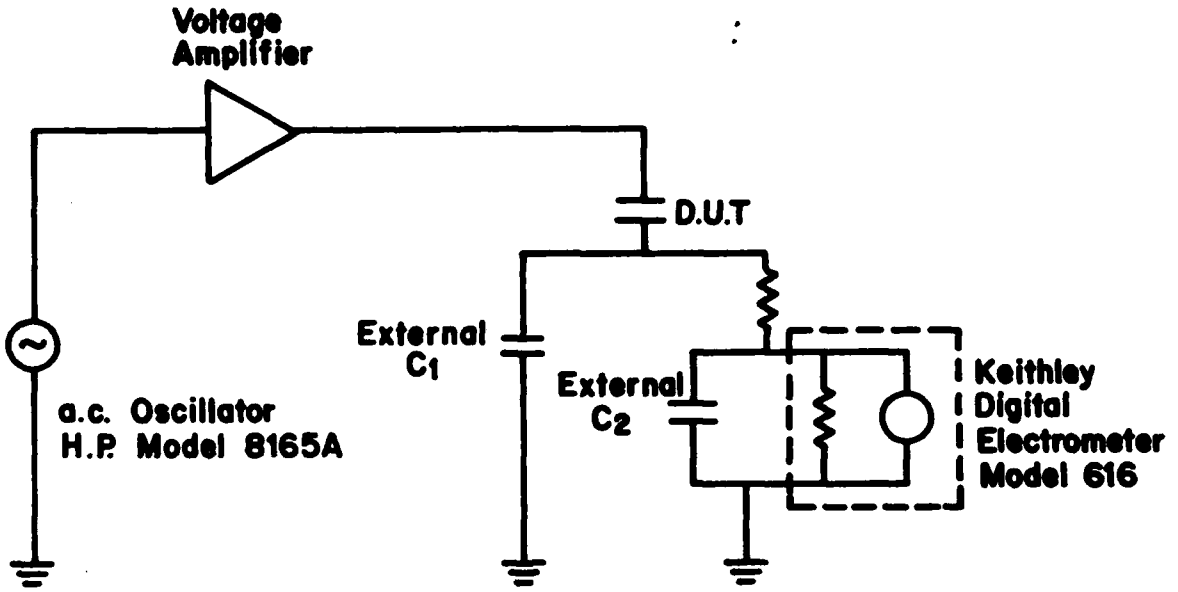


Fig. 4-1 The circuit used for avalanche injection.

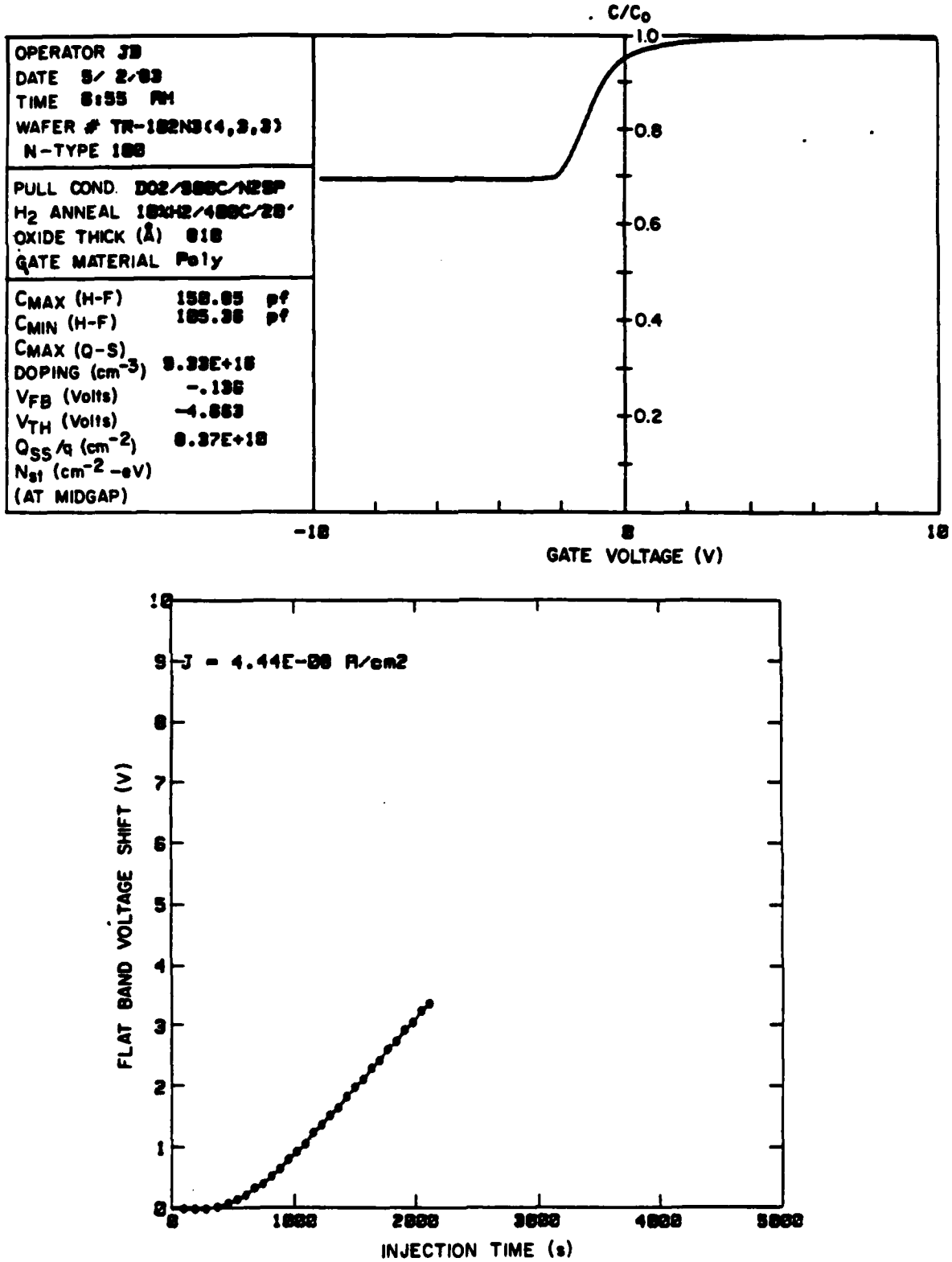


Fig. 4-2 A typical plot of the normalised C/V measurement and avalanche experiment from the computer controlled system.

begun. One was that there would be considerable variation in the ΔV_{FB} from device to device within the same wafer. Secondly, some devices would not last the 2000 sec of injection time which was the standard testing time.

Hence a range of experiments were carefully planned at the beginning of the program to work out a screening and selection procedure for devices such that a device

1. would be representative of the wafer
2. would have a good probability of surviving the test.

The main conclusions of these experiments are briefly discussed below.

1. C_{max} and V_T of the devices within a wafer were a good parameter to estimate the scatter for a wafer. The `out of tolerance' dots were removed by calculating the standard deviation σ and then excluding the dots outside $\pm \sigma$ of the original measurement. If the new σ was still greater than 5%, then the sample was rejected as being too non uniform.
2. The rectified current I_{dc} vs the ac voltage v of the oscillator could also be recorded (referred to as the I/v characteristics). This was found to be a good measure of whether the device would survive the test as well as to see if the sample was representative of the population. It was empirically decided that the three dots measured for trapping would have an I_{dc} at a given voltage (4.75V: unamplified oscillator voltage) within a factor of 1.5 of each other, and

that I_{dc} would be below a certain value (7E-11 A in this case). Higher I_{dc} devices had a very high probability of breakdown.

CHAPTER-5

5.0 RESULTS

The results will be reported in three sections as indicated below:

1. Trapping data on oxides grown under different oxidation conditions.
2. Effect of sacrificial oxidation of the substrate on the trapping characteristics of the subsequently grown oxides.
3. Effect of doping (diffused or implanted) of substrates on trapping for on-chip monitoring.

5.1 Trapping Data on Oxides Grown Under Different Oxidation Conditions

5.1.1 Experimental Variables

Given below are the list of the experimental variables that were investigated.

Substrate	<100>, 0.2-0.4 ohm-cm, n-type, manufactured by Fairchild.
Gates	Poly-Si, phosphorus doped, 0.6μm thick, 30 mils diameter.
Oxide	Nominal oxide thickness of 800 Å .
Growth Temp.	900 , 1000 , 1100 °C.
Growth Ambient	Dry oxygen and pyrogenic steam.

In-situ anneal and pull conditions after oxidation:

For dry oxidation: 4 different variants were tried which are given below.

O_2FP^*, O_2SP^*, N_2SP and ArSP.

For wet oxidation: 3 different variants were attempted which are given below.

H_2OFP, N_2SP and ArSP.

Hence this experiment involved 3x7 i.e. 21 different wafers.

Post gate formation anneal: all wafers had an anneal which consisted of

20 min in 10% H_2/N_2 at 400°C.

* FP = fast pull i.e. 1-3 sec, SP = slow pull i.e. 2-10 min

5.1.2 Results of Trapping Measurements and some General Comments

These wafers were divided into 4 quadrants after the processing was complete. On one piece, the trapping measurement was done using the screening procedure described in section 4.3. The other piece was sent off to NRL for radiation measurements. The last two pieces were kept for any future work, e.g., to investigate repeatability.

Typically, two to three dots were trapped on each wafer unless a large scatter was found (in spite of the stringent

screening procedure) or the results were unexpected. Results of this data are shown in Fig. 5-1a and b for dry oxidation and pyrogenic steam respectively. Fig. 5-2a and b also show results of Al gates obtained from the previous report (1). The figures plot average ΔV_{FB} (2000 sec) of trapping verses oxidation temperature for the various pull conditions. The data is shown in this way to preserve consistency with the previous report(1).

First some general points about these figures. Out of the seven conditions tested, three of them have a non-monotonic variation of ΔV_{FB} with temperature. In every case where this happens it is because no trapping is seen i.e. ΔV_{FB} is 0 for a wafer in that group. As indicated in section 3.1, a possible reason for this is electron injection from the gate electrode to annihilate the trapped holes. Hence these points must not be interpreted as good trap free oxides. Since from the previous work with Al gates, which are also shown in Fig. 5-2a and b, these points were not observed, it would appear that a poly-Si gate is more likely to inject electrons than an Al electrode. This in fact was found to be the case in samples for which d.c. I/V data was taken for both polarities on MOS devices with Al gates. As expected Fowler-Nordheim tunnelling was seen but typically when electron injection was from the Al gate, the current for the same field was 2 to 3 orders of magnitude lower than for the case where electron injection was from the silicon substrate.

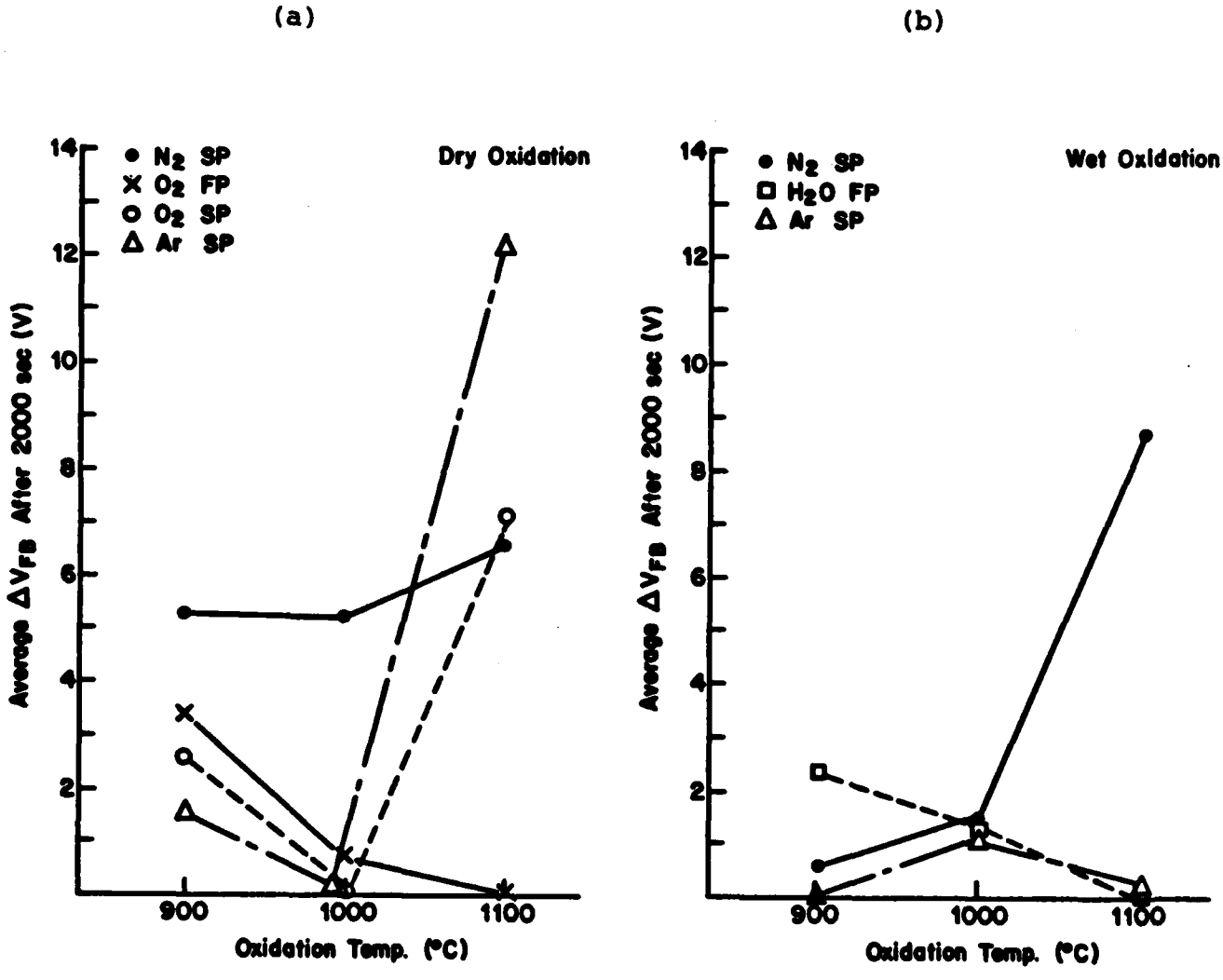


Fig. 5-1 a and b

The variation of ΔV_{FB} with oxidation temperature for dry and wet oxides with various post oxidation pull conditions. The devices had poly-Si gates.

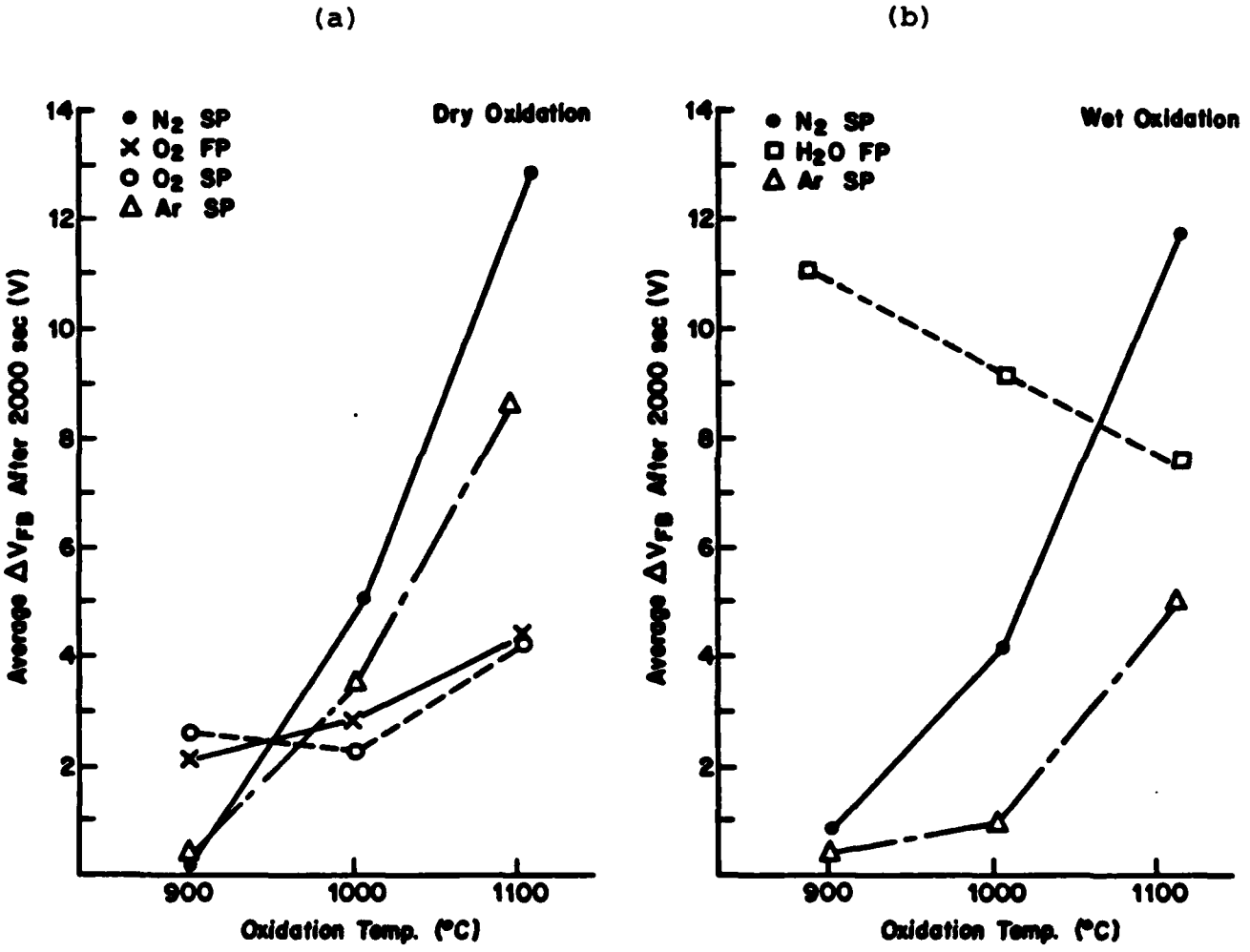


Fig. 5-2 a and b

This data is from reference 1 for which growth and anneal conditions were the same as for Fig. 5-1 samples except that the gate was Al.

As indicated in the description of the screening procedure, the dots were closely spaced and typically two to four were trapped within the same wafer. Even so, large variations in ΔV_{FB} were sometimes found. Neglecting the dots whose V_{FB} did not shift, range of ΔV_{FB} (for some wafers) as a percentage of mean varied from 30% to 130%. This is reflected in the variation of I/v characteristics of the devices as discussed in section 3.3.1. It is for these reasons that it should be emphasized that the results shown in Fig. 5-1 should not be treated as being entirely characteristic of the oxide. The discussion in section 3.4.3 suggests that they are affected by the energy distribution of the hot carriers, which in its turn would be dependent on the substrate quality.

5.1.2.1 Dry Oxidation

If one were to neglect the results at 1000 °C for which it was found that for 2 of the 4 samples, namely for O_2SP and ArSP there was no shift in V_{FB}, one sees that between 900 °C and 1100 °C, all samples have an increase in ΔV_{FB}. The exception was in the case of O_2FP for which the 1100 °C samples again did not shift. These results are similar to the case of the Al gate. The similarity suggest that the effect was predominantly due to the way that the oxide was grown. It has been reported that a high temperature oxide results in a greater level of strain due to the thermal expansion mismatch between the oxide and the silicon substrate. So this could account for the increase in ΔV_{FB} with temperature. However, like the samples quoted in section 3.4.3 there was good correlation

between v and ΔV_{FB} for these wafers. This suggests that a contributory factor in the V_{FB} shift is the injection characteristics of the `hot' holes. In other words, under these conditions of trapping, the trap charge is not just due to the intrinsic oxide but is being created by the hot carriers. This generation process would also depend on the total heat treatment, including the oxidation condition that the wafer is subjected to. A comparision of these results with that due to radiation induced holes would clarify which of the two mechanisms is predominating, since in that situation the holes would not be as energetic and the results would truly reflect the oxide traps. The overall conclusion from this data is that for lowest trap levels, the oxide should be grown at low temperatures and annealed in Ar.

5.1.2.2 Wet Oxidation

As with the dry oxides, one sees that N_2SP increases ΔV_{FB} with temperature. On the other hand, for steam anneal, the opposite is true. It was also seen that for N_2SP annealed samples, the value of ΔV_{FB} increases with v for different dots within the same wafer. This is the same as for dry oxides. However, it was found that the relationship between ΔV_{FB} and v goes in the opposite sense for steam annealed sample, i.e. as v goes up, ΔV_{FB} goes down. This suggests that the nature of the traps of the two post oxidation anneals is different, and the obvious difference is the water content of the two oxides. There are reports in the literature that suggests that water related traps do exist (see section 11.5.1 of reference 9).

Thus N_2 anneal has the effect of drying the steam oxide to give trapping characteristics similar to those of dry oxides.

Neglecting the result for 1100°C for H_2OFP and ArSP, since no shift was seen, again the conclusion was that the lowest traps were seen for lower temperature oxides.

5.2 Effect of Sacrificial Oxidation of the Substrate on Trapping Characteristics of Oxides Subsequently Grown

The results of section 3.4.3 showed evidence that the substrate heat treatment could have a substantial effect on the trapping characteristics, i.e., on ΔV_{FB}. This was seen on the basis of a strong correlation between v and ΔV_{FB}.

An experiment was designed to assess the substrate effects by keeping the oxidation conditions the same but to vary the substrate structure by giving it a sacrificial oxidation prior to gate oxide growth. By substrate structure is meant those structural properties near the Si surface which would affect avalanche multiplication and scattering of carriers within the depletion region during avalanche injection. These structures could be related to stacking faults, metallic impurities creating deep levels, oxygen precipitates or any other structural feature which would affect the energy distribution of the minority carriers as they are injected into the oxide.

In preparing the samples, all processes were the same as before (section 4.1) except for those listed below:

Oxidation Nominal thickness of oxide was 800 Å , dry O_2, O_2SP.

Growth temp. 900 , 1000 and 1100°C.

Sacrificial oxidation

1100 °C for 8 hours in dry O_2 in a mullite lined furnace giving about 0.4 μm oxide thickness.

A control batch was also generated which did not undergo the sacrificial oxidation treatment.

5.2.1 Results of Trapping

Typically four to six dots were trapped from each wafer. The results of the average value of ΔV_{FB} (2000 sec) for the different oxidation temperatures for both experimental and control batches are shown in Fig. 5-3.

It is quite obvious that sacrificial oxidation has a significantly increased trapping . However, again there was very good correlation between v and ΔV_{FB} (see section 3.4.3). Hence it was found that for every case at a given temperature, v for sacrificial oxidation samples were larger than for controls which reflects in the larger ΔV_{FB} for the former.

It was also observed that the samples with sacrificial oxidation had a much tighter ΔV_{FB} for the dots over each quadrant, than controls. Two control samples had a significantly wider variation in the ΔV_{FB} values between the segments within the wafer. Hence sacrificial oxidation has the effect of making the substrate spatial uniformity better even though it apparently creates an oxide that has larger trapping.

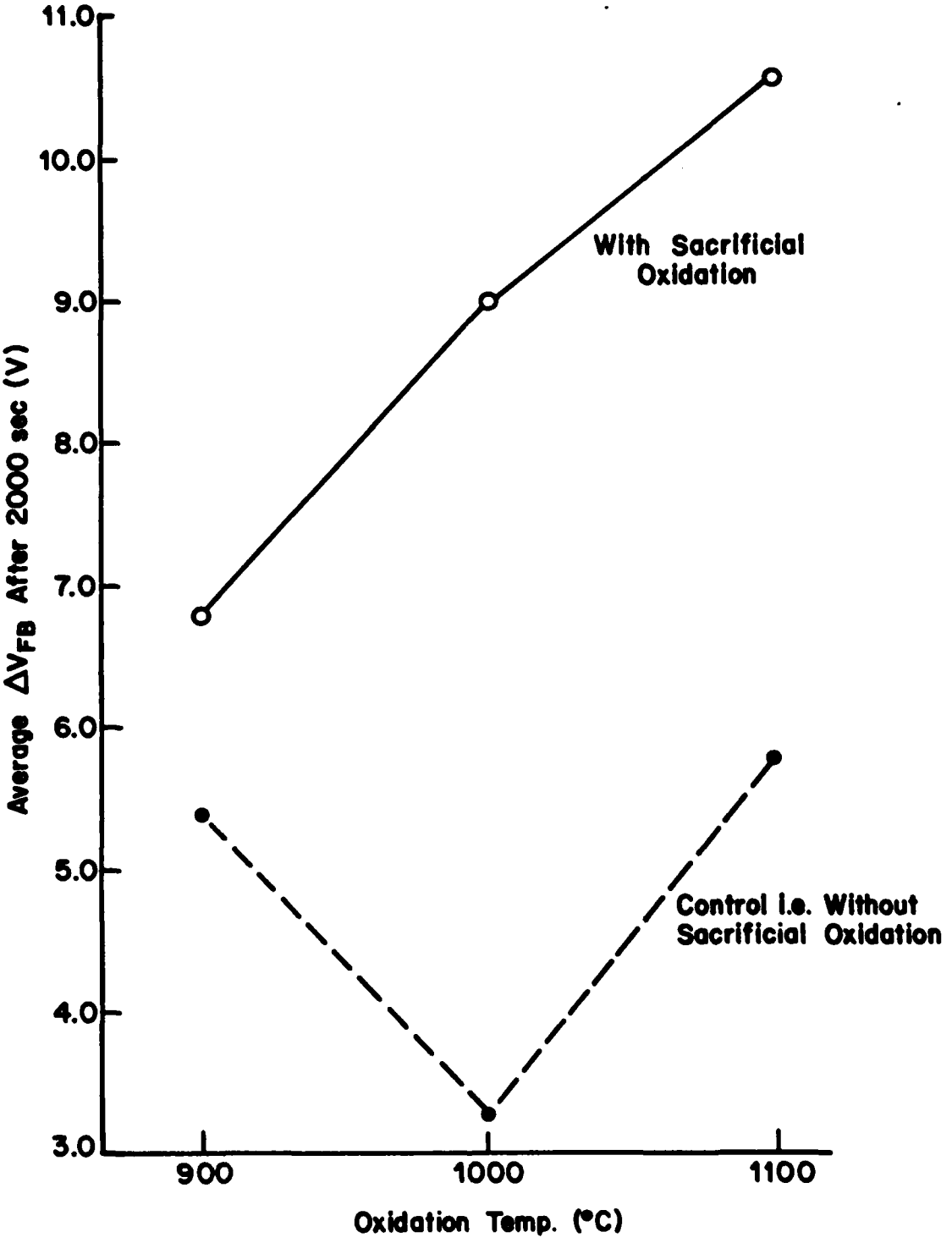


Fig. 5-3 The effect of sacrificial oxidation on the trapping characteristics of subsequent oxides grown at three different temperatures.

However, the close correlation between v and ΔV_{FB} suggests strongly that ΔV_{FB} is more influenced by substrate than the quality of the oxide.

The model that is emerging from this experiment is that the sacrificial oxidation `primes' the surface of the Si by controlling the out diffusion and precipitation of O_i which affects such surface structural parameters as oxidation induced stacking faults. Subsequently, when the thin oxide is grown on this primed surface, depending on the oxidation conditions (temperature in this case), the hot carrier generation is affected. This is reflected in the v value and the implied energy distribution of the injected carriers. The flat band shift then reflect the way in which these carriers create the traps at the interface. It should however be noted that the creation of these traps would not only depend on the energy distribution of the injected carriers but also the `quality' of the interface and that would be dependant on the way the oxide was grown and annealed. This would include any Si surface structure that became incorporated in the oxide when it was formed. Thus it would appear that the substrate and its annealing history play an important role in the trapping characteristic of the subsequent oxide. Further evidence of the effect of heat treatment on substrate quality is provided by an experiment in which wafers of two different manufacturers were examined. It was observed that Fairchild wafers which are used in this experiment, gave precipitates <u>immediately</u> after the first high temperature oxidation indicating that they already

have had a nucleation treatment. On the other hand, the wafers from another manufacturer had to go through a low temperature nucleation anneal before precipitates could be formed.

5.3 Effect of Doping of Substrate (Ion Implanted or Diffused) on Oxide Trapping

The main reason for doing these experiments was to see if it would be possible to dope the substrate to an adequate level for avalanching (typically about 1E17 cm^{-3}) so that the trapping characteristics of the oxide grown on it can be evaluated. This would allow an 'on-chip' monitoring of the oxide quality to be carried out, even on substrates which are typically of much lower doping level than indicated above.

Phosphorus was introduced into the surface both by diffusion from a phosphine source as well as by implantation. All the wafers also had a sacrificial oxidation treatment. Since the trend in VLSI technology is towards lower gate oxide thickness, this was reduced to 500 Å from 800 Å. Processing details are given below:

5.3.1 Process Details:

Wafers: Wafers that were diffused and implanted were 4 in. diameter, 2-4 ohm-cm., n-type <100>; Control wafers were 0.2-0.3 ohm-cm.

Sacrificial Oxidation:

All wafers had a sacrificial oxidation under conditions identical to those reported in section

5.2, and this was completed before any doping was done.

Doping:

Phosphorus Diffused Samples

This was done using a phosphine/oxygen gas mixture at 700°C. After deglazing, the layer was driven-in at 1000 °C for 30 min in dry O_2. Two different source/soak cycles were tried. It was estimated on the basis of ρ_s measurement and diffusion coefficient of phosphorus (Ishikawa(10)), that the first set had a surface concentration Cs of 1.8E17 cm^{-3} and second of 3.3E17 cm^{-3} after final gate oxidation.

Ion Implanted Samples

These were implanted with P^+ ions at an energy of 200 keV through a thermal oxide of 200 A to avoid any channeling. Doses of 3E12, 1E13 and 5E13 cm^{-2} were tried. These would give peak concentrations of 5.4E16, 1.8E17 and 9.2E17 cm^{-3} respectively after anneal and final gate oxidation. These were calculated on the basis of projected range R_p and standard deviation σ estimates from Gibbons et al (11) and diffusion coefficient values of Ishikawa et al (10). Table 5.1 shows these estimated values and compares them with the effective doping

Wafer	Doping Type	Measured Concentration (cm^{-3})	Calculated Concentration (cm^{-3})
N 15/1	Diffused 3/10 Cycle	$0{\cdot}7\text{-}1{\cdot}0\times10^{17}$	$1{\cdot}8\times10^{17}$
N 15/3	Diffused 10/30 Cycle	$1{\cdot}8\text{-}2{\cdot}5\times10^{17}$	$3{\cdot}3\times10^{17}$
N 15/7	Implanted $3\times10^{12}(cm^{-2})$	$3{\cdot}9\text{-}5{\cdot}6\times10^{16}$	$5{\cdot}4\times10^{16}$
N 15/6	Implanted $1\times10^{13}(cm^{-2})$	$1{\cdot}5\text{-}2{\cdot}0\times10^{17}$	$1{\cdot}8\times10^{17}$
N 15/8	Implanted $5\times10^{13}(cm^{-2})$	$3{\cdot}9\text{-}5{\cdot}2\times10^{17}$	$9{\cdot}2\times10^{17}$

Table 5-1

Calculated and the measured values of various concentrations associated with diffused and ion implanted wafers. The measured values were the effective substrate concentration derived from C/V data. The calculated values for diffused and implanted wafers correspond to the surface concentrations C_S and peak concentration respectively.

concentration calculated on the basis of the experimental ratios of C_{min}/C_{max} from high frequency C/V curve. They compare well.

Oxidation:

500 Å of oxide was grown at 1000 °C in dry O_2 with a N_2 slow pull after oxidation.

All other processing was the same as before.

5.3.2 Results of Trapping

Two wafers of each set were processed to see the variation from wafer to wafer, since the results so far indicate that substrates play an important role in governing the trapping results.

The most important point noted was that indeed the devices were prone to breakdown during the initial stages of trapping. It is for this reason that all trapping was done at 5E-11 A rather than the 2E-10 A used in the previous experiments.

The value of ΔV_{FB} (2000 sec) for each wafer that did not breakdown is shown in Fig. 5-4. It is to be noted that for all the diffused wafers, only the one with the 10/30 cycle gave results. The 3/10 cycle showed big scatter in I/v from dot to dot within the same wafer and also between the two wafers. Hence the substrate doping level is important in determining if trapping will occur. However, this cannot be the only important

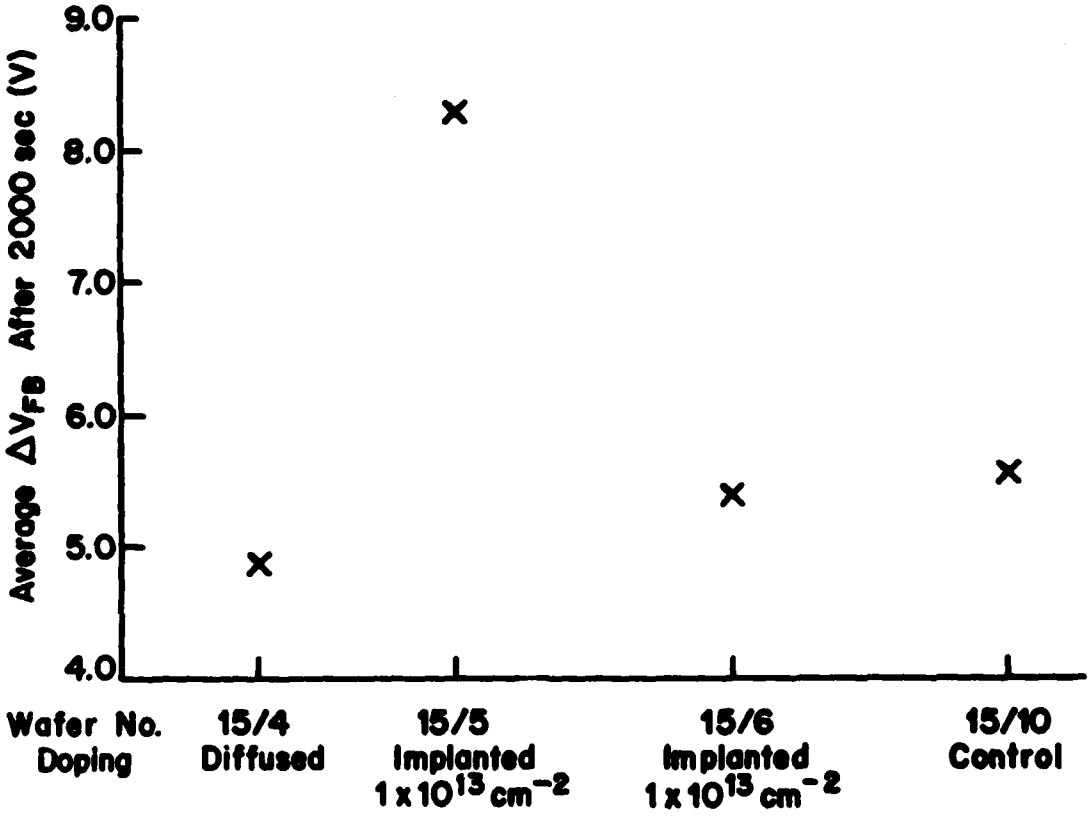


Fig. 5-4 Values of ΔV_{FB} for diffused, implanted and control wafers.

factor since wafers 15/3 and 15/4 were both processed identically and yet only wafer 15/4 worked. One sees the same result for ion implanted wafers; there was a big variation in ΔV_{FB} for wafers 15/5 and 15/6 even though their processing was identical. It is suggested that this was due to the difference in the crystal quality of individual wafers affecting avalanche injection. However, between both diffused and implanted samples, the only ones that survived trapping were doped to a level of about 2E17 cm^{-3}. Others had a very high incidence of breakdown during I/v measurements.

Bearing in mind the scatter within the same sub-set (compare 15/5 to 15/6), the result of ΔV_{FB} for all the wafers shown in Fig. 5-4 are comparable. Hence it would appear that it is possible to dope the substrate by either implantation or diffusion to study the trapping characteristics of the oxide. However, from the evidence that the uniformity and level of doping concentration is important in determining avalanche injection, better results can be expected by implantation rather than diffusion particularly since the doping concentrations required are near 1E17 cm^{-3}. This is difficult to control in a diffusion process. This is a promising possibility for 'on-chip' monitoring but more work needs to be done especially with wet oxides.

6.0 CONCLUSIONS AND FUTURE EXPERIMENTS

A comprehensive summary of all the results are given in the abstract. It became quite clear during the course of this work that, due to the dot to dot scatter within the wafer, device selection had to be made carefully . Even so, certain anomalies were sometimes seen. For example, certain devices showed no shift in flat band voltage, and this needs to be investigated more fully. The actual conditions under which trapping was done was also found to be important. Indeed one of the most important conclusions that has emerged from this study is that the magnitude of trapping as seen by the flat band voltage shift ΔV_{FB} is dependant on the value of v which is the applied ac voltage or I_{dc} which is the dc injected avalanche current. The implication is that part of the measured traps are generated by the hot carriers at the interface. In order to minimize this effect, the measurement should be done at lower I_{dc} such that the carriers are less hot. The measurement then obtained should be more representative of the oxide characteristics. As mentioned before, considerable scatter in the I/v characteristics among dots within the same wafer was observed on occasions. This is attributed to the spatial non-uniformity of the crystal quality of the wafer. Trapping dependence on the pre-oxidation heat treatments of the wafers was also observed. It is suggested therefore that wafers from different manufacturers with different pre-oxidation heat treatments be tried. All wafers used in this study were from Fairchild.

The picture that emerges from this study is that trapping as measured by the ΔV_{FB} is not only a characteristic of the way that an oxide is grown and annealed, but it also depends on the quality of the substrate and its detailed thermal history. This substrate effect shows itself in the I/v characteristic of a particular device. If the dc current I_{dc} was kept constant at a particular level (as was the case for our experiments), then the v value would represent the temperature of the hot carriers. Since the evidence suggests that the hot carriers generate trap levels, then any change in carrier temperature would reflect in ΔV_{FB}. These substrate related effects were found to be significant. It is interesting to to note that as a consequence of the above arguments, the avalanche I/v curves could be a very useful way of characterising the crystal quality of silicon substrates.

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