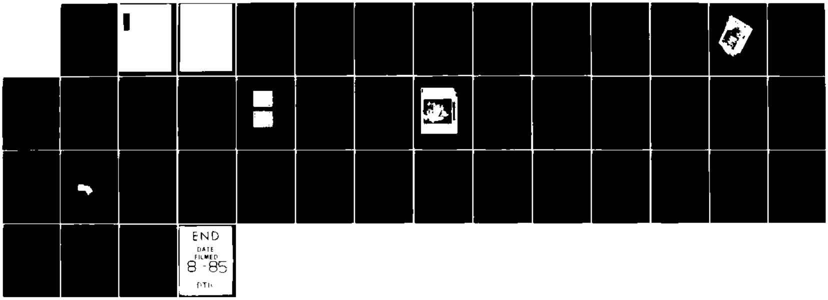
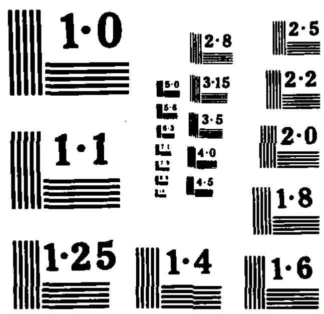
AD-A156 933   5 WATT SOLID STATE EHF TRANSMITTER(U) AIR DEFENSE COMMAND YUMA AZ ROCKET PROFICIENCY CENTER   S L ZOLNAY 15 MAY 85 TR-715 ESD-TR-84-298 F19628-85-C-0002   1/1

UNCLASSIFIED   F/G 9/5   NL




1·0
1·1
1·25
1·4
1·6
1·8
2·0
2·2
2·5
2·8
3·15
3·5
4·0
4·5

AD-A156 933

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

5-WATT, SOLID-STATE, EHF TRANSMITTER

S.L. ZOLNAY

Group 66

TECHNICAL REPORT 715

15 MAY 1985

LEXINGTON MASSACHUSETTS

ABSTRACT

A 5-watt, all solid-state, EHF, rugged, broadband transmitter has been developed for use in satellite-communication ground terminals. This state-of-the-art transmitter demonstrates efficient and cost-effective RF power generation at EHF for commercial and military applications. The specific center frequency and bandwidth (43.5 to 45.5 GHz) are matched to current military requirements. Measured results on the prototype unit are presented. Measured data on the combined outputs of two solid-state, EHF transmitters show 10.5 watts at 44.5 GHz, and the 1-dB bandwidth in excess of 5% (2 GHz). Development of the building blocks (the diodes, the unit amplifiers, the power combiners and the multiplier) are also discussed.

CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont)

LIST OF TABLES

I. INTRODUCTION

One of the salient criticisms of efforts to shift communications toward extra high frequencies (EHF), where there are relatively little or no spectrum allocation problems, is that the state-of-the-art in RF power generation is far below the required levels for closing the link with adequate margin for useful channel capacities. Effective radiated powers in excess of 50 dBW are needed. This requirement translates to several watts of output from the transmitter if the antenna size is to be kept at a modest few feet. In this paper the design, development, and measured performance of a 5-watt, all solid-state, EHF transmitter is presented which demonstrates the efficient, reliable and cost-effective generation of RF power at 45 GHz. The building blocks that make up the transmitter, and their development and performance, are also discussed. The combining of RF power to meet the required goal is treated in detail.

Of the numerous ways in which RF power can be generated at EHF, only the solid-state approach is addressed here. Of the solid-state materials (GaAs, InP, and Si) capable of performance at EHF, the choice here is silicon. Silicon IMPATT diodes combine the desired features of robust power, reliable and long-life operation at low junction temperatures, and ease of broadband circuit design. Therefore, the first building block in designing the transmitter is the Si, double-drift, IMPATT diode.

A silicon, double-drift, IMPATT diode is capable of generating RF power in excess of one watt at EHF. What is required here is an amplifier circuit which extracts this power as added power.[1] Thus, a stable, broadband, low-loss, reflection-amplifier circuit design is needed. Such a circuit consists of a suitable circulator and the waveguide circuit for the diode. Since the output power of one amplifier is on the order of 1 watt, the outputs of several amplifiers have to be combined to produce 5 watts. In addition to the non-trivial combiner circuitry, the amplifiers whose outputs are to be combined should be matched in amplitude and especially in phase. The second building block is the EHF unit amplifier.[2]

The third building block is the power combiner circuit. This is accomplished using E-H hybrid magic tees of reduced height waveguide with good balance and isolation characteristics.

Modulation and other signal processing take place at lower frequencies. Signaling schemes that employ synthesizers and processing hardly progress beyond a few gigahertz and seldom cover the final, desired transmitter bandwidth. The device that bridges the gap between the signal processor and the power amplifier is the frequency multiplier and bandwidth expander.[3] The fourth and final building block then is an efficient and powerful multiplier.

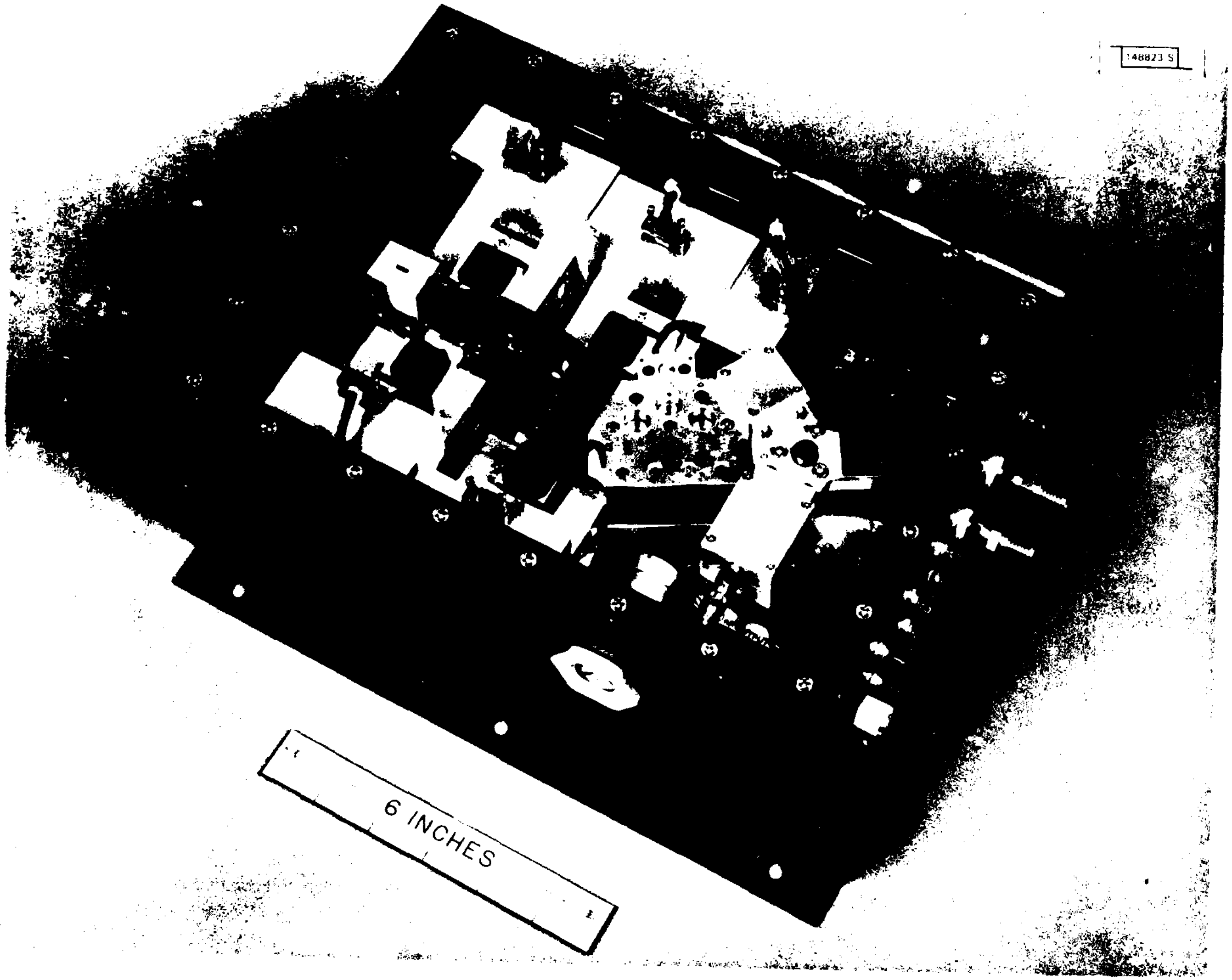


Fig. 1. Photograph of 5-watt, solid-state, EHF transmitter.

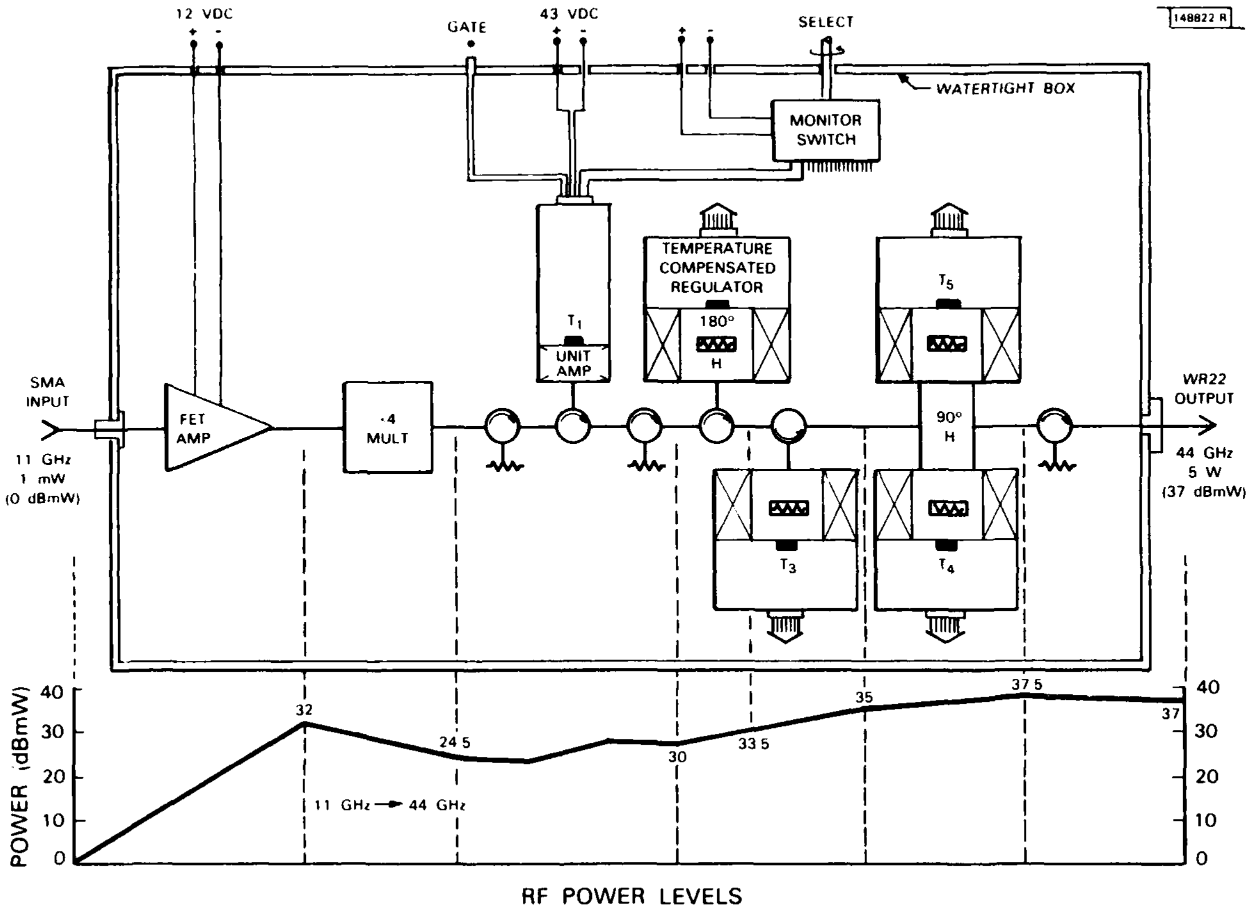


Fig. 2 Block diagram of 5-watt, solid-state, EHF transmitter

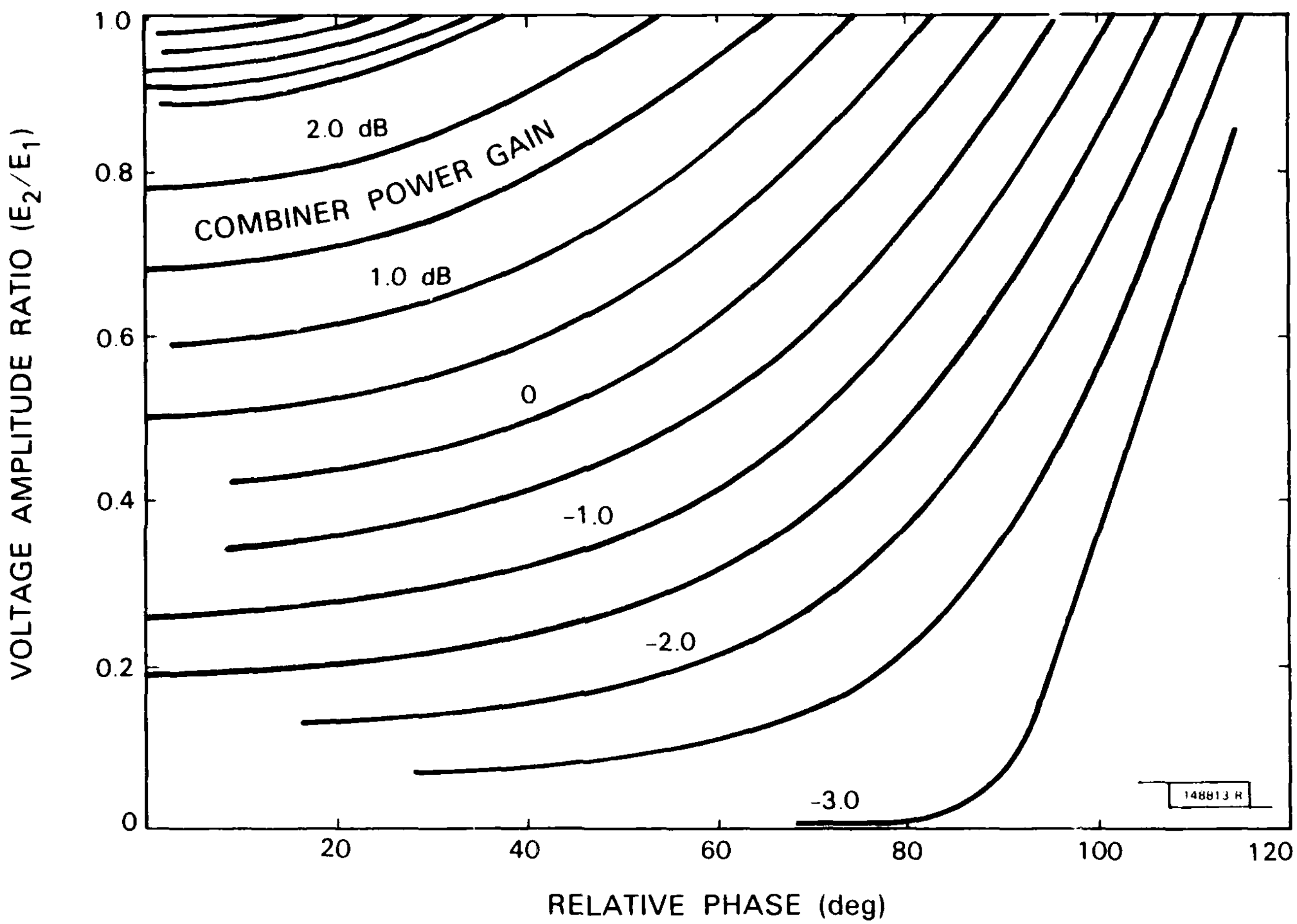
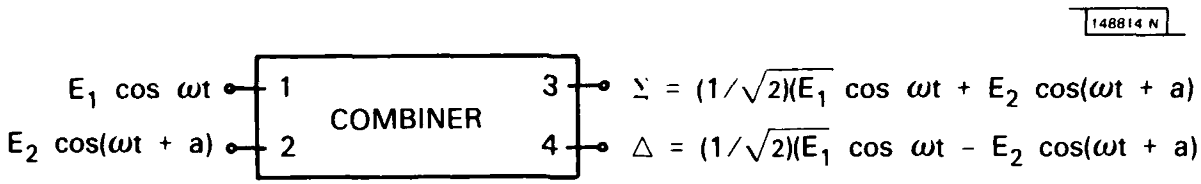


Fig. 11 Combiner power gain for various amplitude ratios and relative phases



P_1 = INPUT 1 = $(E_1/\sqrt{2})^2$

P_2 = INPUT 2 = $(E_2/\sqrt{2})^2$ LET: $E_1 \geqslant E_2$

$P_3 = \Sigma^2 = 1/4\ (E_1{}^2 + 2E_1E_2 \cos a + E_2{}^2)$

$P_4 = \Delta^2 = 1/4\ (E_1{}^2 - 2E_1E_2 \cos a + E_2{}^2)$

$$\text{COMBINER POWER GAIN} = 10\ \text{LOG}_{10} \left[\frac{1 + 2\,(E_2/E_1) \cos a + (E_2/E_1)^2}{2} \right]$$

N.B.: COMBINER LOSS = COMBINER GAIN −3 dB

Fig. 10 Power combiner

An ordinary, but quite important, component of a stable, reflection-amplifier is the EHF circulator which converts the one-port waveguide circuit of the IMPATT diode into two ports. The insertion loss for three cascaded circulators is shown in Figure 9 as a function of frequency. The maximum insertion loss per pass is 0.3 dB. The minimum measured isolation across the band is 22 dB per pass. In normal use the circulator in the center would have the unit amplifier attached to it and the circulators on either side could be used for inter-stage isolation.

C. Power Combiners

The waveguide hybrid (magic tee) structure was used to combine the output powers of the unit amplifiers. The stylized representation of such a device is shown in Figure 10. For two sinusoidal inputs of the same frequency, different amplitudes (E1 and E2) and relative phase "a", the outputs are the sums and differences as shown in the figure. Considering the power in one of the inputs as the reference, the power gain of the combiner relative to that reference is:

$$\text{Combiner Power Gain, dB} = 10 \log_{10} \{ [1+2(E_2/E_1) \cos(a)+(E_2/E_1)^2]/2 \} \quad (1)$$

The combiner gain is clearly a function of amplitude ratio and relative phase. The above expression was evaluated for amplitude ratios $0 > (E_2/E_1) < 1$ and relative phase angle $0 > a < 120$ degrees. The results are plotted in Figure 11. For successful power combining (that is, with low loss and good efficiency), the amplitudes should be matched within 20% and the phases should be within 40 degrees.

The unit amplifiers that are the building blocks of this transmitter all exhibit a match in amplitude within 10%, and relative phase within 10 electrical degrees over the band at nominal gain and input drive level. This results in a minimum combiner gain of 2.5 dB which translates to a minimum combiner efficiency of 89%.

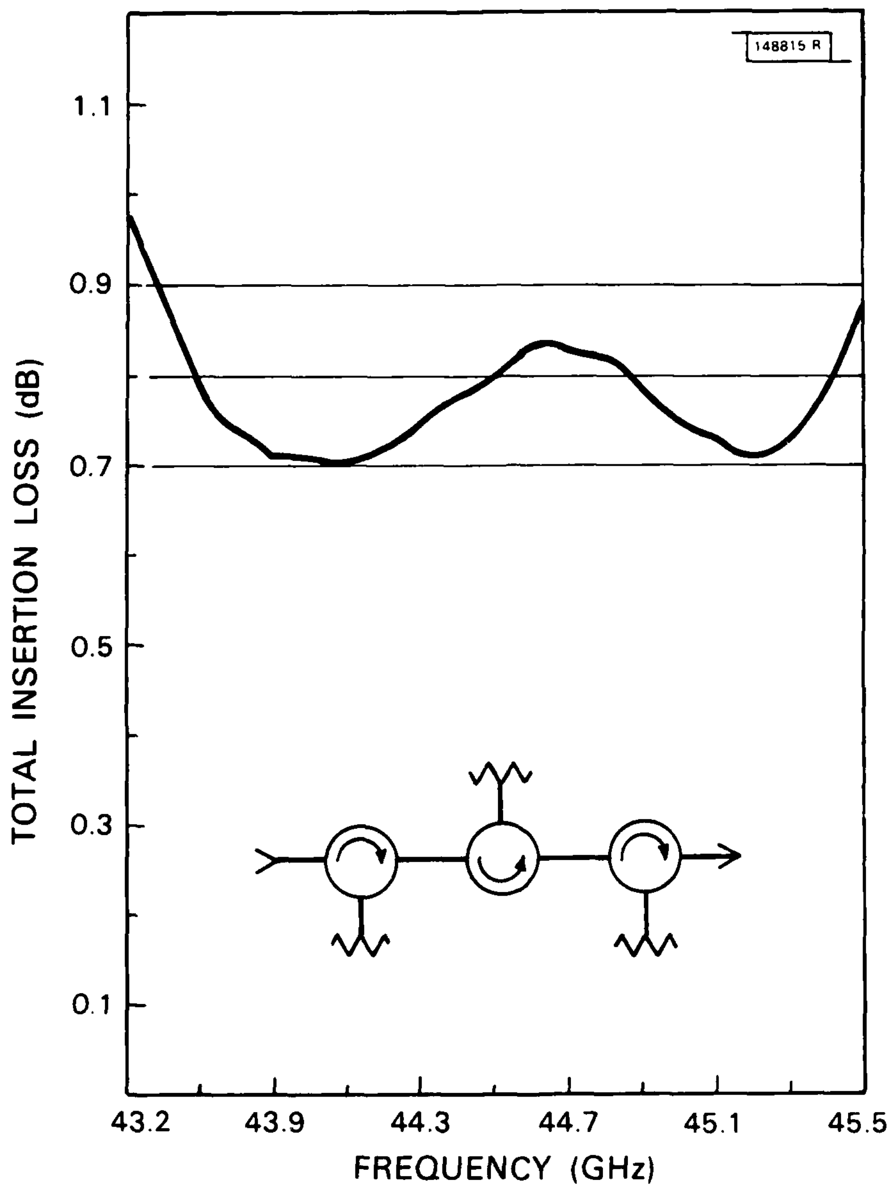


Fig. 9 Measured insertion loss of three cascaded EHF circulators

B. Unit Amplifiers

To make use of the EHF RF power available from the IMPATT diodes described in Section 1 above, an efficient, broadband, unconditionally stable millimeter-wave circuit was developed. The design technique for evaluating and optimizing the operating circuit efficiency of stable, reflection-amplifiers using these devices has been reported.[1,2] A picture of one such stand-alone unit amplifier is shown in Figure 7; its measured characteristics are given in Table 3.

TABLE 3

MEASURED CHARACTERISTICS OF EHF UNIT AMPLIFIER

Center Frequency:	44.5 GHz
Bandwidth:	2 GHz
Input Power, RF:	0.5 watt
Added Power, RF:	1.1 watts
Output Power, RF:	1.6 watts
Gain:	5 dB
Input Power, DC:	15.5 watts
Junction Temperature Rise:	215 °C
Added Power-to-DC Input Efficiency:	7.1%

The amplifier was built, and tested, to withstand a shock pulse of 4.2 g peak amplitude, and vibrations of up to 1.5 g (peak, sinusoidal). Other environmental conditions were -20 to +65°C baseplate temperature, and a 10,000-foot altitude. Normal operation is CW, and a TTL compatible command can turn the amplifier on (full RF output) in 3 microseconds, and turn it off (no coherent RF, no parasitics, no spurious, not even thermal noise output) in less than 1 microsecond. Typical RF performance of the unit amplifier across the 5% bandwidth centered on 44.5 GHz is shown in Figure 8.

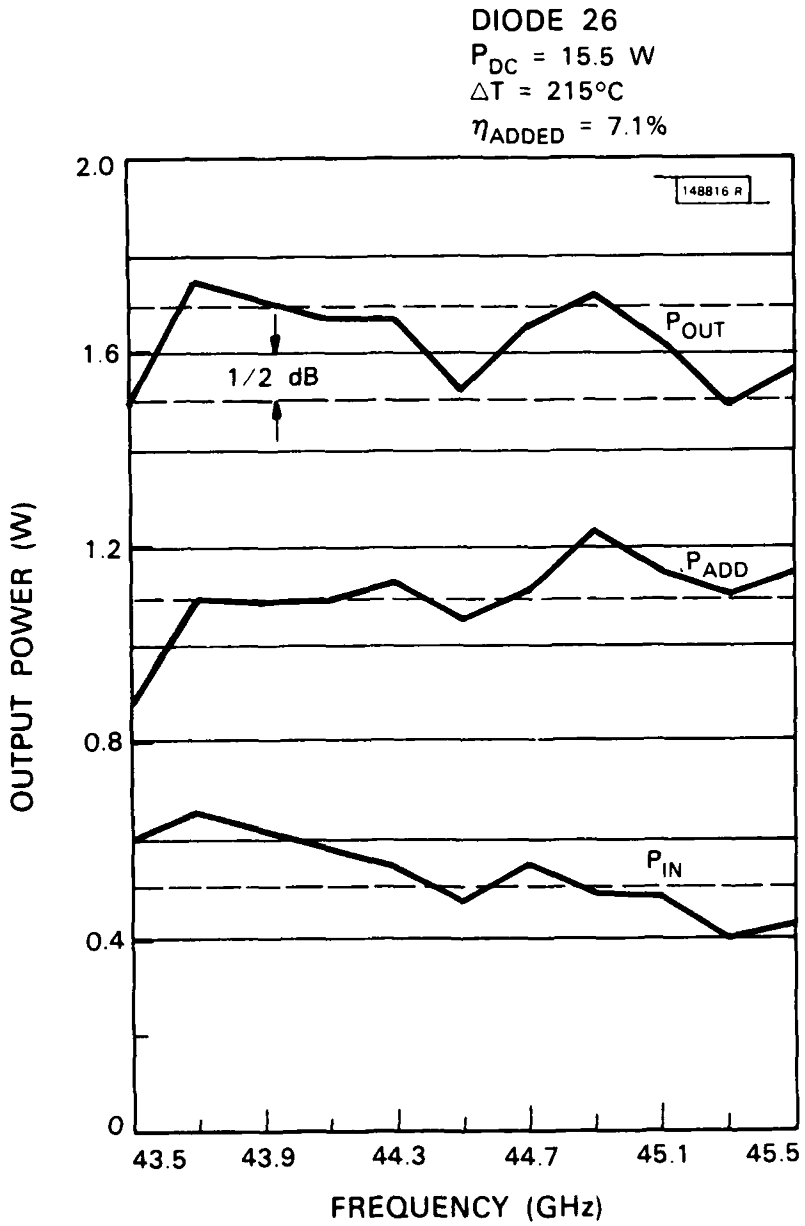


Fig. 8 Output power versus frequency of unit amplifier

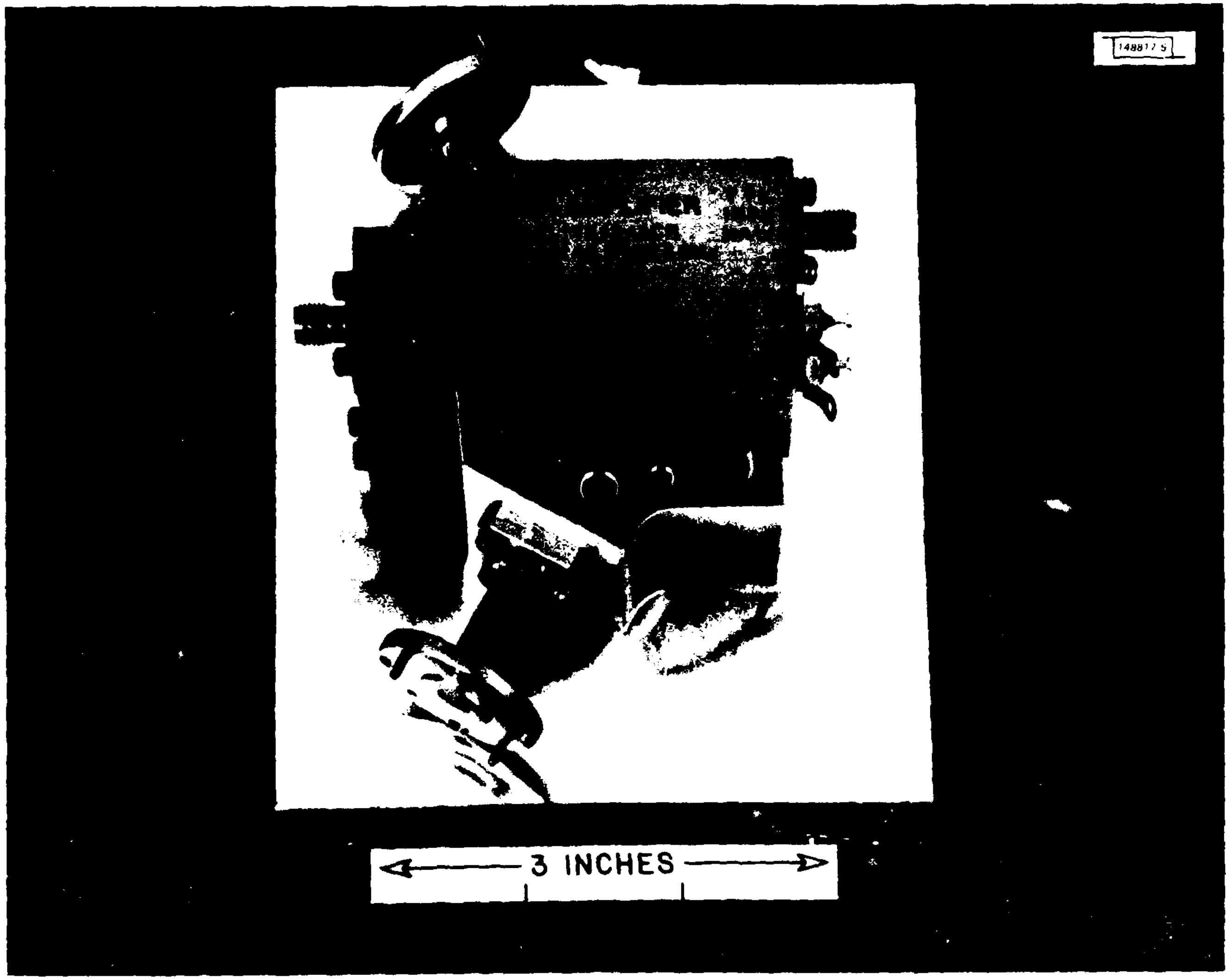


Fig. 7. Photograph of solid-state, EHF unit amplifier.

IV. BUILDING BLOCKS

A. Diodes

In 1980 the only known commercial source for silicon double-drift IMPATT diodes at EHF on diamond heatsinks was the Electron Dynamics Division of the Hughes Aircraft Company (HAC). An order was placed with HAC by Lincoln Laboratory for a quantity of diodes. In addition to meeting the specifications listed in Table 2, the diodes came from a high-yield good wafer, produced the minimum specified RF power, were long lasting, and were repeatable.

TABLE 2

SILICON, DOUBLE-DRIFT IMPATT DIODE PARAMETERS

Breakdown Voltage @ 1 mA	26.6 - 29.9 Vdc
Forward Bias Voltage @ 10 mA	0.72 - 0.88 Vdc
Diode Capacitance @ 0 V	1.86 - [illegible].06 pF
Diode Capacitance @ 0.9 xVb	0.61 - 0.67 pF
RF Output Power	0.80 W minimum
Frequency of Oscillations	43.5 - 45.5 GHz
Junction Temperature Rise	175°C maximum
Thermal Resistance	15°C per W (typ)
Heatsink	Diamond embedded in copper

Very nearly 100% of the diodes delivered met the above specifications. The yield at that time from a good wafer was estimated between 1000-1500 useful diodes about half of which would meet specifications. The required RF output power was met at the maximum allowable junction temperature. At that time the only available test circuit was an oscillator and that was used. The predicted lifetime, neglecting infant mortality, based on reliability data from the manufacturer, is in excess of 10^6 hours for 200°C junction temperature. Uniformity of the devices was sufficiently good to allow "drop-in" replacement in a waveguide circuit one out of three times. The availability of these devices paved the way for the follow-up transmitter design.

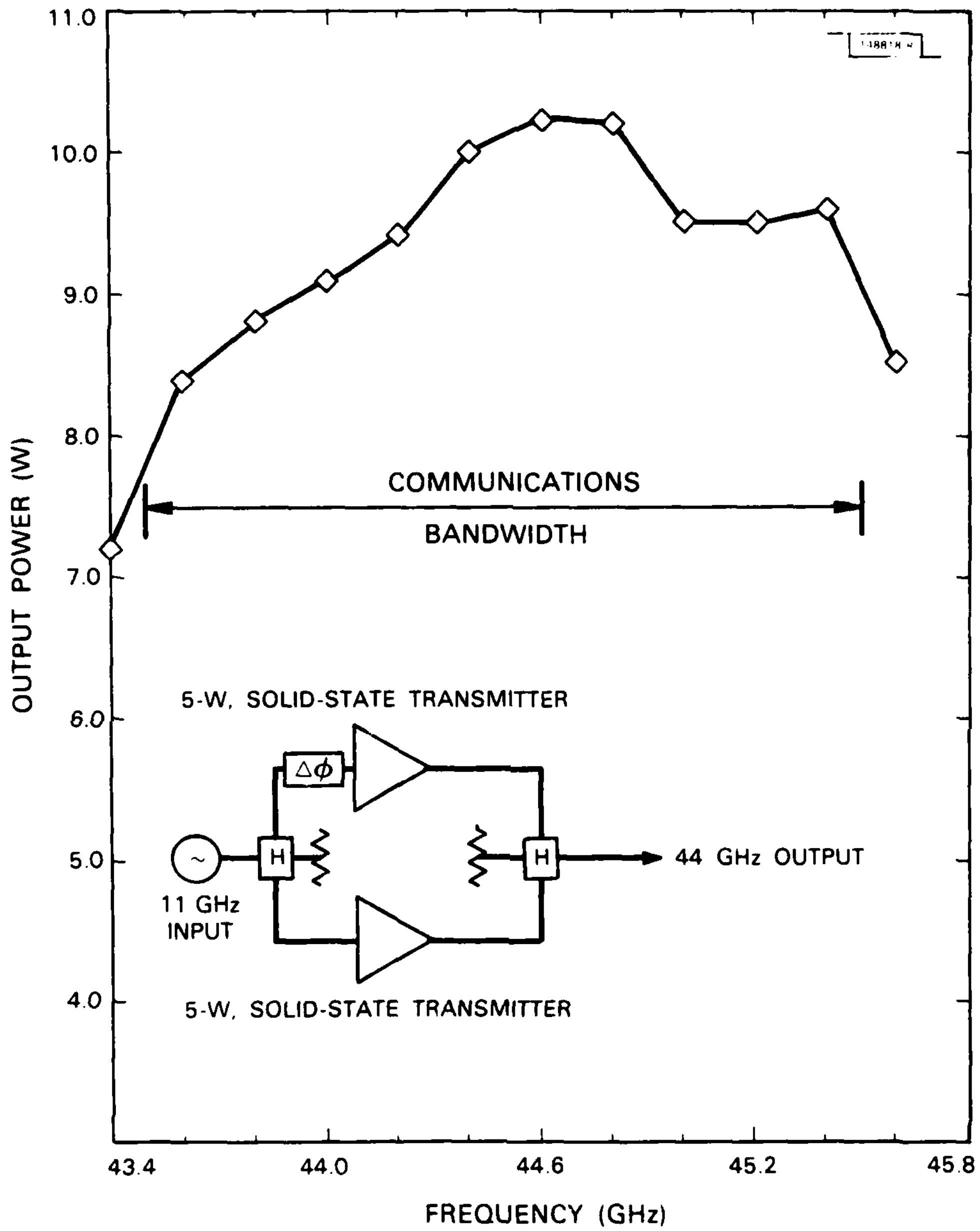


Fig. 6 10-watt, combined outputs of two, 5-watt, solid-state, EHF transmitters

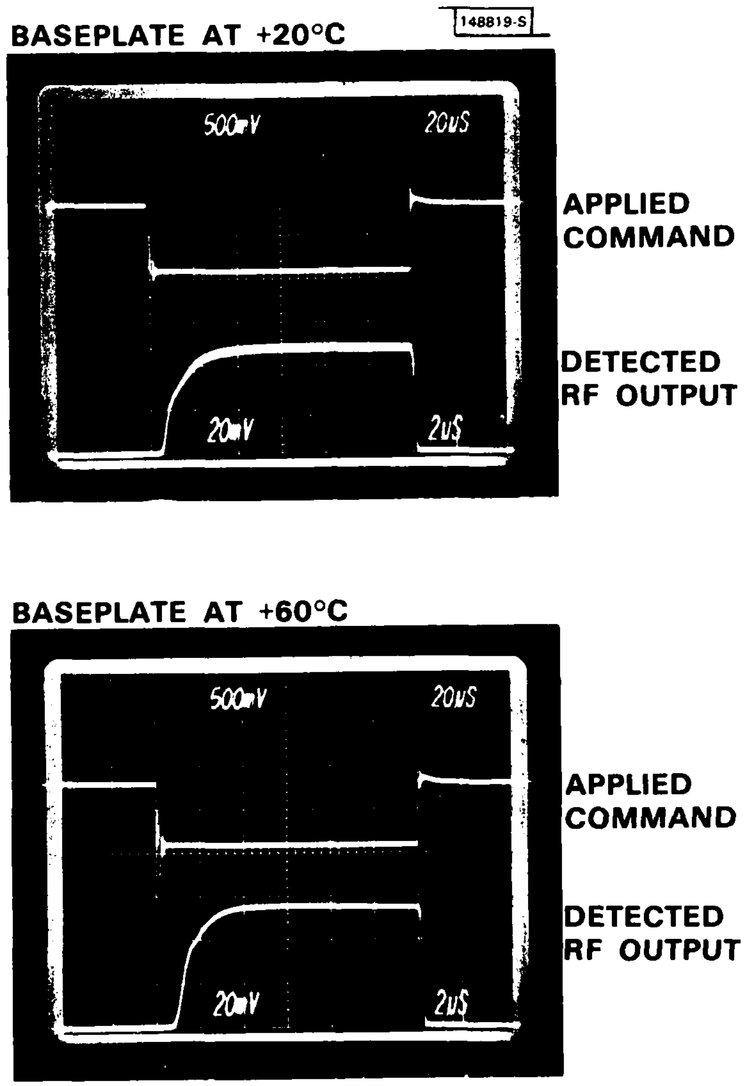


Fig. 5. Turn-on and turn-off characteristics of 5-watt, solid-state EHF transmitter.

III. 10 WATTS AT EHF

When the outputs of two solid-state EHF transmitters were combined, the result was a minimum of 7.8 watts output across the 5% communications bandwidth centered on 44.5 GHz (see Figure 6). Only one phase adjustment was needed at 11 GHz at the input to one of the transmitters. The DC input power requirement is ~300 watts. The two independent transmitters each consist of a GaAs FET amplifier at X-band; an efficient, high-power varactor quadrupler and four stages of stable, reflection amplifiers using a total of 17 (8 and 9, respectively) silicon, double-drift IMPATT diodes. The power divider and combiner is an E-H magic tee.

This experiment demonstrates the feasibility of generating 10 watts RF power at EHF with solid-state devices (even though this combining approach is not the optimum way to achieve 10 watts). The two individual 5-watt transmitters, constructed at different times using devices from different wafers, track each other in phase and in amplitude across greater than 5% bandwidth, resulting in efficient combining of their outputs. It would be relatively easier to build a 10W, solid-state, EHF transmitter with a single, rather than two separate, amplifier chain. This experiement shows that such levels are a reality with solid-state devices.

We all knew that this is feasible. But this is believed to be the first time ever, anywhere, that 10 watts were demonstrated at 45 GHz with solid-state devices in a stable reflection-amplifier mode in a complete transmitter configuration. Watch out traveling-wave-tube-amplifiers: Here come the IMPATTS!

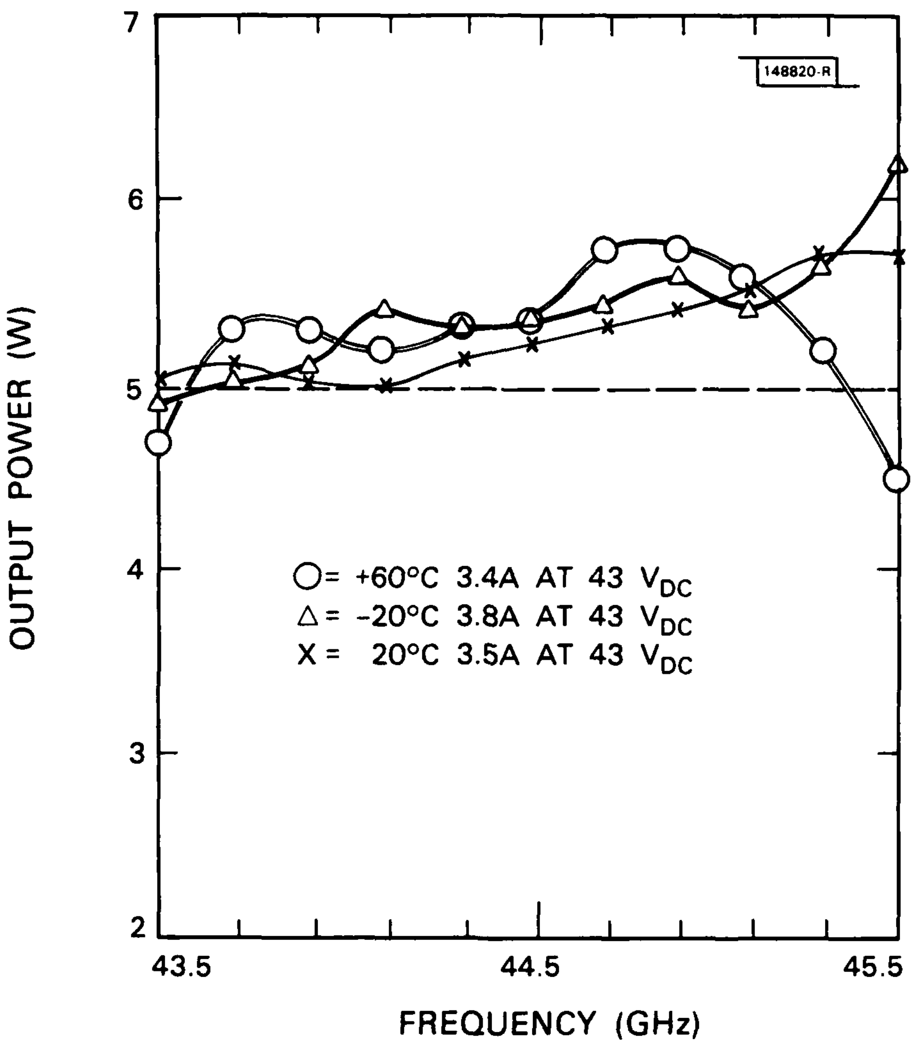


Fig. 4 Solid-state, EHF transmitter measured output power versus frequency with baseplate temperature as a parameter

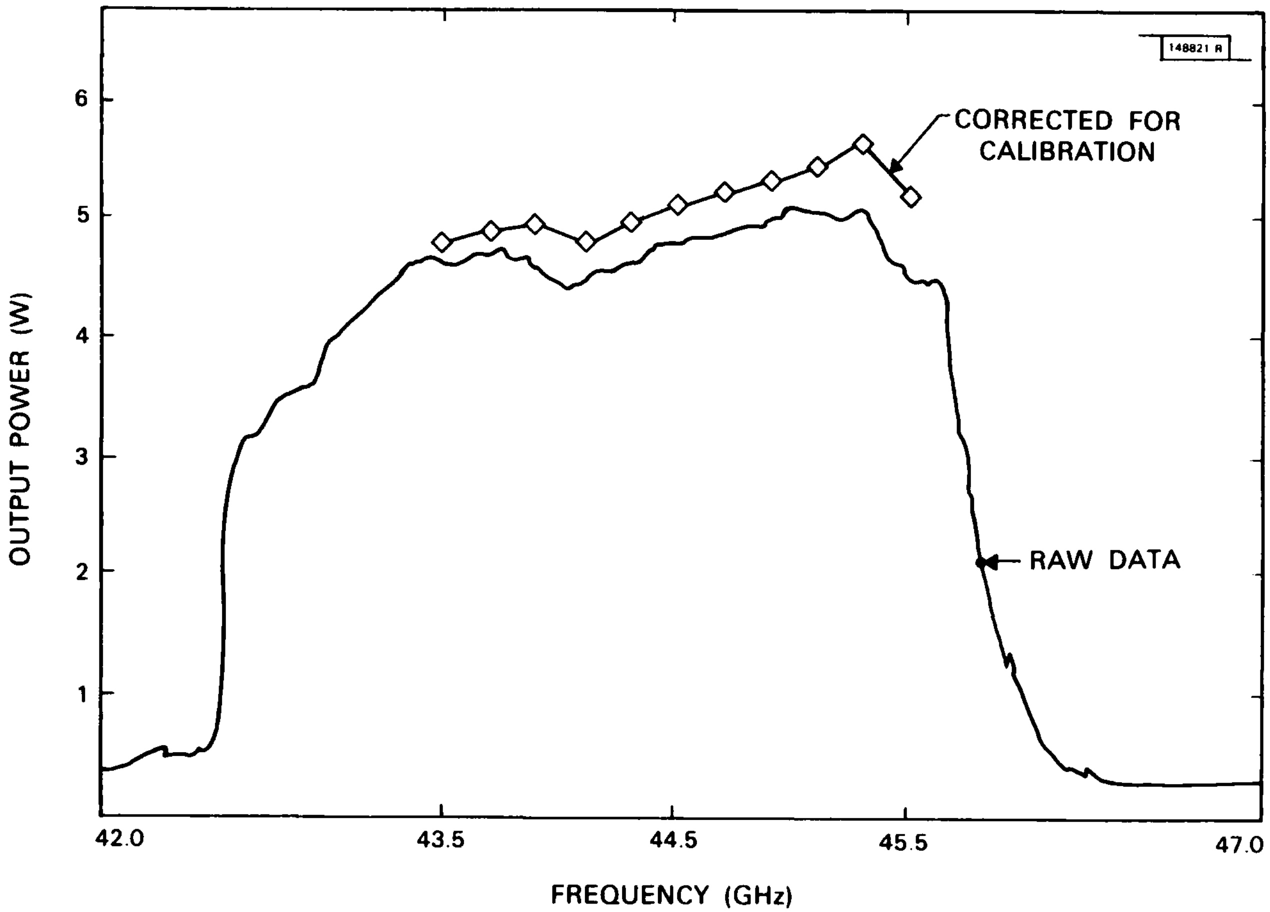


Fig. 3 Solid-state, EHF transmitter output power versus frequencies

II. 5-WATT, SOLID-STATE, EHF TRANSMITTER

A photograph of the 5-watt, solid-state, EHF transmitter developed for MIT Lincoln Laboratory which makes use of the above building blocks is shown in Figure 1. The block diagram and the RF power levels are shown in Figure 2. Bias voltage applied to each diode, and current drawn by the device, can be monitored externally. The 11-GHz GaAs FET amplifier is a commercially available unit. The quadrupler and the unit amplifiers will be described below. Each unit amplifier has an individual bias supply regulated in current, which in turn is compensated for variations in temperature of the baseplate, thereby maintaining the output reasonably constant. The output power as a function of frequency is shown in Figure 3. The same is shown over the bandwidth of interest in Figure 4 with baseplate temperature as the parameter. The detected RF output and the applied TTL command are shown in Figure 5 for two ambient temperatures. The rise time is ~ 2 microseconds, the fall time is much less than a microsecond. The transmitter is capable of being switched on and off at the rate of up to 250 kHz. The measured performance parameters of the transmitter are given in Table 1, the complete specifications are listed in the Appendix.

TABLE 1

PERFORMANCE PARAMETERS OF 5-WATT, SOLID-STATE, EHF TRANSMITTER

Output Frequency Range:	43.5 to 45.5 GHz minimum
Input Frequency Range:	10.875 GHz to 11.375 GHz
Input RF Power:	1 milliwatt ±5 dB
Output RF Power:	>5 watts, CW, 43.50 to 45.50 GHz and over entire input power range.
Devices:	Silicon, double-drift IMPATT diodes
Junction Temperature Rise:	~ 200°C
Estimated Life:	20,000 hours (MTTF 50%, T_j = 270°C)
Base Plate Temperature:	-20° to +65°C
DC Input Power:	3.5 A @ 43V 1.5 A @ 12V
Weight:	15 lbs with heatsink in sealed box. Heatsink and enclosure weigh about 8 lbs.

D. Efficient, High-Power, EHF, X4 Multiplier

In the terminal design, where the transmitter reported here is being used, the signal processing stops at one fourth of the output bandwidth and of the required center frequency. An hermetically sealed, passive, frequency quadrupler with two GaAs varactor diodes in cascaded doubler stages, separated by an isolator, is used to expand the bandwidth by four and to quadruple the center frequency. The diodes are self-biased by the rectified RF current. The volume is approximately 6 cubic inches; the weight is less than 8 ounces. Typical output is in excess of 100 milliwatts over the 43.5 to 45.5 GHz range for 1 watt input at 11 GHz. Output power variations are ~1 dB across the band and the input SWR < 1.5. The output spectrum is the input spectrum multiplied by four. The output power over the 43.5 to 45.5 GHz band for one of the multipliers is shown in Figure 12; the inset is a picture of the actual multiplier. Figure 13 shows that, at a single frequency, almost 300 mW EHF output is feasible with nearly 20% X-band-to-EHF quadrupling efficiency. The limitation is the breakdown of the first doubler when the input is ~2 watts at 11 GHz.

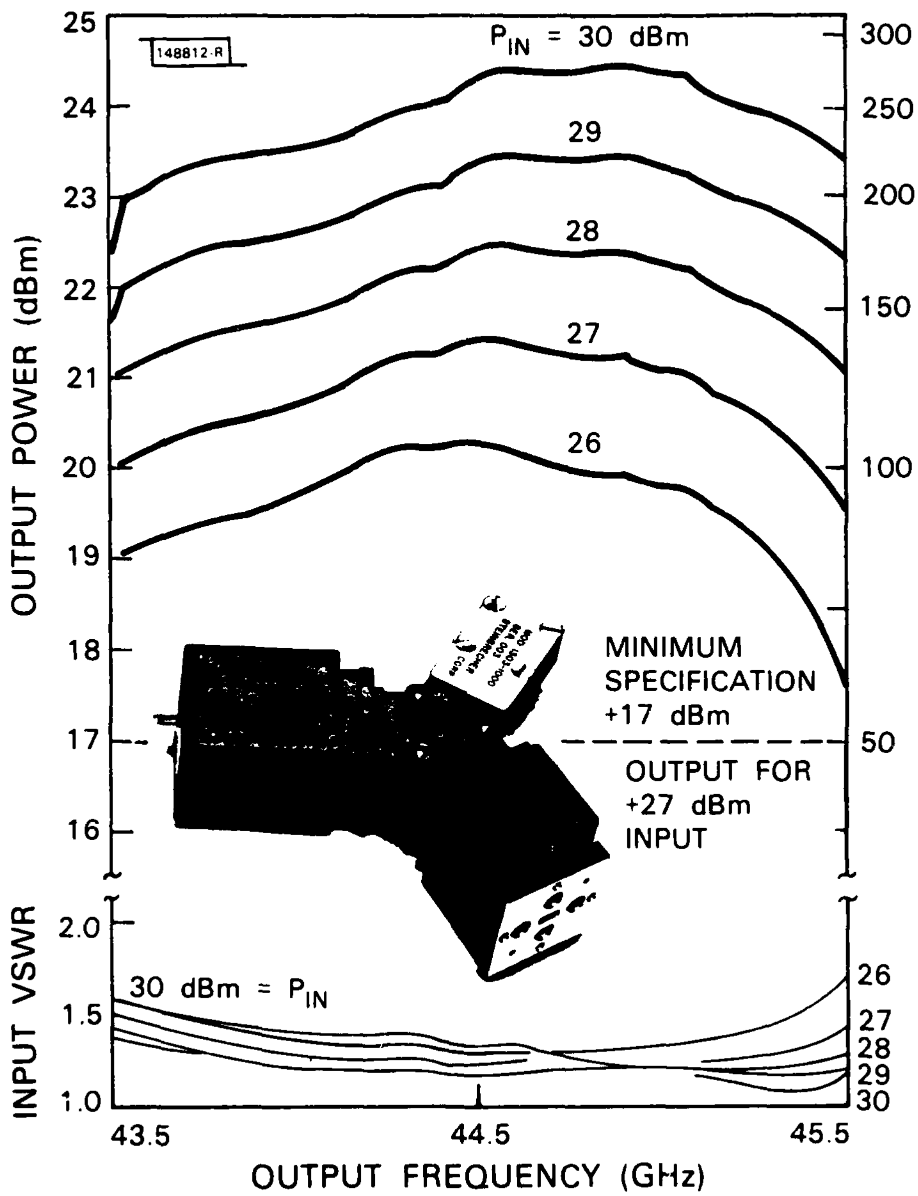


Fig. 12 EHF output power versus output frequency of efficient, high-power frequency quadrupler

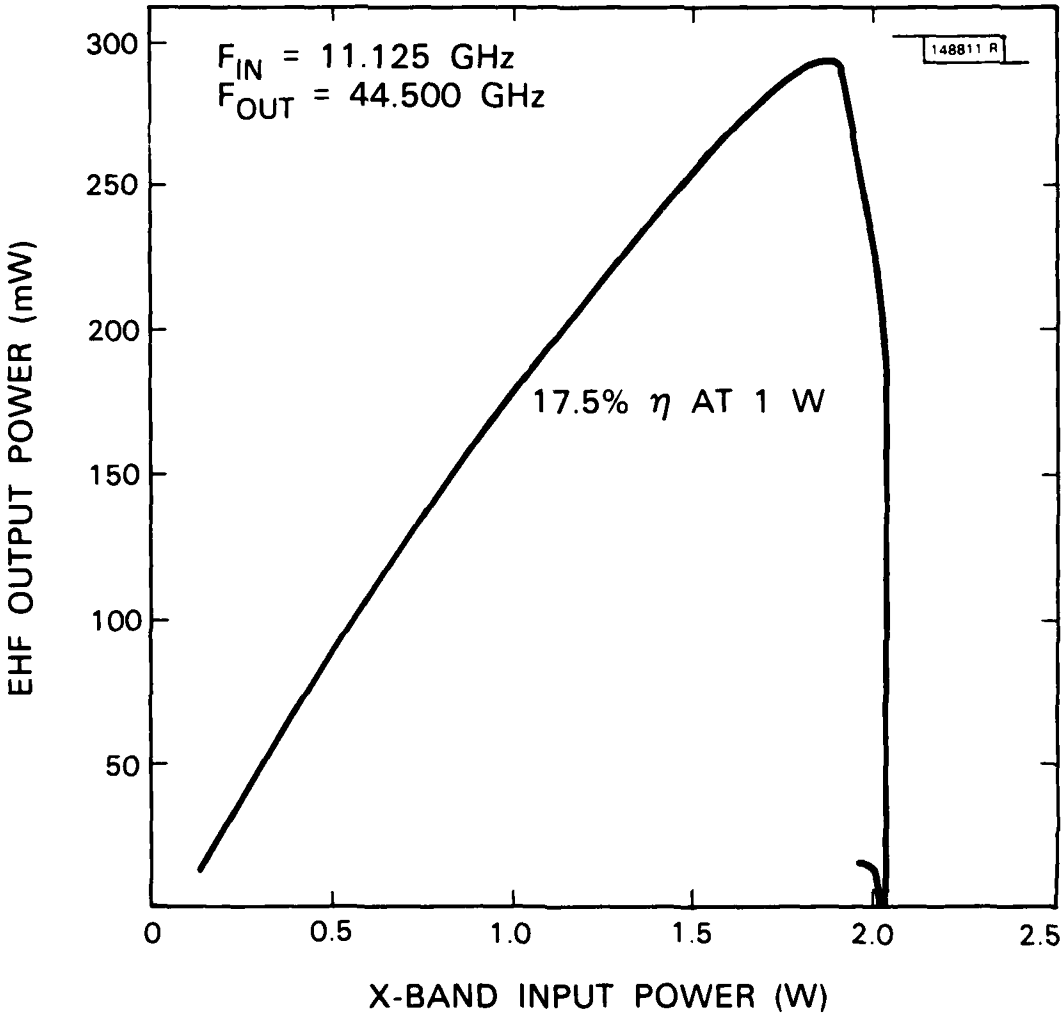


Fig. 13 EHF output power versus X-band power of efficient, high-power frequency quadrupler

V. DESIGN OF THE POWER AMPLIFIER

The block diagram of a multi-stage, broadband, EHF power amplifier is shown in Figure 2. It uses nine silicon, double-drift IMPATT diodes mounted on diamond heat sinks to produce 5 watts total output power with 13 dB gain over the 43.5 to 45.5 GHz frequency range. Each diode, operating as a stable, reflection amplifier, adds about 1 watt RF power. Three of the four stages require a circulator. Additionally, three isolators and five dividers/combiners are also needed. Because of the relatively low RF power per device (~1 watt) and the large number of circuit elements (17) needed to achieve the required level of output power, it is important to minimize the RF losses of each circuit element.

Referring to Figure 2, the output of the times-four frequency multiplier is the input to the power amplifier of the transmitter. This input power, P_I, is passed through two circuit elements, an isolator and a circulator, to the first stage. The input level is reduced by α^2, where α is the circuit loss per element (α is assumed to be the same for circulators and hybrids). The first device adds an amount of RF power, P_A, to the attenuated input. The first stage is really gain limited, $G_1 \approx 6$ dB, rather than added power limited, $P_{01} \approx 700$-800 milliwatts. The output of the first stage is divided by two and it is then applied to the two amplifiers in the second stage. Following the signal path through the RF circuit and accounting for the losses, power divisions and combinings, the following expression for the output power, P_O, is derived:

$$\left(\left\{\left[\frac{(P_I\,\alpha^2 + P_A)\,\alpha^4}{2} + P_A\right]\alpha^4 + P_A\right\}\frac{\alpha^4}{2} + P_A\right) 4\,\alpha^3 = P_O \qquad (2)$$

Solving equation 2 for the added power, P_A:

$$P_A = \frac{\dfrac{P_O}{4\alpha^3}\left(1 - \dfrac{P_I\,\alpha^{17}}{P_O}\right)}{\dfrac{\alpha^{12}}{4} + \dfrac{\alpha^8}{2} + \dfrac{\alpha^4}{2} + 1} \qquad (3)$$

Substituting into equation 3 the required output power, $P_O = 5$, and the required gain, $(P_O/P_I) = 20$, it reduces to an expression for the required added power in watts per device:

$$P_A = \frac{\frac{1.25}{\alpha^3}\left(1 - 0.05\,\alpha^{17}\right)}{\frac{\alpha^{12}}{4} + \frac{\alpha^8}{2} + \frac{\alpha^4}{2} + 1} \qquad (4)$$

The output power of the first stage, P_{O1}, is:

$$P_{O1} = 0.25\,\alpha^4 + P_A\,\alpha^2 \qquad (5)$$

Similarly, the outputs of the second, third and fourth stages are:

$$P_{O2} = 0.25\,\alpha^8 + P_A\left(\alpha^6 + 2\,\alpha^2\right) \qquad (6)$$

$$P_{O3} = 0.25\,\alpha^{12} + P_A\left(\alpha^{10} + 2\,\alpha^6 + 2\,\alpha^2\right) \qquad (7)$$

$$P_{O4} = 0.25\,\alpha^{16} + P_A\left(\alpha^{14} + 2\,\alpha^{10} + 2\,\alpha^6 + 4\,\alpha^2\right) \qquad (8)$$

The total output power, P_O, of the 4-stage, nine-diode amplifier from equation 2 can be expressed as:

$$P_O = 0.25\,\alpha^{17} + P_A\left(\alpha^{15} + 2\,\alpha^{11} + 2\,\alpha^7 + 4\,\alpha^3\right) \qquad (9)$$

The gain of the first stage, G_1, is:

$$G_1 = \alpha^4 + 4\,\alpha^2\,P_A \qquad (10)$$

Similarly, the gains of the second, third and fourth stages are:

$$G_2 = \alpha^4 + \frac{2\,P_A}{0.25\,\alpha^2 + P_A} \qquad (11)$$

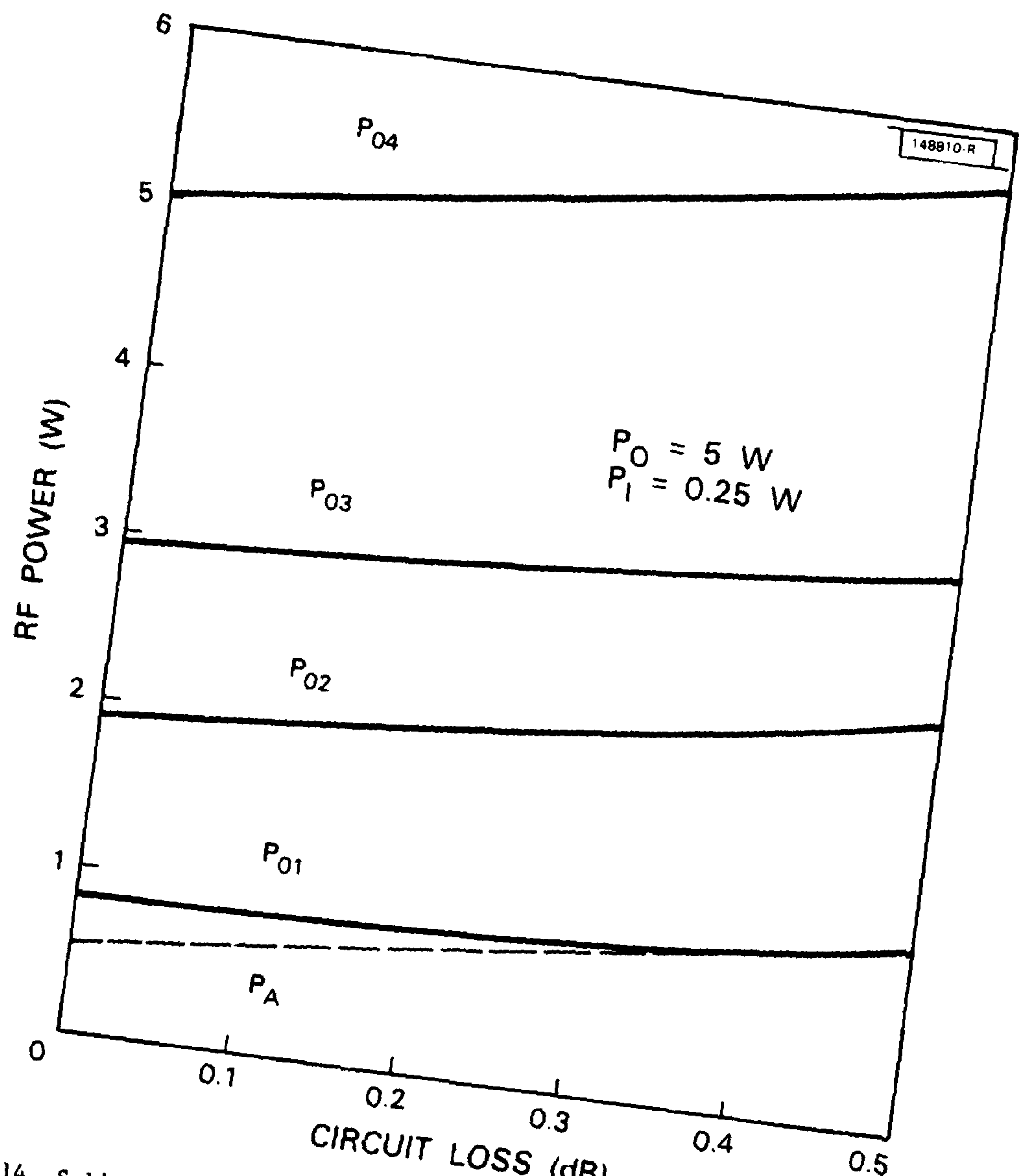


Fig. 14 Solid-state, EHF power amplifier design curves: output power per stage

$$G_3 = \alpha^4 + \frac{P_A}{0.125\,\alpha^6 + 0.5\,P_A\,\alpha^4 + P_A} \quad (12)$$

$$G_4 = \alpha^4 + \frac{2P_A}{0.125\,\alpha^{10} + 0.5\,P_A\,\alpha^8 + P_A\,\alpha^4 + P_A} \quad (13)$$

The total gain, G_{Total}, of the 4-stage, nine-diode amplifier from equation 2 can be expressed as:

$$G_{Total} = \alpha^{17} + 4\,P_A\,(\alpha^{15} + 2\,\alpha^{11} + 2\,\alpha^7 + 4\,\alpha^3) \quad (14)$$

where P_A is in watts.

Equations 4 through 14 were evaluated and plotted to determine the effects of the circuit losses on added power, output powers and gains. The results are tabulated below and are shown in Figures 14 through 16.

TABLE 4

EFFECTS OF CIRCUIT LOSSES ON ADDED POWER, GAIN, AND OUTPUT POWER

Circuit Loss α (dB)	Added Power P_A (watts)	Maximum Gain G_1 (dB)	Maximum Output P_{04} (watts)
0.1	0.63	5.2	2.1
0.2	0.74	5.5	2.2
0.3	0.85	5.7	2.2
0.4	0.98	6.0	2.3
0.5	1.11	6.2	2.3

The added power per device (eq.4) and the output powers from the successive stages (eqs. 5-8) are shown in Figure 14. As the circuit loss per element increases from $\alpha = 0$ to $\alpha = 0.5$ dB, the added power must increase by 3.2 dB from $P_A = 0.5$ watt to $P_A = 1.1$ watt, see the dashed line in the figure.

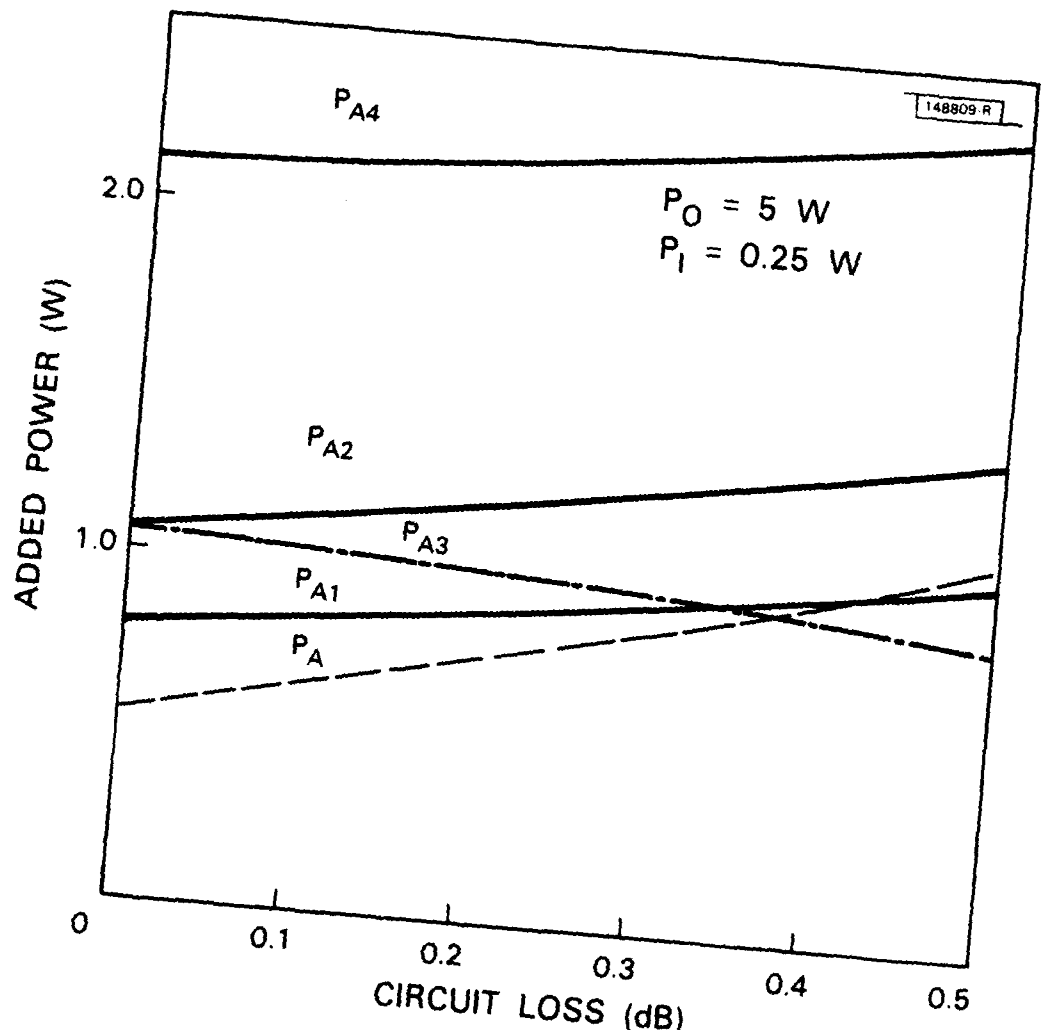


Fig. 15 Solid-state, EHF power amplifier design curves: added power per stage

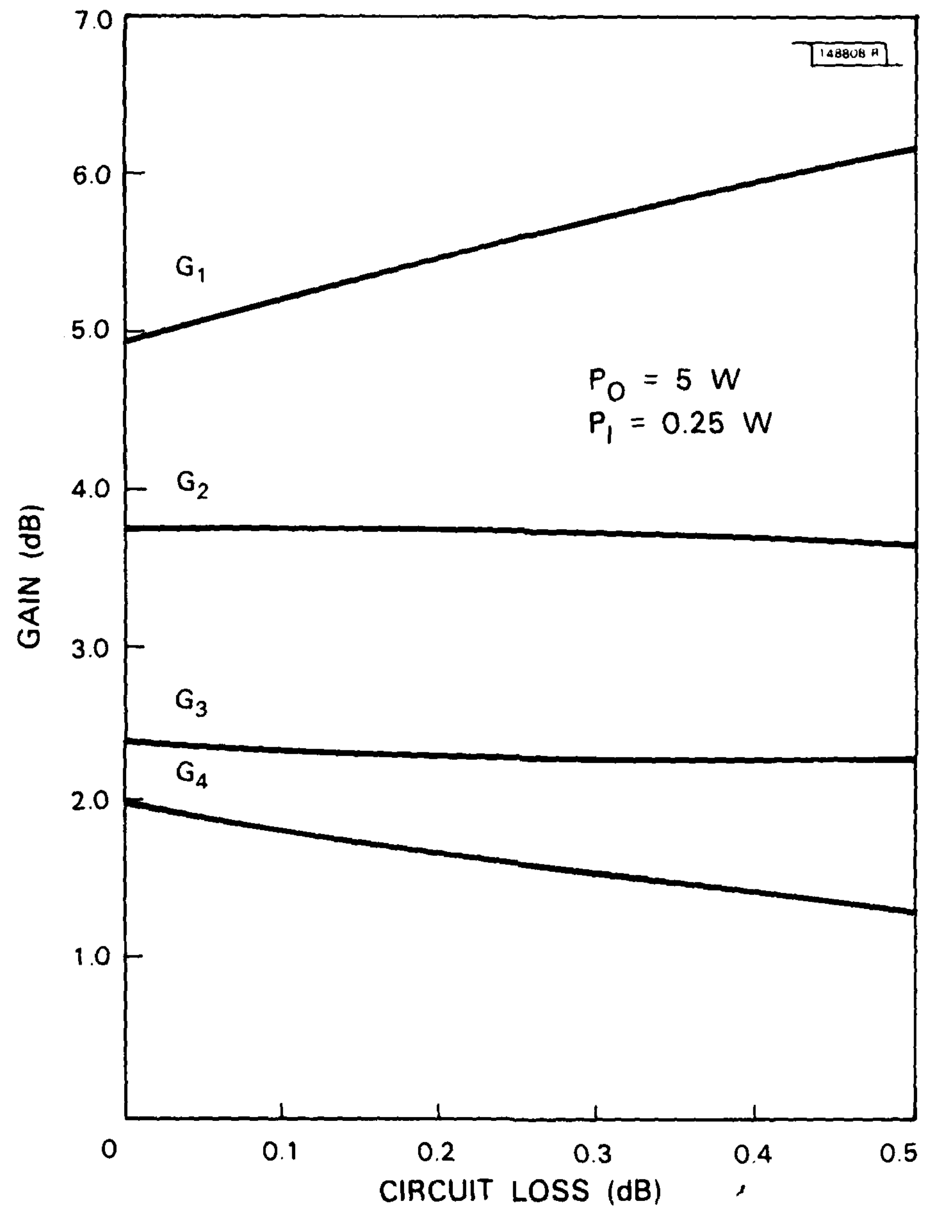


Fig. 16 Solid-state, EHF power amplifier design curves: gain per stage

Consequently, the output from each stage also increases. The largest proportionate increase, 1.3 dB, occurs in P_{01}. The rate of increase in the output power from the second stage is faster than that from the third stage, 1.2 dB and 0.6 dB respectively. The increase in P_{04} makes up for the losses in the combiner circuit to maintain the output at the required 5 watt level.

The added power per device and the added power per stage are shown in Figure 15. Added power per stage is the difference between the output power of the stage and the input power to that stage. Again, as circuit losses increase, added powers must proportionately increase. The added power from stage three decreases slightly since the rate of increase in output power from the second stage exceeds that from the third stage. The maximum added power, in excess of 2 watts, comes from the final stage. A reasonable value for circuit loss is $\alpha = 0.2 - 0.3$ dB. At these values the added power per diode is ~800 milliwatts, P_{A1} and P_{A3} are ~1 watt each, P_{A2} is slightly more, ~1.2 watts, and the fourth stage adds ~2.2 watts.

The gains of the four stages are shown in Figure 16. The first stage is required to produce the maximum gain, greater than 5 dB. The gains of the second and fourth stages are essentially steady 3.7 and 2.3 dB, respectively. The third stage is a high output power, low gain driver for the final stage; its gain is the lowest, ~1.6 dB.

Equations 4 through 14, Table 4, and Figures 14-16 were specific to the solid-state power amplifiers developed. It is interesting to see what output level is achievable with current state-of-the-art devices. Equation 9 is plotted in Figure 17. The added power as a parameter was varied from 0.5 to 1.2 watts. Although there exist silicon devices that are capable of higher power levels than those considered here, for reliability the added power should be limited to about the values shown. The input power was 0.25 watt. As can be seen from the dotted line, doubling the input power from 0.25 to 0.5 watt results in a few tens of milliwatts increase in the output.

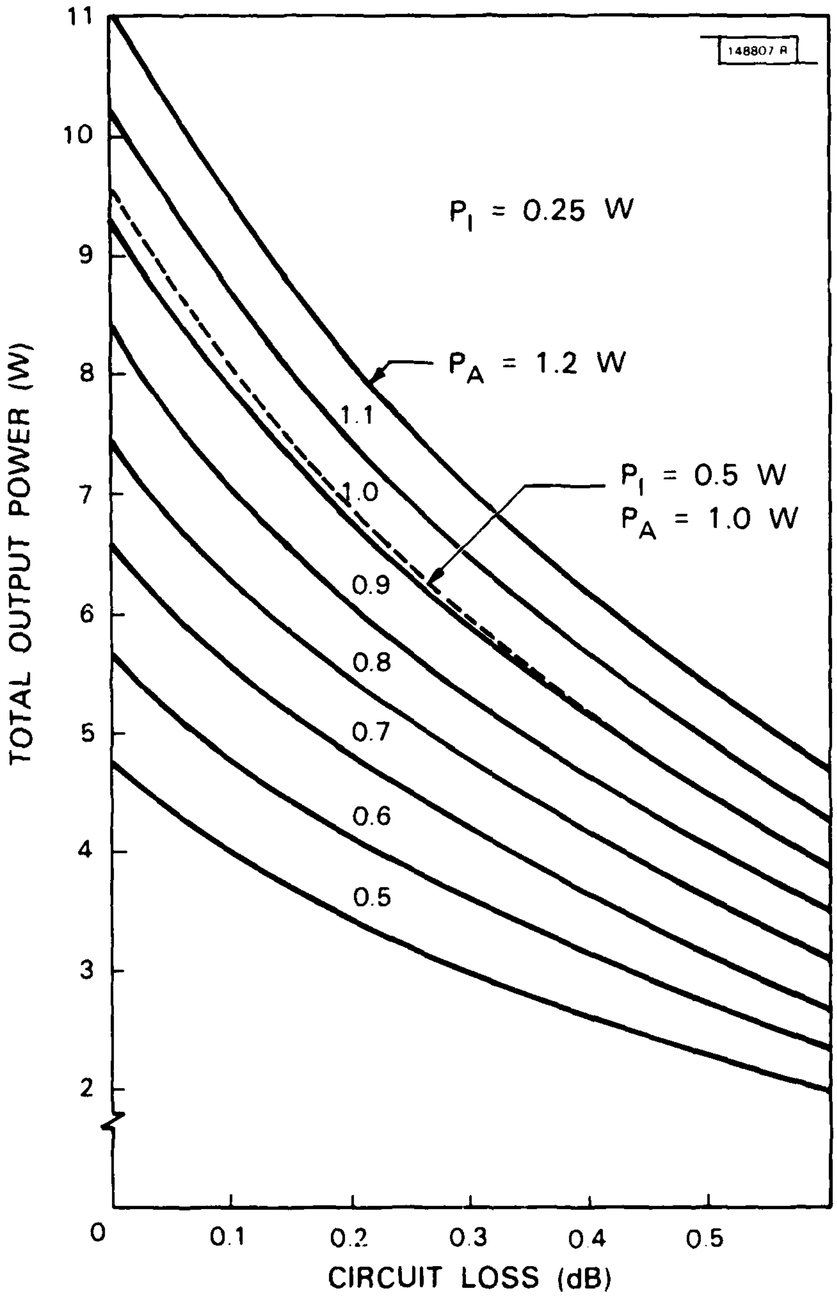


Fig. 17 Solid-state, EHF power amplifier design curves: total output power

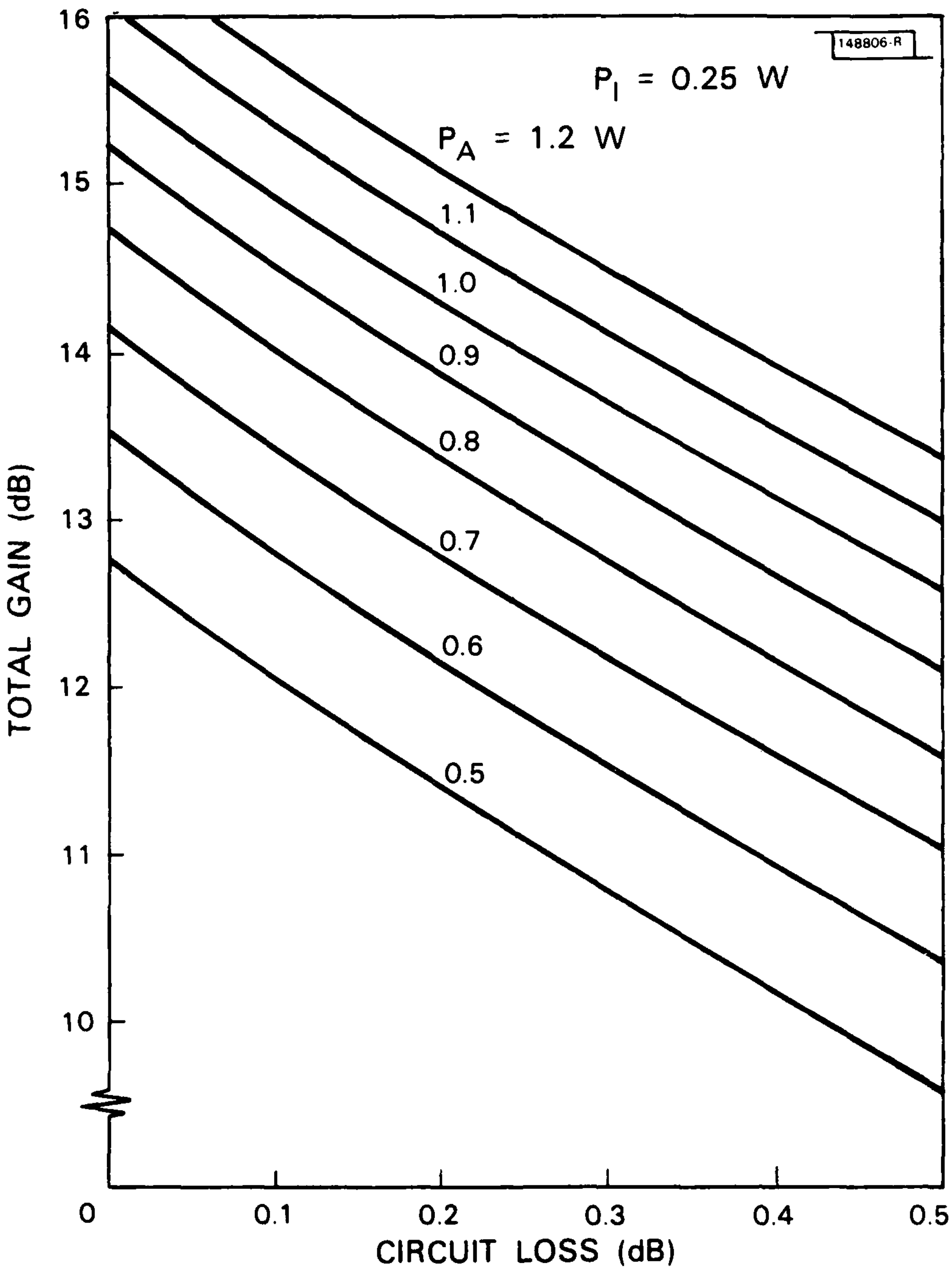


Fig. 18 Solid-state, EHF power amplifier design curves: overall gain

The minimum required added power is 525 milliwatts (see Figure 17) if there are no circuit losses. A realistic minimum value for circuit loss is ~0.1 dB. From Figure 17 and Table 4, an added power of 0.63 watt per device in such a low-loss circuit would produce 5 watts in the output. Maintaining good circuit efficiencies and using "hot" diodes, the solid-state power amplifier could achieve up to 9 watts of output power. Conversely, the minimum 5-watt required output could be achieved in a lossy circuit ($\alpha > 0.4$ dB) only with the most robust devices considered here.

The combined, total power gains of the four stages are shown in Figure 18 as function of the circuit losses, with added power as the parameter. For high values of added power and low circuit losses, up to 16 dB total gain is achievable. Conversely, the 13 dB required gain can be achieved in a lossy circuits only with the added power exceeding 1 watt per device.

Isolators, circulators, and power combiners form an integral part of any solid-state power amplifier. For an efficient design, the losses in these and other circuit elements must be minimized. In this design, the effects of losses per circuit element on added power, gain and output power per stage, total output power, and overall gain from an EHF solid-state power amplifier were evaluated. Uniform loss, α dB, per circuit element was assumed. The effects of amplitude and phase mismatches of unit amplifiers on combined output power are included in α for the hybrids. The required added power per device is 3/4 watt. The maximum gain is 6 dB. The output power per unit amplifier is 1 watt. Nine amplifiers meeting these criteria, embedded in a low-loss circuit where the circuit loss per element does not exceed 0.3 dB, produce 5 watts output power with 13 dB overall gain.

ACKNOWLEDGEMENT

Dr. Dean F. Peterson did the original design and development of the transmitter. David M. Snider is the Project Leader at MIT Lincoln Laboratory and was responsible for the overall design and development effort on the EHF terminal. His continued support contributed significantly to the success of this major breakthrough in solid-state transmitters at EHF. This project was under the sponsorship of USASATCOMA.

REFERENCES

1. Peterson, D.F., "A Device Characterization and Circuit Design Procedure for Realizing High-Power Millimeter-Wave IMPATT-Diode Amplifiers, "IEEE Trans Microwave Theory and Tech, MTT-21, 11, pp. 681-689 (1973).

2. Peterson, D.F., "Efficient, Broadband Circuit Performance of Millimeter-Wave IMPATT Diode Power Amplifiers," 1984 IEEE/MTT-S International Microwave Symposium, May 30-June 1, 1984, Los Angeles, CA.

3. Peterson, D.F., "Design and Performance of an 11 to 44 GHz Varactor Diode Quadrupler," to be published.

APPENDIX

SPECIFICATIONS FOR 5-WATT, SOLID-STATE, EHF TRANSMITTER

Output Frequency Range:	43.5 to 45.5 GHz minimum
Input Frequency Range:	10.875 GHz to 11.375 GHz
Input RF Power:	1 milliwatt ±5 dB
Output RF Power:	>5 watts, CW, 43.50 to 45.50 GHz and over entire input power range.
Stability:	Unconditionally stable. No RF output without input. No spurious output when input power is varied ±5 dB.
Devices:	Silicon, double-drift IMPATT diodes
Junction Temperature Rise:	Less than 225°C
Base Plate Temperature:	-20° to +65°C
Humidity:	100%, condensing
Altitude:	0 to 10,000 feet above MSL
Vibration:	Sinusoidal vibration swept in frequency from 5 Hz to 500 Hz and back down to 5 Hz
Duration:	The sweep time shall be linear for 15 minutes (5-500-5 Hz)
Test Axes:	Vibration shall be applied along each of three mutually perpendicular axes
Spectrum:	1.5g peak 5-60Hz, 20 dB per decade roll-off slope between 60 Hz and 500 Hz, i.e., 0.02 g peak at 500 Hz
Shock:	
Shape:	One-half (positive) sine
Amplitude:	4.2 g peak
Duration:	40 milliseconds for the half-cycle
Number:	One shock pulse per each of the three axes
Packaging:	Watertight enclosure, removable cover with cooling fins, neoprene gasket seal. Provisions for desiccant with humidity indicator and pressurizing with dry inert gas to 5 lbs/in^2. 3 1/4" x 8 1/4" x 11 1/4" w/o fins (fins add 2" to height)

Input Port:	SMA female, watertight, pressurizable
Output Port:	WR-22 waveguide, TE_{10} mode MIL-F-3922/67B-006; round, with threaded holes and alignment pins; mica window
DC Connector(s):	To be determined with packaging
Signal Connector(s):	On/off command and status monitor
Turn-on:	Full RF output within 3 microseconds after on-command which is a TTL compatible signal
Turn-off:	The bias current of sufficient number of IMPATT stages shall be reduced such that there is no thermal noise power output. No coherent RF output nor any spurious nor parasitic outputs within 3 microseconds after off-command (a TTL compatible signal).
On Time:	Normal operation is CW.
VSWR:	Input: 1.5:1.0 or better Output: 1.5:1.0 or better
Mismatch:	There shall be an isolator on the output of the transmitter such that the transmitter shall continue to operate into a SWR of 3.0:1.0.
Mounting:	Any position or orientation
Cooling:	Conduction cooling to baseplate
Turn-on:	Automatic, upon application of input DC potential(s)
Turn-on Transients:	To be stated by vendor
DC Input Power:	3.5 A @ 43V 1.5 A @ 12V
Weight:	15 lbs with heatsink in sealed box. Heatsink and enclosure weigh about 8 lbs.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER ESD-TR-84-298	2. GOVT ACCESSION NO. AD-A156933	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* 5-Watt, Solid-State, EHF Transmitter		5. TYPE OF REPORT & PERIOD COVERED Technical Report
		6. PERFORMING ORG. REPORT NUMBER Technical Report 715
7. AUTHOR*(s)* Stephen L. Zolnay		8. CONTRACT OR GRANT NUMBER*(s)* F19628-85-C-0002
9. PERFORMING ORGANIZATION NAME AND ADDRESS Lincoln Laboratory, M.I.T. P.O. Box 73 Lexington, MA 02173-0073		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Program Element No.33142A
11. CONTROLLING OFFICE NAME AND ADDRESS USA SATCOMA Ft. Monmouth, NJ		12. REPORT DATE 15 May 1985
		13. NUMBER OF PAGES 44
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)* Electronic Systems Division Hanscom AFB, MA 01731		15. SECURITY CLASS. *(of this Report)* Unclassified
		15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

None

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

EHF technology	RF power generation	IMPATT diodes
added power	reflection amplifier	circulator
unit amplifier	power combining	EHF transmitter
gated operation	frequency quadrupler	

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

A 5-watt, all solid-state, EHF, rugged, broadband transmitter has been developed for use in satellite-communication ground terminals. This state-of-the-art transmitter demonstrates efficient and cost-effective RF power generation at EHF for commercial and military applications. The specific center frequency and bandwidth (43.5 to 45.5 GHz) are matched to current military requirements. Measured results on the prototype unit are presented. Measured data on the combined outputs of two solid-state, EHF transmitters show 10.5 watts at 44.5f GHz, and the 1-dB bandwidth in excess of 5% (2 GHz). Development of the building blocks (the diodes, the unit amplifiers, the power combiners and the multiplier) are also discussed.

DD FORM 1473 1 Jan 73 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

DATE
ILMED
-8