REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
2b. DECLASSIFICATION / DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S) NPRDC TR 85-24
6a. NAME OF PERFORMING ORGANIZATION BioTechnology 6b. OFFICE SYMBOL (*If applicable*)	7a. NAME OF MONITORING ORGANIZATION Navy Personnel Research and Development Center
6c. ADDRESS (*City, State, and ZIP Code*) Falls Church, VA 22042	7b. ADDRESS (*City, State, and ZIP Code*) San Diego, CA 92152-6800
8a. NAME OF FUNDING / SPONSORING ORGANIZATION Deputy Chief of Naval Operations 8b. OFFICE SYMBOL (*If applicable*) OP-01	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (*City, State, and ZIP Code*) Washington, DC 20350	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO.: 63720N PROJECT NO.: Z1772 TASK NO.: WORK UNIT ACCESSION NO.: .011

11. TITLE (*Include Security Classification*)

ENRICHED HYBRID JOB PERFORMANCE AID DEVELOPMENT

12. PERSONAL AUTHOR(S)
Smillie, R. J., NAVPERSRANDCEN; Smith, M. G., Post, T. J., Sanders, J. H., BioTechnology, Inc.

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (*Year, Month, Day*)	15. PAGE COUNT
Final Report	FROM 81 Jan TO 81 Dec	1985 May	69

16. SUPPLEMENTARY NOTATION

17 COSATI CODES		
FIELD	GROUP	SUB-GROUP
05	05	

18. SUBJECT TERMS (*Continue on reverse if necessary and identify by block number*)

Job performance aids, performance aids, job satisfaction, user acceptance, hybrid aids, integrated job aids and training, integrated personnel system, job performance aid design, job performance aid research, job performance aid theory, maintenance training, enriched hybrid job performance aids

19. ABSTRACT

Two types of enriched hybrid job performance aids (EHJPA) were developed to help inexperienced technicians troubleshoot complex electronic systems: (1) the decision tree/functional flow logic diagram (DT/FFLD) for relay circuitry and (2) the state table/extracted schematic (ST/ES) for digital solid state circuitry. These hybrid aids contain more functional information than fully proceduralized aids but are easier to use than a technical manual. Technicians using the DT/FFLD aid isolated faults over twice as fast as technicians using ordnance publications, and they achieved almost twice the gain in system understanding. The ST/ES aid also improved performance, as evidenced by a comparison of troubleshooting protocols. Both aids provide succinct functional descriptions that tie theory of system operation to functional flow information needs.

20. DISTRIBUTION / AVAILABILITY OF ABSTRACT ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED
22a. NAME OF RESPONSIBLE INDIVIDUAL Smillie, R. J.	22b. TELEPHONE (*Include Area Code*) (619) 22506617 22c. OFFICE SYMBOL Code 71

DD FORM 1473, 84 MAR 83 APR edition may be used until exhausted. All other editions are obsolete.

NPRDC TR 85-24

MAY 1985

ENRICHED HYBRID JOB PERFORMANCE AID DEVELOPMENT

NAVY PERSONNEL RESEARCH
AND
DEVELOPMENT CENTER
San Diego, California 92152

NPRDC TR 85-24

May 1985

ENRICHED HYBRID JOB PERFORMANCE AID DEVELOPMENT

Robert J. Smillie
Navy Personnel Research and Development Center

M. Gregory Smith
Theodore J. Post
James H. Sanders

BioTechnology, Inc.
Falls Church, VA 22042

Reviewed and approved by
R. E. Blanchard

Released by
J. E. Kohler
Commander, U.S. Navy
Commanding Officer

Navy Personnel Research and Development Center
San Diego, California 92152-6800

SUMMARY

Problem

The presentations of troubleshooting data in technical manuals assume that the technician already has specific skills and knowledges, usually attained through both formal training and experience. This approach to system information puts a large burden on front-end training and assumes that inexperienced personnel will be slower and less productive on the job.

To facilitate troubleshooting by inexperienced technicians, fully proceduralized troubleshooting aids can be developed. However, they are costly and usually do not include the functional information needed to build an understanding of the system--the basis for applying troubleshooting skills to system problems not covered by job aids.

Earlier research demonstrated (1) the feasibility of hybrid troubleshooting aids that present both step-by-step procedures and reasons and (2) the potential for enriching hybrid aids with information designed to facilitate the transition from novice to expert technician. Format flexibility for different types of circuitry, however, has not been demonstrated.

Purpose

The purpose of this effort was to develop and evaluate enriched hybrid job performance aids (EHJPAs) that would (1) enable inexperienced technicians to troubleshoot electronic systems and (2) facilitate their transition to deductive reasoning from data in the technical manual as they gain experience. The EHJPA is an integral component of the Enlisted Personnel Individualized Career System (EPICS). In EPICS, inexperienced technicians use EHJPAs to acquire skills and perform tasks that are not normally accomplished so early in a career.

Approach

Two types of EHJPAs were developed, the decision tree/functional flow logic diagram (DT/FFLD) relay circuitry, and the state table/extracted schematic (ST/ES) for digital solid state circuitry. To evaluate the DT/FFLD, 13 instructors and 3 students used the DT/FFLD or conventional ordnance publications (OPs) for fault isolation. Solution rates, fault isolation times, and differences in pre- and posttest system understanding were measured. In addition, protocols for troubleshooting the same fault with OPs or the DT/FFLD were described so that search and decision behaviors could be compared. To evaluate the ST/ES aid, troubleshooting protocols using the aid, state tables alone, or OPs alone were delineated and compared based on discussions with three students and three instructors.

Results

Technicians using DT/FFLDs solved all the problems in half the time that technicians using OPs took to solve 75 percent of the problems. Technicians using DT/FFLD also achieved a 56 percent gain in system understanding on the posttest, compared to a gain of 27 percent by technicians using OPs. The feasibility of the ST/ES aid was indicated in the comparison of troubleshooting protocols, where fault isolation was demonstrated to be easier with ST/ESs.

Conclusions

Both the DT/FFLD and the ST/ES are effective troubleshooting aids. These aids, which contain enrichment information, can support inexperienced technicians during their earliest troubleshooting tasks. Over time, these technicians can be expected to gain the system understanding needed to use conventional technical documentation. These aids can also be used in formal school training to provide succinct functional descriptions of complex Navy electronic systems.

Recommendations

It is recommended that DT/FFLDs be developed for relay circuitry and that ST/ESs be developed for digital solid state circuitry. These aids can enable inexperienced technicians to troubleshoot these specific areas of circuitry and facilitate the growth of system understanding on the job or in formal school training.

FOREWORD

This research and development was guided by Navy Decision Coordinating Paper (NDCP) 63720N Z01772.011.01 (Enlisted Personnel Individualized Career System (EPICS), formerly entitled, Performance Aids Test and Evaluation), under the sponsorship of the Deputy Chief of Naval Operations for Manpower, Personnel, and Training (OP-01). the objectives of the NDCP are to define the state of the art in job performance aid (JPA) technology, develop a conceptual model for an integrated JPA-based personnel system including cost benefits and tradeoff analysis, test the JPA concept, and quantify performance increments and costs benefits obtainable for various applications.

This report is the ninth NAVPERSRANDCEN report dealing with JPA technology development: (1) NPRDC TR 77-33 presents seven papers assessing the state of the art in JPA technology, (2) NPRDC TN 78-6 describes a preliminary enlisted personnel system concept with major emphasis on the use of JPAs, (3) NPRDC TR 78-26 systematically reviews and organizes existing JPA techniques, related research data, and various applicable principles and concepts, (4) NPRDC TN 79-1 defines a JPA selection algorithm for an integrated personnel system, (5) NPRDC TR 79-25 discusses development of hybrid and enriched hybrid troubleshooting JPAs, (6) NPRDC TR 82-7 describes the development and test of a troubleshooting aid for digital systems, (7) NPRDC SR 83-32 describes a field evaluation of enriched hybrid troubleshooting JPAs, and (8) NPRDC SR 83-39 presents 12 papers delivered at an invitational conference on factors influencing JPA costs. The purpose of the present effort was to develop troubleshooting aids that would (1) allow inexperienced technicians to troubleshoot electronic systems and (2) facilitate the use of technical troubleshooting data. Results are intended for the JPA and technical documentation community.

Appreciation is expressed to the personnel of the Combat Systems Technical School Command, Mare Island, California and the Naval Guided Missile School, Dam Neck, Virginia for their cooperation in this effort.

J. E. KOHLER
Commander, U.S. Navy
Commanding Officer

J. W. TWEEDDALE
Technical Director

CONTENTS

LIST OF TABLES

LIST OF FIGURES

INTRODUCTION

Problem

The presentation of troubleshooting data in technical manuals assumes that the personnel using these data possess specific skills and knowledge usually attained through a particular course of instruction. These data are presented in a way to foster a general troubleshooting procedure with proficiency achieved through experience. This approach puts a large burden on front-end training and places inexperienced personnel at a disadvantage.

The Navy has and is acquiring technologically complex systems that, regardless of the sophisticated built-in test equipment (BITE) and automatic test equipment (ATE), will still require troubleshooting and fault isolation by technicians. The level of detail may change, but the process of fault isolation will not, provided the technician is still a part of the man-machine interface. Instead of fault isolation to a specific component, subassemblies may become the lowest level of fault isolation. BITE, ATE, and diagnostics will provide coverage for most of the troubleshooting. The technician, however, will still be required to troubleshoot, to some level, the remainder of the system.

Navy manpower, personnel, and training aggravate the troubleshooting problem. The available population from which enlistees are drawn is shrinking. The gap between entry level skills of enlistees and the skills required to maintain modern equipment continues to widen. Training costs are becoming prohibitive. Thus, there is a need for improving the troubleshooting process with an emphasis on using inexperienced personnel to troubleshoot successfully. Improvements can be made by providing the technician with the technical information in a format that will facilitate troubleshooting and allow proficiency to increase through experience.

Troubleshooting information can be presented in a fully proceduralized format to permit inexperienced users to troubleshoot. Fully proceduralized troubleshooting aids, however, are costly and are usually developed without the functional information the users need to obtain an operational understanding of the system (Potter & Thomas, 1976). The technical information in hybrid troubleshooting aids facilitates troubleshooting proficiency by providing (1) opportunities to learn, (2) challenges, and (3) meaningful work (Post & Price, 1972). In addition, the hybrid aid can be used by inexperienced personnel. Format flexibility, however, has not been demonstrated.

Purpose

The purpose of this research was to develop and evaluate enriched hybrid job performance aids (EHJPAs) that would (1) enable inexperienced technicians to troubleshoot electronic systems and (2) facilitate the technicians' use of more deductive technical troubleshooting data as they gain experience. Two types of EJHPAs were developed. Decision tree/functional flow logic diagrams (DT/FFLDs) were developed for relay circuits and state table/extracted schematics (ST/ESs) were developed for digital circuitry.

Background

Troubleshooting is a deductive process in which the technician makes a series of logical decisions based upon equipment readings and observations. For most systems,

troubleshooting is supported by technical manuals that contain the data necessary to isolate faults after the symptoms have been identified.

To become a competent troubleshooter, a technician must possess the skills and knowledge necessary to (1) understand the functional operation of a system and (2) use the available technical documentation to augment that functional understanding. Troubleshooting is a skill acquired over time. Although troubleshooting logic can be taught, knowledge of the system is attained from the technical documentation. After experience with the system, technicians develop their own unique troubleshooting strategies that are based on functional understanding of the system.

The troubleshooting data of the technical manuals have, over the years, been presented in a variety of formats that are supposed to provide the required functional understanding of the system. All of these formats, however, appear to be directed at the experienced technician.

If a population of high aptitude (for troubleshooting) individuals who can be trained with formalized courses and provided the experience necessary to develop expert troubleshooting skills is available, the various formats of technical manuals will probably be adequate. On the other hand, if, as in the Navy, the training costs have become prohibitive and the population from which to draw is small, the need exists for an alternative format that can be used by inexperienced technicians and that facilitates the acquisition of troubleshooting skills.

One alternative is to develop fully proceduralized troubleshooting aids that enable inexperienced technicians to troubleshoot (Serendipity, Inc., 1969). Unfortunately, the training cost savings will probably be offset by the increased technical documentation development costs, because the fully proceduralized job performance aids will have to include all possible symptom combinations (Potter & Thomas, 1976). In addition, continued reliance on fully proceduralized troubleshooting aids will not allow the technician to develop a functional understanding of the system and will eventually become a demotivator.

Nonfully proceduralized troubleshooting aids have been developed that describe the functional relationships of the system. These include FORECAST, JOBTRAIN, MAINTRAIN, FOMM, and the hybrid job performance aid, which are discussed below.

1. FORECAST (Shriver, Fink, & Trexler, 1964) was designed to incorporate subject matter expertise in the training of new technicians and the development of electronic maintenance data. It is a top-level breakdown approach to facilitate the fault isolation process that describes a logical flow through successive levels. FORECAST has decreased training time by 60 percent (Shriver, 1960) and improved performance (identified malfunctions) by 40 percent when compared to performance using conventional technical manuals (Shriver, et al., 1964).

2. MAINTRAIN (Rogers & Thorne, 1965), which was developed for improving troubleshooting performance by fully trained technicians, incorporated improved indexing techniques. Although training time was not reduced, 40 percent more malfunctions were identified.

3. In the JOBTRAIN (Gebhard, 1970) approach, job aids for electronic communication equipment were designed with input from experienced personnel. JOBTRAIN personnel were trained in 50 percent less time, but performed as well as conventionally trained personnel.

4. Functionally oriented maintenance manuals (FOMMS) have been developed for many years under various names (e.g., BAMAGAT, integrated maintenance concept (IMC), and symbolic integrated maintenance system or manual (SIMS, SIMM). The FOMM approach incorporates improved formatting of the technical data. Fault isolation with FOMM improved 30 to 40 percent (U.S. Coast Guard, 1964; U.S. Army, 1966).

Although all of these approaches attempt either to improve performance or reduce training time, none attempts to provide the technician the opportunity to transition to the more conventional and readily available schematics. One format that has been developed for troubleshooting and that satisfies the needs of the inexperienced user by providing the means to develop troubleshooting strategies is the hybrid job performance aid.

The hybrid job performance aid is a mixed level job performance aid that presents the information in two formats, directive and deductive. The purpose of a hybrid performance aid is to enhance performance on the job by allowing individual flexibility in troubleshooting. A secondary objective is incidental learning. Thus, inexperienced technicians can troubleshoot using the directive element and gradually transition to the deductive element as they gain a functional understanding of the system.

The EHJPA is a hybrid aid with amplifying information in either element, directive or deductive, or both. The additional information gives technicians the opportunity to learn more about their job.

The hybrid job performance aid concept, as first conceived by Post and Price (1972), consisted of combining two or more existing techniques while capitalizing on each technique's strong points and minimizing their weak points. This combination would provide two levels of troubleshooting data: a directive element for inexperienced technicians and a deductive element for experienced technicians. Post and Price (1973) described the key component of the hybrid troubleshooting aid as designing the interface between the two elements so that "with continued usage, the inexperienced technician will gradually become proficient in troubleshooting with only the deductive element" (p. 11).

Evaluation of the EHJPA concept (Post & Smith, 1979; Smith, Post, & Smillie, 1983) demonstrated that subjects were able to transition from the directive element of the EHJPA to the deductive element after several trials. In a field study, Smith et al. (1983) compared the categories of enrichment and found that the additional information, which was integrated with--and referenced--the technical manuals, enhanced the acceptability of the EHJPAs by the users.

DESCRIPTION OF THE EHJPAs

Decision Tree/Functional Flow Logic Diagram (DT/FFLD)

The directive element of the EHJPA for the relay circuit has multiple decision trees (DTs), while the deductive element has a single block diagram, the function flow logic diagram (FFLD). The DT/FFLD directive element is a series of independent decision trees. Each decision tree is accompanied by symptom statements. Thus, the choice of which decision tree to use depends upon the symptoms observed. Figure 1 shows an example of the directive element. Hexagons enclose the decision points that determine branching in the decision tree.

TRAIN

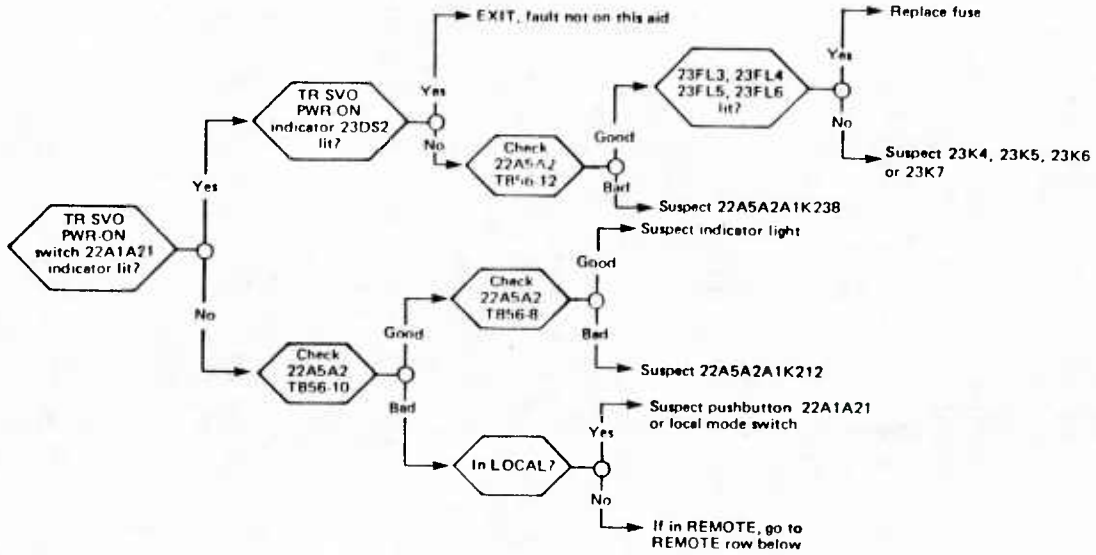
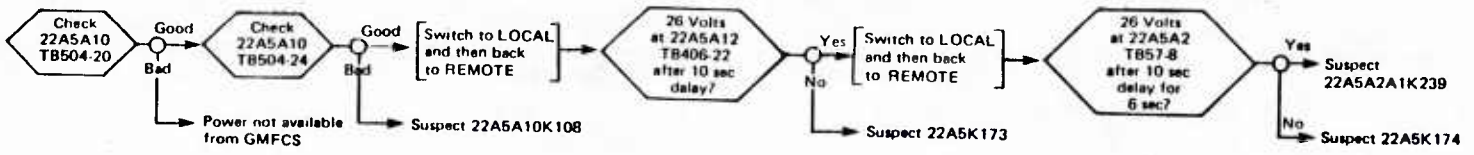
Symptom	Procedures
Launcher will not train.	
In REMOTE mode: Launcher will not train or elevate; TR and EL STOW LOCK DISENG Indicators not lit; and TR and EL SVO PWR-ON Indicators are not lit.	

Figure 1. Directive element of a DT/FFLD aid.

Figure 2, which is the FFLD that corresponds to the DT example in Figure 1, represents the sequential arrangement components. Each block represents a component and lists the nomenclature and reference designation for that component. The FFLD is integrated with the technical manuals that support the system. The alphanumeric in parentheses near each block (see callout A on Figure 2) is the grid coordinate location of that component in the fault diagram of the related technical manual, OP 4006, Vol. 2, Part 2. In addition, each EHJPA is identified by its related figure number in the technical manual (callout B). Test points are labeled with their complete identifying alphanumeric. A legend (callout C) on each FFLD defines the component symbols. Enrichment is added to each EHJPA by including paragraph references of relevant operational descriptions from the technical manuals (callout D).

In the DT/FFLD EHJPA, the directive element is designed for inexperienced technicians to use to troubleshoot. Then, over time, these technicians should become familiar with using the FFLD to trace the actions illustrated by the DT, as well as gain a functional understanding of the system. Since the EHJPA is integrated with the fault/logic diagrams in the technical manual, technicians should also become familiar with system nomenclature, relay troubleshooting logic, and procedures. Eventually technicians should be able to make the transition to using only the technical manuals for troubleshooting.

State Table/Extracted Schematic (ST/ES)

The directive element of the EHJPA for solid state circuits has state table (ST) information while the deductive element has schematic information. The ST is coupled with a troubleshooting guide that directs the technician through various tests, checkpoints, and procedures. Following the procedural information of the troubleshooting guide, the technician is referred to a particular ST. With an ST (see Figure 3), the technician starts with the column on the far left and works to the column on the far right. For each column, the technician uses the CARD AND PIN NUMBER information to locate the correct test point and then the STATE information (CLOCK 1, CLOCK 2, etc.) to determine when the values listed in the cell (0 or 1) will occur. The technician continues to move to the right until a mismatch is encountered.

The remaining information on the ST, SIGNAL NAME and ACTION/COMMENT is enrichment information. This information is not needed to solve a straight-forward problem but is intended to explain what is occurring--thus providing the technician a functional understanding of the system. The extracted schematic (ES) was developed to make this information more meaningful as well as to help technicians understand how an instruction is executed and to help in troubleshooting with the ST. The test point numbers are used to link the information on the ST with the representative circuitry on the ES.

An ES (see Figure 4) identifies only the circuits involved in executing a particular instruction. While troubleshooting, technicians should be able to use the enrichment on the ST to follow the sequence of events on the ES. The ES is designed to provide the information the technician needs to understand how to isolate the fault. Similar to the DT/FFLD, the ST/ES is integrated with the technical manuals (technical manual page numbers are given on the ST) and should foster transition from the directive ST to the deductive ES and eventually to the relevant technical manuals.

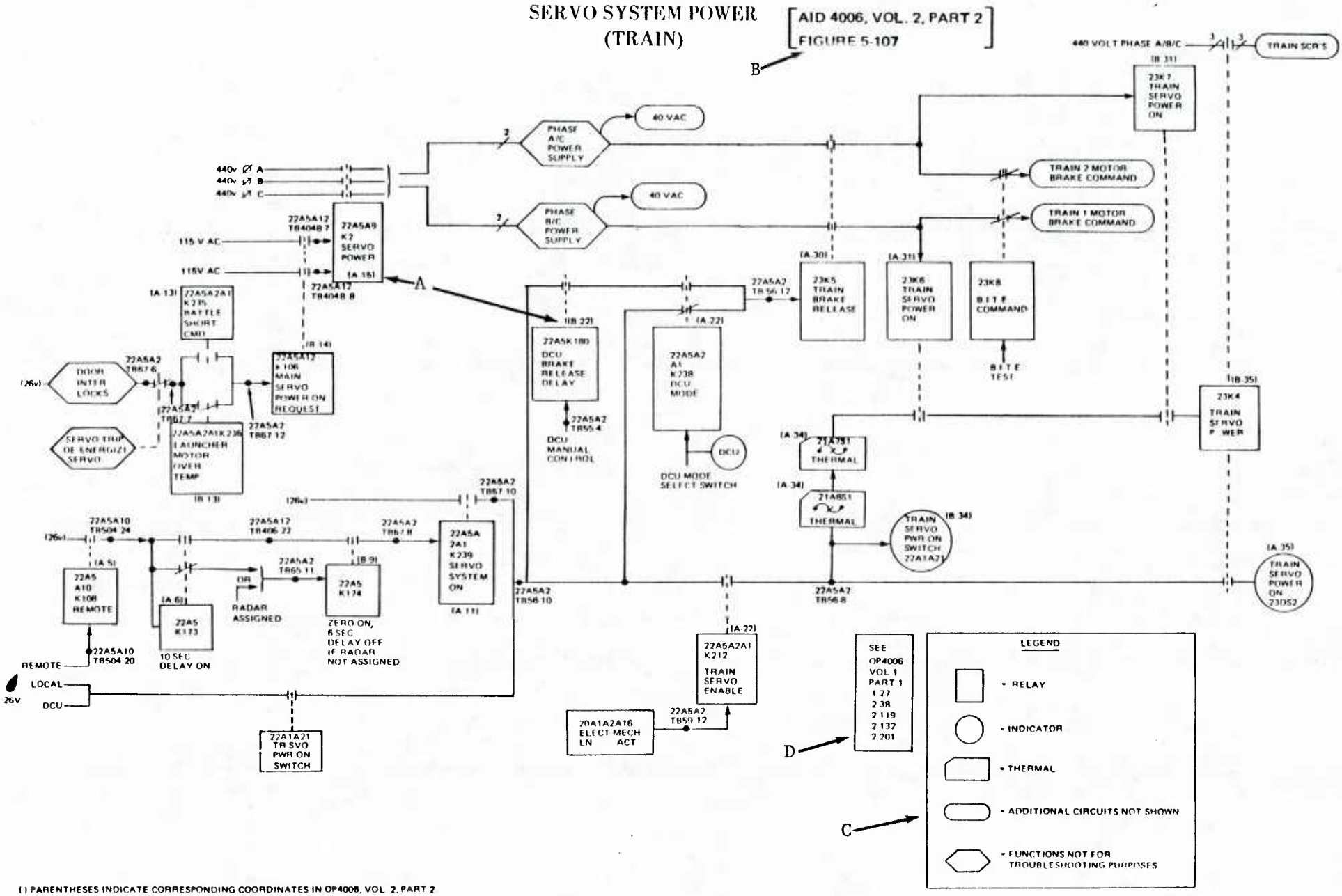


Figure 2. Deductive element of a DT/FFLD aid (directive element shown in Figure 1).

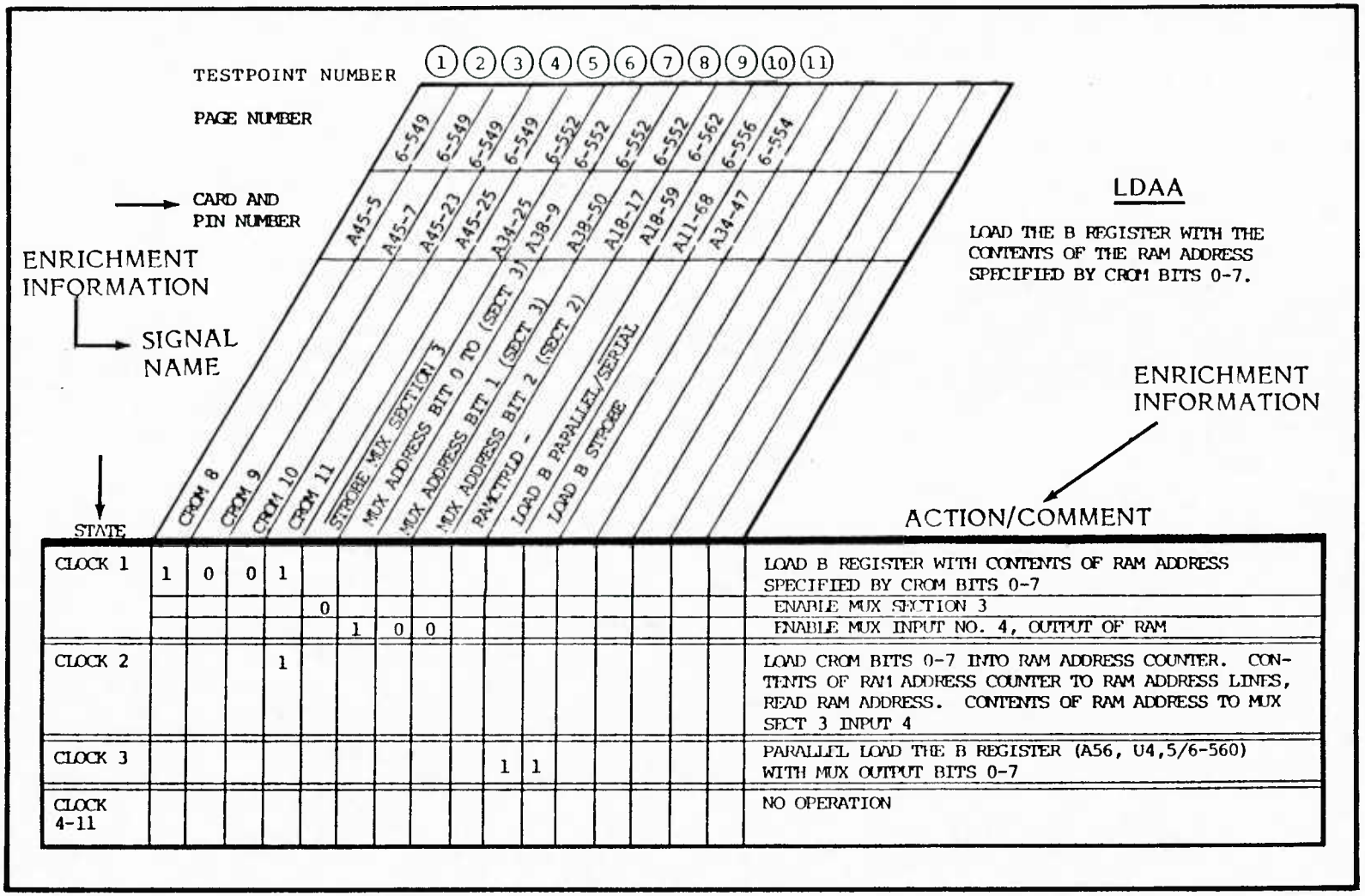


Figure 3. Sample state table (ST).

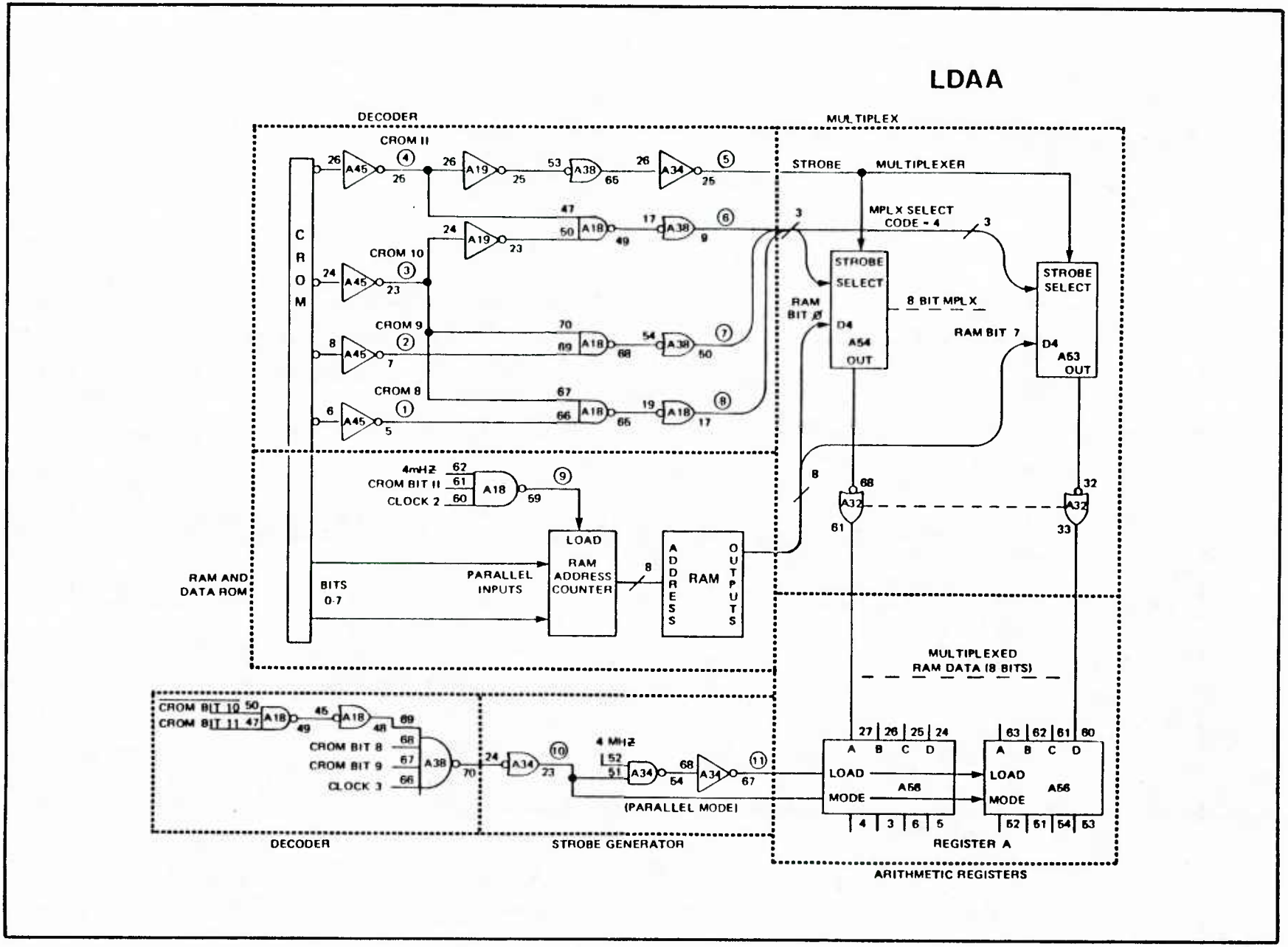


Figure 4. Example of an extracted schematic (ES).

APPROACH

EHJPAs were developed for relay circuitry, the DT/FFLD, and for solid state circuitry, the ST/ES. Samples of each EHJPA type were evaluated.

DT/FFLD EHJPAs

Subjects

For the DT/FFLD comparison, the subjects were 16 fire control technicians (FTMs), who were tested at two locations: eight at the Guided Missile School, Dam Neck, Virginia and eight at the Combat Systems Technical Schools Command, Mare Island, California. Thirteen subjects were instructors and three were students in the NATO SEASPARROW Surface Missile System (NSSMS) Fire Control System Mk 29 course. There were nine FTM3s, two FTM2s, four FTM1s, and one FTMC.

Six subjects were rated high in electronics experience because they had attended both FT "A" and NSSMS "C" schools and had shipboard experience. Seven were rated medium because they had attended the same schools as the high-rated subjects but had no shipboard experience. Three were rated low because they were students and had only attended the FT "A" school. Thus, six subjects had a high level of experience and 10 had little or no experience.

Materials

Six DT/FFLD EHJPAs were developed for relay circuitry in the maintenance interconnect cabinet (MIC) of the NSSMS. The MIC is the only cabinet in the NSSMS having substantial amounts of relay components. The EHJPAs for the MIC address all the major relay portions of the MIC. Those functions consisting of relay components of the MIC not covered by the aids are considered to be straightforward. Thus, development of EHJPAs for those components was viewed as providing little that might contribute to the technician's comprehension of the MIC circuits.

The MIC operates in three modes, LOCAL, DCU, and REMOTE. Some relays are dedicated to only one mode while other relays are used in more than one mode. A finite number of functions are performed in each mode. Once the mode and the functions required by that mode were identified, the combination of relays in the MIC that are used to accomplish that function were specified and their circuit paths drawn.

The development of the FFLD is discussed below:

1. Major functions were identified. If the circuitry for the major function could not be condensed to fit on a single page, smaller functional units were identified.

2. All the components and circuit paths relevant to all functional units were identified in the conventional documentation.

3. The appropriate circuits were redrawn so that component placement paralleled the functioning of the smaller unit and provided the information necessary to illustrate how the smaller units were related to the major function units.

The rationale for this approach was to accelerate the troubleshooting understanding and logic when the functional unit was not operating correctly. Figure 5 shows the FFLD for the servo system power (elevation) functional unit, which elevates the launcher. When a casualty does occur, the technician should be able to use the aid to determine which components are or are not influenced by a given mode. Figure 5 shows that only the

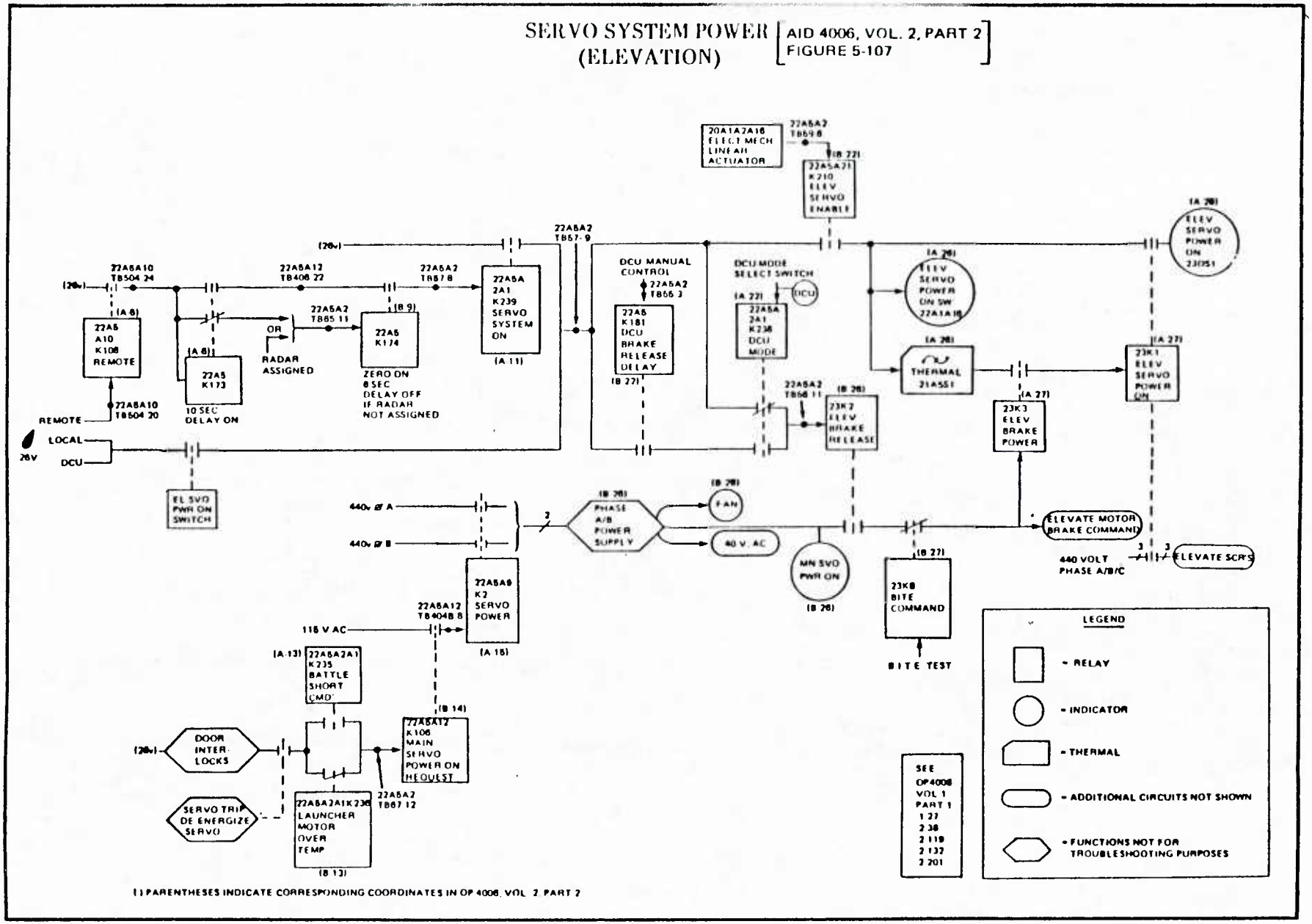


Figure 5. FFLD of the DT/FFLD aid for the servo system power (elevation) functional unit.

REMOTE mode influences the K106, K173, K174, and the K239 relays. If the launcher can be elevated normally in LOCAL/DCU but not in REMOTE, the amount of suspect circuitry is reduced. Likewise, a casualty in the remaining circuit would be evident in all modes.

As the functions were identified and described for FFLD, the symptoms of failed function were used to develop the directive element, the DT. For each component failure within a given function, there are a finite number of symptoms.

In building the directive element of the aid, the types of symptoms for that function were first categorized. For example, the servo system power (elevation) exhibits symptoms involving launcher movement (the launcher does or does not elevate), indicator lights (indicator lights are or are not illuminated), and mode (failure in REMOTE or DCU/LOCAL). By using combinations of these three types of symptoms, the suspected causes of the casualty are reduced. Consequently, the DTs on the directive element for the associated FFLD are quite short.

The meaningful combination of symptoms was identified and placed on the directive aid. Figure 6, which illustrates the directive element for the servo system power (elevation), shows the list of symptoms and DTs. Inexperienced technicians would enter the directive element of the EHJPA via the symptom column, locate the row with the correct symptom(s), and follow the troubleshooting instructions on the DT.

The DT should save the technician troubleshooting time. Which circuits belong to which symptom has already been thought through and the correct test points have been included in the decision tree. The order of testing the test points in the DT should provide a troubleshooting logic. With practice, the technician should be able to identify on the FFLD which circuits belong to which operation, why a given casualty produces a particular combination of symptoms, and why the DT represents a good troubleshooting logic.

The EHJPAs were developed using the fault oriented interconnecting diagrams (FOIDs) in OP 4006, Vol. 2, Part 2; Table 5-4, Maintenance Turn-on Procedure, in OP 4006, Vol. 2, Part 1, pages 5-22 through 5-26A; the theory of operations descriptions in OP 4006, Vol. 1, Part 1; and civilian and Navy subject matter experts.

Test Procedures

A between-subjects test design was selected to eliminate the possible differential confounding effects of using one type of technical documentation prior to using a different type. Subjects were divided into two groups, one using DT/FFLDs and the other using OPs. Each group contained three fire control technicians with a high level of experience and five with little or no experience. The sequence of events comprised (1) a system understanding pretest, (2) five troubleshooting tasks, and (3) a system understanding posttest. Although six DT/FFLDs had been developed, only the servo system power (elevation) was used in the evaluation.

The independent measures were solution rates, fault-isolation times, and the differences in the pre- and posttest system understanding scores. If the subject was unable to determine the casualty within the 40-minute time limit imposed for each troubleshooting, the trial was scored as no solution. There were no time limits for the paper-and-pencil test.

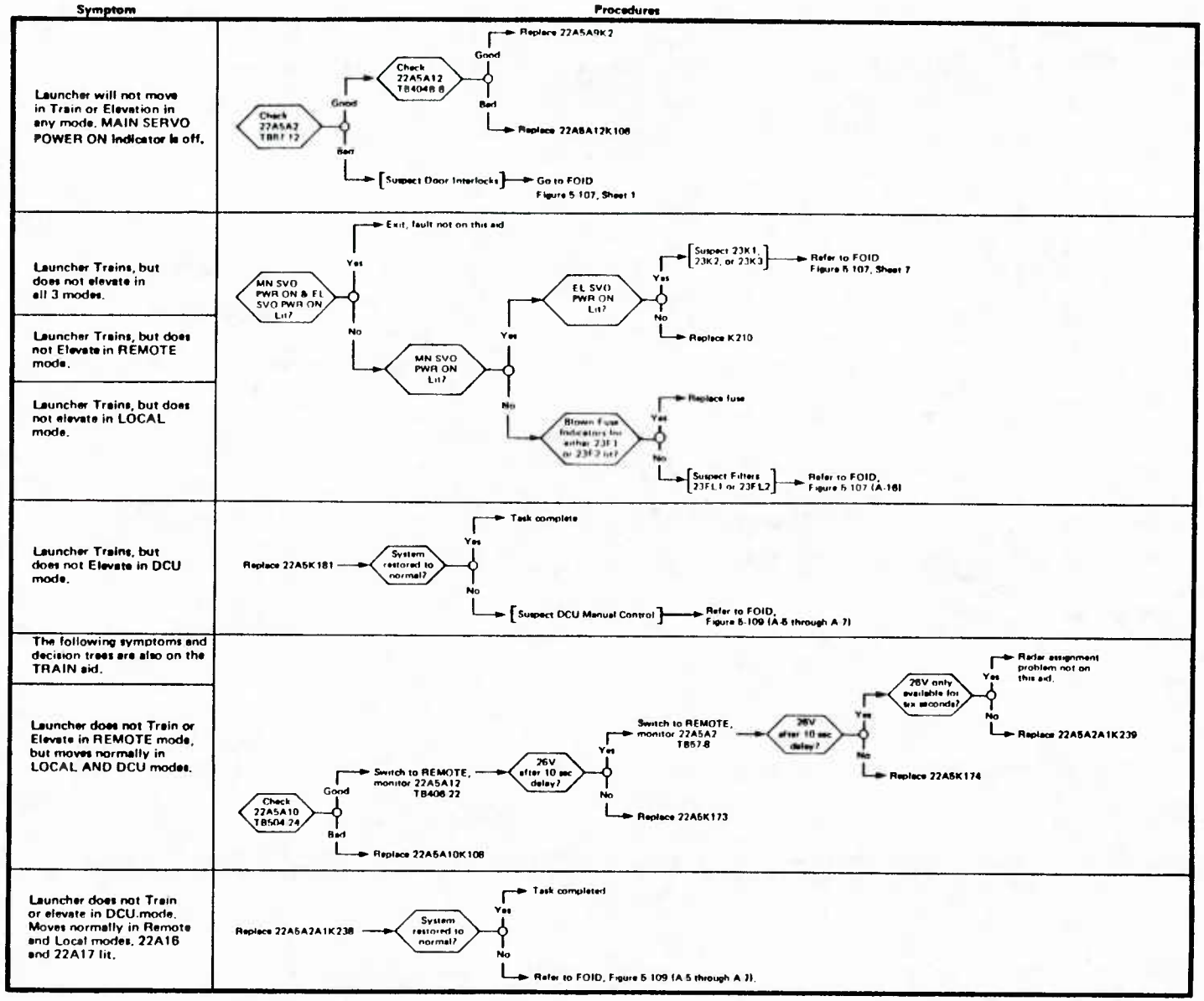


Figure 6. DT of the DT/FFLD aid for the servo system power (elevation) functional unit.

It was considered important to compare performance measures when evaluating technical information formats as well as to analyze the functional differences between the formats. Thus, two troubleshooting protocols were delineated and compared--in one the OPs were used to support troubleshooting; in the other, DT/FFLD EHJPAs were used. These protocols were the basis for a functional analysis that compared the search and decision behaviors that both experienced and novice FTMs might exhibit when troubleshooting using either OPs or DT/FFLD EHJPAs for support. Subject matter experts determined the troubleshooting path and identified the troubleshooting parameters that would be required to isolate the hypothetical failure. Based on the technical information needed to isolate the failure, the two protocols were contrasted.

To evaluate the efficiency of design, a page count comparison was also made. All the OP pages needed to develop the six DT/FFLDs were totaled and compared to the total number of DT/FFLDs needed to portray the same information.

ST/ES EHJPAs

Subjects

For the state table/extracted schematic (ST/ES) demonstration, six subjects from the Guided Missile School, Dam Neck, Virginia were used. Three subjects were instructors, either gunner's mates (missiles) first class (GMM1) or FTM1s, and three were students, FTM3s, for the NSSMS.

Materials

Eleven ST/ESs were developed for the solid state circuitry of the missile control unit (MCU) in guided missile launcher control Mk 29 of the NSSMS. To understand the development, it is necessary to understand the relationships among BITE tests, jump waveforms, instructions, subroutines, and check points.

The BITE tests are hardwired into the MCU. Each performs a specific sequence of tests to determine if the instructions in the MCU are correct. This sequence never varies and, upon reaching the last test, the BITE test is programmed to cycle back to the first test and go through the test sequence again. The recycling continues until the BITE test is halted.

When the jump test card is placed into Slot A62 of the MCU, the oscilloscope is set up and connected to the jump test card, and BITE Test A is run, a signal of high and low values is generated. If all instructions are working properly, the waveform on the oscilloscope will look like the jump waveform given in the OP and shown in Figure 7.

If a casualty is present, the waveform will differ from that shown in Figure 7. The points at which the actual waveform differs from the jump waveform is the starting point for the troubleshooter. As seen in Figure 7, the jump waveform has been drawn on top of a grid or matrix. Each cell of the grid along the jump waveform represents one instruction. The high or low value for each cell represents the output of the test point being monitored as a result of being (or not being) modified by that instruction. An instruction is one sequence of events to accomplish a given function. When the execution for one instruction is completed, the program moves to and executes the next instruction and so forth.

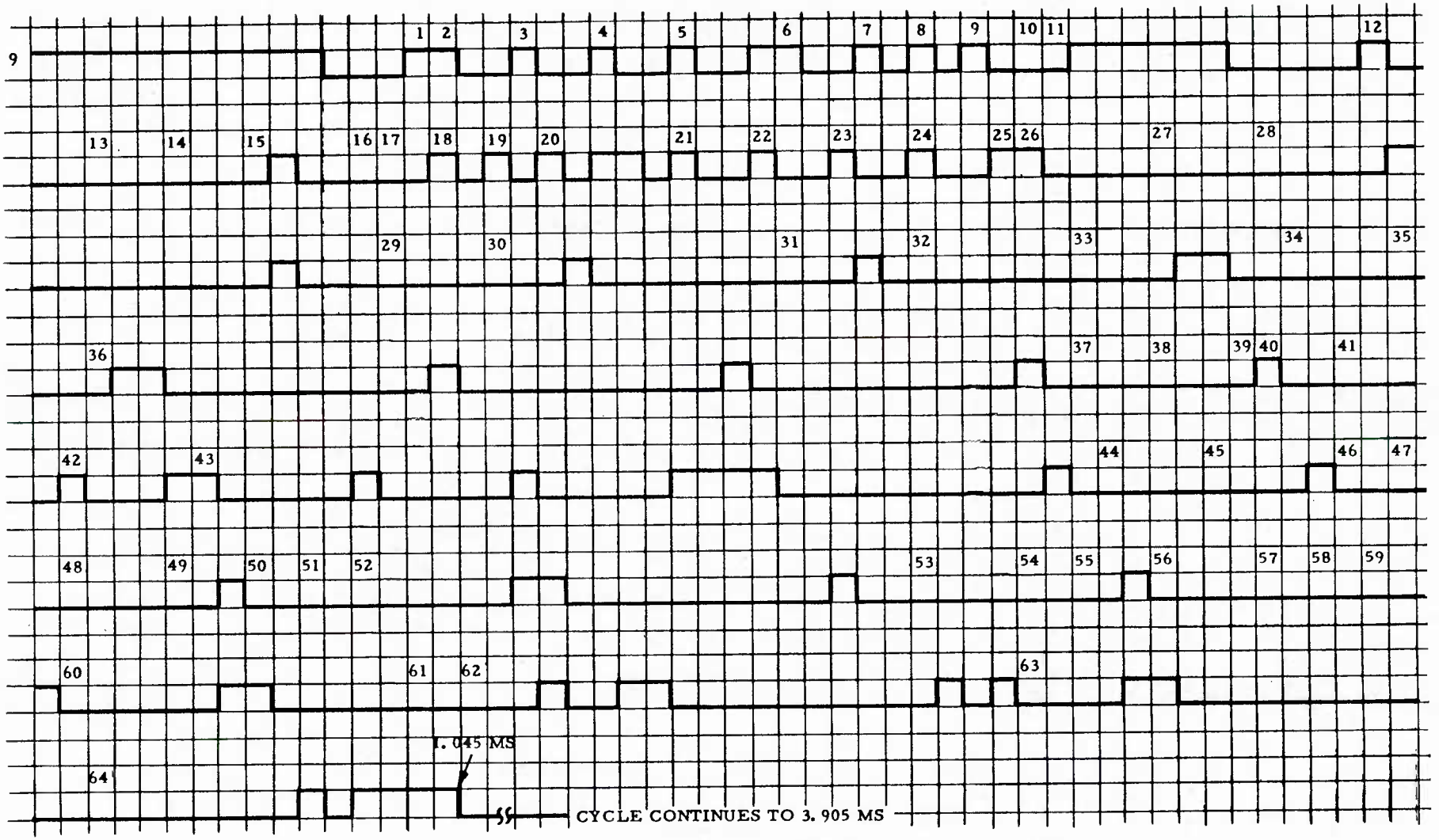


Figure 5-18. BITE Checkpoints Waveform (Jump Signal)

Figure 7. Jump waveform for BITE Test A.

The solid-state-circuit EHJPAs were developed using the MCU state tables and troubleshooting guide, logic diagrams (schematics) of OP 4006, Vol. 2, Part 3, and the operation diagrams in OP 4006, Vol. 1, Part 2. One ST/ES aid was developed for each of 11 state instructions.

Figure 8 shows the ST for the LDAA instruction. Test points for the instruction were numbered consecutively across the columns beginning with the column on the far left. In this example, there are 11 columns and, therefore, 11 possible test points. The arrow in Figure 8 points to the circled test-point numbers that were added above the columns.

The first step in developing the LDAA ES was to identify the relevant OP page numbers of the logic diagrams from the LDAA state table. In this instruction, only four OP pages are listed: 6-549, 6-552, 6-554, and 6-562 of OP 4006, Vol. 2, Part 3. Next, the card and pins that are used as test points were located on the logic diagrams. As each test point was located, it was given the test point number corresponding to the column number.

The four logic diagram pages were laid out to correspond to the flow path and not by consecutive pages. For example, the LDAA circuit corresponds to the page relationship shown in Figure 9. The pages are laid out and the ES was constructed according to that layout pattern. Figure 10 shows the completed LDAA extracted schematic with components found on a given OP page circled and labeled with the appropriate OP page number.

Paths between test points were determined. Many times the output of a component branched to several other components. To determine the branches relevant to a particular instruction required programming expertise or a subject matter expert.

After determining the flow pathways between the original four logic diagram pages, additional circuitry was needed to complete the aid. The information to find the location of these additional circuits was in the margin of the logic diagram pages. Thus, while the ST identified four pages in OP 4006 as relevant to the LDAA instruction, three additional pages were needed to complete the ES.

After the complete circuit had been identified, the ES was drawn and arranged so that functional blocks could be identified. The LDAA operation diagram found in Figure 2-74 on page 2-656 of OP 4006, Vol. 1, Part 2 (see Figure 11) was used to decide where to draw the functional blocks.

Figure 11 cannot be used for troubleshooting because there are no card and pin numbers. However, they do give the flow between functional units. The components on the ES were grouped, boxed, and labeled using this information.

Figure 11 also includes the timing information. Each instruction has 11 clocks (cycles or pulses) that are generated by a 4 MHz clock. One cycle, which consists of one low followed by one high, equals one clock. The 11 clocks for this instruction are shown on the left side of the operation diagram shown in Figure 11. Although 13 waveforms are listed, two (labeled Clocks 2 and 3) were repeated from the 4 MHz waveform to make it easier to see where Clocks 2 and 3 begin. The remaining 11 waveforms correspond to the signals listed in the 11 LDAA ST columns (Figure 8) and the names of the 11 signals are the same as on the operation diagram (Figure 11). The timing information for the ST can be derived from the operation diagram (Figure 11).

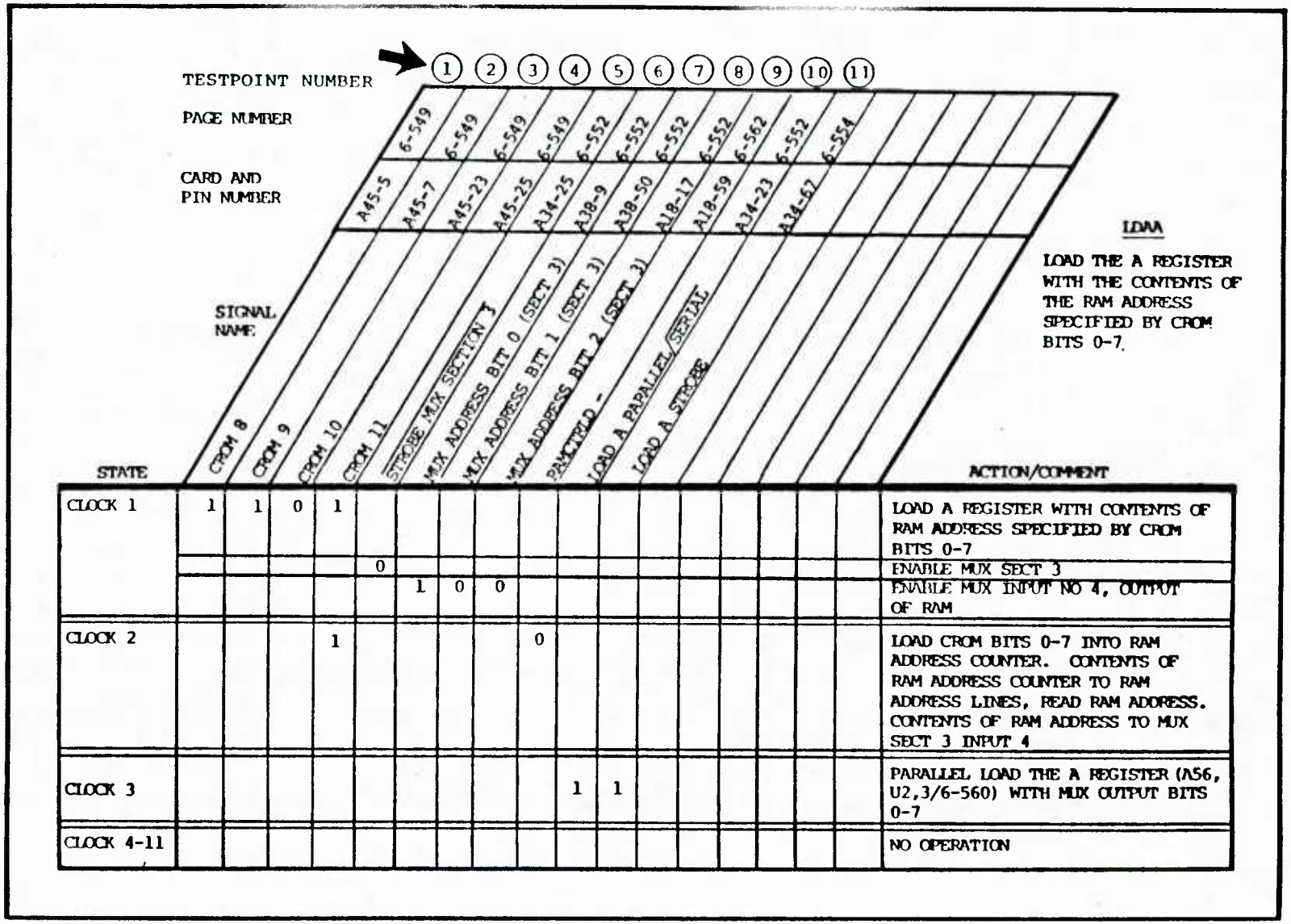


Figure 8. LDAA ST with test points numbered consecutively.

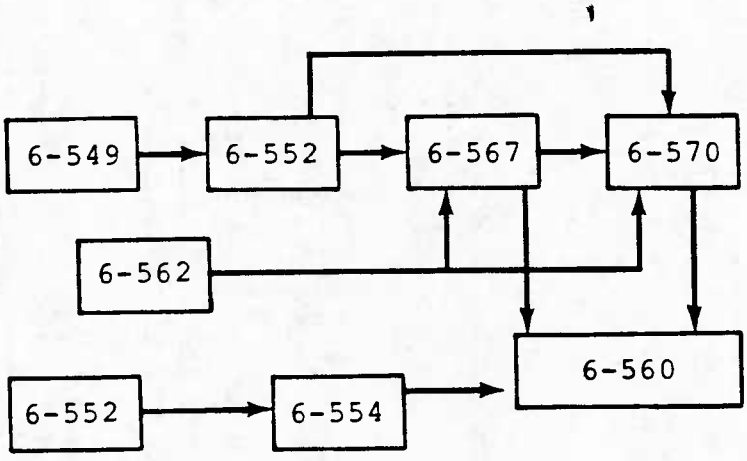


Figure 9. Layout of relevant OP 4006 pages corresponding to flow path.

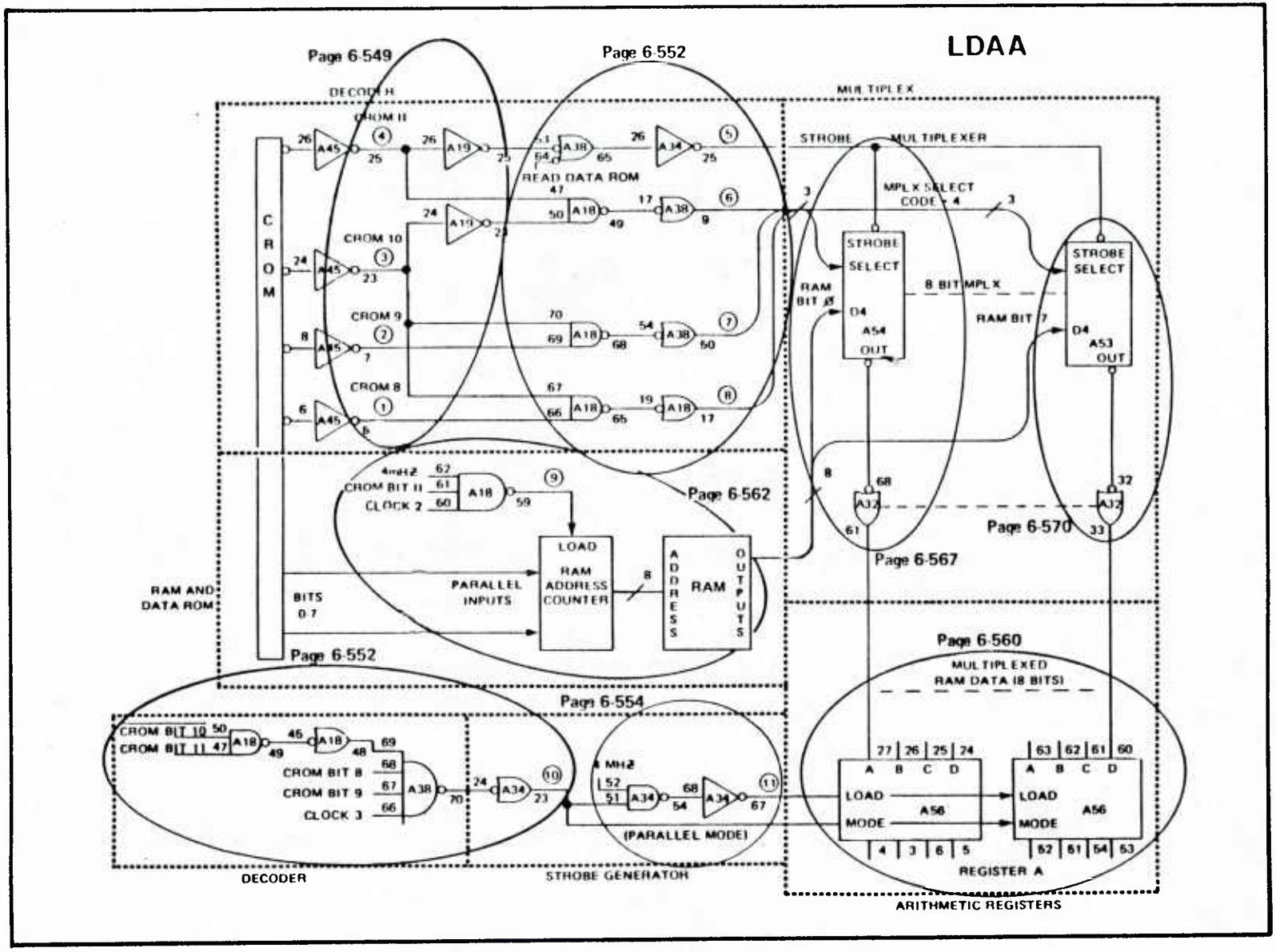


Figure 10. Completed LDAA extracted schematic. Components located on same logic diagram page are circled and labeled with OP page numbers.

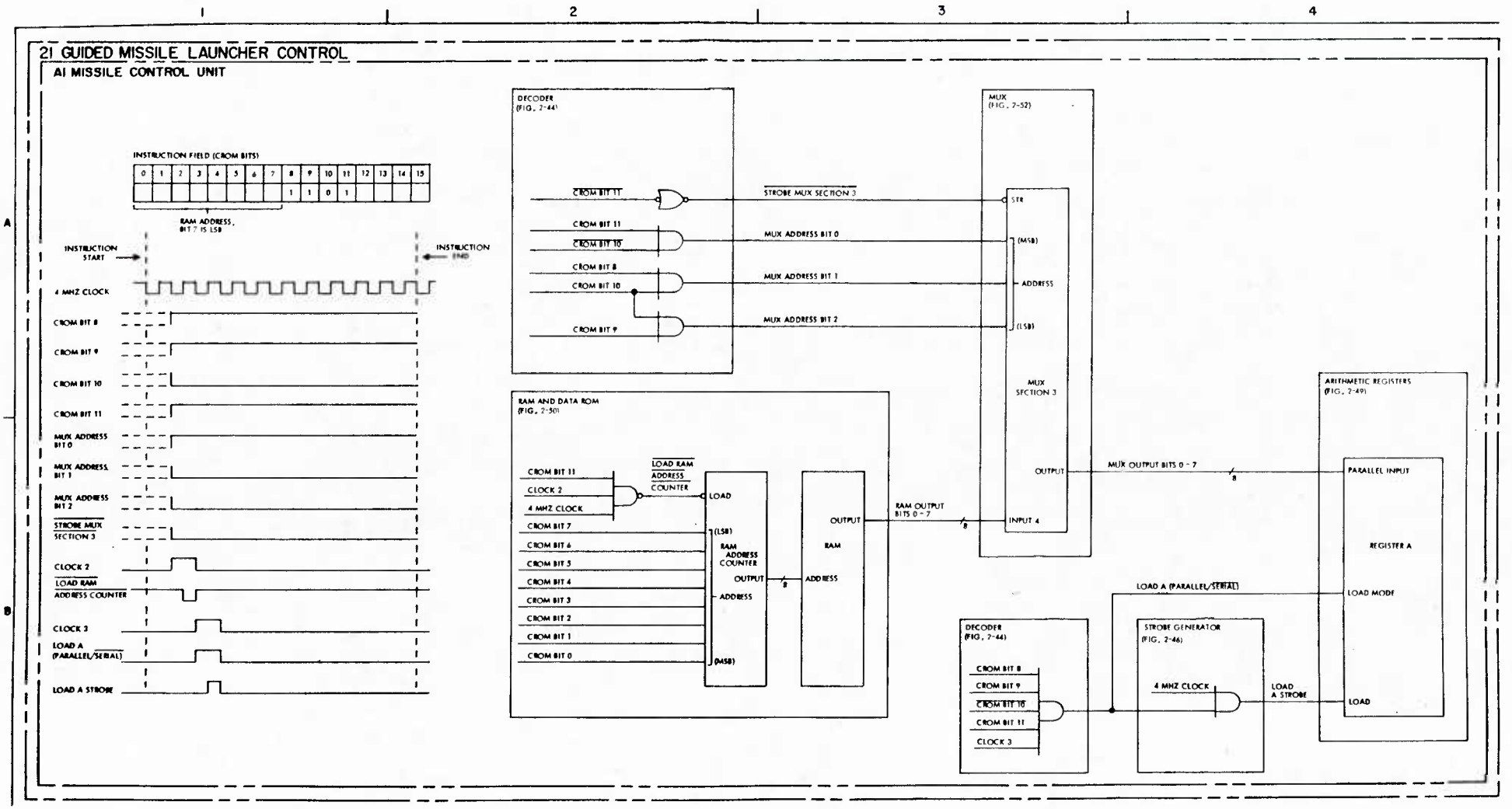


Figure 2-74. LDAA Instruction, Operation Diagram

Figure 11. LDAA operation diagram (taken from OP 4006, Vol. 1, Part 2, page 2-656).

Demonstration

An earlier study (Smillie & Porta, 1981) showed that STs were effective troubleshooting aids in comparison to OPs. Thus, this demonstration was conducted to evaluate the ease of using the ES. The six subjects tried to isolate hypothetical faults in the MCU using the ST/ES, ST, or OP and were evaluated according to whether or not the malfunction was isolated. No descriptive statistics were collected.

As in the OP-DT/FFLD functional comparison, protocols were constructed for hypothetical failures. Subject matter experts determined the troubleshooting path and identified the troubleshooting parameters necessary to define the technical information required to isolate the failure. Since three types of technical information were available, OP alone, ST alone, or ST/ES EHJPA, three protocols were analyzed.

Similar to the DT/FFLD, page count was compared to evaluate efficiency of design. All OP pages needed to develop the ST/ESs were totaled and compared to the total number of ST/ESs needed to portray the same information.

RESULTS

DT/FFLD EHJPAs

Solution Rates

The mean solution rates for each task and for overall performance for the two groups are presented in Table 1. The grand means indicate that the DT/FFLD EHJPA group isolated faults within the time limit in contrast to only 75 percent of the OP group. There were five troubleshooting tasks for each individual or a total of 40 tasks for each group. The OP group isolated the fault in only 30 of the 40 casualties.

Fault-Isolation Times

The mean fault-isolation times for each task and for overall performance for the two groups are also shown in Table 1. The grand means indicate that the OP group took 11.4 minutes (24.0 vs. 12.6 minutes) longer to isolate the faults than did the EHJPA group.

System Understanding Test

Table 2 gives the mean results of the system understanding test. Again the EHJPA group performed better than did the OP group. The ability of the aid to impart system understanding is reflected by the gain of 56 percentage points on the posttest for the EHJPA group. The OP group gained only 27 percentage points.

Functional Comparison

Subject matter experts were interviewed to compare the steps that inexperienced and experienced technicians might take troubleshooting the MIC using either OPs or DT/FFLD EHJPAs for technical documentation. Table 3 summarizes the protocols inexperienced and experienced technicians might follow when using OPs or DT/FFLDs to troubleshoot. The complete protocols are given in Appendix A.

. Table 1

OP and DT/FFLD EHJPA Groups: Mean Solution Rates and Fault-Isolation Times

Group	Task 1	2	3	4	5	Grand Mean
	Mean Solution Rates (%)					
OP	63	88	88	75	63	75
DT/FFLD EHJPA	100	100	100	100	100	100
	Mean Fault-Isolation Times (minutes)					
OP	27.1	15.6	21.4	25.4	30.5	24.0
DT/FFLD EHJPA	9.0	11.4	12.4	18.8	11.2	12.6

Table 2

OP and DT/FFLD EHJPA Groups: Mean Results of System Understanding Test

Group	Mean Percent Correct		
	Pretest	Posttest	Gain
OP	10	37	27
EHJPA	3	59	56

Table 3

OP-DT/FFLD Troubleshooting Protocols

OP (Inexperienced)	DT/FFLD (Inexperienced)	OP (Experienced)	DT/FFLD (Experienced)
1. System placed in operation.	1. System placed in operation.	1. System placed in operation.	1. System placed in operation.
2. Observe fault symptoms.	2. Observe fault symptoms.	2. Observe fault symptoms.	2. Observe fault symptoms.
3. Use FOIDs to aid troubleshooting, which requires: a. Tracing signal through 6 sheets. b. Making tests at 5 test points. c. Knowledge of timing patterns to know when to switch between modes to test for signals.	3. Use the single sheet DT of EHJPA to aid troubleshooting. a. Match up observed symptoms with listed symptoms. b. Folow DT procedure to isolate failed component.	3. Use FOIDs to aid troubleshooting, which requires: a. Tracing signal through 2 sheets. b. Making tests at 5 test points. c. Knowledge of timing patterns to know when to switch between modes to test for signals.	3. Use single sheet FFLD of EHJPA to aid troubleshooting: a. Identify components related to affected function. b. Requires making tests at from 1 to 5 test points.
4. Identify suspected failed component.	4. Remove and replace suspected component.	4. Identify suspected failed component.	4. Identify suspected failed component.
5. Remove and replace suspected component.	5. Verify correct operation of system.	5. Remove and replace suspected component.	5. Remove and replace suspected component.
6. Verify correct operation of system.		6. Verify correct operation of system.	6. Verify correct operation of system.
(Because inexperienced technician is unlikely to be able to integrate timing information, the suspected component is likely to be wrong.)			

Page Count

To develop the DT/FFLDs, it was necessary to identify the appropriate functional components of each particular circuit. To do this, the circuit had to be traced to determine what other components were or were not influencing the circuit of interest. In addition, outputs had to be followed to determine if they were part of a feedback loop that influenced the circuit under study. The theory of operation was studied and understood to ensure the correct redrawing of the OP circuit. Table 4 lists various inputs and outputs (identified from the OP FOIDs) of the circuit, the theory of operation references, and the number of pages those data require in the OPs. The 6 two-page DT/FFLD EHJPAs referenced 197 pages or an average of 32.8 pages per aid.

ST/ES EHJPAs

Demonstration Results

Smillie and Porta (1981) reported that eight participants using the troubleshooting guide and STs solved 32 problems in 25 hours and that participants using OPs solved 9 problems in 33.8 hours. Thus, the focus of this demonstration was to assess the effectiveness of the ES.

After the 11 ST/ESs were developed, each of the six subjects were given the OP, ST alone, or ST/ES and instructed to use the materials to isolate a hypothetical failure based on the symptoms provided. For each type of technical documentation, both an instructor and a student attempted to find the fault. Using the OPs as the source for troubleshooting information, the failure was not found. Using STs, the failure was partially isolated. Only with ST/ESs were the failures identified correctly.

Functional Comparison

Subject matter experts were interviewed to compare the steps technicians might take troubleshooting the MCU using OPs, STs, or ST/ES EHJPAs for the technical documentation. Table 5 summarizes the protocols technicians might follow when using OPs, STs, or ST/ESs to troubleshoot. The complete protocols are given in Appendix B.

Page Count

Table 6 shows the number of pages from OP 4006, Vol. 2, Part 3 that correspond to the 11 ESs. The mean was 6.7 OP pages per aid.

Table 4

OP Paragraphs, OP Figures, and Number of OP Pages
Referenced in Developing the DT/FFLD EHJPAs

DT/FFLD EHJPA	Operation Theory		OP Figure		Total Number of Pages
	Paragraph Number	Number of Pages	Figure Number	Number of Pages	
Servo system power (elevation)	1-27	1	5-90	1	
	2-38	1	5-103	1	
	2-119	4	5-106	1	
	2-132	1	5-107	9	
	2-201	1	5-109	1	
			5-123	5	
			5-136	2	
			5-139	1	
			5-140	2	
			5-141	1	
			5-143	1	
			5-145	2	
		8		27	35
Servo system power (train)					35
Stock lock operation (elevation)	2-116	1	5-106	5	
	2-117	1	5-107	3	
	2-118	1	5-123	1	
	2-119	4	5-136	2	
			5-140	2	
			5-141	4	
			5-145	4	
		7		21	28
Stow lock operation (train)					28
DCU	1-17	1	5-95	1	
	2-44	1	5-107	4	
	2-132	2	5-109	5	
			5-123	13	
			5-132	2	
			5-145	3	
		4		28	32
Firing save/MIM and EHIM operation	2-120	2	5-99	4	
			5-119	15	
			5-91	1	
			5-93	1	
				1	
			5-104	2	
			5-107	1	
			5-118	1	
			5-123	1	
			5-128	1	
			5-131	1	
			5-133	1	
			5-135	1	
			5-141	2	
			5-145	3	
			5-146	1	
		2		37	39
					197

Table 5

OP-ST-ST/ES Troubleshooting Protocols

OP	ST	ST/ES
1. System placed in operation.	1. System placed in operation.	1. System placed in operation.
2. Run BITE test.	2. Run BITE test.	2. Run BITE test.
3. Observe fault lights.	3. Observe fault lights.	3. Observe fault lights.
4. Follow troubleshooting procedures in OP (1 sheet).	4. Follow troubleshooting procedure in ST (3 sheets).	4. Follow troubleshooting procedure in ST (3 sheets).
5. Set up test equipment. (No information is available to technician.)	5. Conduct test.	5. Conduct test.
6. Conduct test (1 sheet).	6. Follow troubleshooting procedure in ST (4 sheets).	6. Follow troubleshooting procedure in ST (4 sheets).
7. Refer to fault locator in OP (1 sheet).	7. Conduct two tests.	7. Conduct two tests.
8. Use timing diagram (1 sheet) to conduct from 1 to 8 tests and use schematic diagrams to aid troubleshooting. This requires: a. Tracing signals through 3 sheets. b. Conducting tests at 17 test points.	8. Use ST (1 sheet) to conduct 10 checks to identify location of suspected fault.	8. Use ST (1 sheet) to conduct 10 checks to identify location of suspected fault.
9. Remove and replace suspected failed component.	9. Use schematic diagrams (2 sheets) and conduct tests at from 1 to 8 test points.	9. Use ES (1 sheet) to conduct test at 1 test point.
10. Verify correct operation of system.	10. Remove and replace suspected failed component.	10. Remove and replace suspected failed component.
	11. Verify correct operation of system.	11. Verify correct operation of system.

Table 6

Number of OP Pages Referenced in Developing Each ST/ES EHJPA

Instruction	Number of OP Pages
JBT	3
JMP	3
LDAB	8
LDOB	11
JBNZ	7
JPB	6
LDOA	10
CLR 1	7
SUB	5
LDAA	8
SRB	6
Total	74
Mean	6.7 pages/EHJPA

DISCUSSION

DT/FFLD EHJPAs

The evaluation supported the premise that the DT/FFLD EHJPA was an effective aid in troubleshooting. Technicians using DT/FFLD solved all the problems in one half the time (12.6 vs. 24.0 minutes) that the OP group took to solve only 75 percent of the problems. In an evaluation of the enrichment concept, technicians who had used DT/FFLD aids achieved a 56 percent gain on a posttest on system understanding, while technicians who had used OPs achieved 27 percent gain.

In comparing the two troubleshooting protocols, inexperienced technicians would have to use at least six FOIDs (in the OPs) to trace the signal. At the same time, at least five test readings might be required to determine the proper signal path to follow. In addition, the inexperienced technicians would find matching equipment mode to signal path difficult because the equipment mode is not explicit in the FOIDs as it is in the DT/FFLD.

Inexperienced technicians, who used the DT/FFLD aid, however, might isolate the fault with the single page of technical data and take only four test readings. Since the

equipment mode dependency was identified on the DT/FFLD, the inexperienced technicians should be able to determine the correct signal path easily.

On the other hand, experienced technicians using OPs would probably recognize the mode dependency from past experience and isolate the fault using only two FOIDs. While experienced technicians would probably take the same number of test readings regardless of technical data used, tracing the signal would be simpler with the FFLD because a single page provides the complete functional description related to a given set of symptoms and all relevant components related to a particular function are identified.

The ratio of the number of OP pages to the number of DT/FFLD pages exemplifies the economy of presenting relay circuitry in a DT/FFLD EHJPA. A total of 197 pages of technical data were used to develop the 6 two-page DT/FFLDs, an average of 32.8 pages per DT/FFLD.

ST/ES EHJPAs

Fault isolation was easier and more successful when technicians used the ST/ES for troubleshooting. The ST was sufficient for partially isolating the fault; the ES, however, contained the information necessary to determine if the failure was between test points identified on the ST. The troubleshooting protocol comparison provided the information necessary to examine the differences among the three fault isolation procedures that might be employed using OPs, STs, or ST/ES aids for technical information.

CONCLUSIONS

Both types of the EHJPAs are effective troubleshooting aids. They demonstrate that it is possible to develop JPAs, based upon the enriched hybrid methodology, for different types of circuitries. DT/FFLD aids are compatible for circuits whose component states remain constant in a given mode and ST/ES aids are compatible with solid state circuitry having BITE. Inexperienced technicians can be expected to follow the directive portion of an EHJPA to perform limited troubleshooting. Over time, inexperienced technicians will gain experience and develop the necessary system understanding to use the deductive element of the EHJPA, eventually transitioning to the OPs.

The EHJPA can also be used in training to provide students with a succinct functional description that is related to both theory of operation and more detailed functional flows or schematics. Thus, students would be provided an opportunity to develop a more thorough understanding of the system and how the technical data are organized.

RECOMMENDATIONS

It is recommended that (1) DD/FFLD EHJPAs be developed for relay circuitry and (2) ST/ES EHJPAs be developed for digital solid state circuitry. These EHJPAs can be used to allow technical training students to develop an understanding of the functional relationships within electronic systems and understand and become familiar with the organization of the technical data. More importantly, in a work environment, these aids can replace difficult sections of technical manuals to facilitate troubleshooting for both inexperienced and experienced technicians. As part of Enlisted Personnel Individualized Career System (EPICS), technicians can use these aids earlier in their technical career to troubleshoot on a limited basis.

REFERENCES

Blanchard, R. E., & Laabs, G. J. (February 1978). A personnel system concept with job performance aiding as a principal component: Preliminary model (NPRDC Tech. Note 78-6). San Diego: Navy Personnel Research and Development Center.

Booher, H. R. (Ed.). (June 1977). Symposium proceedings: Invitational conference on status of job performance aids technology (NPRDC Tech. Rep. 77-33). San Diego: Navy Personnel Research and Development Center. (AD-A040 540)

Booher, H. R. (July 1978). Job performance aids: Research and technology state-of-the-art (NPRDC Tech. Rep. 78-26). San Diego: Navy Personnel Research and Development Center. (AD-A057 562)

Booher, H. R. (October 1978). Job performance aid selection algorithm: Development and application (NPRDC Tech. Note 79-1). San Diego: Navy Personnel Research and Development Center.

Gebhard, R. M. (1970). Development of a training program and job aids for maintenance of electronic communication equipment (HumRRO-TR-70-19). Alexandria: George Washington University. (AD-718 025)

Naval Sea Systems Command. (1 July 1976). Guided missile launching system MK 29 MOD 0 (NAVSEA OP 4006 (PMS/SMS), Vol. 1, Parts 1 & 2). Washington, DC: Author.

Naval Sea Systems Command. (1 July 1976). Guided missile launching system MK 29 MOD O (NAVSEA OP 4006 (PMS/SMS), Vol. 2, Parts 1-3). Washington, DC: Author.

Osga, G. A., & Smillie, R. J. (June 1983). Proceedings of an invitational conference on job performance aid cost factors (NPRDC Spec. Rep. 83-39). San Diego: Navy Personnel Research and Development Center.

Post, T. J., & Price, H. E. (May 1972). Development of innovative job aid concepts: Vol. I. Description of contents. Falls Church, VA: BioTechnology, Inc. (AD-751 044)

Post, T. J., & Price, H. E. (April 1973). Development of optimum performance aids for troubleshooting. Falls Church, VA: BioTechnology, Inc.

Post, T. J., & Smith, M. G. (July 1979). Hybrid job performance aid technology definition (NPRDC Tech. Rep. 79-25). San Diego: Navy Personnel Research and Development Center. (AD-A072 445)

Potter, N. R., & Thomas, D. L. (September 1976). Evaluation of three types of technical data for troubleshooting: Results and project summary (AFHRL-TR-76-74(I). Wright-Patterson Air Force Base: Air Force Human Resources Laboratory.

Rogers, J. P., & Thorne, H. W. (March 1965). The development and evaluation of an improved electronics troubleshooting manual (Tech. Rep. 65-1). Arlington, VA: George Washington University. (AD-614 606)

Serendipity, Inc. (May 1969). Project PIMO final report. Vol. I. Summary (SAMSO TR-69-155(I)). Chatsworth, CA: Author. (AD-852 101)

Shriver, E. L. (June 1960). Determining training requirements for electronic system maintenance: Development and test of a new method of skill and knowledge analysis. Alexandria: George Washington University. (PB-149 202)

Shriver, E. L., Fink, C. C., & Trexler, R. C. (May 1964). FORCAST systems and training methods for electronics maintenance training (Res. Rep. 13). Alexandria, VA: George Washington University, Human Resources Research Office. (AD-441 248)

Smillie, R. J., & Porta, M. M. (October 1981). Comparison of state tables and ordnance publications for troubleshooting digital equipment (NPRDC Tech. Rep. 82-7). San Diego: Navy Personnel Research and Development Center. (AD-A107 945)

Smith, M. G., Post, T. J., & Smillie, R. J. (May 1983). Field evaluation of enriched hybrid job performance aids (NPRDC Spec. Rep. 83-32). San Diego: Navy Personnel Research and Development Center.

U.S. Army. (October 1966). Military potential test of symbolic integrated maintenance manuals for the Hawk missile and its organization maintenance test equipment. White Sands, NM: U.S. Navy Air Defense Board.

U.S. Coast Guard. (July 1964). A report on the evaluation of SIMS maintenance charts as an aid in performing corrective maintenance on the AN/SPS-29 air search radar systems. Washington, DC: Author.

APPENDIX A

PROTOCOLS FOR TROUBLESHOOTING THE MIC USING OPs AND DT/FFLD EHJPAs

PROTOCOLS FOR TROUBLESHOOTING THE MIC USING OPs AND DT/FFLD EHJPAs

OP Troubleshooting Protocol

The following steps represent the protocol to isolate the 22A5A2A1K239 relay fault causing the casualty using OPs:

1. Put system into REMOTE mode.

2. Observe symptoms--Launcher does not train or elevate in REMOTE but moves normally in LOCAL/DCU. Evaluation-servo power-on-switch indicator does not illuminate.

(Inexperienced technicians probably would not know which portion of the involved circuit is dedicated to the REMOTE mode. One strategy would be to start where the indicators do not illuminate and work upstream.)

3. Locate the indicators in the FOIDs, in zones A-28 and A-26 of OP 4006, Vol. 2, Part 2, Figure 5-107, shown in Figure A-1a. Trace the circuit upstream. The voltage reading at 22A5A2ATB56-7 (zone B-23, Figure A-1b) is zero volt. (Before taking any readings, the technician must take the system out and then back into the REMOTE mode to restart the timing sequences upstream to these components, which none of the inexperienced technicians in this test knew.) The next voltage reading at 22A5A2TB56-9 (zone B-21, Figure A-1b) is also bad--zero volt. Moving further upstream through Figures A-1c and A-1d, the technician encounters 22A5A2A1K239 relay (zone A-11, Figure A-1d). Input to K239 relay contacts comes from Figure 5-145, B-6. Technician goes to Figure 5-145 (B-6) and checks A5A2TB68-4, which is approximately 26 volts. Back at Figure A-1d, the technician tries to determine if 26 volts are going to K239 coil, the voltage is read at 22A5A2TB57-8, zone A-10, Figure A-1d (again, the timing pattern must be known). This reading would also be bad--zero volts. The reading would be zero because the technician did not take system out of and back into REMOTE or because too much time was taken to monitor the changing readings. Moving further upstream on Figure A-1e, a good reading at 22A5A12TB406-22 (zone A-6) would conclude that K174 (Figure A-1d) would have to be the casualty.

4. Remove and replace K174.

5. Determine whether the MIC is now operating properly, which it would not be. It would show the same symptoms as before.

An alternate strategy that an experienced technician might take would be to start at the REMOTE relay K108 and test 22A5A10TB504-24, zone A-6, Figure A-1e (good); take the system out of and back into the REMOTE mode and monitoring 22A5A12TB406-22 (zone A-6, Figure A-1e) to see if there are 26 volts after 10 seconds (good); take the system out of and back into REMOTE mode and monitor 22A5A2TB57-8 (zone A-10, Figure A-1d) to see if, after 10 seconds, 26 volts are available for only the next 6 seconds and there are zero volt thereafter (good); take system out of and back into REMOTE mode and monitor relay output at 22A5A2TB57-10 (zone A-11, Figure A-1d) to see if, after 10 seconds, 26 volts are available for only the next 6 seconds and there are zero volt thereafter (bad). Check relay input by taking reading at A5A2TB68-4, zone B-6, Figure 5-145; reading is good. Using this approach, the technician has isolated the casualty to K239.

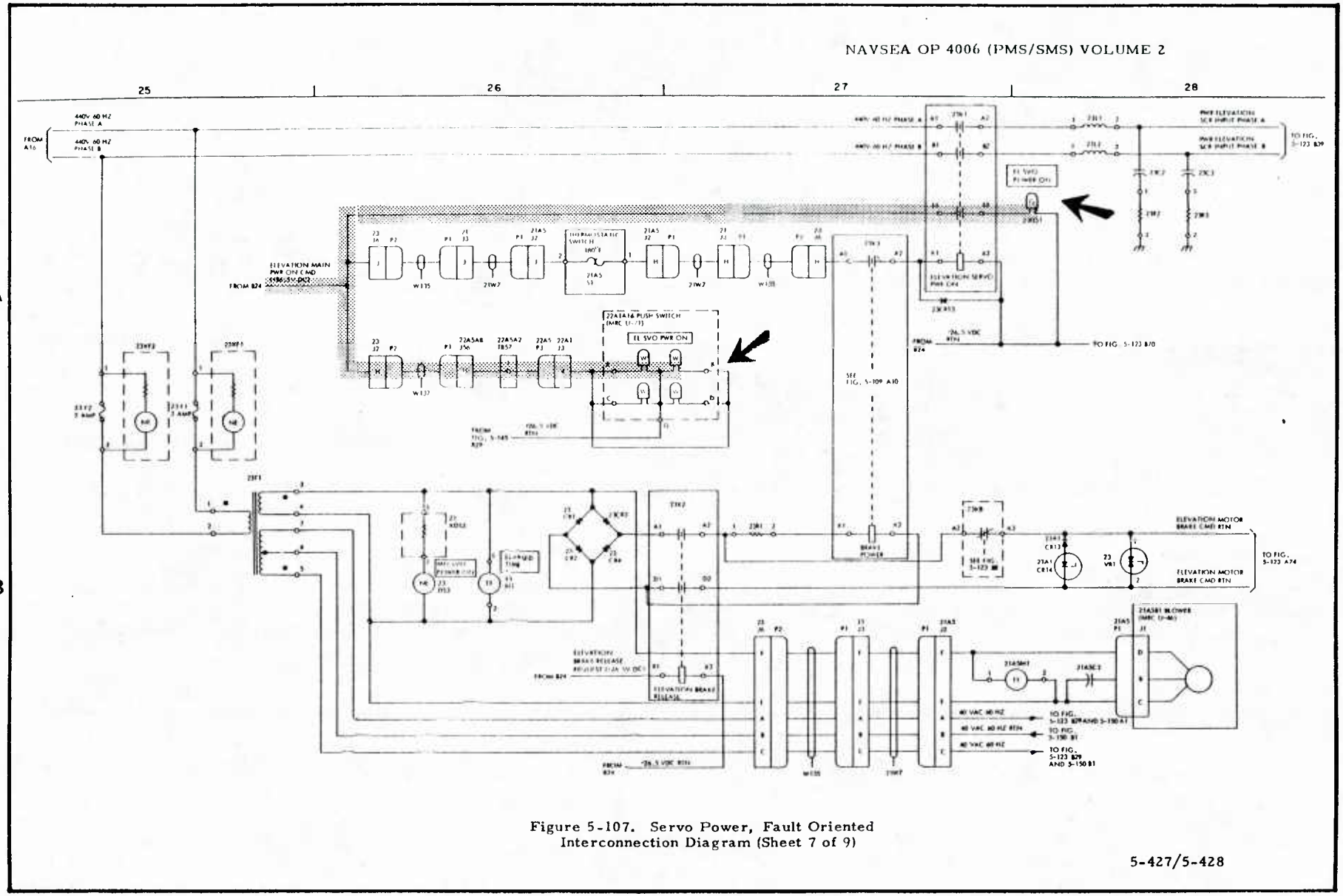


Figure 5-107. Servo Power, Fault Oriented Interconnection Diagram (Sheet 7 of 9)

5-427/5-428

Figure A-1a. Figure 5-107, sheet 7 of 9 (OP 4006).

Figure A-1. Troubleshooting MIC using FOID.

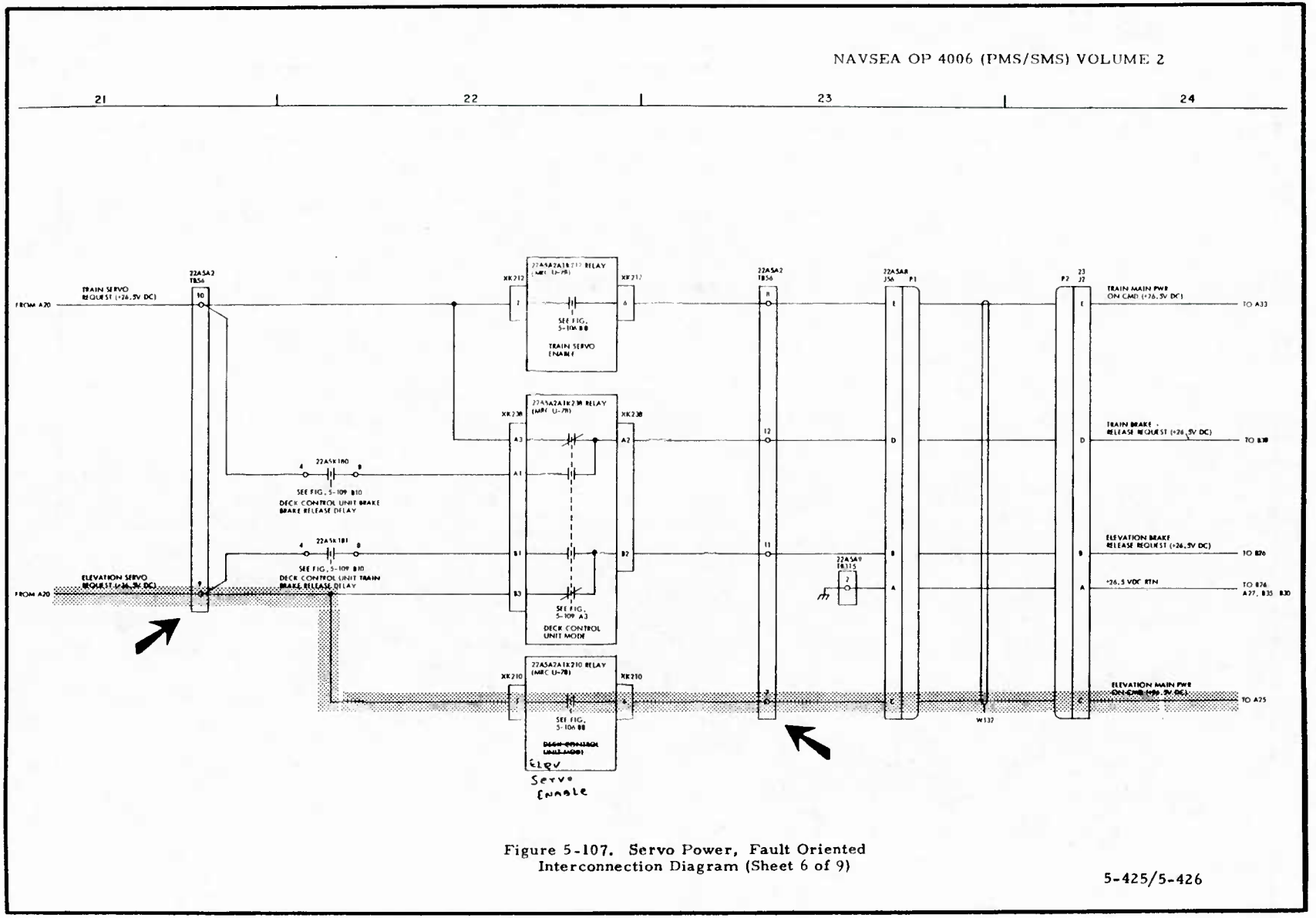


Figure 5-107. Servo Power, Fault Oriented Interconnection Diagram (Sheet 6 of 9)

5-425/5-426

Figure A-1b. Figure 5-107, sheet 6 of 9 (OP 4006).

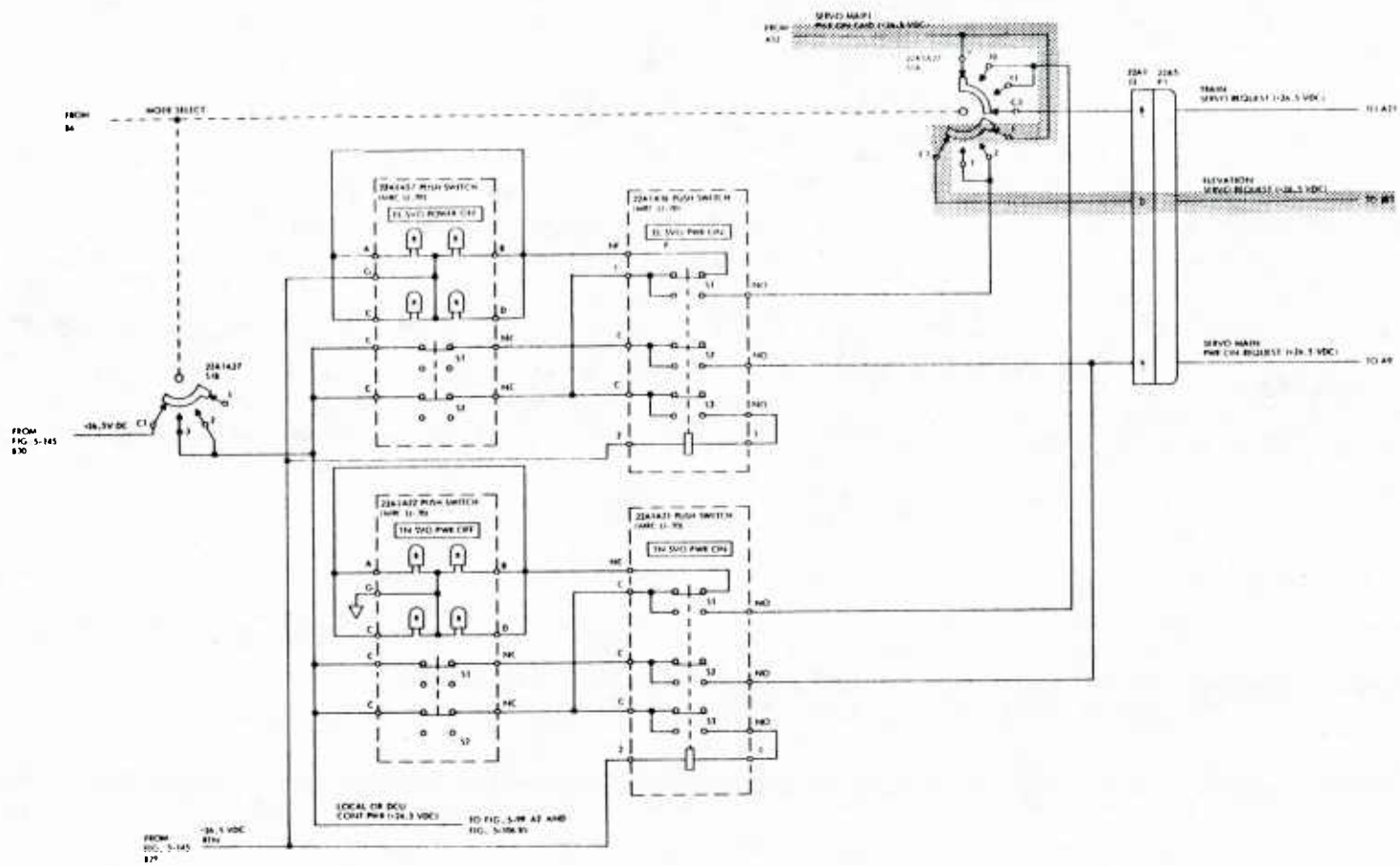


Figure 5-107. Servo Power, Fault Oriented Interconnection Diagram (Sheet 5 of 9)

5-423/5-424

Figure A-1c. Figure 5-107, sheet 5 of 9 (OP 4006).

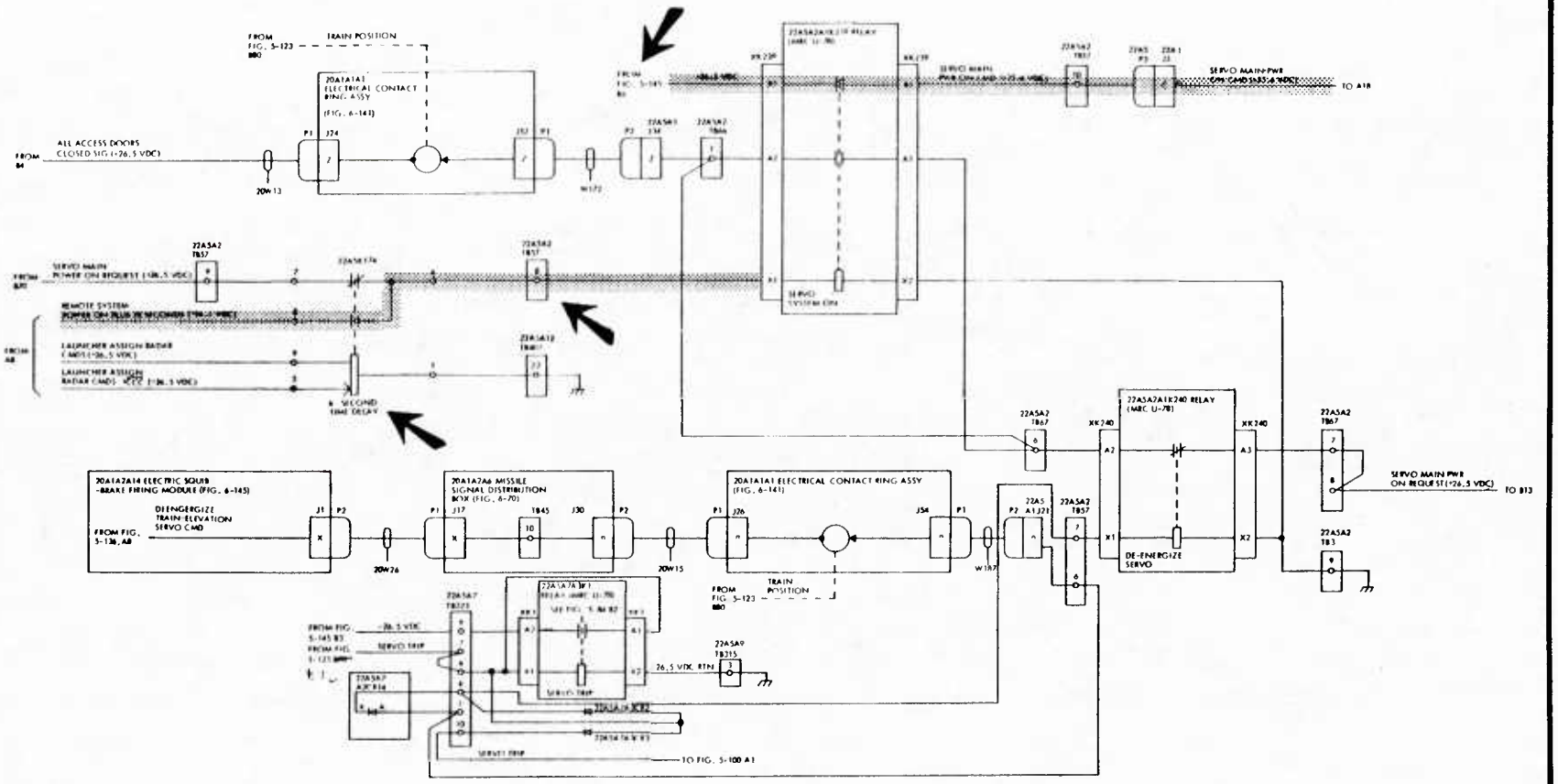


Figure 5-107. Servo Power, Fault Oriented Interconnection Diagram (Sheet 3 of 9)

5-419/5-420

Figure A-1d. Figure 5-107, sheet 3 of 9 (OP 4006).

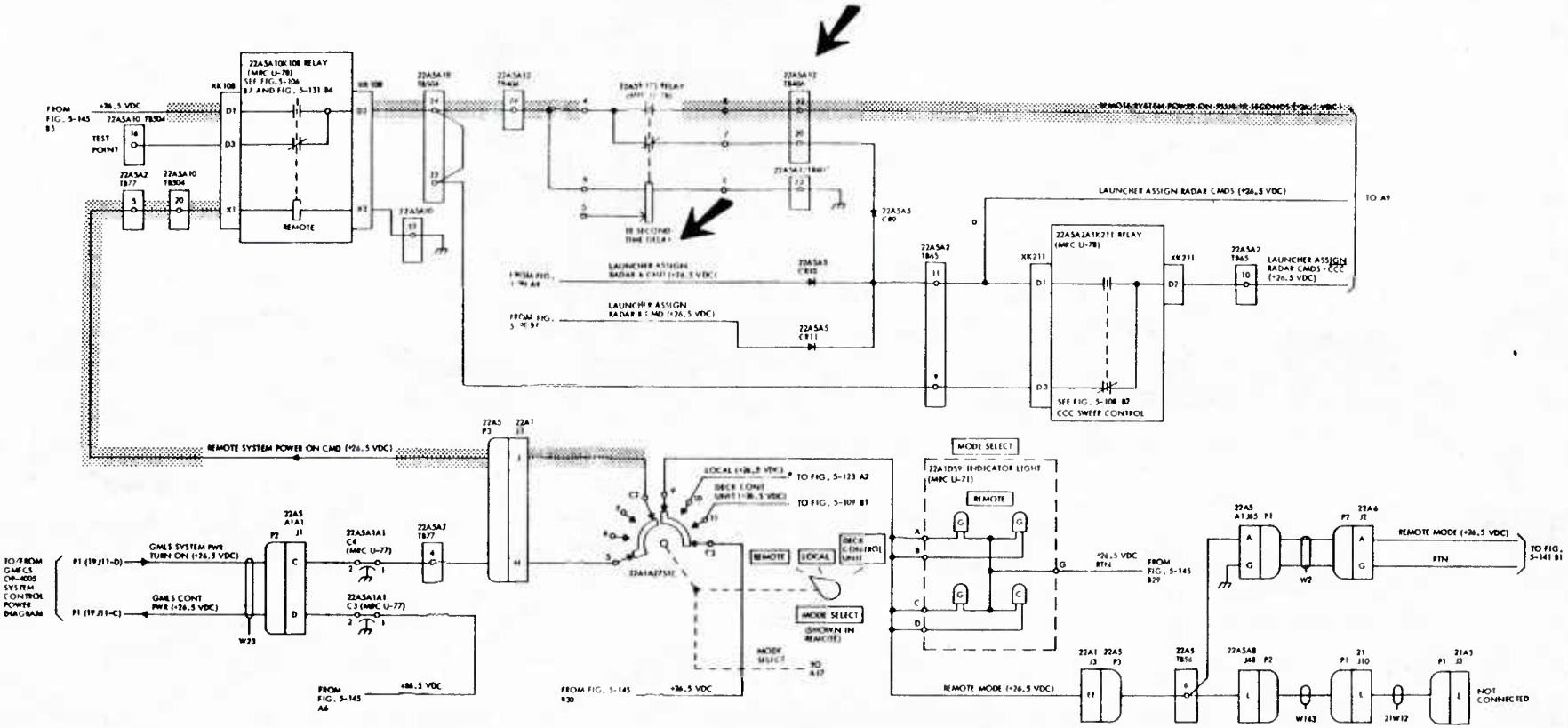


Figure 5-107. Servo Power, Fault Oriented Interconnection Diagram (Sheet 2 of 9)

5-417/5-418

Figure A-1e. Figure 5-107, sheet 2 of 9 (OP 4006).

DT/FFLD Troubleshooting Protocol

The following steps represent the protocol to isolate the same (22A5A2A1K239 relay) casualty using DT/FFLDs:

1. Observe symptoms; launcher does not train or elevate in REMOTE, but moves normally in LOCAL/DCU.

2. Use directive element to servo system power (elevation) (OP 4006, Vol. 2, Part 2, Figure 5-107), which is shown in Figure A-2. Find symptom in symptom column that says to use DT in the fourth row of the procedures column.

3. Perform troubleshooting as directed by DT.

4. Isolate the fault to K239 relay.

5. Remove and replace K239 relay.

6. Determine whether MIC is now operating properly.

A more experienced technician would go directly to the FFLD, shown in Figure A-3. The technician can readily see that the K108, K173, K174, and K239 relays are used only when the switch is in REMOTE and never in LOCAL/DCU and that two indicator lights would not be illuminated if the casualty were in the REMOTE portion of the circuit.

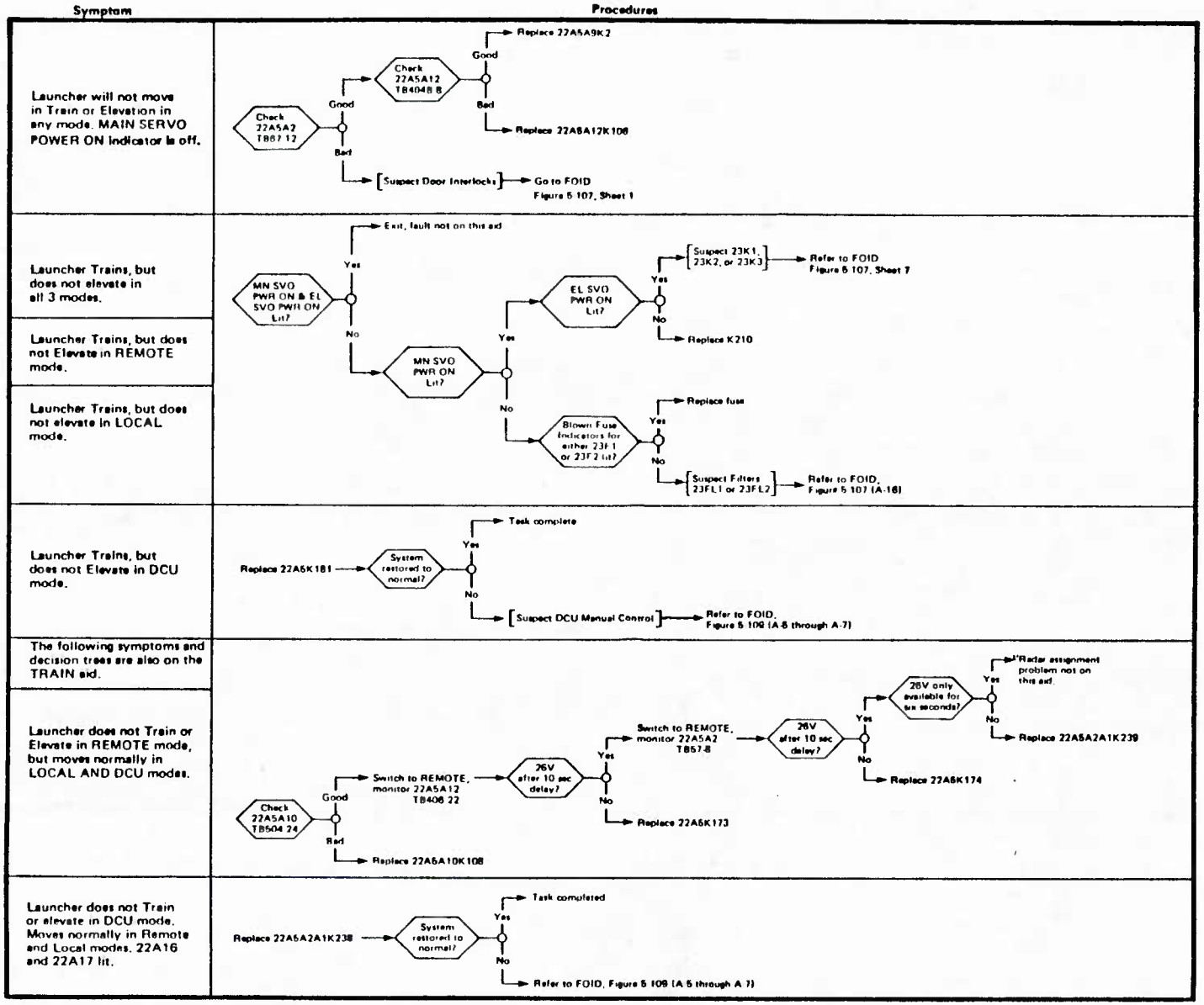


Figure A-2. Servo system power (elevation) directive element (DT).

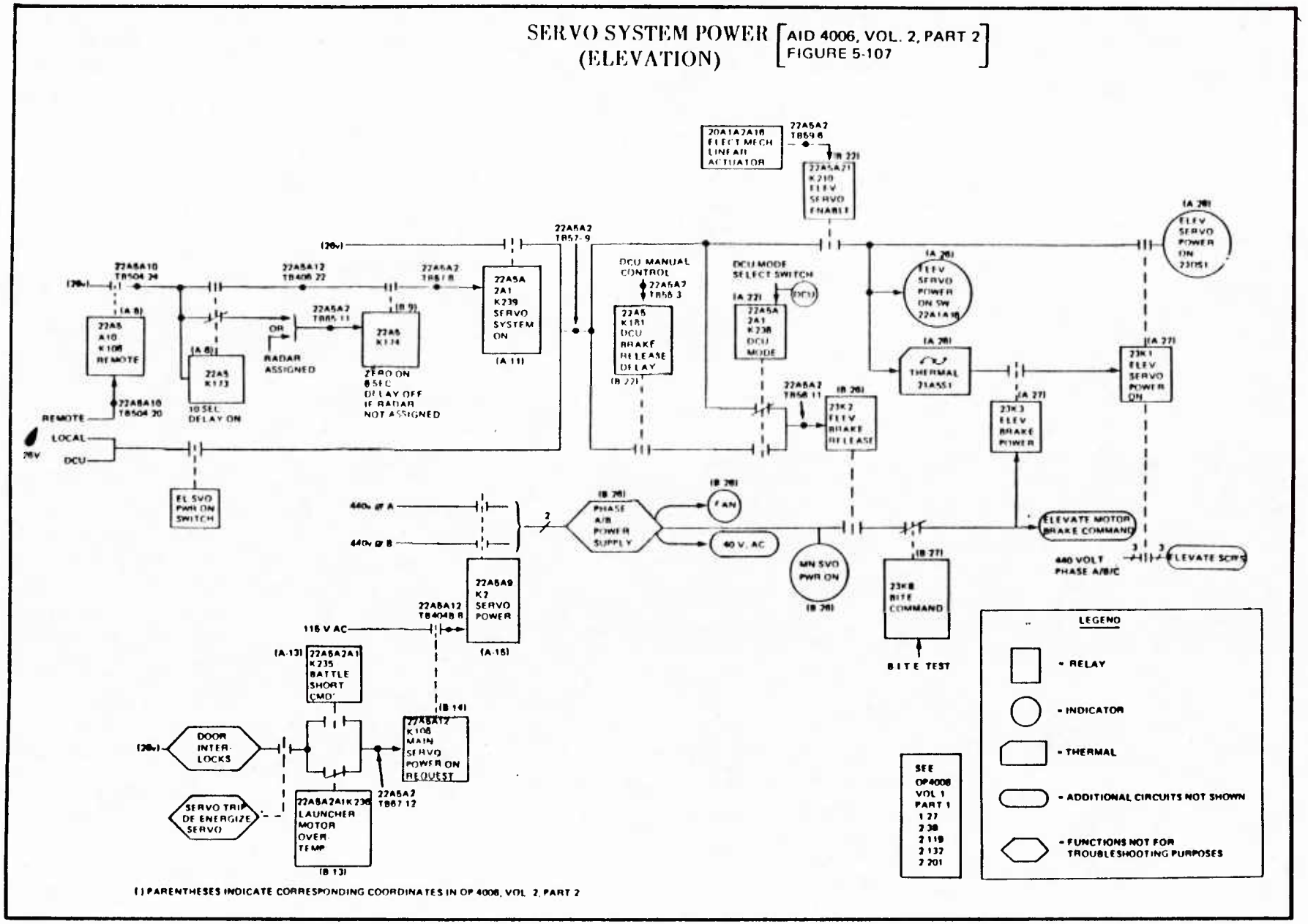


Figure A-3. Servo system power (elevation) deductive element (FFLD).

APPENDIX B

PROTOCOLS FOR TROUBLESHOOTING THE MCU USING OPs, STs, AND ST/ES EHJPAs

PROTOCOLS FOR TROUBLESHOOTING THE MCU USING OPs, STs, AND ST/ES EHJPAs

OP Troubleshooting Protocol

The following steps represent the protocol to isolate the A18 pin 4 casualty using OPs:

1. Turn power on.

2. Turn BITE test switch to the BITE Test A position and run test. Fault light 1 illuminates.

3. Turn BITE test switch to the OFF position.

4. Turn power off.

5. Open MCU and pull out drawer.

6. Refer to OP 4006, Vol. 2, Part 1, Table 5-9 (page 5-44) (shown in Figure B-1).[1] Read procedures associated with Fault Indicators Lit No. 1 on Table 5-9.

   a. Install JUMP card.

   b. Set up oscilloscope.

   c. Compare JUMP waveform on oscilloscope with that on Figure 5-18 (shown in Figure B-2). Assume that waveform differs at Checkpoint 27.

7. Go to Table 5-10 of OP 4006, Vol. 2, Part 1 (shown in Figure B-3). The probable fault for the waveform differing at Checkpoint 27 is the SRB1 instruction.

8. Table 5-10 (Figure B-3) also refers to Figure 5-45 of OP 4006, Vol. 2, Part 2 (Figure B-4), which shows the JUMP waveform in the failed mode at the top. The waveform at Checkpoint 27 should be low, but is high in the failed mode (see Figure B-4). The three instructions (3 cells) shown prior to Checkpoint 27 in Figure B-4 are the LDOB, SRB, and LDOA/SUB instructions. The output of these three instructions influences the output of the SRB instruction.

Figure B-4 consists of rows of waveforms each showing the normal operating waveform for the card and pin number listed to the left of the waveform. For example, below the JUMP waveform is the normal waveform from the output lines of the B Register (labeled BREG00, BREG01, BREG02, BREG03, BREG04, and BREG05) located on card A56, pins 32, 31, 34, 33, 10, and 9 respectively.

If the output of the SRB instruction is faulty, Figure B-4 gives all the information needed to begin troubleshooting. This includes card and pin number, shape of the waveforms, the timing of the waveform (the 11 cells for each instruction are the 11 clock pulses from the 4 MHz clock), and the OP figure and sheet number reference.

---

[1]Because of the large number of figures included in this section relative to the amount of text, the figures are provided at the end of this section, starting on p. B-4.

The technician can begin troubleshooting by testing the card and pin on the first row and working down. Once a failed waveform is located, the technician can refer to OP 4006, Vol. 2, Part 3 for the schematic and check components upstream to the pin that produced the faulty waveform.

If the casualty is pin BREG04 of card A18, then the waveform on row one of Figure B-4 coming from A56-32 will be "bad" (high). The technician is referred to sheet 16 of Figure 6-172, shown in Figure B-5a. There the technician locates A56-32 and begins to test components upstream to it. The inputs for A56-32 are A56-36, -35, -37, and -42. A56-42 will test bad. The technician would then move upstream along the B input (Serial) (shown in Figure B-5b) and check A21-9 and its inputs, A21-19, -18, -17, -14, -13, -12, -10, and -7. A21-14 is bad. Moving to A18-6 (shown in Figure B-5b), inputs A18-3 and -4 are tested. A18-4 is bad. Troubleshooting upstream to A18-7 (shown in Figure B-5c), the output of A18-7 is good and the input at A18 pin 4 is bad. A18-4 is the casualty.

ST Troubleshooting Protocol

Figure B-6 shows the relationship of the parts of the troubleshooting guide, the STs, and the OPs. In the troubleshooting guide, Part 1 deals with the procedures for running BITE Test A; Part 2 with the procedures for setting up the MCU and oscilloscope for fault lights 1 and 2.

Parts 3 and 4 have the most straightforward relationship to the STs and use them the most. Part 3 deals with casualties of the first 11 jumps in the JUMP waveform of BITE Test A and Part 4 addresses the casualties in Checkpoints 1 through 64 in the JUMP waveform of BITE Test A.

Part 5 of the troubleshooting guide deals with multiple fault light problems; Part 6, with no fault lights when BITE Test A is run; and Part 7, with troubleshooting the MCU when BITE Test A is all right.

The following steps represent the troubleshooting protocol to isolate the casualty, using the STs.

1. Turn power on.
2. Turn BITE test switch to the BITE Test A position and run BITE test.
3. Fault light 1 illuminates.
4. Turn BITE test switch to the OFF position.
5. Turn power off.
6. Open MCU and pull out drawer.
7. Refer to Part 1 of the troubleshooting guide (shown in Figure B-7).
8. Part 1 refers the technician to Part 2 when Fault Light 1 is illuminated.
9. Set up oscilloscope as shown in Figure B-8.
10. Perform setup procedures for the MCU as shown in Figure B-9.

11. Run BITE Test A again.

12. Compare JUMP waveform on oscilloscope with that on OP Figure 5-18 (shown in Figure B-2) to determine that failure occurs at Check point 27.

13. Troubleshooting guide refers the technician to Part 4 (arrow in Figure B-9).

14. Table of contents of Part 4 (in Figure B-10) refers the technician to page 4-41 for a Checkpoint 27 failure.

15. Read page 4-41 (Figure B-11).

16. Read page 4-42 (Figure B-12).

17. Begin troubleshooting procedures on troubleshooting guide page 4-43 (Figure B-13).

18. The answer to the Step 1 question on page 4-43 (Figure B-13) is Yes. Go to Step 2.

19. The answer to the Step 2 question is No. The troubleshooting guide directs the technician to troubleshoot the SRB state table (Figure B-14).

20. The technician begins at the column on the far left of the SRB state table and moves across the columns to test the test points listed at the top of the column. After getting an incorrect reading, the technician would need to look at the OPs to be sure that the actual failed component is not upstream to the tested component. For example, without referring to OP page 6-557, the technician might replace card 21 according to the STs. Component A21-9 of the 11th column is the first component to have a bad reading if A18-4 is the casualty.

21. The technician must determine which of the multiple inputs at NOR gate A21U6 (shown in OP) are relevant for the SRB instruction and must determine if the STs lists any components between this one and others. The single component between A21-9 (column 11) and A18-7 (column 5) is A18U2D, which is the casualty.

22. Technician replaces card 18 and runs the BITE test again to confirm that the casualty has been repaired.

ST/ES Troubleshooting Protocol

The troubleshooting protocol for the ST/ES is basically the same as that for the ST protocol with only one difference. Once the technician begins troubleshooting using the SRB ST, there would be no need to refer to the OPs to determine if other components upstream to the one listed on the ST could give a faulty reading because the ES element of the EHJPA furnishes that information. The ES saves troubleshooting time and allows the technician to identify more readily the card housing the failed component. Using the same example as in the ST protocol, the technician can readily identify the one component between A21-9 (test point 11) and A18-7 (test point 5) while looking at the SRB ES shown in Figure 15.

TABLE 5-9. TEST A FAILURE MCU TROUBLESHOOTING PROCEDURE

Fault Indicators Lit	Procedure
	NOTE After jumper installed, initiate cycle testing by switching out of Test A at the Maintenance Interconnection Cabinet, then switch back to Test A and depress BITE INITIATE switch.
None	Signal trace circuit shown on figure 5-83.
1	Install a jumper between A62-67 and A62-71 (ground). Synchronize a dual trace scope with the signal at A62-63. Connect one oscilloscope input to A62-60 (JUMP) and connect the other input to A62-59 ($\overline{\text{CLOCK 3}}$). Compare the JUMP waveform with that of figure 5-18 and determine the BITE checkpoint at which the waveform differs. Refer to the waveforms appropriate to the BITE checkpoint as listed in table 5-10. The $\overline{\text{CLOCK 3}}$ waveform is useful as a counter when comparing the JUMP waveform to figure 5-18.
1-2	The JUMP instruction or the CROM is faulty. Install a jumper between A62-67 and A62-71 (ground). Synchronize oscilloscope with signal at A62-63. See figure 5-4A for waveforms and timing diagram of possible faulty signals.
1-4-5-7-10	MCU Bite Result 1 always high at A99-5. See fig. 6-172 , sh 44.
2-4-5-7	MCU Bite Result 2 always high at A100-5. See fig. 6-172 ., sh 44.
3	Install jumper (See Note) between A62-72 and A62-68. Check for +26.5V MISSILE 8 UNLOCK HOLDBACK CMD at A123-11, figure 6-172 , sheet 45.
3-4	Install jumper (See Note) between A62-72 and A62-68. Check for +26.5V MISSILE 8 EHIM IGNITE CMD MCU at A122-69, figure 6-172 , sheet 44.
3-4-5-6-7	Install jumper (See Note) between A62-72 and A62-68. Synchronize oscilloscope with signal from A62-64 ($\overline{\text{C SYNC}}$). The jump waveform will repeat either every 33 µs or 55 µs. The shorter waveform implies that the INTERROGATE FF is not being set when commanded and the long waveform implies that it is not resetting when commanded. See figure 5-5 for appropriate waveform.
3-4-5-6-7-8	Install jumper (See Note) between A62-72 and A62-68. Synchronize oscilloscope with signal for A62-64 ($\overline{\text{C SYNC}}$). See figure 5-6 for waveforms of possible faulty signals.
3-4-5-6-7-8-9	Same as above, except waveforms on figure 5-7.
3-4-5-6-7-8-10	Same as above, except waveforms on figure 5-8.

Figure B-1. Troubleshooting MCU using OP--troubleshooting index.

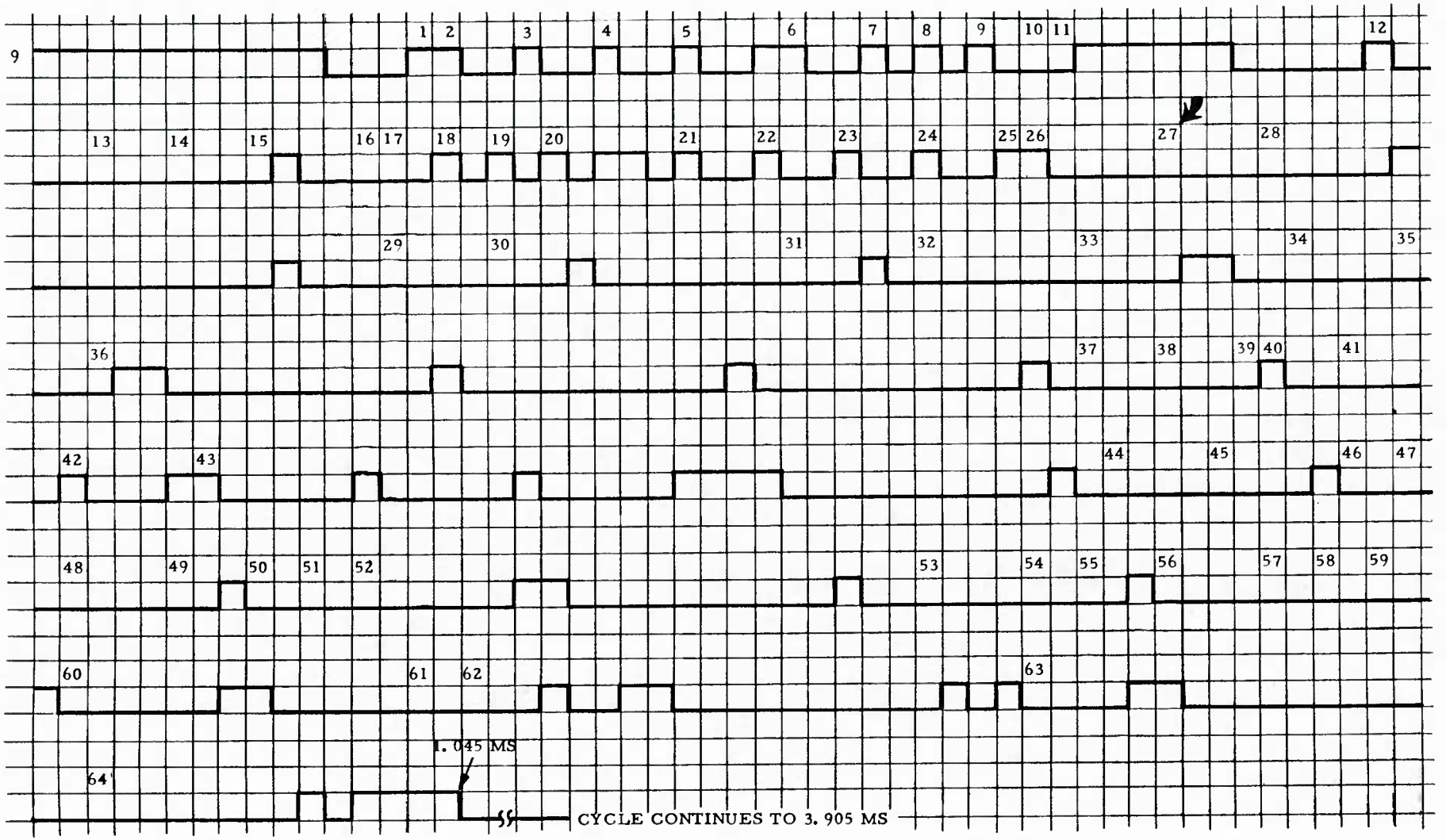


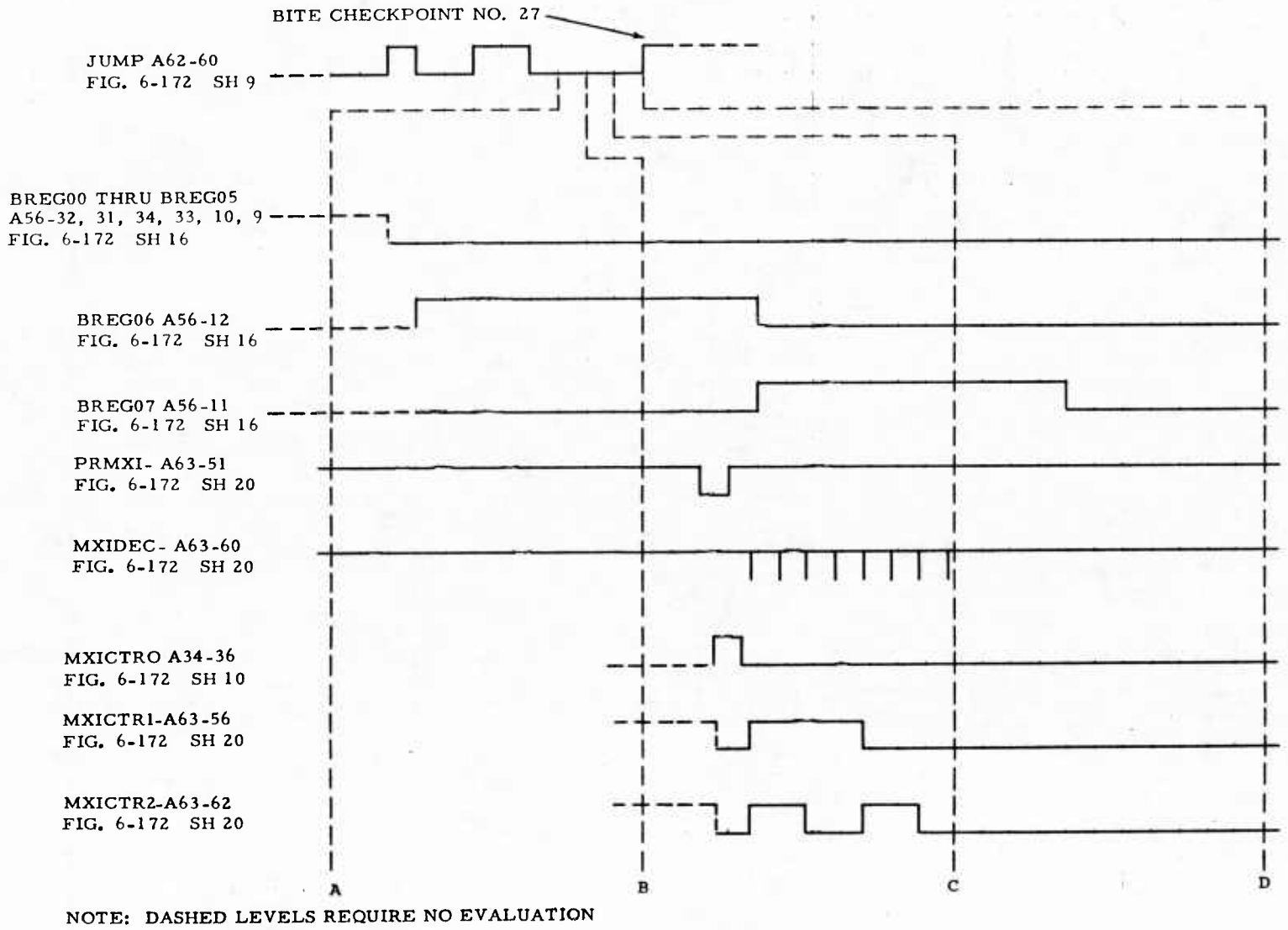
Figure 5-18. BITE Checkpoints Waveform (Jump Signal)

Figure B-2. Troubleshooting MCU using OP--jump waveform.

TABLE 5-10. PROBABLE FAULTS ASSOCIATED WITH FAULT INDICATORS 1 DURING TEST A (Cont)

BITE Checkpoint No. at which waveform differs	Probable Fault	Waveforms/Timing Diagrams of possible faulty signals
22	Register B Bit 3	5-40
23	Register B Bit 2	5-41
24	Register B Bit 1	5-42
25	Register B Bit 0	5-43
26	JPB instruction	5-44
27	SRB1 instruction	5-45
28	SRB7 instruction	5-46
29	STAA, LDAA instructions	5-47
30	STAA, LDAA instructions	5-48
31	STAB instruction	5-49
32	STAB instruction	5-50
33	AND instruction	5-51
34	OR instruction	5-52
35	INVA instruction	5-53
36	INVB instruction	5-54
37	BZD, STAD instruction	5-55
38	JPC instruction	5-56
39	CTB instruction	5-57
40	JPC, CTB instructions	5-58
41	CTB instruction	5-59
42	SLC1 instruction	5-60
43	SLC7 instruction	5-61
44	DUS8 instruction	5-62
45	DUS8 instruction	5-63
46	DUS8 instruction	5-64
47	DUS8 instruction	5-65
48	DUS8 instruction	5-66

Figure B-3. Troubleshooting MCU using OP--fault locator.



NOTE: DASHED LEVELS REQUIRE NO EVALUATION

Figure B-4. Troubleshooting MCU using OP--BITE checkpoint.

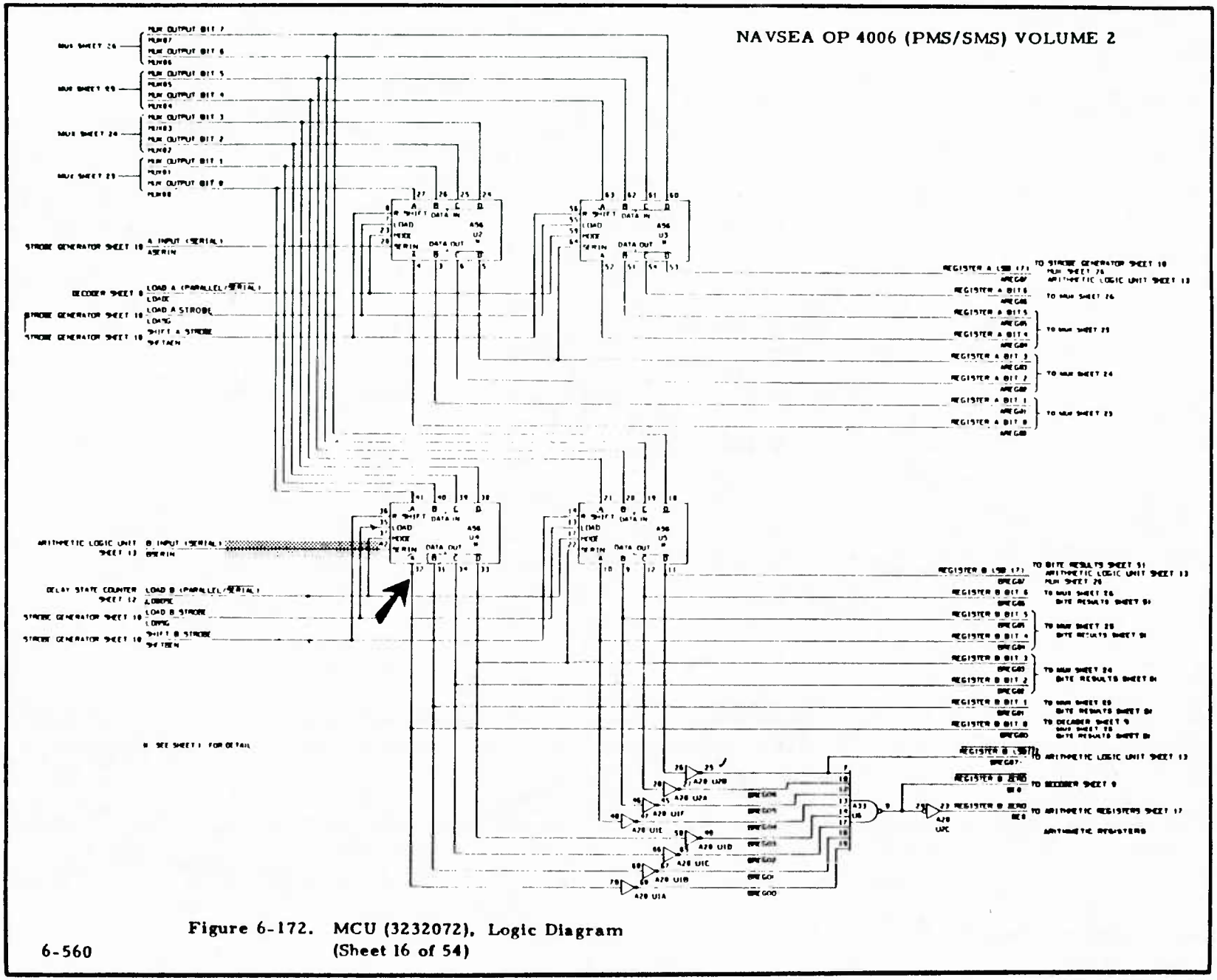


Figure 6-172. MCU (3232072), Logic Diagram (Sheet 16 of 54)

6-560

Figure B-5a. Figure 6-172, sheet 16 of 54 (OP 4006).

Figure B-5. Troubleshooting digital-solid state circuitry in the MCU.

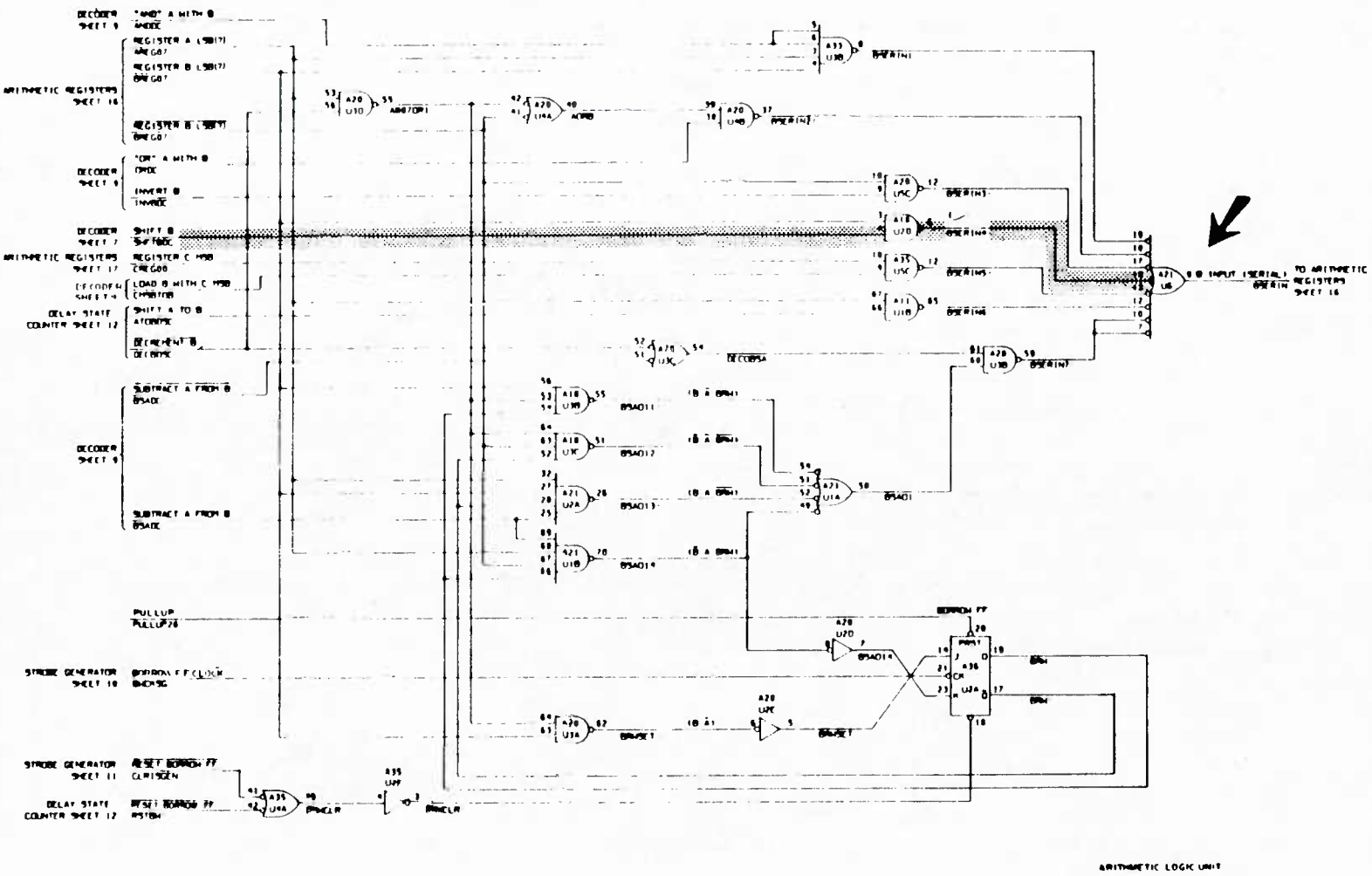


Figure 6-172. MCU (3232072), Logic Diagram
(Sheet 13 of 54)

6-557

Figure B-5b. Figure 6-172 sheet 13, of 54 (OP 4006).

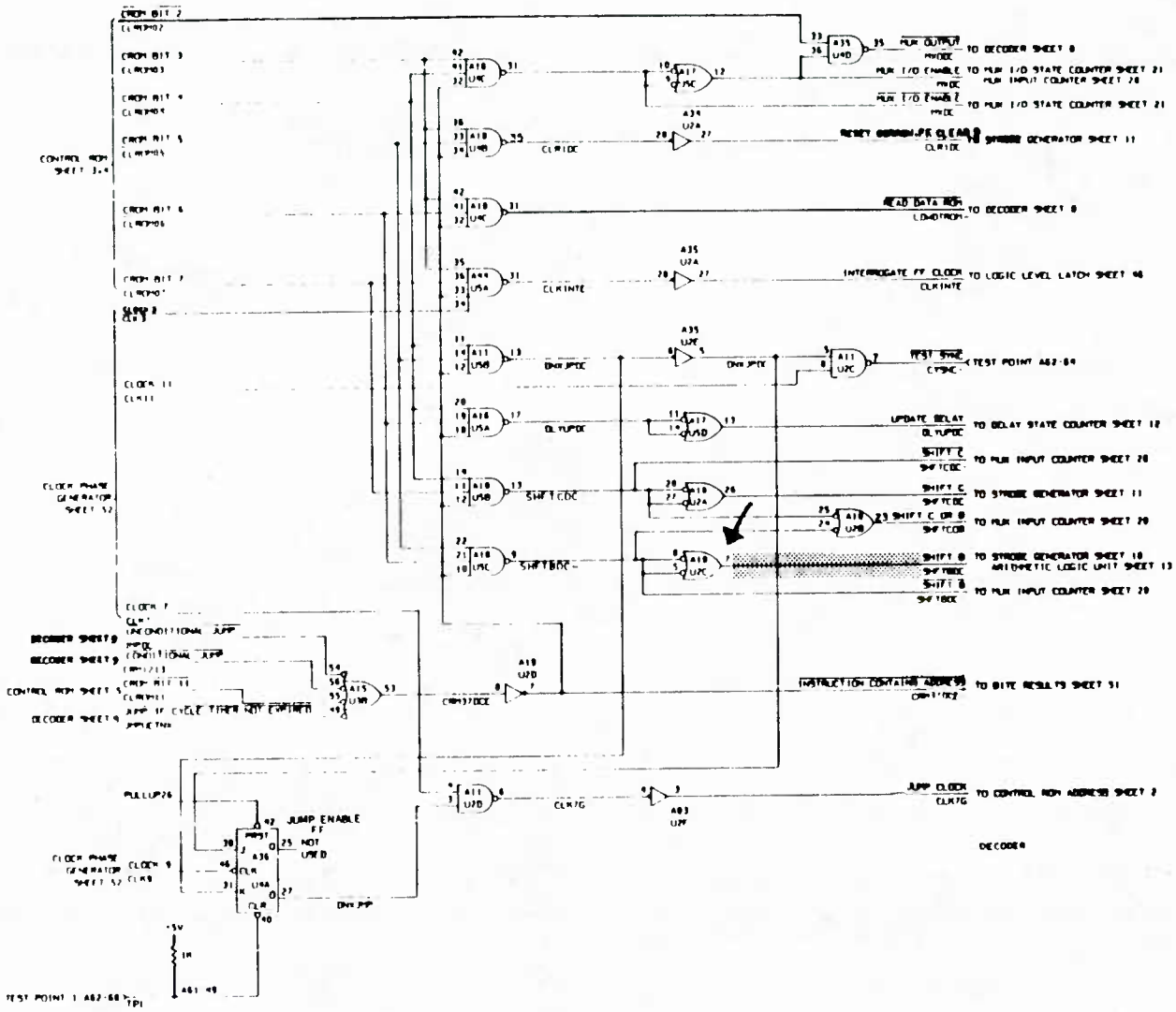


Figure 6-172. MCU (3232072), Logic Diagram
(Sheet 7 of 54)

6-55f

Figure B-5c. Figure 6-172, sheet 7 of 54 (OP 4006).

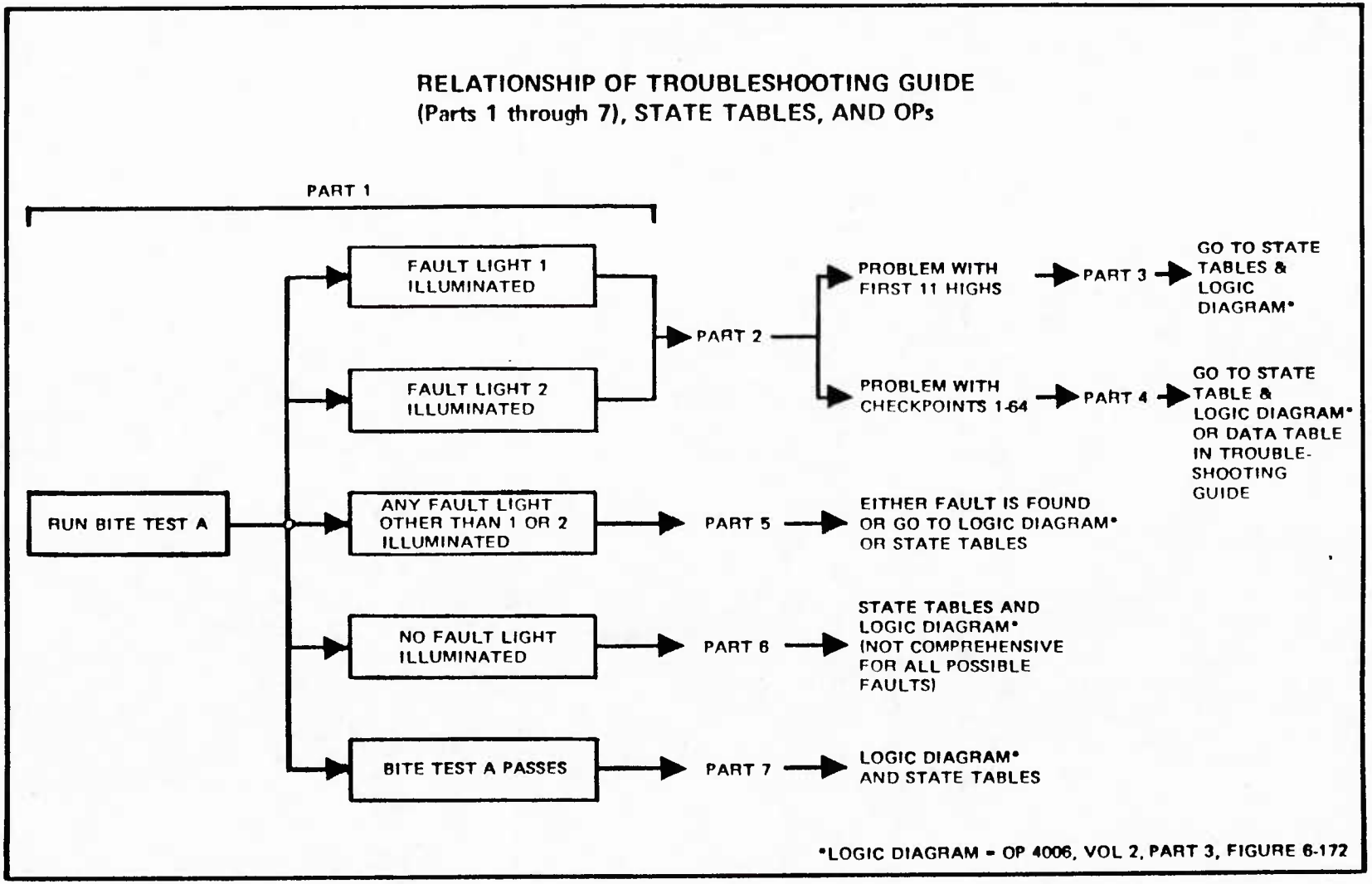


Figure B-6. Relationship of troubleshooting guide parts, STs, and OPs.

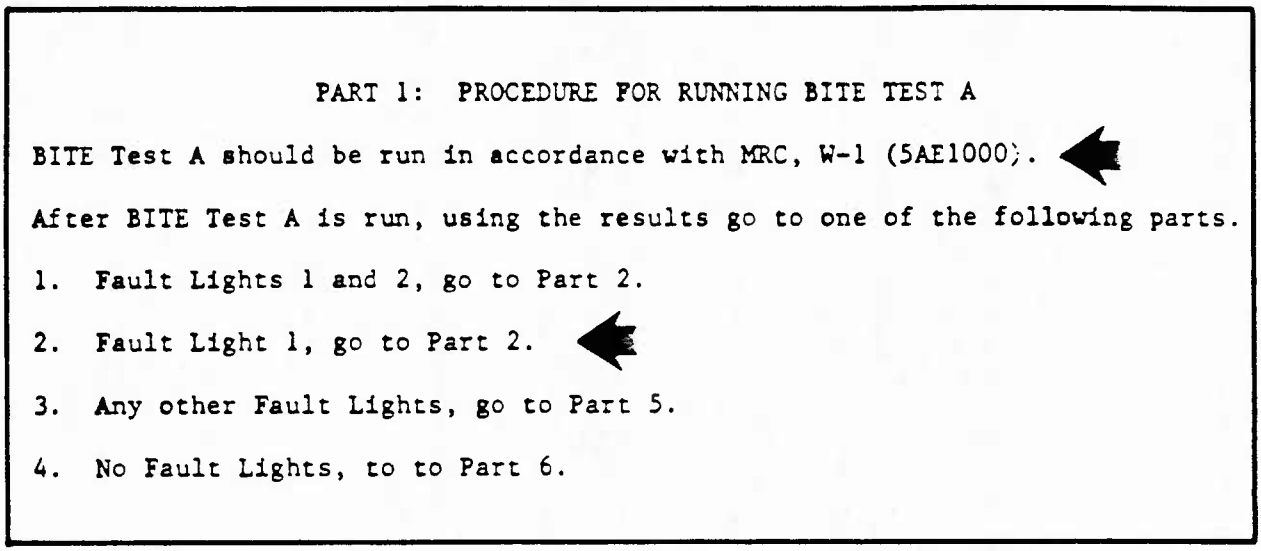


Figure B-7. Troubleshooting MCU using troubleshooting guide, Part 1.

PART 2
Section 1:

TURN ON PROCEDURE

464 STORAGE OSCILLOSCOPE

Make all adjustments prior to turning oscilloscope ON

Procedure is for 64 BITE Checkpoints

Vertical Section	
Position knob (Ch 1 & 2)	Midposition
Volts/Div (Ch 1 & 2)	2 (on 10X scale)
(Ensure 10X probe is in 10X Mode)	
Coupling (Ch 1 & 2)	DC
Vert Mode	Alt
Intensity	Midposition (then adjust)
Focus	Midposition (then adjust)
Storage	
Save pushbutton	out
Non Store pushbutton	in
Var Pers pushbutton	out
Fast pushbutton	out
Position	Midposition
A Time Base (Lower section)	
Trig Mode	Auto
Coupling	DC
Source	Ext
Slope	+
Level	Midposition
B Time Base (Upper section)	
Delay Time Position	0.5
Coupling	DC
Source	Starts After Delay
Slope	+
Level	Midposition
A/B Time/Div	
Outer ring (A - clear)	0.1 ms/div
Inner ring (B - gray - pull out to turn	5 us/div
Horizontal Display	B Dlyd
All Var knobs	Calibrate (full cw)

Turn ON by pulling ON pushbutton
Adjust Intensity and Focus to satisfy
Use Delay Time Position to observe different parts of
64 BITE Checkpoints waveform

Figure B-8. Troubleshooting MCU using troubleshooting guide, Part 2, Section 1.

PART 2
SECTION 2:

SETUP PROCEDURE FOR THE MCU

The following procedure is to be used for Fault Lights No. 1 and No. 2.

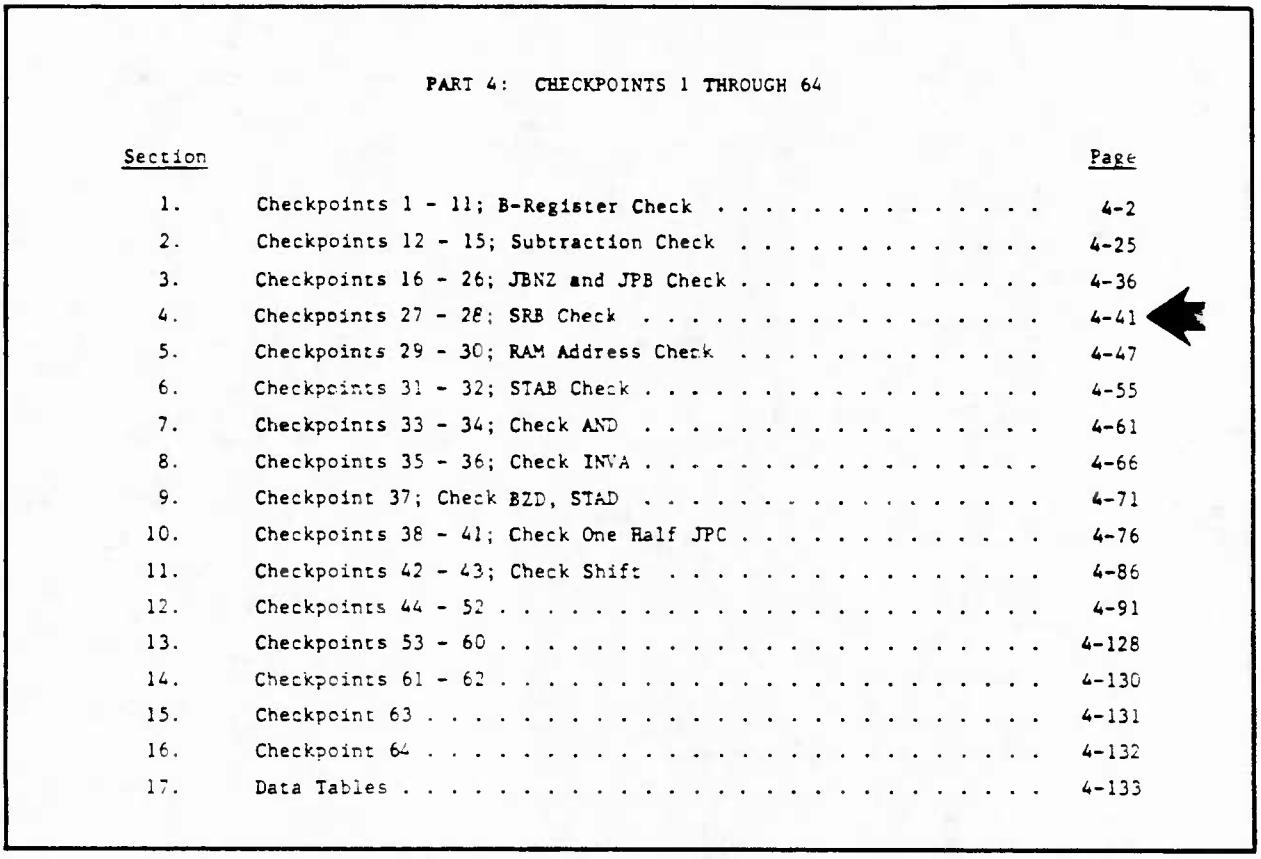
SETUP PROCEDURE:

1. Turn BITE Test switch to off.
2. Turn power off.
3. Install a jumper between Pins 67 and 71, on the Jumper Test Card.
4. Insert the Jumper Test Card into Slot A62 of the MCU.
5. Synchronize the oscilloscope to A62-63.
6. Connect Channel A to A62-60, the Jump Signal.
7. Connect Channel B to A62-59, the $\overline{\text{Clock 3}}$ signal.
8. Turn power on.
9. Run BITE Test A again.
10. Now use Section 3 (Part 2), the Jump Waveform to find the BAD CHECKPOINT.

    If the problem is with the first 11 Highs, then proceed to Part 3.

    If the problem is with Checkpoints 1 thru 64, then proceed to Part 4.

Figure B-9. Troubleshooting MCU using troubleshooting guide, Part 2, Section 2.



PART 4: CHECKPOINTS 1 THROUGH 64

Figure B-10. Troubleshooting MCU using troubleshooting guide, table of contents for Part 4.

SECTION 4: CHECKPOINTS 27 AND 28 (SRB CHECK)

1. TEST DESCRIPTION:

Checkpoints 27 and 28 verify the SRB Instruction and that the B-register can shift properly.

The B-register is loaded with a known value then shifted by an SRB Instruction. The A-register is then loaded with the same value that the shifting should have caused in the B-register. A subtract is then performed. The result should be zero. A JBNZ Instruction is then performed. No jump should take place. A jump would indicate the SRB Instruction is not shifting the B-register properly. The same process is then repeated, this time however, the shift is large enough to check out the end around feature of the B-register.

A failure at this JBNZ Instruction would indicate that the end around is not functioning properly.

2. TEST VERIFICATION:

(a) SRB Instruction

(b) ROM Addresses

3. Proceed to the write-up on the first individual checkpoint that has malfunctioned, using the following Table of Contents.

TABLE OF CONTENTS

Figure B-11. Troubleshooting MCU using troubleshooting guide, Section 4.

SECTION 4: CHECKPOINTS 27 AND 28 (SRB CHECK)

TOPIC 1: CHECKPOINT 27

1. VERIFICATION:

Checkpoint 27 verifies that each of the following are functioning properly.

1. SRB Instruction
2. The B-register will right shift correctly.
3. ROM Address 20 contains $(01)_{16}$.
4. ROM Address 24 contains $(02)_{16}$.

2. DESCRIPTION:

An LDAB Instruction is executed to load the RAM Counter with $(04)_{16}$. It will also load the B-register but the data is insignificant since the B-register is immediately reloaded by an LDOB Instruction. The B-register will be loaded from ROM Address $(24)_{16}$ and at the completion of the LDOB Instruction the B-register will contain $(02)_{16}$. The SRB Instruction that is executed next will right shift the B-register one bit position. Now the B-register contains $(01)_{16}$. The next instruction will perform two operations an LDOA and a subtract. The LDOA will load the contents, $(01)_{16}$, of ROM Address $(20)_{16}$ into the A-register. Now the contents of the A-register from the B-register. The result is placed in the B-register which is $(00)_{16}$. A JBNZ Instruction is now executed. No jump should take place since the B-register equals $(00)_{16}$.

Failure at checkpoint 27 indicates that the SRB Instruction is not shifting the B-register properly.

3. WAVEFORM:

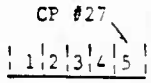


Figure B-12. Troubleshooting MCU using troubleshooting guide, Section 4, Topic 1.

4. INSTRUCTIONS

INSTRUCTIONS					TROUBLESHOOTING PROCEDURES
TIME	HEX ADD	HEX CON	MNE	ACTION PERFORMED	
1	41B	FB6F	LDAB	Loads $(04)_{16}$ into the RAM Counter. Will also load the contents of RAM Address $(04)_{16}$ into the B-register.	Step 1 - Check the contents of the B-register at A56 (6-560). Does the B-register contain $(02)_{16}$ at the end of Time 2? (a) YES - Proceed to Step 2. (b) NO - Proceed to Step 4.
2	41C	6D7F	LDOB	Loads the contents of ROM Address $(24)_{16}$ into the B-register. The B-register will contain $(02)_{16}$.	Step 2 - Check the contents of the B-register at A56 (6-560). Does the B-register contain (01) at the end of Time 3? (a) YES - Proceed to Step 3. (b) NO - Troubleshoot the SRB State Table during Time 3. If the B-register equals $(81)_{16}$ pay particular attention to the B-input (serial) (A21 page 6-557) and BSE41N4 (A18 page 6-557).
3	41D	F9FF	SRB	Will right shift the B-register one bit position. The B-register will contain $(01)_{16}$.	
4	41E	ED3A	LDOA	Loads the contents of ROM Address $(20)_{16}$ into the A-register. The A-register will contain $(01)_{16}$.	
			SUB	The contents of the A-register is subtracted from the B-register. The result will be placed in the B-register which will be $(00)_{16}$.	Step 3 - Check the contents of the A-register at A56 (6-560). Does it equal $(01)_{16}$ during Time 4? (a) YES - Troubleshoot the Subtract State Table using Data Table 6 during Time 4. Data Tables are located in Part 4 Section 17. (b) NO - Troubleshoot the LDOA State Table during Time 4. Verify all the data is correct as well as the Control Signals.
5 (CP27)	41F	A391	JBNZ	Conditional Jump. Will only jump if the B-register does not equal zero. Should not jump.	Step 4 - Check the output of the RAM Counter at A63 (6-562). Does the RAM Counter equal $(04)_{16}$ at the end of Time 1? (a) YES - Troubleshoot the LDOB State Table during Time 2. Verify all data is correct as well as the Control Signals.

Figure B-13. Troubleshooting MCU using troubleshooting guide instructions.

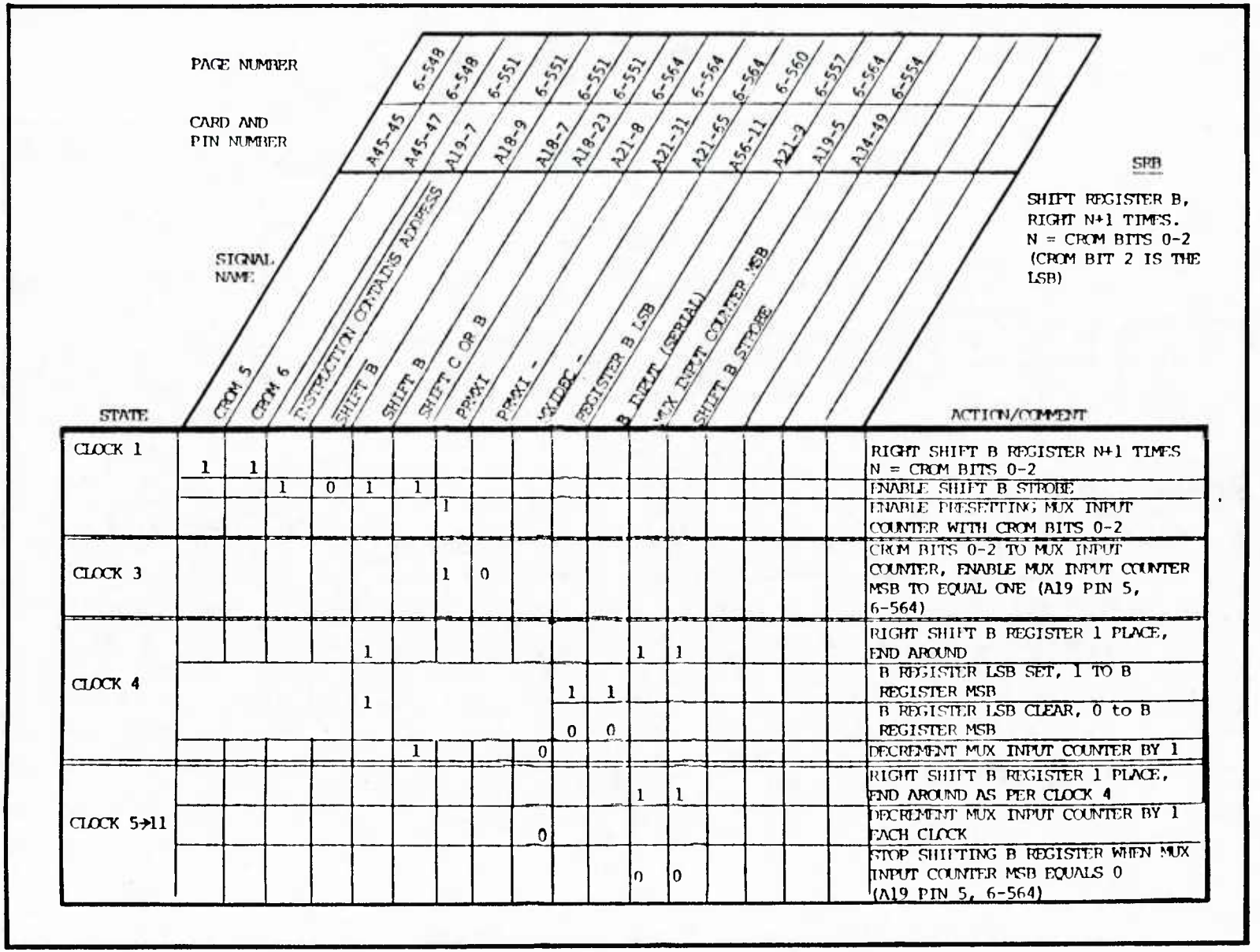


Figure B-14. Troubleshooting MCU using ST.

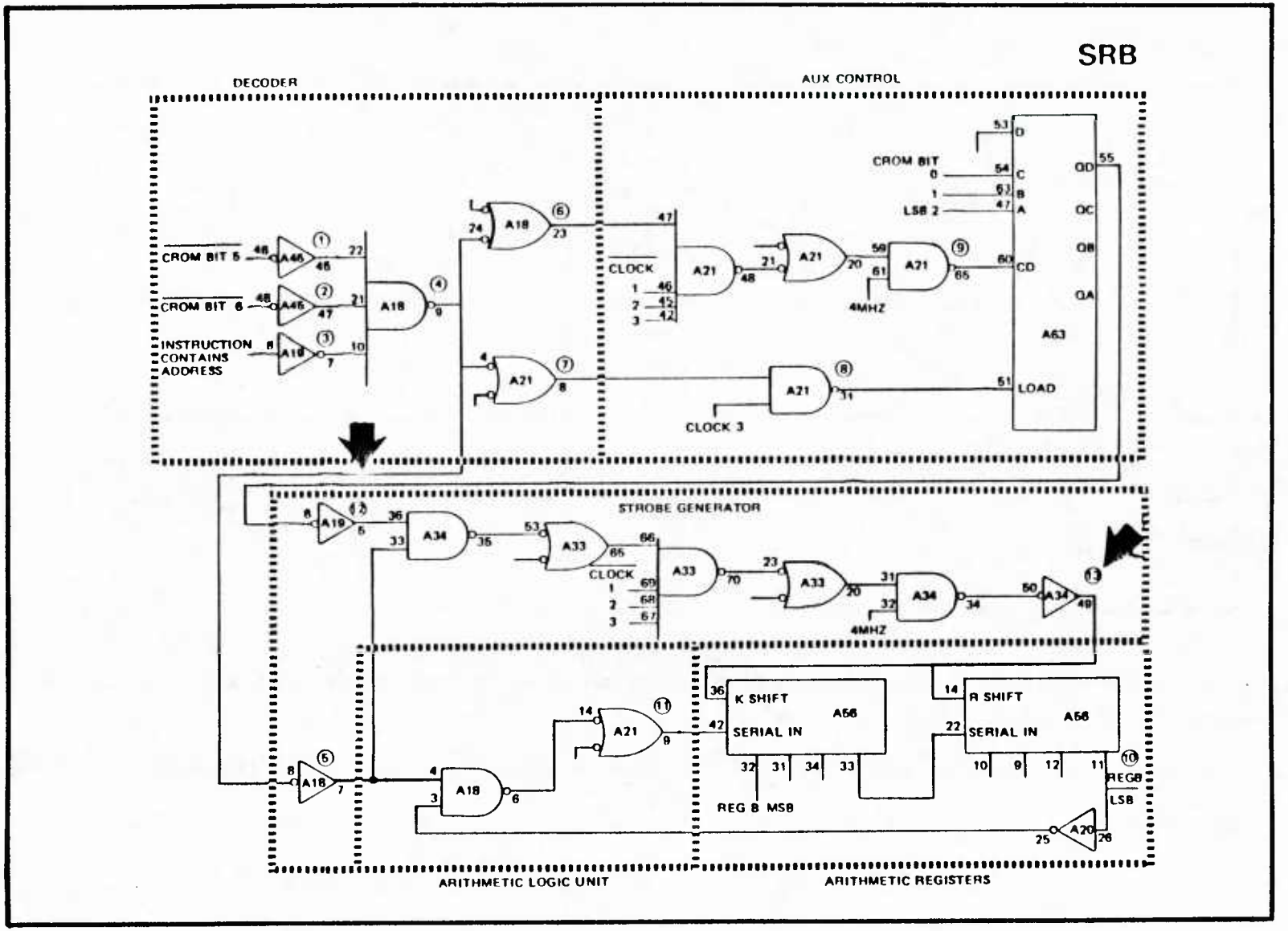


Figure B-14. Troubleshooting MCU using ST.

DISTRIBUTION LIST

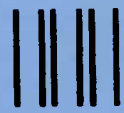
Deputy Under Secretary of Defense for Research and Engineering (Research and Advanced Technology)
Military Assistant for Training and Personnel Technology (OSUDS) (R&AT)
Chief of Naval Operations (OP-01), (OP-01B7) (2), (OP-11), (OP-135C4), (OP-140F2), (OP-987H)
Chief of Naval Material (NMAT 0722)
Chief of Naval Research (Code 270), (Code 440), (Code 442), (Code 442PT)
Chief of Naval Education and Training (Code 00A), (Code N-21), (Code N-24), (Code L-02)
Director, Naval Education and Training Program Development Center, Millington
Commanding Officer, Naval Education and Training Program, Personnel and Training Research, (Code IPD) Pensacola
Naval Education and Training Support Center, Pacific
Chief of Naval Technical Training (Code 00), (Code N-6)
Commander, Naval Ocean Systems Center
Commander, David W. Taylor Naval Ship Center
Commanding Officer, Naval Training Equipment Center (Technical Library) (5), (Code 1), Code 7)
Commanding Officer, Naval Underwater Systems Center
Commander, Naval Air Systems Command (AIR 37)
Commander, Naval Electronic Systems Command
Commander, Naval Sea Systems Command
Commander, Army Research Institute for the Behavioral and Social Sciences, Alexandria (PERI-ASL), (PERI-ZT), (PERI-SZ), (Director, U.S. Army ATCO (Ft. Eustis, VA))
Director, U.S. Army Tradoc Systems Analysis Activity (ATTA-SL) (White Sands Missile Range, NM)
Commander, Air Force Human Resources Laboratory, Brooks Air Force Base (Manpower and Personnel Division) (2), (Scientific and Technical Information Office) (TSRL/Technical Library), (AFHRL/DOJZ)
Commander, Air Force Human Resources Laboratory, Williams Air Force Base (AFHRL/OT)
Commander, Air Force Human Resources Laboratory, Wright-Patterson Air Force Base (AFHRL/LR-TDC)
Commander, Air Force Human Resources Laboratory, Lowry Air Force Base (AFHRL/LRT)
Superintendent, Naval Postgraduate School
Director of Research, U.S. Naval Academy
Defense Technical Information Center (DDA) (12)

U2190S6

DEPARTMENT OF THE NAVY

NAVY PERSONNEL RESEARCH AND
DEVELOPMENT CENTER
SAN DIEGO, CALIFORNIA 92152

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300



POSTAGE AND FEES PAID
DEPARTMENT OF THE NAVY
DoD-316

SUPERINTENDENT
NAVAL POSTGRADUATE SCHOOL
MONTEREY CA 93940-0000

0142