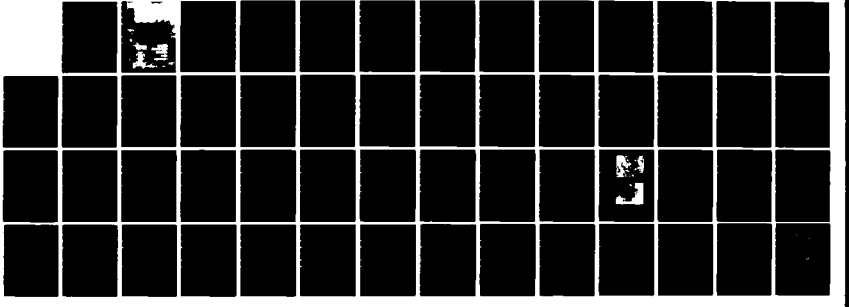
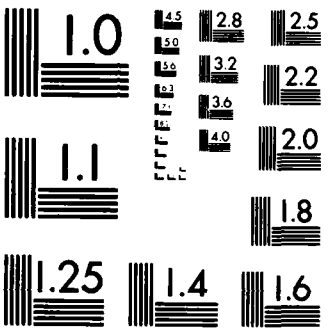
AD-A156 638 INTRINSIC MECHANISMS OF MULTILAYER CERAMIC CAPACITOR FAILURE(U) VIRGINIA POLYTECHNIC INST AND STATE UNIV BLACKSBURG L C BURTON APR 85 N00014-83-K-0168 1/1

UNCLASSIFIED F/G 9/1 NL





INTRINSIC MECHANISMS OF MULTI-LAYER CERAMIC CAPACITOR FAILURE

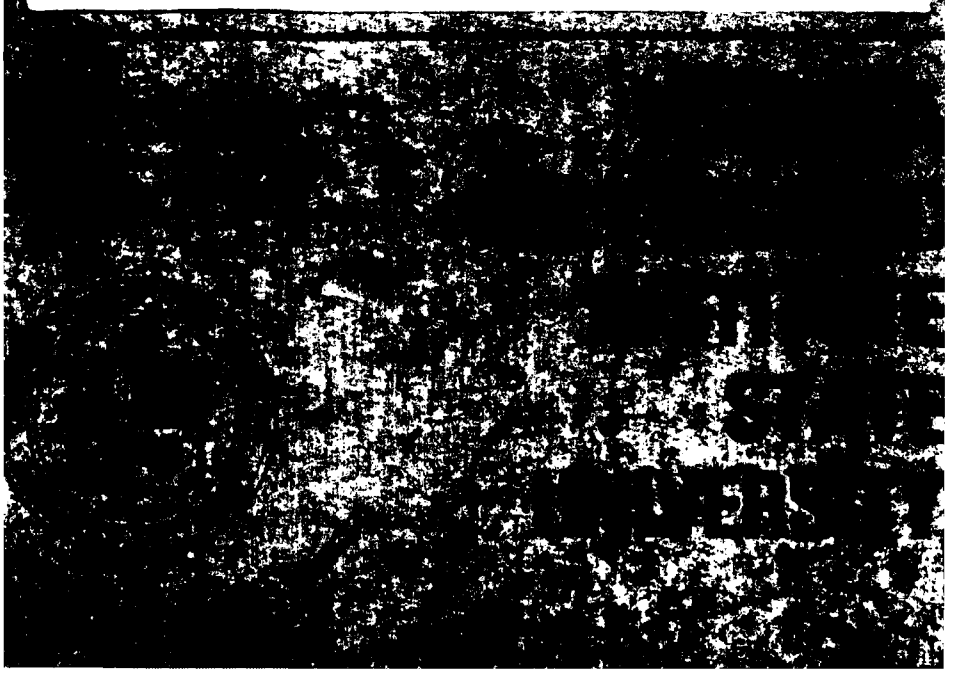
ANNUAL REPORT

Time Period: 3/15/84-3/14/85

ONR Contract No. N00014-83-K-0168

Principal Investigator: L. C. Burton

April, 1985



INTRINSIC MECHANISMS OF MULTI-LAYER CERAMIC CAPACITOR FAILURE

ANNUAL REPORT

Time Period: 3/15/84-3/14/85

ONR Contract No. N00014-83-K-0168

Principal Investigator: L. C. Burton

April, 1985

Departments of Electrical Engineering and Materials Engineering

Virginia Polytechnic Institute and State University

Blacksburg, VA 24061

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION: Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT: Approved for Public Release: Distribution Unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION: VPI&SU; 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION
6c. ADDRESS (City, State and ZIP Code): EE Dept. Blacksburg, VA 24061	7b. ADDRESS (City, State and ZIP Code)
8a. NAME OF FUNDING/SPONSORING ORGANIZATION: Office of Naval Research; 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER: N00014-83-K-0168
8c. ADDRESS (City, State and ZIP Code): Division of Materials Research Arlington, VA 22217	10. SOURCE OF FUNDING NOS. — PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO / WORK UNIT NO.
11. TITLE (Include Security Classification): Intrinsic Mechanisms of Multilayer Ceramic Capacitor Failure	
12. PERSONAL AUTHOR(S): L. C. Burton	
13a. TYPE OF REPORT: Annual; 13b. TIME COVERED: FROM 3/15/84 TO 3/14/85; 14. DATE OF REPORT (Yr., Mo., Day): 1985 April; 15. PAGE COUNT	
16. SUPPLEMENTARY NOTATION	

17. COSATI CODES		
FIELD	GROUP	SUB GR.

18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
Multilayer Capacitors; Capacitor Reliability; Leakage Currents; Transport Physics; Grain Boundaries

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

The possible role of grain boundaries (GB) in MLC capacitors, with respect to insulation resistance and its degradation, is reviewed. Activation energy (E_A) can be related directly to GB barrier height, ϕ_B. The voltage dependent activation energies for poly-Si, ZnO varistors and PTC devices has been attributed directly to ϕ_B. Varistor and PTC device degradation is caused GB passivation. A similar voltage dependence is reported here for barrier layer and COG capacitor types where E_A decreases from 0.91 to 0.44eV and from 1.61 to 0.90eV respectively, with concurrent super-ohmic increases in leakage current. Such a voltage dependent E_A is not seen for X7R devices, even though the current is super-ohmic. Reasons to account for this are discussed.

It is concluded that the GB potential barrier may offer a major source of impedance to leakage current for MLC capacitors, and its decrease may result in failure.

It has been ascertained that E_A decreases for degraded X7R devices, with an increase in

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT: UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS ☐	21. ABSTRACT SECURITY CLASSIFICATION
22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE NUMBER (Include Area Code); 22c. OFFICE SYMBOL

DD FORM 1473, 83 APR EDITION OF 73 IS OBSOLETE

SECURITY CLASSIFICATION OF THIS PAGE

the I-V slope. These results are consistent with our earlier reports on degraded devices, and with the space charge limited current model for emission from electrodes.

X7R chips with no internal electrodes exhibit both ohmic and super-ohmic characteristics, with activation energies independent of voltage. The super-ohmic is ambient dependent; the ohmic region is not. This indicates the importance of electrode dominated injection at higher voltages. These measurements are correlated with those from similar internally electroded chips. It is proposed that space charge limited electron current controls the steady state leakage current for X7R capacitors above roughly 1 volt bias.

A near-exponential rate of current increase with time, accompanied by a linear decrease in E_A, was seen for both X7R and Z5U capacitors. The current increase for the Z5U could be reversed for a time by changing polarity, with degradation ensuing. This cyclical phenomenon is attributed to the movement of a low resistivity front across the ceramic layer.

1. INTRODUCTION

The objectives of this program are to study leakage currents in MLC capacitors and capacitor related ceramic, and to try and understand what controls the current, and causes it to increase.

During the first year of our work, we modelled the leakage current for X7R devices on space charge controlled emission from non-planar electrodes. Thermoelectric studies on X7R chips indicated that carrier concentration and mobility both increase for reduced ceramic, with activation energy being largely due to mobility. Activation energies decreased for degraded devices.

During this year, we have made an effort to better understand the role of grain boundaries from an electrical viewpoint, and how these could control activation energy and current. There is much literature related to grain boundary controlled currents for other devices, where current is a key output parameter (which it is not for an MLC capacitor, except in the context of degradation). The importance of grain boundaries in current transport is reviewed, and measurements made on MLC devices are reported. There are striking similarities between the leakage current properties of barrier layer and COG capacitors, and those of various other poly crystalline devices.

Last year we proposed the importance of electron injection from electrodes, which resulted in space charge limited currents. We have extended these studies to X7R chips with no internal electrodes, and have been able to separate the ohmic and super-ohmic regimes of current. The latter current is similar to that seen for X7R capacitors, is dependent on ambient, and is dependent on the metal-ceramic interface. The distinct ohmic region is not seen in actual capacitors, due to the thinness of the dielectric; space charge current dominates for all voltages over about 1 volt.

The results reported below have enhanced the possible role of grain boundaries as being major factors in MLC ceramic resistance. These results also confirm the significance of the metal-ceramic interface with respect to leakage current.

Additional participants in this program include H. Y. Lee, K. C. Lee, J. N. Schunke and S. Agarwal.

2. RESULTS AND DISCUSSION

2.1 ROLE OF GRAIN BOUNDARIES IN MLC CAPACITOR LEAKAGE CURRENTS

It is known that grain boundaries (GB) control charge transport in several types of polycrystalline materials and devices. These include poly-Si[1], ZnO varistors[2], $BaTiO_3$ based thermistors[3], grain boundary capacitors[4] and thin film solar cells.[5] Since currents are controlled by GB in these cases, so is leakage current degradation, since current is an important output parameter for all of them. A pertinent question therefore is: What roles, if any, do GB play with respect to insulation resistance and its degradation for multilayer ceramic capacitors?

We have addressed this question by reviewing published reports for the other types of polycrystalline devices, and then applying these analyses to MLC capacitors. Some background information is first given below, followed by a discussion of the measurements.

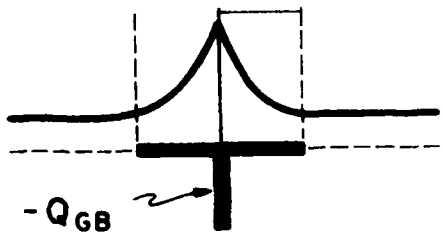
Impedance of a GB to current flow is caused by a potential spike (in the conduction band for electrons or the valence band for holes) due to charge at the GB. In an n-type semiconductor or semi-insulator, this charge consists of electrons trapped at the GB, with an equal and opposite charge induced in adjacent layers. Additional charge can arise from electrons trapped while traversing the GB under biased conditions, from a discontinuity in the normal component of polarization, and from trapped ions. The latter two sources of charge can be compensating as well, reducing the net charge at the GB.

Several possible types of GB potential energy diagrams are shown in Figure 1. Any of these, and other, could pertain to MLC capacitors.

The most common depiction of a charged GB is shown in Fig. 1a, where negative charge Q_{GB} trapped at the GB equals induced positive charge in adjacent regions. The barrier height ϕ_B at zero bias is given by

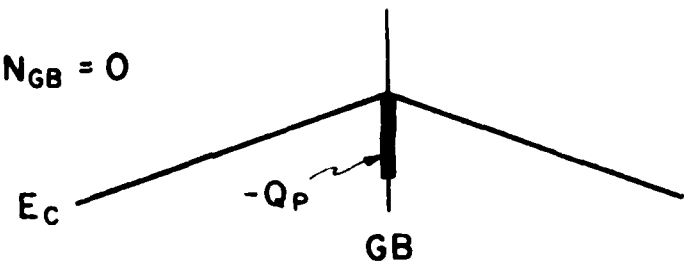
a) $\Delta P_N = 0$; $Q_{GB} = qN_{GB}$

Homogenous grains



Examples: poly-si thin films

b) $\Delta P_N = Q$; $N_{GB} = 0$



c) $\Delta P_N = N_{GB} = 0$
(Flat bands)

Example: reduced poly-si

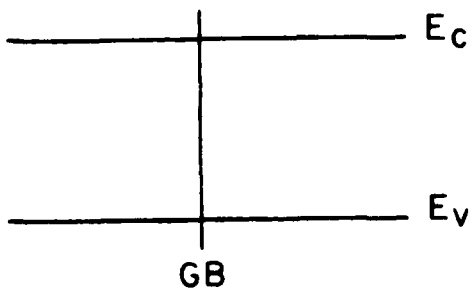


Figure 1: Grain boundary (GB) potential energy diagrams, for a) negative charge trapped at GB, b) normal polarization discontinuity, and c) no charge at or near GB.

$$\phi_B(V=0) = \phi_{BO} = \frac{q^2 N_D W^2}{2\varepsilon} = \frac{q^2 N_{GB}^2}{2\varepsilon N_D} \qquad (1)$$

where N_D = donor density in the grains

N_{GB} = density of filled states in the GB

W = width of space charge region

The grains are assumed to be homogeneous in this case. Examples where this model is often applied are poly-Si, thin films, and varistors.

Another source of GB potential barrier is charge Q_p resulting from spontaneous polarization discontinuity, as illustrated in Fig. 1b. Here the GB state density is assumed zero, and GB charge is due solely to ΔP_N, the discontinuity in the normal component of polarization P_N, across the interface: $Q_p = \Delta P_N$ (coul/m^2)*. The potential is linear because the only charge resides at the GB. One model where this type of charge density is used is that for the low temperature (high conductivity) region of $BaTiO_3$ based thermistors.

If there is no charge in the GB region, then Poisson's equation dictates that the bands be flat, as shown in Fig. 1c. Thermal emission of carriers across the GB is not impeded in this case, which is therefore analogous to a single crystal. There are some pertinent polycrystalline cases that are modelled on Fig. 1c: a) poly-Si hydrogenated during or subsequent to growth; hydrogenation passivates dangling bonds at the GB, and $N_{GB} \approx 0$; b) $BaTiO_3$ based thermistor heated in reducing ambient (H_2,CO or NH_3); c) many other

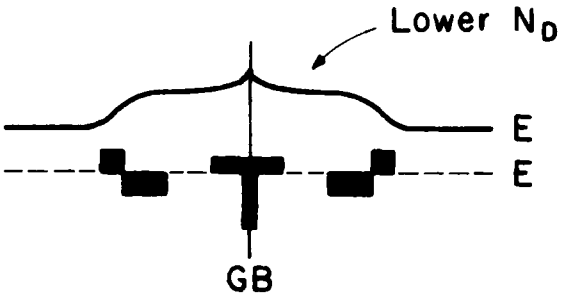
---

*This relation comes from $\nabla \cdot D = \rho$, which results in $\Delta D_N = \rho \Delta X$. Since $D = \varepsilon_o E + P \approx P$ for $\varepsilon >> \varepsilon_o$, $\Delta D_N = \Delta P_N = \rho \Delta X \equiv Q_p$

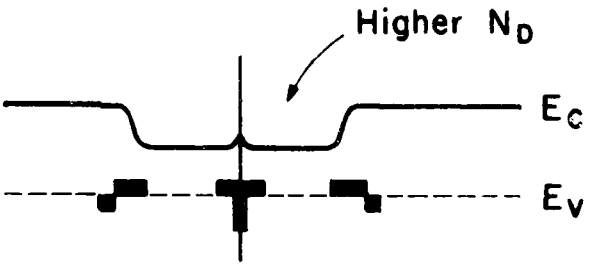
Inhomogeneous Grain

Example:

a) $BaTiO_3$ Ceramic
(Thermistor)



b)



c) 2nd Material

Example:

BL Capacitor

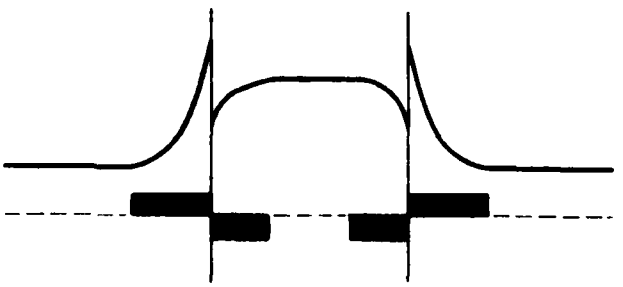


Figure 2. Band diagrams for inhomogeneous grain boundaries; a) high resistance layer near GB, b) low resistance layer, c) presence of second material or phase.

polycrystalline materials (including semiconductor thin films) heated in reducing ambients.

A reduction in the GB barrier height is desirable if lower resistance is desired (such as for hydrogenated poly-Si, for example). However, this process can be detrimental if high resistance is desired, and has been used to model degraded ZnO varistors.[6] Reduced thermal activation energies and degraded characteristics can be attributed to reduced GB barrier height. From equation 1, reduced ϕ_B can result from a decrease in N_{GB} or an increase in N_D (and from the temperature dependence of ϵ in the case of the thermistor.) Positive ion accumulation at the GB could also reduce Q_{GB} and ϕ_B.

Modelling of electrical properties and degradation of GB impedance depends on assumed properties of the GB. The grains were assumed homogeneous for the GB of Fig. 1a. Other examples are shown in Fig. 2, for the following cases: a) Lower donor density (N_D) region near the GB, which is totally depleted; b) Higher N_D region near the GB; c) second phase or composition region separating the GB. It is expected that the structure of Fig. 2a will be less sensitive to applied voltage than that of Fig. 1a, since it is "clamped" by the lower N_D layer.

The GB charge Q_{GB} due to electrons trapped there is given by

$$Q_{GB} = q \int_{E_v}^{E_c} N^*_{GB}(E)\, dE = q \int_{E_F}^{E_c} N_{GB}(E) F(E,E_F) dE$$

or

$$Q_{GB} \approx q \int_{E_v}^{E_F} N_{GB}(E) dE \qquad (2)$$

where N_{GB} = GB state density (per eV)

N^{*}_{GB} = occupied GB state density

Sources of the GB states N_{GB} are lattice mismatch dangling bonds and interface strain and defects. Additional sources of negative charge are anion acceptors ($O^{=}$ and Cl^{-} for example), cation vacancies (eg. Ba in $BaTiO_3$) and the normal spontaneous polarization discontinuity.

Sources of positive space charge adjacent to the GB are ionized donors ($V_O^{\cdot\cdot}$, Nb^{+} etc.), and charge resulting from donor density gradients. This latter charge is real charge independent of the GB charge, and has the form*

$$\rho(x) = \frac{-\varepsilon kT}{q}\left[\frac{1}{N_D}\frac{d^2N_D}{dx^2} - \frac{1}{N_D{}^2}\left(\frac{dN_D}{dx}\right)^2\right] \qquad (3)$$

For example, if N_D increases outward from the GB, then a built-in electric field normal to the GB exists, and the potential energy decreases away from the GB. A potential hump will thus exist in this region, and electron flow will be impeded in the same manner as if the hump were due to negative charge trapped in GB states. Homogenization of N_D in this region will smooth out the energy bands and lower the resistivity. This may be a factor related to stability of non-homogeneous ceramic.

If charge transport is controlled by GB, then the GB barrier height ϕ_B can be deduced from activation energy E_A, using the relation

$$\phi_B = E_A + T\,\partial\phi_B/\partial T \qquad (4)$$

---

*If N_D is a function of x, then the built-in field E in 1-dimension is $E = \frac{-kT}{qN_D}\frac{dN_D}{dx}$. From $dE/dx = \rho/\varepsilon$, where ρ is the charge density, we obtain equation 3.

The temperature correction may be substantial and is often neglected in the literature. The magnitude of $\partial\phi_B/\partial T$ is small and negative, paralleling that of the band gap. (For example, if $\partial\phi_B/\partial T = -2 \times 10^{-4}$eV/K and T = 500K then a -0.1eV correction results, which is substantial, since leakage current varies exponentially with ϕ_B).

Changes in ϕ_B caused by applied voltage (i.e. voltage dropped across the GB space charge, and/or causing GB state occupation to change) will be followed by a change in E_A, since

$$\phi_B(V) = E_A(V) + T\,\partial\phi_B/\partial T \qquad (5)$$

and the temperature correction term is probably voltage independent. Thus, with applied voltage, a decrease seen in the experimental parameter E_A is accompanied by an equal decrease in ϕ_B. This fact has been used to model GB transport for poly-Si[1] and ZnO varistors.[2] We propose that it may also apply to certain types of MLC capacitors. In this context, the GB potential could not only effect leakage current, but a decrease in ϕ_B with time could cause degradation of the device. These points are discussed below in greater detail.

The GB barrier height ϕ_B under zero bias is caused by charge in the GB vicinity. Applied voltage is expected to change ϕ_B by two mechanisms*:

---

*In a high resistivity grain material, a large fraction of applied voltage may be dropped across the grain itself. This fraction depends on grain resistivity and current, which depends in turn on ϕ_B. In this discussion, we are considering only that fraction of applied voltage dropped across the GB, per GB.

i) ϕ_B on the forward biased side (negative polarity for n-type grains) will decrease, similar to the Schottky diode; ii) additional GB charge, and ϕ_B increase, can result from trapping in GB states of carriers injected across the barrier. These two mechanisms are compensating. If all GB states are occupied prior to biasing, then the bias voltage per GB is divided equally across the left and right sides of the space charge, and ϕ_B is expected to decrease as

$$\phi_B = \phi_{BO}\left(1 - \frac{qV}{4\phi_{BO}}\right)^2 \qquad (6)$$

where ϕ_{BO} is the un-biased barrier height. Thus, ϕ_B is expected to decrease immediately with voltage, arriving at a flat band ($\phi_B = 0$) condition when $V = 4\phi_{BO}/q$. If $\phi_{BO} \approx$ leV, this condition could occur when V ~ 4V per GB. That such a strong decrease is not seen for poly-Si and ZnO varistors (both of which have low resistance grains) indicates that the second above mechanism may also be present. In that case, empty GB states above E_F are occupied by electrons with increasing bias. This tends to increase ϕ_B, but is compensated by an increase in E_F, ϕ_B remaining essentially constant. This condition persists until all GB states are full, at which point we revert back to the previous case, and ϕ_B rapidly decreases with further applied voltage. This type of behavior is what is seen for poly-Si and the varistor, and also for the barrier layer (BL) and COG capacitors, as discussed below.

Then one must ask "How are the transport equations modelled according to this decrease in ϕ_B?" For a Schottky barrier (controlled either by thermionic emission or by diffusion) the I-V relation has the general form

$$I = I_o e^{-\phi_B/kT}\left(e^{qV/kT} - 1\right) \qquad (7)$$

where I_o is a constant and V is the voltage dropped across the barrier. There are other cases, described by different equations, that should also be considered. Some of these are: a) at low voltages, ohmic behavior is expected for most transport models; b) current may be controlled by hopping; c) at higher voltages, space charge limited currents (SCLC) may predominate. Even though these current types have different voltage dependences, they all commonly depend on a single activation energy, E_A:

$$I \propto e^{-BE_A/T} \tag{8}$$

where B = constant. E_A can be attributed to many mechanisms, including grain boundary potential (discussed above), hopping potential, band gap, impurity ionization energy, and Schottky barrier height (at a metal-ceramic interface). For the ohmic and SCLC cases, which apply to MLC capacitors, equation 8 arises from electron mobility. From thin film theory[5], effective mobility μ_{eff} can be expressed as

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_g} + \left(\frac{nk}{dA^*T}\right) e^{(\phi_B + \mathcal{E})/kT} \tag{9}$$

where μ_g = grain mobility

n = grain carrier density

A^* = Richardson constant

d = grain diameter

For large μ_g and/or large n, this becomes

$$\mu_{eff} \approx \frac{qd}{\sqrt{2\pi m^* kT}} e^{-\phi_B/kT} = \mu_o e^{-\phi_B/kT} \tag{10}$$

where m^* = carrier conductivity effective mass. A similar temperature dependence applies to hopping transport of polarons.[7]

Thus, it is known that current is controlled by GB for poly-Si, varistors, thermistors and BL capacitors. What can we say about MLC capacitors? To address this, we have measured current and activation energy versus voltage for COG and X7R capacitor types, with ZnO varistors and BL capacitors measured similarly for comparison. In order to set a frame for comparison, the varistor and BL measurements are presented first.

Results for a commercial ZnO varistor are shown in Figure 3. An ohmic current region exists below about 10 volts. This is followed by a strongly super-ohmic increase, which is accompanied by a strong decrease in activation energy. The current increase and E_A decrease have both been attributed to a voltage dependent GB barrier height.[2]

Similar characteristics for a BL capacitor* are seen in Figure 4. Three regions are evident on the I-V curve: 1) ohmic below about 2 volts; 2) sub-ohmic from about 2 to 10 volts; 3) super-ohmic above 10 volts. These regions are consistent with the voltage dependence E_A: constant below 10V and rapidly decreasing above. The low voltage ohmic regime is expected for most current mechanisms. The sub-ohmic region has been reported for poly-Si[1,8], although not for varistors or BL capacitors. Since grain boundaries of the Fig. 1a type can be viewed as back to back Schottky diodes, the sub-ohmic region represents the onset of current saturation. The super-ohmic region occurs due to the rapid decrease of E_A (and ϕ_B) above 10 volts.

---

*10nF, Taiyo-Yuden

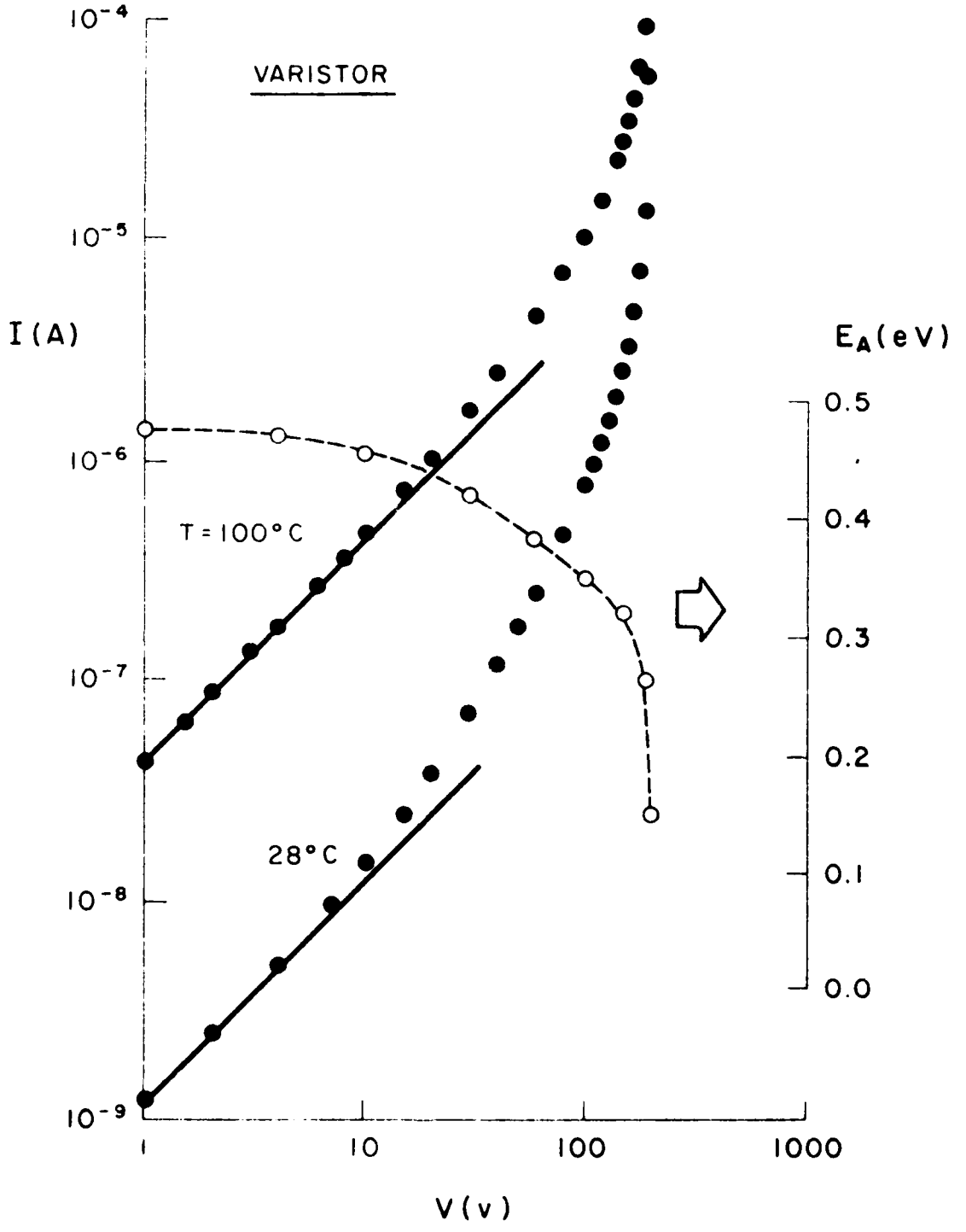


Figure 3. Current and activation energy versus voltage for commercial varistor.

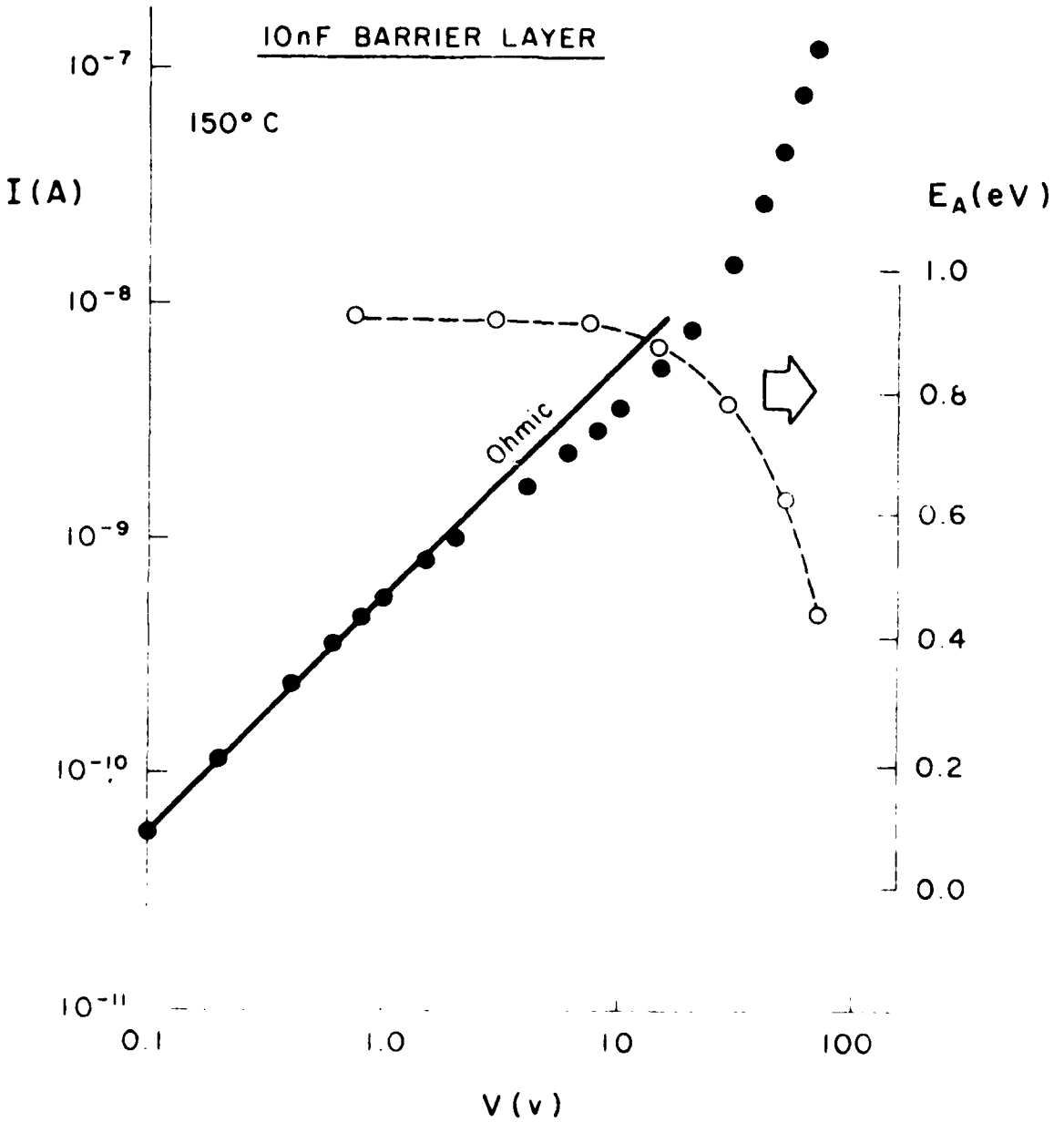


Figure 4. Current and activation energy for barrier layer capacitor.

As far as MLC capacitors are concerned, only COG and X7R types have thus far been measured. There is a striking difference between the voltage dependences of these devices. Characteristics for a commercial 0.69nF COG device are seen in Figure 5. The I-V behavior is unlike those seen for poly-Si, varistors or BL capacitors in that it consists of two distinct linear regions: a near ohmic region ($I \alpha V^{1.17}$) below 10V, and a super-ohmic one ($I \alpha V^{2.46}$) above.

The I-V curve linearity above 10V, and concavity of the E_A curve, distinguish the COG characteristics from those of the varistor and BL devices. This could be due in part to the following:

1) Voltage drop across the COG grains, which is not a factor for the BL or varistor devices. With increasing current, a smaller fraction of voltage is dropped across the GB in the super-ohmic region, since

$$V_{GB} = V \left(1 - \frac{IR_G}{V}\right) \tag{11}$$

where R_G is grain resistance and V is the total applied voltage per grain.

2) If the decrease of E_A is caused by GB trap filling, the nature of the decrease will depend on the energy distribution of the states. According to one model[9], an exponentially increasing state density in the band gap (as might be expected for a highly disordered material) should result in a barrier height voltage dependence of the form

$$\Phi_B = A - B \ln V \tag{12}$$

where A and B are material-dependent constants. This is the approximate form for the E_A curve for the COG, which above 10 volts, can be represented by the relation

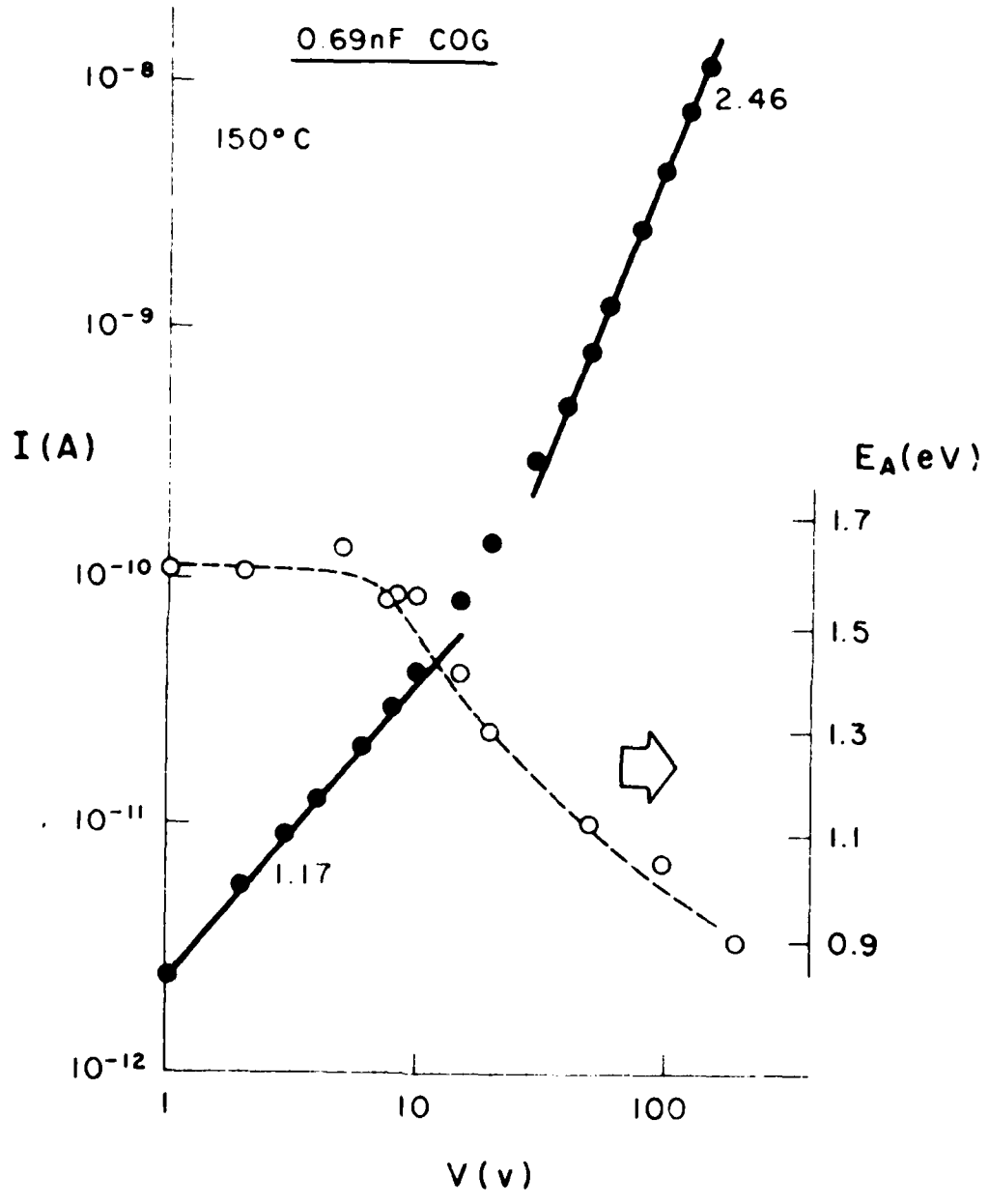


Figure 5. Current and activation energy versus voltage for commercial COG capacitor.

$$E_A = (1.95 - 0.195\ell nV)eV \qquad (13)$$

This relation resulted from a measurement of the equation $I = I_o e^{-E_A/kT}$ at different voltages, leading to $E_A(V)$. The parameter I_o is also strongly voltage dependent (moreso than the linear dependence on V expected in the ohmic region). This can be seen by substituting equation (13) for E_A, giving (at 150°C)

$$I = I_o\, e^{-\frac{1}{kT}(1.95 - 0.195\ell nV)} = B\, I_o\, V^{5.5} \qquad (14)$$

The experimental voltage dependence for the COG (above 10V) is $I \sim V^{2.5}$. Thus, I_o must decrease as V^{-3} in order for these relations to be internally consistent. The I_o values corresponding to the E_A curve of Fig. 5 above 10 volts do decrease with voltage, roughly to the power of -3 ± 0.5, which is in the expected range. Modelling the voltage dependence of I_o is more difficult than that of E_A, since each type of current will have a different form of I_o, whereas E_A may be common to several types (if E_A is due to GB barrier height, for example). The voltage dependence of I_o may yield information about current mechanisms, and will be investigated in greater detail in the future.

We have thus established that activation energies are strongly voltage dependent in the super-ohmic current regions for BL (as expected) and COG capacitors. Such is not the case for X7R capacitors from two manufacturers, or for non-electroded X7R chips from one of the same manufacturers. Activation energies are essentially constant over the entire voltage range.

Characteristics for a 1uF X7R are shown in Figure 6. The near 1.5 power law dependence above 10V is consistent with previous findings.[10] Activation energies do not depend strongly on voltage, even in the super-ohmic region.

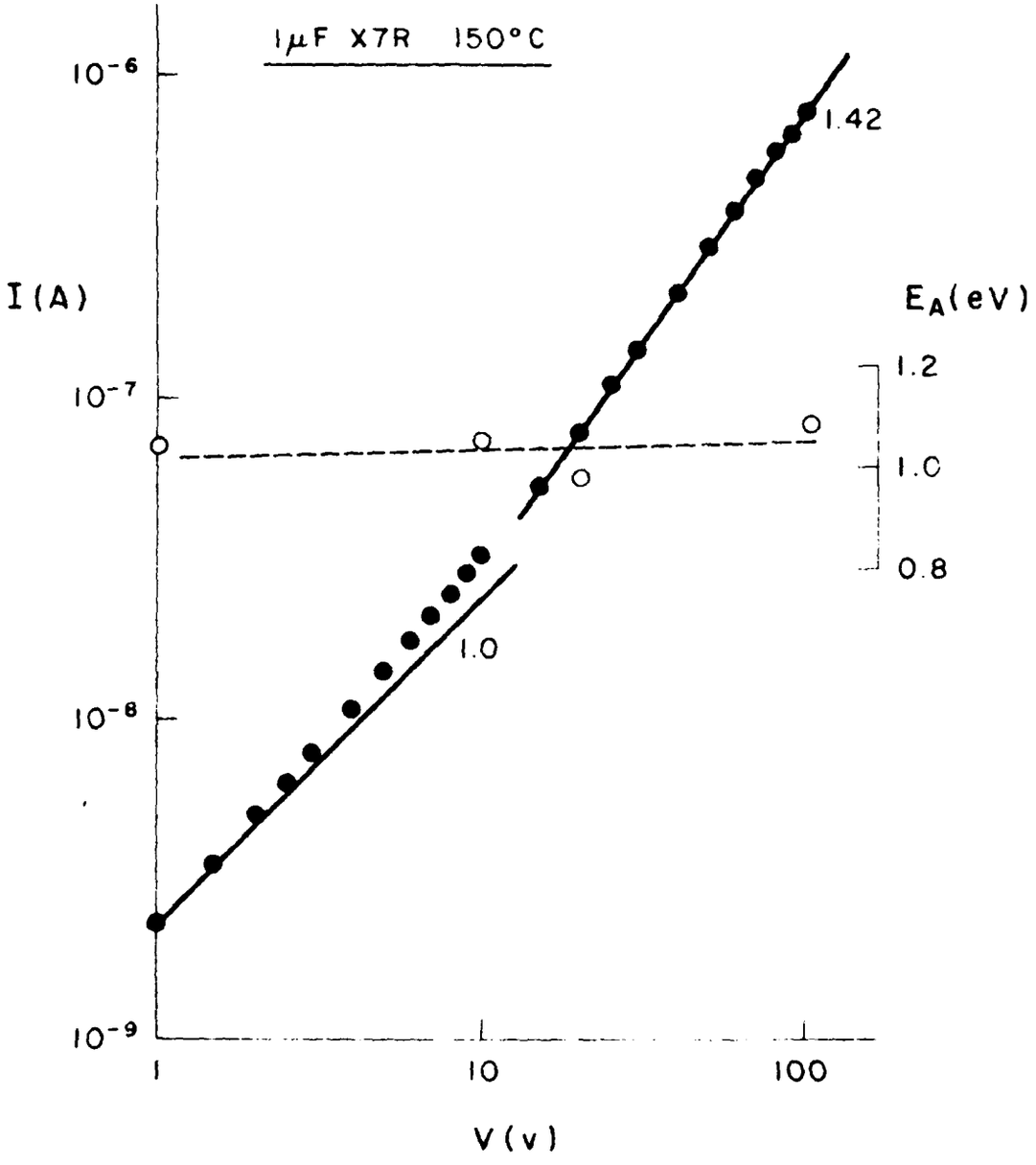


Figure 6. Current and activation energy versus voltage for commercial X7R capacitor.

Non-electroded chips of capacitor X7R material 2mm thick were also measured, using Pt/Au electrodes fired onto the surface. Both ohmic and SCLC currents are evident, the latter varying as $\sim V^2$ (when measured in argon), with a transition voltage of about 400V. (The SCLC characteristic depends strongly on the ambient, and is discussed in a later section.) Activation energies for the chip were found to be 1.33, 1.33 and 1.31eV at 10, 100 and 600 volts respectively.

The upper voltage region of the chip (400-1000V) corresponds to 10-25V for the capacitor (for equal electric fields), which fell within the range of measurements. Even though the chip currents have some variation in the upper voltage region caused by the ambient, their super-ohmic nature resembles that seen for the capacitor, and is dependent on the electrode-ceramic interface. Additional measurements related to this are discussed in a later section.

It is likely that the voltage dependence of E_A for the varistor and BL capacitor is due to the filling of energy states across the band gaps at grain boundaries. It is also possible that the E_A reduction for the COG type is caused by a similar mechanism, with the added condition that applied voltage is divided between grain bulk and boundary.

The question must be asked as to why the X7R activation energy is independent of voltage. There are several possible reasons for this. The larger dielectric constant would result in a reduced ϕ_B, since ϕ_B varies as $1/K$. The rather large activation energy (1-1.3eV) would then be due to other transport mechanisms, such as hopping. Another reason could be due to GB charge Q_p resulting from the discontinuity in spontaneous polarization across the GB. The Q_p would tend to compensate the charge trapped in GB states (Q_{GB}) at half of the GB area, thus removing the GB as an effective source of

impedance. (Such is the model for the $T < T_c$ regime of the $BaTiO_3$ thermistor.) Again, the activation energy would have to be due to other mechanisms. A third possibility is that the density of GB states is so large that they don't become exhausted over the range of applied voltage. A fourth possibility could be a higher resistivity region (i-layer) straddling the grain boundaries. This could tend to clamp the space charge region and ϕ_B, and has been discussed in greater detail elsewhere (see Appendix).

If the current is controlled by GB barriers (as it is for the varistor, PTC and poly-Si devices, and possibly is for MLC devices), then the maintainance of that barrier is critical for a stable device. For the simplest GB barrier considered (Fig. 1a), with ϕ_B given by eqn. 1, degradation can occur by two mechanisms (assuming ϵ remains constant). GB change can be brought about by heating in a reducing ambient (H_2, CO, NH_3, etc.), and by ionic segregation at the GB. N_{GB} and ϕ_B are thus reduced. A second mechanism is increased donor density N_D.

The main goal of this section is to raise the possibility, with some supporting data, that GB barriers may be important with respect to insulation resistance for some types of MLC devices. BL and COG types have E_A voltage dependences that resemble those of known GB controlled devices; the X7R does not. The latter point has been addressed; the reduction of the X7R E_A with time under stress will be discussed in the following section. Before leaving this section, the question should be asked: What other sources of E_A (and ϕ_B) can exist in MLC devices other than GB barriers? The conditions are that a) E_A values lie roughly in the 0.7 to 1.3eV range for a new device; b) E_A decreases with voltage for some devices (BL and COG) but not

for others (X7R - for the devices we have measured); c) E_A of the X7R decreases with time, under voltage and temperature stress. Two mechanisms are listed below.

1. Schottky type of barrier lowering,

$$\Delta\phi_B = \left(\frac{qE}{4\pi\varepsilon}\right)^{1/2} \tag{15}$$

Assuming $E = 10^5$ v/cm and $\varepsilon = 10^{-11}$ F/cm (COG), barrier height reduction is only 0.01eV, whereas the actual ϕ_B decreased from about 1.6 to 0.9eV ($\Delta\phi_B = 0.7$eV). Schottky lowering would be even less for a higher K material. This also applies to the Poole-Frenkel effect in the bulk.

2. If the charge carrier concentration is large enough, potentials may be screened. Consider the potential in the vicinity of an electron trapped in a neutral region. For low charge carrier concentration, let the ionization energy of that electron be E_i (this could also be a deep donor level.) As carrier concentration increases, E_i is reduced due to screening, by an amount

$$\Delta E_i = \frac{q^2}{4\pi\varepsilon\lambda} \tag{17}$$

where λ is the Debye length. For non-degenerate statistics, λ is given by

$$\lambda = \sqrt{\frac{\varepsilon k T}{2q^2 n}} \tag{18}$$

For $\varepsilon = 100\varepsilon_o$ and T = 300K, this relation becomes

$$\Delta E_i = \frac{900}{\sqrt{n}} \text{ eV}$$

For $n = 10^{18}$ cm^{-3}, $\lambda = 90\text{Å}$, and the resulting E_i decrease is only 0.0015eV, which is negligible. It is thus difficult to see how screening could be a significant factor, especially for high K materials, as the device degrades, and carrier concentration increases. This discussion also applies to polaron hopping potentials.

2.2 DEGRADATION OF ACTIVATION ENERGY

We have reported, for a large number of degraded X7R devices, that there is a monotonic decrease in activation energy with the degree of degradation (device resistivity at 125°C).[10] Subsequent thermoelectric studies on similar but non-electroded X7R chips indicated that E_A decrease could be attributed largely to mobility, even though mobility and carrier concentration both increase.

It was desired to observe this E_A decrease as leakage current increases for a single device. Several 10nF X7R capacitors were aged at 150°C and 4 times rated voltage (400V) in air, over a period of 9 weeks. I-V curves (at 150°, from 1 to 100V) and E_A values (at 5V, from 150 to 130°C)were measured periodically.

Leakage current increase with time at 5V bias is shown in Figure 7. The increase is roughly exponential.

A group of I-V curves are shown in Figure 8. A trend similar to that reported earlier[11], for the set of degraded X7R devices, is evident: as degradation proceeds, the slope of the I-V curve increases. In Fig. 8, this increase is from about 1.25 to 1.65. (The curve would eventually become ohmic if the test had proceeded further; this was not done for lack of time.)

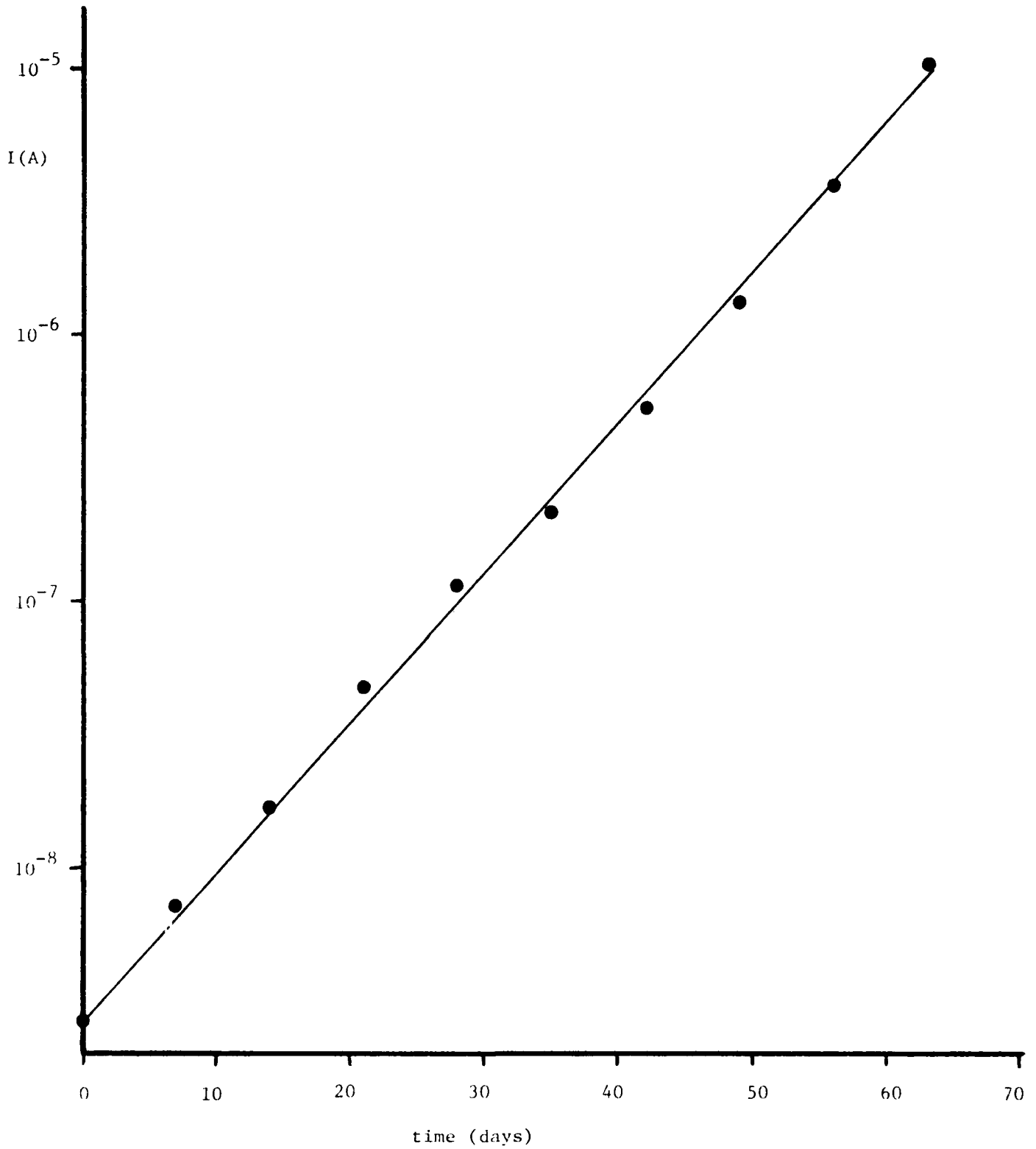


Figure 7. Leakage current versus time for 10nF X7R device (stressed at 150°, 400V; this measurement at 130°, 5V).

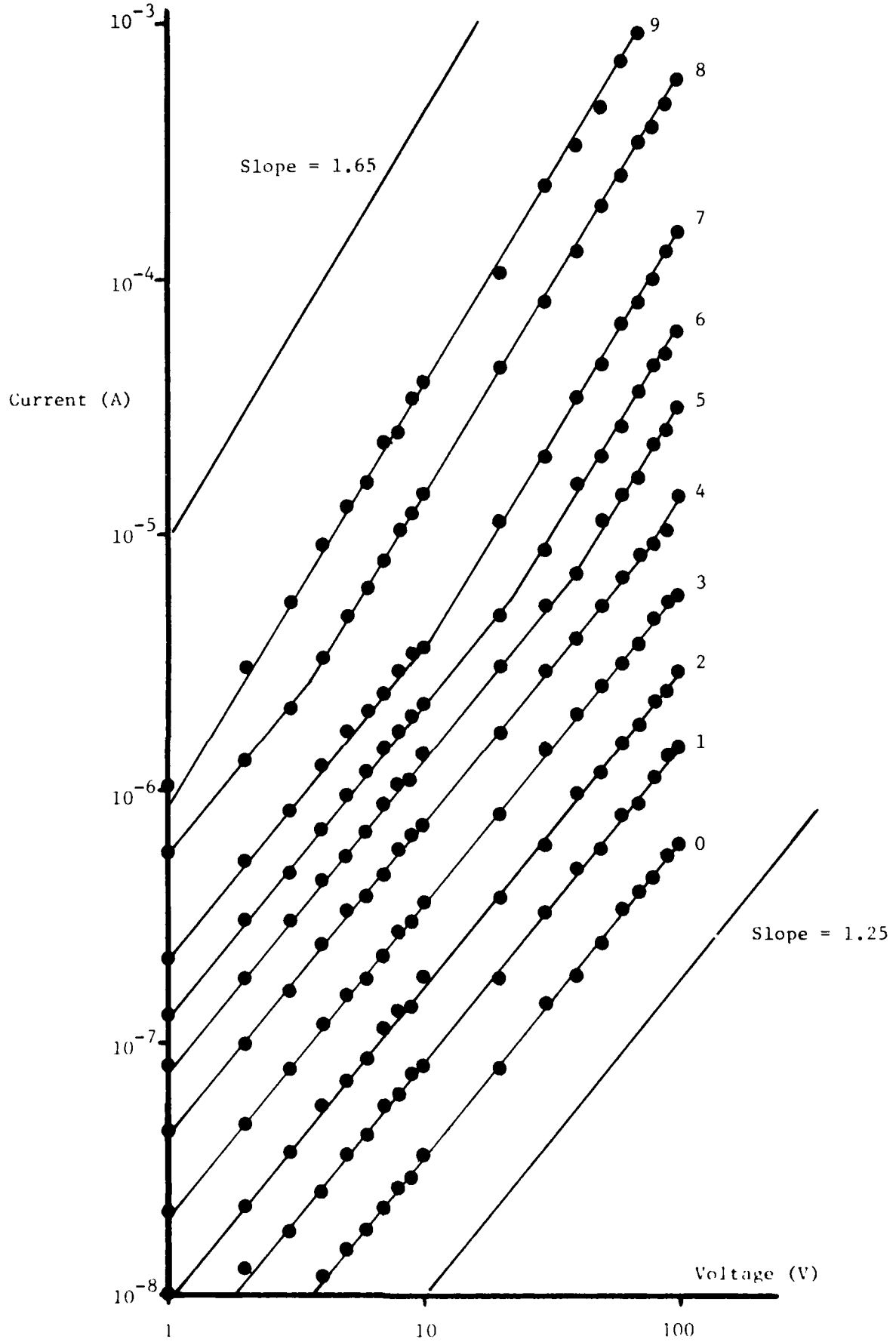


Figure 8. I-V curves for degrading X7R device (stressed at 400V, 150°C) Aging time in weeks indicated on right.

As leakage current increased with time, E_A decreased. This is shown in Figure 9. The linear decrease of E_A is somewhat striking, with E_A decreasing from an initial value 1.28eV to a final value of 0.14eV. The linear decrease in E_A is consistent with the exponential increase in current (Fig. 7 and equation 8).

A general model can't be proposed from the characteristics of a single device. However, some comments should still be made about the decrease of E_A with time seen in Fig. 9 (and the resulting near-exponential increase in current.) If E_A is GB controlled, its decrease could be related to some of the mechanisms mentioned earlier (decrease in N_{GB}, increase in N_D). For example, the total number of ions arriving at (or leaving) a GB could be a linear function of time, over a limited time interval. Processes such as oxygen ion and vacancy migration, and barium migration, could be factors.

2.3 SCLC IN NON-ELECTRODED CHIPS

We previously reported thermoelectric measurements made on non-electroded chips of X7R material.[11] We have made additional measurements on similar chips* for comparison to capacitors of the same material. Measurements on both the non-electroded chips and electroded chips (i.e. MLC capacitors) are reported below.

Current-voltage behavior was studied using a 3-electrode guard ring geometry. Chip dimensions are 6.21 x 5.30 x 2.18 mm, and Au/Pt electrodes were fired onto the broad faces. I-V measurements were made from 10 to 1000V,

*Supplied by Corning Electronics, Raleigh, NC

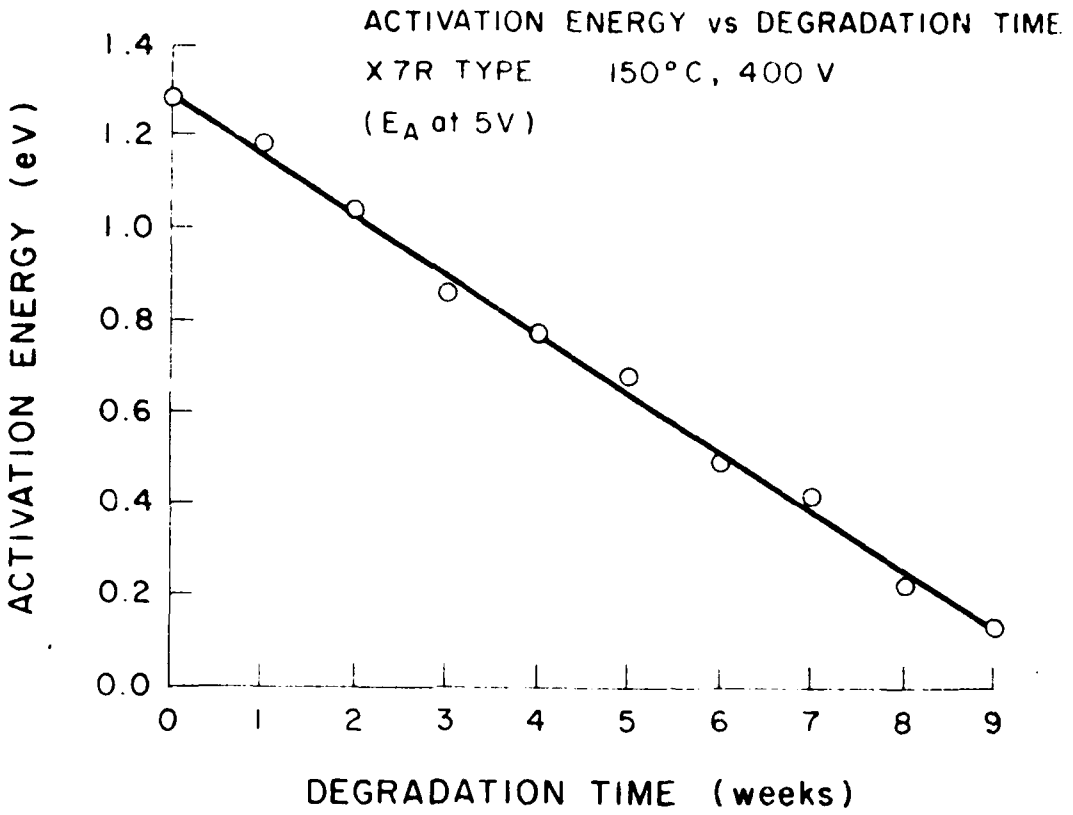


Figure 9. Decrease in activation energy for X7R capacitor with degradation time.

at temperatures from 200 to 350°C, in argon and air ambients.

The major points from these measurements are summarized below. (See Figure 10)

1. There are two distinct regions of different voltage behavior: an ohmic region below about 400V, and a super-ohmic region above 400V.

2. The upper characteristic depends on the ambient; currents increase as $\simeq V^{1.9-2.1}$ in argon, and as $V^{1.3-1.7}$ in air. The ohmic region is independent of ambient.

3. Activation energies are (1.31 ± 0.02)eV, and independent of voltage.

We attribute the upper voltage region to space charge limited currents (SCLC). In a model reported earlier[10,11], the near 3/2-power law voltage dependence was attributed to SCLC emitted from electrode asperities. We proposed there that, as the ceramic in the electrode vicinity degrades, a higher power law should evolve, as the increased ceramic conductivity results in a more nearly planar effective electrode.

The upper voltage regions ($V > 400V$) of Fig. 10 are consistent with a model whereby current injection depends on metal-ceramic interface properties. In these measurements, this interface is exposed to the ambient (through the Au/Pt electrode, which is oxygen permeable). According to the above model, the I-V slope should increase if the near-electrode ceramic becomes oxygen deficient. Such slope increases do occur, without exception, in argon, with the air ambient always resulting in the lower slope.

The time dependence of leakage currents, in air and argon ambients, are shown in Figure 11, for two sets of electrodes (A-C and A-B, as shown in Figure 12) at 10V (ohmic) and 600V (SCLC).

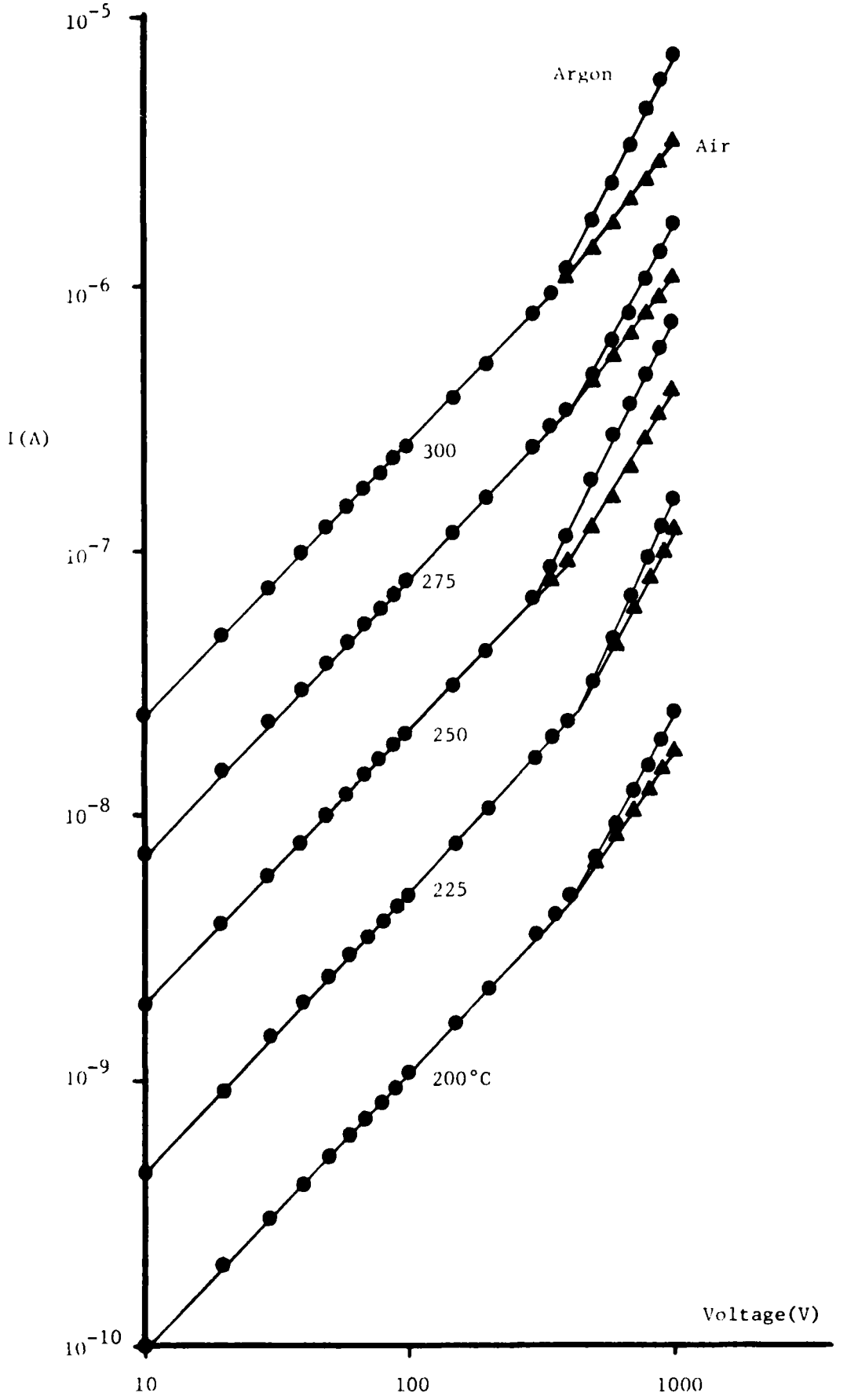


Figure 10. I-V curves for 2mm thick chips at 5 temperatures, in argon and air ambients.

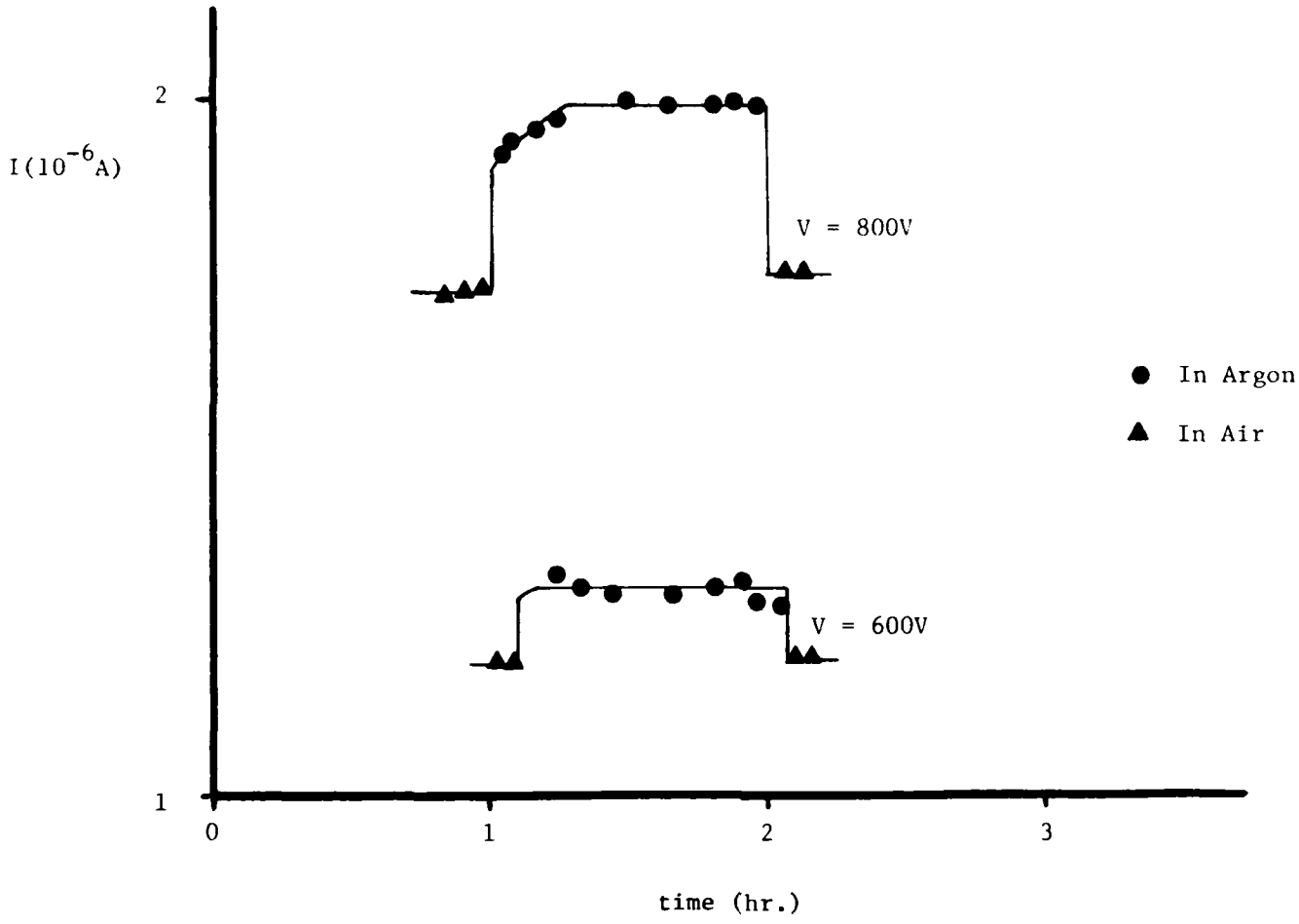


Figure 11. Increase in leakage current in argon ambient (T = 300°C), for electrode configuration A-C. No change in current occured for the A-B hookup.

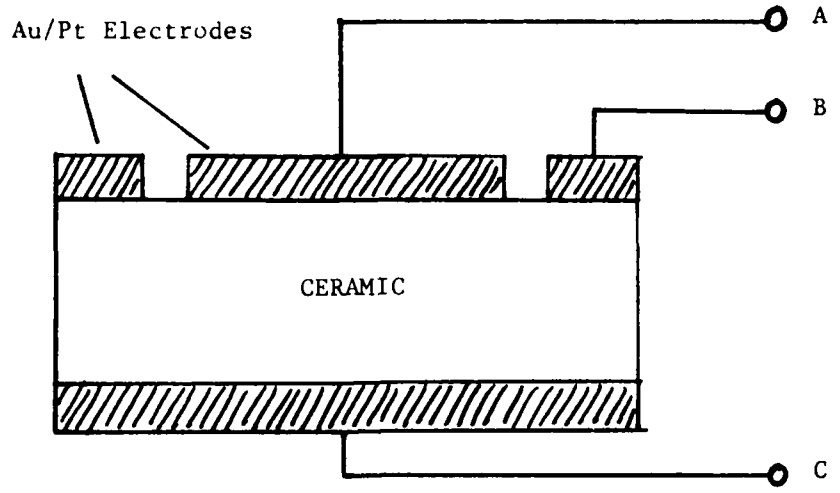


Figure 12. Guard ring electrode configuration

The only case where current is affected by the inert ambient is A-C at 600V.

If oxygen is leaving the ceramic when measured in argon, only a very thin region (< 1μm) has to be affected. That only a thin layer (or even just the interface, or the metal itself) is involved is substantiated by two facts:

1. No change in current occurs in the ohmic region, therefore the ambient sensitive part is a negligible fraction of the total thickness.

2. No change in the resistance between the central electrode and the guard ring (A-B hookup) was evident.

This latter result is somewhat surprising, since even though a thin low resistance layer may not show up in the bulk resistance, you could expect to see a detectable change in surface resistance. Since none was seen, it must be proposed that the current increase seen above 400 volts could also

be due to an oxygen deficient interface, or even the electrode itself, with no change occuring in the ceramic (outside of 20Å or so from the interface).

It seems clear, though, that the high voltage increase is due to an injection mechanism that depends on the interfacial and/or near-interfacial region.[12]

In order to check the validity of the SCLC model in the upper voltage region, a chip was polished to a thickness of 0.57 mm, and guard ring electrodes attached in the same manner as for the 2 mm chips. An I-V characteristic for such a thinner chip is shown in Figure 13, measured in air and argon ambients.

Current for the thinner sample increases by a factor of ≈ 5, which is expected since it has a slightly larger electrode. However, the ohmic to SCLC transition voltage V_T only decreases to 250V (from ~ 400V). For SCLC with planar electrodes, V_T should increase as d^2. For this case, the thinner sample should thus have a V_T of ≈ 25V. However, it is known that the electrode-ceramic interface is not planar. This is seen in Fig. 14, where the surfaces of as received and polished chips are shown. Some roughness is seen on both, in varying degrees. According to SCLC theory[13], the main condition for a $V^{3/2}$ power relation is that the anode radius r_a be much larger than that of the emitting cathode (r_c). An I-V relation of the form $I = KV^{3/2}$ could be expected in both cases, with K depending on the concentration of traps in the band gap, but independent of both r_a and r_c, provided that $r_a \gg r_c$. Thus, it is not expected that V_T would decrease as rapidly with sample thickness as for the planar electrode case. Additional samples polished to varying thicknesses are being measured in order to clarify these points.

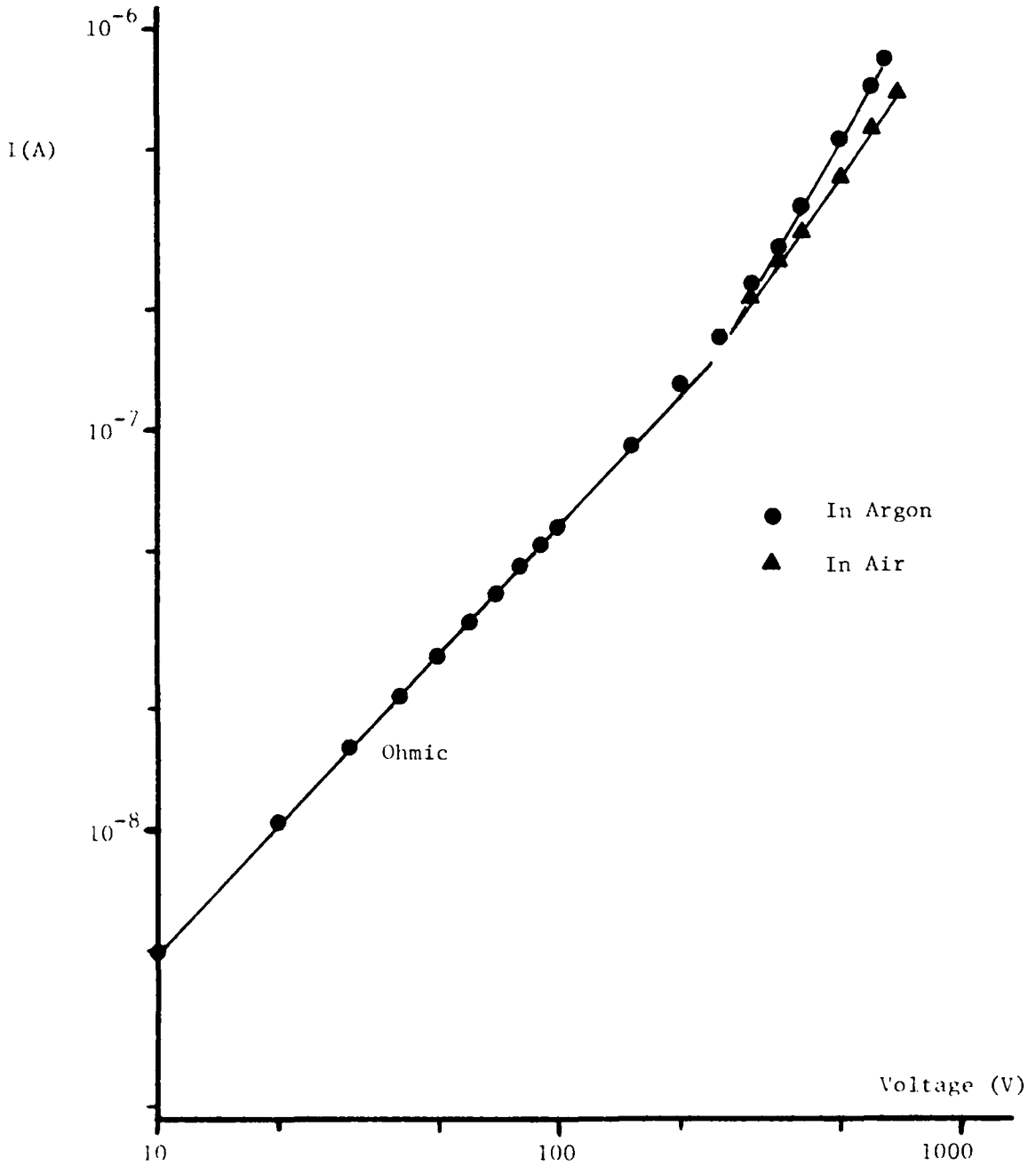
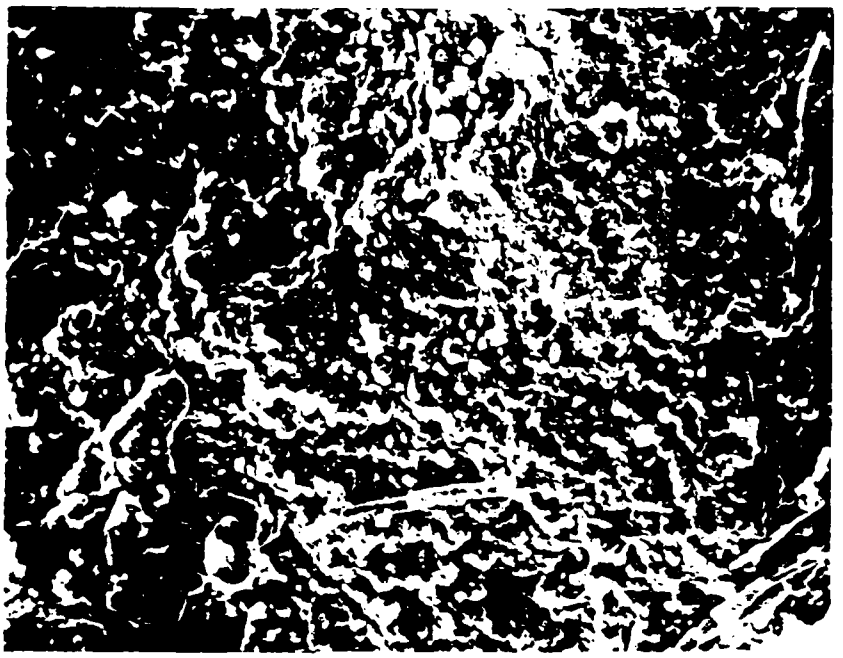


Figure 13. I-V curves for 0.57mm thick chip (250°c).



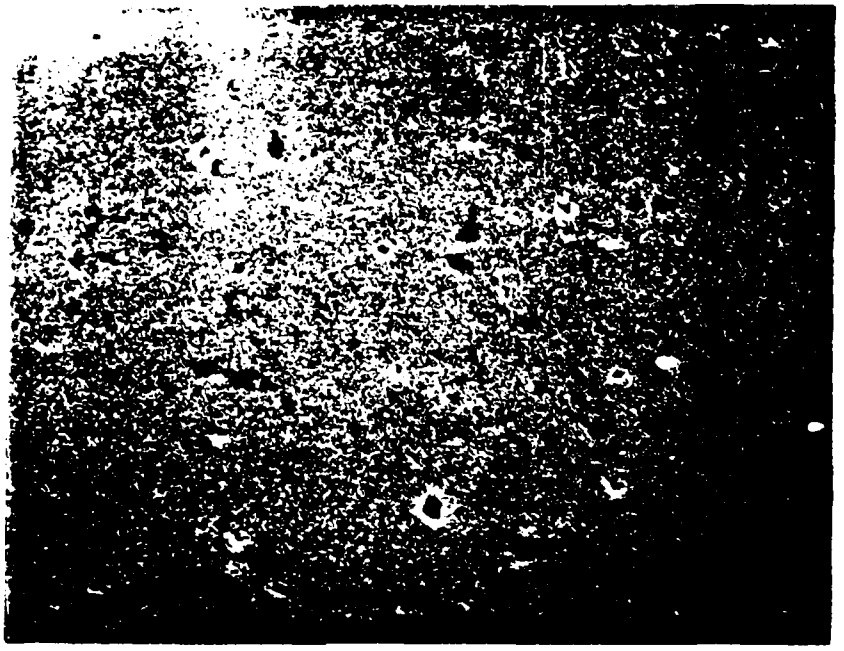


Figure 14. SEM pictures of as-received (upper) and polished (lower) X7R chip surfaces. The polished surface is not smooth, due to lift-out and pores. (2,000X).

I-V characteristics for an MLC X7R capacitor chip made from the same type of ceramic sheets as the non-electroded chips are shown in Figure 15. (These measurements were not extended below 10V due to the long settling times for the currents.) The near 3/2 slope of these curves is as reported elsewhere for non-degraded X7R devices. The curves are similar when measured in air or argon because the device is buried in ceramic, thus protecting the interface. The 3/2 slope is not inconsistent with the upper voltage regions of Figure 10. The transition to ohmic behavior is not evident in Figure 15. From Figure 6, for an X7R made by another manufacturer, this transition appears at about 1-2 volts.

There is another important correlation between the X7R chips and capacitors. The 1.25-1.5 power dependence seen for new capacitors (Figures 6, 8, and 15) corresponds to the lower SCLC curves seen for the chips (Fig. 10). The power dependence increases (to $\simeq 2 \pm 0.1$) for moderately degraded X7R capacitors (which we have attributed to a "smoothing" of the electrodes[11]). This corresponds to the upper SCLC curve of Fig. 10, for the chips, which we have attributed in this report to interface effects.

It thus appears that an MLC capacitor of the type shown in Figure 6 operates in an SCLC regime, when biased above roughly 1 volt. However, the baseline current level is still governed by ohmic current, or the $n\mu$ product. As this increases, so does the SCLC. And μ may be determined largely by the grain boundary potential ϕ_B.

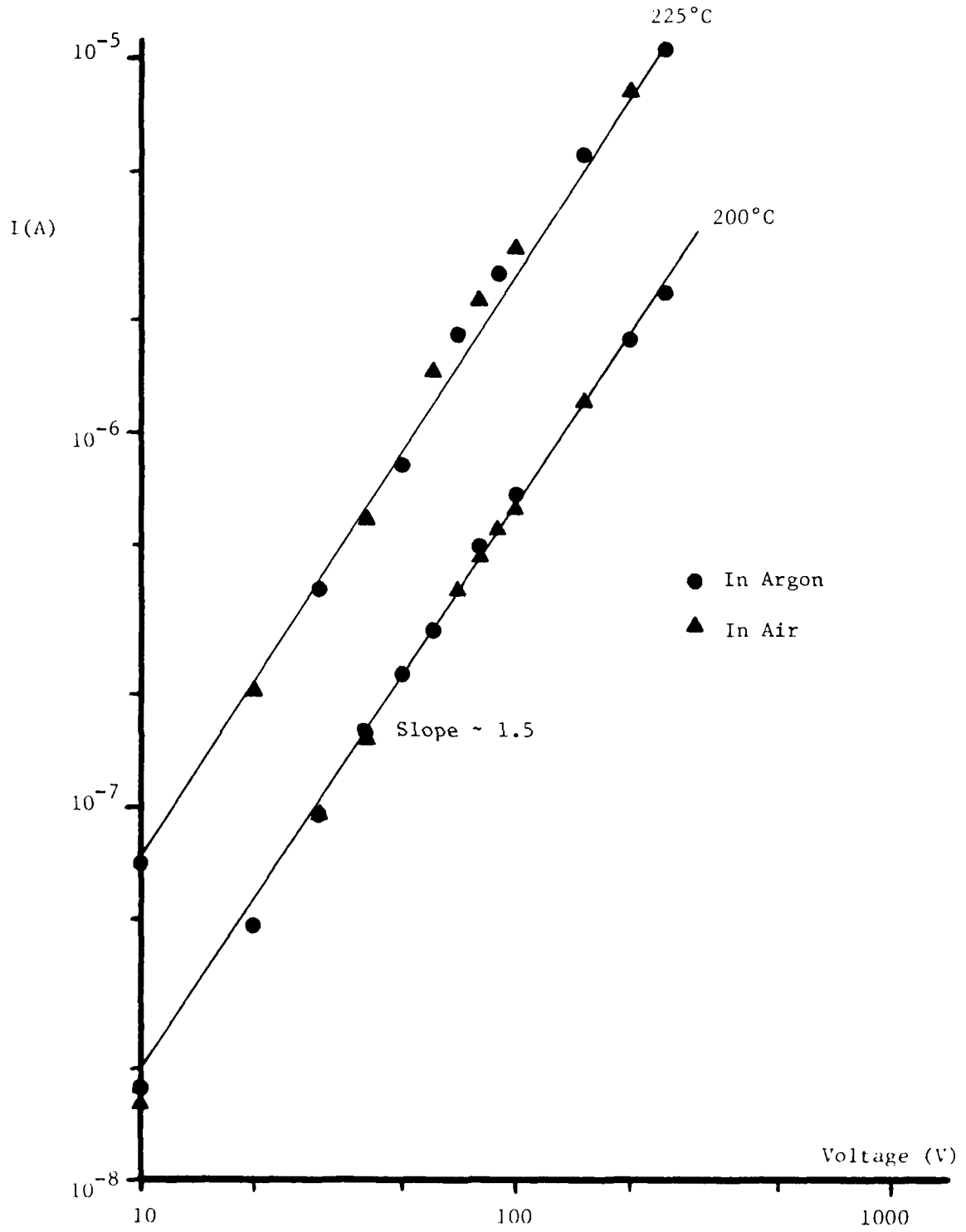


Figure 15. I-V characteristics for 100nF X7R capacitor chips at 200 and 225°C, in argon and air ambients.

2.4 EVIDENCE OF IONIC MOVEMENT DURING DEGRADATION

Some interesting characteristics have been observed during 1μF Z5U capacitor accelerated degradation. We show these results to illustrate evidence of ionic movement during degradation, and to indicate the variability of characteristics for devices of the same type from two different manufacturers.

When tested at 200V (4 times rated voltage) at 150°C, devices from one manufacturer always proceeded to rapid failure, whereas devices from another manufacturer actually improved. This is illustrated in Figure 16. It was found that the degradation process for the poorer class of capacitors could be reversed by changing voltage polarity, but that failure eventually occurred if maintained in any polarity long enough, as indicated in Figure 16. This reversal of degradation can be maintained over at least several cycles of polarity reversal, as shown in Figure 17. The leakage current minimum increases slightly each cycle, so the process is not totally reversible.

The degradation process under these conditions also exhibits a near exponential time dependence, as shown earlier for an X7R. The activation energy for the degrading Z5U was also found to decrease linearly with time, as was the case for the X7R.

An interesting aspect of these measurements is the cyclic changes seen in Figs. 16 and 17. This is probably caused by a low resistivity front spreading across the layer, somewhat like that originally reported by Lehovec and Shirn for point contacts.[14] If it spreads to the anode, the device fails. The front motion can be reversed by changing polarity, but failure will occur either way because the process is the same. Such a polarity and time dependent phenomena is indicative of large scale ionic

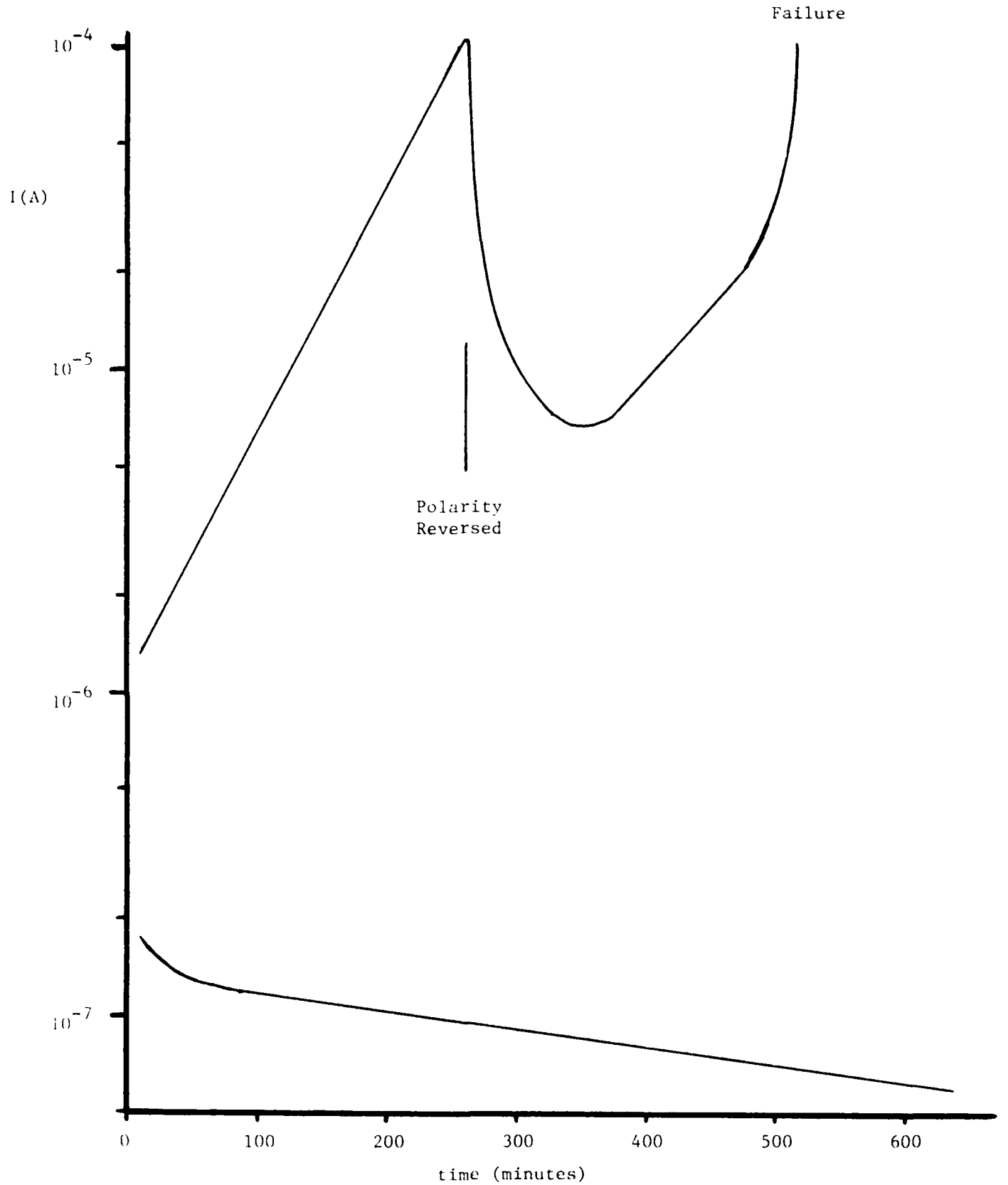


Figure 16. Current versus time for 1μF, 50V, Z5U devices from two manufactures (measured at 200V, 150°C.)

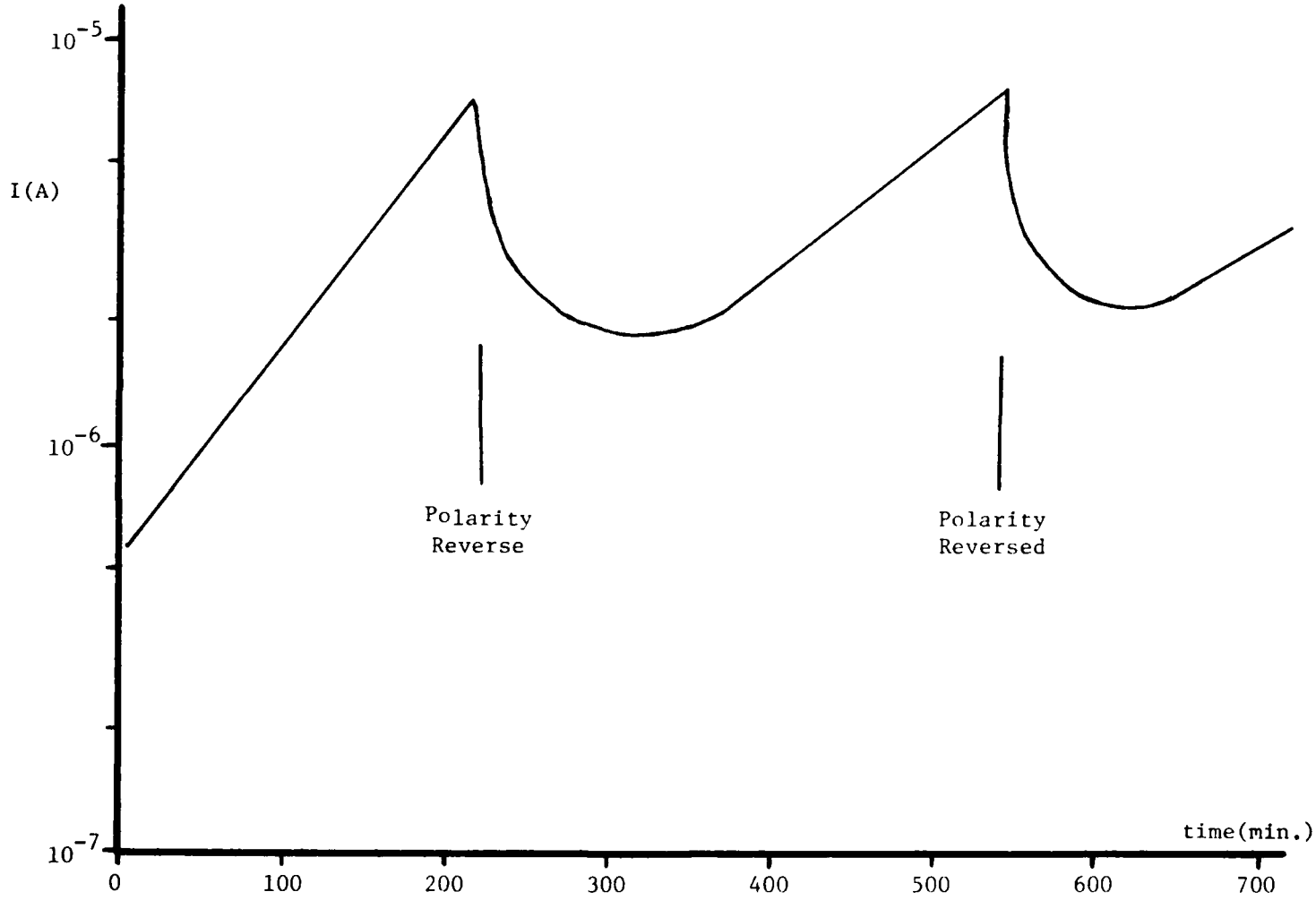


Figure 17. Degradation leakage current for 1μF Z5U showing polarity reversal effect, which prevents failure. (100V, 150°C)

movement, probably $O^{=}$. This is consistent with results we previously reported, for a similar type of device from the same manufacturer, whereby a color gradient was evident across the layers of a cross-sectioned degraded capacitor.[11]

3. CONCLUSIONS

From the work performed over the past year, we have concluded the following:

a) Grain boundaries may play a dominant role in the resistance of some types of MLC devices.

b) Two distinct current regions were seen for non-electroded X7R chips; the upper region is attributed to space charge limited current and depends on the ambient.

c) No ohmic region is evident for X7R capacitors above 1 volt because SCLC dominates in the thinner layers.

d) Leakage current polarity reversal effects are due to the movement of an ionic front across the layer.

4. FUTURE WORK

Future work will include the following:

a) To continue to clarify the role of grain boundaries by more extensive measurements on MLC devices, with comparison to known grain boundary controlled devices;

b) Further studies on polished non-electroded X7R chips, to determine the importance of two parameters: i) degree of surface roughness (related to electrode interface), and ii) sample thickness (to assist in modelling the space charge current).

c) A galvanic cell will be setup to distinguish ionic and electronic transport numbers for X7R capacitor ceramic (to be supplied by Corning Electronics).

d) Transport measurements on ceramic samples of varying types of porosity (to be supplied by Lehigh University).

e) Measurements and modelling for PLZT layers of different thickness (to be supplied by Sprague Electric).

REFERENCES

[1] G. E. Pike and C. H. Seager, "The DC Voltage Dependence of Semiconductor Grain-Boundary Resistance," J. Appl. Phys. 50, 3414 (1979).

[2] G. D. Mahan, L. M. Levinson and H. R. Phillip, "Theory of Conduction in ZnO Varistors", J. Appl. Phys. 50, 2799 (1979).

[3] G. H. Jonker, "Equilibrium Barriers in PTC Thermistors", from Grain Boundary Phenomena in Electronic Ceramics (L. M. Levinson, Ed.), American Ceramic Society, 1982 (p. 155).

[4] H. D. Park and D. A. Payne, "Characterization of Internal Boundary Layer Capacitors", ibid, p. 242.

[5] L. L. Kazmerski (Ed.), Polycrystalline and Amorphous Thin Films and Devices, Academic (1980).

[6] K. Sata et al, "Electrical Conduction of ZnO Varistors under Continuous DC stress", Jap. J. Appl. Phys. 19, 909 (1980).

[7] P. Nagels, "Experimental Hall Effect Data for a Small-Polaron Semiconductor", in The Hall Effect and Its Applications, C. L. Chien and R. Westgate, Eds, Plenum Press (1980).

[8] C. H. Seager and G. E. Pike, "Grain Boundary States and Varistor Behavior in Silicon Bicrystals", Appl. Phys. Lett. 35, 709 (1979).

[9] J. D. Levine, "Theory of Varistor Electronic Properties", CRC Critical Reviews in Solid State Sciences, p. 597 (1975).

[10] L. C. Burton et al, "Leakage Currents in Multilayer Ceramic Capacitors", IEEE CHMT Transactions, CHMT-7, 443 (1984).

[11] Annual Progress Report, "Intrinsic Mechanisms of Multilayer Ceramic Capacitor Failure", ONR Contract N00014-83-K-0168, Virginia Polytechnic Institute (1984).

[12] R. T. Thomas, "Time Dependence of the Electrical Conductivity of $BaTiO_3$ Single Crystals Heated in Oxygen", J. Phys. D: Appl. Phys. 3, 1434 (1970).

[13] M. A. Lampert and P. Mark, Current Injection in Solids, Academic (1970).

[14] K. Lehovec and G. A. Shirn, J. Appl. Phys. 33, 2036 (1962).

APPENDIX

Paper to be presented at the 35th Electronic Components Conference, Washington, DC, May 20, 1985.

VOLTAGE DEPENDENCE OF ACTIVATION ENERGY FOR MULTILAYER CERAMIC CAPCITORS

by

Larry C. Burton
Departments of Electrical Engineering and Materials Engineering
Virginia Polytechnic Institute and State University
Blacksburg, VA 24061

Abstract

Current-voltage and activation energy measurements can be used to probe grain boundary potentials. A common type of activation energy for current conduction in a polycrystalline material is that due to the grain boundary potential energy barrier. The height of this barrier depends on occupation of grain boundary energy states. Its decrease with applied voltage accounts for the current breakdown characteristics of polycrystalline silicon, and of ZnO varistors. Barrier layer and COG capacitor types exhibit strongly voltage dependent activation energies, which can account for their super-ohmic current-voltage behavior. Activation energies are essentially independent of voltage for X7R capacitors and ceramic, even in super-ohmic regions. This may be accounted for by several mechanisms. A reduction of the grain boundary barrier can result in leakage current increase and device failure.

Introduction

For multilayer ceramic (MLC) capacitors, activation energy pertains to the temperature dependence of leakage current, and may be ascribed to carrier generation and/or transport mechanisms. Grain boundaries (GB) can play a dominant role in activation energy and leakage current. GB potential barriers (specified by a barrier height energy) can be the dominant impedance to both electron and hole flow. This can be the case for any polycrystalline material, including thin films[1], barrier layer (BL) capacitors[2], polycrystalline silicon[2-5], and ceramic varistors[2,6,7] and thermistors[4,8]. Thermal activation energies for these devices can be attributed exclusively to transmission across GB potential.

The signature of GB controlled transmission is a voltage dependent activation energy. We have ascertained that certain types of commercial MLC capacitor activation energies decrease with voltage. GB barrier height and its dependence on voltage are reviewed below. Measurements were made on varistors, boundary layer, COG and X7R capacitors. These results are related to the resistance and stability of MLC capacitors.

GRAIN BOUNDARY CONTROLLED TRANSPORT

For a polycrystalline material, grain boundaries can control electron transport and current activation energy. The latter is determined by the GB barrier height, which can be voltage dependent.

Three GB types are shown in Figure 1 for n-type material. (Similar diagrams pertain to p-type material, only band-bending is in the downward direction.)

Figure 1a shows a GB with energy states (of density N_{GB}) occupied up to the Fermi energy E_F. ϕ_{BO} is the GB barrier height under zero bias conditions, and X_1 and X_2 are the space charge widths ($X_1 = X_2$ under zero bias). If thermal activation energy E_A is due solely to the GB potential barrier, the two are related by

$$E_A(V = 0) = \phi_{BO} - \Delta T \qquad (1)$$

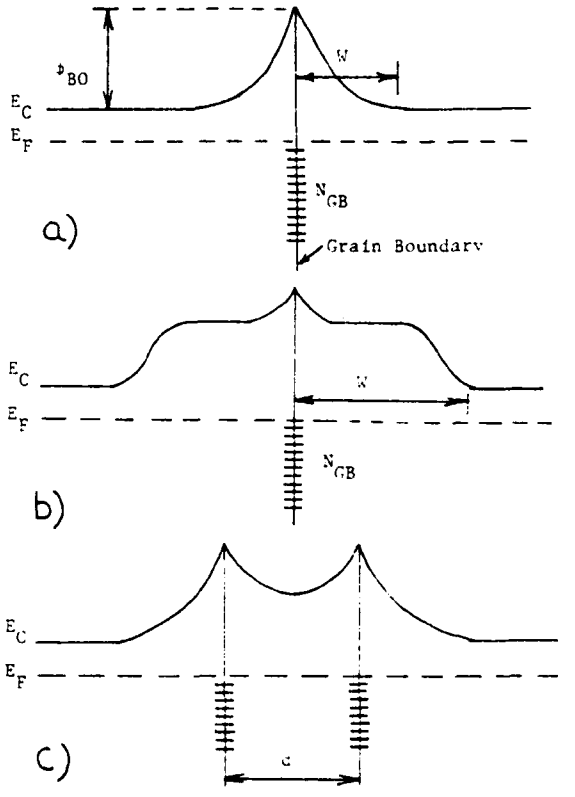


Figure 1. Grain boundary potential energy diagrams for three cases: a) thin boundary region with uniform donor density in the grains; b) higher resistivity region (i-layer) adjacent to GB; c) layer of second material separaring the grains.

where ΔT is a temperature correction, with α being negative and in the range -10^{-4} to -10^{-3} eV/K. The zero bias barrier height is thus somewhat less (several tenths of an eV) than the measured activation energy.

At voltage V (per grain boundary), we can likewise say

$$\phi_B(V) = E_A(V) + \Delta T \qquad (2)$$

The zero voltage barrier height is given by

$$\phi_{BO} = \frac{q^2 N_D^2}{2\epsilon} \qquad (3)$$

where N_D, ϵ and X are donor density, permittivity and space charge width, respectively. For charge neutrality, $qN_D X = qN_{GB}/2$ where N_{GB} is the filled grain boundary state density (here assumed uniform). Thus, ϕ_{BO} can be written

$$\phi_{BO} = \frac{q^2 N_{GB}^2}{8\epsilon N_D} \qquad (4)$$

ϕ_{BO} thus depends on one GB parameter (N_{GB}) and two grain parameters (χ and N_D). This type of grain boundary pertains to the poly-Si and $BaTiO_3$ based thermistor.

The barrier of Fig. 1b is similar to that of 1a except that there is a higher resistance region (intrinsic, or i-layer) near the GB. One consequence of the i-layer is that space charge width may be clamped at a nearly constant value, independent of voltage. This type will be discussed further in the context of X7R measurements.

In Figure 1c, a thin layer of second material exists between the grains. (This can be a 2nd phase or a different material.) Charge induced in this material depends on interface states, resistivity and energy band parameters. This structure pertains to the BL capacitor, and for small interlayer thickness, to the ZnO varistor.

Figure 2 shows a GB when under voltage bias. (This GB could be one of several existing in series across an MLC capacitor layer. Voltage drop across the bulk of the grain is neglected.)

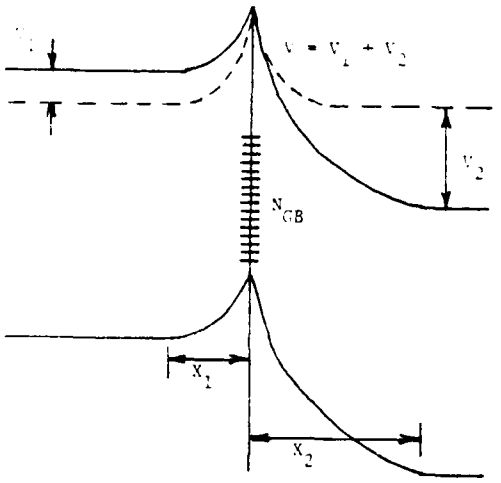


Figure 2. Voltage V across a GB. $V=V_1+V_2$, and x_1 and x_2 are space charge widths on the two sides. Unbiased conduction band edge is shown as dashed lines.

We are concerned with the GB barrier height ϕ_B and how it is effected by GB state filling and applied voltage. The specific mode of current is not of prime concern (i.e. ohmic, thermionic, Schottky etc.) since all types will be effected by ϕ_B similarly.

Zero bias barrier height ϕ_{BO} (Fig. 1a) exists because of negative charge trapped at the GB, and equal positive charge induced in adjacent depleted regions. The voltage dependence of ϕ_B (Figure 2) will depend on availability of additional GB states which can trap electrons when a voltage is applied. With regard to GB state occupation, two cases are of interest.

Case 1 - All States Occupied

In this case all GB states are filled prior to application of a voltage, and no electrons travelling across the GB as a result of bias are trapped. The bias increases x_2, and therefore x_1 must decrease so that total positive charge remains constant. Thus, x_1 decreases with voltage as[7]

$$x_1 = x_{10}\,(1 - qV/4\phi_{BO}) \qquad (5)$$

and barrier height decreases as

$$\phi_B = \phi_{BO}\,(1 - qV/4\phi_{BO})^2 \qquad (6)$$

where V is voltage across the GB. When $V=4\phi_{BO}/q$, $x_1=0$, the flat band condition is obtained, and the barrier height to electron flow from the left is zero. A rapid increase in current is expected at this point, limited only by bulk grain and contact resistance.

Case 2 - Empty States Above E_F

In this case there are empty states in the band gap above the Fermi energy E_F which are available for electron occupation. When such occupation occurs under bias, E_F moves up due to the increased electron concentration in the GB, and ϕ_B is therefore reduced by the same amount (neglecting the small voltage drop V_1 on the left hand side of the boundary.)* Almost the entire voltage V is on the right side of the junction, both x_1 and the positive space charge increase, and x_1 is essentially clamped. If the density of grain boundary states near E_F is large, ΔE_F will be small ($\ll \phi_{BO}$). Barrier height voltage dependence as GB states are filling is then

$$\phi_B(V) = \phi_{BO} - \Delta E_F - V_1 \approx \phi_{BO} - \Delta E_F \qquad (7)$$

and ϕ_B remains almost constant since $\Delta E_F \ll \phi_{BO}$.

This situation continues as voltage increases until all GB states are full, and then reverts back to case 1: due to charge neutrality the total depletion layer width is clamped, and the barrier to electron flow from the left rapidly collapses, with a concomitant increase in current.

Examples of such voltage dependent decreases in GB barrier heights, and resulting increases in current, have been established for poly-Si[3-5] and ZnO varistors.[7]

MEASUREMENTS AND DISCUSSION

It is known that the most widely used types of MLC capacitors (Z5U, X7R, COG for example) exhibit super-ohmic currents. As noted above, such increases in current seen for poly-Si and varistors can be modelled on increased transmission over GB barriers. Can a similar model pertain to any type(s) of MLC capacitor? For which MLC types are activation energies voltage dependent, and if so, what is the form of the resulting current increase?

In order to address these questions we have measured I-V characteristics and activation energies for BL, X7R and COG capacitor types. For comparison, commercial varistors were also measured.

Varistor characteristics are shown in Figure 3. Current and activation energy dependences on voltage are more or less as expected.[2,7] It is seen that

*The voltage drop V_1 across the left hand (forward biased) side of the junction is approximately equal to $kT \ln 2$, which is negligible at normal temperatures and voltages.

activation energy (which is proportional to GB barrier height at a given voltage) decreases rapidly near the current breakdown region of voltage.

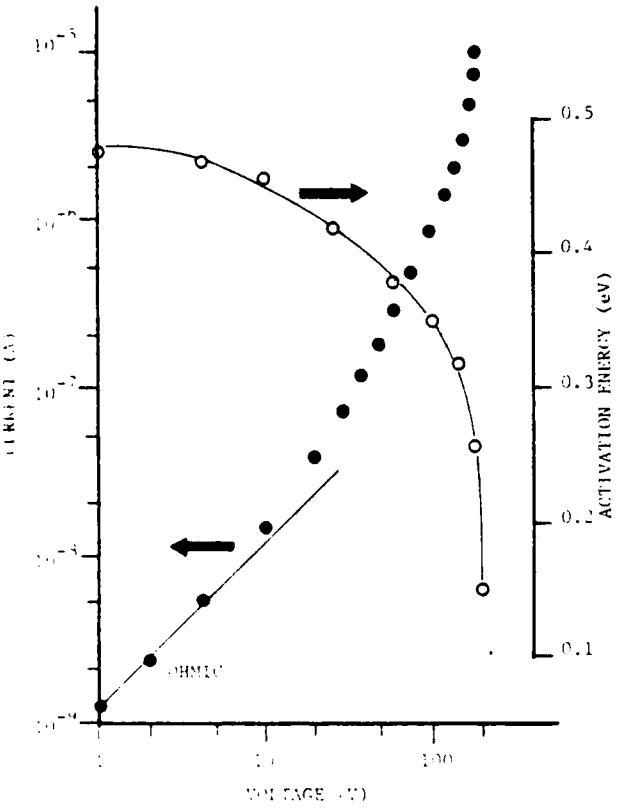


Figure 3. I-V and activation energy characteristics for commercial varistor.

Commercial BL capacitors show characteristics somewhat similar to those of the varistors (Figure 4). Three regions are evident on the I-V curve: 1) ohmic below about 1 volts; 2) sub-ohmic region for $2^{\sim}V^{\sim}10V$; 3) super-ohmic for $V^{\sim}10V$. These regions are consistent with the shape of the activation energy: constant below 10V and rapidly decreasing above. A low voltage ohmic region is expected for most current mechanisms (where the voltage per GB is less than kT/q). The sub-ohmic region has been predicted and reported for the poly-Si case,[3] although not reported for varistors. Since the grain boundaries can be viewed as back-to-back Schottky diodes, the sub-ohmic region represents a partial current saturation similar to the total saturation for a Schottky diode in reverse bias. The degree of saturation (ie. of sub-ohmicity) should depend strongly on donor density in the grain.[4] The super-ohmic region occurs due to the rapid decrease in activation energy above 10 volts.

Characteristics for a commercial COG device (C = 0.69 nF) are shown in Figure 5. The I-V characteristic is unlike those seen for poly-Si, varistors or BL capacitors in that it consists of two distinct linear regions: a near ohmic region ($I \propto V^{1.2}$) below 10V, and a super-ohmic one ($I \propto V^{2.5}$) at higher voltages.

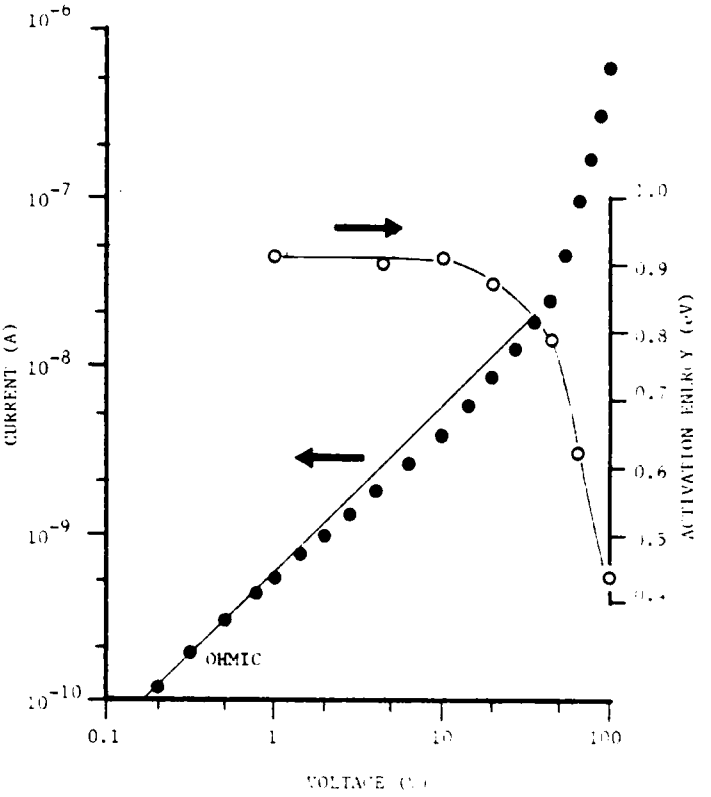


Figure 4. I-V and activation energy curves for commercial BL capacitor.

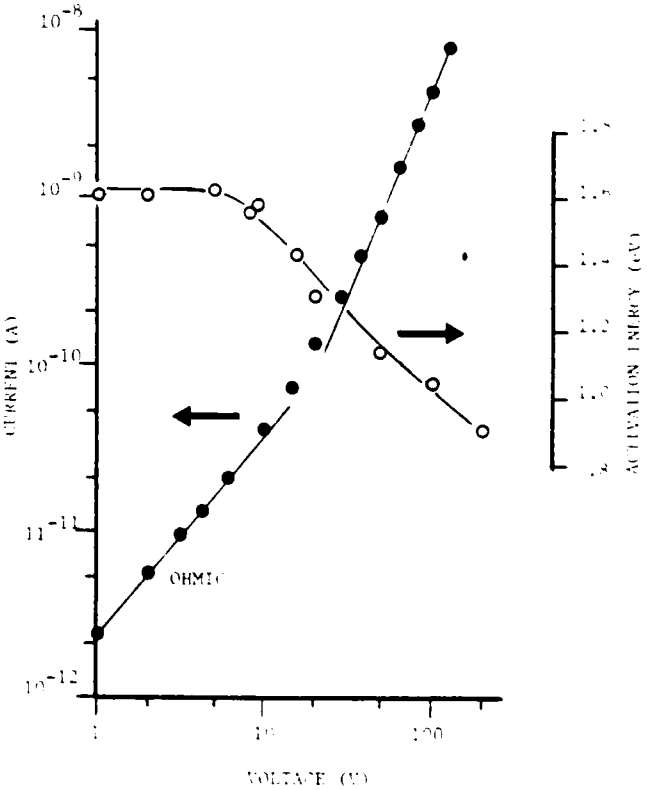


Figure 5. I-V and activation energy characteristics for 0.69 nF COG capacitor.

Even though the COG activation energy does decrease strikingly with voltage, it does so in a manner different from the BL case or the varistor. This could be due to the following:

1) If the E_A decrease is caused by GB trap filling, the nature of the decrease will depend on the energy distribution of states. According to Levine,[6] an exponentially increasing state density in the band gap (such as might be expected for a highly disordered material) should result in a GB barrier height that decreases with voltage as

$$\phi_B = A - B \ln V \qquad (8)$$

where A and B are material dependent constants. This is the approximate form for the decreasing E_A seen in Figure 5. The linear approximation to the curve above 10 volts is

$$E_A = 1.95 - 0.195 \ln V \qquad (9)$$

2) The voltage drop across the bulk of the grains should be taken into account. (This is not a large correction for the BL capacitor or varistor due to the low grain resistivity.) Assuming large grain resistivity for the COG, the IR drop will increase with current, and the decrease of E_A with voltage will be less severe due to the reduced fraction of voltage supplied to the GB. This may also account for the slight concavity of the E_A curve seen in Figure 5.

We have thus established that activation energies are strongly voltage dependent for the BL (as expected) and COG capacitors that we have measured. Such is not the case for the X7R type. For capacitors from two manufacturers, and for non-electrodes chips from one of the same manufacturers, activation energies were found to be voltage independent, even though currents show super-ohmic voltage behavior.

Characteristics for a 1 μF X7R capacitor are shown in Figure 6. The near 1.5 power law dependence above 10V is consistent with previous findings.[9] Activation energies for devices from both manufacturers were essentially voltage independent.

Silver-electroded chips 2mm thick of capacitor X7R material were also measured, using platinum/gold electrodes fired onto the surfaces. These chips exhibit both ohmic and space charge characteristics, the transition voltage occuring at about 400 V and being temperature independent. (See Figure 7.)

Activation energies for the chip were found to be 1.61, 1.33 and 1.31 eV at 10, 100 and 600 volts respectively.

The transition voltage from ohmic to space charge behavior for the chip is about 400 V. Where the transition voltage V_T would be for the capacitor (assuming the same type of planar electrode space charge current) can be found by equating the currents at $V=V_T$.

$$\varepsilon \frac{V_T}{d} = \theta \frac{V_T^3}{d^3} \qquad (10)$$

where ε and θ are materials constants and d is dielectric thickness. Values of V_T = 400 V and d = 0.2 cm [illegible]

$$V_T = [illegible] \text{ volts} \quad (d \text{ in cm}) \qquad (11)$$

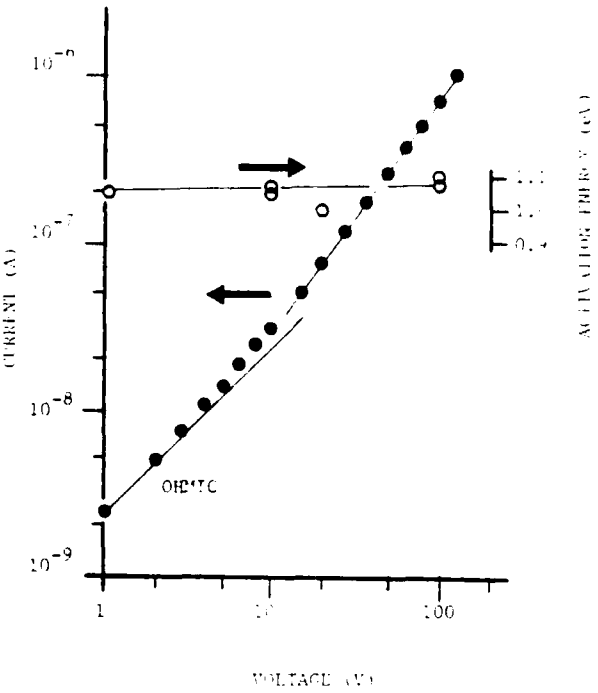


Figure 6. I-V and activation energy characteristics for 1 μF X7R capacitor.

Thus, for the capacitor, with $d \sim 5 \times 10^{-3}$ cm, V_T is expected to be about 0.25 V. This is below the minimum voltage (1 volt) at which we have attempted to obtain stable measurements for X7R capacitors. However, as seen in Figure 6, the I-V characteristic appears to be approaching ohmic behavior at the lower voltages. True ohmic behavior ($I \propto V$) might be expected for this type of X7R capacitor somewhere in the 0.1-1 volt decade.

The quadratic voltage region of the chip (400 - 1000 V) corresponds to 10 to 25 V for the capacitor (for equal electric fields), which fell within the range of measurement (Fig. 6). Why does the capacitor current change as $V^{1.5}$ whereas that of the chip goes as V^2? At present we feel that the different power law behaviors seen for the 2mm chip and MLC capacitor made from the same material are due to the increased importance of electrode roughness for the thinner layers of the capacitor.[9]

It is likely that the voltage dependence of E_A for the varistor and BL capacitor is due to the filling of energy states distributed across the band gap at grain boundaries. It is also possible that the E_A reduction for COG devices is caused by a similar mechanism, with the added condition that applied voltage is divided between grain bulk and boundary.

Why is the X7R activation energy (for samples from two manufacturers) independent of voltage? Firstly, there may be no significant GB potential barrier in X7R type ceramic to begin with. This could be an inherent property of the GB (which is unlikely, since charged states probably exist) or due to the fact

the dielectric constant is larger for this material and ϵ_B varies as $1/\epsilon$.* Therefore, ϵ_B would be smaller and have less effect on current. The rather large activation energy (1-1.3 eV) would then be due to other transport mechanisms, such as hopping. If this is the case, then one would not anticipate GB controlled transport for Z5 devices either, since its dielectric constant is even larger.

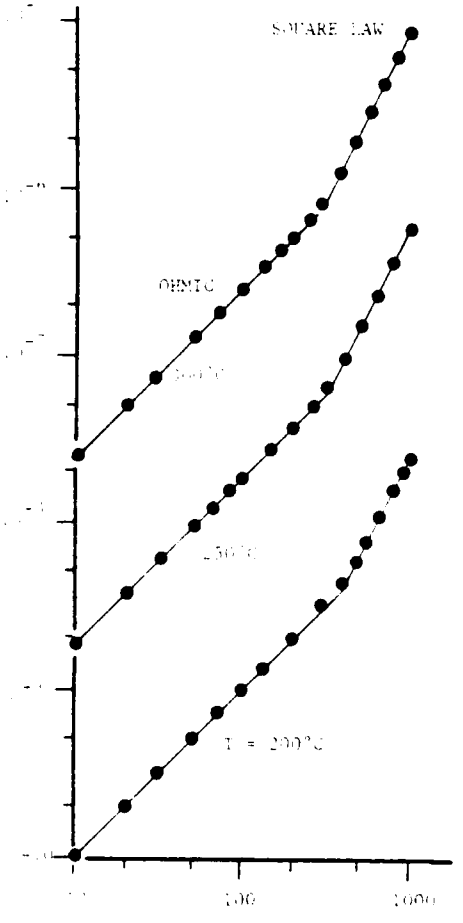


Figure 5. I-V characteristics for 2mm thick, non-electroded chip of X7R capacitor material.

A second possible reason for the independence of E_λ on voltage could be that the density of interface states is so large that they don't become exhausted over the range of applied voltage. The states may also have small capture cross sections for electrons.

Another possible reason is that there may be a higher resistivity region near the grain boundaries. Then the band diagram would resemble that shown in Fig. 1b. Space charge width could be clamped, mostly in the high resistance region. As electron trapping in grain boundaries occurs, positive charge (required for charge neutrality) is supplied by only a very small movement of the space charge into the lower resistivity region of the grain, on the right. The left hand side will not collapse as rapdily under bias if it extends any significant distance into the lower resistivity region. It is feasible that if the resistivity on both sides of the GB is large enough, ϵ_B could remain clamped at its zero bias value. This high resistance region could be close to intrinsic (i-layer). The Fermi energy would lie near mid-gap, and the resulting band bending could influence the barrier height more than the occupation of grain boundary states. The resistivity of this near-grain boundary i-layer could thus control leakage current by virtue of its voltage independent barrier, which would decrease if the layer became semiconducting n-type during voltage/temperature stress. Then the barrier height (as reflected in activation energy) would decrease and leakage current would increase, which are both observed for degraded X7R devices.

It is worthwhile to examine how degradation of ceramic resistance can occur if that resistance is controlled by grain boundaries. We just mentioned a possible degradation mechanism for a GB barrier height of the Figure 1b type. How about for the Fig. 1a type, which is for homogeneous grains? Here the barrier height at zero bias (ϵ_{BO}) is given by equation 4. It is seen that ϵ_{BO} can be reduced by two mechanisms (assuming ϵ is constant). GB charge can be reduced by hydrogen annealing or impurity segregation for example. Grain boundary states are "passivated" and trapped charge, barrier height and overall resistance are reduced. Another mechanism is to increase the donor density N_D. Thus, the maintainance of a large GB potential barrier can be just as important as a low carrier concentration in the grain for minimizing leakage current.

CONCLUSIONS

1. A decrease in activation energy with voltage for barrier layer capacitors is accompanied by a rapid rise in leakage current. This is attributed to a GB barrier height decrease as energy states in the band gap at the GB are filled.

2. A similar decrease in ϵ_B for COG devices is also accompanied by a change in current from ohmic to super-ohmic ($I \propto V^{2.5}$). The decrease in ϵ_B is not as rapid as for the BL type, perhaps due to the larger grain resistance of the COG.

3. Activation energies for X7R capacitors and ceramic chips are voltage independent, even though currents become super-ohmic. Several possible reasons for the constant E_λ are given including higher dielectric constant, larger density of interface states, smaller electron capture rate and the existance of an i-layer near the GB.

4. Reduction of the GB barrier height by means of energy state passivation and/or increase in bulk donor density will result in lower resistivity and enhanced leakage current.

ACKNOWLEDGEMENTS

We would like to acknowledge the Office of Naval Research for supporting this work, and Corning Electronics for supplying samples.

*A reasonable model for the $BaTiO_3$ type thermistor is based on the variation of dielectric constant with temperature, with ϵ_B becoming large above the Curie temperature due to the decrease in dielectric constant. (See reference 2, p. 154.)

REFERENCES

[1] L. L. Kazmerski, Polycrystalline and Amorphous Thin Films and Devices, Academic Press (1980).

[2] L. M. Levinson (ed.), Grain Boundary Phenomena in Electronic Ceramics, American Ceramic Society (1981).

[3] G. E. Pike and C. H. Seager, "Grain Boundary States and Varistor Behavior in Silicon Bicrystals," Appl. Phys. Lett. 35, 709 (1979).

[4] G. E. Pike and C. H. Seager, "The DC Voltage Dependence of Semiconductor Grain-Boundary Resistance," J. Appl. Phys 50, 3414 (1979).

[5] P. L. Leamy, G. E. Pike and C. H. Seager (eds.), Grain Boundaries in Semiconductors, North Holland (1982).

[6] J. P. Levine, "Theory of Varistor Electronic Properties," CRC Critical Reviews in Solid State Sciences, p. 597 (Nov. 1975).

[7] G. D. Mahan, L. M. Levinson and H. R. Philipp, "Theory of Conduction in ZnO Varistors, J. Appl. Phys. 50, 2799 (1979).

[8] W. Heywang, "Resistivity Anomaly in Doped Barium Titanate," J. Amer. Ceram. Soc. 47, 484 (1964).

[9] E. Y. Lee, K. C. Lee, J. N. Schunke and L. C. Burton, "Leakage Currents in Multilayer Ceramic Capacitors," IEEE Transactions, CHMT-7, 443 (1984).

END

FILMED

8-85

DTIC