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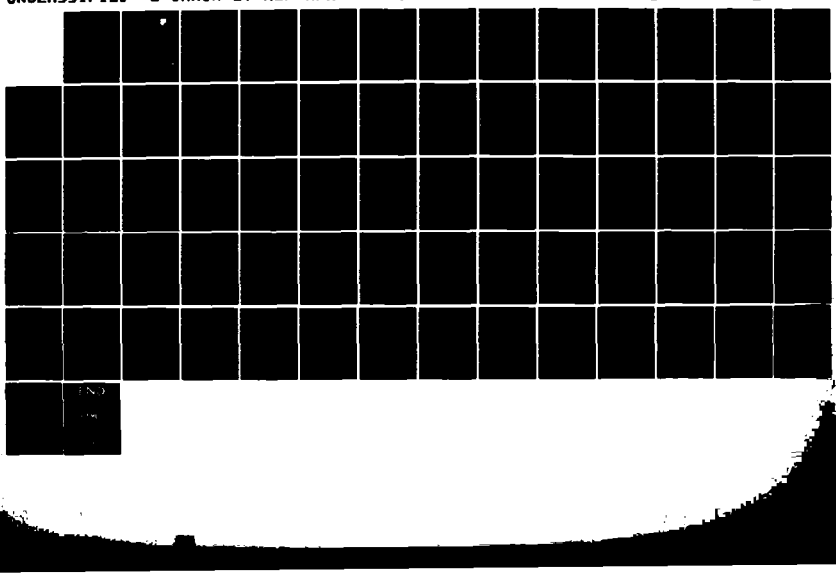

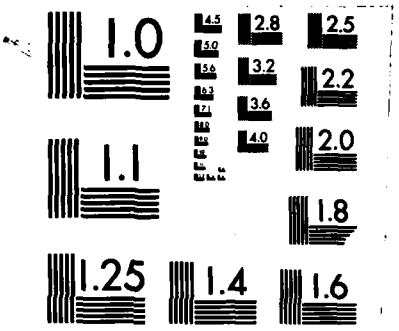

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RADC-TR-82-286, Vol IIIb (of six)
Final Technical Report
April 1985

BASIC EMC TECHNOLOGY ADVANCEMENT FOR C³ SYSTEMS Computer Simulation Of EMI Effects In A Differential Line Receiver

Southeastern Center for Electrical Engineering Education

Z. Chair, T. Dave, H. Ouibrahim and D. Weiner

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441-5700

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APPROVED: Roy F. Stratton

ROY F. STRATTON
Project Engineer

APPROVED: W. S. Tuthill

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19. ABSTRACT (Continue on reverse if necessary and identify by block number)

It is frequency necessary to transmit baseband digital data over long transmission lines such as system interconnect cables. When the cables are located in a high EMI environment, ordinary integrated logic circuits cannot be used to synthesize the line driver and receiver because such circuits are unable to discriminate between a valid signal and the externally induced interference. One solution for combating the interference is to convert the ground referenced digital data at the driver into a differential signal which is transmitted over a pair of wires such as a twisted-pair line. A differential line receiver is used at the other end. Interference which appears equally on each wire is referred to as common-mode interference. Ideally, the line receiver responds only to the differential signal transmitted over the line and rejects the common-mode interference.

This report describes some preliminary results dealing with the computer simulation of EMI effects due to sinusoidal interference in a DS 55155 differential line receiver. Attention

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is focused on the receiver, as opposed to the line driver, because the receiver is significantly more susceptible. Consequently, the susceptibility of the driver-received pair, in most cases, is determined by that of the receiver.

The computer program selected for the investigation was SPICE (Simulation Program with Integrated Circuit Emphasis) which was exercised in its transient mode. Thus, a time-domain analysis was performed and time waveforms were generated at all nodes of interest. Parameter values of the semiconductor devices embedded in the integrated circuit for the receiver are not published in the interface handbooks. Reasonable values were determined by adjusting nominal values until the computer simulated characteristics closely agreed with typical performance characteristics supplied by the manufacturer. These included curves of 1) input current vs. input voltage, 2) output voltage vs. common-mode input voltage, 3) high level output voltage vs. high level output current, 4) low level output voltage vs. low level output current, 5) output voltage vs. differential input voltage, 6) output voltage vs. strobe input voltage, and 7) power supply current vs. power supply voltage.

The sinusoidal interference was impressed at the two data inputs, the strobe terminal, and the response-time control input. Waveform distortion in the output signal was noted for suitably strong interferers. Waveform parameters for describing the distortion are defined and plotted as a function of the frequency and/or amplitude of the sinusoidal interferer.

Particular attention is devoted to dc offsets caused by rectification in the base-to-emitter and base-to-collector transistor junctions. The input voltage at which the output changes state is defined as the input threshold voltage. The rectification of RF energy causes the input threshold voltage to change. The concept of using this change to define receiver susceptibility is examined.

In addition to decreasing the noise margin, a change in the input threshold voltage can cause time variations in the receiver output (i.e., pulses may appear shifted in time and some pulses may appear longer or shorter). The resulting jitter contrains the minimum pulse width and, therefore, the maximum data rate which can be used. This effect is examined as a function of the amplitude and/or frequency of the sinusoidal interference.

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Chapter 1

INTRODUCTION

The interfacing of systems (or subsystems) frequently requires transmission of baseband digital data from one location to another. Line drivers, transmission lines, and line receivers are used for this purpose. When the lines are located in a high EMI environment, conventional logic circuits are inadequate for use in the line driver and receiver because such circuits cannot discriminate between an intended signal and the externally induced interference. One solution for combating both ground noise due to ground-loop currents and induced interference on the line is to convert the ground referenced digital data at the line driver into a differential signal which is transmitted over a pair of wires such as a twisted-pair line. A differential line receiver, which receives the differential data and delivers typical TTL voltages at its output, is used at the receiving end of the line. Interference which appears equally at the two terminals of the receiver input port is referred to as common-mode interference. Ideally, the differential line receiver responds only to the differential signal transmitted over the line and rejects the common-mode interference.

This paper discusses the computer simulation of sinusoidal interference in a National DS 55115 integrated circuit differential line receiver. The receiver is designed to sense differential signals (i.e., differences in the signals at the two terminals of the input port). Typically, the receiver is used in conjunction with the National DS 55114 integrated circuit differential line driver which provides

differential output signals with high current capability for driving balanced lines such as twisted pairs. Attention in this effort is focused on the receiver, as opposed to the line driver, because the receiver is significantly more susceptible. Consequently, the susceptibility of the driver-receiver pair is determined by that of the receiver for most interference situations.

Chapter 2

MODELING THE DIFFERENTIAL LINE RECEIVER

The computer program selected for the investigation was SPICE (Simulation Program with Integrated Circuit Emphasis) which was exercised in its transient mode of operation. A complete schematic of the differential receiver is shown in Figure 1. The two terminals of the input port are referred to as inputs A and B, respectively. If v_A and v_B denote the corresponding voltages between input and ground, the differential input is defined to be $v_{ID} = v_B - v_A$ while the common-mode input is given by $v_{ICM} = (v_A + v_B)/2$. The circuit is somewhat complex, containing 19 transistors, 3 diodes, 27 resistors, and 3 capacitors. Observe that, during the entire investigation of EMI effects, the pull-up and sink outputs were connected together with a resistive load of 3.9 kΩ tied from the output to the power supply voltage, $V_{cc} = 5V$, a capacitive load of 3pF tied from the output to ground. The resistor and capacitor values given in Figure 1 are those provided by the manufacturer. Unfortunately, the manufacturer does not specify parameter values for the transistors and diodes embedded in the integrated circuit.

Reasonable parameter values were determined by adjusting nominal values until the computer simulated characteristics closely agreed wtih typical performance characteristics supplied by the manufacturer. These included curves of input current vs. input voltage (see Figure 2), output voltage vs. common-mode input voltage (See Figure 3), high level

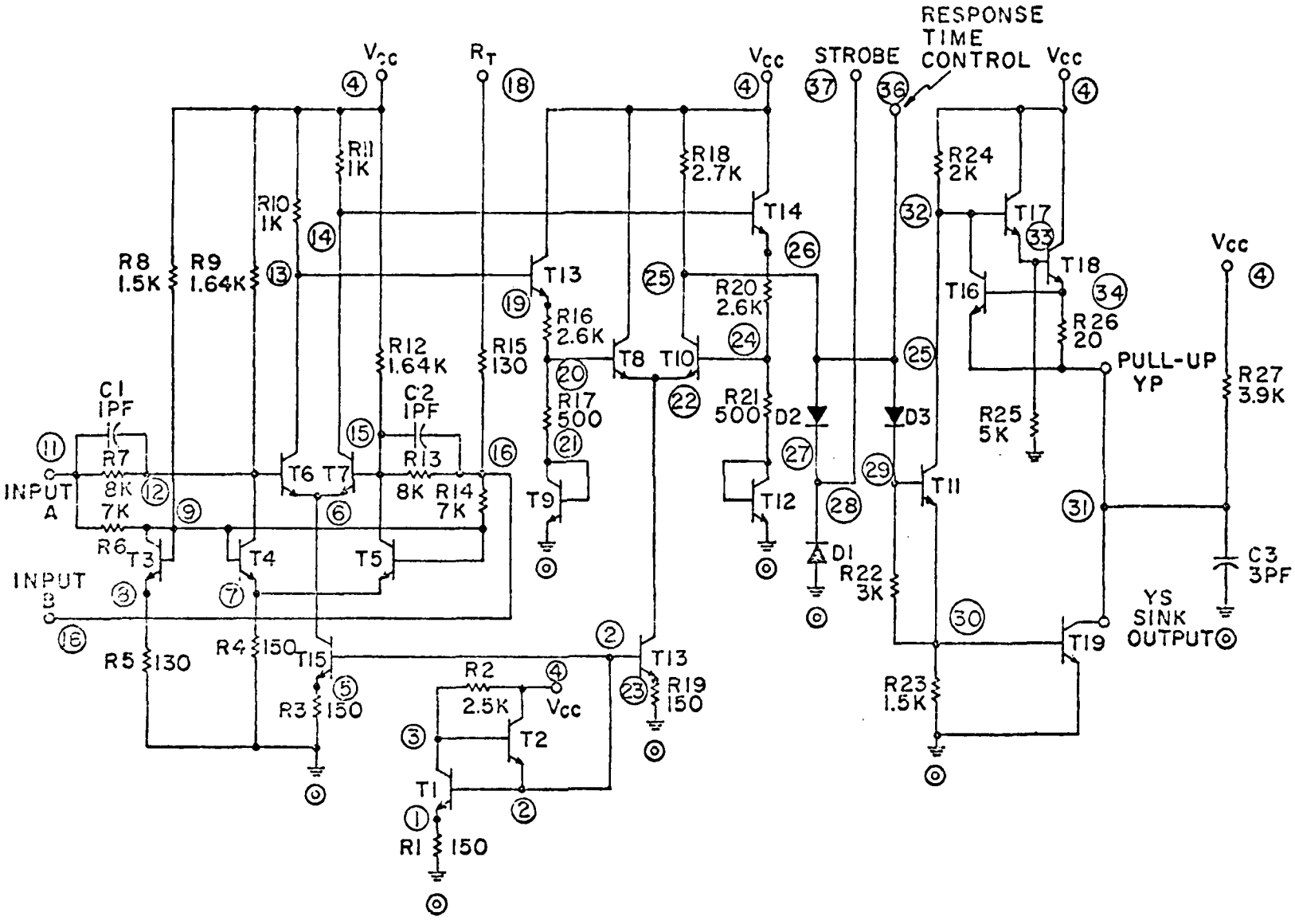
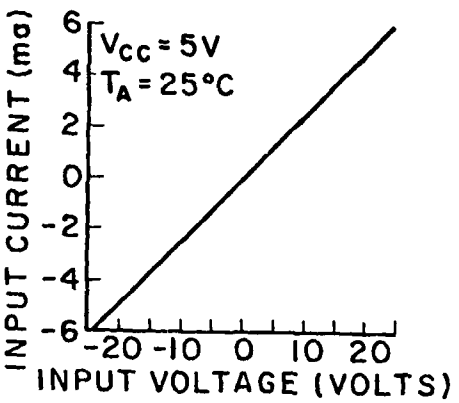
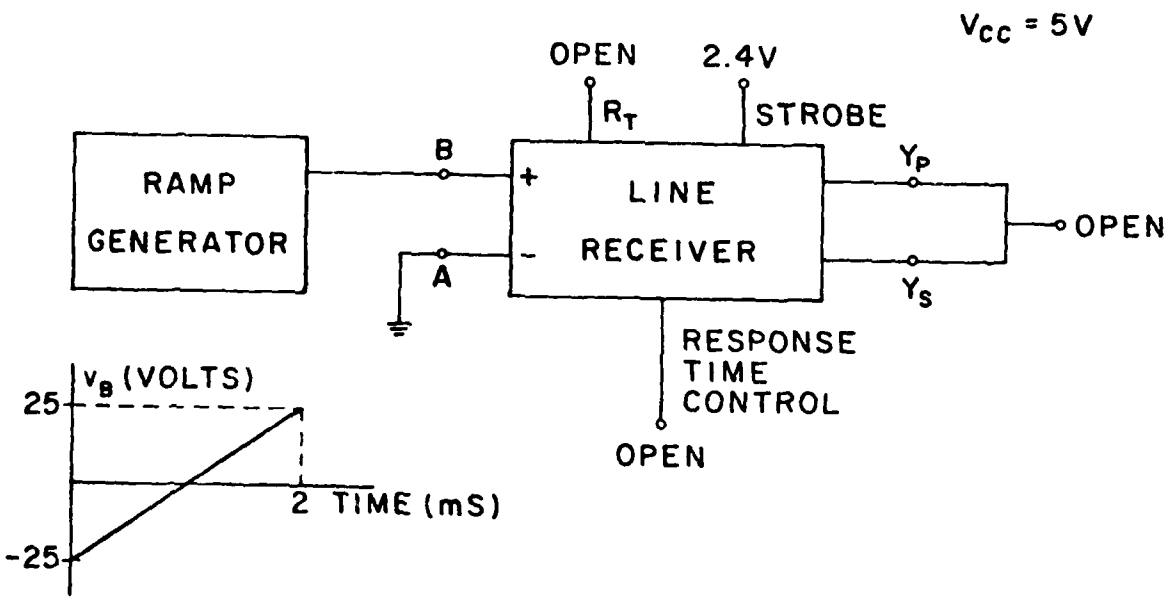


Figure 1. Complete schematic of DS 55115 differential line receiver.



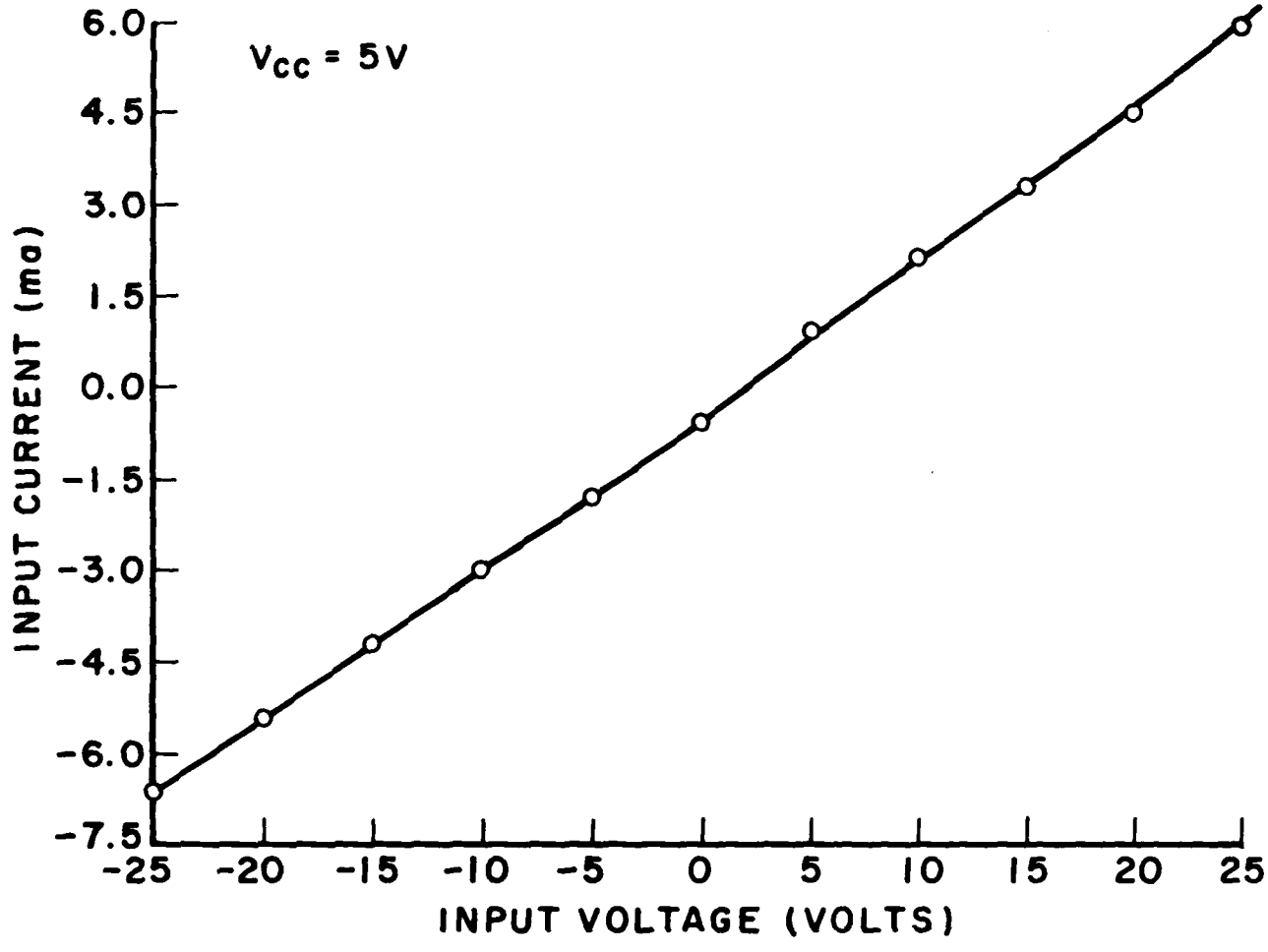
2(a)



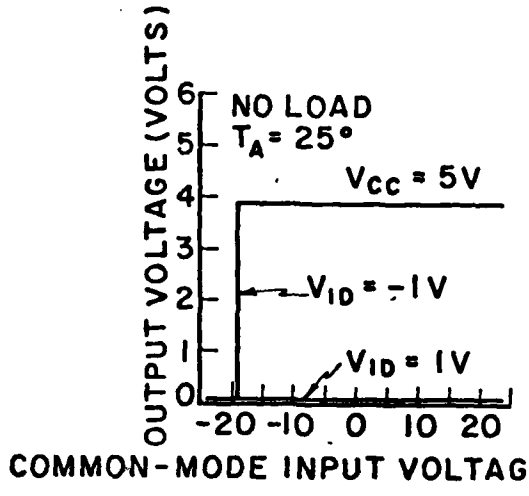
2(b)

Figure 2 Input current vs. input voltage.

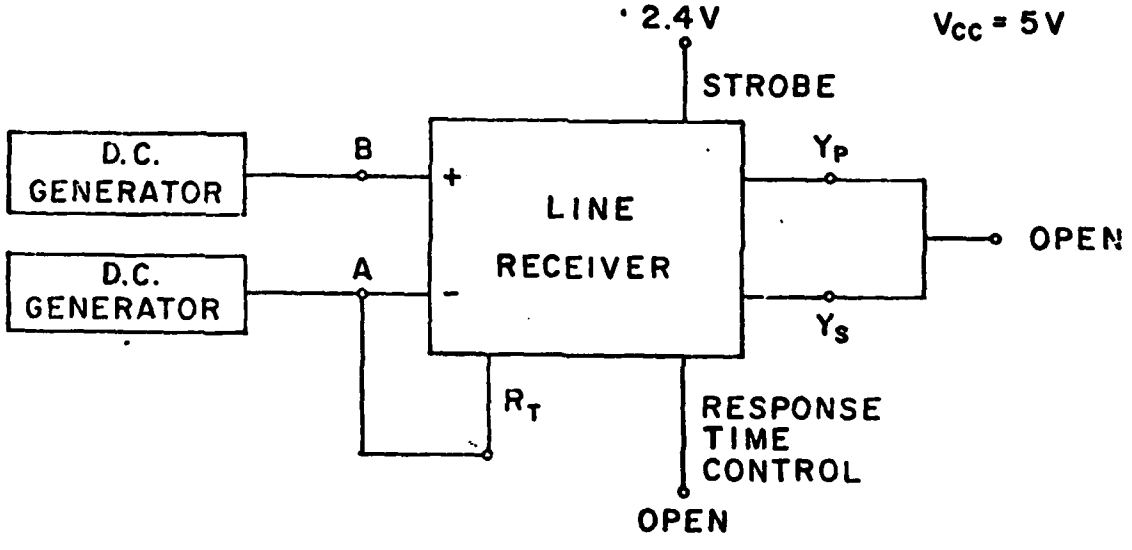
(a) Manufacturer's typical characteristic.
(b) Test circuit used in the computer simulation.
(c) Computer simulated characteristic.


V_{CC} = 5V
INPUT CURRENT (ma)
6.0
4.5
3.0
1.5
0.0
-1.5
-3.0
-4.5
-6.0
-7.5
-25
-20
-15
-10
-5
0
5
10
15
20
25
INPUT VOLTAGE (VOLTS)

2(c)

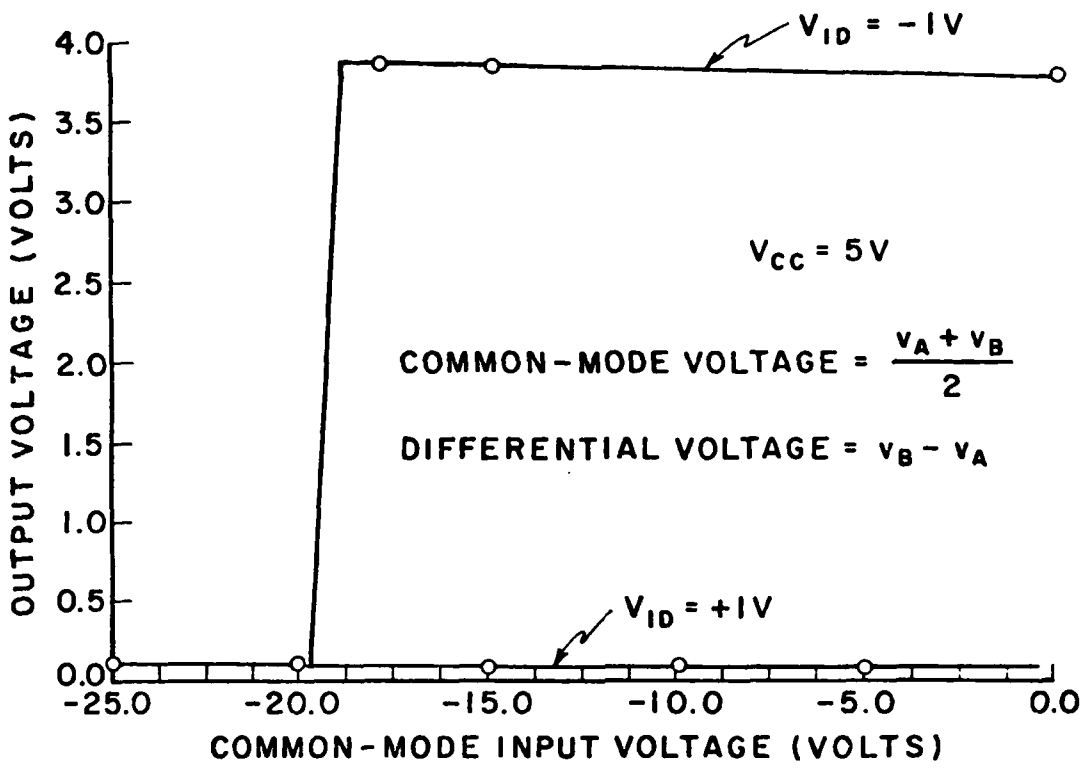


3(a)



3(b)

Figure 3. Output voltage vs. common-mode input voltage.
(a) Manufacturer's typical characteristic.
(b) Test circuit used in the computer simulation.
(c) Computer simulated characteristic.



INPUT VOLTAGES USED IN SIMULATION WERE:

$V_{ID} = +1V$

V_A (VOLTS)	-25.5	-15.5	-10.5	-0.5	9.5	19
V_B (VOLTS)	-24.5	-14.5	-9.5	0.5	10.5	20

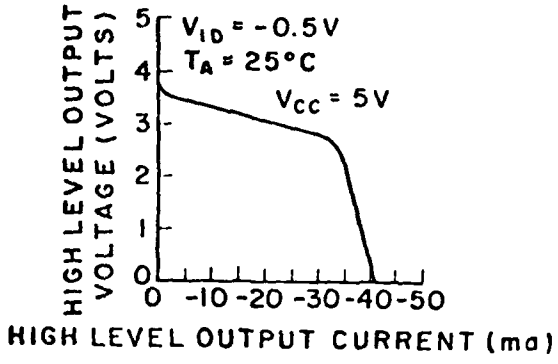
$V_{ID} = -1V$

V_A (VOLTS)	+0.5	-14.5	-17.5	-18.5	-19	-19.5	-24.5	19.5
V_B (VOLTS)	-0.5	-15.5	-18.5	-19.5	-20	-20.5	-25.5	18.5

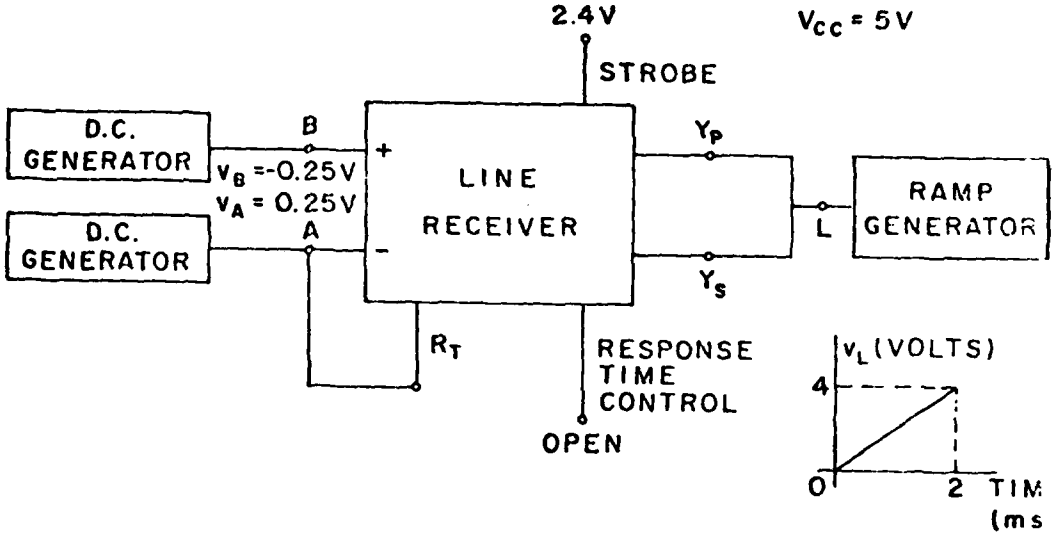
3(c)

output voltage vs. high level output current (see Figure 4), low level output voltage vs. low level output current (see Figure 5), output voltage vs. differential input voltage (see Figure 6), output voltage vs. strobe input voltage (see Figure 7), and power supply current vs. power supply voltage (see Figure 8). In each figure, part (a) shows the manufacturer's typical characteristic, part (b) presents the test circuit used in the computer simulation, and part (c) gives the computer simulated characteristic. The curves in figures 2, 3, 6, and 7 show excellent agreement while those in figures 4,5 and 8 show the correct trend although the currents tend to be low. It should be noted that there are two DS 55115 line receivers in a single package. Since the currents in the computer simulated characteristics of Figures 4,5, and 8 are approximately one half of those in the manufacturer's characteristics, a possible explanation is that the manufacturer's curves were obtained under load conditions different from those used in the computer simulation.

Also of use in modeling the line receiver were the rise and fall times, t_r and t_f, and the propagation delay times, t_{PHL} and t_{PLH}. These are defined in Figure 9, as taken from the manufacturer's data sheet. The rise and fall times are guaranteed to be less than or equal to 5 nS while the propagation delay times are guaranteed to

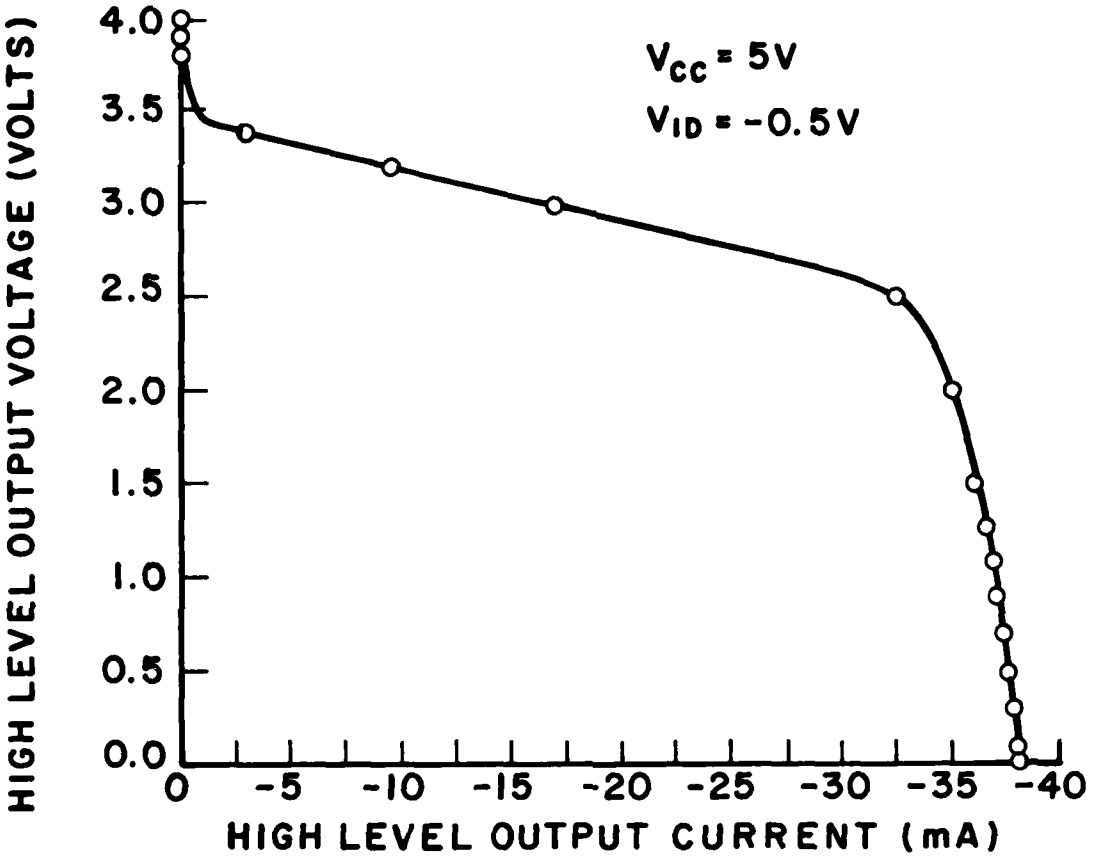


4 (a)



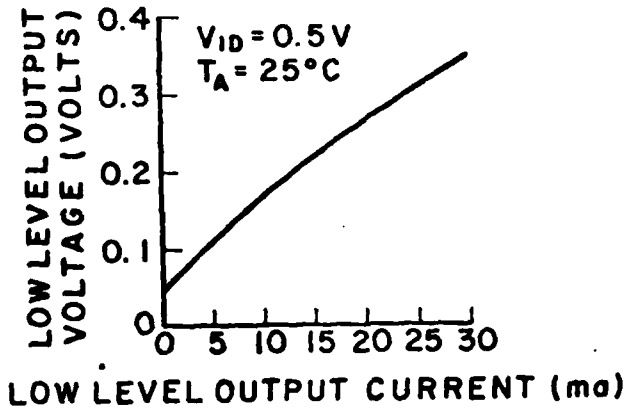
4 (b)

Figure 4. High level output voltage vs. high level output current.
(a) Manufacturer's typical characteristic.
(b) Test circuit used in the computer simulation.
(c) Computer simulated characteristic.

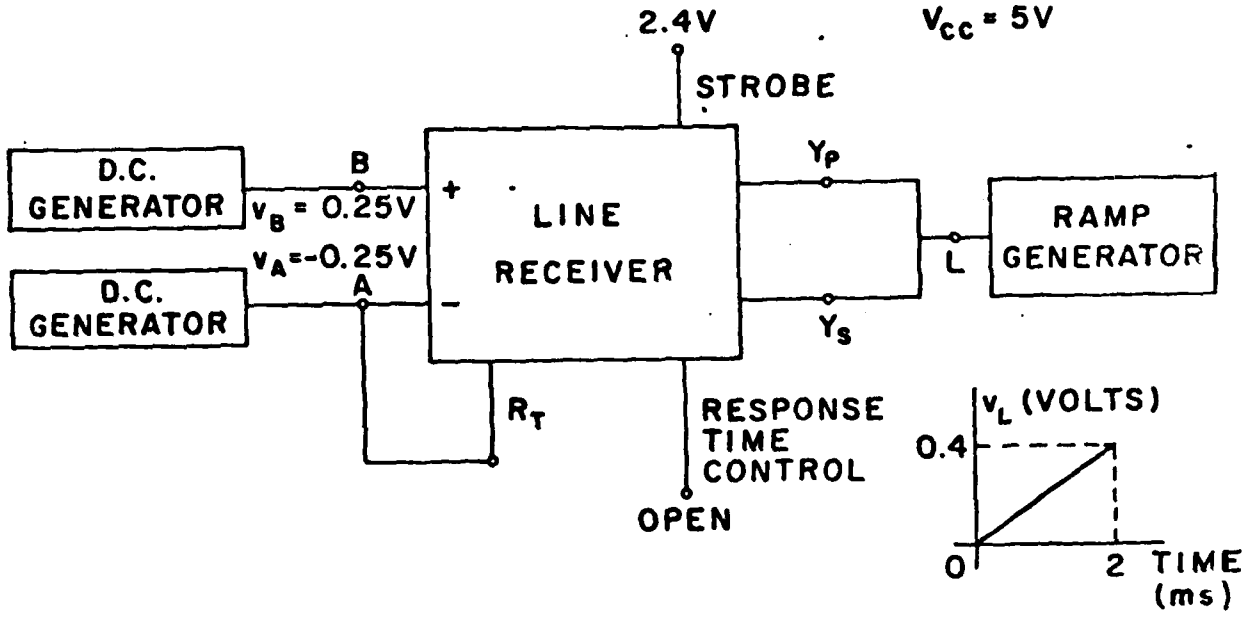


4(c)

Figure 4. High level output voltage vs. high level output current.
(a) Manufacturer's typical characteristic.
(b) Test circuit used in the computer simulation.
(c) Computer simulated characteristic.

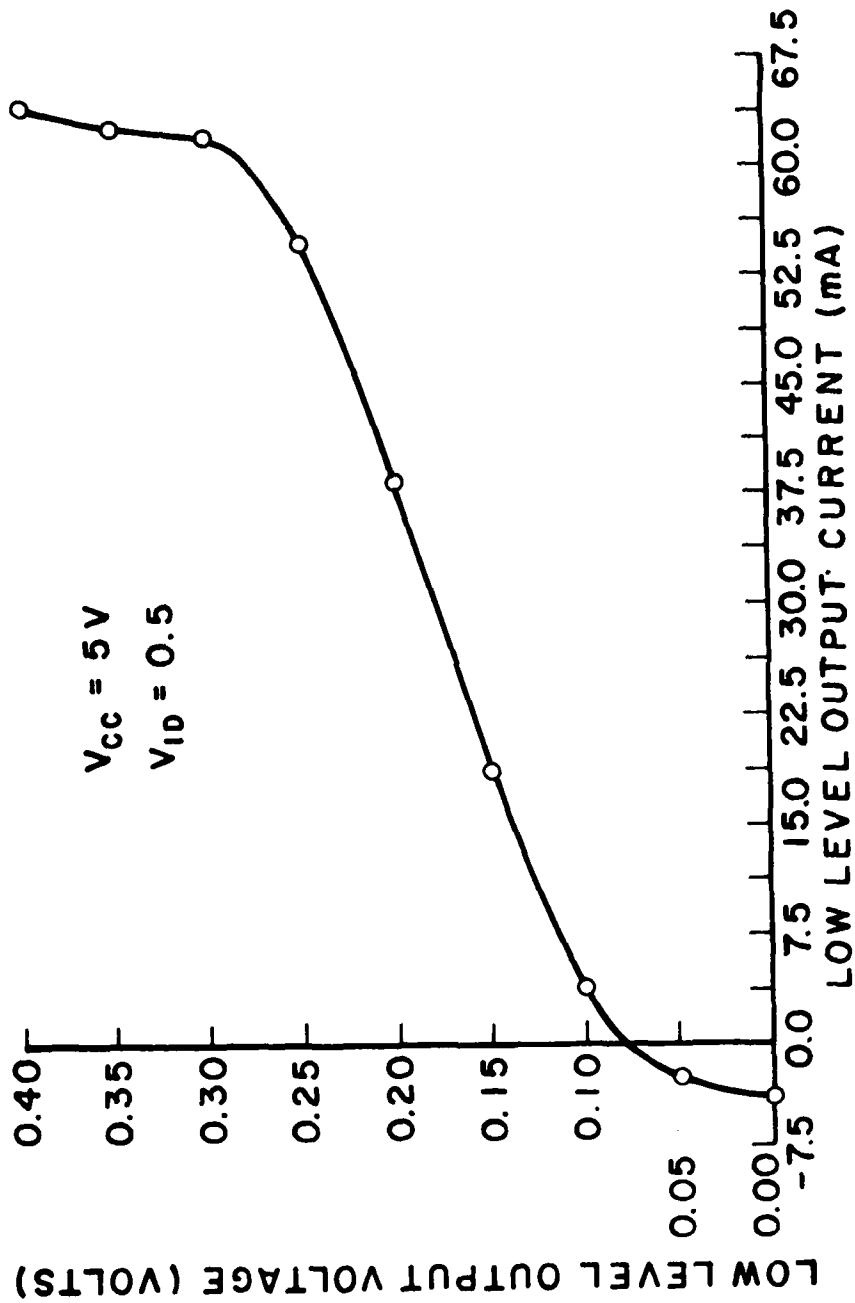


5(a)

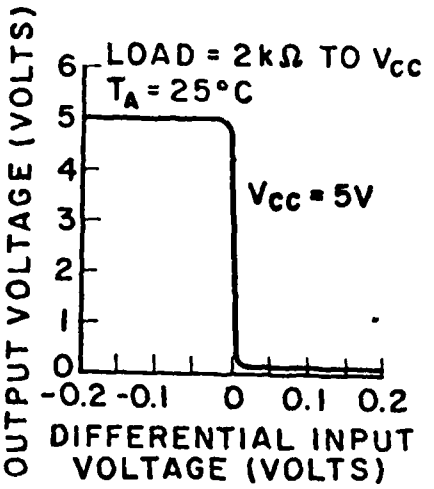


5(b)

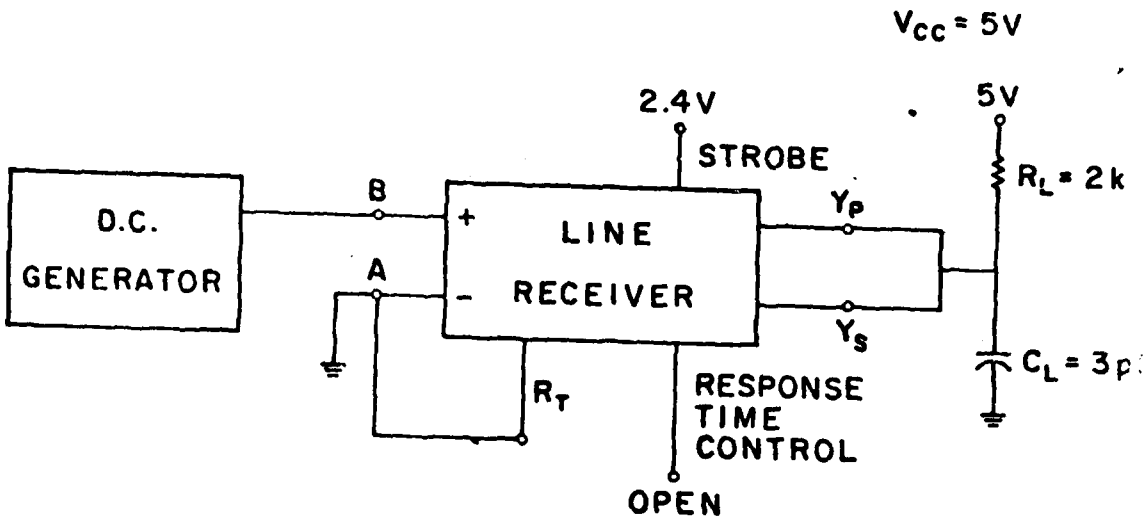
Figure 5. Low level output voltage vs. low level output current.
(a) Manufacturer's typical characteristic.
(b) Test circuit used in the computer simulation.
(c) Computer simulated characteristic.


LOW LEVEL OUTPUT VOLTAGE (VOLTS)
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
-7.5
0.0
7.5
15.0
22.5
30.0
37.5
45.0
52.5
60.0
67.5
LOW LEVEL OUTPUT CURRENT (mA)
V_{CC} = 5V
V_{ID} = 0.5

5(c)

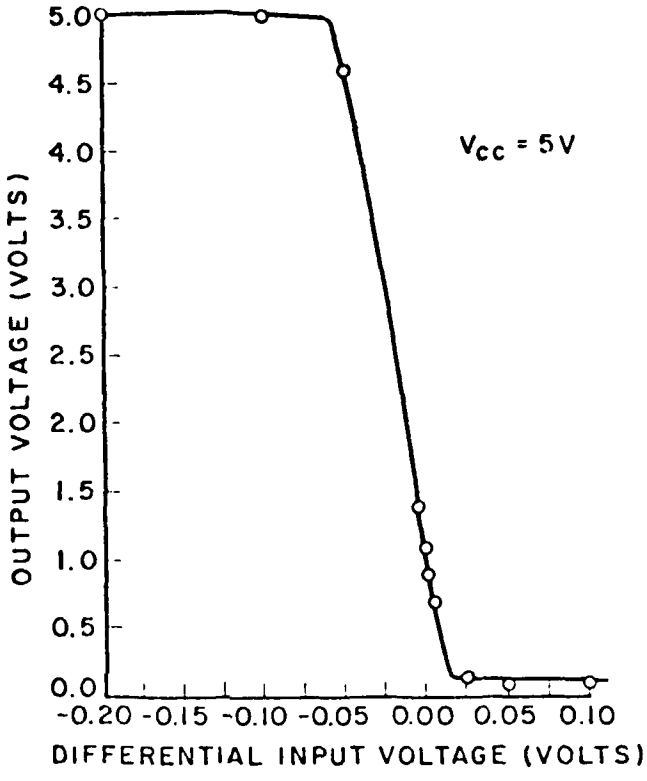


6 (a)



6 (b)

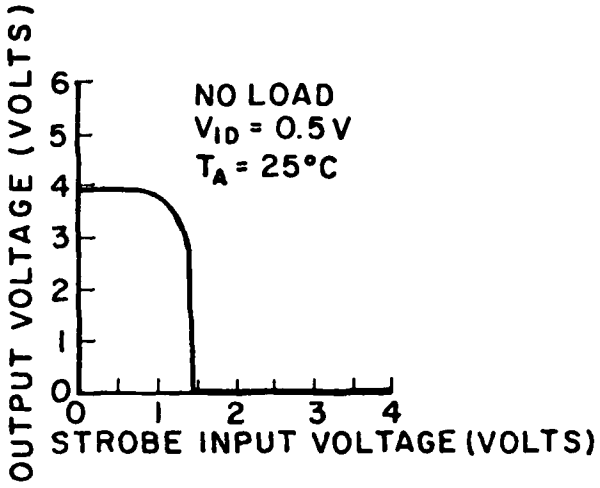
Figure 6. Output voltage vs. differential input voltage.
(a) Manufacturer's typical characteristic.
(b) Test circuit used in the computer simulation.
(c) Computer simulated characteristic.



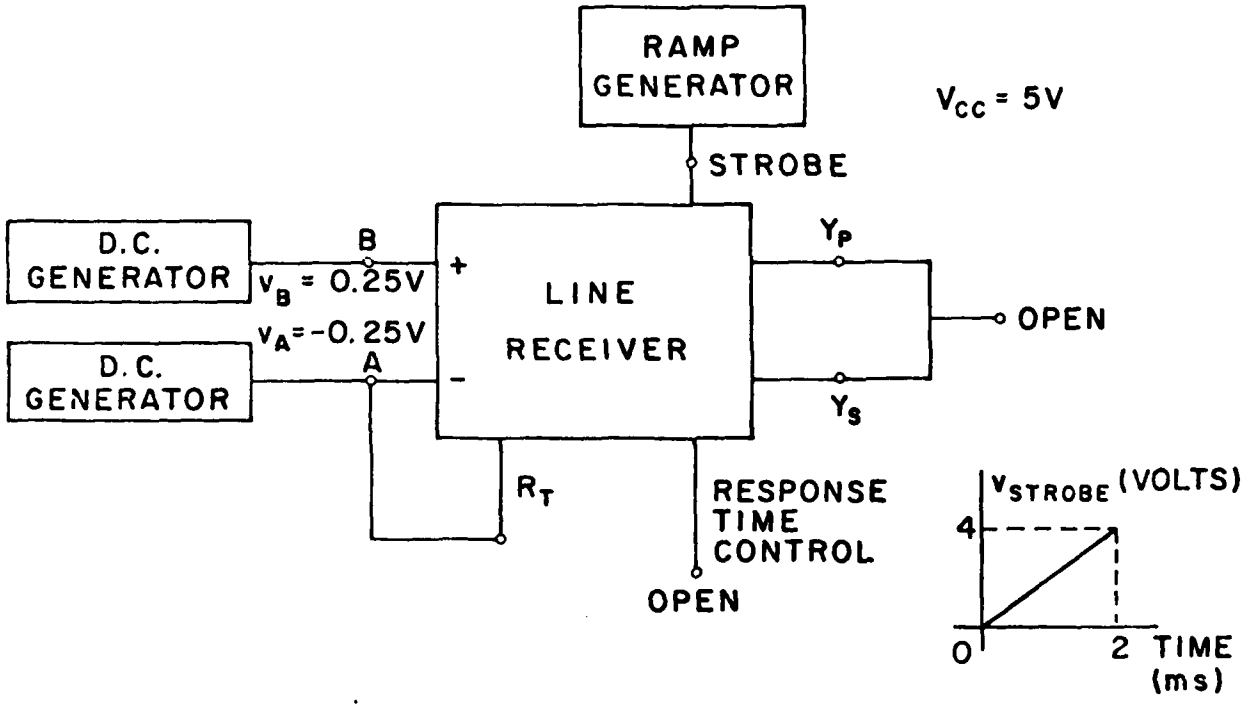
DATA POINTS ON THE CURVE ARE:

V_A (VOLTS)	0	0	0	0	0	0	0	0	0	0
V_B (VOLTS)	-0.2	-0.1	-.075	-.05	-.005	-.001	.001	.005	.1	.2
V_{ID} (VOLTS)	-0.2	-0.1	-.075	-.05	-.005	-.001	.001	.005	.1	.2
V_{OUT} (VOLTS)	5	5	4.99	4.6	1.4	1.1	.9	.69	.08	.08

6(c)

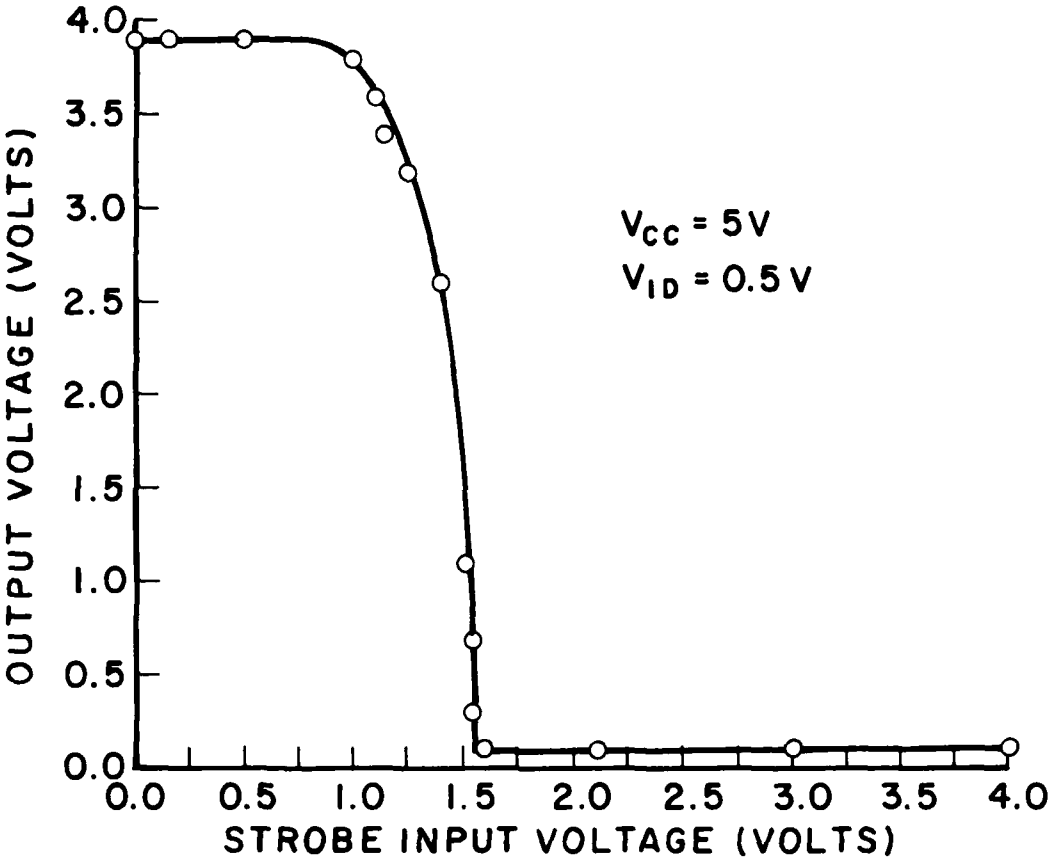


7 (a)

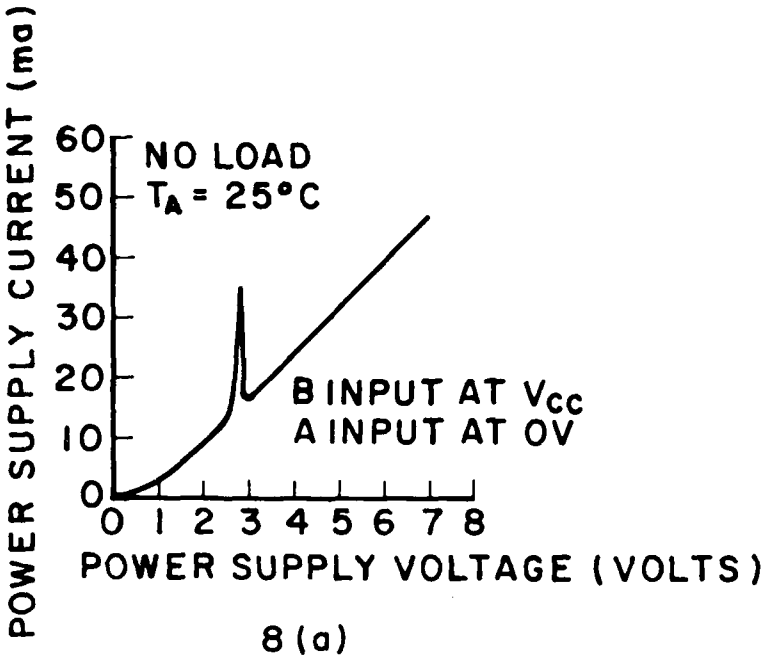


7 (b)

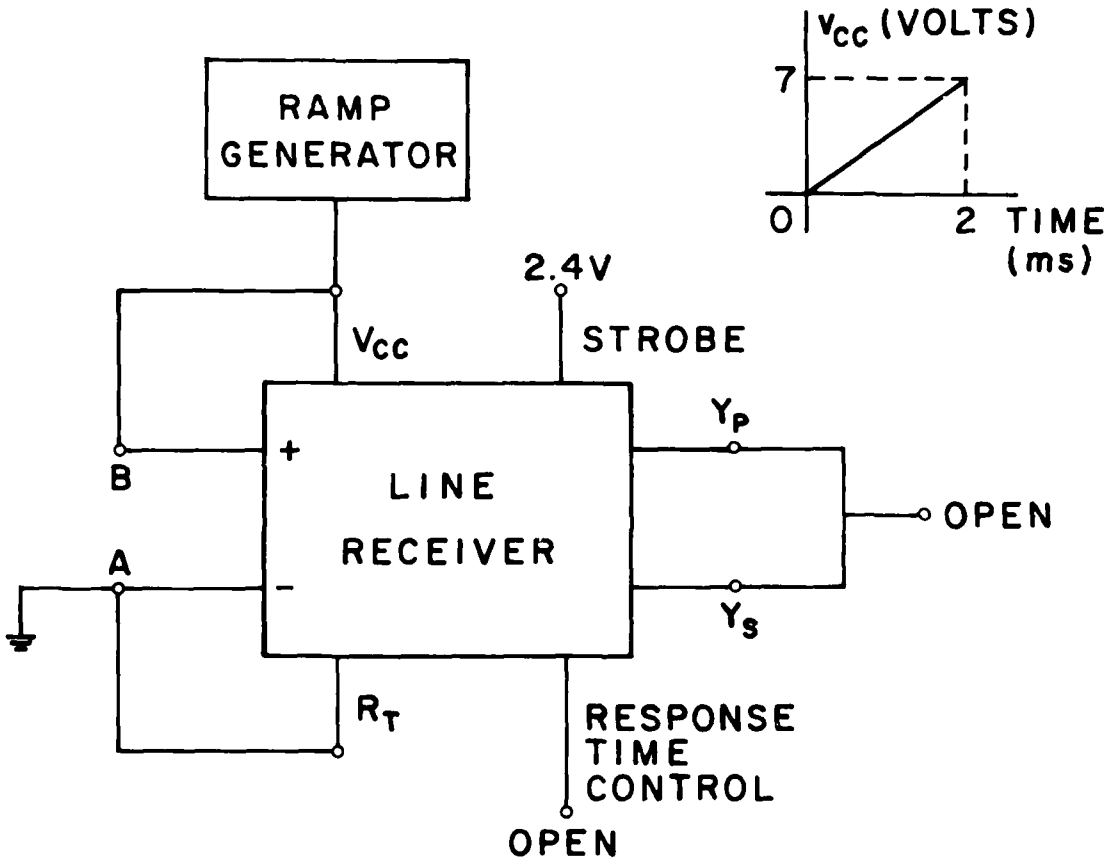
Figure 7. Output voltage vs. strobe input voltate
(a) Manufacturer's typical characteristic.
(b) Test circuit used in the computer simulation.
(c) Computer simulated characteristic.


4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
OUTPUT VOLTAGE (VOLTS)
V_{CC} = 5V
V_{ID} = 0.5 V
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0
STROBE INPUT VOLTAGE (VOLTS)

7 (c)

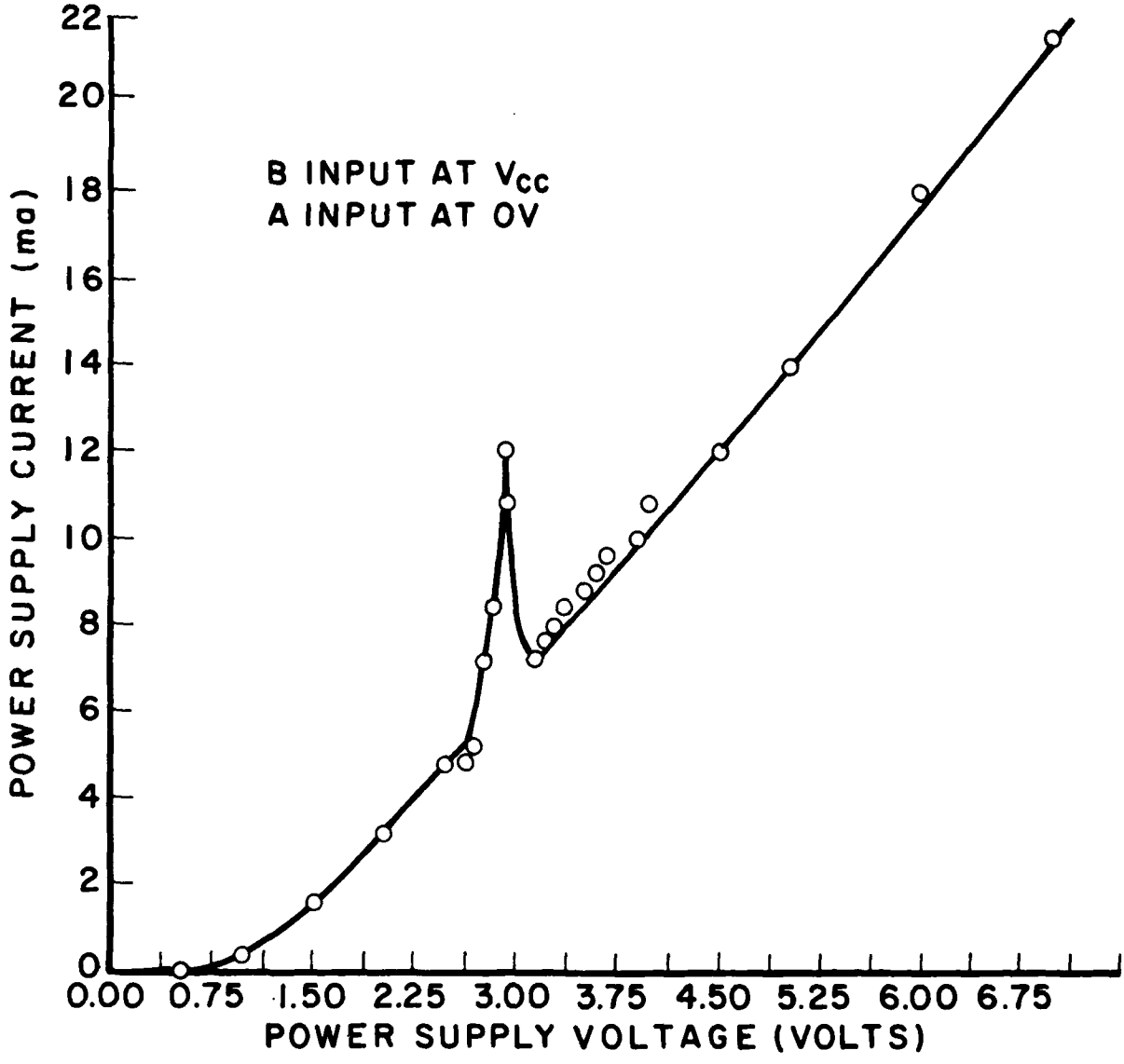


8 (a)



8(b)

Figure 8. Power supply current vs. power supply voltage.
(a) Manufacturer's typical characteristic.
(b) Test circuit used in the computer simulation.
(c) Computer simulated characteristic.


B INPUT AT V_{CC}
A INPUT AT 0V
POWER SUPPLY CURRENT (ma)
0
2
4
6
8
10
12
14
16
18
20
22
0.00 0.75 1.50 2.25 3.00 3.75 4.50 5.25 6.00 6.75
POWER SUPPLY VOLTAGE (VOLTS)

8(c)

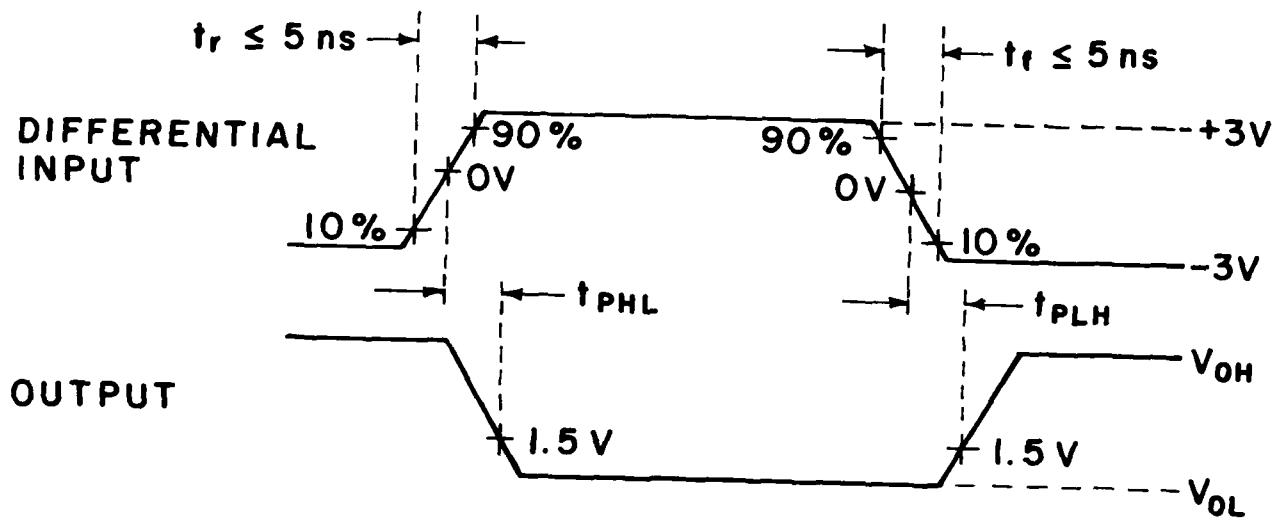


Figure 9. Definition of the rise and fall times, t_r and t_f, and the propagation delay times, t_{PHL} and t_{PLH}.

be less than or equal to 50 nS. Typical values for the propagation delays are t_{PLH} = 18 nS and t_{PHL} = 20 nS. Values obtained for the circuit used in the computer simulation are $t_r = t_f$ = 5nS, t_{PLH} = 23 nS, and t_{PHL} = 13 nS. These values fall within the manufacturer's specifications.

The SPICE parameters used to model the diodes and transistors in the circuit schematic of Figure 1 are listed in the Appendix along with values for the discrete resistors and capacitors.

Chapter 3

RESULTS OF COMPUTER SIMULATION

A. Quasi-stationary Behavior

In TTL logic an output voltage must exceed 2.4 volts if it is to be considered HIGH and must be below 0.4 volts if it is to be considered LOW. From Figure 6(c) it is seen that the line receiver output is HIGH when the differential input is less than -0.015 volts and is LOW when the differential input exceeds +0.01 volts. For differential inputs below -0.075 volts, the output remains constant at 5.0 volts while, for differential inputs above +0.025 volts, the output is fixed at 0.08 volts. The input voltage at the middle of the switching region is defined to be the input voltage threshold and is approximately zero for the characteristic of Figure 6(c). When the receiver follows the static characteristic of Figure 6(c), the receiver is said to behave in a quasi-stationary manner. At high enough input frequencies, the receiver departs from quasi-stationary behavior. Of interest is the maximum input frequency for which the receiver obeys the static characteristic of Figure 6(c).

To produce a reference output waveform, the line receiver was excited by a pulsed differential input which varied from -0.2 volts to +0.2 volts. The pulsed differential input and corresponding output are shown in Figure 10. The response is seen to rise exponentially to the HIGH voltage of 5 volts and to fall exponentially to the LOW voltage of 0.08 volts, as expected from the static characteristic of Figure 6(c).

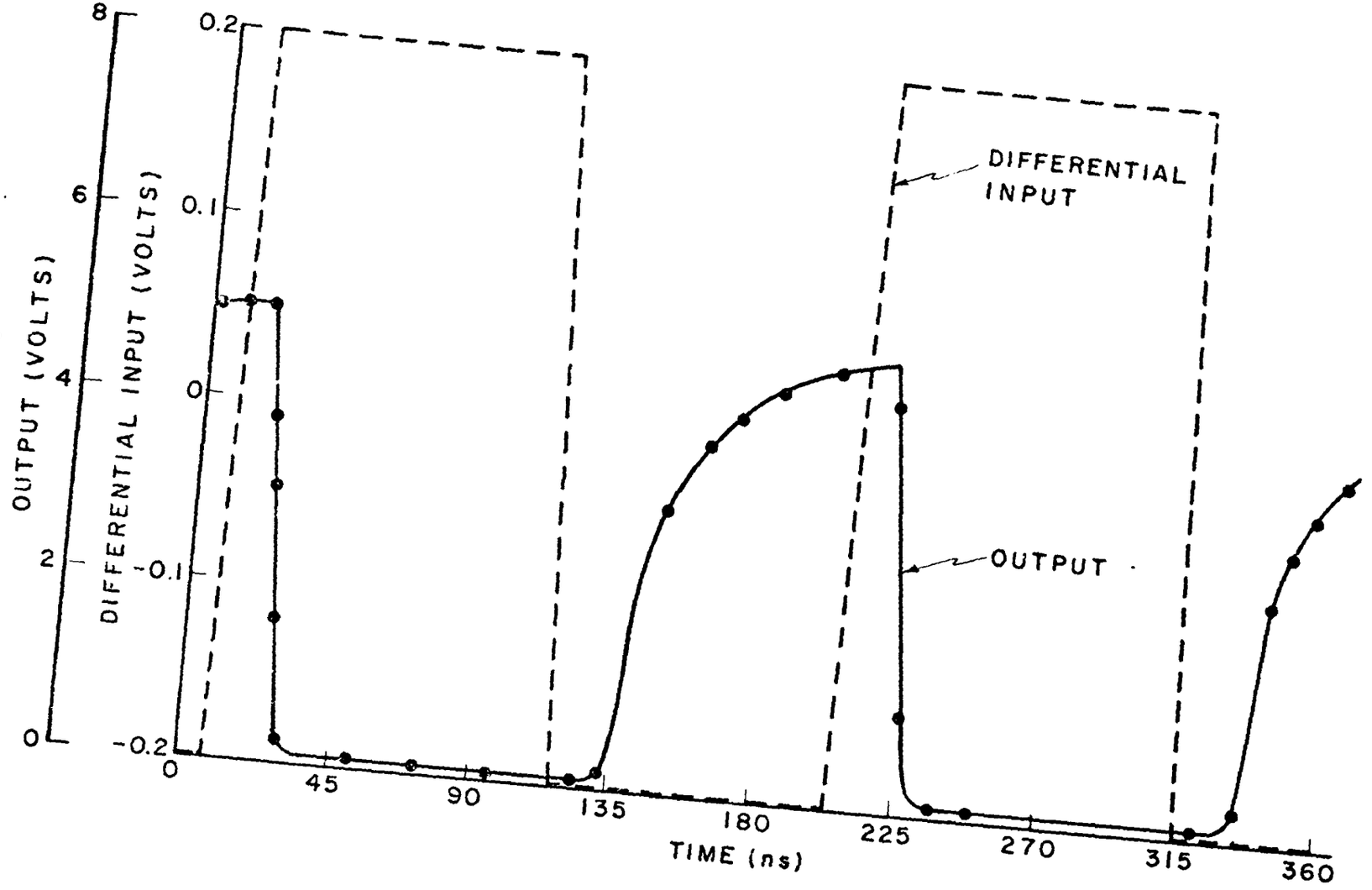


Figure 10. Response of line receiver to pulsed differential input.

The differential input was then changed to a sinusoidal waveform. The input frequency was increased until the output voltage was unable to switch between the HIGH and LOW voltages of 5 and 0.08 volts, respectively. The maximum frequency for which quasi-stationary behavior was noted was in the vicinity of 4MHz. (The actual value of this frequency varied slightly according to the amplitude of the sinusoid.) The response for a sinusoidal differential input of amplitude 0.5 volts and frequency 4 MHz is presented in Figure 11. At frequencies above 4 MHz, the HIGH output voltage did not reach the 5 volt level and the receiver was no longer considered to behave in a quasi-stationary manner. As an example, the response for a sinusoidal differential input of amplitude 6 volts and frequency 10 MHz is shown in Figure 12 where the maximum HIGH output voltage is approximately 4.3 volts.

B. Input Impedance

As can be determined from the curve of Figure 2(c), the input impedance of the line receiver at low frequencies is approximately 4000 ohms. A plot of the magnitude of the input impedance as a function of frequency, obtained using the SPICE computer program, is presented in Figure 13. Identical impedance plots were obtained with both positive and negative differential inputs applied to the input. Observe that the 3dB-point of the impedance magnitude curve occurs at a frequency of approximately 50 MHz.

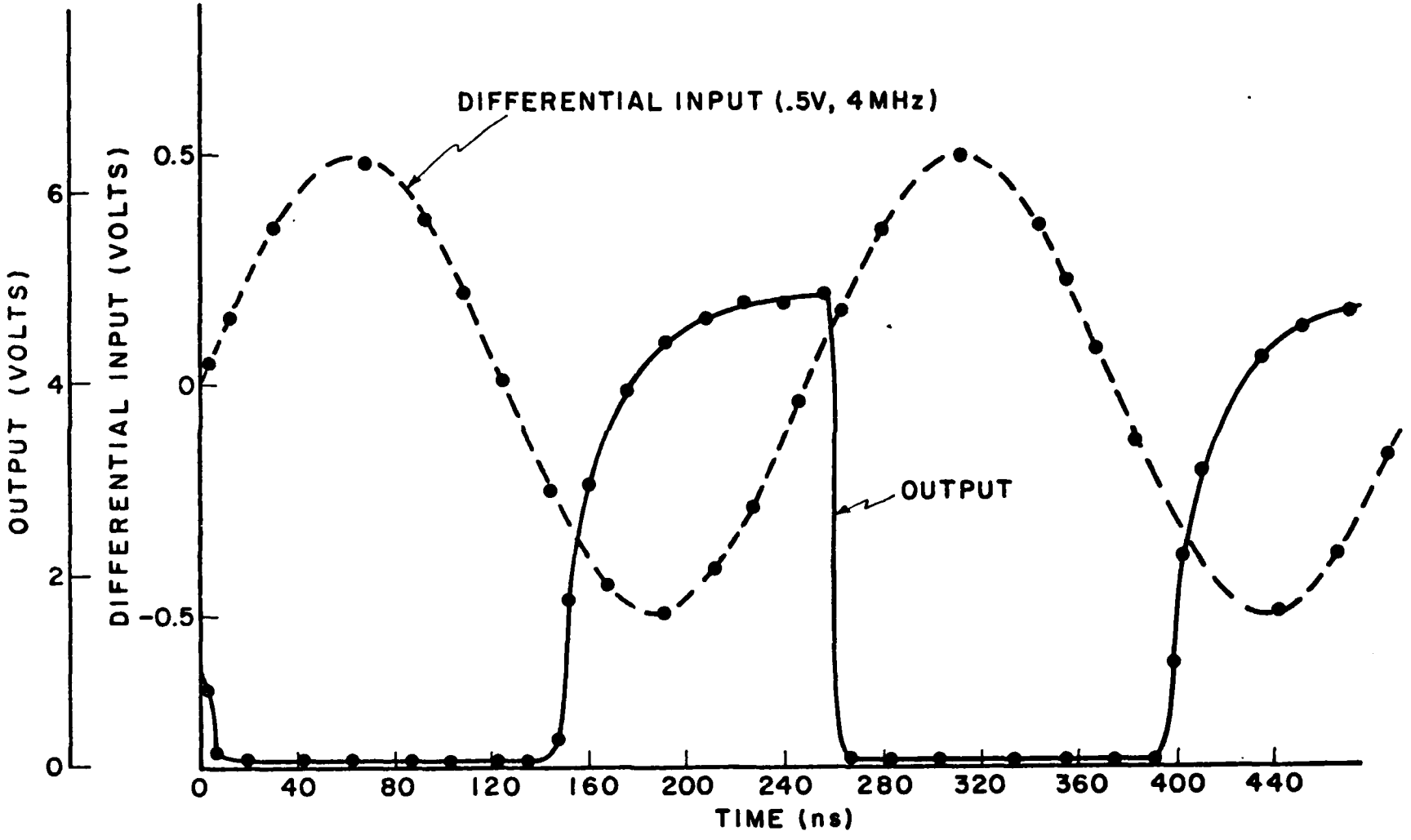


Figure 11. Response of line receiver to sinusoidal differential input of amplitude 0.5 volts and frequency 4 MHz.

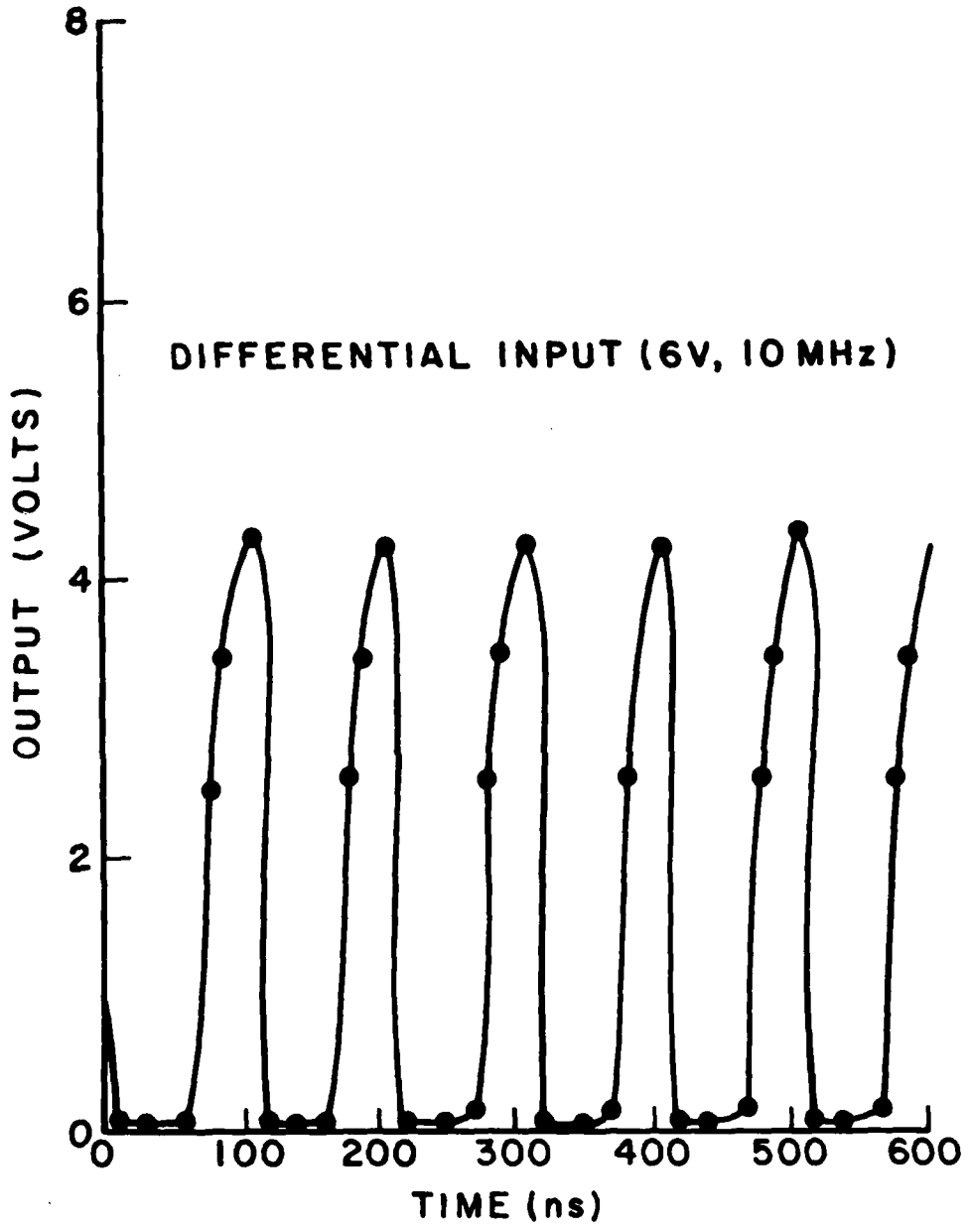


Figure 12. Response of line receiver to sinusoidal differential input of amplitude 6 volts and frequency 10 MHz.

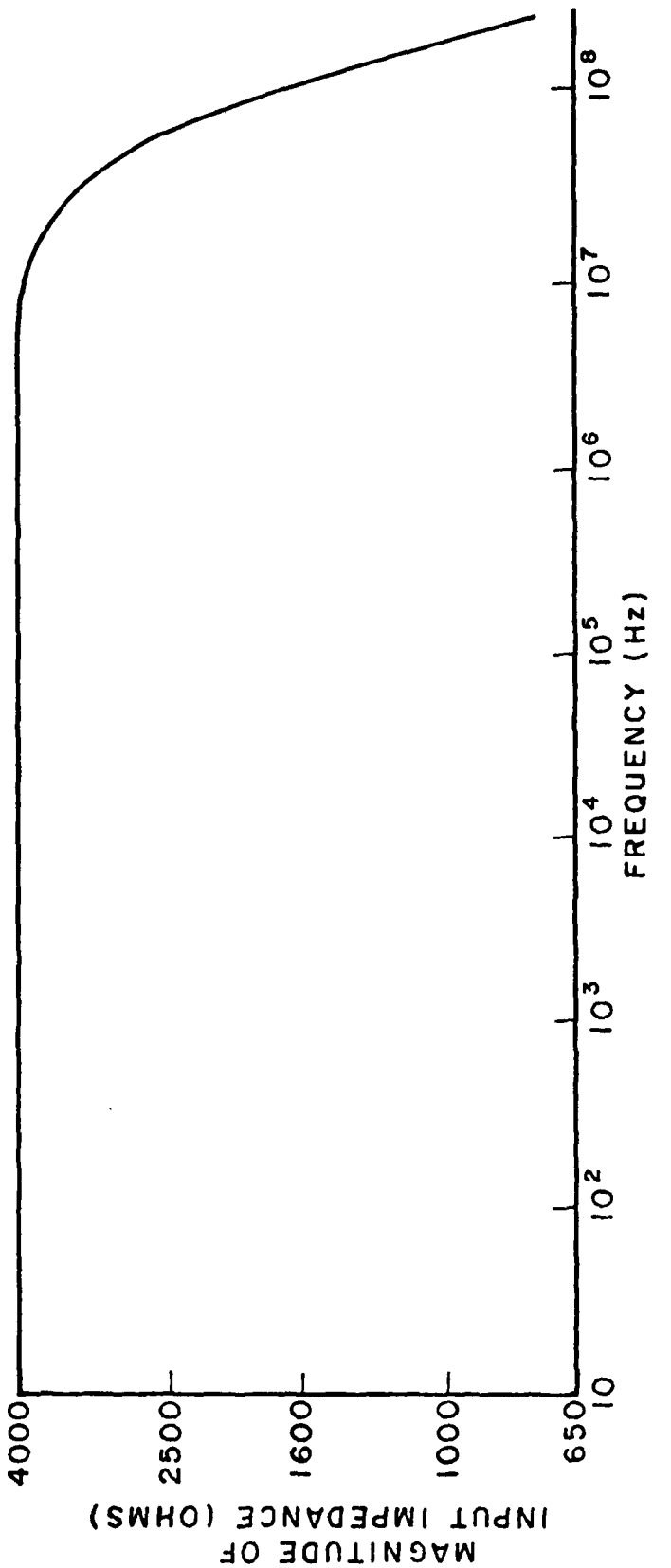


Figure 13. Magnitude of input impedance as a function of frequency.

C. Common-mode Interference

To investigate the effect of common-mode interference, a constant differential signal was applied between the two inputs A and B. Depending upon the polarity of the differential signal, the receiver output was caused to be either HIGH or LOW. Two identical sinusoidal signals were then applied as common-mode voltages to each input. The test circuit used in the computer simulation is given in Figure 14. The d.c. generators produced the constant differential input voltage while the a.c. generators provided the common-mode interference.

For a constant value of differential input and a fixed frequency of the sinusoidal common-mode interference, the amplitude of the interference was increased until the receiver output began to change from the output state dictated by the differential input. The simulation was repeated both for various values of the differential input and for different frequencies of the common-mode interference. The results for positive values of the differential input voltage, where the output is supposed to remain LOW, are shown in Figure 15. On the vertical axis is plotted the minimum amplitude of the sinusoidal common-mode interference needed to cause the receiver output to rise from the LOW region. Note, for a constant frequency, that this amplitude is fairly insensitive to the size of the differential input voltage. Also, the minimum amplitude required increases as the frequency is decreased. Computer runs were also made for a frequency of 500 KHz. The results

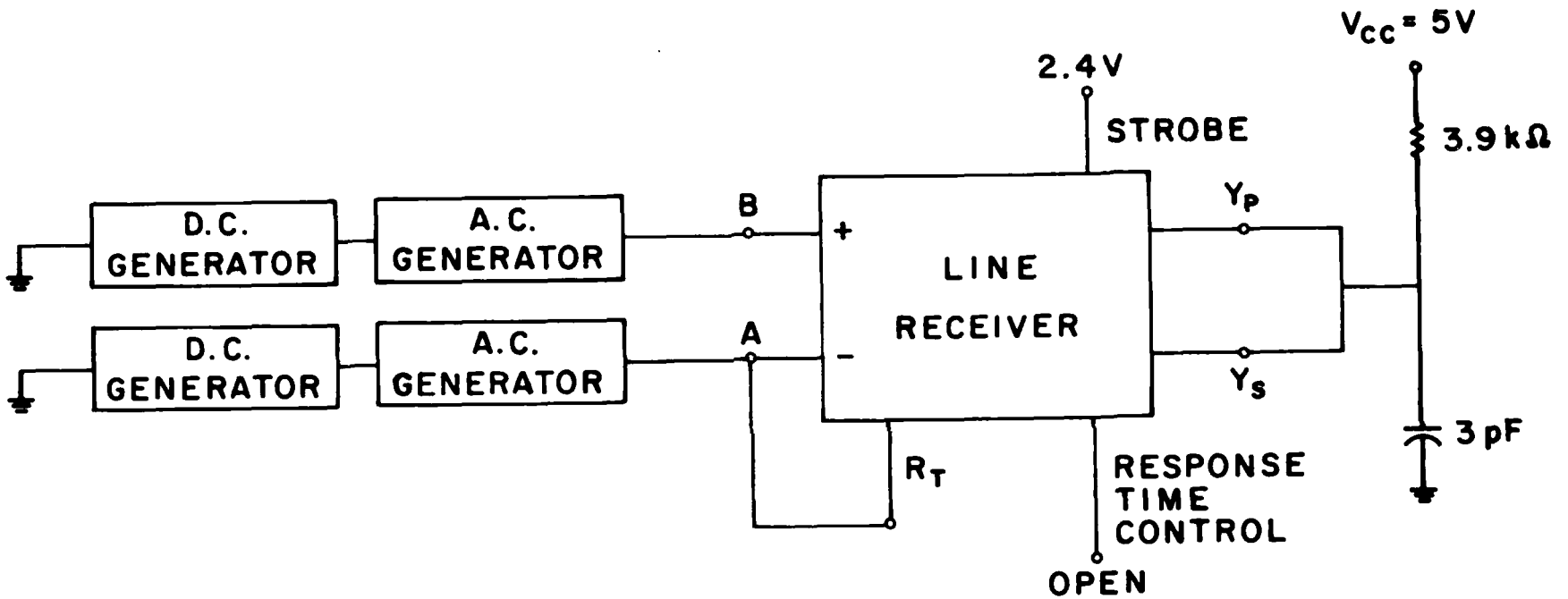


Figure 14. Test circuit used in computer simulation of common-mode interference.

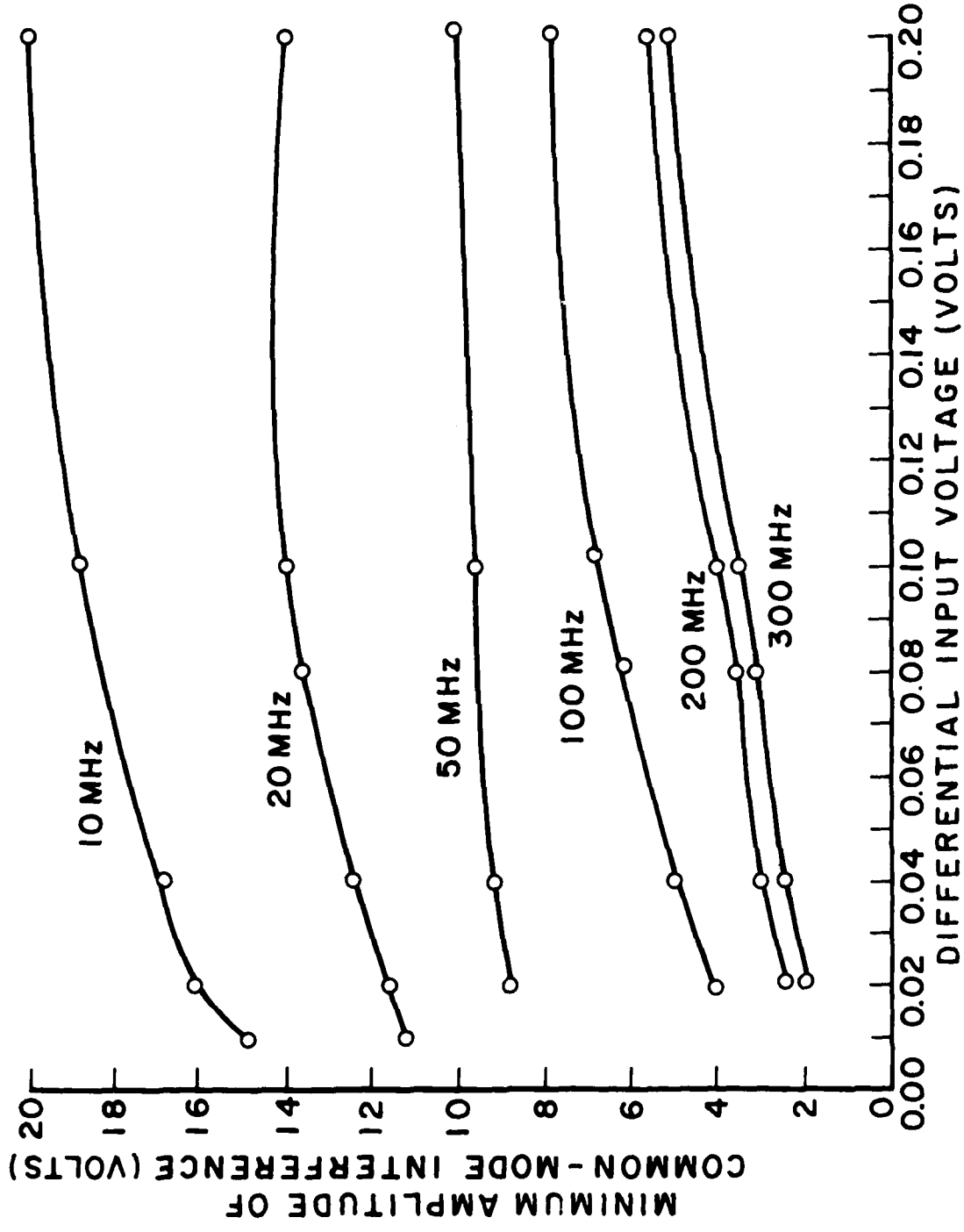


Figure 15. Minimum amplitude of the sinusoidal common-mode interference required to cause the receiver output to rise from the LOW region with positive differential inputs.

are not shown in Figure 15 because amplitudes in excess of 35 volts failed to cause departures from the LOW state. As an example, the response for a differential input of +0.1 volts with common-mode interference having an amplitude of 36 volts and a frequency of 500 KHz is shown in Figure 16. Note that the output voltage remains in the LOW region at a value slightly smaller than the nominal value of 0.08 volts. Figure 17 shows the results for negative values of the differential input, where the receiver output is supposed to remain HIGH. Here the minimum amplitude of the sinusoidal common-mode interference needed to cause the receiver output to drop from the HIGH region is plotted on the vertical axis. The trend with respect to decreasing frequency, which was observed in Figure 15, is not followed in Figure 17. At 50 MHz and 100 MHz the minimum amplitudes are larger than those for lower frequencies. (Results at 100 MHz are not shown because amplitudes in excess of 35 volts failed to cause departure from the HIGH state.) Observe that the 500 KHz sinusoid, which was ineffective in producing interference for positive differential inputs, does cause interference with negative differential inputs.

Examples of output waveforms encountered during the computer simulation of common-mode interference are presented in Figures 18-21. In Figures 18 and 19 the outputs remain in the correct state, as dictated by the differential input, while in Figures 20 and 21 the common-mode interference causes the receiver output to vary from

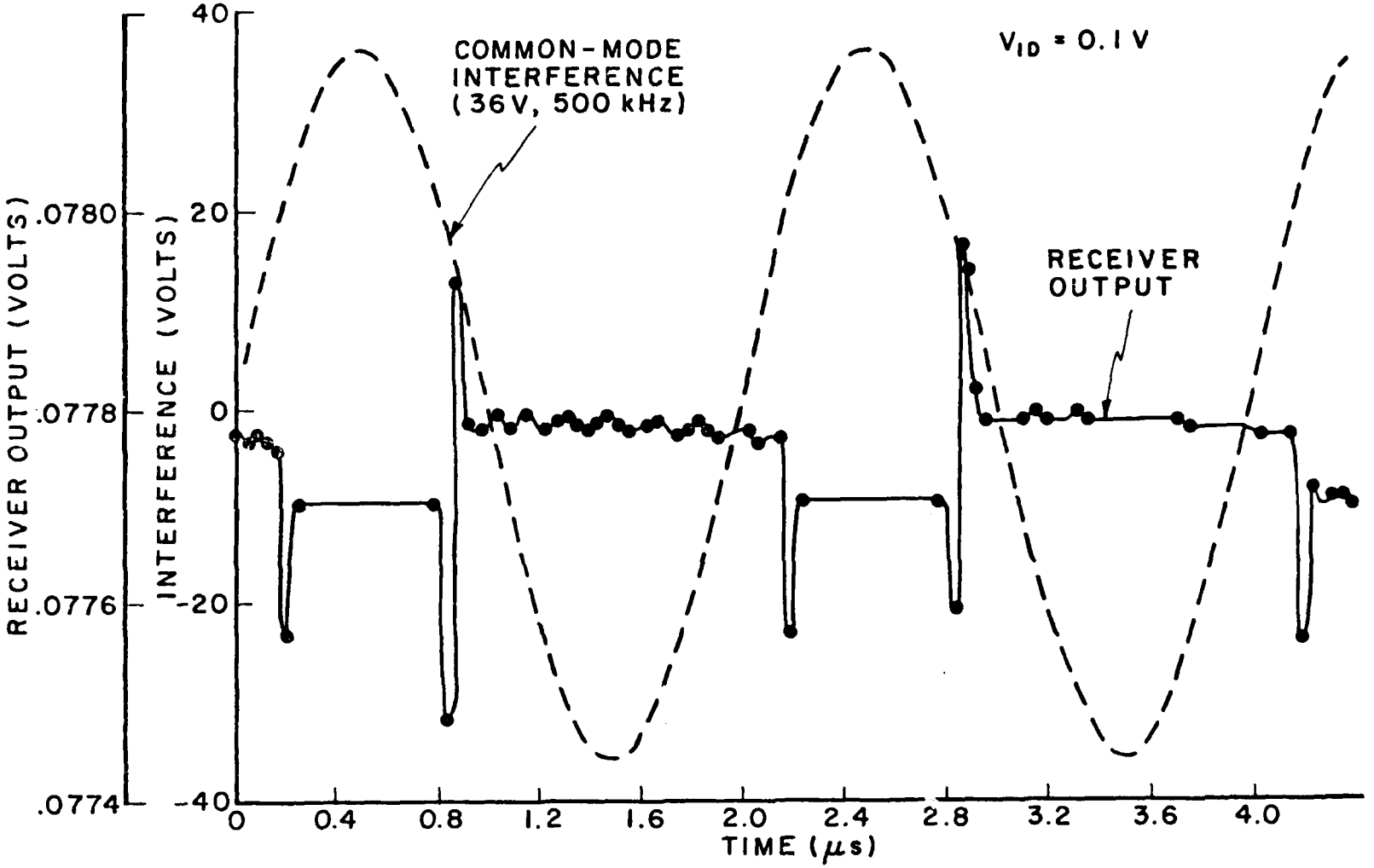


Figure 16. Response for a differential input of +0.1 volts with common-mode interference having an amplitude of 36 volts and a frequency of 500 KHz.

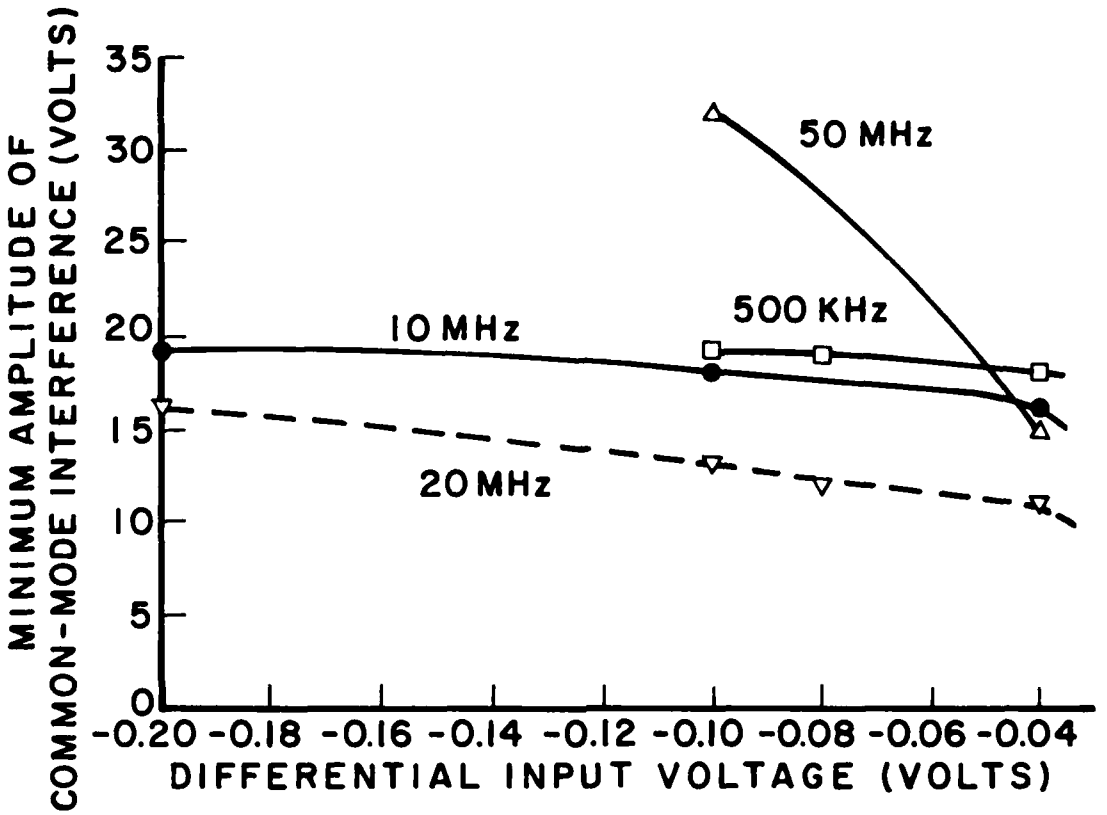


Figure 17. Minimum amplitude of the sinuosidal common-mode interference required to cause the receiver output to drop from the HIGH region with negative differential inputs.

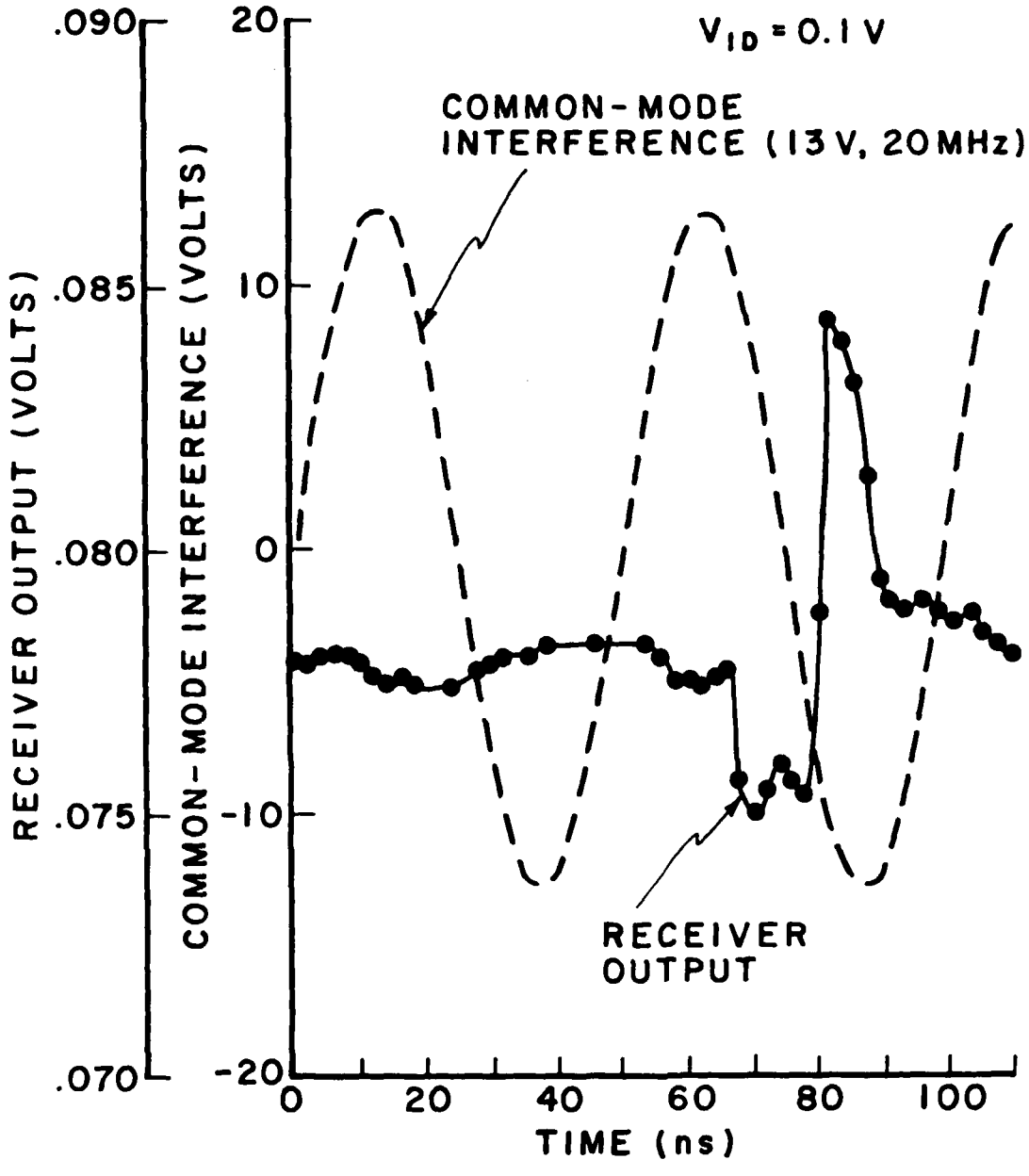


Figure 18. Response for a differential input of +0.1 volts with common-mode interference having an amplitude of 13 volts and a frequency of 20 MHz.

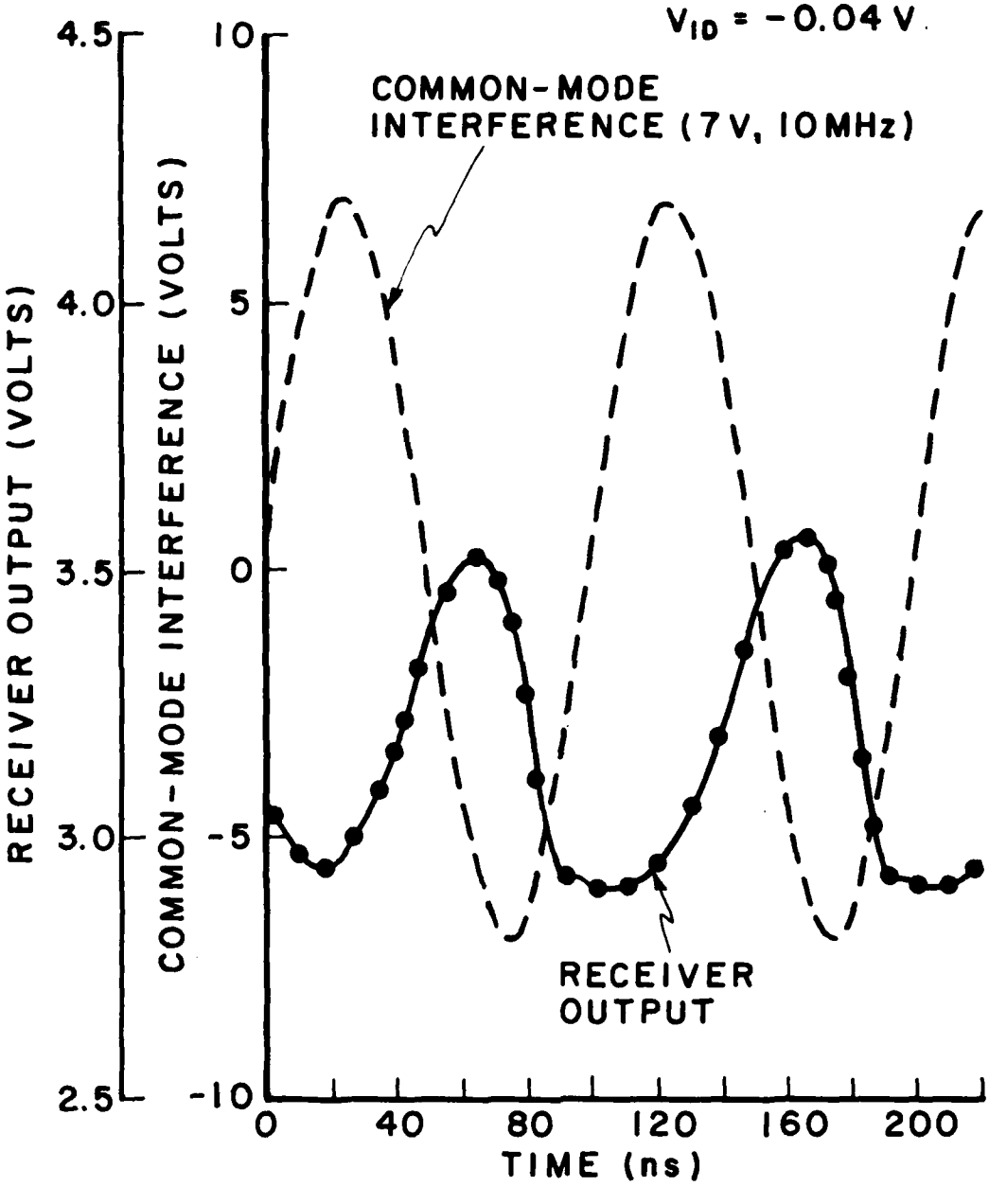


Figure 19. Response for a differential input of -0.04 volts with common-mode interference having an amplitude of 7 volts and frequency of 10 MHz.

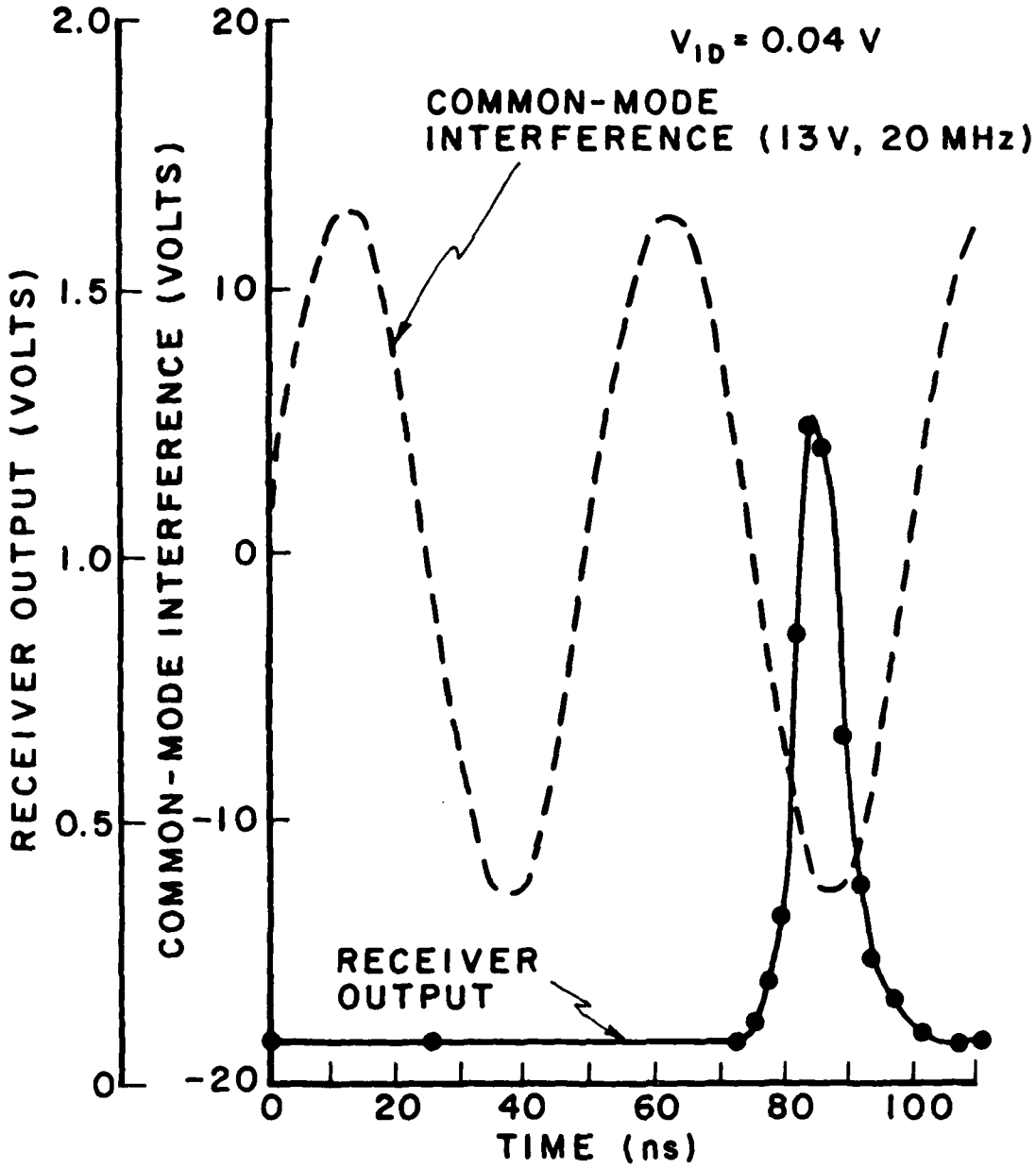


Figure 20. Response for a differential input of 0.04 volts with common-mode interference having an amplitude of 13 volts and frequency of 20 MHz.

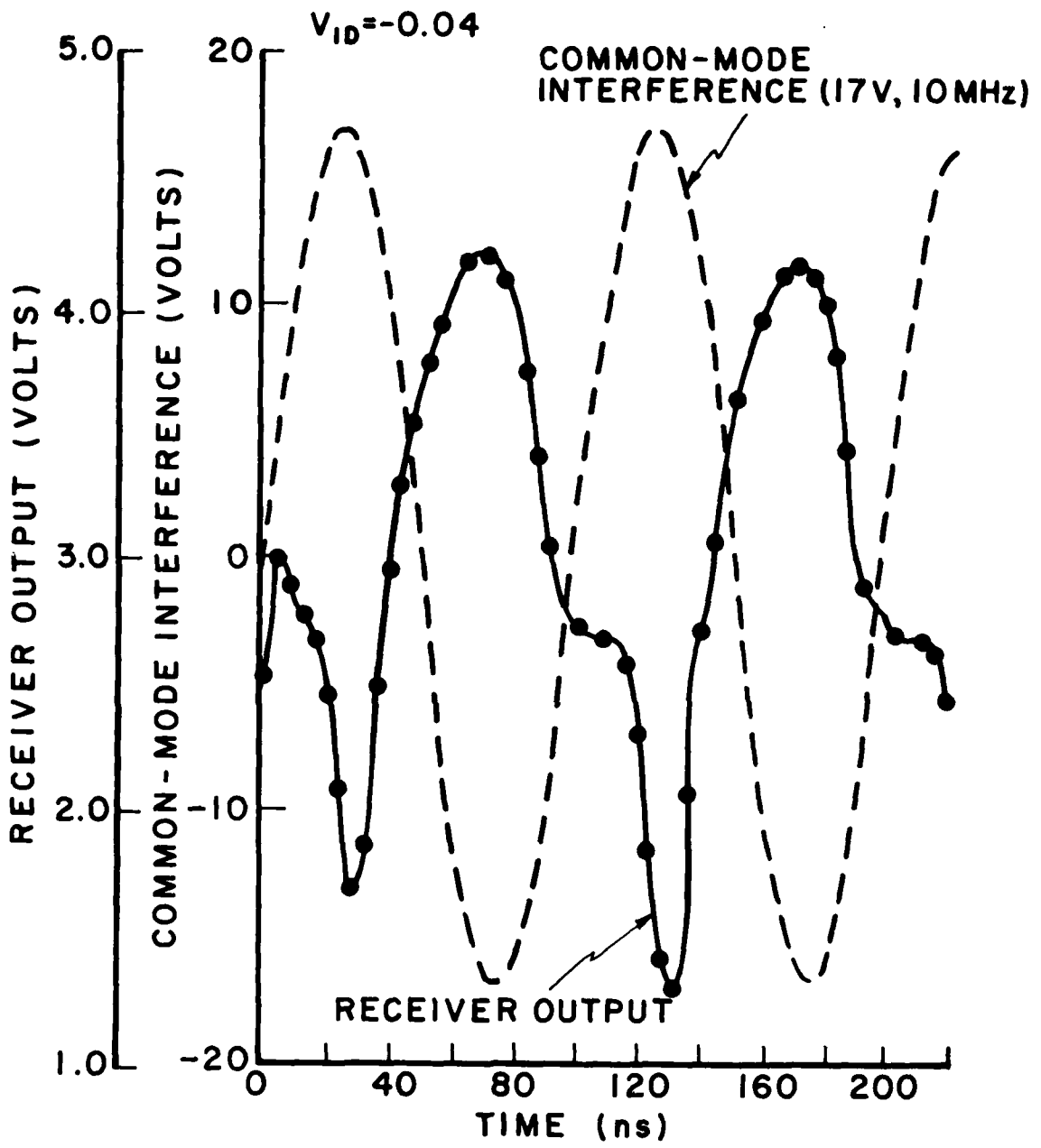


Figure 21. Response for a differential input of -0.04 volts with common-mode interference having an amplitude of 17 volts and frequency of 10 MHz.

the correct state.

D. Differential-mode Interference

The effect of differential-mode interference was investigated by injecting the sinusoidal interferer as a differential signal in series with a differential switching voltage applied to the input port. In the first series of simulations, the differential switching voltage was abruptly changed from -0.2 volts to +0.2 volts. In the absence of interference, this causes the receiver output to switch from the HIGH to LOW states. When interference was applied, severe distortion of the output waveform was noted as a function of the amplitude and frequency of the interferer.

If the amplitude of the interferer is held constant, various cases arise as the interferer frequency is increased in value. These cases are now discussed for an interferer amplitude of 6 volts. At frequencies below 4 MHz, the receiver behaves in a quasi-stationary manner and the output switches between the HIGH and LOW states as would be predicted by the static differential input-output characteristic of Figure 6(c). For frequencies between 4 MHz and 40 MHz, the output is almost periodic. However, the maximum amplitude no longer reaches the "predicted" value of 5 volts. This is illustrated in Figure 22 for a sinusoidal interferer having an amplitude of 6 volts and a frequency of 30 MHz. For frequencies between 40 MHz and 110 MHz, a different response was noticed. As illustrated in Figure 23, the receiver output now switched to the desired LOW state in an oscillatory

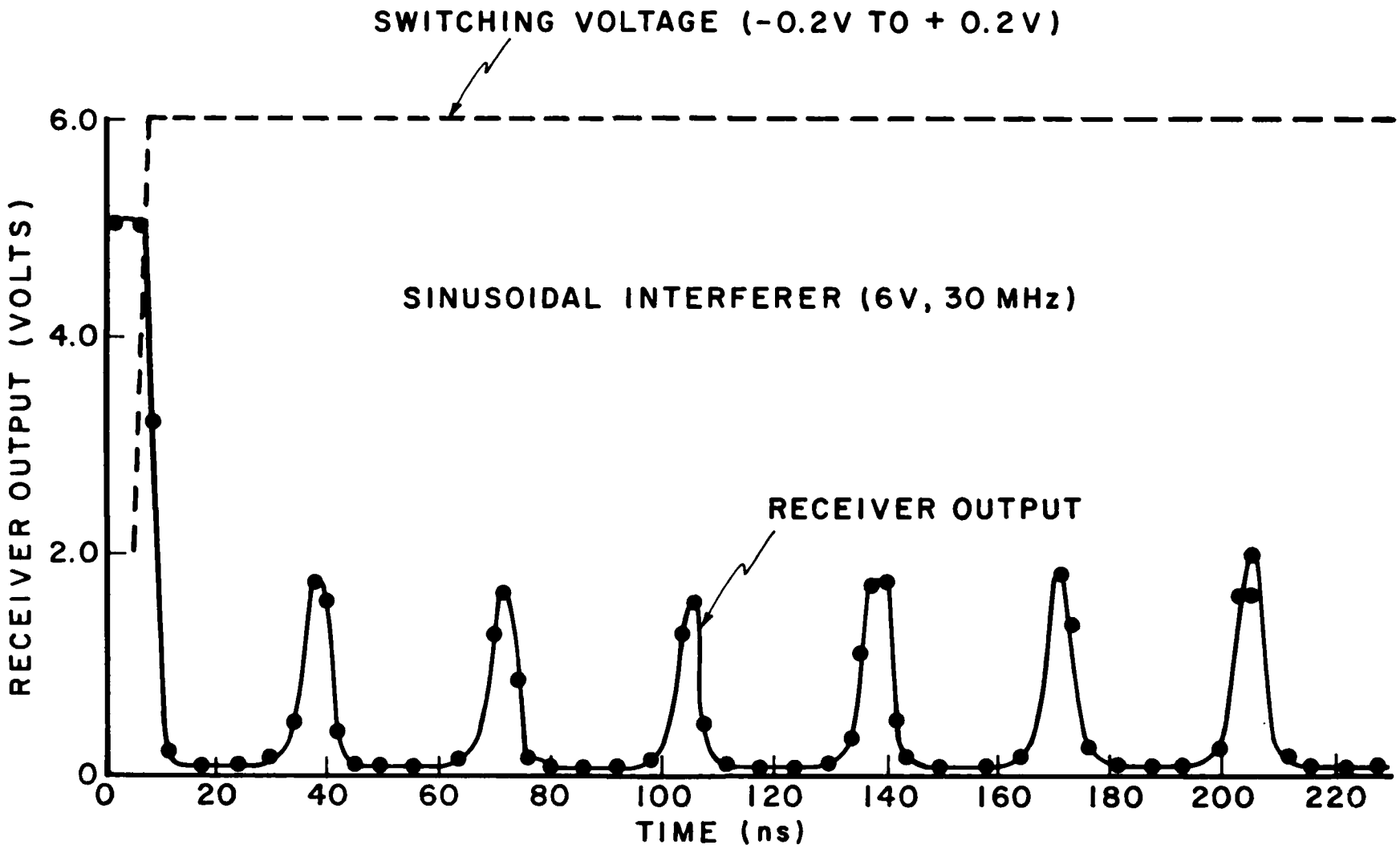


Figure 22. Response for a differential input consisting of a switching voltage (-0.2V to +0.2V) in series with a sinusoidal interferer having an amplitude of 6 volts and a frequency of 30 MHz.

manner. Finally, at frequencies above 120 MHZ, yet another type of response occurred. The output waveform no longer varied from the HIGH state! An example of this case is shown in Figure 24.

Responses of the type shown in Figure 23 can be characterized by the time delay required to switch to the LOW state. This delay is denoted by t_p in Figure 23 and is defined to be the time between the instant at which the switching voltage equals zero volts and the instant beyond which the output waveform remains in the LOW state. The time delay is plotted in Figure 25 as a function of frequency for the case in which the interferer amplitude is 6 volts and the switching voltage switches from -0.2 volts to +0.2 volts. Using the same switching voltage, the investigation was repeated for an interferer amplitude of 2 volts. A similar sequence of responses was observed. However, the various cases arose for a different set of frequency ranges. The time delay is plotted in Figure 26, once again, for the type of response illustrated in Figure 23. Observe that the behavior for 2 volts is very much different from that for 6 volts.

Failure of the output to change state in responses of the type shown in Figure 24 suggest that a shift has occurred in the input voltage threshold, as defined in the discussion of quasi-stationary behavior (see Section 3A). To determine the threshold shift, the step size of the differential switching voltage was

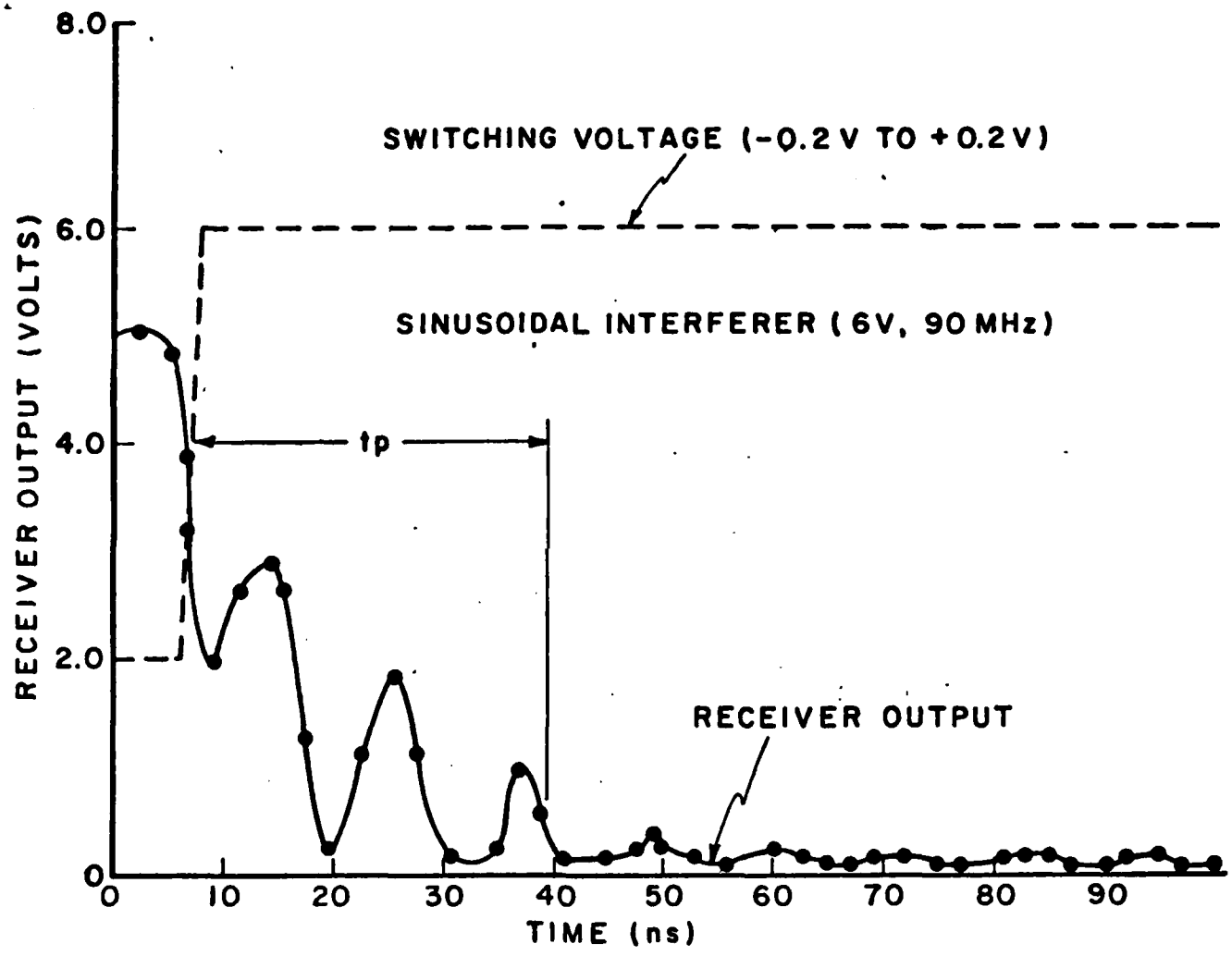


Figure 23. Response for a differential input consisting of a switching voltage (-0.2V to +0.2V) in series with a sinusoidal interferer having an amplitude of 6 volts and a frequency of 90 MHz.

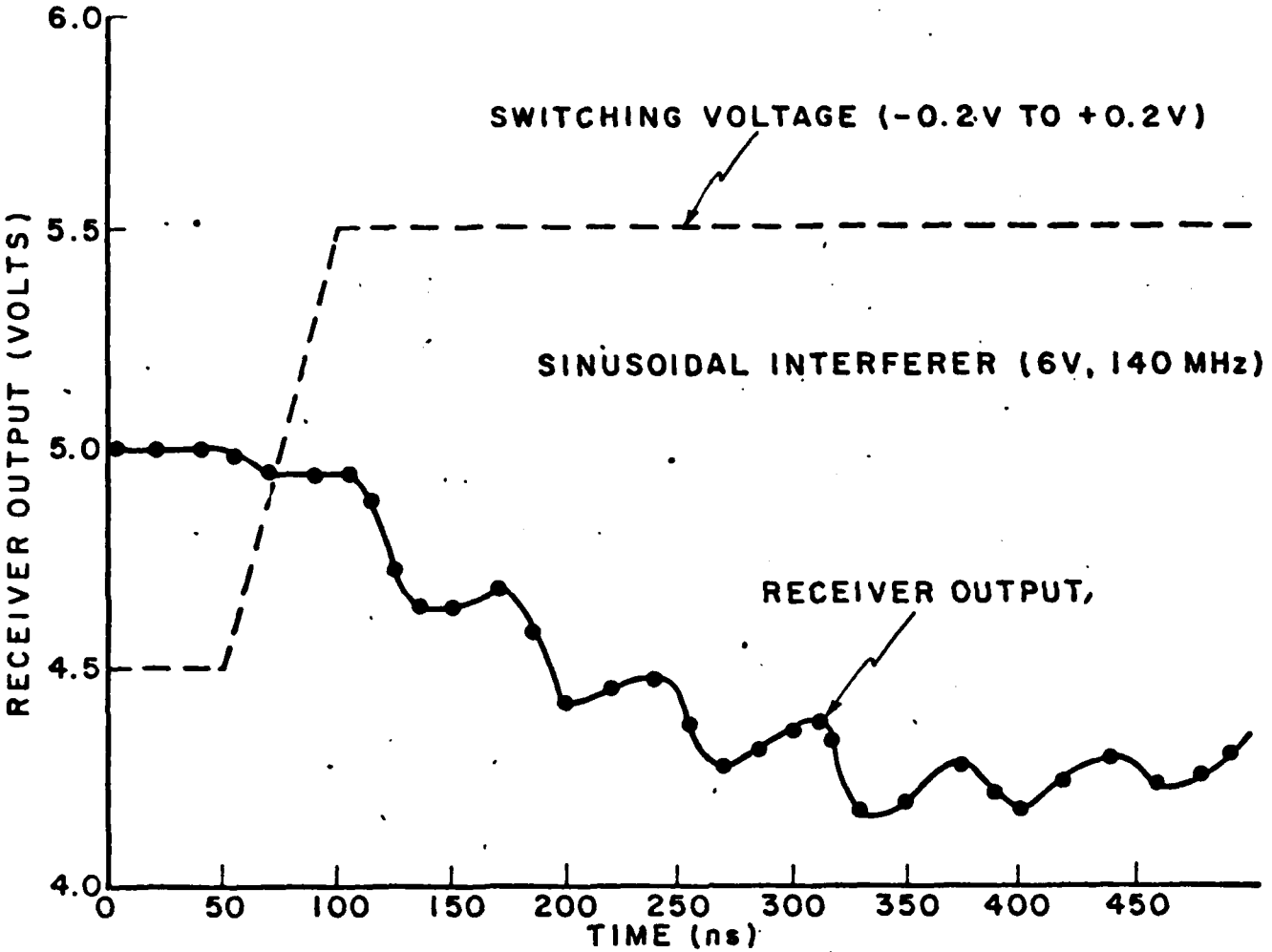


Figure 24. Response for a differential input consisting of a switching voltage (-0.2V to +0.2V) in series with a sinusoidal interferer having an amplitude of 6 volts and a frequency of 140 MHz.

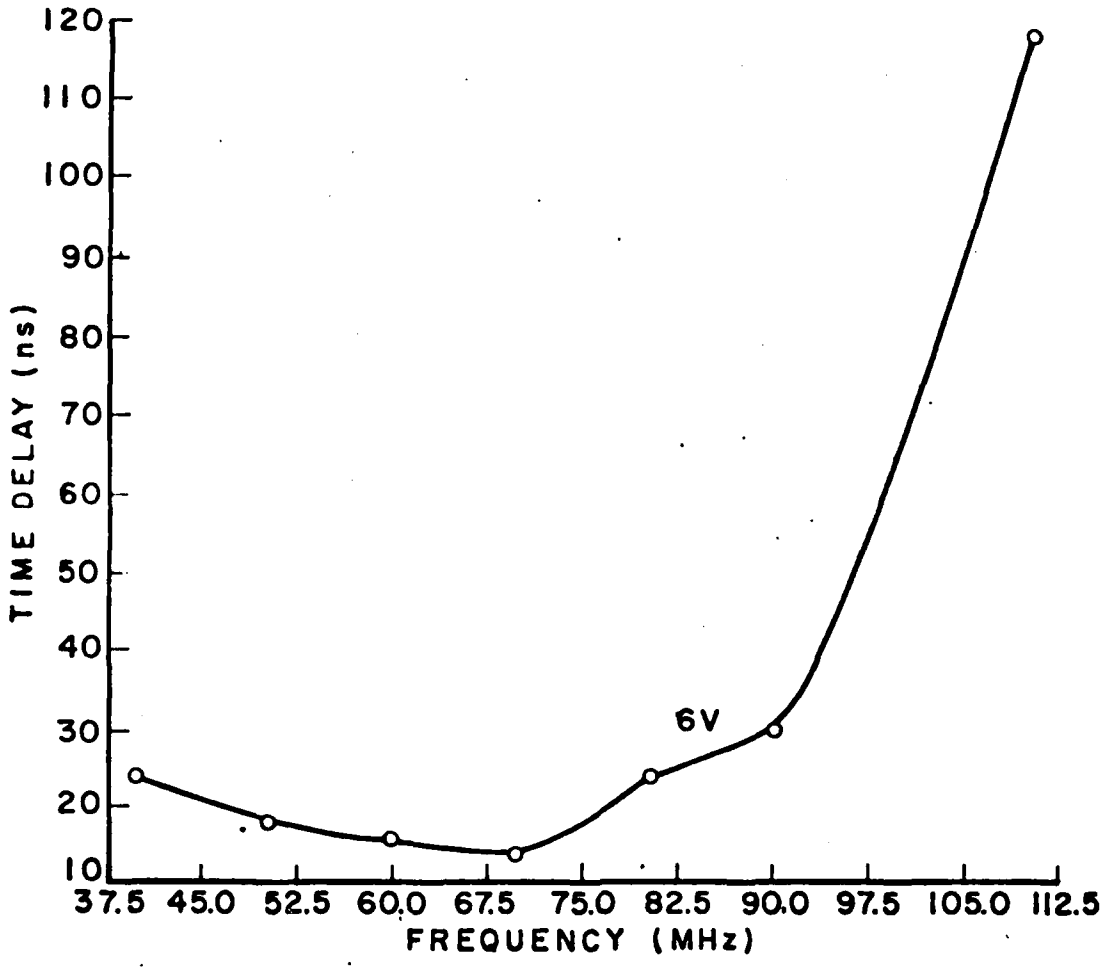


Figure 25. Time delay as a function of frequency for the case in which the interferer amplitude is 6 volts and the switching voltage switches from -0.2 volts to +0.2 volts.

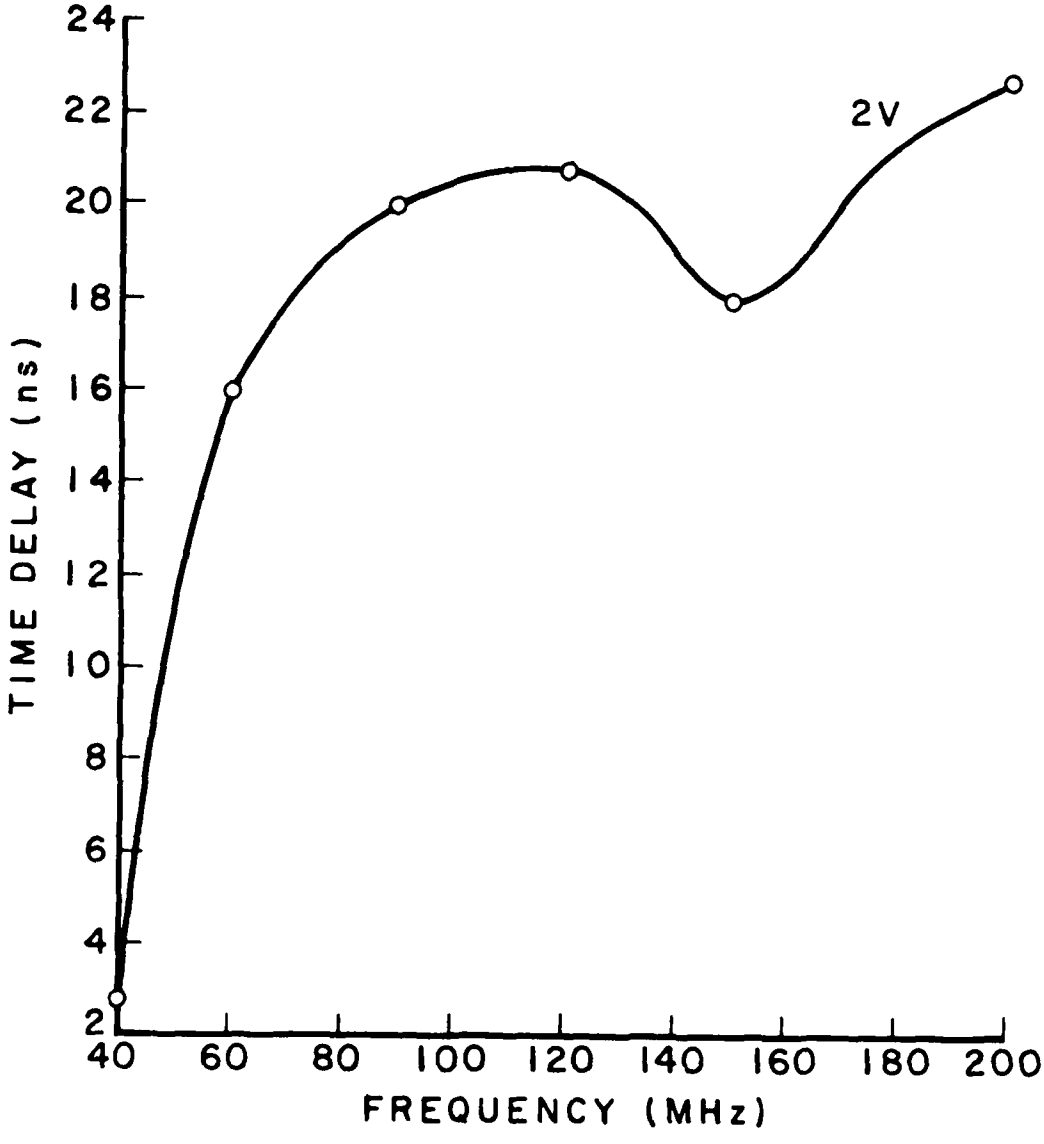


Figure 26. Time delay as a function of frequency for the case in which the interferer amplitude is 2 volts and the switching voltage switches from -0.2 volts to +0.2 volts.

gradually increased in the presence of interference until the receiver output switched from the HIGH to LOW state. This is illustrated by Figures 27 and 28 for a sinusoidal interferer of amplitude 6 volts and frequency 120 MHz. In Figure 27 the switching voltage switched from -0.2 volts to +0.2 volts. However, the receiver output failed to switch to the LOW state. The step size of the switching voltage was then increased until, as shown in Figure 28, the desired transition had occurred with the switching voltage jumping from -0.5 volts to +0.5 volts. From this it was conjectured that the sinusoidal interference had produced an offset in the input voltage threshold from its original value of 0 volts to 0.5 volts. Additional impetus to the conjecture of a threshold shift is provided by the response shown in Figure 29. Initially, the input voltage threshold is at 0 volts. Since the switching voltage begins at 0.1 volts, the receiver output is LOW. As time progresses, the sinusoidal interference causes the input voltage threshold to gradually shift to a value slightly less than 1 volt. Consequently, because the switching voltage remains at 0.1 volts, the receiver output switches to the HIGH state. The switching voltage then switches to a value equal to 1 volt. Since this is just above the new input voltage threshold, the receiver output slowly switches back to the LOW state. The shift in the input voltage threshold was investigated as a function of the interferer frequency with the interferer amplitude held

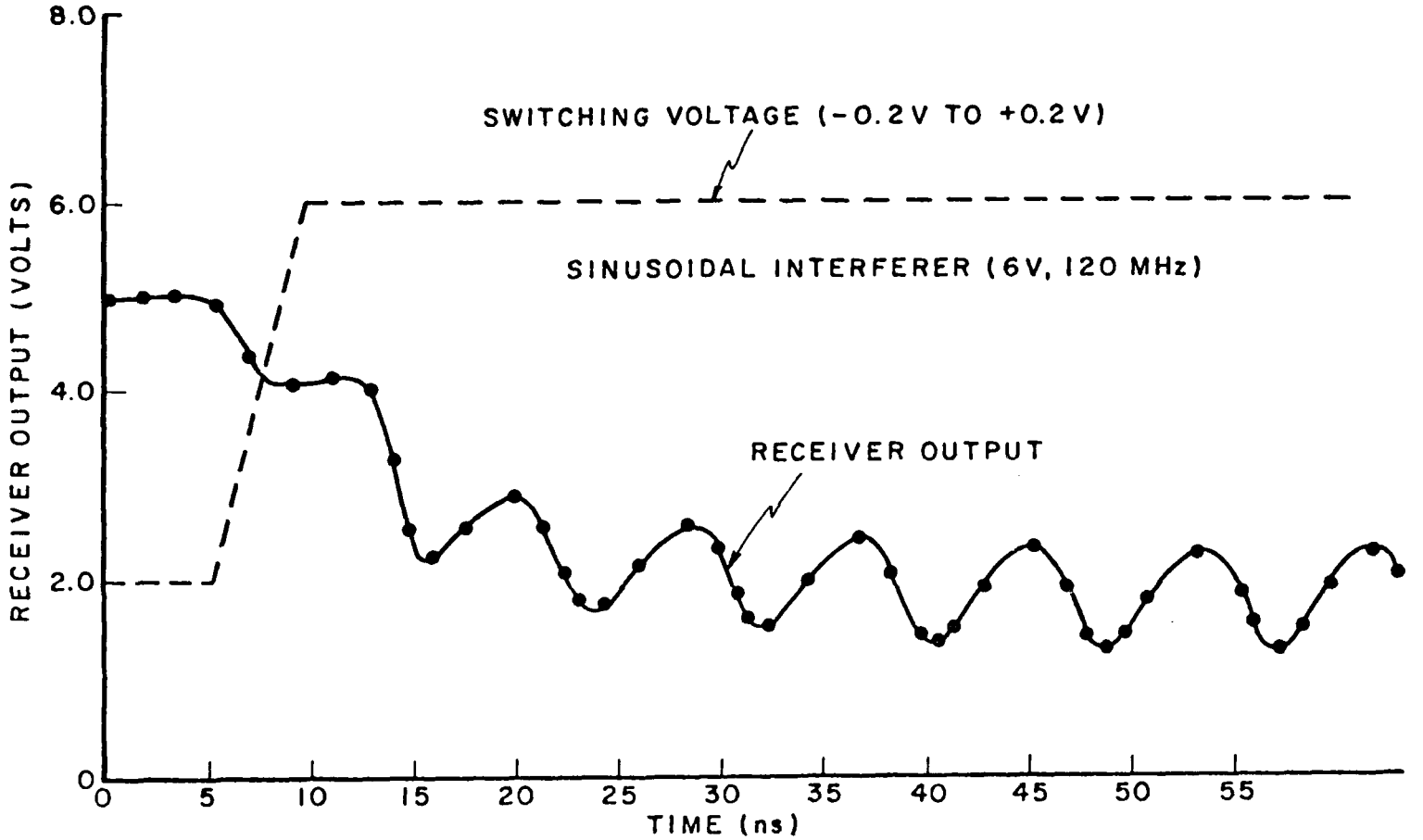


Figure 27. Response for a differential input consisting of switching voltage (-0.2V to +0.2V) in series with a sinusoidal interferer having an amplitude of 6 volts and a frequency of 120 MHz.

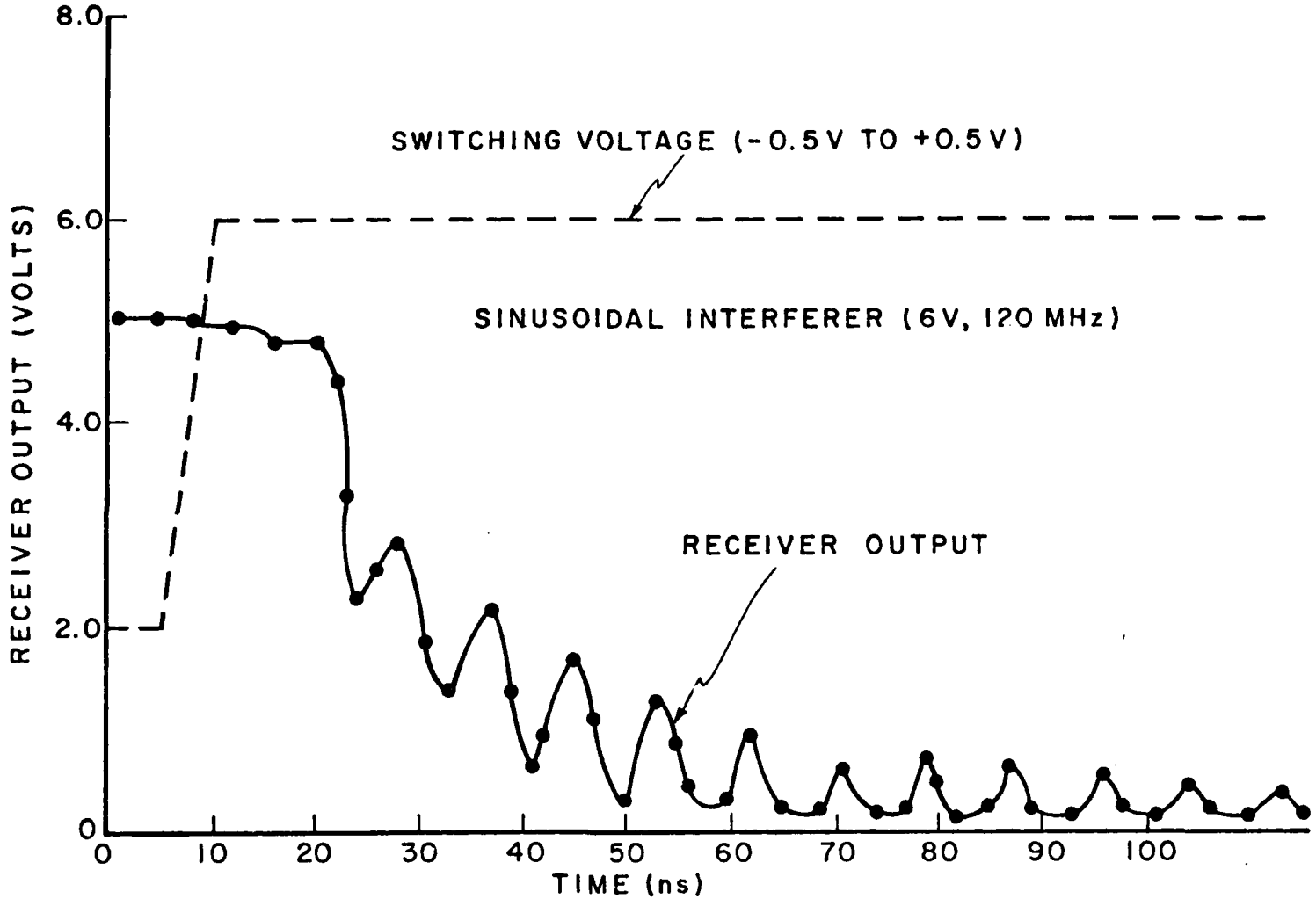


Figure 28. Response for a differential input consisting of a switching voltage (-0.5V to +0.5V) in series with a sinusoidal interferer having an amplitude of 6 volts and a frequency of 120 MHz.

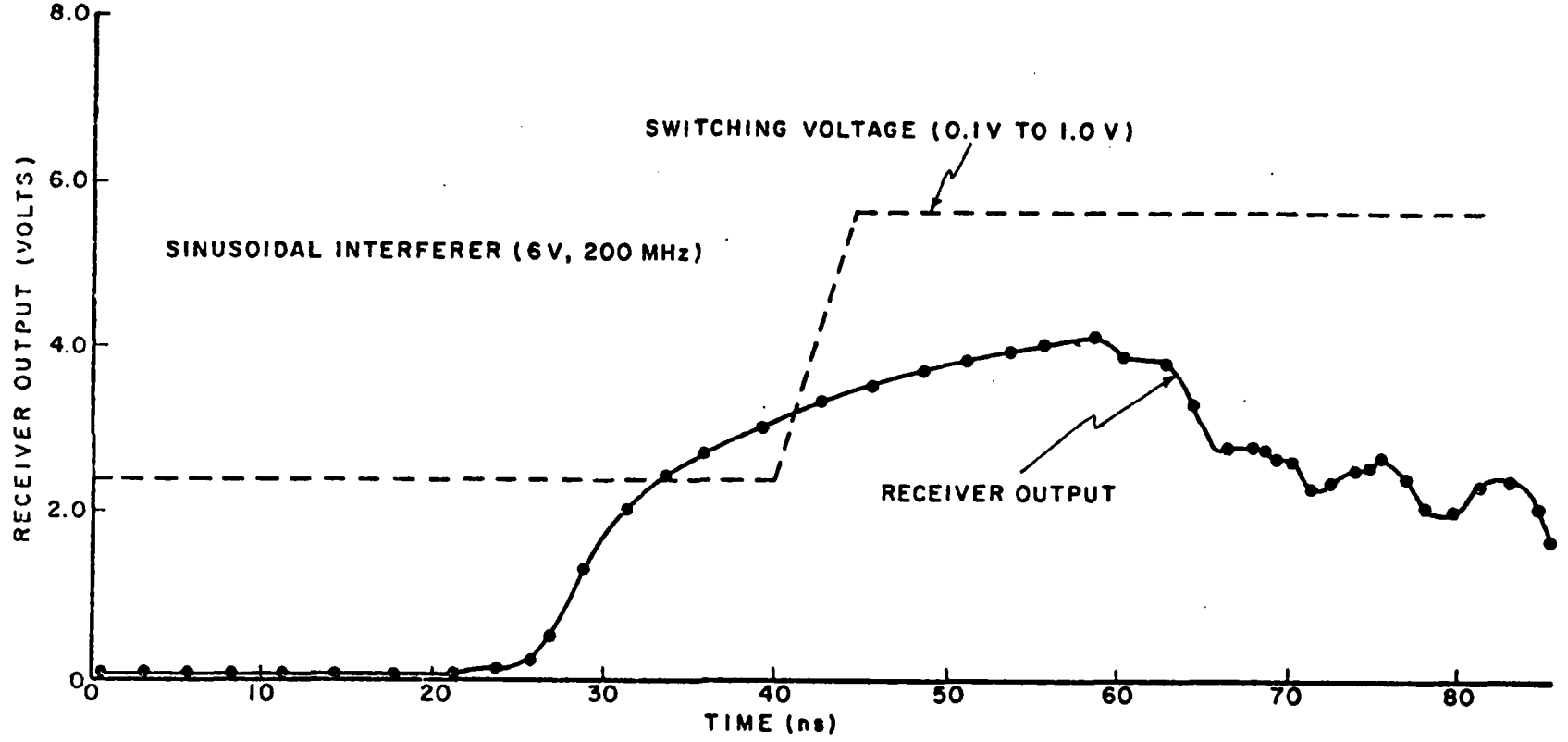


Figure 29. Response for a differential input consisting of a switching voltage (0.1V to 1.0V) in series with a sinusoidal interferer having an amplitude of 6 volts and a frequency of 200 MHz.

constant at 6 volts and the switching voltage going from LOW to HIGH. The results are summarized in Figure 30. The shift in the input voltage threshold is seen to increase with frequency.

In the next series of simulations involving differential-mode interference, the switching voltage was inverted such that it abruptly changed from +0.2 volts to -0.2 volts. In the absence of interference, this caused the receiver output to switch from the LOW to HIGH states. As before, various cases arose as the interferer frequency was increased while the interferer amplitude was held constant at 6 volts. Quasi-stationary behavior was observed for frequencies below 4MHz. For frequencies between 4 MHz and 40 MHz, the output fluctuated between the LOW state and either the HIGH or UNDEFINED regions. Failure of the output to reach the HIGH state suggests the beginning of a threshold offset. For frequencies between 50 MHZ and 80 MHZ, the receiver output remained in the LOW state. This is illustrated by the response in Figure 31. Consequently, the shift in the input voltage threshold has been confirmed. However, in contrast to the previous results, the shift does not increase with frequency. For frequencies between 90 MHZ and 110 MHz, the output, once again, fluctuates between the LOW and HIGH states. Finally, at frequencies above 110 MHz the receiver output switched to the desired HIGH state. This is seen in Figures 32 and 33. As shown in Figure 33, the transition from the LOW to HIGH states is

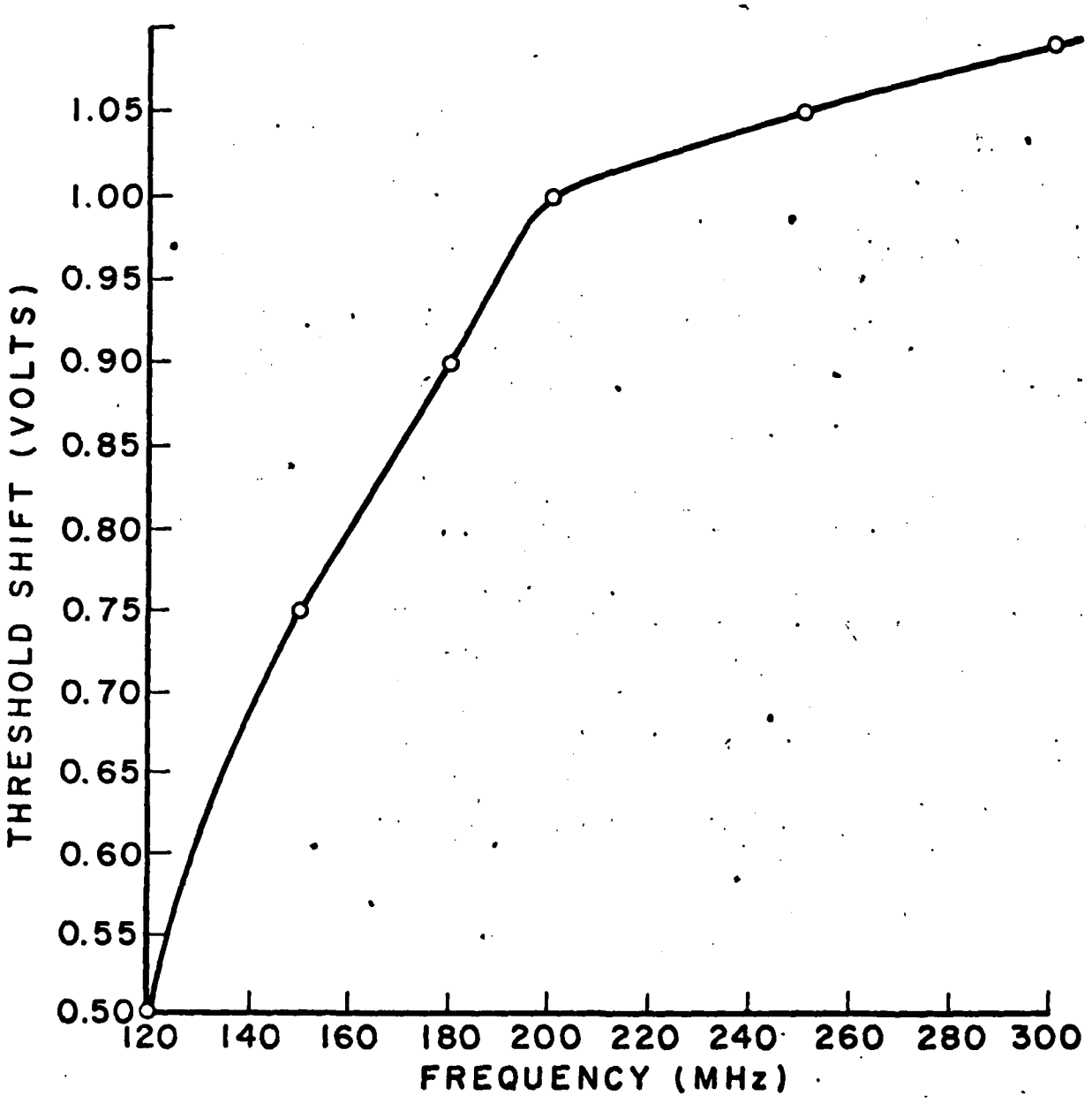


Figure 30. Shift in the input voltage threshold as a function of the interferer frequency with the interferer amplitude held constant at 6 volts and the switching voltage going from LOW to HIGH.

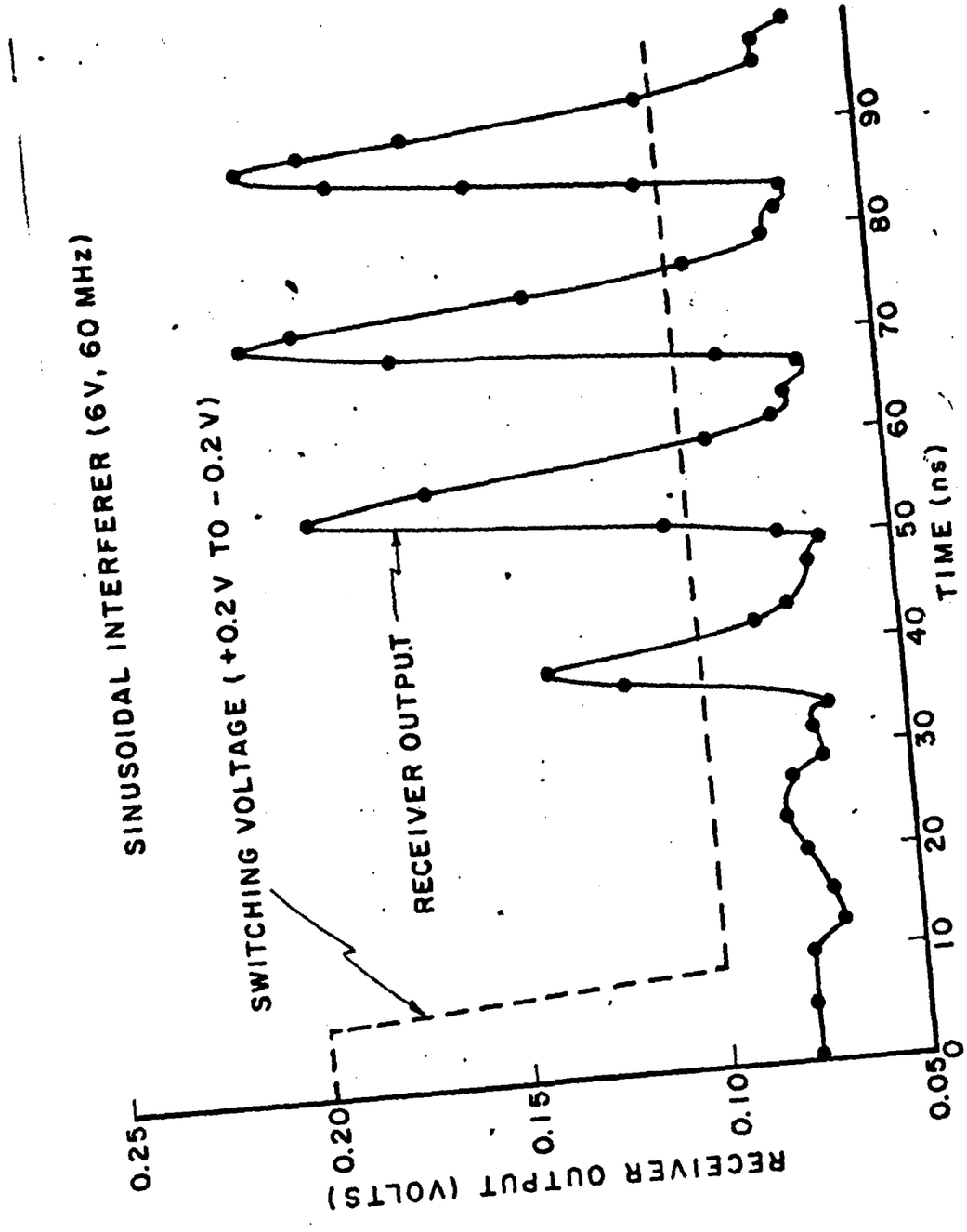


Figure 31. Response for a differential input consisting of a switching voltage (+0.2V to -0.2V) in series with a sinusoidal interferer having an amplitude of 6V and a frequency of 60 MHZ.

extremely smooth for frequencies of 150 MHz and above. The time delay for those cases in which the output switched to the HIGH state is presented in Table 1. The line receiver is seen to respond differently depending upon the polarity of the swtiching voltage.

Table 1

Time Delay, t_p

Frequency (MHz)	Delay (nS)
120	51
130	35
140	31
145	30
150	29

Finally, a study was made of the receiver sensitivity to sinusoidal interference injected as a differential signal. In Figure 34, as a function of frequency, is plotted the minimum interferer amplitude required to cause improper switching of the receiver output when the differential input consists of a sinusoidal interferer in series with a switching voltage which transitions from -0.2V to +0.2V. At low frequencies the minimum required amplitude is approximately 0.2 volts as would be expected from quasi-stationary behavior. However, the receiver is relatively insensitive to differential interference at frequencies between 30 MHz and 50 MHz where considerably larger amplitudes are needed. Above 50 MHz the output did eventually switch

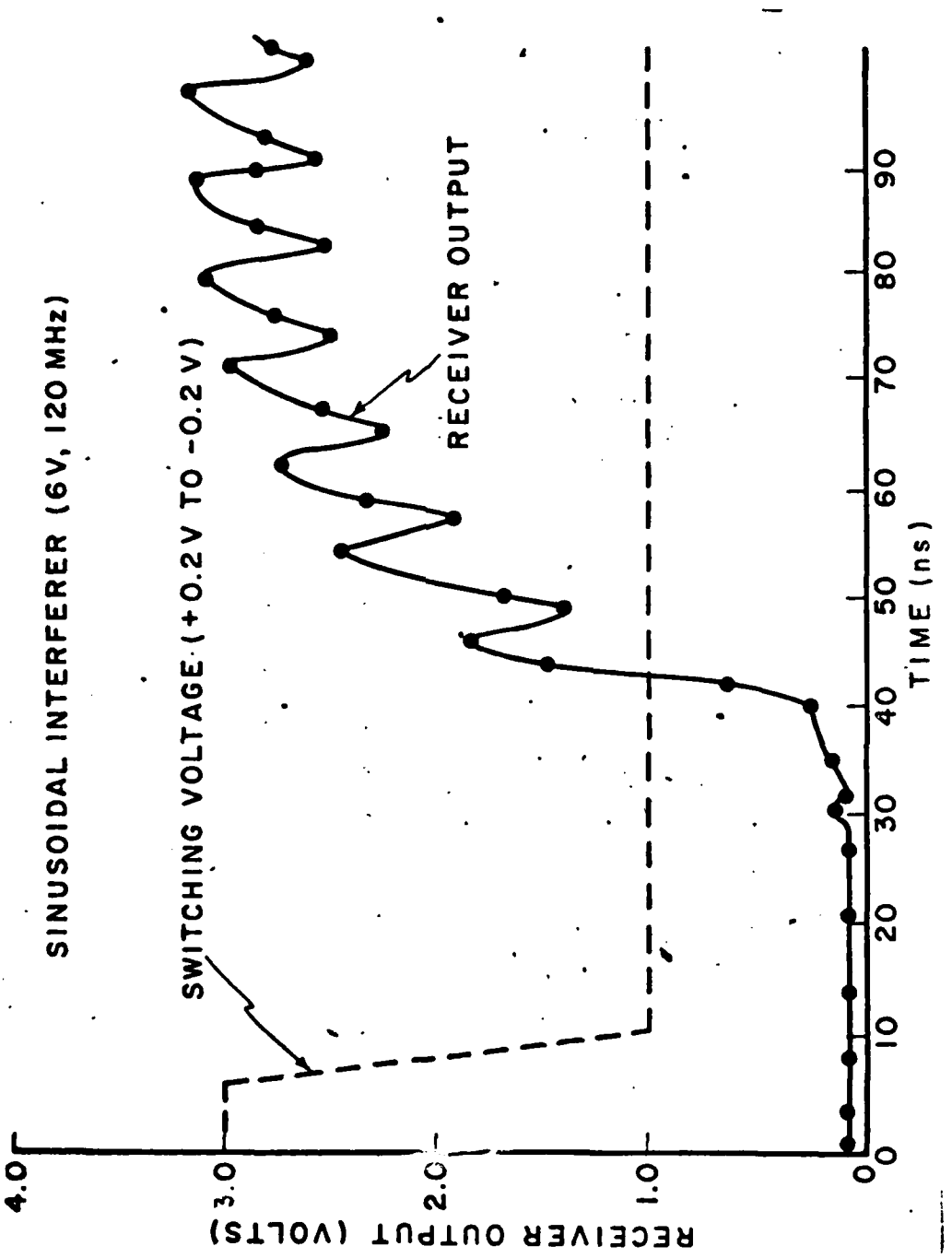


Fig. 32. Response for a differential input consisting of a switching voltage (+0.2V to -0.2V) in series with a sinusoidal interferer having an amplitude of 6 volts and a frequency of 120 MHz.

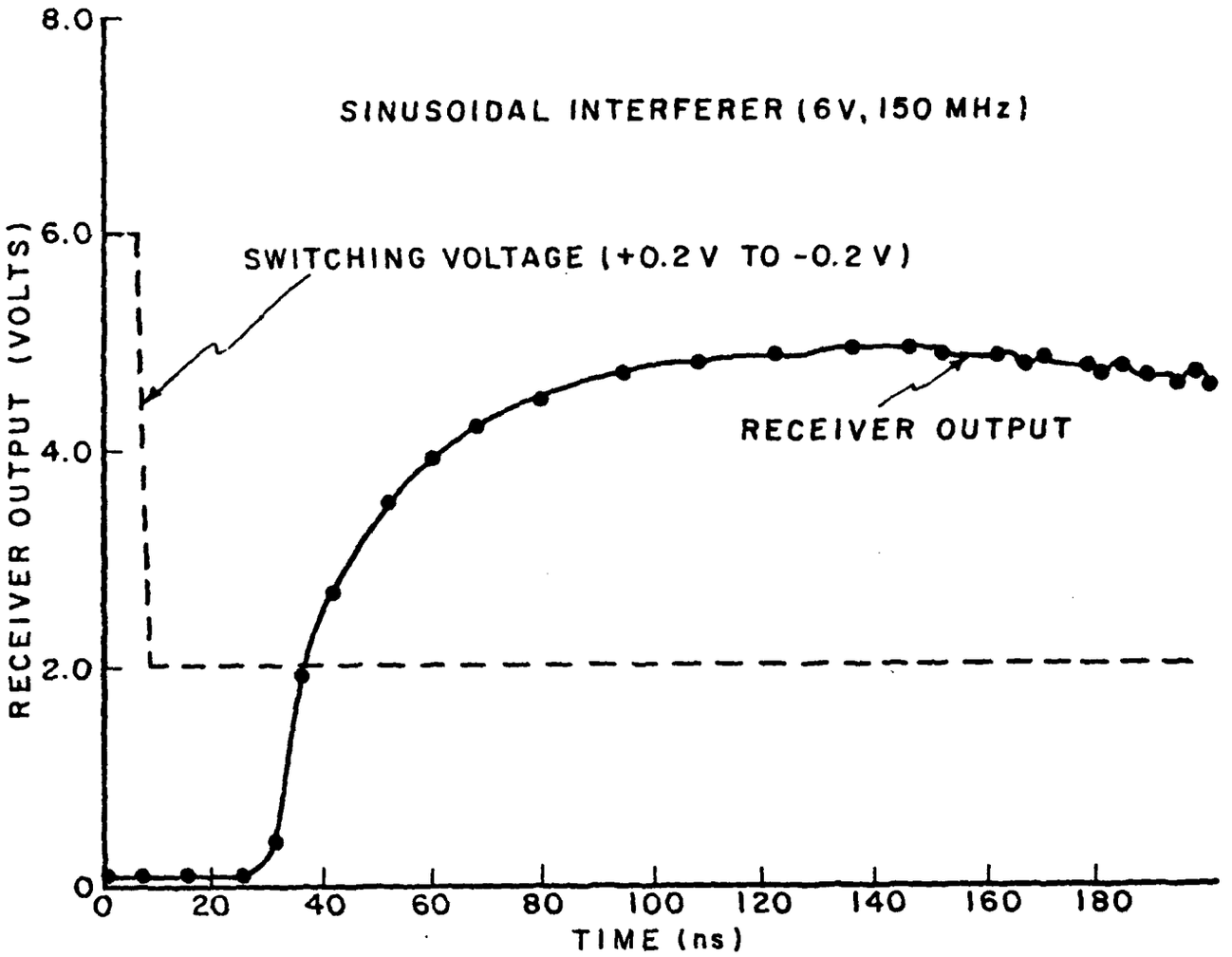


Figure 33. Response for a differential input consisting of a switching voltage (+0.2V to -0.2V) in series with a sinusoidal interferer having an amplitude of 6 volts and frequency of 150 MHz.

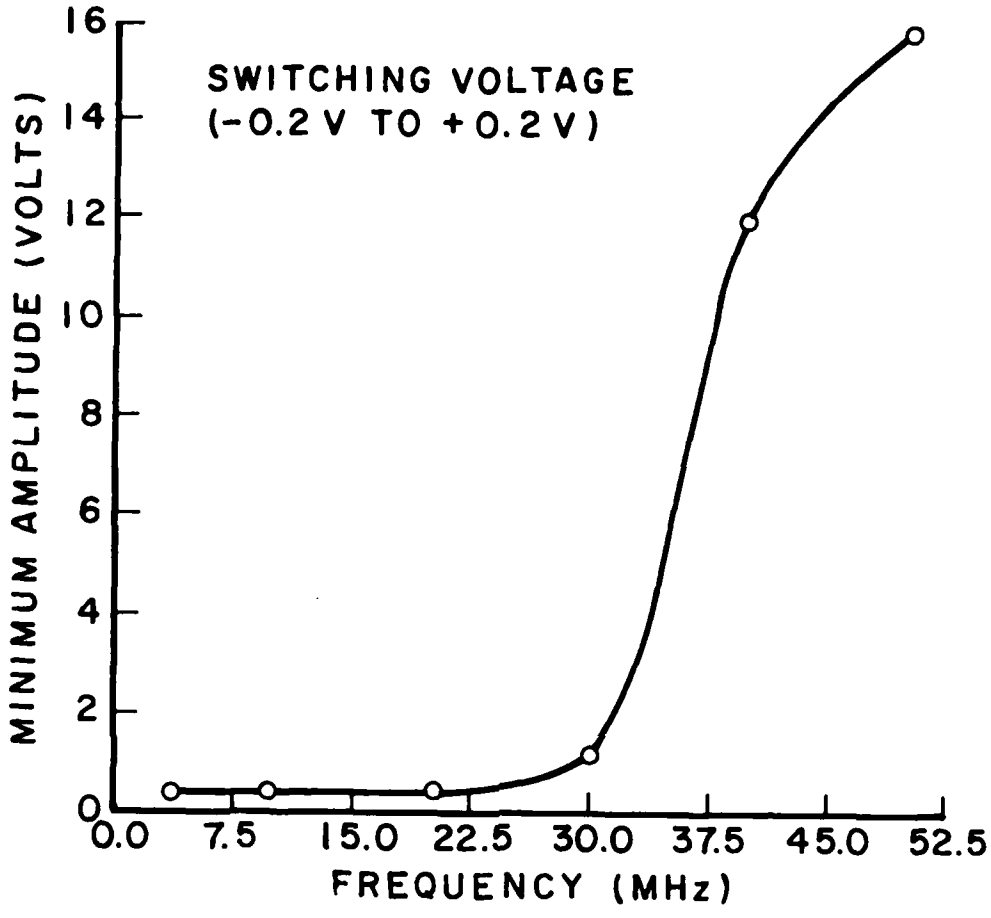


Figure 34. Minimum amplitude of the sinusoidal differential interference, when in series with a -0.2V to +0.2V switching voltage, required to cause improper switching of the receiver output.

to the correct LOW state although the time delay increased with interferer amplitude. The plot of Figure 35 resulted when the polarity of the switching voltage was changed to yield a transition from +0.2V to -0.2V. Observe that the receiver is much more sensitive for this switching voltage.

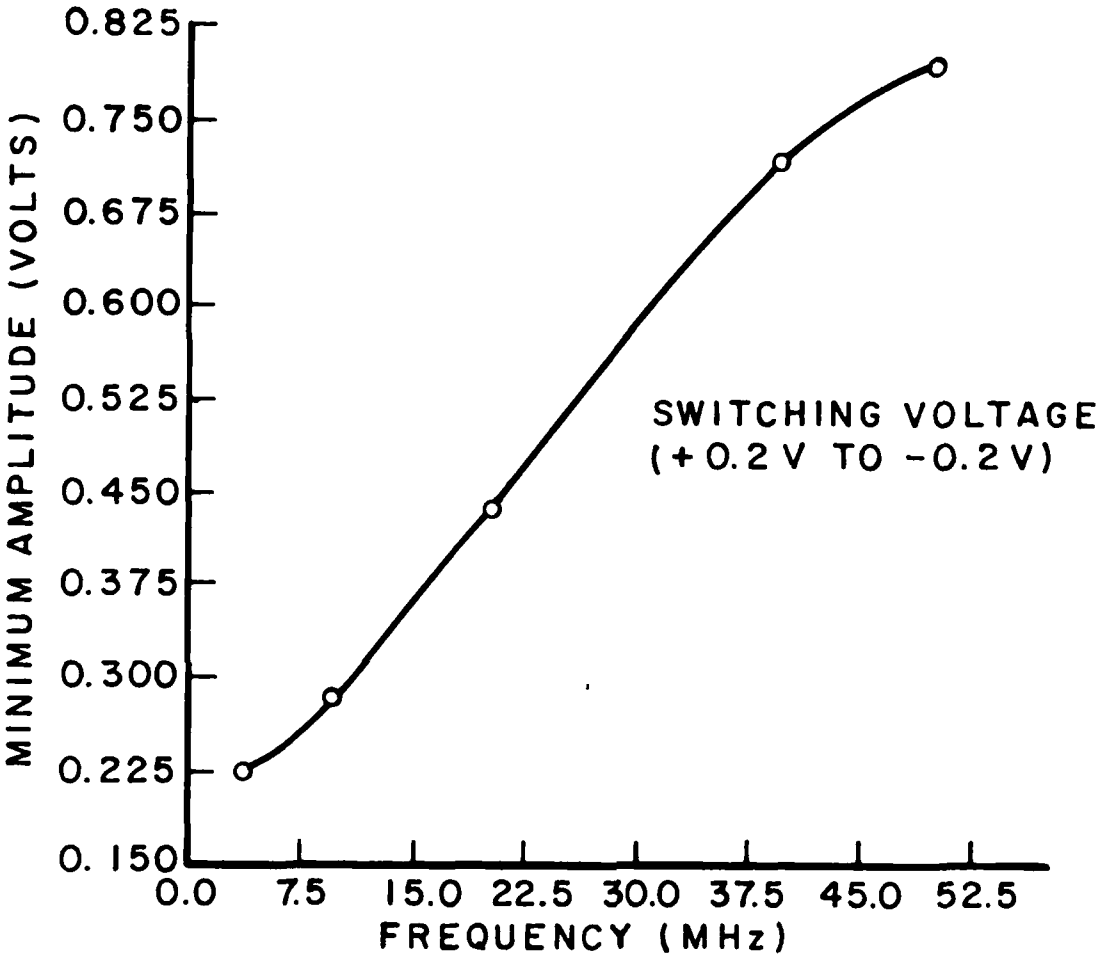


Figure 35. Minimum amplitude of the sinusoidal differential interference, when in series with a +0.2V to -0.2V switching voltage, required to cause improper switching of the receiver output.

Chapter 4

CONCLUSION

This work has used computer simulation to investigate EMI effects due to sinusoidal interference in a DS 55115 differential line receiver. The receiver was found to be relatively immune to common-mode interference. However, severe waveform distortion resulted when the interference entered the receiver as a differential signal. Shifts in the input voltage threshold and time delays were noted in addition to transitions into the incorrect state.

APPENDIX

SPICE Data for Circuit in Figure 1

*Resistors	Nodes		
R1	0	1	0.15K
R2	3	4	2.50K
R3	0	5	0.15K
R4	0	7	0.15K
R5	0	8	0.13K
R6	9	11	7.0K
R7	11	12	8.0K
R8	4	9	1.5K
R9	4	12	1.64K
R10	4	13	1.0K
R11	4	14	1.0K
R12	4	15	1.64K
R13	16	15	8.0K
R14	9	16	7.0K
R16	19	20	2.5K
R15	16	11	0.13K
R17	19	21	.50K
R18	4	25	2.7K
R19	0	23	.15K
R20	24	26	2.6K
R21	24	27	.50K
R22	29	30	3.0K
R23	0	30	1.5K
R24	0	33	5.0K
R25	4	32	2.0K
R26	31	34	.020K
R27	31	4	3.9K

*Capacitors	Nodes		
C1	12	11	1PF
C2	16	15	1PF
C3	31	0	3PF

*Diodes	Nodes		
DI01	0	28	Stan
DI02	25	28	Stan
DI03	25	29	Stan

*Transistors	Nodes			
Q0	3	2	1	TR1
Q1	4	3	2	TR1
Q2	6	2	5	TR1
Q3	9	9	8	TR1
Q4	12	9	7	TR1
Q5	15	9	7	TR1
Q6	13	12	6	TR1
Q7	14	15	6	TR1N
Q8	4	13	20	TR1
Q9	21	21	0	TR1
Q10	4	19	22	TR1
Q11	25	24	22	TR1
Q12	27	27	0	TR1
Q13	22	2	23	TR1
Q14	4	14	26	TR1
Q15	32	29	30	TR1
Q16	32	34	31	TR1
Q17	4	32	33	TR1
Q18	4	33	34	TR1
Q19	31	30	0	TR1

```
*Model Cards for diodes and transistors
.Model Stan D(RS=60 OHMS TT=0.1NS CJO=2PF PB=0.6V BV=40V IS=6E-16)
.Model TR1 NPN(BF=30 BR=0.1 RB=30 OHMS TF=0. 1NS TR=100NS
+RE=1 OHM VA=200V VB=200V CCS=2PF CJE=1PF PE=0.7V ME=0.33V
+CJC=0.5PF PC =0.7V MC=0.33 KF=6.6E-16 IS=6E-16)
.Model TR1N NPN(BF=20 BR=0.02 RB=30 OHM RC=10 OHM
+RE=1 OHM VA=200V VB=200V CCS=2PF CJE=2PF PE=0.7V
+PC=0.7V CJC=0.5PF TF=0.1NS TR=10NS KF=6.6E-16 IS=6E-16)
```

MISSION
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Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, solid state sciences, electromagnetics and electronic reliability, maintainability and compatibility.

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