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QUARTER-INCH STREAMING TAPE DRIVE APPLICATION  
WITH THE SERIAL ASCII INSTRUMENTATION LOOP  
(SAIL) SYSTEM

by

Roderick Mesecar  
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QUARTER INCH STREAMING TAPE DRIVE APPLICATION WITH THE SAIL SYSTEM

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ABSTRACT

This report describes a bulk-data recorder based on the integration of a 1/4-inch streaming magnetic tape drive with interface circuitry to the Serial ASCII Instrumentation Loop (SAIL) concept. The development capitalizes on newly implemented industry standards for electronic interfacing to the tape drive and standards for data formatting on the tape. As the capability of this recording media becomes more apparent to the user, it should help resolve some of the issues dealing with methods and recording media for effectively moving digitized data in the marine community.



INTRODUCTION

Streaming tape drives were developed for use as disk-backup devices for mid-size computer systems. The word "streaming" relates to the operation of the tape unit, wherein the tape motion, once begun, is not stopped until the entire tape has been written to or read from.

The more common tape drive has nine-track capability, with recording taking place one track at a time and in both directions of tape travel. Recording takes place in bit-serial form where tape speed is 90 inches per second (ips) and the recorder bitdensity is 10,000 flux changes per inch (fci).

For our interests, the attractive features of the streaming drives are the standards which a number of manufacturers have adopted.

The first standard proposal adopted by the group, announced on August 20, 1982, addressed the need for an intelligent interface.(5) Named QIC-02, this interface was designed to work with the majority of existing controllers designed for quarterinch streamers while also permitting an extended command set for future applications.

The second standard proposal, QIC-24, was adopted by the group and announced on February 24, 1983. This agreement proposed a standardized recording format, enabling the interchangeability of recorded cartridges across several manufacturer's quarterinch streamers. QIC-24 provides for recording a tape in a block format. A block is made up of a preamble, a start-of-data marker (one byte), 512 bytes of data, a block address, a cyclic redundancy check (CRC), and a postamble.

By reference, the streamer QIC standards incorporate the 1/4-inch tape cartridge (similar to model DC-300XL) as the recording medium. This tape cartridge is described by ANSI Standard 3.55-1977.

A preliminary design review indicated that a simple SAIL to QIC-02 interface with a 4-Kbyte buffer memory would handle the application requirements of the streamer drive coupling to the SAIL system. Using the tape drive in this mode reduces tape storage efficiency but the remaining capacity appears more than adequate for vessel parameter data recording requirements. Another inducement for using streamers for the bulk data recording media is their projected cost. Current cost for a 4060 Mbyte model is \$1300. Because of projected high volume production, expected cost for an equivalent streamer model is in the \$800 range.

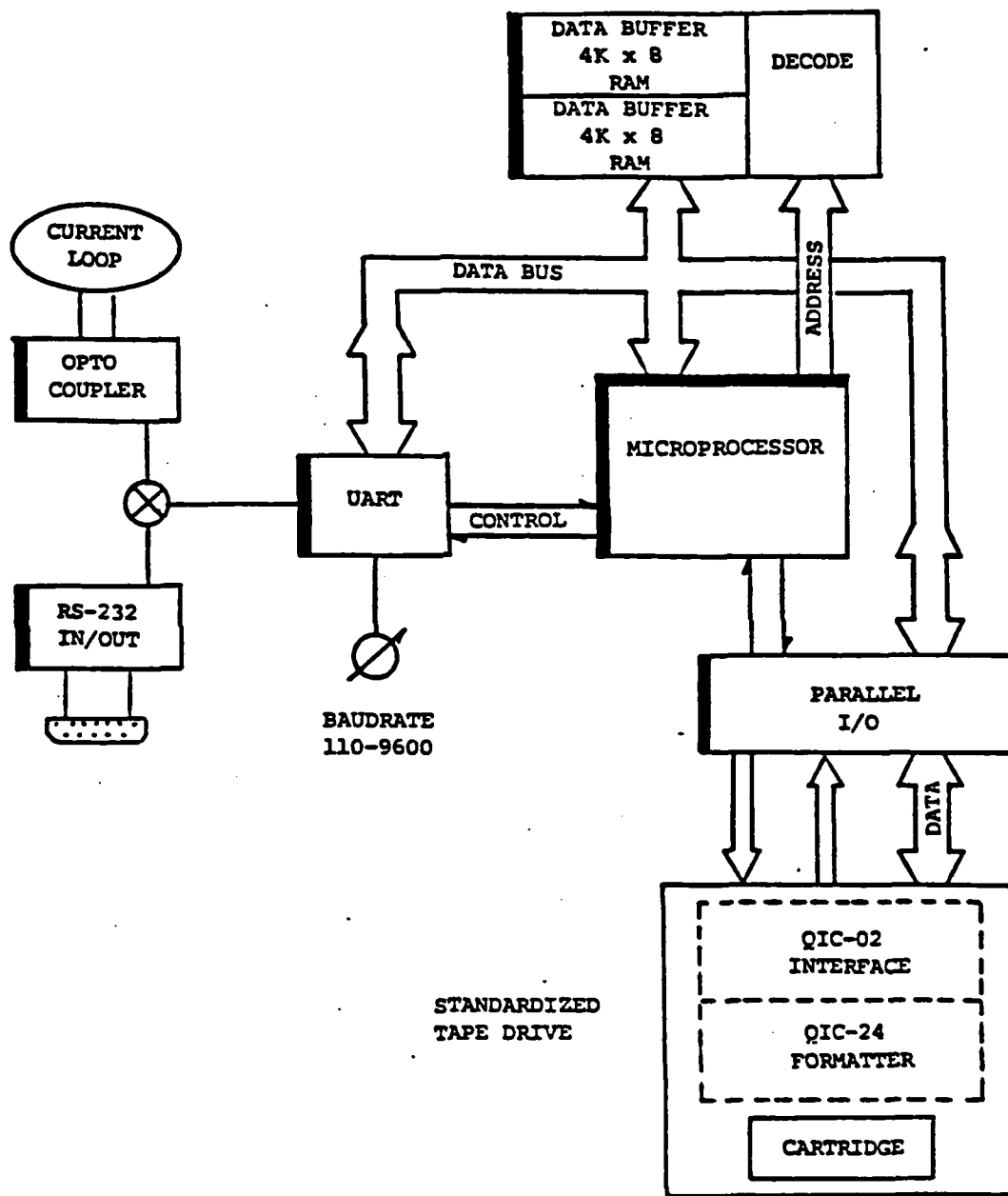
## APPLICATION WITH THE SAIL SYSTEM

Our resolve was to develop interface circuitry that would accept the serial information from the SAIL loop and link it with the QIC standard tape drive as effectively as possible. Functionally the interface provides:

- tape read/write capability
- two time-shared buffer memories
- opto-isolated SAIL input
- RS-232C type input/output

The interface circuit as implemented, is microprocessor controlled and shown in block diagram form in the next figure. Before examining the interface circuitry in detail, a discussion of the data flow in the system will be useful. Assume that the recorder is connected to a functioning SAIL loop on the left side of the figure. Serial ASCII characters on the SAIL loop pass through the recorder's optically-isolated loop coupler and are presented to a UART. As each character is received by the UART, it is loaded into a buffer memory. (There are two buffer memories, each with a capacity of 3584 ASCII characters.) A buffer is filled at the character rate of the SAIL loop. When a buffer becomes full, the loop input is switched to the other buffer; the tape drive is notified by sending it a write command; the contents of the full buffer are then transferred at high speed (about 86 Kbytes/sec) to the tape drive.

Initially, the tape is at rest. When a write command is received by the tape drive, tape motion is started and the memory buffer contents are written onto the tape. The interface then causes a file mark to be written at the end of 3584 bytes of transferred data. Tape motion is then stopped. The entire recording process takes about two seconds. In the meantime, any activity on the SAIL loop is routed to the second buffer



Block diagram of the bulk-data recorder proposed for the research vessel environmental data instrumentation or equivalent systems.



memory. The tape will remain at rest until the second buffer is full, at which time data from the loop is switched to the first buffer and the second full buffer is transferred to the tape drive. This method of buffer switching (sometimes called ping-pong) ensures that no data from the SAIL loop will be lost while the tape drive is in operation. It may also be noticed that the tape drive is not operating in the "streaming" mode for which it was designed. The final step in the system data flow is a taperead facility. The bulk-data recorder includes a means for reading data from the tape which will be expanded on later.

A more detailed account of the interface circuitry can now be presented. The interface is controlled by a Zilog Z-80B microprocessor operating at 5 MHz. The Z-80B has an 8-bit data bus and a separate 16-bit address bus. Two interrupt inputs (one maskable, one non-maskable) are provided. In addition to separate read and write outputs, the processor supplies a signal for memory-type operations and a signal for input/output operations. These signals can be used with address decoding logic to synchronize the operation of peripheral circuits. The Z-80B also has a rich and powerful instruction set. One of the I/O-type instructions permits a block transfer of up to 256 bytes, and uses the low eight address lines to supply a peripheral address.

The operating program (firmware) for the interface is stored in a 2732A-type EPROM (an ultra-violate erasable, programmable read-only-memory). The 2732A has a 4K by 8 bit capacity, but only the lower 2K locations are used. The 2732A was chosen because it has a faster access time than 2K x 8 EPROMs, and allows the Z-80B to operate without using "wait" states.

In addition to the EPROM, connected to the Z-80B microprocessor are a UART, a parallel I/O circuit (PIO), and four 2K by 8-bit RAM chips

(expandable). The data recorder input circuits provide for an opto-isolated SAIL connection and an RS-232C-level input. For either input to work, the other input must be disconnected.

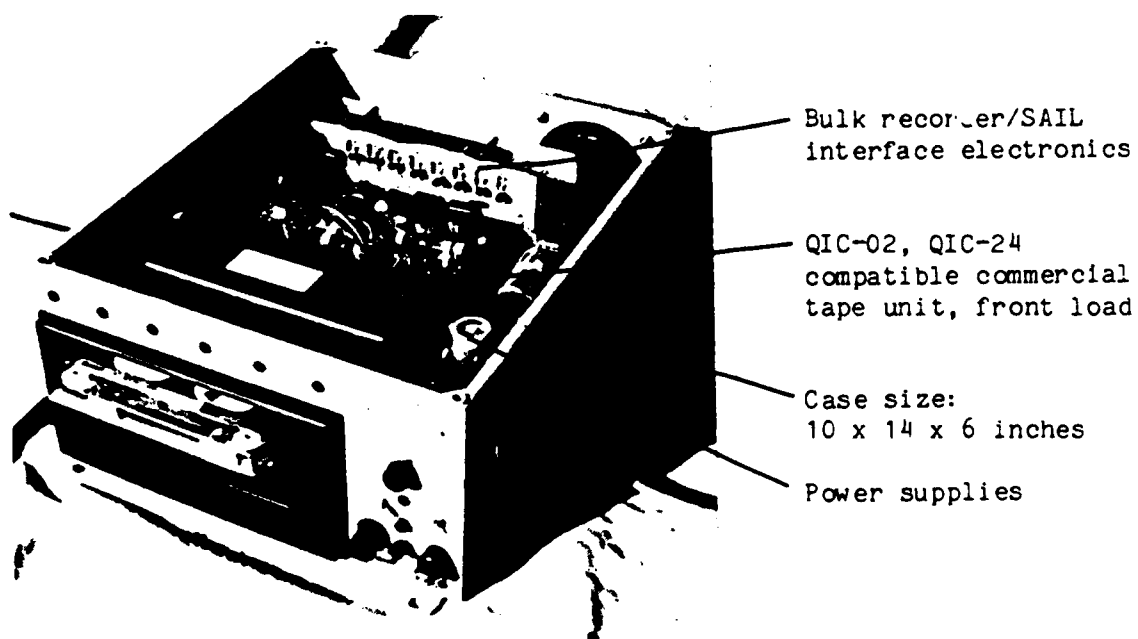
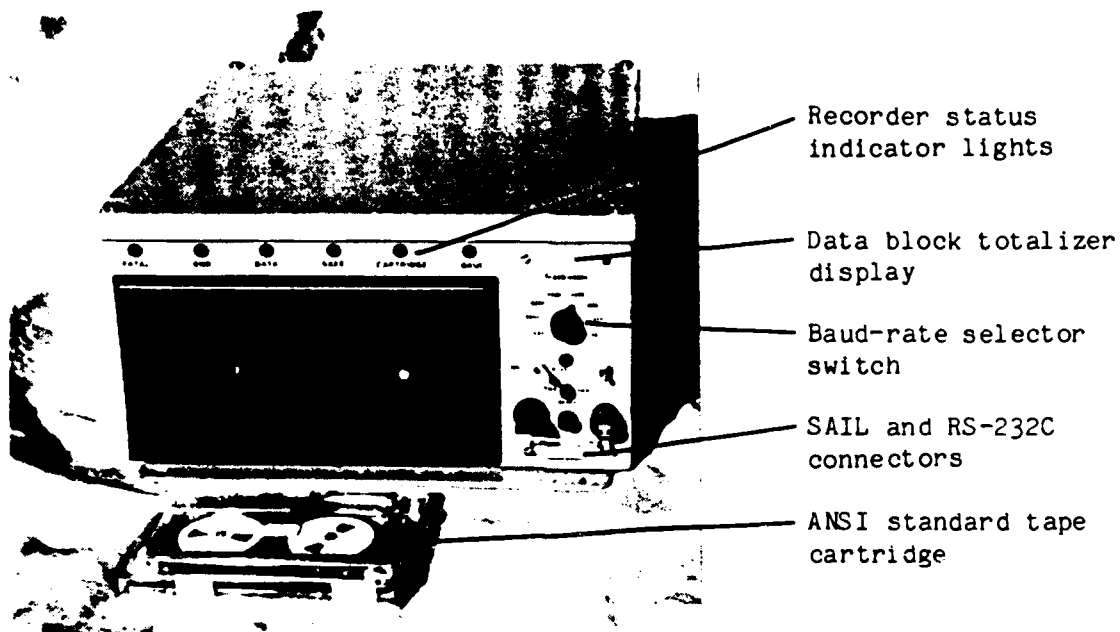
Data transfer to the tape unit is in blocks of 512 bytes (ASCII characters). Tape motion is not started until at least 512 bytes have been transferred to the tape drive's input buffer. Each data byte is transferred from the interface to the tape drive in less than 6 milliseconds under handshake control.

If the data block just transferred is the first block sent following a Write Command, the tape drive will start the tape in motion. The tape first backs up, then proceeds in the direction of recording ("forward" and "reverse" are ambiguous here, because recording takes place in either tape direction). The reason for the tape backing up is so that the next recorded segment can be placed adjacent to the last recorded segment, eliminating the "gaps" due to start/stop. Once the tape is travelling in the direction of recording, succeeding data blocks will be recorded without the tape stopping. Tape motion is stopped after a Write File Mark command is received and a file mark (block) is written by the tape drive. The tape will remain stopped until the other buffer memory is filled by data from the SAIL loop. The total time the tape is in motion to record 3584 bytes is just under two seconds; several minutes may elapse, however, while a buffer is being filled from the SAIL loop. During the time that a buffer is being written onto tape, any incoming data from the SAIL loop is entered into the other buffer (remember this is a ping-pong buffer system). In the unlikely event that the alternate buffer becomes full while waiting for the other buffer to be recorded, the alternate buffer to be over written with subsequent incoming data.

The bulk-data recorder uses front panel LED's to indicate selected error or status conditions. After the status bytes from the tape drive are stored in memory, the interface processor pulls out bytes 0 and 1 and examines them for applicable error bits. There are five error/status conditions indicated on the recorder front panel (see Figure 2) . These are:

- CARTRIDGE -- (Read or Write mode) indicates that a cartridge is not in place.
- SAFE -- (Write mode) indicates that a cartridge is in a "safe" (write protected) condition. Recording cannot be accomplished.
- DATA -- (Read or Write mode) indicates that an unrecoverable data error occurred.
- END -- (Write mode) indicates that the end of tape has been reached (all nine tracks have been recorded).
- FATAL -- (Write mode) indicates that a fatal error has occurred and that the cartridge should be replaced.

In the WRITE mode, after a non-protected tape cartridge has been inserted and tape motion has begun, any error which occurs will be a fatal condition. The two errors of most concern are write errors and end-of-tape errors. If the tape drive is unable to properly record (write) a data block after several tries, the drive assumes the tape is bad and rewinds to the beginning of tape and sets the FATAL indicator. Due to the design of the QIC tape drive, it is impractical for the bulk-data recorder to append data to the end of the data block which could not be properly written). The user must then replace the cartridge (if the data is to be saved) and restart the recording process.



Photographs illustrating the mechanical configuration of a commercial 1/4-inch streaming tape drive with the interface electronics to form the SAIL system bulk-data recorder.

A limited-function TAPE READ capability has been incorporated in the bulk-data recorder to give the user the option to couple it to any processor with a RS-232 port. The main purpose of the read capability is to allow recorded tapes to be examined, and to aid in troubleshooting. However, the read function can also be used for data reduction purposes, but is more time-consuming than when the streamer is coupled directly through the QIC-02 interface to a host computer. In the READ mode, error conditions are more forgiving. Data blocks which cannot be properly read can still be transferred from the tape drive to the interface. These will be indicated on the front panel as DATA errors. However, the read operation may continue. There are no FATAL errors in READ mode.

A front panel BAUDRATE switch gives the user the option of two-way baud rates from 110 to 9600. All of the RS-232 port communications with the bulkdata recorder are done in ASCII through a connector on the front panel and a few commands. Also incorporated on the front panel is a four digit counter display. This display indicates the amount of data recorded on a tape. The display counter counts files as they are recorded. Each file is presently 3584 bytes, so each time the display value increases by one, that indicates that an additional 3584 bytes (ASCII characters) have been recorded. When the display (counter) value reaches 9800, the audible alarm is sounded and the END indicator light will flash. This serves as an early warning that the tape is nearly full and should be replaced before data is lost. There should be approximately ten files (35000 bytes) capacity remaining on the tape.

#### REFERENCES

1. Evans, F. and R. S. Mesecar, "Common Computer Interface Advantages." Proceedings, Working Conference on Oceanographic Data Systems, Woods Hole, MA, 1975, p. 257-270.
2. Mesecar, R. S. and F. Evans, "A Partitioned Data Communications System." Proceedings, Second Working Conference on Oceanographic Data Systems, Woods Hole, 1978, p. 372.
3. Copies of the SAIL standard can be obtained from W. D. Barbee, Executive Secretary, UNOLS, WB-15, University of Washington, Seattle, WA 98105.
4. Mesecar, R. S. and W. Dillon, "Proposal for the Exchange and Recording Media of Research Vessel Parameter Data--SAIL." Proceedings, Third Working Conference on Oceanographic Data Systems, Woods Hole, MA, 1983, p. 179.
5. Copies of the QIC standards and a list of companies participating in their preparations can be obtained from: Freeman Associates, Inc., 311 E. Carrillo St., Santa Barbara, CA 93101.

#### IV. Circuit Description

##### K. BULK DATA RECORDER

(refer to drawings OC-1567, OC-1568, OC-1569)

- 1.0 The Bulk Data Recorder is a self-contained magnetic tape recording system capable of storing more than 35 million ASCII characters. The recording system utilizes a commercially-produced cartridge tape drive to accomplish the actual recording. The tape drive operates in accordance with the QIC-02 and QIC-24 industry standards for quarter-inch cartridge streaming tape drives. The QIC standards define the electrical interface requirements and the recording format.
  - 1.1 A microprocessor-based interface and buffer memory serve as a link between the SAIL loop and the tape drive.
  - 1.2 The recorder is designed to plug into the loop just as a regular SAIL module would. The recorder may also be operated through an OSU Output Port Module, if addressability is desired.
  - 1.3 Main components of the bulk-data recording system are the cartridge tape drive, the electronic interface and memory, power control and power supplies, and the front panel. Each of these components will be covered in the descriptions which follow.
- 2.0 The cartridge TAPE DRIVE is a commercially-produced streaming tape unit which accepts an ANSI standard quarter-inch tape cartridge such as the 3M type 300XL.
  - 2.1 In general, streaming tape drives were developed for use as disk-backup devices for computer systems. The word "streaming" relates to the operation of the tape unit, wherein the tape

motion, once begun, is not stopped until the entire tape has been written to or read from.

2.2 The tape drive used with the bulk-data recorder has nine-track capability, with recording taking place one track at a time and in both directions of tape travel. Recording takes place in bit-serial form. Tape speed is 90 inches per second (ips) and the recorder bit-density is 10,000 flux changes per inch (fci).

3.0 The tape drive contains its own electronics, and was designed and built to conform to industry standards QIC-02 and QIC-24. QIC-02 is the standard for an "intelligent interface", and QIC-24 is the format standard for recording.

3.1 The interface standard defines electrical signals and their timing; delineates a set of standard and optional commands; and describes various status bits and bytes. Descriptions of the two handshakes involved are also given.

3.2 The format standard defines the number of tape tracks and their locations on the tape; the track recording sequence and beginnings and ends of tracks on the tape; the data "blocking" required; and other aspects of the recording process. The ANSI standard governing the tape cartridge is incorporated in QIC-24 by reference.

3.3 Data recording takes place in a block format. The standard calls for each block to be made up of a preamble, a data block marker, 512 bytes of data, a block address, a cyclic-redundancy-character (CRC), and a postamble. Each portion of the block is controlled by the standard. A file mark block has the same



configuration as a data block, except that the data content is 512 bytes of a special bit pattern.

3.4 The details of standards QIC-02 and QIC-24 are too extensive to be included in this writing, but the standards are set forth in Appendix B1 and Appendix B2 at the end of this manual.

3.5 For details on the features and operation of the tape drive, see the manufacturer's manual for that drive.

4.0 The INTERFACE circuitry serves as the link between a SAIL loop and the QIC-standard tape drive. The interface provides a tape read/write capability, contains two time-shared buffer memories, and has an opto-isolated serial current loop input and an RS-232C-style input/output.

4.1 Before examining the interface circuitry in detail, a discussion of the data flow in the system will be useful. Assume that the recorder is connected to a functioning SAIL loop, and that a tape cartridge has been inserted and is ready to accept data.

4.2 Serial ASCII characters on the SAIL loop pass through the recorder's optically-isolated loop coupler and are presented to a UART. As each character is received by the UART, it is loaded into a buffer memory. (There are two buffer memories, each with a capacity of 3584 ASCII characters.) A buffer (memory) is filled at the character rate of the SAIL loop.

4.3 When a buffer becomes full, the loop input is switched to the other buffer; the tape drive is notified by sending it a write command; the contents of the full buffer are then transferred at high speed (about 86 Kbytes/sec) to the tape drive.

4.4 Initially, the tape is at rest. When a write command is received by the tape drive, tape motion is started and the memory buffer contents are entered (see 4.3) and are written onto the tape. The interface then causes a file mark to be written (at the end of 3584 bytes of data).

4.5 Tape motion is then stopped. The entire recording process takes about two seconds. In the meantime, any activity on the SAIL loop is routed to the second buffer memory (see 4.2). The tape will remain at rest until the second buffer is full, at which time data from the loop is switched to the first buffer and the second (full) buffer is transferred to the tape drive. This method of buffer switching (sometimes called ping-pong) ensures that no data from the SAIL loop will be lost while the tape drive is in operation. It may also be noticed that the tape drive is not operating in the "streaming" mode for which it was designed. The final step in the system data flow is a tape-read facility. The Bulk-Data Recorder includes a means for reading data from the tape. This will be discussed later.

5.0 A more detailed account of the interface circuitry can now be presented. The interface is controlled by a Zilog Z-80B microprocessor operating at 5 MHz. The Z-80B has an 8-bit data bus and a separate 16-bit address bus. Two interrupt inputs (one maskable, one non-maskable) are provided. In addition to separate read and write outputs, the processor supplies a signal (MREQ) for memory-type operations and a signal (IORQ) for input/output operations. These signals can be used with address decoding logic to synchronize the operation of peripheral cir-

cuits. The Z-80B also has a rich and powerful instruction set. One of the I/O-type instructions permits a block transfer of up to 256 bytes, and uses the low eight address lines to supply a peripheral address.

- 5.1 The operating program (firmware) for the interface is stored in a 2732A-type EPROM (an ultra-violet erasable, programmable read-only-memory). The 2732A has a 4K by 8 bit capacity, but only the lower 2K locations are used. The 2732A was chosen because it has a faster access time than 2K x 8 EPROMs, and allows the Z-80B to operate without using "wait" states.
- 5.2 In addition to the EPROM, connected to the Z-80B microprocessor are a UART, a parallel I/O circuit (PIO), and four 2K by 8-bit RAM chips. The RAM chips and the address decoding logic are located on a p.c. board separate from the rest of the interface circuitry. This physical arrangement allows the memory portion to be expanded as desired.
- 5.3 The data recorder input circuits provide for an opto-isolated SAIL connection and an RS-232C-level input. For either input to work, the other input must be disconnected.
- 5.4 The RS-232C input is designed to operate with signal levels as low as  $\pm 5$  volts. For a negative RS-232C input (at connector pin 2) the voltage at pin 5 of the 4N37 will be approximately zero, due to the current through the 3K resistor. With zero volts on its base, the 2N3904 transistor will be off, and its collector voltage will be a +5 volts. This high level represents a MARKING condition at the UART serial input, pin 20.
- 5.5 If a positive RS-232C level is applied to connector pin 2, the voltage at pin 5 of the 4N37 will be high. The diode in

series with the RS-232C input is reverse biased for positive inputs, thereby blocking the input voltage. Base current for the 2N3906 transistor is then supplied by the +5 volt supply through the 3K and 10K resistors, causing the transistor to turn on. With the transistor on, its collector voltage will be near zero volts. This low level represents a SPACING condition at the UART serial input, pin 20.

5.6 If the data recorder is connected to a SAIL loop, the loop current will flow through the diode bridge in such a direction that the 4N37 LED will be forward biased. The LED will thus be illuminated, causing the phototransistor to be turned on. With the photo transistor on, its collector voltage (at pin 5) will be near zero volts. The 2N3906 transistor, with its base at zero volts, will be off and its collector voltage will be at +5 volts. This high level represents a MARKING condition at the UART serial input, pin 20.

5.7 With no current flowing in the SAIL loop, there will be no current through the 4N37 LED, and consequently the photo transistor will be off. Under this condition, the 2N3906 transistor will be turned on due to base current supplied through the 3K and 10K resistors. Since the 2N3906 is on, its collector voltage will be near zero volts. This low level represents a SPACING condition at the UART serial input, pin 20.

5.8 The foregoing described individually the operation of the SAIL input and the RS-232C input. It must be emphasized again that each input will function properly only if the other input is not connected. This is because the two inputs are ORed at pin 5 of the 4N37.

- 6.0 In the WRITE mode, the microprocessor repeatedly samples the UART Data Received flag (UART pin 19) by reading it through a tri-state buffer (LS367A) which is connected to the data bus. If an ASCII character is received by the UART, the Data Received flag will come high (+5 v) and will be gated onto data bus bit 7 by the RDSTAT signal. RDSTAT is generated by the address decoder (on the memory board) during a memory-read cycle of the processor.
- 6.1 The processor then determines that data bit 7 (Received Data flag) is high, and reads the UART data register by issuing a RDUART signal (another memory-read cycle) to UART pins 4 and 18.
- 6.2 The processor stores the UART data in a buffer memory at a previously determined location, increments the buffer pointer, and checks to see if the buffer is full. If the buffer is not full, the processor resumes testing the UART Data Received flag, awaiting the next character from the UART.
- 6.3 Each time the processor detects a character from the UART (Received Data flag high) the processor also tests bit 0 to see if there is a framing error (FE, UART pin 14) for that character. The most likely cause of a framing error is a baudrate disagreement between the incoming serial data and the interface UART. Therefore, if a framing error occurs (bit 0 high) an indicator LED on the recorder front panel is lit, warning the user that the recorder baudrate is not the same as the incoming data baudrate. Whether or not a framing error is present, the UART character is stored in the buffer memory.

6.4 Referring to paragraph 6.2, if a buffer memory is full (3584 characters) the processor prepares the interface to write the buffer onto tape. Several tasks must be accomplished before data is transferred from memory to tape: (a) A pointer is set up so that incoming data will be stored in the alternate buffer memory; (b) the pointer to the full buffer is initialized so that transfer to the tape unit will begin at the first location of the full buffer; (c) the non-maskable interrupt is enabled (as explained later).

6.5 After these housekeeping chores are done, the processor involves itself with the data transfer process to the tape drive. This is fairly complicated, and the different parts of the process will be explained in sequence. A parallel I/O (PIO) chip (Z-8420) and miscellaneous logic are used to interface with the tape drive. The PIO has two 8-bit ports (A and B) which may be used as bit-wise inputs or outputs. Three address lines from the processor address bus are used to control the PIO. Address bit <sup>2</sup> is inverted and acts as a chip enable for the PIO. Address bits 0 and 1 determine the function of the PIO, and connect to the control inputs at pins 5 and 6. These address inputs are effective only when the IORQ pulse (PIO pin 36) is active, during a processor I/O instruction. The processor data bus also connects to the PIO. Of the two ports available, port A is used as the data port to and from the tape drive. All eight lines of port A are programmed either as input or as output as required. Port B is used as flag/control lines, and various lines are programmed as fixed inputs or outputs. The PIO also has a pair of "handshake" lines associ-

ated with port A. These lines are called A-READY and A-STROBE. The PIO has RD (read) input, but does not have a write input. An IORQ pulse and the absence of a RD causes a write function to take place within the PIO.

6.6 Returning now to the data transfer process, the microprocessor reads the condition of the PIO port B lines and tests bit 3 to see if the EXC (exception) line (from the tape drive) is high, indicating lack of an error condition. Finding the EXC line high, the processor then tests (by reading port B) the RDY (ready) line (bit 6). If the tape drive is not ready, bit 6 will be high and the processor will execute a loop, testing EXC and RDY, waiting for an error indication or for the tape drive to come ready.

6.7 If (or when) the tape drive is "ready" (RDY line is low), the processor outputs a Write Data command (hex 40) through PIO port A to the bi-directional drivers (74LS242) for the tape drive data bus. (The 'LS242 are set up as outputs by the DIR line being high.) All commands sent must be synchronized by handshaking two lines with the tape drive. The handshake lines used with commands (and status) are the RDY line from the tape drive, and the REQ (request) line to the tape drive. Immediately after the Write Data command is sent, the processor makes bit 5 of PIO port B high, which is sent through the 7438 driver as a REQ signal to the tape drive. As part of the handshaking, the RDY line goes high, then goes low again to indicate that the tape drive accepted the Write Command. The processor monitors the RDY line for this action; then, after RDY has gone low, sets PIO port B bit 5 low, clearing the REQ signal at the

tape drive. The handshake cycle is complete. The processor then waits for the RDY line to again go high (indicating the tape drive is busy acting on the command).

6.8 Sensing that the RDY line is high, the processor then waits for RDY to go low again. This time, a low RDY signal indicates that the tape drive is ready to accept a data transfer.

7.0 Data transfer to the tape unit is in blocks of 512 bytes (ASCII characters). Tape motion is not started until at least 512 bytes have been transferred to the tape drive's input buffer.

7.1 Each data byte is transferred from the interface to the tape drive under handshake control. A different set of handshake lines is used for data than for commands. The two data handshake lines are XFER to the tape unit and ACK from the tape unit.

7.2 The PIO (see paragraph 6.5) also has two handshake signals, A-READY and A-STROBE. These will be used with the XFER and ACK signals from the tape drive. Under microprocessor control, a data byte from the interface buffer memory will be transferred through the PIO port A to the tape drive.

7.3 The PIO is set up in an "output with handshake" mode. In this mode, the A-READY output from the PIO is initially low. After a byte is read from memory to the PIO and presented at port A, the A-READY signal goes high. The high A-READY is gated by the READ/WRITE mode switch (front panel) and XFER ENABLE and is presented as a low XFER signal through the 7438 driver to the tape drive.



7.4 The low XFER signal informs the tape drive that data is present on the tape drive data bus. The tape drive responds by accepting the data byte and issuing a low ACK signal. The ACK signal going low triggers a one-shot (74LS123) circuit which supplies an A-STROBE pulse to the PIO at pin 16. The A-STROBE pulse resets (to low) the PIO A-READY signal, making the XFER signal high to the tape drive. The tape drive then makes the ACK signal high, thereby completing the handshake cycle. As mentioned previously (7.1) a handshake cycle is required for each data byte transferred.

7.5 A block of data (512 bytes) must be transferred to the tape drive in less than 6 milliseconds. To accomplish this, the processor's maskable interrupt is used in conjunction with a form of block-transfer output instruction.

7.6 After the Write Command is sent, a byte-count register in the processor is loaded with the value zero (for 256 bytes). XFER ENABLE is asserted to allow the handshake to take place. The interrupt service routine (written as a subroutine) is then called to initiate the data transfer. [The maskable interrupt (INT) is initially disabled.] The service routine accomplishes the following:

- (a) Outputs a byte directly from memory to PIO port A, increments the memory pointer and byte-count register (with one instruction).
- (b) Checks the byte-count register for zero value (using a conditional jump).
- (c) Enables the interrupt if the byte count is not zero (if fewer than 256 bytes transferred).

(d) Returns (with interrupt disabled if 256 bytes have been sent).

- 7.7 During the transfer of 256 bytes, each time the processor returns from the interrupt service routine, the interrupt will be enabled. When the A-READY (PIO) signal goes low after a handshake cycle, the low A-READY will cause an interrupt to the processor (at Z-80B pin 16). In this fashion, the processor is forced to output data at a rate determined by the tape drive handshake.
- 7.8 After the last of 256 bytes is transferred, the processor will return from the interrupt service routine with the interrupt disabled. The byte-count register will once again have a zero value in it (overflow). The operating program will then enable the interrupt, and the byte transfer will be repeated for another 256 bytes. The requisite 512 bytes constituting one data block have now been transferred to the tape drive.
- 7.9 If the data block just transferred is the first block sent following a Write Command, the tape drive will start the tape in motion. The tape first backs up, then proceeds in the direction of recording ("forward" and "reverse" are ambiguous here, because recording takes place in either tape direction). The reason for the tape backing up is so that the next recorded segment can be placed adjacent to the last recorded segment, eliminating the "gaps" due to start/stop. Once the tape is travelling in the direction of recording, succeeding data blocks will be recorded without the tape stopping. Tape motion is stopped after a Write File Mark command is received and a file mark (block) is written by the tape drive.

- 8.0 After each data block is transferred, the interface microprocessor checks to see if the buffer memory has been emptied (7 blocks, or 3584 bytes have been sent). If the buffer is not empty, the processor waits in a loop for the tape unit RDY signal to come low, indicating that the tape unit is ready for another block of data (or a command). In this loop, the processor checks the EXC line from the tape drive, to see if an error condition has occurred; then checks the RDY line and loops back. When the tape drive is ready for more data, the transfer process described previously is repeated a 512-byte block at a time until the interface buffer memory is empty.
- 8.1 When the processor detects that the buffer is empty, it sends a Write File Mark command to the tape drive (after checking RDY to determine that the tape unit is ready for the command). The tape drive records a file mark block (same size as a data block) on tape then stops the tape motion. The tape will remain stopped until the other buffer memory is filled by data from the SAIL loop. The total time the tape is in motion to record 3584 bytes is just under two seconds; several minutes may elapse, however, while a buffer is being filled from the SAIL loop.
- 8.2 During the time that a buffer is being written onto tape, any incoming data from the SAIL loop is entered into the other buffer (remember this is a ping-pong buffer system). The Data Received line from the UART (pin 19) is connected to a gate which has been enabled by NMI ENABLE (PIO port B, bit 1, pin

28). See paragraph 6.4. The output of this gate is connected to the processor's non-maskable interrupt (NMI) input, pin 17.

8.3 The NMI can interrupt at any time, even during the service routine for the maskable interrupt (INT). The NMI service routine (for incoming data) accomplishes the following:

- (a) Selects current pointer to a location in the alternate buffer memory.
- (b) Reads the character from the UART and stores it in the buffer.
- (c) Increments the buffer pointer
- (d) Checks if the buffer is full, decrements the pointer if it is.
- (e) Restores conditions which existed prior to NMI, and returns.

In item (d) above, in the unlikely event that the alternate buffer becomes full while waiting for the other buffer to be recorded, the alternate buffer's pointer is decremented; this causes the top location in the buffer to be over written with subsequent incoming data. This is done simply to keep the buffer pointer in bounds.

9.0 It has been mentioned several times that, while waiting for the tape drive to come ready, the EXC (exception) line is tested by the processor. If an error condition exists in the tape drive, the EXC line will be a low (zero volts) level. If an error exists, the tape drive will not come ready (RDY will not go low), so it is necessary to test the exception line each time before the ready line is tested, except during handshaking.

- 9.1 The processor reads PIO port B and then tests bit 3 (PIO pin 30). If bit 3 (EXC) is low, the processor issues a Read Status command to the tape unit. The Read Status command is sent using the RDY/REQ handshake as described in paragraph 6.7.
- 9.2 After the Read Status command is accepted, the tape drive will make the DIR line low, reversing the direction of data flow in the LS242 drivers. The tape drive will then send six status bytes to PIO port A. Each of the six status bytes is sent under handshake control, again using the RDY and REQ lines. Each time the RDY line goes low, the processor reads PIO port A and stores the status byte in an auxiliary section of memory. The processor counts the bytes, and when it has read six, it stops reading port A and monitors port B for the DIR (direction) line to go high, indicating that the tape drive has finished sending.
- 9.3 The first two bytes of the six status bytes contain information about error conditions; the remaining four bytes are not used by the interface, and will not be discussed. After a Read Status command, however, it is necessary, because of the handshaking involved, to read all six bytes. Refer to the QIC-02 standard and/or the tape drive manual for details on the status bytes.
- 9.4 The Bulk Data Recorder uses front panel LED's to indicate selected error or status conditions. After the status bytes from the tape drive are stored in memory, the interface processor pulls out bytes 0 and 1 and examines them for applicable error bits set.

- 9.5 There are four error/status conditions indicated on the recorder front panel. These are: CARTRIDGE (not in place); SAFE (cartridge is write-protected); DATA (a tape data block cannot be properly written or read); and END (tape is at end, all nine tracks have been used). In addition, the processor manufactures a status condition labeled on the front panel as FATAL. An audible alarm (beeper) is associated with the FATAL conditions, so that any time a conditions which is fatal occurs, the user will be alerted by the beeper. The front panel LED's will then indicate the fatal condition. (A fatal condition is one which will cause improper operation of the recorder.)
- 9.6 When power is applied (or the front panel RESET is pushed) and there is no tape cartridge inserted, the CARTRIDGE indicator should be lit. This is not a fatal condition, but operation will not proceed until a cartridge is inserted. If the recorder is in the WRITE mode (front panel switch) and the inserted cartridge is in the "safe" condition (write protected) then the SAFE indicator will be lit, and operation will not proceed until the cartridge is removed, set to the nonprotected state, and reinserted. In the READ mode, the cartridge "safe" condition will not interfere with normal operation.
- 9.7 In WRITE mode, after a non-protected tape cartridge has been inserted and tape motion has begun, any error which occurs will be a fatal condition. The two errors of most concern are write errors and end-of-tape errors. If the tape drive is unable to properly record (write) a data block after several tries, the drive assumes the tape is bad and rewinds to the beginning of tape, setting the fatal write error bit in status byte 0. Due

to the nature of the QIC tape drive, it is impractical for the Bulk Data Recorder to append data to the end of the bad block (the data block which could not be properly written). Therefore, if a write error occurs, the data recorder signals a FATAL condition and sounds the beeper alarm. The user must then replace the cartridge (if its data is to be saved) and push the front panel RESET switch. Arriving at the end of the tape means, of course, that no more recording can be done on that tape. The cartridge must be removed and replaced with a different cartridge. The RESET switch must be operated to begin recording on the new cartridge. And obviously, if the cartridge is removed after recording has begun, recording cannot continue. To clear any FATAL condition, the RESET switch must be operated.

9.8 In the READ mode, error conditions are more forgiving. Data blocks which cannot be properly read can still be transferred from the tape drive to the interface. These will be indicated on the front panel as DATA errors. However, the read operation may continue. There are no FATAL errors in READ mode.

10.0 A limited-function TAPE READ capability has been incorporated in the Bulk Data Recorder. The main purpose of the read capability is to allow recorded tapes to be examined, and to aid in troubleshooting. The read function can be used for data reduction purposes, but is more time-consuming than is a more sophisticated system using a host computer.

10.1 The RS-232C connector on the recorder front panel is utilized for reading tapes. The SAIL loop must be disconnected (refer

to paragraph 5.8). The front panel BAUDRATE switch must also be set to the desired (two-way) rate. All communication through the RS-232C connector is serial ASCII, at RS-232C levels. See paragraphs 5.4 and 5.5.

10.2 Four commands sent through the RS-232 port are recognized by the recorder in READ mode. They are:

REWIND -- rewinds tape to BOT

READ -- reads a tape until a file mark is encountered on the tape.

SKIP -- advances tape until next file mark is encountered.

DATA -- causes 256 characters from the buffer to be returned.

These commands are chosen from the ASCII character set as follows:

REWIND: the ASCII character for the letter R (52 hex)

READ: the ASCII character for ENQ (05 hex)

SKIP: the ASCII character for the letter 'M' (4D hex)

DATA: the ASCII character for DC2 (12 hex)

The recorder will furnish the following responses to the commands:

REWIND: no response; operator must determine when rewind complete.

READ: After a file has been read from tape into the buffer, the response is the ASCII character for ACK (06 hex)

SKIP: After the next file mark on the tape is found, the response is the ASCII character for ACK (06 hex).



DATA: After each 256 character data block is sent, response is the ASCII character for DC4 (14 hex). When an entire file has been transferred, the response is the ASCII character for "SUB" (1A hex), (also Control Z).

During the execution of a DATA command, the interface checks for the receipt of XON and XOFF characters, which can be used to control the transmission of data.

- 10.3 The interface microprocessor repeatedly samples the DR output of the UART by reading the UART status with a RDSTAT signal. When DR (data bit 7) comes high, indicating a character has been received by the UART, the processor reads the character from the UART. The character is examined to see if it is one of the valid command characters (paragraph 10.2). If it is not, the processor resumes testing DR for the next incoming character.
- 10.4 Assume the character just received is the code (05 hex) for a Read Command. The processor checks to see if the tape drive is "ready"; if it is, the Read Command is sent, using the RDY/REQ handshake (as explained in paragraph 6.7).
- 10.5 The interface sets up the PIO in the receive-with-handshake mode; does a dummy read to clear the A-READY line; sets up a buffer memory pointer (one of the buffers used in Write mode); and waits for the tape drive to indicate it has data to transfer.
- 10.6 After the Read Command is accepted by the tape drive, the drive makes the DIR line low (zero volts) causing the LS242 bi-direc-

tional drivers to be set up as inputs. Tape motion is started and a 512-byte block of data is read into the tape drive's buffer memory. The tape drive then asserts the RDY signal to indicate that data is ready to be transferred to the interface.

- 10.7 When it detects that the tape drive has data to send, the processor activates the XFER ENABLE signal and initializes a byte counter (to count 256 bytes). In READ mode, tape data from the tape drive is handled with a polling operation (not with interrupts as in Write mode). However, as with a data transfer in WRITE mode, the READ data transfer is done with a handshake for each byte. The handshake signals are ACK from the tape drive and XFER to the tape drive.
- 10.8 As initialized for the READ mode, the PIO A-READY line is high (+5 v). The A-READY line is connected to PIO port B, bit 7 (pin 34). When the tape drive sends a data byte to PIO port A, the drive brings the ACK line low (zero volts). The low ACK signal triggers the LS123 one-shot, which supplied a narrow pulse to the PIO A-STROBE input. The A-STROBE pulse causes the PIO A-READY line to go low, furnishing a low XFER to the tape drive. The A-READY line will remain low until port A is read by the processor.
- 10.9 The processor repeatedly reads PIO port B and tests bit 7 for a low. When the processor detects bit 7 low, it reads the data byte at port A, stores the byte in buffer memory, increments the buffer pointer and the byte counter. As implied above, reading PIO port A will cause the A-READY line to go high. When A-READY goes high, that causes XFER to the tape drive to

go high. The tape drive detects that XFER has gone high and brings ACK high. Thus, the handshake is completed. The tape drive then sends another byte to port A and makes ACK low; the processor detects A-READY low (at bit 7, port B), reads and stores the byte, increments that byte counter, etc. This process continues until 256 bytes have been transferred and the byte counter is at zero (due to overflow). The process is then repeated for 256 more bytes. The processor then resets the XFER ENABLE signal and waits for the tape unit to make the RDY line low, indicating that the tape drive has another data block ready.

11.0 Assuming no errors occur, the tape drive will continue sending data blocks, and the interface will continue storing them, until the tape drive reads a file mark from the tape. The tape drive will then stop the tape motion and inform the interface of a file mark by way of the EXC signal.

11.1 The processor, detecting the EXC (exception) signal, reads the tape drive status with a Read Status command and determines that a file mark was encountered by the tape unit. The processor then loads the UART with the ASCII character for ACK (06 hex); the UART transmits the character through the level-shifter (TLO-81) to the RS-232C connector, informing the user that a file (3584 bytes) is available in the recorder memory. The tape will remain stopped until the recorder receives another Read Command (see paragraph 10.4). The processor again starts testing the UART DR line, waiting for another input character.

11.2 Assume now that the UART receives a Data Command (12 hex, DC2) from the RS-232 connector. The processor then initializes the buffer memory pointer and sets up a byte counter for 256 bytes. The first data byte is read from the buffer and loaded into the UART. The buffer pointer and byte count are incremented. The UART transmits the character through the RS-232 connector to the user. This process is repeated until 256 data bytes (characters) have been sent.

In the foregoing, before each data character is sent, the processor checks the UART to see if an XOFF character has been received. If no XOFF is present, data transmission continues. If an XOFF is received, the processor ceases transmission and goes into a looping operation until an XON character is received. Upon receipt of an XON, data transmission is resumed. Note that the XON-XOFF control is in effect only during the transmission of each 256 character data block.

11.3 The processor checks to see if the buffer is empty. If it is not, then the ASCII character for DC4 (hex 14) is loaded into the UART and sent to inform the user that 256 data bytes have been sent. If the buffer is empty, the processor loads into the UART and sends the ASCII "SUB" character (hex 1A) to inform the user that the 256 characters just sent was the last of a file. The processor then resumes testing the UART DR line, waiting for another input character.

11.4 The only other command that the recorder will accept is a rewind command. Assume that the UART receives the Rewind Command (52 hex, ASCII for the letter R). The processor translates the

ASCII 'R' into the Rewind Command for the tape drive, and, if the tape drive is "ready", sends the Rewind Command.

11.5 The tape drive recognizes the command and rewinds the tape to BOT (beginning of tape). The drive will then select tape track zero (tracks are numbered 0-8 for 9 track systems). The user must determine when the tape has been rewound.

12.0 The BUFFER MEMORY and address decoding circuits are located on a p.c. board separate from the rest of the interface circuitry. Locating the memory and decoding circuits on a separate board permits memory-size changes to be accommodated more easily. The sixteen address lines and 8 data lines, as well as RD, WR, and MREQ (a memory-cycle signal) from the microprocessor are bussed to the memory board. In addition, various "select" lines are run from the memory board back to the main interface board.

12.1 Address allocations for the various functions will depend upon the particular memory arrangement in use. Of course, firmware changes to the various pointers in use must be made to agree with the memory configuration.

12.2 As supplied, the memory board contains a total of 8K of ram. This 8K is made up of four 2K x 8 CMOS rams (HM6116). The 8K of memory is split into two blocks of 4K, referred to as LORAM and HIRAM.

12.3 The first 3584 locations of HIRAM and LORAM are used as the two data buffer memories. The remaining 512 locations of each 4K block are used for other purposes. In LORAM, the upper 512 locations are used as auxiliary ram, to store status, etc. In

HIRAM, the upper 512 bytes are used as the processor stack. The Z-80B microprocessor requires its stack to be in external ram. the stack is arranged as a "push-down" stack; that is, the stack pointer is decremented during each load operation, and incremented during each unload operation. Therefore, the stack pointer is initialized to point to the high end of HIRAM. Each stack operation utilizes 2 locations (16 bits) in the stack.

12.4 Memory address allocations presently in use are as follows:

ROM	0000H to 0FFFH (operating program)
LORAM	1000H to 1FFFH
HIRAM	2000H to 2FFFH
STACK	2FF0H (initialized at top)
AUXRAM	1E10H to 1FFFH
DATBUF A	1000H to 1DFFH
DATBUF B	2000H to 2DFFH

12.5 Select lines (which are combined with RD or WR) are decoded from address lines as follows:

RDUART	3000H	(UART read enable)
LDUART	4000H	(UART load pulse)
UARTST	5000H	(UART status read)
ERLACH	6000H	(error latch, write only)

Error latch drives front panel indicators and supplies XFER ENABLE signal. Unused address space is from 7000H to FFFFH (for the 16-bit address capability).

12.6 It should be mentioned that the LS259 (3/8 decoder) supplies high true outputs, but all outputs are low except during the time that MREQ is low. The MREQ and IORQ signals from the

Z-80B microprocessor are used to distinguish between memory-type operations and input/output operations. The LS-259 decoder insures that addresses on the address bus will be active for the memory board only during memory-type operations.

13.0 The FRONT PANEL consists of the cartridge slot on the tape drive, various control switches for reset, baudrate, power, and read/write selection, and the SAIL and RS-232 connectors. In addition, there are various indicator lights on the panel, as follows:

BAUD -- (Write mode) when blinking, indicates that the incoming data baudrate and the recorder baudrate are not in agreement.

CARTRIDGE -- (Read or Write mode) indicates that a cartridge is not in place.

SAFE -- (Write mode) indicates that a cartridge is in a "safe" (write protected) condition. Recording cannot be accomplished.

DATA -- (Read or Write mode) indicates that an unrecoverable data error occurred.

END -- (Write mode) indicates that the end of tape has been reached (all nine tracks have been recorded).

FATAL -- (Write mode) indicates that a fatal error has occurred and that the cartridge should be replaced.

PWR FAIL -- Indicates that a.c. power to the recorder has been interrupted. If failure occurs during the recording process, the cartridge must be replaced and the power brought back up.

READ -- This light does not indicate an error condition. It serves to warn the operator that the unit is in the READ mode, and of course will not record data.

13.1 In the upper right corner of the front panel is a 4-digit LED display. This display indicates the amount of data recorded on a tape. The display counter counts files as they are recorded. Each file is presently 3584 bytes, so each time the display value increases by one, that indicates that an additional 3584 bytes (ASCII characters) have been recorded. When the display (counter) value reaches 9800, the audible alarm is sounded and the END light should flash. This serves as an early warning that the tape is nearly full and should be replaced before data is lost. There should be approximately ten files (35000 bytes) capacity remaining on the tape. But if the tape actually reaches its end, the tape drive will reject subsequent data. The RESET switch must be operated to clear the alarm condition.

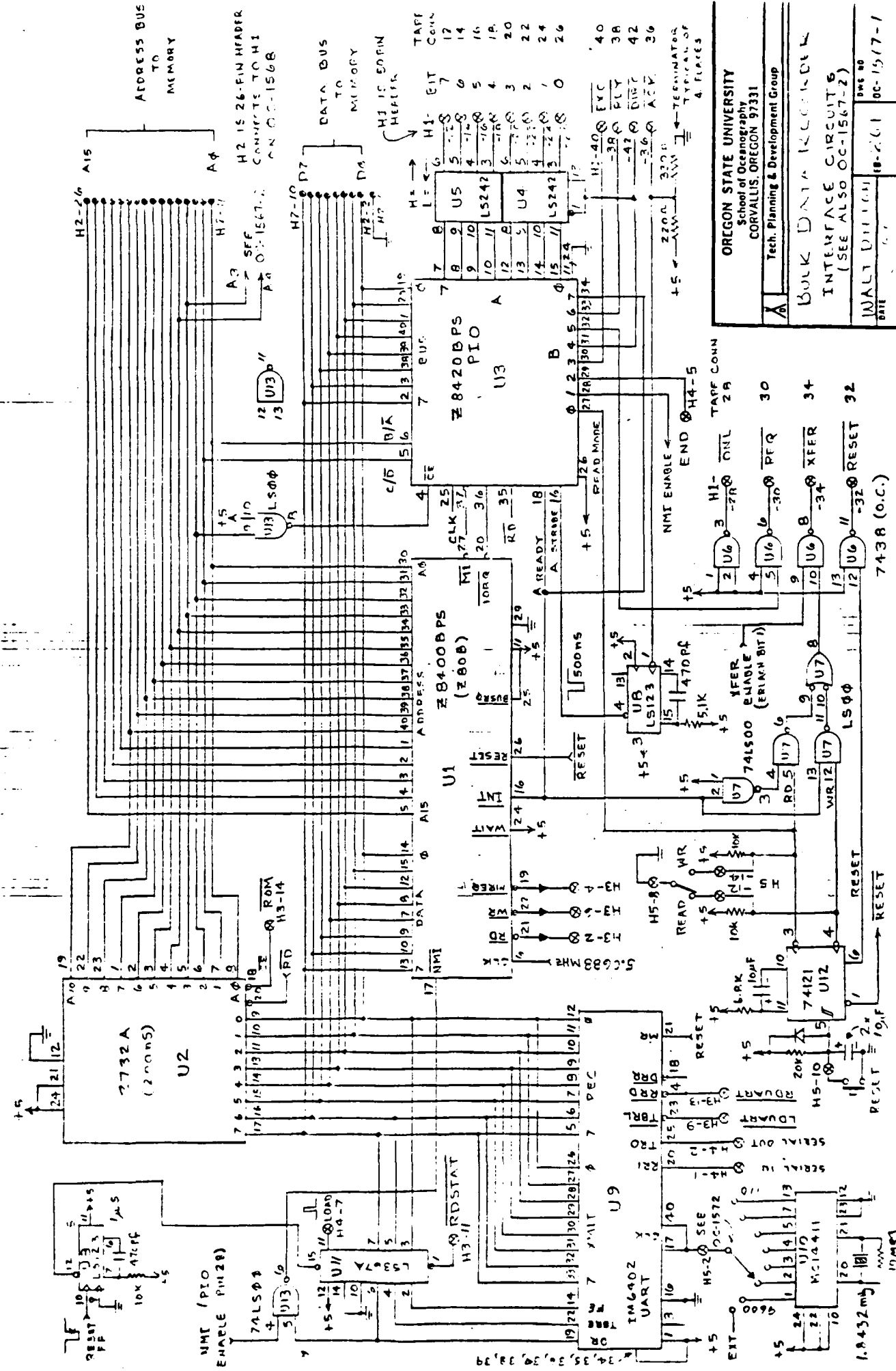
14.0 The POWER CONTROL circuits utilize a "drop-out" relay to control the application of a.c. power to the d.c. power supplies. The Bulk Data Recorder requires +5 volts d.c. at 3 amps and +24 volts at 1.5 amps (or +12 volts, depending on the tape drive utilized).

14.1 Because data cannot be appended to a partially written tape, provision must be made to accommodate a power failure, which would interrupt the recording process. The drop-out relay mentioned above serves as a power-fail detector, and insures that the user is warned that a power failure has occurred.



- 14.2 Referring to the power control schematic (OC-1569) relay K1 is shown de-energized. Primary power (120 vac) is applied to the d.c. power supplies through the contacts of relay K1 and the 3-position power switch. When the power cord is first connected to the 120 V source, the relay is not energized, so no voltage reaches the power supplies.
- 14.3 Power does reach the PWR FAIL indicator and the lower contact on the power switch. The PWR FAIL indicator on the front panel should be illuminated. Moving the toggle handle of the power switch to the lower (momentary) position energizes the relay coil, extinguishing the PWR FAIL indicator and applying power to the cooling fan and to the center (common) contact of the power switch. When the power switch handle is released, it will return to the center position.
- 14.4 Then, moving the switch handle to the upper position applies 120 vac to the two d.c. power supplies, thus providing d.c. power for the data recorder circuitry. The relay will remain energized due to current flow through its holding contacts and the relay coil. The d.c. power may now be controlled at will by use of the power switch. Note that the fan will continue to operate even though d.c. power may be off.
- 14.5 If a power failure occurs, either due to loss of primary power or to a blown fuse, the relay will lose power and become de-energized. When the relay "drops out", power will be removed from the fan and from the d.c. supplies. The back-contacts of the relay will cause the PWR FAIL indicator to be lighted, if or when primary power is available to the power cord. The

audible alarm will not sound, since there is no d.c. voltage  
from which to drive it.



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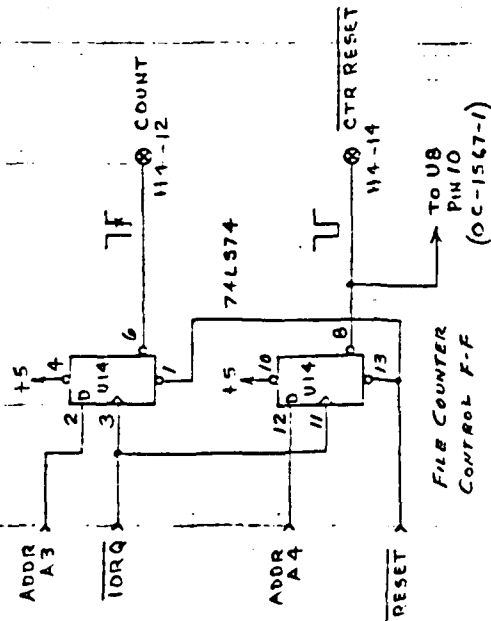
BULK DATA RECORDING  
 INTERFACE CIRCUITS  
 (SEE ALSO OC-1547-2)

WALT DUNN  
 DATE 10-2-61

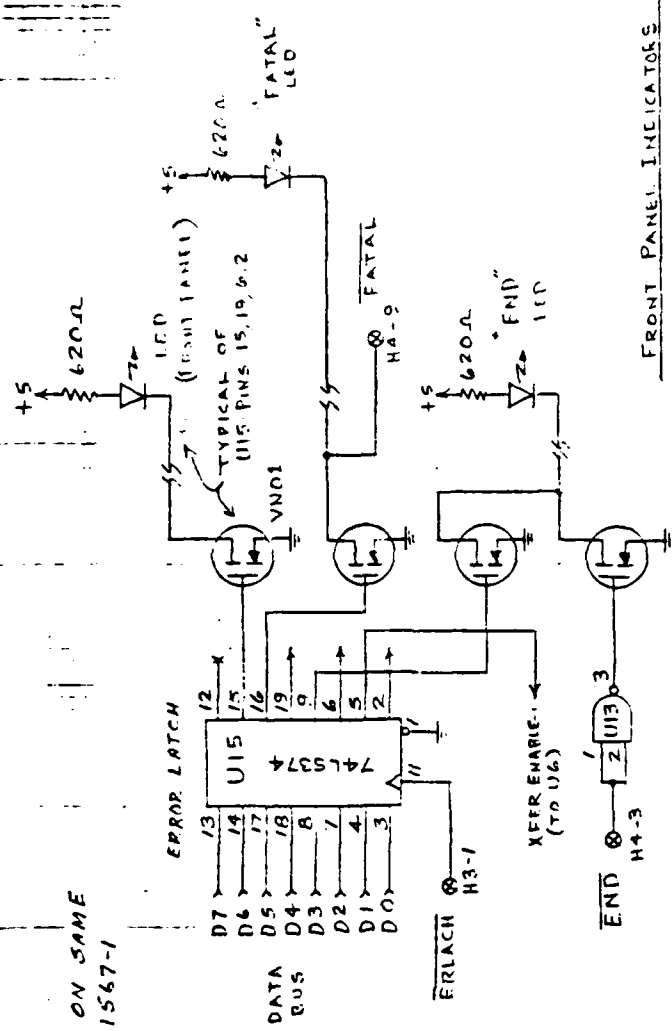
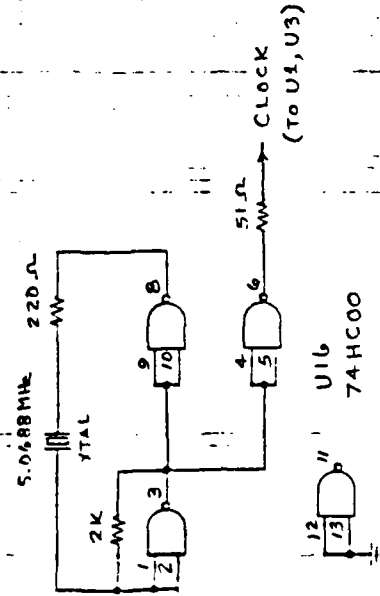
DWS 80  
 OC-157-1

7438 (O.C.)

CIRCUITRY SHOWN HERE IS ON SAME BOARD AS THAT FOR OC-1567-1



FILE COUNTER CONTROL F-F



FRONT PANEL INDICATORS

DATA BIT	LATCH OUT
BAUD	0
DATA	2
END	3
SAFE	4
FATAL	5
CARTRIDGE	6

OC-1567-1, -2  
HEADER CABLEING

- H1 CONNECTS TO TAPE DRIVE
- H2 CONNECTS TO H1 ON OC-156A
- H3 CONNECTS TO H2 ON OC-156A
- H4 CONNECTS TO H1 ON OC-1569
- H5 CONNECTS TO H2 ON OC-1572

- 42 - DOT INDICATES
- 2 0 0 1
- 4 0 0 3
- 6 0 0 5
- 8 0 0 7
- 10 0 0 9
- 12 0 0 11
- 14 0 0 13
- 16 0 0 15
- 18 0 0 17
- 20 0 0 19
- 22 0 0 21
- 24 0 0 23
- 26 0 0 25
- 28 0 0 27
- 30 0 0 29
- 32 0 0 31
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- 84 0 0 83
- 86 0 0 85
- 88 0 0 87
- 90 0 0 89
- 92 0 0 91
- 94 0 0 93
- 96 0 0 95
- 98 0 0 97
- 100 0 0 99

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BULLA WITH A RECORDER  
PART OF INTERFACE CIRCUITS

UNIT DIRECTOR: 18-261  
DATE: 4-1-77

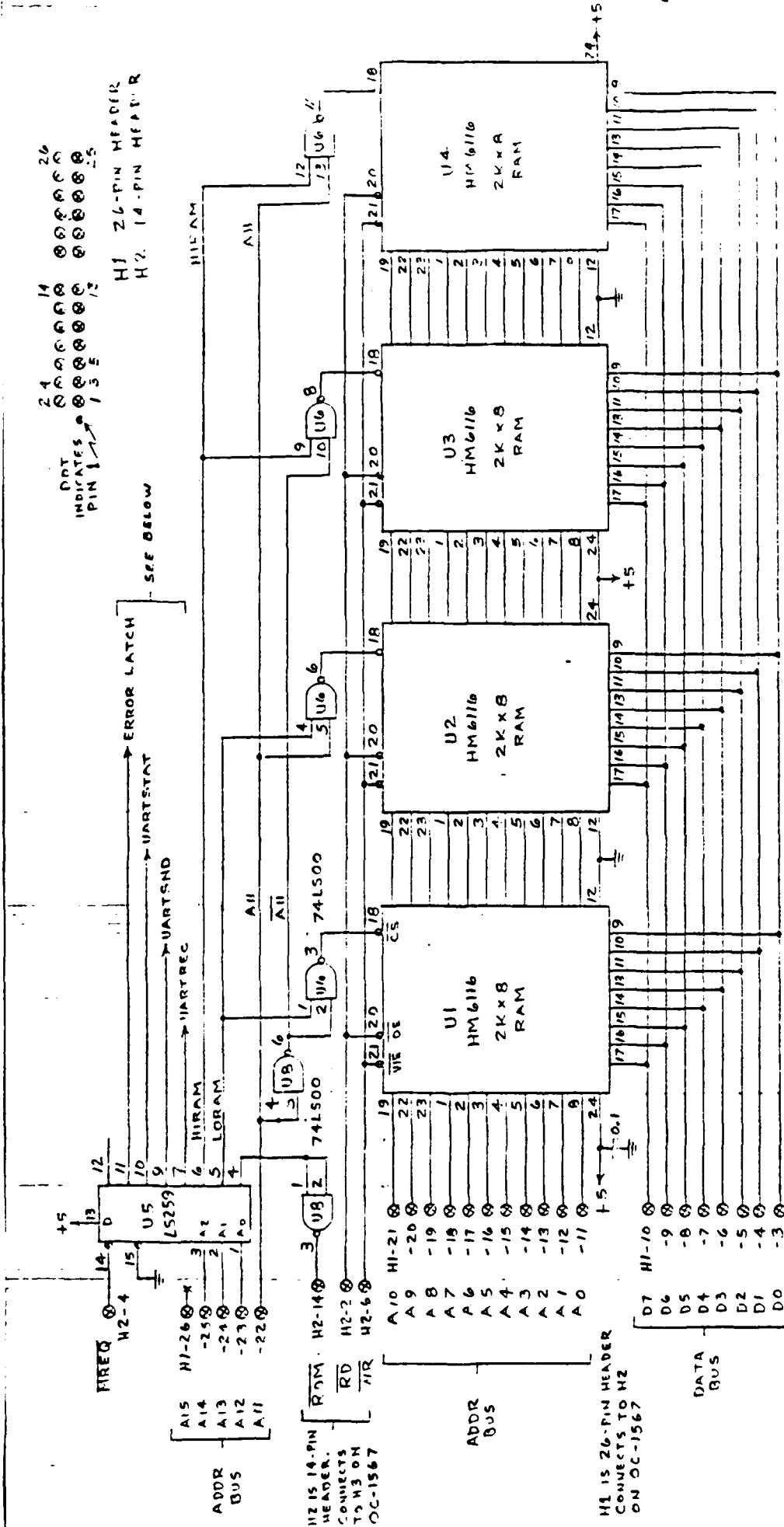
DESIGN NO: OC-1567-2

DPT INDICATES PIN 1

24	14	26
00000000	00000000	00000000
00000000	00000000	00000000
135	13	25

H1 26-PIN HEADER  
H2 14-PIN HEADER

SEE BELOW

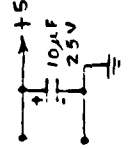
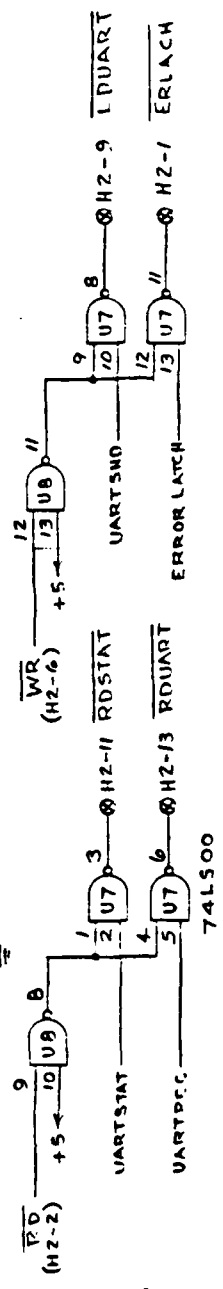


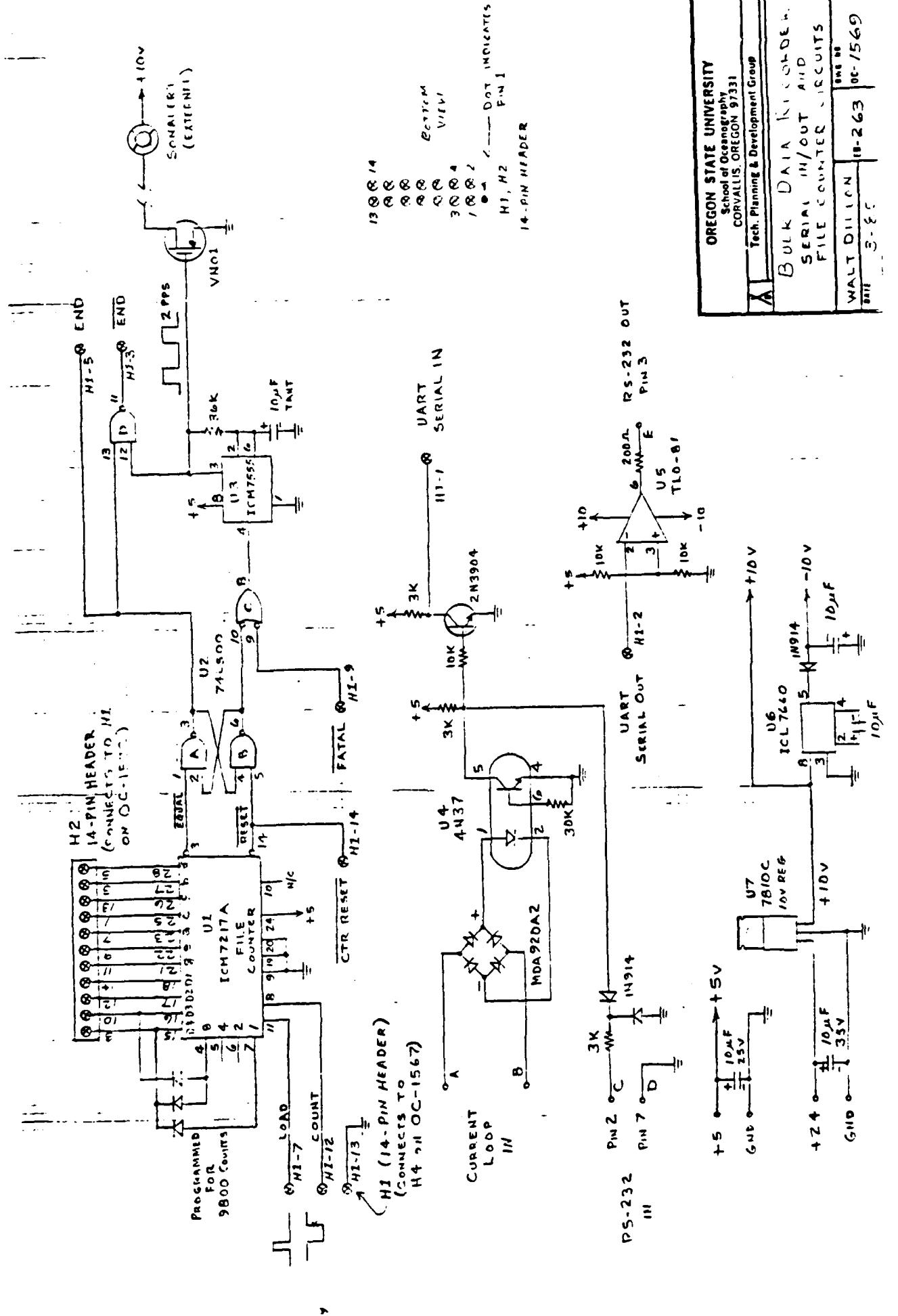
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BULK DATA DECODER  
MEMORY AND DECODE CIRCUITS

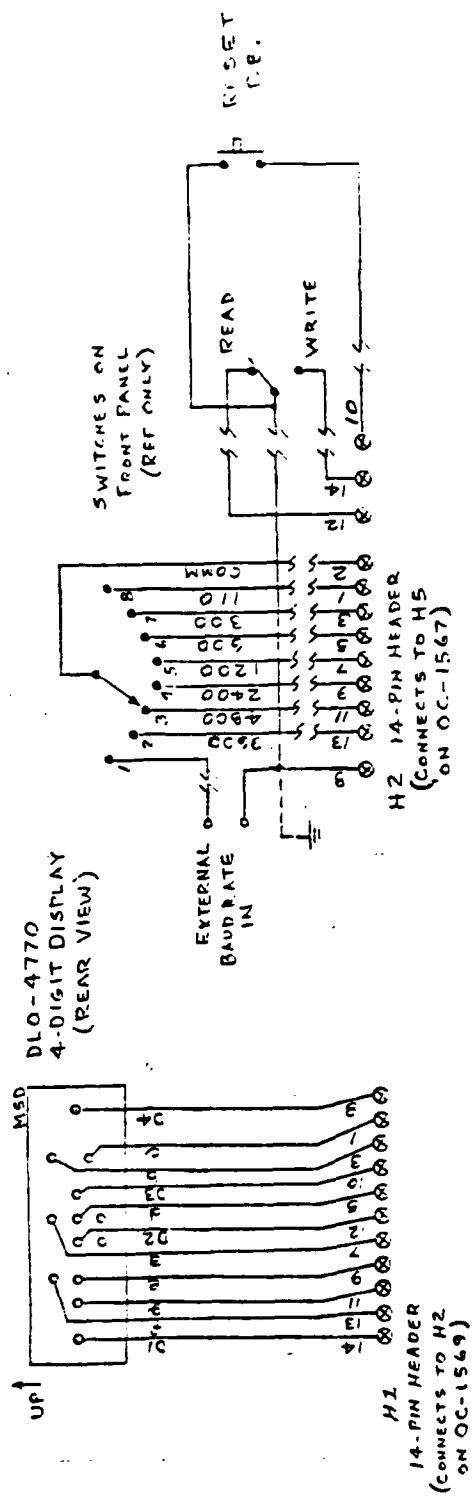
WALT L. L... 18.262 Pr. 1/568





13 Ⓞ 14  
 Ⓞ Ⓞ  
 Ⓞ Ⓞ  
 3 Ⓞ 4  
 1 Ⓞ 2  
 HI, H2 - DOT INDICATES  
 - PIN 1  
 14-PIN HEADER

OREGON STATE UNIVERSITY School of Oceanography CORVALLIS, OREGON 97331 Tech. Planning & Development Group		BULK DATA RECORDER SERIAL IN/OUT AND FILE COUNTER CIRCUITS	PAGE NO 18-263	OC-1569
A				
WALT DILLON 18-263 3-8-C				

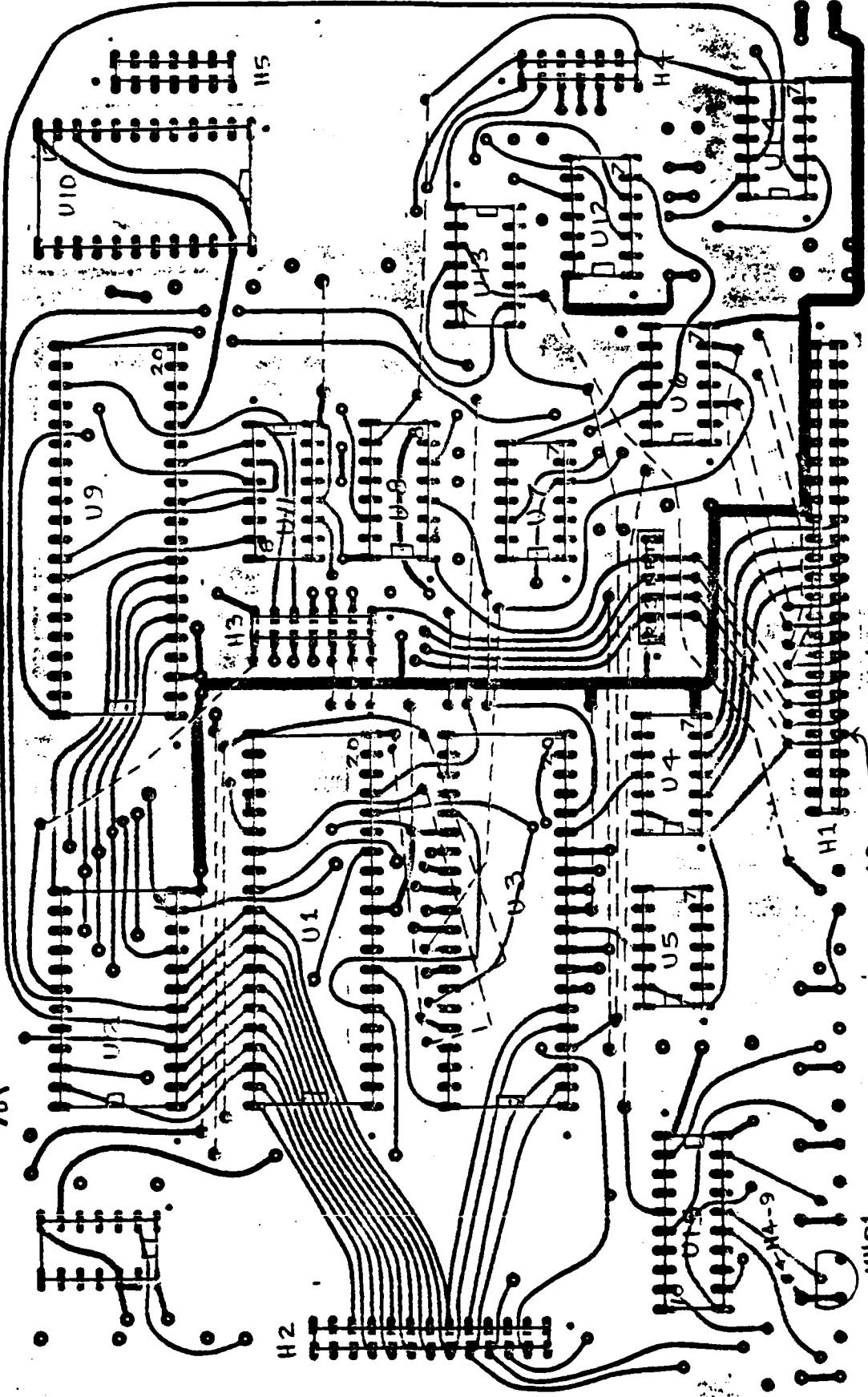


- 14 ● ● 13
  - ●
  - ●
  - ●
  - ●
  - 4 ● ● 3
  - 2 ● ● 1
  -
- DOT INDICATES PIN 1.
- H1, H2  
14-PIN HEADER

OREGON STATE UNIVERSITY School of Oceanography CORVALLIS, OREGON 97331	
Tech. Planning & Development Group	
BULK DATA RECORDER FILE COUNT DISPLAY BOARD (FRONT PANEL)	
PROJECT NUMBER	OS-264
DATE	3-5
DSG NO	OC-1572

OSU TP&D EB-261

A



PIN 42 BULK DATA RECORDER  
INTERFACE CIRCUITS  
EB-261 OC-1567-1, -2

JUMPER PLAN  
SEE ALSO JUMPER LIST  
INSULATED JUMPER



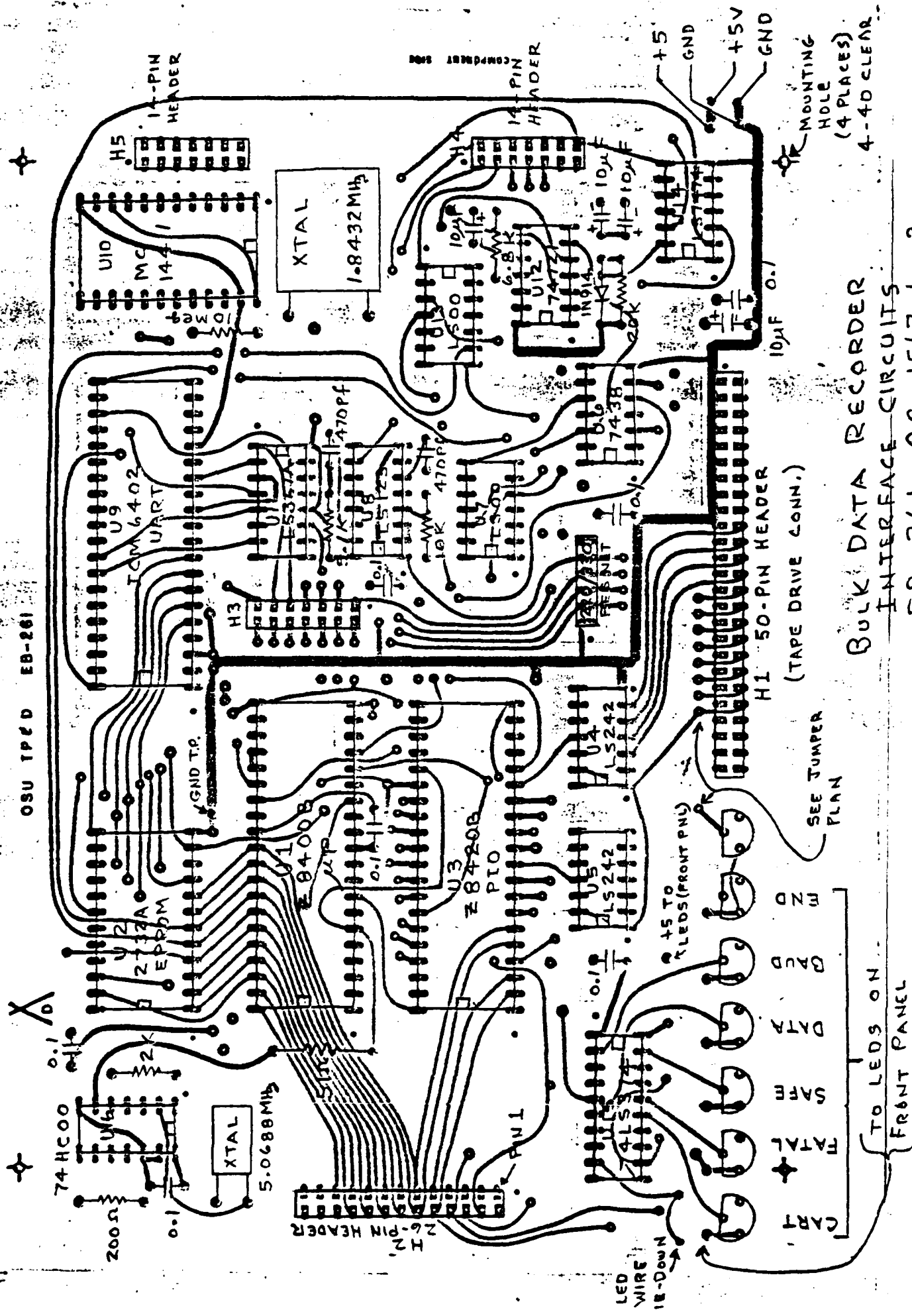
BULK DATA RECORDER  
EB-261 OC-1567-1,-2

JUMPER LIST

Device-Pin	Connects To	Device-Pin
U1-20		U14-3
U1-26		U12-1
U3-27		U7-5
U3-28		U13-4
U3-29		H4-5
U3-30		H1-40 (resistor network)
U3-31		H1-42 " "
U3-33		H1-38 " "
U11-11		H4-7
H4-9		VN01

See Also Jumper Plan

OSU TPED EB-261



**BULK DATA RECORDER  
INTERFACE CIRCUITS**

EB-261 OC-1567-1, -2

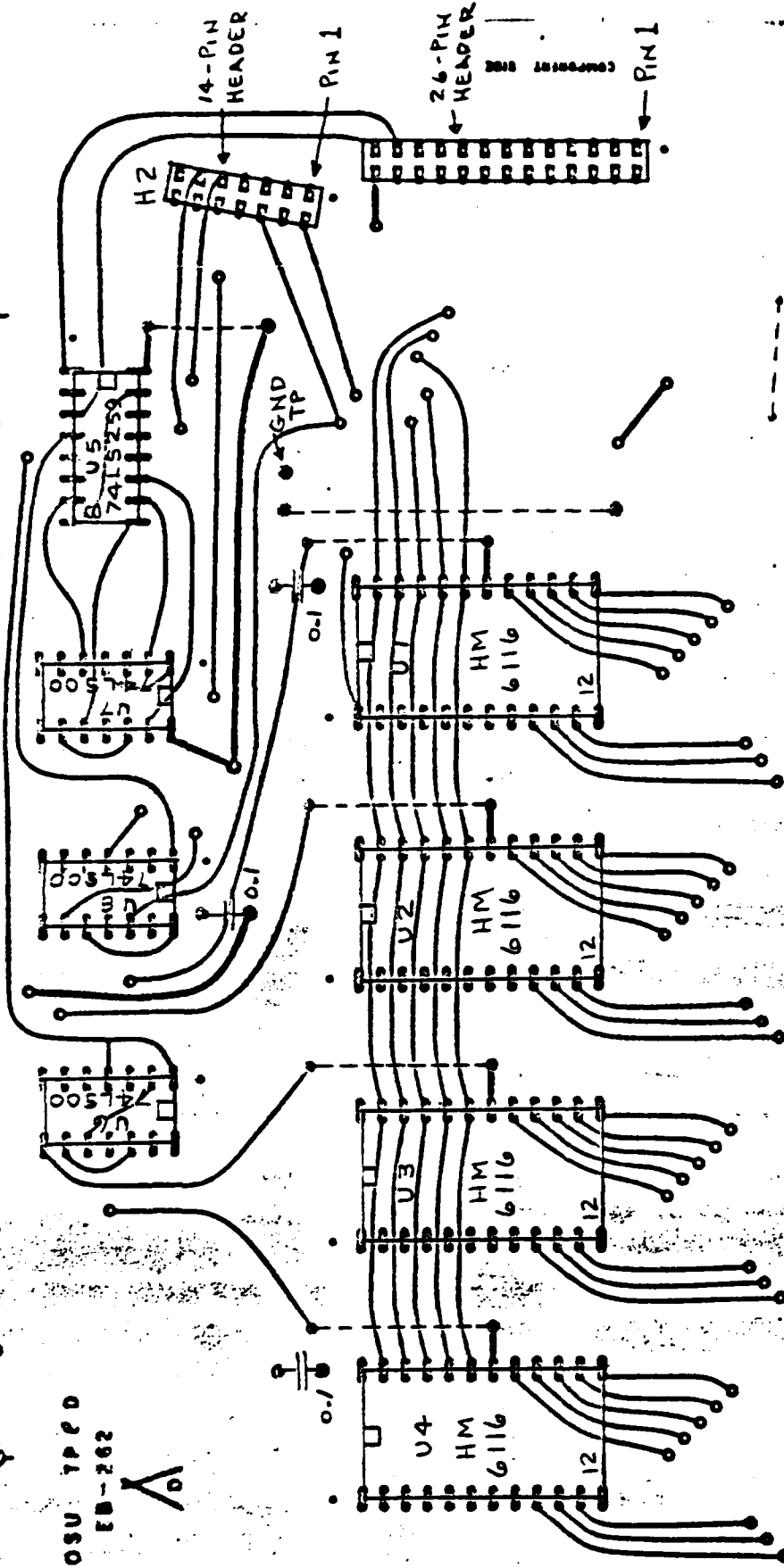
MOUNTING HOLE (4 PLACES)  
4-40 CLEAR

H1 50-PIN HEADER (TAPE DRIVE CONN.)

SEE JUMPER PLAN

TO LEDS ON FRONT PANE

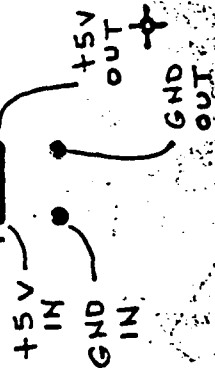
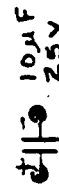
OSU TPD  
EB-262

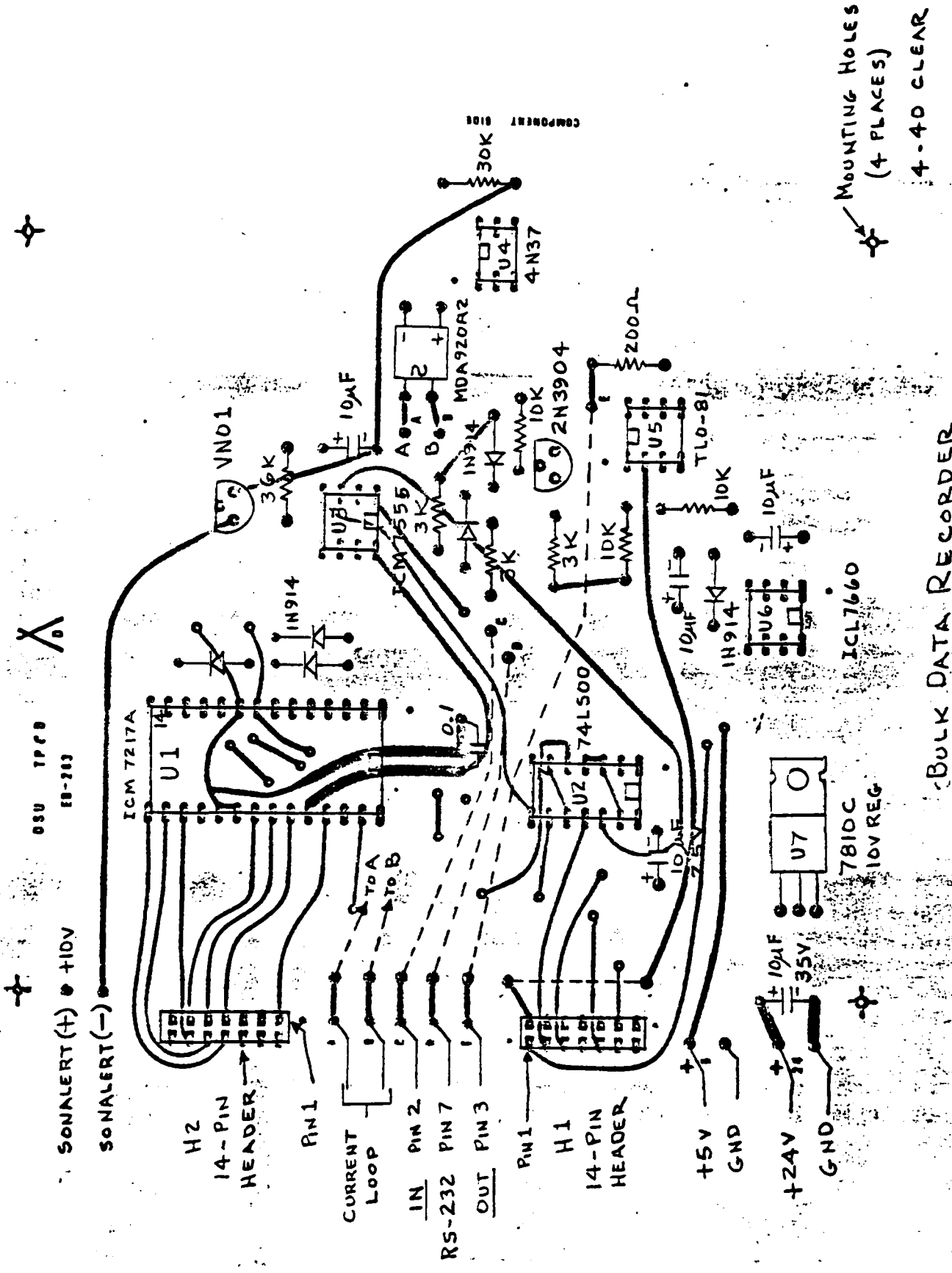


DEUTES INSULATED  
JUMPER (6 PLACES)

MOUNTING HOLES  
(4 PLACES)  
4-40 CLEAR.

BULK RECORDER  
MEMORY BOARD  
EB-262  
OC-1568





OSU TPCB  
EB-203

SONALERT (+) +10V  
SONALERT (-)

H2  
14-PIN  
HEADER

CURRENT  
Loop  
IN PIN 2  
OUT PIN 3

RS-232  
IN PIN 2  
OUT PIN 3

H1  
14-PIN  
HEADER

+5V  
GND

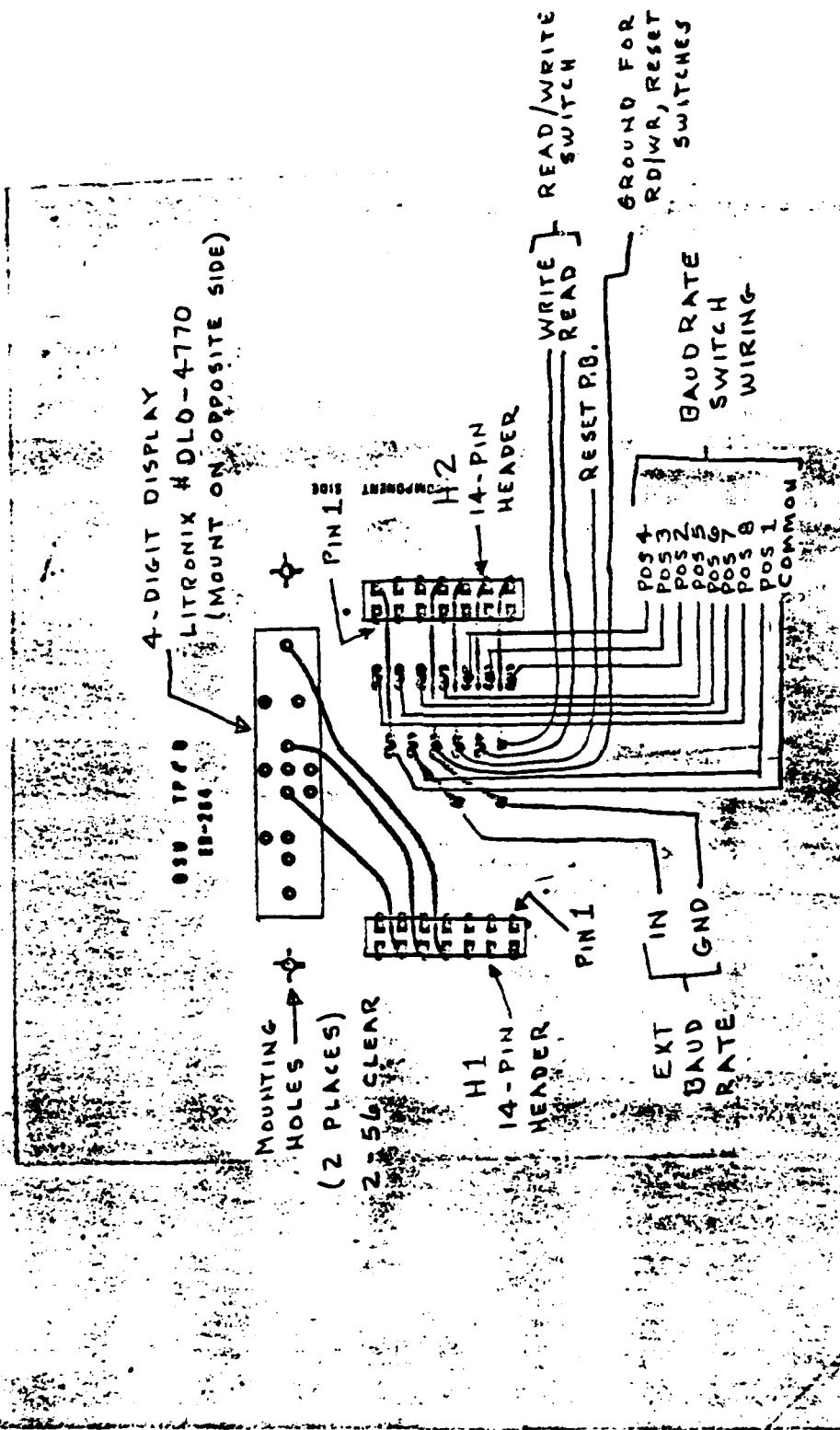
+24V  
GND  
U7  
7810C  
10V REG

ICL7660

Mounting HOLES  
(4 PLACES)  
4-40 CLEAR

BULK DATA RECORDER  
SERIAL-IN/OUT & FILE COUNTER  
ED 263 OC-1569

COMPONENT  
SIDE



BULK DATA RECORDER  
 DISPLAY BOARD  
 (FRONT PANEL)  
 EB-264  
 OC-1572

PARTS / ORDER LIST

Assembly Description Bulk Data Recorder  
Interface Board

E.B. 261

Date 2/85

P.O. OC-1567

ITEM	QUAN.	PART NO.	MANUFACTURER	DESCRIPTION	ORDER #		DATE
					QUAN.	VENDOR	
	1	Z84008BPS	ZILOG	Microprocessor		KIERULFF	
	1	Z8420BPS	ZILOG	PIO		"	
	1	2732A	Various	4K x 8 EPROM, 200ns			
	1	IM6402	INTERSIL	UART, CMOS			
	1	MC14411P	MOTOROLA	Bit-Rate Generator			
	1	SN74LS374N	T.I.	Octal D Flip-Flop			
	1	SN74LS367AN	"	3-State Buffer			
	2	SN74LS242N	"	Quad Bus Transceiver			
	1	SN74LS123N	"	Dual One-shot			
	1	SN74121N	"	One-shot			
	1	SN74LS74N	"	Dual D-Flip-flop			
	1	SN7438N	"	Quad 2-in Nand buffer			
	2	SN74LS00N	"	Quad 2-in Nand Gate			
	1	MC74HC00N	MOT	Hi-speed CMOS 2-in nand			
	7	VN0104N3	Supertex, Inc. 714)533-0481	DMOS Transistor, N-Type		Zepher	
	1	IN914	--	Silicon Diode			
	1	4305R-104-221/331 C06-5-221/331-J	Bourns TRW	Terminator Resistor Network, 6 pin SIP		Bourns = J.J. Backer, Portland TRW = Hamilton/Avnet	

Assembly Description Bulk Data RecorderE.B. 261Interface BoardDate 2/85P.O. OC-1567

ITEM	QUAN.	PART NO.	MANUFACTURER	DESCRIPTION	ORDER #	
					QUAN.	DATE
1				Resistor, 10 MEG, 1/4 W ± 5%		
1				" 20 K		
3				" 10K		
1				" 6.8K		
1				" 2K		
6				" 620 Ω		
1				" 220 Ω		
1				" 51 Ω		
4				Capacitor, 10μF25V, TANTALUM		
8				" 0.1μF Monolithic ceramic		
2				" 470 pf		
1						
1			FOX SEIKO	Crystal, 5.0688 MHz		
1			SEIKO	Crystal, 1.8432 MHz with wire leads		
4			A/EPCO	7-Pin Pin Strip (header)		
2			"	13-Pin "		
2			"	25-Pin "		
1			OSU-TP & D	Etched Circuit Board		
		EB-261				





Assembly Description Bulk Data Recorder  
~~Serial Data/File Counter~~

E.B. 263Date 2/85P.O. OC-1569

ITEM	QUAN.	PART NO.	MANUFACTURER	DESCRIPTION	ORDER #	
					QUAN.	DATE
				CMOS		
	1	ICM7217A1PI	Intersil	4-Digit BCD Coincidence Counter		
	1	SN74LS00N	T.I.	Quad 2-in nand Gate		
	1	ICM7555IPA	Intersil	CMOS Timer		
	1	TL0-81	T.I.	OP-AMP (BI-FET)		
	1	4N37	MOT	OPTO-Coupler		
	1	ICL7660	Intersil	Negative Voltage Converter		
	1	7810C	"	Voltage Regulator, 10V		
	1	VH0104N3	Supertex	DMOS Transistor, N-Type		
	1	2N3904	"	Transistor, NPN		
	6	1N914	"	Silicon Diode		
	1	HDA920A2	Mot	Bridge Rectifier		
	1			Resistor, 30K, $\pm$ 5% 1/4 W		
	3			" 10K "		
	3			" 3K "		
	1			" 220 $\Omega$ "		
	1			" 36K "		
	5			Capacitor, 10 $\mu$ F 35V, Tantalum		
	2			" 0.1 $\mu$ F Monolithic ceramic		
	4	22-03-2071	M&PCO	7-Pin Pin Strip (header)		
	1	EB-263	OSU-TP & D	Etched Circuit Board		

Assembly Description Bulk Data Recorder  
Power Control/Front Panel and Misc

E.B. 264Date 2/85

P.O. \_\_\_\_\_

ITEM	QUAN.	PART NO.	MANUFACTURER	DESCRIPTION	ORDER #	
					QUAN.	VEH DOR DATE
1		B 5-3	Condor	DC Power Supply 5V @3A		
1		B24-1.2	"	" " 24V @1.2A		
1		KUP5A15-120V	Potter & Brumfield	Relay, SPDT		United Radio
1		27E043	"	Relay Socket w/hold-down spring #200228		
1		35-086	G C Electronics	Switch, toggle, on-off-MOH SPDT		Radar
1				Lamp, Neon, 12 VAC w/resistor		
1				Fuseholder, extraction type 1 1/4" Fuse		
1		MTL-106D	ALCO Switch	Switch, SPDT, locking toggle		ACMAC
1		MRS-1-10	ALCO Switch	Switch, rotary, 10 Pos 1 Pol 36°		
1				Switch, Pushbutton, N.O.		
1		DB-25S	TRW Cinch and others	Connector, 25 Pin female (RS-232)		
1		<del>44-103-10004</del> 44-102-1914S	Amphenol	Connector, 4 pin fem (LOOP)		
1				Power cord, 3 cond #18, w/plug 6 ft. long		
7		TIL -220	T.I.	LED, RED, 0.2" Dia		
7		-	T.I.	Mounting Bushing for LED		
1		DLO 4770	Litronix (Siemens)	4-digit LED display, C.C. MPX		Hamilton Avnet
1		SNP428	Hallory	Sonalert (audible alarm)		Radar
1				Fan		
1				Enclosure		
1		EB-264	OSU-TP & D	Etched Circuit Board		

**END**

**FILMED**

7-85

**DTIC**

