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A SAMPLING PHASEMETER DESIGN FOR PULSED CONTINUOUS WAVE SIGNALS

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A continuous wave phasemeter was designed with the capability to operate with short duration pulses of continuous wave signals (pulsed cw) in a background of noise. An exclusive-OR gate provides the phase detection between the input signal and a reference signal. Sample and hold devices are used to provide the capability of averaging phase fluctuations from one pulse to another. The unique concept of quadrature phase logic is implemented in achieving a truly linear transfer curve even with the presence of noise in the input signal.

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I. INTRODUCTION

This report documents the sampling phasemeter designed for use in an acoustic scattering experiment in a laboratory water tank. Since the objective of the experiment is to obtain measurements of acoustic pressure field variations, amplitude and phase measurements are necessary.

Two methods are commonly used to measure the pressure field with a sonar transducer. The first is to analog record the output of the transducer for subsequent digitization and processing on a digital computer. The other method is to use realtime instrumentation for retrieval of the amplitude and phase. The latter method is preferred because errors in the experiment can more easily be detected and corrected.

Amplitude measurements are made in realtime with voltmeters which measure the voltage output (peak, rms, average, etc.) of the transducer, the voltage being proportional to the pressure amplitude. Continuous wave (cw) phasemeters are used to measure the transducer signal phase relative to a reference signal. However, when pulsed cw signals are used (for example, in the laboratory water tank), the measurement of phase is complicated in that the pertinent phase information is contained in a shorter period of time. Even in the best experimental environments, phase measurement is confused by noise, either acoustic or electronic, and the effects of noise have to be reduced. The phasemeter described in this report has been specifically designed to operate with pulsed cw signals in a background of noise.

II. CONCEPTS OF SAMPLING PHASE DETECTION

In this section the concept of pulse phase detection is developed assuming a minimum of background knowledge in electronics or electrical engineering. The conceptual design is described in block diagram form, dividing the operation of the device into three basic blocks: a linear transfer function phase detector, a pulse averager, and a noise compensation circuit.

Figure 1 is a general description of the sampling phasemeter design. Block I, the averaging phase detector, yields an average phase ϕ of the signal relative to a reference signal over a number of cw cycles. Block II is the pulse phase averager which averages the phase variation over a sequence of pulses. If the reference signal is shifted by 90° and the signal phase determined with blocks I and II, the quadrature phase of the signal results. Block III corresponds with the noise compensation necessary for accurate phase retrieval. Both the actual signal phase and the quadrature signal phase are necessary inputs for block III, the operation of which is described below. Figure 2 represents the predicted output of each of the blocks of the phasemeter under various operating conditions.

The phase detector of block I must have a full operating range of 360° and possess a single-valued linear transfer function to map a continuous variation of a signal's phase. A phase detector is chosen which yields a voltage output linearly proportional to the absolute value of the signal phase between -180° and 180°. This results in a transfer function (represented in Fig. 2 by the solid curve) which is linear with a positive slope for phases between 0° and 180°, or voltages between the values V0 and V180, respectively. For a phase between 0° and -180°, the line has a negative slope which results in a triangular wave for a noiseless cw signal and continuously varying phase. However, this means that the distinction between plus and minus phases must be made in addition to the detection of the magnitude of the absolute phase. With

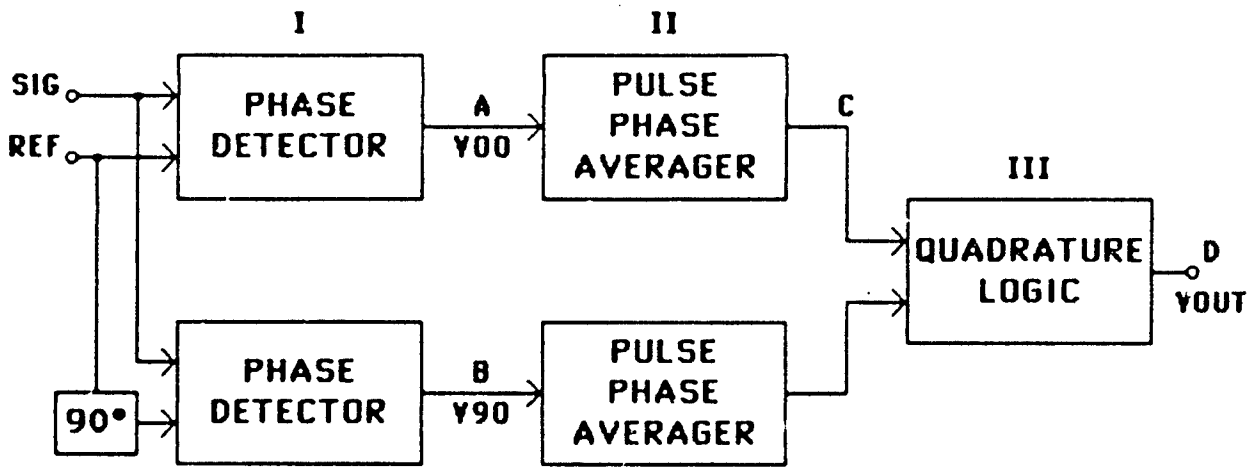


FIGURE 1
SAMPLING PHASEMETER BLOCK DIAGRAM

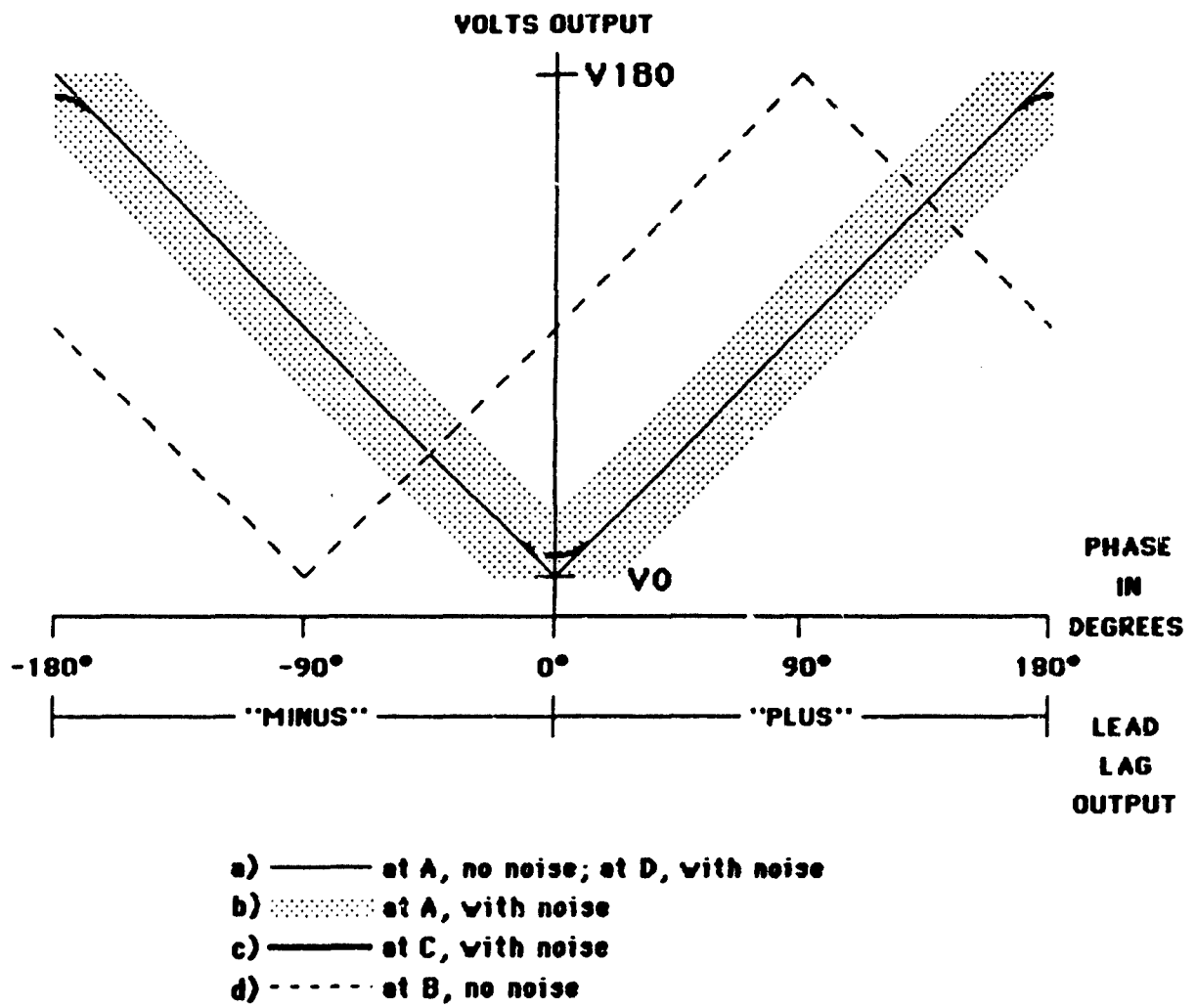


FIGURE 2
SAMPLING PHASEMETER TRANSFER FUNCTIONS

noise added to the signal, the phase fluctuates with the noise, which is represented with the ambiguous output at A, or the shaded region of Fig. 2.

Block II is used to detect a pulsed cw signal phase. A sample and hold (S/H) device samples the output of block I during the time period of the pulse and holds a value of the phase before the pulse dies out. The hold period of the S/H should be long enough to hold the value of the phase until the occurrence of the next pulse. Then any pulse-to-pulse difference is averaged over. If we assume a noise distribution which results in a zero-mean variation of the phase, an averager will optimally determine an estimated phase of a noisy signal. Thus with pulsed cw operation, the output at point C is represented by the wide solid line in Fig. 2 whenever noise is added to the signal. Note the traces of nonlinearity in the output at the transition points of $\pm 0^{o}$ and $\pm 180^{o}$. As the signal phase fluctuates due to the noise, the absolute value operation of block I will yield biased phase estimates for the transition points when the pulse-to-pulse phase is averaged.

One method which could be used to reduce the bias is to perform an algebraic average of the phase with knowledge of the sign of the phase at the transition points. But rather than keep up with the sign of the phase variation in the averaging process, a unique approach is taken to achieve a linear transfer function. This approach requires knowledge of the quadrature shifted phase of the signal as well as the actual phase of the signal. When the transfer functions of both signals are compared at A and B, it should be noted that, when a nonlinearity arises in one of the transfer curves at the transition points, a linear portion of the other transfer curve is present. The only logical conclusion then is to piece together linear portions of these two curves to achieve the desired linear transfer function for phase detection. Thus, the quadrature logic of block III is needed to compensate for the noise in the input signal. With successful piecing together of the transfer curves, the output at D, even with noise, would trace over that at A without noise.

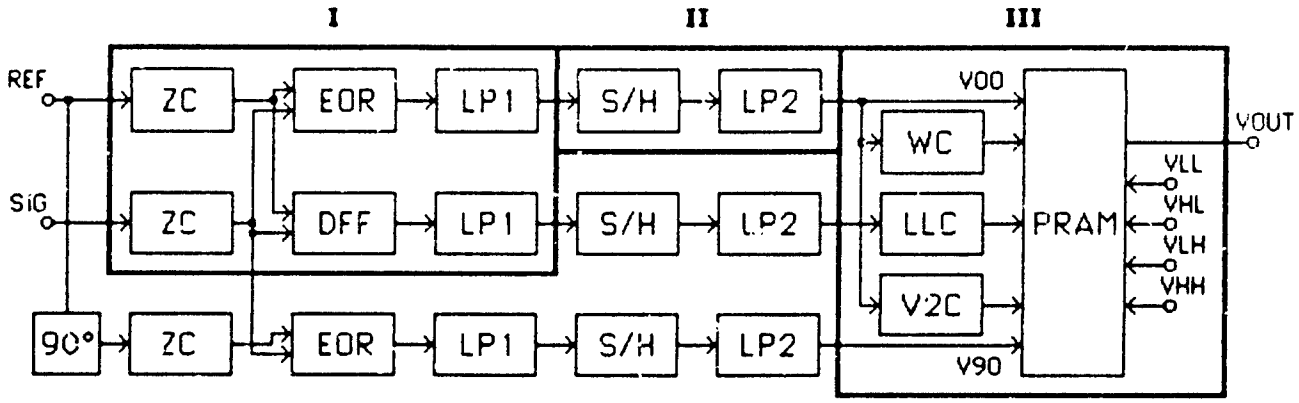
III. CIRCUIT DESIGN REQUIREMENTS

This section is a more detailed engineering description of the block diagram operation of the phasemeter. Figures 3 and 4 provide details at the device level for Figs. 1 and 2, respectively.

The average phase detector (block I) is actually composed of four parts: a zero-crossing detector (ZC), an exclusive-OR (EOR), an integrator (LP1), and a data flip-flop (DFF). The ZC takes a sinusoidal input and outputs a square wave of the same phase. Both the reference signal (REF) and the unknown signal (SIG) are squared with ZC and then input into the EOR. The EOR outputs a train of pulses whose pulse width is proportional to the absolute value of ϕ between the two inputs. This pulse train must then be integrated or averaged with LP1 to yield an average ϕ. Since phase ϕ must be averaged within the duration of the cw pulse, the cutoff frequency of LP1 is determined by the pulse width. Finally, the sign of ϕ must be determined with the DFF. With the preset set to a logic level high and the S/H signal input into the clear (S is high, H is low), REF is input into the data input and SIG is input into the clock input. If the clock is on the rising edge of SIG while REF is low, then the output at Q is low, indicating a leading phase of SIG with respect to REF (or, if REF is high, a lag). The output Q is also averaged over the pulse width with LP1.

The pulse averager (block II) is represented by two parts, a sample and hold (S/H) and an integrator (LP2). The S/H is used to sample the valid part of ϕ (or lead-lag signal) within the cw pulse occurrence and holds the sampled value. The integrator LP2 is then used to average any pulse-to-pulse difference. The cutoff frequency is chosen with knowledge of the repetition rate and the number of pulses over which the averaging is to occur.

The quadrature logic circuit (block III) is implemented with use of a programmable amplifier (PRAM) whose operation is to select portions of the quadrature and normal transfer curves to be combined into a linear



ZC	ZERO-CROSSING DETECTOR	**LP2**	LOW PASS (REP-RATE)
EOR	EXCLUSIVE-OR	**WC**	WINDOW COMPARATOR
DFF	DATA FLIP-FLOP	**LLC**	LEAD-LAG COMPARATOR
LP1	LOW PASS (PULSEWIDTH)	**V2C**	V2 COMPARATOR
S/H	SAMPLE AND HOLD	**PRAM**	PROGRAMMABLE AMPLIFIER

FIGURE 3
CIRCUIT DIAGRAM

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transfer curve. The operation can best be described with Fig. 4. The inputs into the PRAM are the quadrature and normal phase detector outputs (V90 and V00), three logic comparator outputs (WC, LLC, and V2C), and four dc level signals (VLL, VHL, VLH, and VHH) used in the quadrature and normal curve combinations. The window comparator (WC) output is low whenever the V00 output is within a certain voltage range corresponding to the range of phases $135^{o} < \phi < 45^{o}$, and high otherwise. When the WC is low this means the normal transfer curve is selected, and when WC is high the linear portions of the quadrature curve are selected. The V2C and LLC are used to make the decisions required to piece together the quadrature curve with the normal curve. LLC is low for a leading phase and high for a lagging phase. V2C is high whenever the V00 output is less than a voltage corresponding to a phase of $\phi = 90^{o}$. With the four possible logic combinations of V2C and LLC, the appropriate decisions are made by the PRAM to piece the quadrature curve with the normal curve.

COMPARATOR	LOGIC STATE							
LEAD-LAG	HIGH				LOW			
V2	LOW		HIGH				LOW	
WINDOW	HIGH	LOW		HIGH		LOW		HIG I
PRAM OPERATION	V90 +VLH	V00	V00	VHH -V90	V90 -VHL	V00	V00	VLL -V90

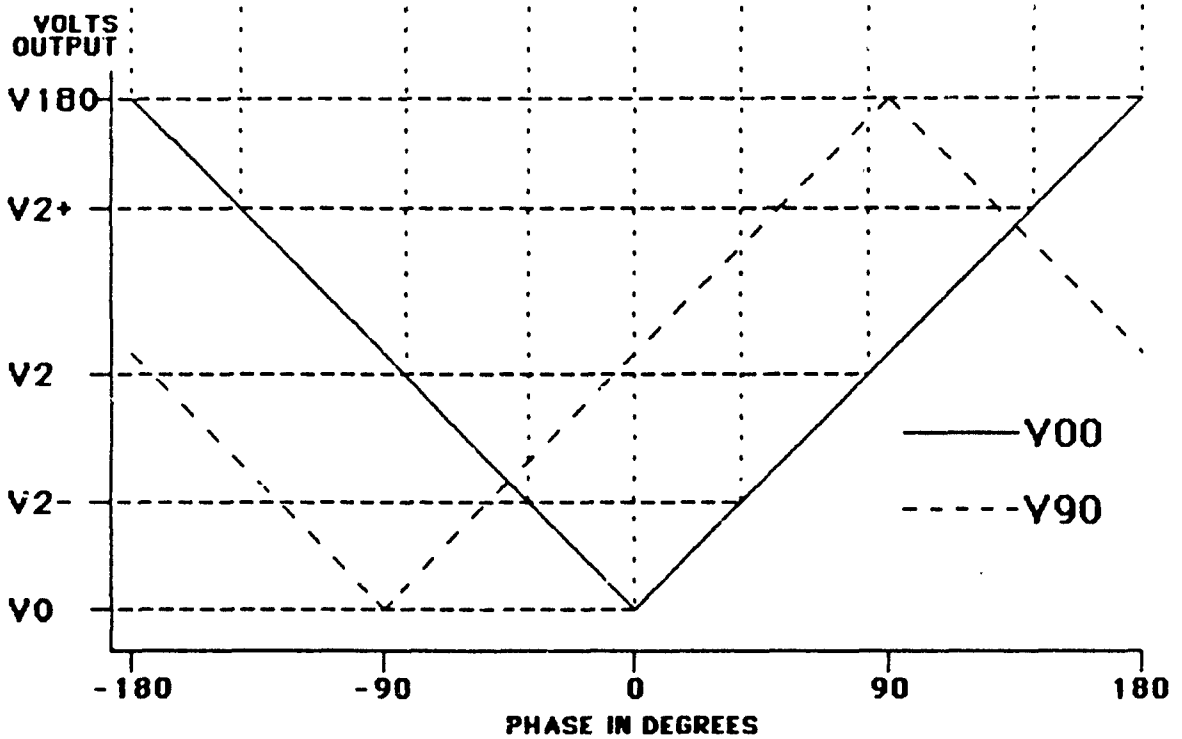

FIGURE 4
QUADRATURE LOGIC OPERATIONS

IV. CIRCUIT SOLUTION, CALIBRATION, AND TESTING

The electronic details of the design are described in this section; the analog circuit is shown in Fig. 5 and the components used are listed in Table I. The limitations of the circuit and the components critical in the design are discussed so that the phasemeter can be constructed to meet various design specifications.

The phase accuracy of the circuit mainly depends upon the phase response of the components in the phase detector block. Therefore the analog bandwidth restrictions of the various components affect the phase accuracy of the circuit. The ZC's bandwidth depends upon the component used (U5), in this case, a high speed comparator. The bandwidth of the 90^0 phase shifter circuit[1] depends upon the operational amplifier used (U6), along with the values of R1-R8 and C1-C8. The analog bandwidth is also determined by the frequency response of the EOR (U1), in this case, the fastest TTL logic EOR. The particular components used in the circuit of Fig. 5 allowed a bandwidth from 10 kHz to 1 MHz with a $\pm 5.5^0$ phase error across the bandwidth.

The response of the circuit to a change in phase depends upon the rise time of the S/H and the RC time constants of LP1 and LP2. The product [Zon × C15] = 30 μs (Zon is the on-impedance of the analog switch U3) should be less than the pulse width of the cw pulse. For LP1, the product [R14 × C14] = 15.8 μs should be selected so that it corresponds to several periods of the input signal, and yet is less than the pulse width of the pulse. For LP2, the product [R17 × C17] = 0.1 s should be selected with knowledge of the pulse repetition rate and the number of pulses that should be averaged over. The sign (±) accuracy of the lead-lag circuit depends upon the speed of the DFF (U2) selected.

Although the circuit of Fig. 5 can be constructed using the information provided, proper operation is not ensured until the circuit has been calibrated. For proper calibration, two phase locked oscillators, a digital voltmeter (DVM), and an oscilloscope should be

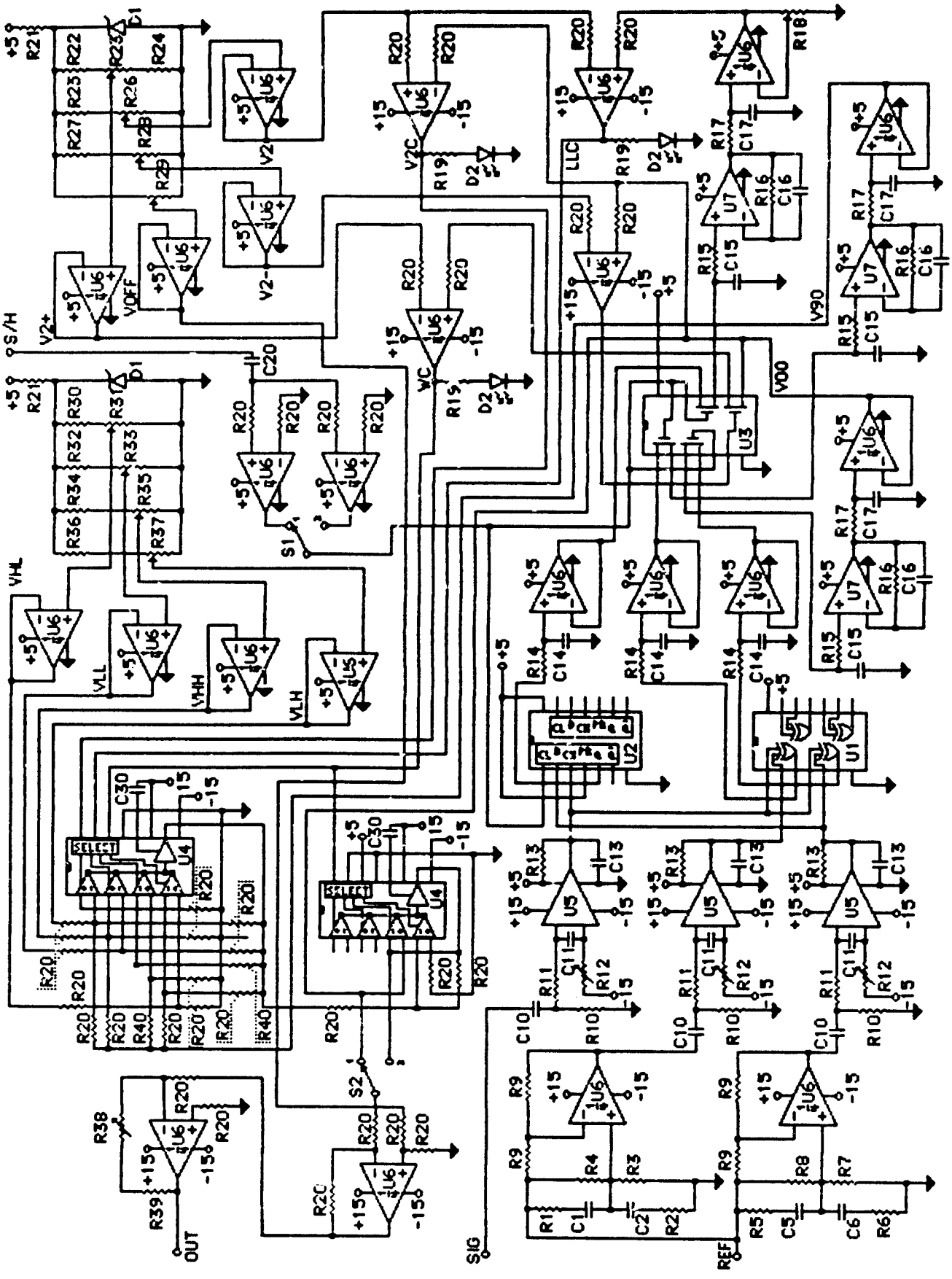

FIGURE 5
SCHEMATIC DIAGRAM OF SAMPLING PHASEMETER

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TABLE I

PARTS SUMMARY

U1	SN74S86N	TTL quad exclusive-OR
U2	SN74S74N	TTL dual data flip-flop
U3	CD4066A	Quad CMOS analog switch
U4	HA2425-5	Quad programmable operational amplifier
U5	LM361N	TTL output high speed comparator
U6	HA4741	Quad operational amplifier
U7	LF157A	JFET operational amplifier
D1	1N4732A	4.7 V zener
D2		LED
C1,C5		200 pF
C2,C6,C11,C14		1000 pF
C10		1 µF
C13		1 pF
C15		0.1 µF polycarbonate
C16		10 pF
C17-C20		0.1 µF
C30		15 pF
R1		430 Ω
R2,R10,R13		1 kΩ
R3		9.77 kΩ
R4		4.2 kΩ
R5		2.17 kΩ
R6		5.05 kΩ
R7		49.16 kΩ
R8		21.13 kΩ
R9,R20		10 kΩ
R11,R19		100 Ω
R12		1 MΩ potentiometer
R14		15.8 kΩ
R15		100 kΩ
R16		5 kΩ
R17		1 MΩ
R18		500 kΩ potentiometer
R21,R39		10Ω
R22+R23+R24,R25+R26, R27+R28,R29,R30+R31, R32+R33,R34+R35, R36+R37		1.25 kΩ
R38		10 kΩ potentiometer
R40		20 kΩ

used. The reference oscillator is input into the REF input, and the phase shifted oscillator is input into the SIG input. Both are operating in the pulsed cw mode with the pulse envelope input into the S/H of the circuit. The switch S1 is switched to 1 for a normal S/H signal (sample-high, hold-low) or to 2 for an inverted S/H. The first thing to check for is the proper operation of the ZCs. The components R10 and C10 are selected to block any dc bias that might be present in the signal. The resistor R12 is then adjusted so that a 50% duty cycle square wave is output from the ZC with a sinusoidal input. The oscillators are set for $\phi=45^{o}$, 90^{o}, and 135^{o} (by looking at the oscilloscope at the output of the ZCs) and the output at VOO is noted for each. Then R28, R26, and R24 are set for values of V2-, V2, and V2+ to match the respective values of VOO above. The oscillators are then set for a negative ϕ value and R18 is set so the output of the operational amplifier at this stage equals 2 x V2. This should complete the calibration of the input phase comparators and the logic comparators.

The final calibration is the calibration of the quadrature circuit. The oscillators are adjusted to the various switching points of the comparators and S2 is switched to 1 to note the VOUT level; S2 is then switched to 2 and the level of VOUT is adjusted to the previously noted level by means of VLH, VHL, VHH, or VLL, whichever is appropriate for the particular transition region as noted in Fig. 4, and by way of the three LEDs of WC, V2C, and LLC. When each of the transition regions has been adjusted so that the piecewise transfer curves match, the gain on VOUT is set with R38 to a convenient scale. R39 is also adjusted so that when $\phi=0^{o}$, VOUT=0. The only process left is to determine the relative phase shift introduced by the 90^{o} phase shifter. This is done by placing the reference signal into both REF and SIG inputs and reading the phase correction directly from the DVM and LLC LED.

When the circuit is initially constructed and calibrated on a prototype circuit board, it is tested with pulsed cw signals at a frequency of 80 kHz, a pulse width of 600 μs, and a repetition rate of 30/s. The resulting transfer functions (Figs. 6-8) are shown to compare

FIGURE 6
BLOCK I OUTPUT, NO NOISE

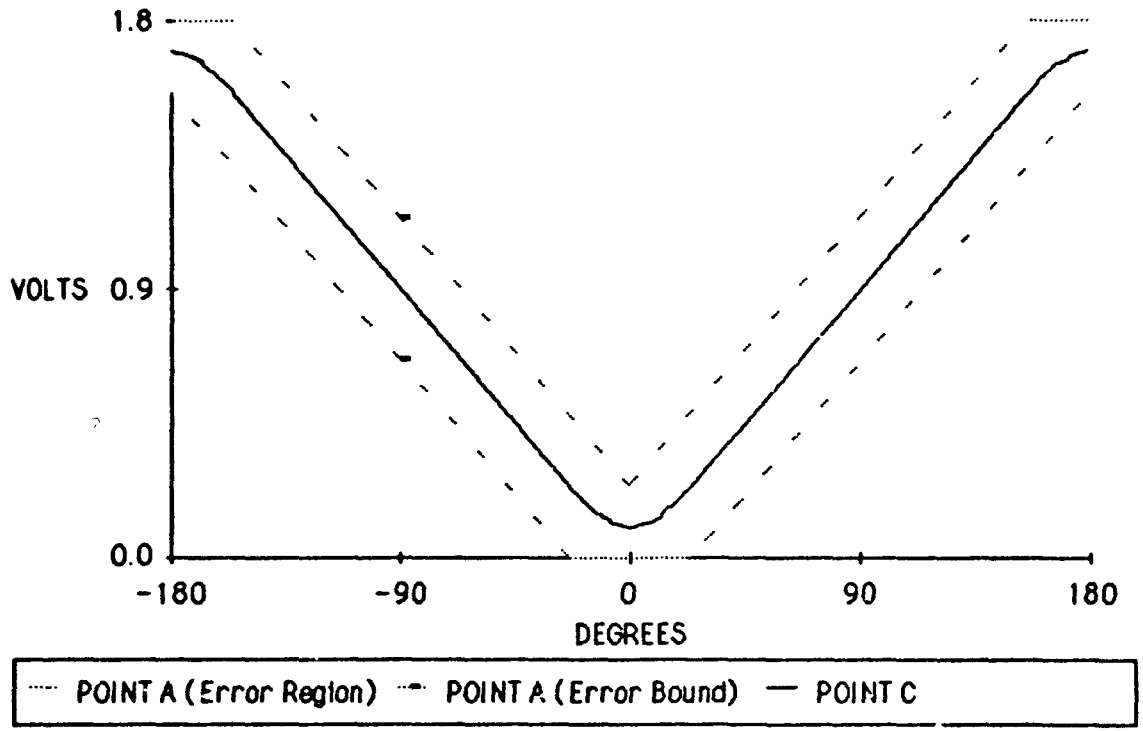

FIGURE 7
BLOCKS I AND II OUTPUT, WITH NOISE

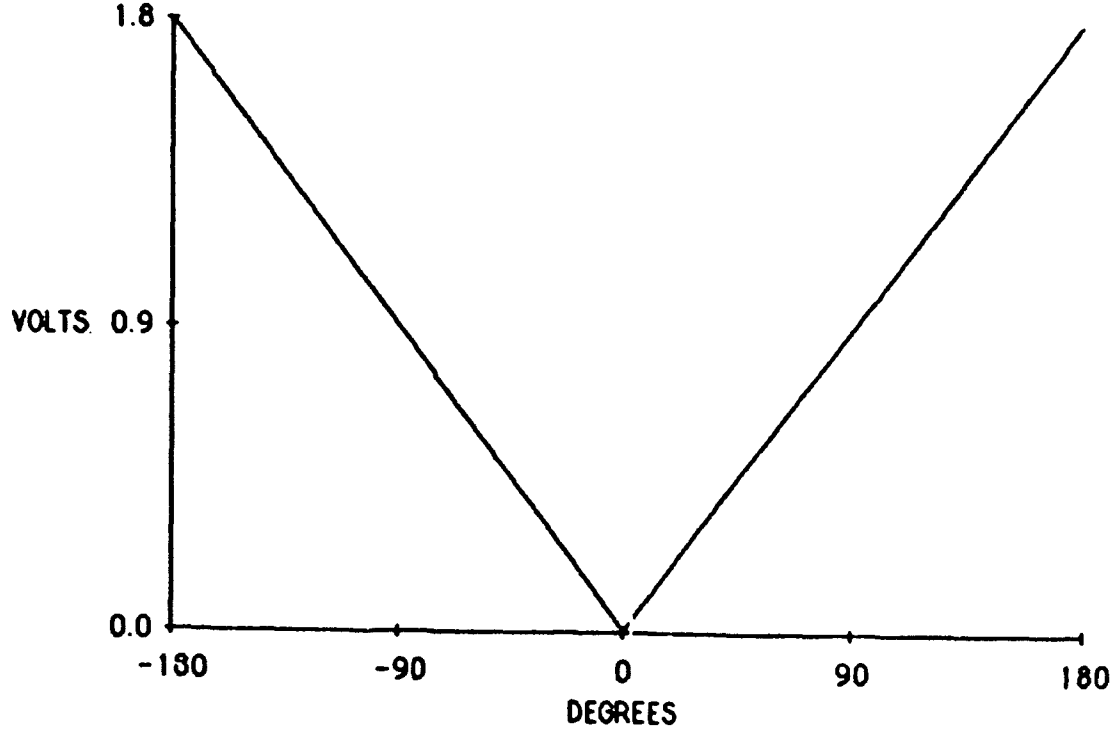

FIGURE 8
BLOCK III OUTPUT, WITH NOISE

with those in Fig. 2. This was done by linearly sweeping the phase of one of the oscillators and plotting VOUT versus the linear phase sweep. Figure 6 corresponds to a) of Fig. 2. When noise is added to produce a signal-to-noise ratio of 20 dB, Fig. 7 results, which corresponds to b) and c) of Fig. 2. The shaded region represents the observed deviation of the DVM output (rms). Figure 8 is the output of the circuit with the noise as above. Note that the nonlinearity of c) is no longer significant.

After being calibrated and tested, the pulse phasemeter was successfully used in acquiring pressure field data from rough surface scattering.[2] Subsequent processing of the pressure data yielded excellent results, thus adding to one's confidence in the circuit design.

V. CONCLUSIONS

The pulse phasemeter concept presented here was successfully carried out with a circuit design and implementation and was used in the actual collection of data. The testing of the circuit and the analysis of the data taken with the phasemeter have verified the practicality of the concept. The realtime analysis possible with the circuit avoids some of the pitfalls of analog recording, digitizing, and postprocessing of data used to achieve amplitude and phase information. The linear nature of the design allows immediate interpretation of the phase of a signal. Also, the restriction of pulsed cw signals poses no problem for the current design, since the designer can select a time period spanning a number of pulses over which an average phase can be obtained. And, finally, the matter of noise compensation is hurdled with a unique design implementation of quadrature logic.

However, the current design does have some limitations which could be overcome with a more careful design and the use of more sophisticated components. The operation of the current design is limited to one frequency, one pulse width, and one repetition rate. A recalibration process is necessary if any of these parameters are changed (due to the fixed components of LP1, LP2, and S/H and the phase error over the bandwidth of the 90^{o} shifter). Also, if operation outside of practical sonar frequency ranges is needed, components with greater analog bandwidths are required. Thus care must be taken in the selection of many of the components of the current design. But, most importantly, the major fault of the design is its reliance upon the linear nature of portions of both the normal and quadrature transfer curves. This linearity is tied directly to the noise, which means that the device can be used in a limited noise environment. However, the device is sufficient for use in the almost ideal experimental environment of the underwater tank.

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