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LSI/VLSI ION IMPLANTED PLANAR GaAs IC PROCESSING

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February 1, 1984 through July 31, 1984

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Program Manager

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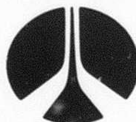

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The scope of this program is to complete and stabilize the development of a planar fabrication process for high speed digital integrated circuits on 3-in. GaAs wafers. In the six-month period covered by this report progress was made in the areas of materials characterization, uniformity evaluation, and gate array design.

Annealing experiments were performed on as-grown GaAs wafers to evaluate methods of damage gettering to reduce the metal concentration in active layers and to improve the reproducibility of the implant process. The results were somewhat inconsistent because of unusually high manganese levels in the ingot.

To help determine those factors which influence threshold voltage variation, a simple C-V technique was established. One feature illustrated by the C-V data is that most reported nonuniformities in the LEC material which has been reported is due to systematic rather than random variations in threshold voltages. The statistical variations in threshold voltage are generally much smaller being on the order of 20 mV. Standard deviations due to the larger systematic variations have been typically 50-70 mV.

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The AR8 mask set is in the second phase of the on-going gate array development program. The masking plates for fabricating the generic underlayers have been received in-house, and Mayo has completed the customization layers. The UCSB circuits have been placed on the mask. The customization layers are ready to be sent to the mask shop.

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1.0 INTRODUCTION

At the present time programs to develop GaAs ICs for such DoD applications as electronic warfare, secure communications and ballistic missile defense are being supported by several DoD agencies. These programs involve demonstration of circuits as complex as a 16-bit GaAs microprocessor. In addition, possible use of GaAs ICs in such DARPA sponsored programs as the Advanced Onboard Signal Processor (AOSP) is of strong interest because of the considerable radiation hardness of GaAs ICs. For these potential applications of GaAs ICs to progress beyond the feasibility demonstration stage, further process development activities directed towards processing improvements and a significant increase in the yield of complex GaAs ICs must be carried out. The main objective of this program, therefore, is to develop and stabilize a planar ion implanted fabrication process for high speed digital ICs on 3-inch diameter GaAs wafers. The demonstration vehicle for this process development will be gate arrays up to the 1K gate level complexity. Additional tasks include an effort on mask programmable logic arrays related to ERADCOM needs, and a task to fabricate wafers for contractors to the DARPA Information Processing Technology Office.

This report covers the third semester of the 23-month program. The areas of discussion include materials characterization results related to wafer annealing, uniformity studies for 3-inch wafers, a review of the gate array mask set (AR8), and finally, a status report on the mask programmable array design (ERADCOM).

2.0 MATERIALS CHARACTERIZATION

During the last reporting period at least two mechanisms were shown to influence axial (wafer-to-wafer) uniformity of FET threshold voltage along undoped semi-insulating LEC ingots. On the one hand, carbon* segregation during crystal growth leads to an increase of the carbon concentration toward the last portion of the crystal to solidify (tail). Since carbon is an acceptor, the corresponding FET threshold voltage profile increases toward the tail. On the other hand, a second mechanism has the opposite effect of carbon and actually counterbalances the carbon-controlled profile. This mechanism was uncovered in studies of ultra-low carbon GaAs.

One possible explanation for the second mechanism is outdiffusion of transition metal acceptors from the bulk of the substrate material and accumulation in the implanted layers. Annealing experiments were conducted to evaluate methods of damage gettering to reduce the metal concentration in active layers and to improve the reproducibility of the implant process.

Ultra-low carbon material ($< 8 \times 10^{14}$ cm^{-3}) was used in the first set of annealing studies. One-inch squares were obtained from as-sliced wafers from the seed end and tail of the crystal. The samples were heated for 4 h at 850°C. After cooling, the samples were lapped and polished. C-V depletion voltage measurements were made by our standard technique on as-grown and annealed samples. Twenty data points were taken on each sample.

A comparison of C-V depletion voltages at the seed end and tail of the as-grown and annealed samples, given in Table 1, shows that the 200 mV depletion voltage difference along the crystal was virtually eliminated after annealing and that exceptionally high uniformity was achieved. These results could be explained because transition metals such as Fe were gettered to the saw damage induced by the annular I.D. saw and were removed by subsequent polishing steps.

*Carbon is a predominant background acceptor in LEC GaAs.

Table 1

Effect of Annealing on Threshold Voltage Uniformity LED Ingot*

	Depletion Voltage, Volts	
	Seed End	Tail End
As-Grown	1.47	1.27
Annealed	1.41	1.41

*Low-Carbon Ingot

As a result of this experiment, another annealing series was conducted using samples from three different crystals containing low (R88), medium (R99), and high (R84) carbon levels, respectively. The carbon concentration and the depletion voltages before and after annealing are given in Table 2.

Table 2

Effect of Annealing on Threshold Voltage Reproducibility

Crystal No.	Carbon Concentration cm^{-3}	Ave. Depletion Voltage (Annealed), V	Ave. Depletion Voltage (As-Grown), V	DV (As-Grown)-(Annealed), V
88-4	U.D.	1.35	1.43	0.08
88-53	U.D.	1.20	1.23	0.03
ΔDV (Tail Seed)		-0.15	-0.20	
99-1	4.4×10^{15}	1.18	1.09	-0.09
99-61	U.D.	0.97	1.07	0.10
ΔDV (Tail Seed)		-0.21	-1.02	
84-5	3.4×10^{16}	0.55	0.69	0.14
84-45	1.2×10^{16}	1.01	1.04	0.03
ΔDV (Tail Seed)		0.46	0.35	

Based on the first annealing experiment, two results were anticipated. First, the seed-to-tail uniformity of the low carbon crystal was expected to improve. However, the observed 50 mV improvement (200 mV difference as grown vs 150 mV after annealing) is small compared to the change observed in the first experiment. Second, the threshold voltage was expected to increase at the tail of all crystals after annealing. In fact, all three values decreased.

The apparent irreproducibility of the annealing experiments does not necessarily mean that transition metals do not play a role in controlling the threshold voltage level of implanted layers. In fact, SIMS chemical analysis of the material annealed in the first experiment (Table 1) indicated an unusually high concentration of manganese. Therefore, the effort of annealing could be accounted for by manganese gettering. However, this same mechanism is not consistent with the ineffectiveness of annealing of crystal R88, notwithstanding possible variations of the annealing process itself. The central conclusion to be drawn from this work is that a more quantitative approach to evaluating transition metals is needed during routine processing. The application of DLTS would seem to be a preferred method. However, a quantitative measure of hole traps would require p-type implants, which would be difficult to implement.

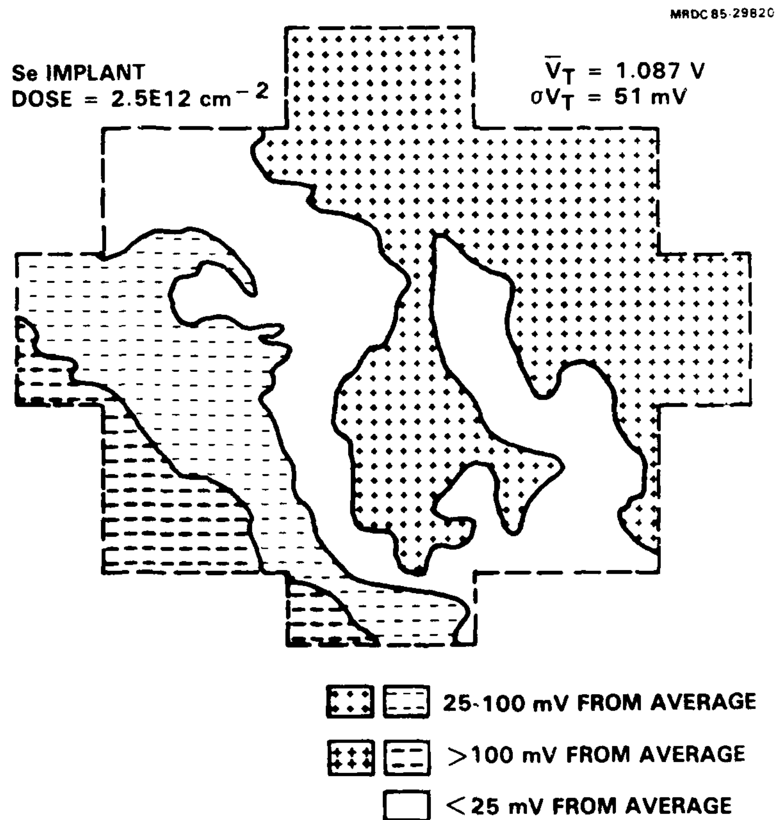
3.0 UNIFORMITY OF THRESHOLD VOLTAGE ACROSS 3-INCH GaAs WAFERS

To obtain high yield consistency for GaAs circuits, maintaining good threshold voltage uniformity across GaAs wafers and minimizing absolute threshold variations on a wafer-to-wafer basis will be necessary. Typically, such variations should be less than 100 mV peak to reach across 3-in. wafer for SDFL and BFL logic circuits. For enhancement mode devices deviations from the average ultimately should be less than 50 mV peak to peak.

Threshold variations may arise from a number of different sources. For a through-the-cap implant process the thickness of the cap, singular variations of the implant scan, thickness of the native oxide between cap and substrate, and uniformity errors associated with the implant process can significantly affect threshold voltage uniformity. Material properties such as residual acceptor content and dislocation density may also play a significant role.

To help determine those factors which influence threshold voltage variations in the standard GaAs IC fabrication process, a simple C-V process was established to help isolate factors which contribute to nonuniformities in threshold uniformity. The process consists of capping a 3-inch wafer with Si_3N_4, implanting the wafer, annealing the wafer, defining a high density array of pseudo-ohmic Schottky diodes across the 3-inch wafer, and measuring the depletion voltage using an automatic wafer stepping system across the entire wafer. The advantages of this simplified process are that: 1) only one mask level is required. which simplifies fabrication and accelerates the turnaround time; 2) most of the critical fabrication steps in the normal IC fabrication process are included so that the simplified process closely replicates the actual fabrication; 3) complicating factors such as short channel effects or piezoelectric effects which can shift FET thresholds are not present, so they can be effectively separated from activation and implant related nonuniformities; and 4) interpretation of the C-V results can be obtained rapidly in a relatively short period of time for a large density array of points.

Three wafers were processed to establish potential sources of nonuniformity across wafers. The first two wafers received implants of Si and Se at doses of 2.5E12 with energies 130 KeV and 320 KeV, respectively, through a 750 A Si_3N_4 cap. The third wafer was implanted at a 45° angle with respect to axis of the ion beam with Se at a dose of 2.5E12 cm^{-2} at 320 KeV. Figures 3.1 and 3.2 show 3-dimensional plots across the wafer for the depletion voltage in each of these cases. Figure 3.3 shows individual cross sections across the Se implanted wafer.



Figs. 3.1 Implant uniformity, Se implant.

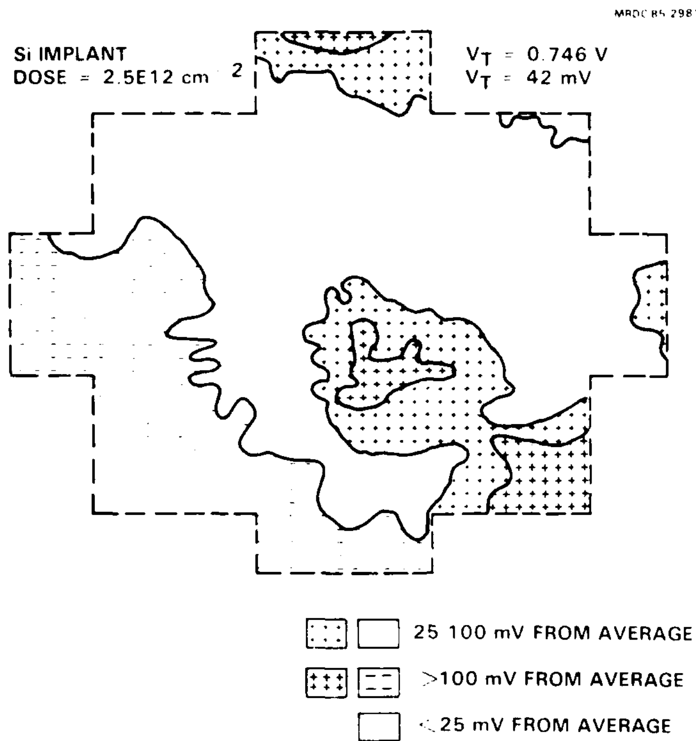


Fig. 3.2 Implant uniformity, Se implant.

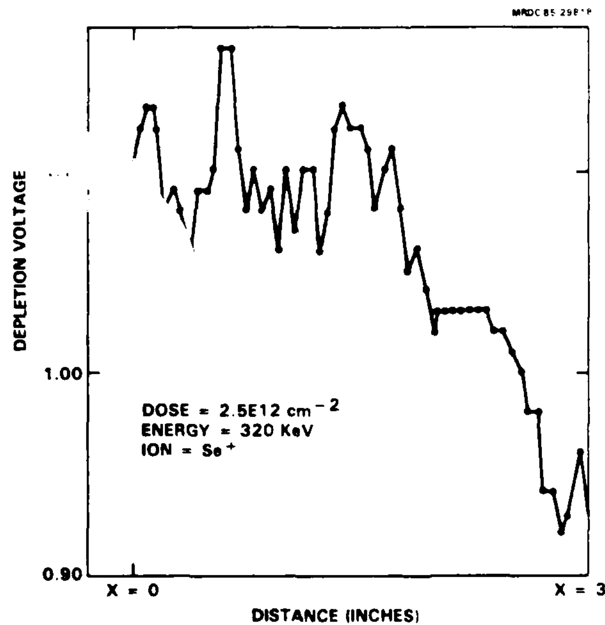


Fig. 3.3 Implant uniformity, Se implant.

The first two wafers were run to compare the overall uniformity between Si and Se implants and to test whether residual dislocations have any influence on the uniformity across wafer. Si might be expected to behave differently than Se since it is an amphoteric dopant. Although the Si does show lower activation across wafer than the Se, the uniformity of each across wafer is comparable. In both cases, however, the uniformity is dominated by a systematic gradient across the wafer which coincides with the angular orientation of the flat relative to the ion beam. This orientation is chosen to be 7° in order to reduce channeling effects. To test whether the implant uniformity was affecting threshold uniformity, the third wafer was implanted with a 45° rotation about the axis of the wafer. A discontinuity was found in the threshold voltage (vertically oriented in the center of the profile for the first two wafers) rotated by 45°, suggesting that the nonuniformities were associated with implanted nonuniformities rather than material properties.

One important feature illustrated by the C-V data is that most reported LEC material nonuniformities are due to systematic rather than random variations in threshold voltage. The statistical variations in threshold voltage are generally much smaller, being on the order of 20 mV. Standard deviations due to the larger systematic variations typically have been 50-70 mV. The magnitude of the variations across wafer shown in Figs. 3.1 and 3.2 are similar to those associated with dislocations by researchers at other laboratories. However, any obvious effects of the dislocations on threshold voltage uniformity have not been observed. Dislocation densities exhibit a distinctive W-shaped pattern in LEC material which would be apparent in Figs. 3.1, 3.2 and 3.3. Similar arguments can be made regarding the uniformity of residual impurities in the substrate. The distribution of impurities also typically shows a W-shaped pattern which would be apparent.

Nonuniformities which have a strong dependence on the device area can be ruled out. The deviations of depletion voltage of the C-V dots is comparable to the deviation in threshold voltage of FETs fabricated on similar wafers even though the difference in area is roughly 2000.

4.0 AR8 MASK SET REVIEW

The AR8 mask set is the second phase of the ongoing GaAs gate array development. It is an array of 1K equivalent uncommitted BFL gates in the medium speed/power range of the technology. It is an expansion of the AR7 400 gate array and uses the same basic cell.

The objective of this iteration is to demonstrate the capability of a large array of uncommitted logic that can be customized for rapid turnaround of designs. The computerized auto placer and router developed by Mayo Clinic was used to customize two arrays. Test cells were included to monitor the process and to characterize the array and the performance of the circuit. In addition some operational amplifier circuits developed at University of California, Santa Barbara (Prof. Steve Long's group), have been included on the mask set.

The mask reticle is divided into quadrants of which a 1K array fits. Three arrays fill three-fourths of the area. Two of the arrays were customized by the computer program developed at Mayo. The two circuits are an eight-bit parallel multiplier and a portion of the protocol circuit of the AOSP bus. The third array is a test array to characterize library macro cells in a real environment. The major macros used in the multiplier and AOSP circuits are isolated and connected to the I/O. Four shift register test circuits were designed for evaluation. Also a signal cross-coupling test circuit was constructed. All of these circuits are built on the actual 1K gate array.

The fourth quadrant is a pattern of test circuits. Individual patterns of the basic cell, I/O cell, FETs, and resistors were built for evaluation of the components. A ring oscillator was lifted from AR7 for comparison of speed. The 5 × 5 multiplier was also lifted from AR7 for comparison. A GaAs Opamp was designed at UCSB. Several versions and test circuits were placed. The Opamp versions differ in size of the compensation capacitance. A layout of the AR8 reticle is shown in Fig. 4.1.

Fig. 4.1 AR8 mask set layout.

The AR8 phase will have circuits to continue the characterization and understanding of the GaAs gate array concept. Information pertaining to all levels will be attainable, from the basic components to the aspects of the auto router. From this iteration further development will expand the macro library, will extend the router to the I/O hookup, and will define the interface to the router and from the router to the test computer. Array performance itself will be evaluated for improvement and design projection purposes.

The masking plates to fabricate the generic underlayers have been received in-house. Mayo has completed the customization layers, and they have been merged with our data base. The UCSB circuits have been placed on the mask. The customization layers are ready to be sent to the mask shop.

The array is built with the Rockwell Planar depletion mode process. The 732 basic cells have a 1.4 gate equivalent each. There are 84 I/O cells and 96 pads. The basic cells are buffered FET Logic and are arranged in pairs. The customization is accomplished in the two metal layers and the via layer. 12 routing channels are between each cell pair in the horizontal and vertical directions.

The auto router is hierarchical in nature to save time by using macro cells for subcircuits. The subcircuits are then interconnected to build the overall circuit. The program has the intelligence to use the high current output driver when an output has a large fanout. Ultimately the program will extract the parasitic parameters affecting the circuit performance.

5.0 MASK PROGRAMMABLE FUNCTIONS AND LOGIC ARRAYS

This report covers the activities performed during the period Feb. 1, 1984, through July 1, 1984.

Three wafer tote numbers JE1-1X, JE1-2X and JE1-3X (of 4 wafers each) were processed during this reporting period.

Wafer probing of the Buffered FET Logic (BFC) test devices on wafers from lot JE1-1X was initiated, and the results are included in Section 5.2 of this report. The test results indicated circuit parameters were within design specifications. Also a few small scale integrated (SSI) circuits were tested as outlined in Section 5.3.

Magnetic tapes containing geometric data of the circuits designed for this program have been shipped to ERADCOM.

5.1 Wafer Processing

Processing of wafer lot JE1-1X (4 wafers) was started on January 23, 1984 and was completed on April 10, 1984, with delivery of 3 wafers (one was broken during processing).

Initial test data from these wafers indicated threshold voltages of -1 V ± 400 mV on two wafers and -1 V ± 100 mV on wafer JE1-14.

A photoresist adhesion problem was encountered during processing of wafer lot JE1-2X. Processing of this lot was completed; however, we have not tested these devices to determine the extent of damage or operability of the circuits.

Wafer lot JE1-3X (3rd wafer lot) was completed and delivered in July. No testing of these wafers has been performed to date.

5.2 Buffered FET Logic Test Data

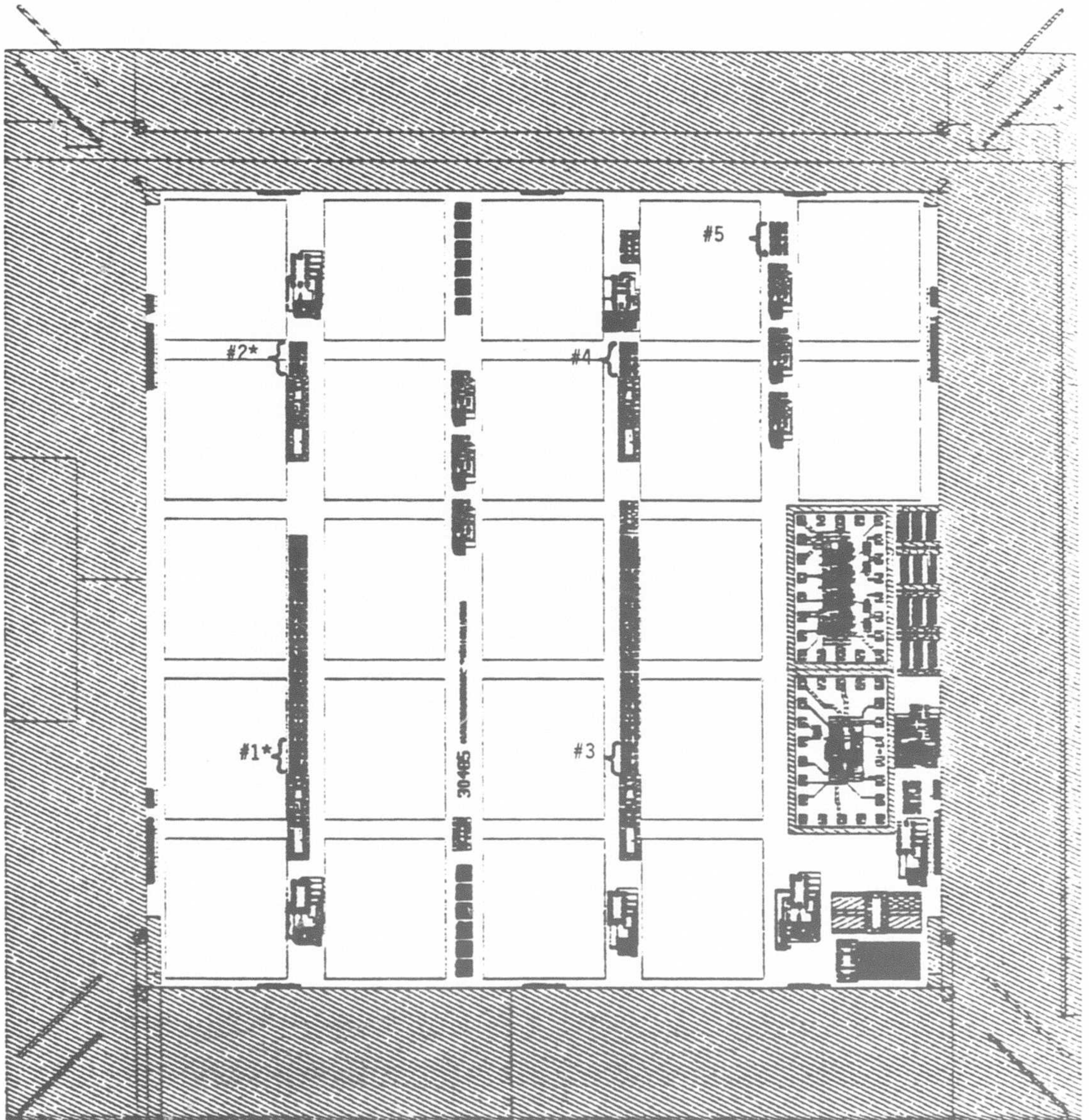
The Buffered FET Logic test devices (BFLTD2) on wafer JE1-11 were completely tested to determine basic characteristics of the transistors, diodes and basic circuit elements. The data were collected, from two of five test sites (Fig. 5.1) within each of the 44 die locations, and the average value was plotted. The tests performed are listed in Table 3. Data of particular interest are the tracking characteristics of the matched pair (transistor and vertical saturated resistor) as indicated in test number 3 and the transfer curves from test number 7.

5.3 Integrated Circuit Testing

Testing of the SSI circuits on wafer JE1-14 (proton implanted) was initiated and include the following:

Prescaler ÷ 6/7
÷ 10/11
÷ 20/21
÷ 40/41
PRN Sequence Generator
Bi-directional Output Drivers

Since the testing was not completed during this reporting period, full details of the test results will be included in the final report.



*Selected Test Sites

Fig. 5.1 Buffered FET Logic (BFL) test sites.

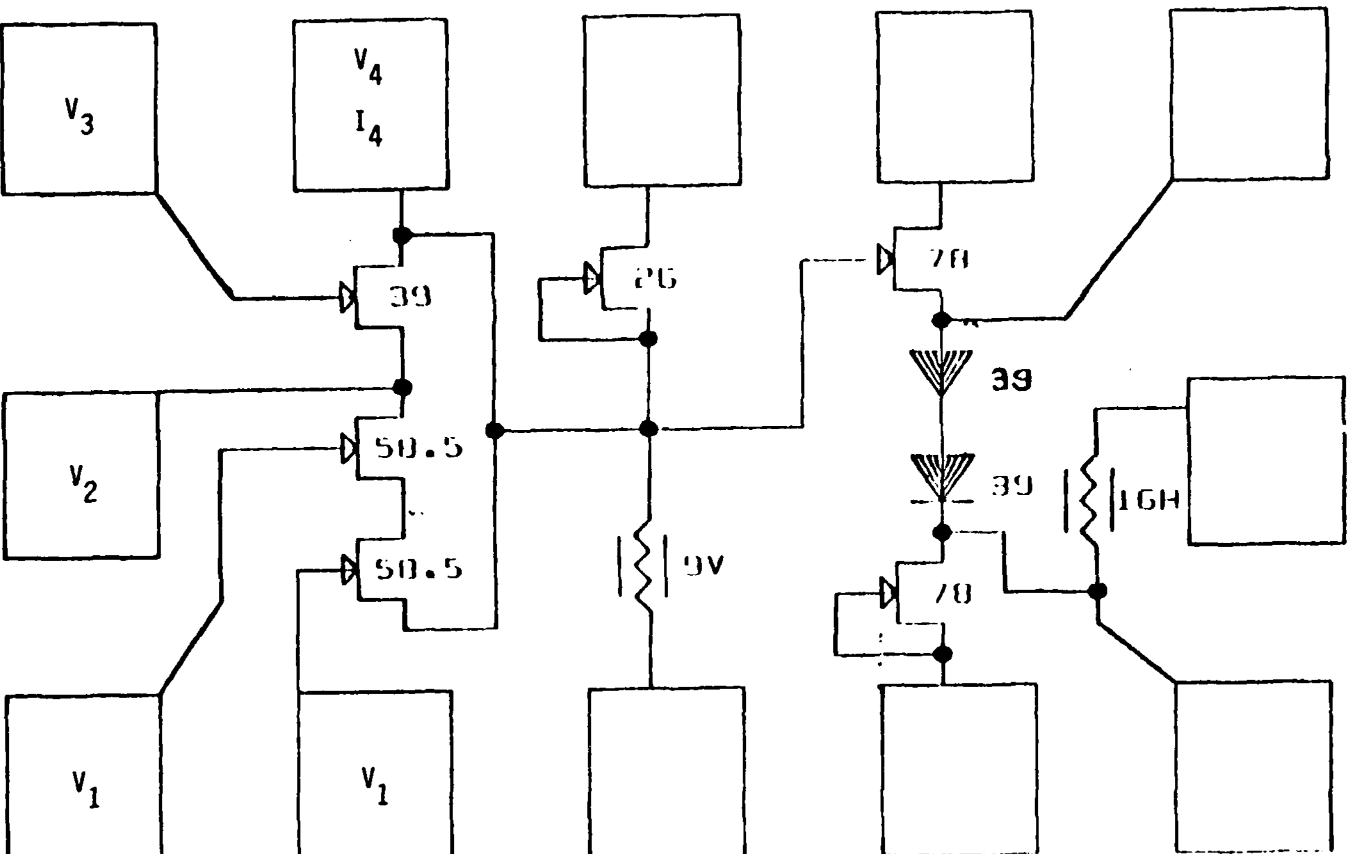
Table 3

BFLTD2 Parametric Test

Test No.	Parameters Measured
1	I/V characteristics of a 39μ wide MESFET.
2	I/V characteristics of (2) 58.5μ wide pull-up series connected MESFETS.
3	I/V characteristics of a 26μ wide pull-up MESFET. I/V characteristics of a 9μ wide vertical saturated resistor.
4	I/V characteristics of a 78μ wide pull-down MESFET. I/V characteristics of a 16μ wide horizontal saturated resistor.
5	I/V characteristics of a 78μ wide source follower MESFET.
6	I/V characteristics of (2) 39μ × 2μ series diodes.
7	Transfer curve characteristics of a MESFET inverter.
8	Transfer curve characteristics of a MESFET/saturated resistor inverter.
9	Transfer curve characteristics of a MESFET/diode source follower.

APPENDIX

Parametric Test Data



V_1 = -2.0 volts
V_2 = GROUND
V_3 = -1.2 TO +0.8 VOLT (SWEEP)
V_4 = 0.0 TO 4.0 VOLTS (1 VOLT STEPS)

FIGURE 1. TEST NUMBER 1 FOR MEASUREMENT OF I/V CHARACTERISTICS OF 39μ WIDE MESFET

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#1
TEST # 1 - P4 VOLTAGE VS I4 CURRENT (UA)
DIE AVERAGE FROM 38 DIE

DATE: 11-APR-84
TIME: 14:50:02
WAFER PROBE TEST

11.00MA

(1.000MA/DIV)

-1.000MA

-1.200 V

(400.0MV/DIV)

800.0MV

V_4

4 VOLT

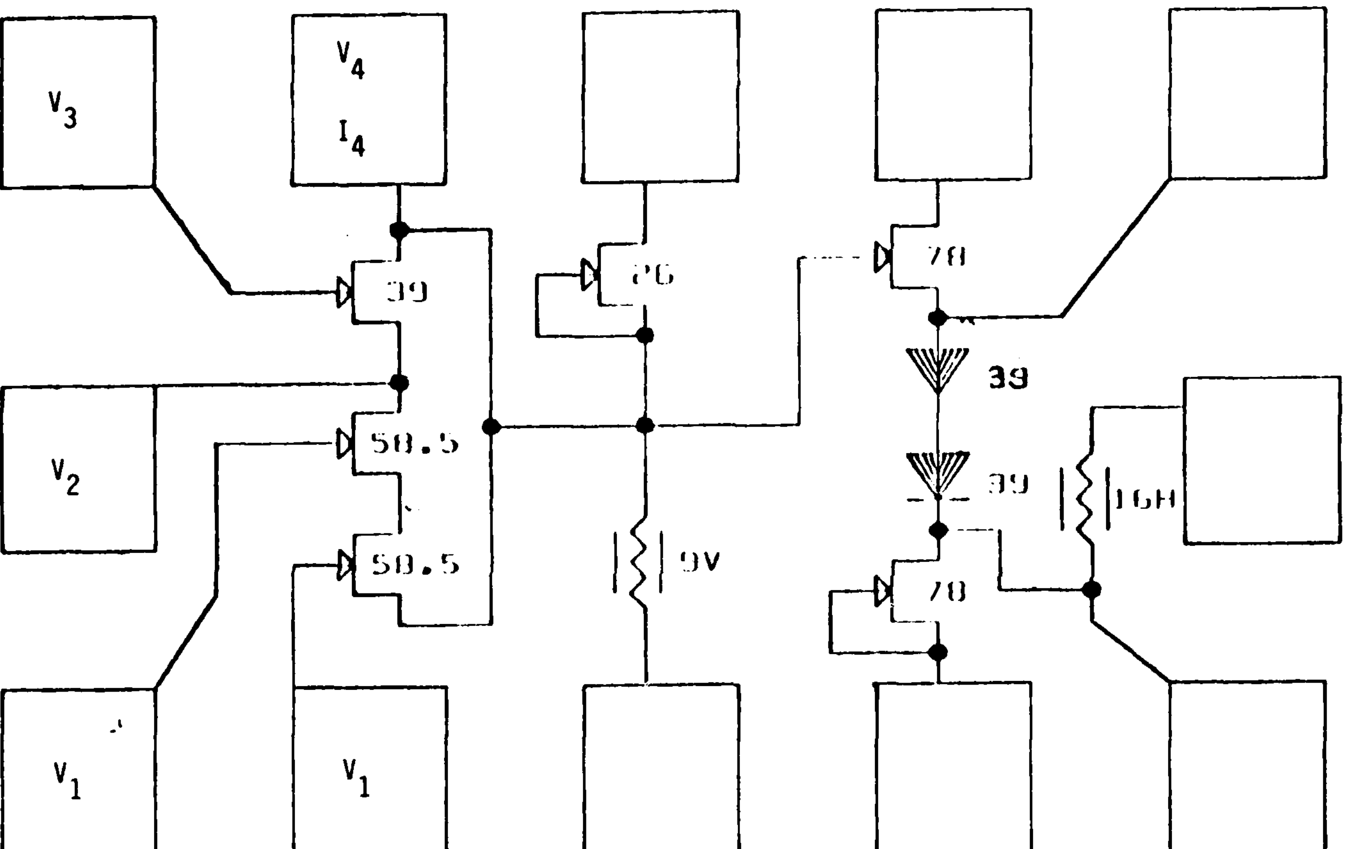
3 VOLT

2 VOLT

1 VOLT

FIGURE 1a. TEST NUMBER 1 RESULTS

FIGURE 1b. TEST NUMBER 1 RESULTS



V_1 = +0.8V TO -1.2V (SWEEP)
V_2 = GROUND
V_3 = -2.0 VOLTS
V_4 = 0.0 TO 4.0 VOLTS (1 VOLT STEPS)

FIGURE 2. TEST NUMBER 2 FOR MEASUREMENT OF I/V CHARACTERISTICS OF 58.5μ WIDE DUAL MESFET

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#1
TEST # 2 - P4 VOLTAGE VS I4 CURRENT (UA)
DIE AVERAGE FROM 37 DIE

DATE: 11-APR-84
TIME: 14:50:02
WAFER PROBE TEST

11.00MA
(1.000MA/DIV)
-1.000MA

800.0MV
(-400.0MV/DIV)
-1.200 V

V_4 = 4 VOLT
V_4 = 3 VOLT
V_4 = 2 VOLT
V_4 = 1 VOLT

FIGURE 2a. TEST NUMBER 2 RESULTS

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#2
TEST # 2 - P4 VOLTAGE VS I4 CURRENT (UA)
DIE AVERAGE FROM 28 DIE

DATE: 18-APR-84
TIME: 15:25:29
WAFER PROBE TEST

11.00MA

V_4 = 4 VOLT

(1.000MA /DIV)

V_4 = 3 VOLT

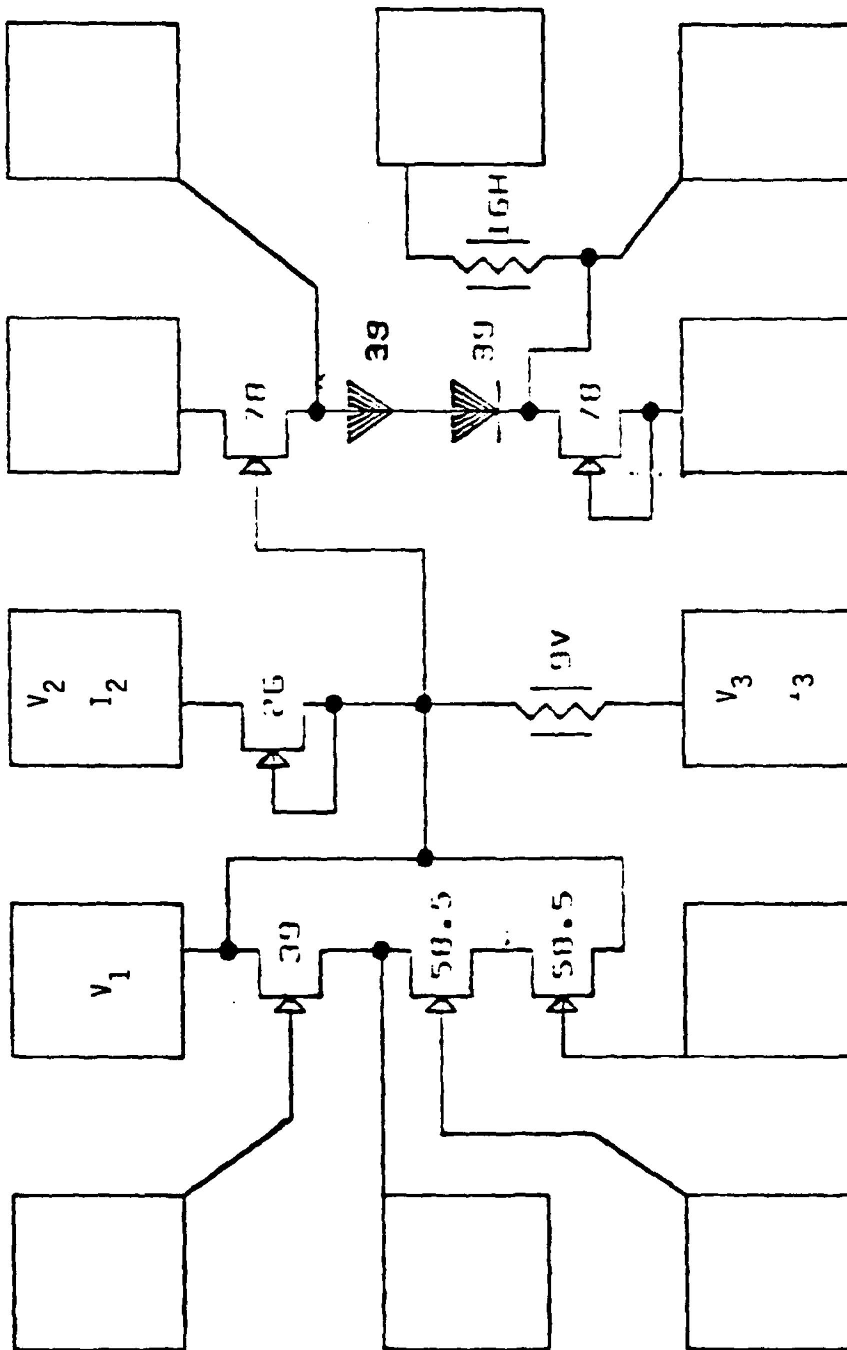
V_4 = 2 VOLT

V_4 = 1 VOLT

-1.000MA

800.5MV (-400.0MV/DIV) -1.200 V

FIGURE 2b. TEST NUMBER 2 RESULTS



V_1 = GROUND
V_2 = 0.0 TO 4.0 VOLT (SWEEP)
V_3 = 0.0 TO 4.0 VOLT (SWEEP)

FIGURE 3. TEST NUMBER 3 FOR MEASUREMENT OF I/V CHARACTERISTICS OF 26μ WIDE PULL-UP MESFET AND 9μ WIDE VERTICAL SATURATED RESISTOR

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#1
DATE: 11-APR-84
TIME: 14:50:02
WAFER PROBE TEST
TEST # 3 - P5,P11 VOLTAGE VS P5,P11 CURRENT (UA)
DIE AVERAGE FROM 38 DIE

FIGURE 3a. TEST NUMBER 3 RESULTS

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 1102
TEST # 3 - P5,P11 VOLTAGE VS P5,P11 CURRENT (UA)
DIE AVERAGE FROM 22 DIE

DATE: 18-APR-84
TIME: 15:25:29
WAFER PROBE TEST

11.00MA

(1.000MA/DIV)

-1.000MA

0.000 V

(800.0MV/DIV)

4.000 V

TRANSISTOR

SATURATED RESISTOR

FIGURE 3b. TEST NUMBER 3 RESULTS

V_1 = 0.0 TO 4.0 VOLT (SWEEP)

V_2 = GROUND

V_3 = 0.0 TO 4.0 VOLT (SWEEP)

FIGURE 4. TEST NUMBER 4 FOR MEASUREMENT OF I/V CHARACTERISTICS OF 78μ WIDE PULL-DOWN MESFET AND 16μ WIDE NORIZONTAL SATURATED RESISTOR

FIGURE 4a. TEST NUMBER 4 RESULTS

FIGURE 4b. TEST NUMBER 4 RESULTS

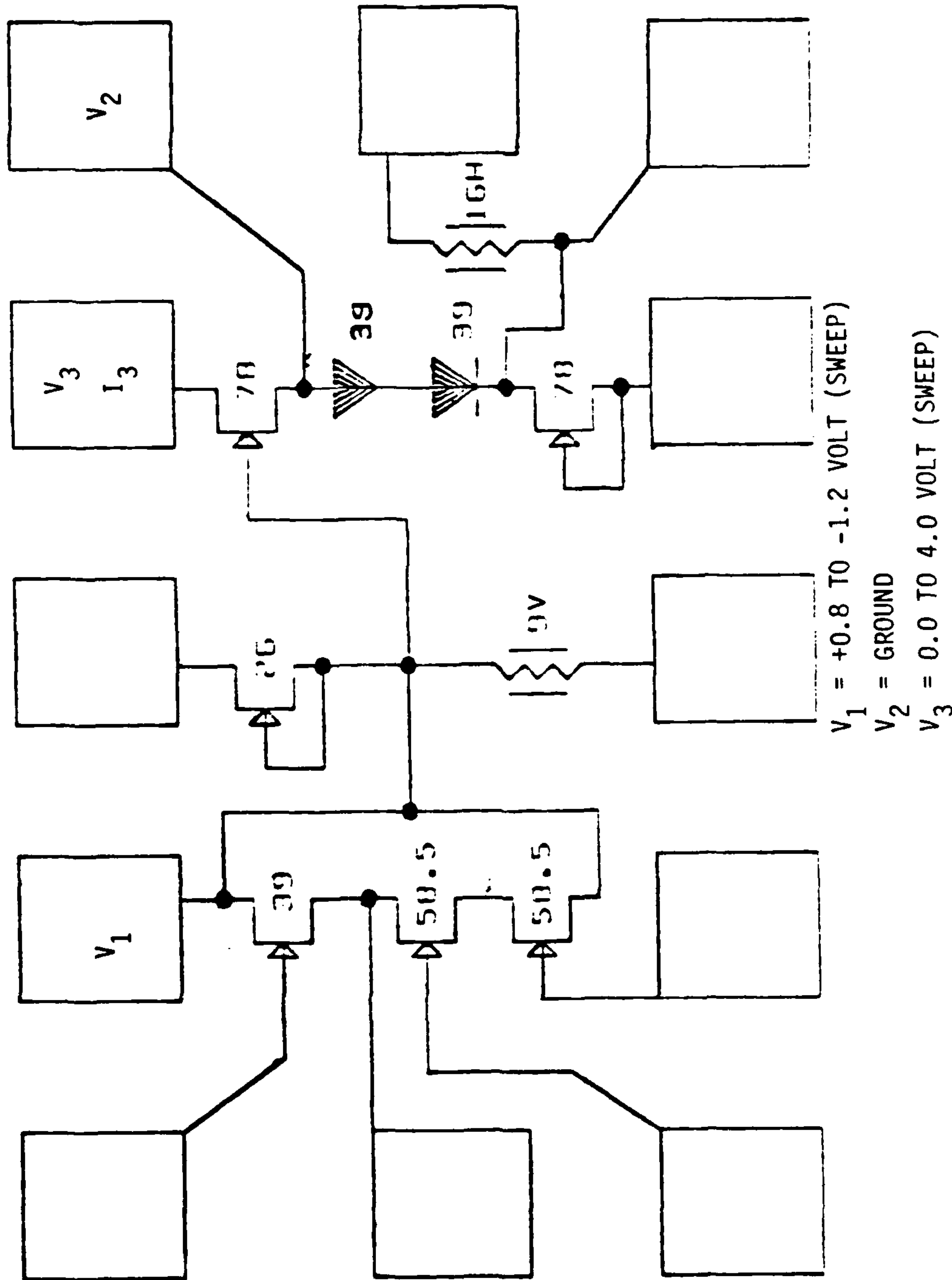


FIGURE 5. TEST NUMBER 5 FOR MEASUREMENT OF I/V CHARACTERISTICS OF 78μ WIDE SOURCE FOLLOWER FET

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#1
TEST # 5 - P6 VOLTAGE VS I6 CURRENT (UA)
DIE AVERAGE FROM 41 DIE

DATE: 11-APR-84
TIME: 14:50:02
WAFER PROBE TEST

15.00MA

V_3 = 4 VOLT

V_3 = 3 VOLT

V_3 = 2 VOLT

(1.000MA /DIV)

V_3 = 1 VOLT

-1.000MA

000.0MV (-400.0MV/DIV) -1.200 V

FIGURE 5a. TEST NUMBER 5 RESULTS

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#2
TEST # 5 - P6 VOLTAGE VS I6 CURRENT (UA)
DIE AVERAGE FROM 38 DIE

DATE: 18-APR-84
TIME: 15:25:29
WAFER PROBE TEST

15.00MA

V_3 = 4 VOLT

V_3 = 3 VOLT

(1.000MA /DIV)

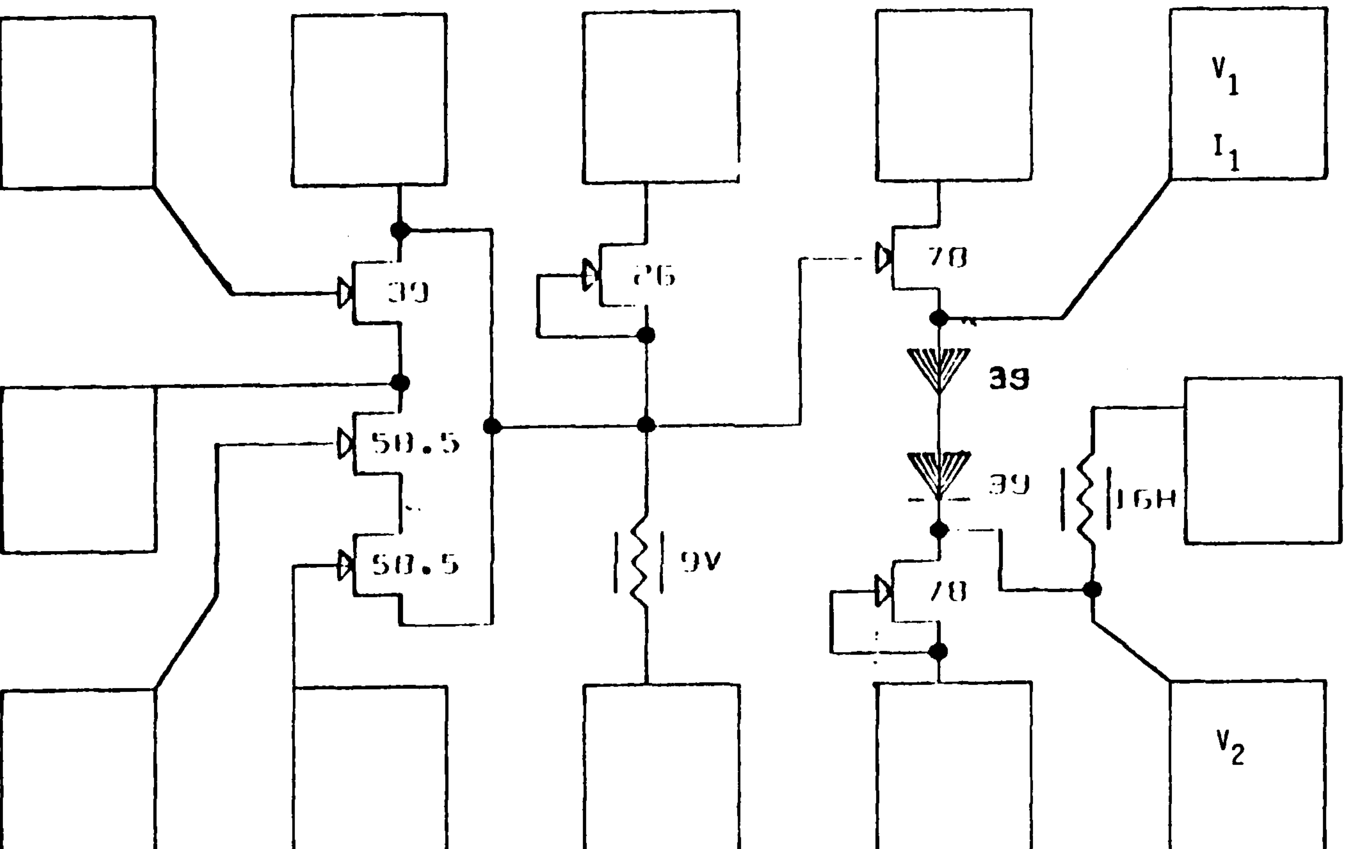
V_3 = 2 VOLT

V_3 = 1 VOLT

-1.000MA

800.0MV (-400.0MV/DIV) -1.200 V

FIGURE 5b. TEST NUMBER 5 RESULTS



V_1 = +2.0 TO -18.0V (SWEEP)
V_2 = GROUND

FIGURE 6. TEST NUMBER 6 FOR MEASUREMENT OF I/V CHARACTERISTICS OF THE TWO 39μ X 2μ DIODES

FIGURE 6a. TEST NUMBER 6 RESULTS

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#2
TEST # 6 - P7 DIODES I7(MA) VS V7(VOLTS)
DIE AVERAGE FROM 44 DIE

DATE: 18-APR-84
TIME: 15:25:29
WAFER PROBE TEST

-400.0UA
(-400.0UA /DIV)
2.000MA

3.000 V
(-2.000 V/DIV)
-21.00 V

FIGURE 6b. TEST NUMBER 6 RESULTS

V_1 = -1.1 VOLT
V_2 = GROUND
V_3 = -1.4 TO +0.6V (SWEEP

V_4 = OPEN
V_5 = +2.5 VOLT
V_6 = +2.5 VOLT
V_7 = OPEN

V_8 = OPEN
V_9 = OUTPUT
V_{10} = -2.0 VOLT
V_{11} = OPEN

FIGURE 7. TEST NUMBER 7 FOR MEASUREMENT OF TRANSFER CURVE CHARACTERISTICS OF INVERTER USING ALL MESFETs

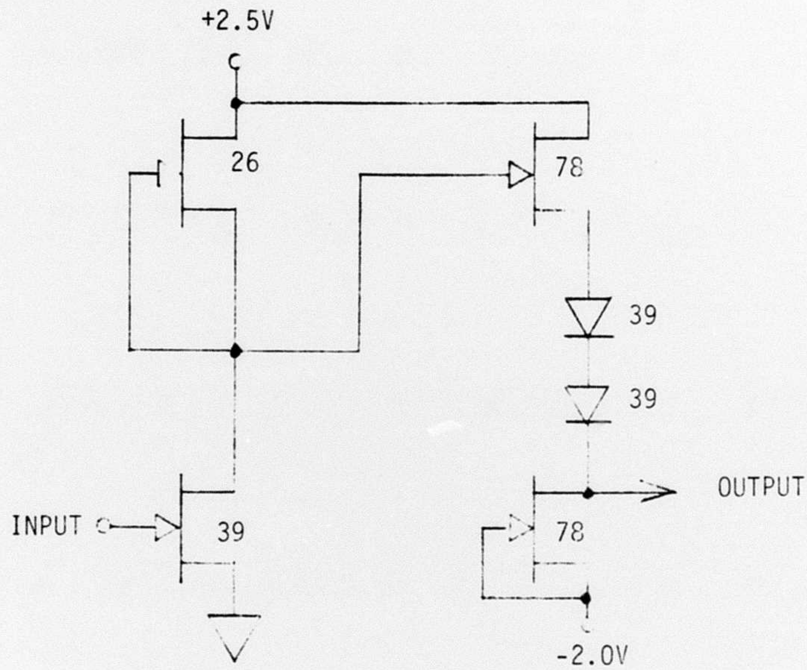


FIGURE 7a. INVERTER CIRCUIT USED IN TEST NUMBER 7

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#1

DATE: 11-APR-84
TIME: 14:50:02
WAFER PROBE TEST

TEST # 7 - P3 INPUT VOLTAGE VS P9 OUTPUT VOLTAGE - FET RESISTORS
DIE AVERAGE FROM 41 DIE

600.0MV

(400.0MV /DIV)

-1.400 V

-1.400 V (400.0MV/DIV) 600.0MV

FIGURE 7b. Test Number 7 Results

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#2

DATE: 18-APR-84
TIME: 15:25:29
WAFER PROBE TEST

TEST # 7 - P3 INPUT VOLTAGE VS P9 OUTPUT VOLTAGE - FET RESISTORS
DIE AVERAGE FROM 38 DIE

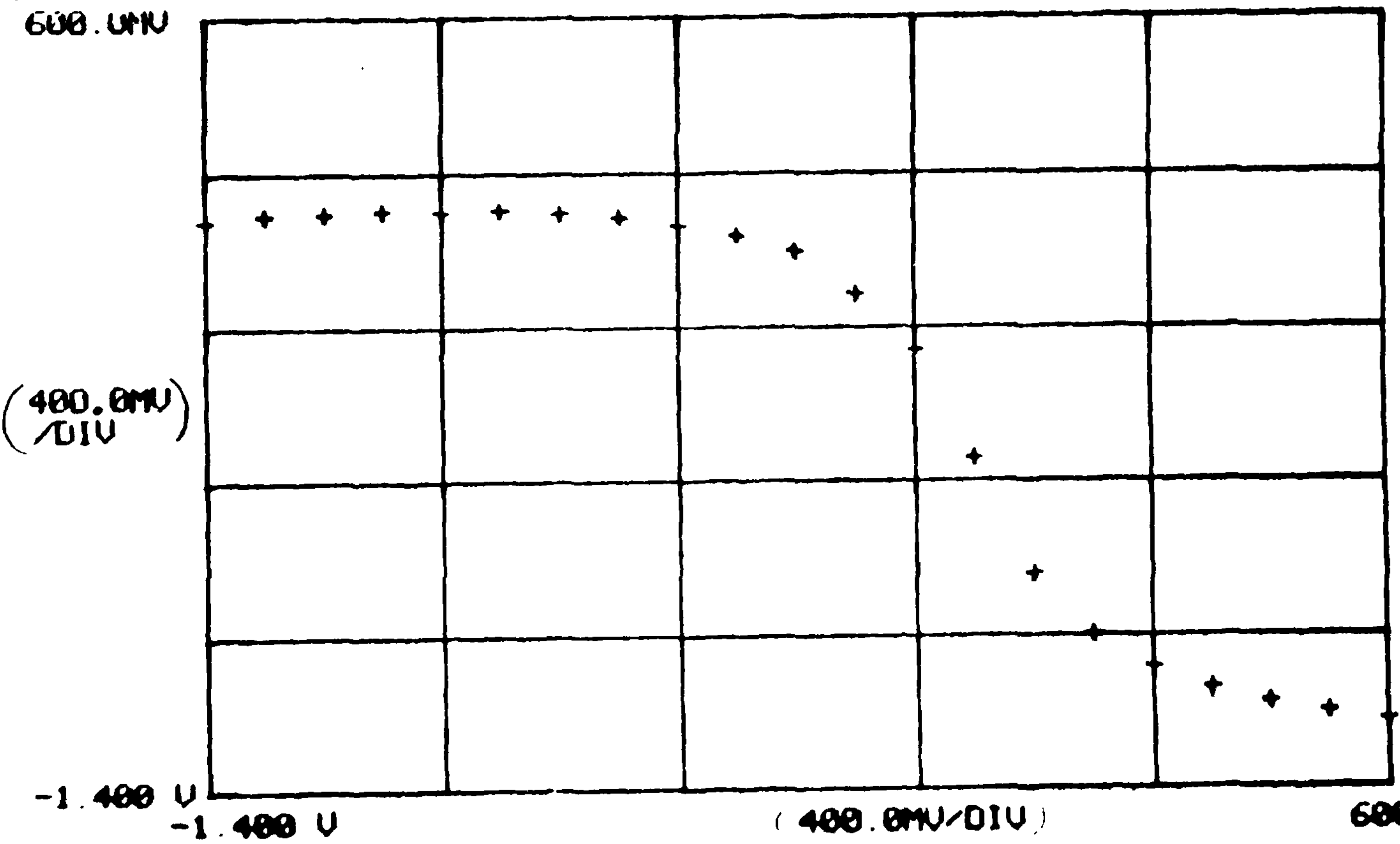


FIGURE 7c. Test Number 7 Results

V_1 = -1.1V
V_2 = GROUND
V_3 = -1.4V TO +0.6V (SWEEP)
V_4 = OPEN
V_5 = OPEN

V_6 = +2.5 VOLT
V_7 = OPEN
V_8 = -2.0 VOLT
V_9 = OUTPUT

V_{10} = OPEN
V_{11} = +2.5 VOLT

FIGURE 8. TEST NUMBER 8 FOR MEASUREMENT OF TRANSFER CURVE CHARACTERISTICS OF INVERTER USING MESFETs AND SATURATED RESISTOR

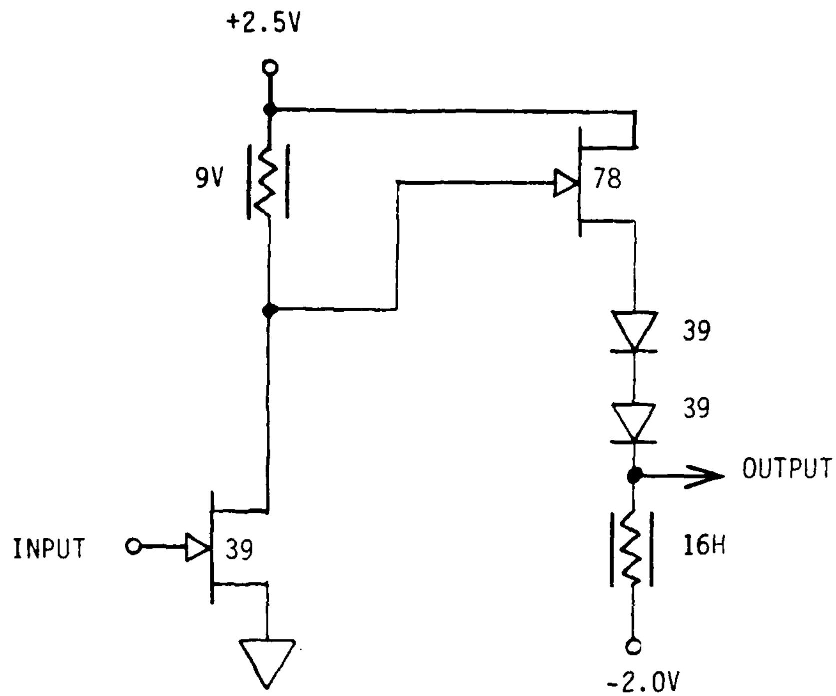


FIGURE 8a. INVERTER CIRCUIT USED IN TEST NUMBER 8

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#1

DATE: 11-APR-84
TIME: 14:50:02
WAFER PROBE TEST

TEST # 8 - P3 INPUT VOLTAGE VS P9 OUTPUT VOLTAGE - SAT RESISTORS
DIE AVERAGE FROM 40 DIE

600.0MV

(400.0MV/DIV)

-1.400 V

-1.400 V (400.0MV/DIV) 600.0MV

FIGURE 8b. TEST NUMBER 8 RESULTS

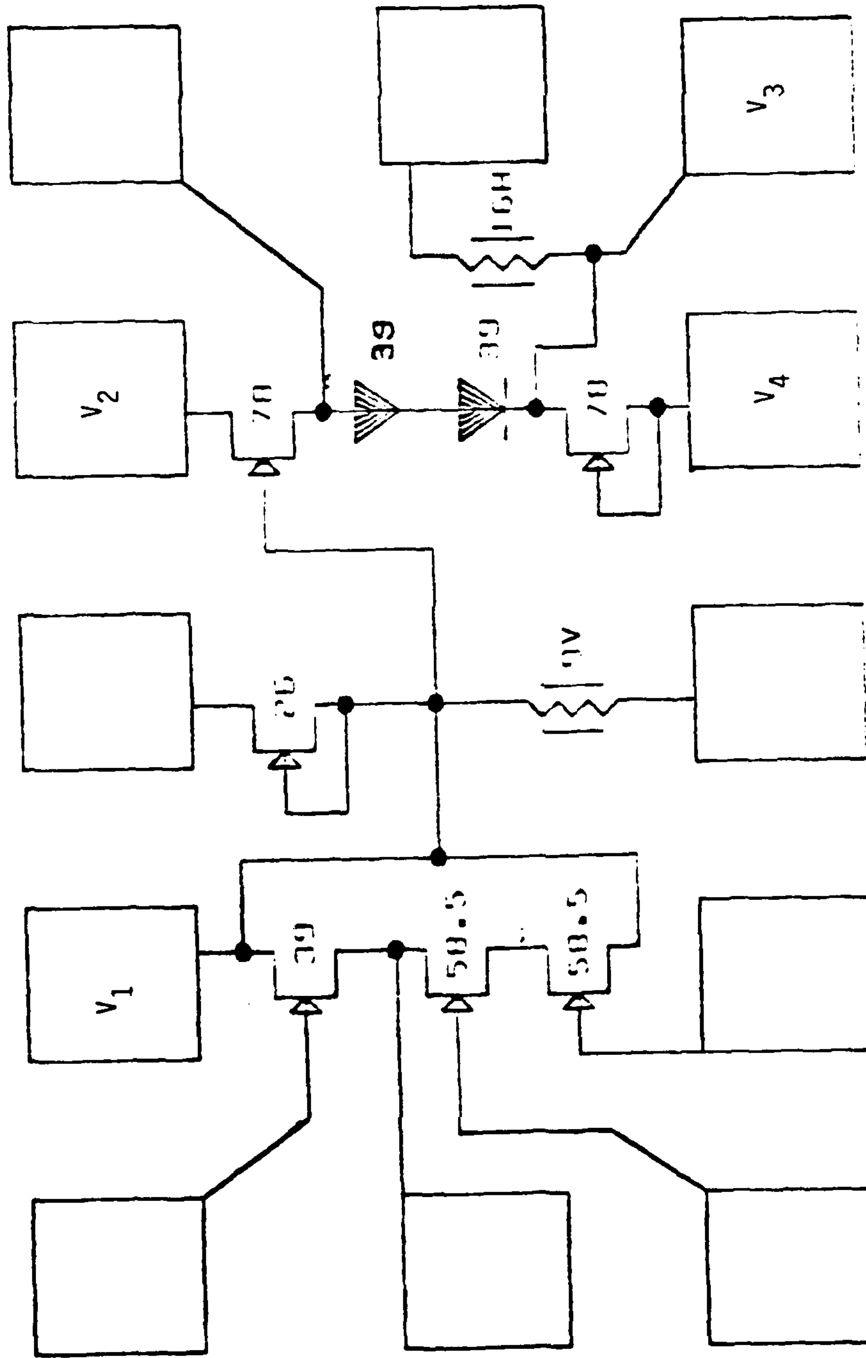
DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 1102

DATE: 18-APR-84
TIME: 15:25:29
WAFER PROBE TEST

TEST # 8 - P3 INPUT VOLTAGE VS P9 OUTPUT VOLTAGE - SAT RESISTORS
DIE AVERAGE FROM 33 DIE

600.0MV
(400.0MV/DIV)
-1.400 V
-1.400 V
(400.0MV/DIV)
600.0MV

FIGURE 8c. TEST NUMBER 8 RESULTS



V_1 = 0 TO 2.5V (SWEEP)
V_2 = +2.5V
V_3 = Vout
V_4 = -2.0V; -1.0V

FIGURE 9. TEST NUMBER 9 FOR MEASUREMENT OF TRANSFER CURVE CHARACTERISTICS OF SOURCE FOLLOWER

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#1
TEST # 9 - P4 VOLTAGE VS P9 VOLTAGE
DIE AVERAGE FROM 44 DIE
P10 = -2V + ,P10 = -1V

DATE: 11-APR-84
TIME: 14:50:02
WAFER PROBE TEST

1.000 V

(500.0MV /DIV)

V_4 = -1V

V_4 = -2V

-2.000 V

0.000 V

(500.0MV/DIV)

2.500 V

FIGURE 9a. TEST NUMBER 9 RESULTS

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#2
TEST # 9 - P4 VOLTAGE VS P9 VOLTAGE
DIE AVERAGE FROM 44 DIE
P10 = -2V + .P10 = -1V

DATE: 18-APR-84
TIME: 15:25:29
WAFER PROBE TEST

1.000 V
(500.0mV /DIV)
-2.000 V

0.000 V
(500.0mV/DIV)
2.500 V

V_4 = -1V

V_4 = -2V

FIGURE 9b. TEST NUMBER 9 RESULTS