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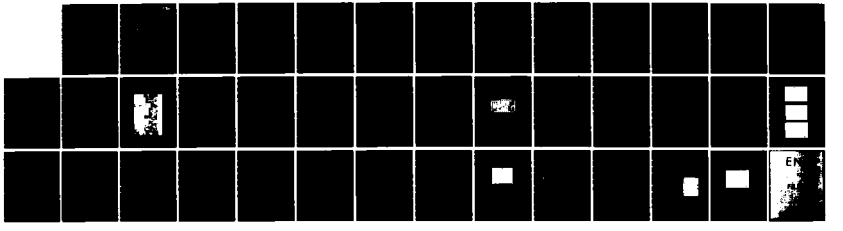

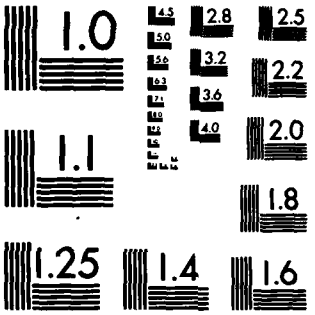

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Final Report

1.4 Gb/s Optical Repeater Development

March 1984

Prepared for
Naval Research Laboratory
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We report on the design and implementation of several optical repeaters at 1.4 Gb/s with both short (0.85 μm) and long (1.3 μm) operating wavelength for use in single mode fiber transmission system.

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I

Summary

Fully regenerative repeaters operating at 1.4 Gbits/s have been developed at both short (0.85 μm) and long (1.3 μm) wavelengths. The fabrication technology involves thin film hybrid circuit for the low noise preamplifier, SAW filter for timing extraction and discrete components for the rest of the circuitry. Apart from the hybrid preamplifiers and SAW filters which are fabricated at TRW, all other discrete components are obtained via commercial vendors.

The long wavelength repeater has been tested and is operating at 1.4 Gbits/s. The short wavelength repeater does not quite work at the above rate due to inadequate preamplifier bandwidth and laser resonance. However, this problem is not fundamental, and can be resolved by improved hybrid layout and design.

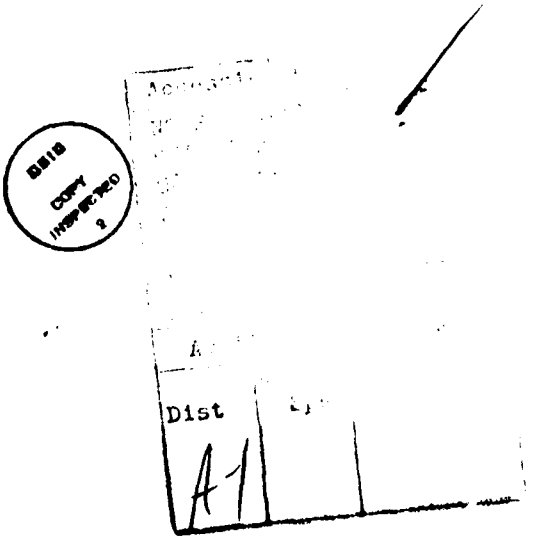


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Cont'd)

1. Repeater Development Overview

1.1 Objectives

The program goal is the design, development, and delivery of four fiber optic digital repeaters operable at a 1400 Mbps data rate. Each repeater uses single mode optical fiber as the transmission medium. Two repeaters each are deliverable at 830 and 1300 nm. The repeaters are intended for laboratory evaluation; there is no requirement for a significant optical dynamic range or operation over extended temperature ranges. Laser and detector biasing are not under closed loop control, making tradeoff evaluations easier. Full digital testing was limited by a lack of proper equipment capable of 1400 Mbps bit error rate testing. Such equipment is now part of our 1984 capital plan, but it was not available during this program. We developed a 1400 Mbps word generator to exercise the equipment developed under this program. This returned qualitative data on repeater performance although precise bit error rate and accumulated jitter data were not measurable.

1.2 Critical Technologies

The 1400 Mbps data rate requires a system bandwidth of 1 to 1000 MHz. TRW EORC had developed several linear systems at both 830 nm and 1300 nm which show excellent performance over this frequency range. In our view the critical repeater development issues lay in the electronics and signal processing areas which are essentially nonlinear in nature.

The high data rate is at the traditional limit in speed for bipolar emitter coupled logic. In order to achieve that rate fully custom or semi-custom monolithic integration is usually necessary, with good performance but very high development costs and fabrication delays. We selected instead an approach which allowed rapid, low cost prototyping with discrete semiconductors and microwave printed circuit techniques. This approach preserved the low development cost and rapid fabrication

of surface mounted printed circuit modules. It also provided a clear migration path to an enhanced hybrid microcircuit or monolithic IC implementation.

All circuits were extensively modeled for performance before fabrication using either SPICE (for nonlinear applications) or COMPACT (for linear stages). SPICE was especially useful in circuit tuning. It was unable to predict a recurring instability at 2.3 GHz found in the digital circuits, but this instability was isolated and removed by a combination of empirical passivation and rebiasing experiments.

The 1.4 GHz surface acoustic wave retiming filter was another critical development, as it must operate at the upper frequency limits of the technology. The devices were designed and manufactured at the TRW MicroElectronics Center and are the highest frequency filters so far fabricated by that group. We elected to use quartz substrates instead of the original lithium niobate design to minimize the effects of temperature on device phase delay.

1.3 Design Options

There are several design options in repeater development involving trades among speed, sensitivity, power and consumption, and reliability. The choice of long or short wavelength transmission affects these tradeoffs. Wherever possible we chose a repeater design which would function well for either 830 or 1300 nm transmission. The major difference lies in the detector choices. Figure 1.1 shows the basic repeater block diagram.

A silicon avalanche photodiode can provide very low noise gain over a broad bandwidth with low power consumption. These devices are useful only below 900 nm, and were used in the short wavelength detector/preamplifier module. Long wavelength avalanche gain is much noisier, due to material physics, so that there is no advantage over the use of a simple PIN diode as the detector. The 40 dB of gain available

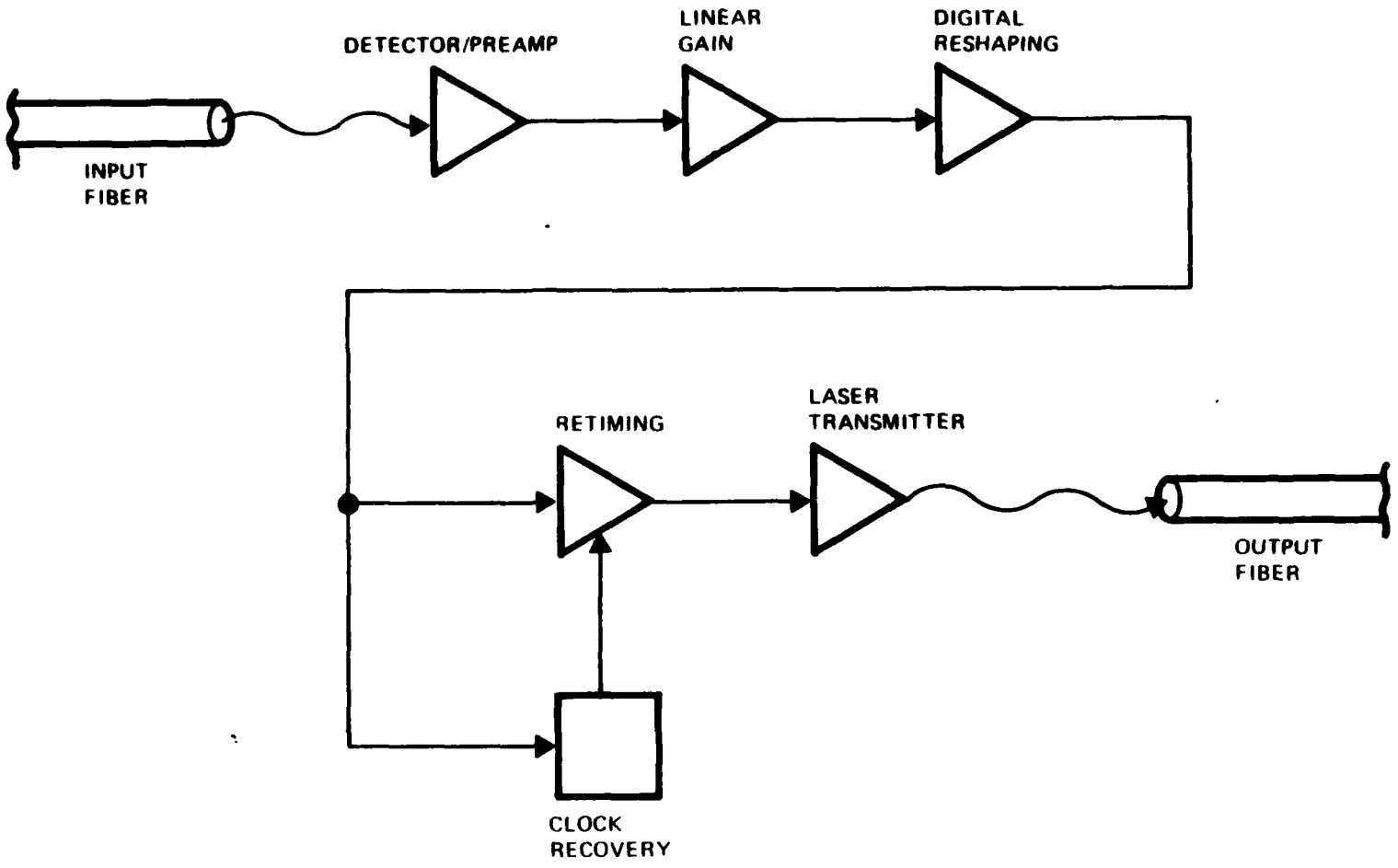


Figure 1.1. Repeater Block Diagram

in a silicon APD must be replaced with noisier electronic gain, which increases the power consumption while reducing receiver sensitivity. Therefore the 1300 nm repeater is more complicated and power hungry, as well as less sensitive than the 830 nm repeater.

The limited signal to noise ratio in the long wavelength repeater demands a high quality clock recovery scheme to prevent further degradation to the sensitivity. One approach is to simply amplify and reshape all transitions, without enforcing the rule that all transitions occur only on bit boundaries. This can be done with a digital buffer which takes the received waveform and minimizes the transition times. Such a scheme is very sensitive to noise and jitter accumulation.

An improved approach develops an internal bit rate clock from the input data stream. The data stream is sampled and retimed using this clock to provide well-shaped output signalling with maximum noise immunity. Extra circuitry is needed to develop the clock signal and sample the data stream. A certain amount of data is lost after each transmission interruption since the clock reference signal must be averaged over 100 or more bit periods. We chose to use this fully retimed scheme for both short and long wavelength repeaters to minimize differences between the two repeaters.

All repeater electronics use AC coupling in the signal path consistent with the NRZ coding spectrum requirements. This selection simplifies circuit design greatly, since complex level shifting and bias control loops are unnecessary. This is permissible under the assumption tha each repeater receives the signal of a single transmitter, and that the transmitter laser is always biased at a constant level. The repeater would not operate efficiently in a multitransmitter star network, for instance, since the fluctuations in laser bias levels would upset the receiver biasing and threshold determination.

The sensitivity of this repeater technology to transmitter interruption can be summarized as: (1) any discontinuity in transmitter

laser modulation will result in the loss of the first several hundred bits from the renewed data stream, and (2) a discontinuity in transmitter laser bias will cause a probable loss of several thousand bits from the renewed data stream.

2. Electro Optic Components

The electro optic transmitter and receiver modules include the laser, the detector, and closely coupled support circuitry. The lasers include RF input matching and basic biasing, but no feedback stabilization of average optical power or junction temperature. The detectors are integrated with preamplifiers in thin film hybrid circuitry. The close coupling between detectors and preamplifiers is necessary to transform the detector source capacitance to a broadband 50 ohm interface with minimum added noise. Like the transmitters, the receivers are fully functional for development purposes though they lack production features like AGC biasing and status telemetry.

2.1 Laser Transmitters

The short wavelength (830 nm) transmitter uses the MACOM (Laser Diode Lab) LDT-480 device, a multimode GaAlAs laser with a single mode fiber pigtail. Figure 2.1 shows the schematic for this simple module. Coupled optical power is 200 μw average into the single mode fiber. Bias current is 68 mA with a full scale modulation current requirement of 6 mApp for a 400 μW optical modulation. The built in reference photodiode provides a photocurrent sense output which is proportional to the output power. This is useful for optical feedback control purposes.

The two devices delivered by MACOM do not have reference diodes installed, although the documents imply that the diodes are standard. In laboratory tests we biased the lasers for a flat response in the 0-1000 MHz power bandwidth of the NRZ signalling method. Biasing is rather touchy with these devices, and the resonance at 1.3 GHz is a problem in any production system. The MACOM devices are especially

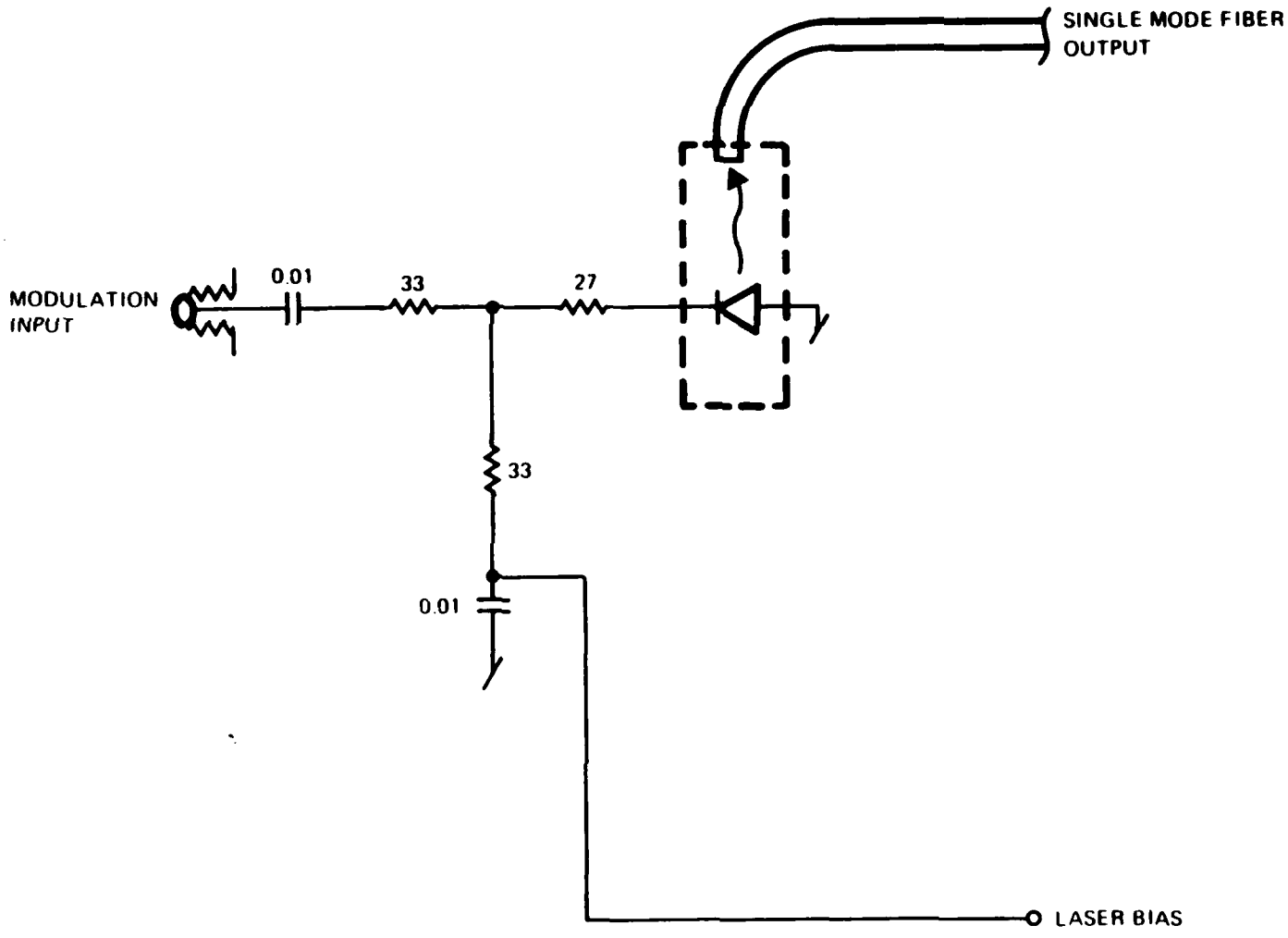


Figure 2.1. Laser Transmitter Module

sensitive to optical reflection, much more so than the Hitachi 1300 nm devices. The reflection from the single mode fiber pigtail is sufficient to cause a large instability in the laser linear response. We used single mode to multimode coupling with index matching gel to minimize the effects of reflection in bench testing. The laser power consumption is 100 mW at 25C, making thermoelectric cooling unnecessary in a laboratory environment. The laser uses a modified Hitachi package for good RF coupling and heat removal. The multimode nature of the laser will impose a significant dispersion limit on link distance. So far this vendor is the only apparent supplier of single mode pigtailed 830 nm lasers.

The long wavelength (1300 nm) transmitter uses the Hitachi HLP-5500S laser with the same input matching and bias configuration as the LDT-480. Bias currents are lower, 30 to 40 mA, and rated average power is 150 µW for a 300 µW peak level. The HLP-5500S does not include a photodiode optical power monitor, although an optical port is available to use an external reference detector. The device also lases in multiple longitudinal modes, but this is of less importance due to the low fiber dispersion at 1300 nm. Several vendors can supply similar parts, as those are expected to become the preferred components in terrestrial commercial telecommunications.

During operation each laser is biased at a nominal operating current for 200 µW average optical output. This power level is subject to aging and thermal effects. A full production module would include closed loop control of both laser junction temperature and average optical power. Both are simple facilities which we have installed on several transmitters in the past. They are not required under the current program.

2.2 Optical Receivers

The optical receivers must usefully absorb light from the input fiber, convert it to an electrical signal, and then provide low noise

amplification while preserving the bandwidth and linearity of the signal. A high electrical gain is usually needed to overcome conversion and coupling losses, especially if the receiver is to operate at or near its sensitivity limit.

There is always quantum shot noise associated with an optical signal which establishes the lower limit in optical power for on-off signalling at a particular bit error rate. For a bit error rate of 10^{-9} this quantum requirement is 20.8 photons per "1" bit or an average of 10.4 photons per bit period. At a 1400 Mbit/s rate, this quantum limit is 3.5 nW (-54.6 dBm) at 830 nm or 2.3 nW (-56.3 dBm) at 1300 nm.

Performance is always degraded from this limit due to light lost in the detector, excess detector noise, and noise in the preamplifier electronics. The detector and preamplifier must be tightly coupled to give the best performance and the lowest added noise. High speed preamplifier design is well developed for 50 ohm source impedance applications, but experience is more limited with the capacitive source impedance of a photodetector. A considerable effort is necessary to achieve simultaneously low noise, high gain, a high dynamic range, and complete RF stability. The two detector/preamplifier hybrid microcircuit modules used in this program are the most sensitive ever reported in their respective wavelength bands.

The short wavelength receiver uses a silicon avalanche photodiode as the low noise detector. This device is capable of >1.5 GHz bandwidth with a photocurrent gain of 100, or 40 dB. The detector is an ultra low noise developmental part based upon the RCA C30902E commercial device. The hybrid substrate before APD attachment is shown in Figure 2.2. The APD mounts in the lower left corner of the photo. All gold metallization and epoxy bonding is used throughout, following the highest reliability standards used by TRW's Microelectronics Center.

The detector/preamplifier schematic is shown in Figure 2.3. Microwave transistors Q_1 through Q_4 provide four stages of low noise,

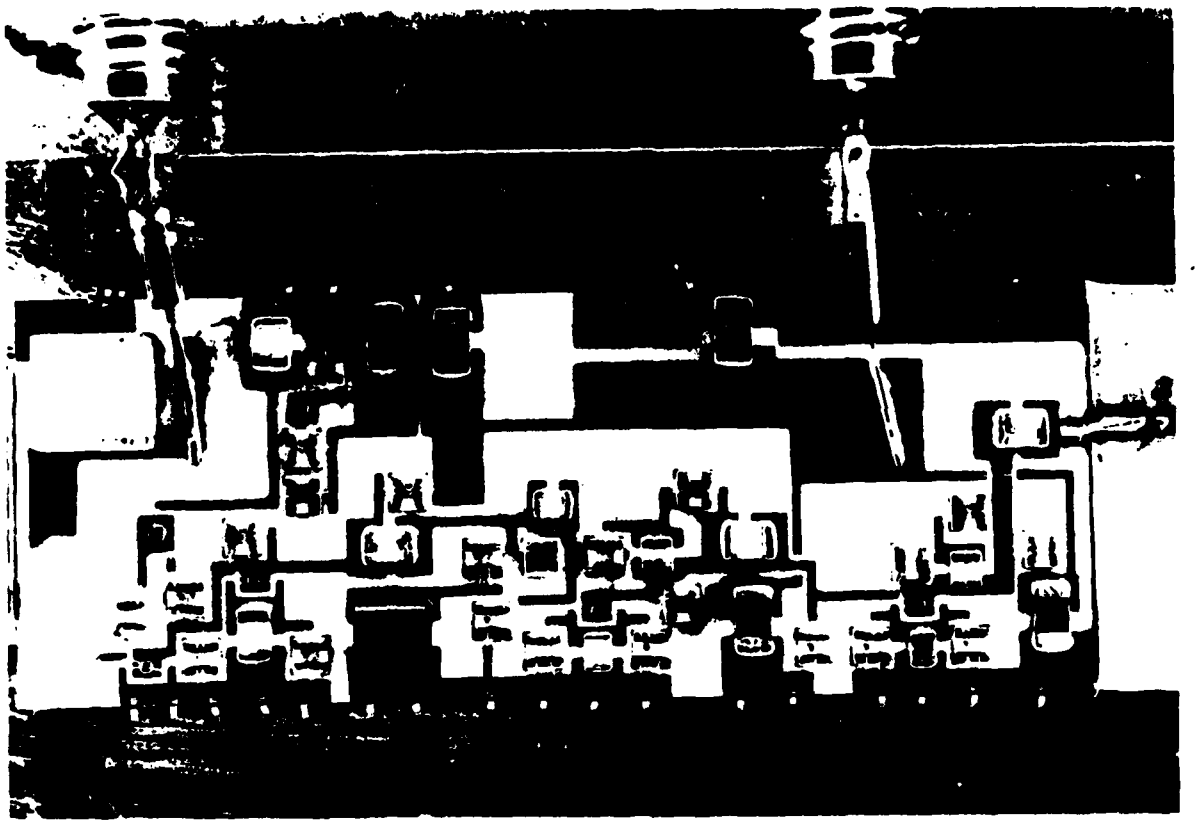


Figure 2.2. 830 nm Receiver Hybrid Substrate

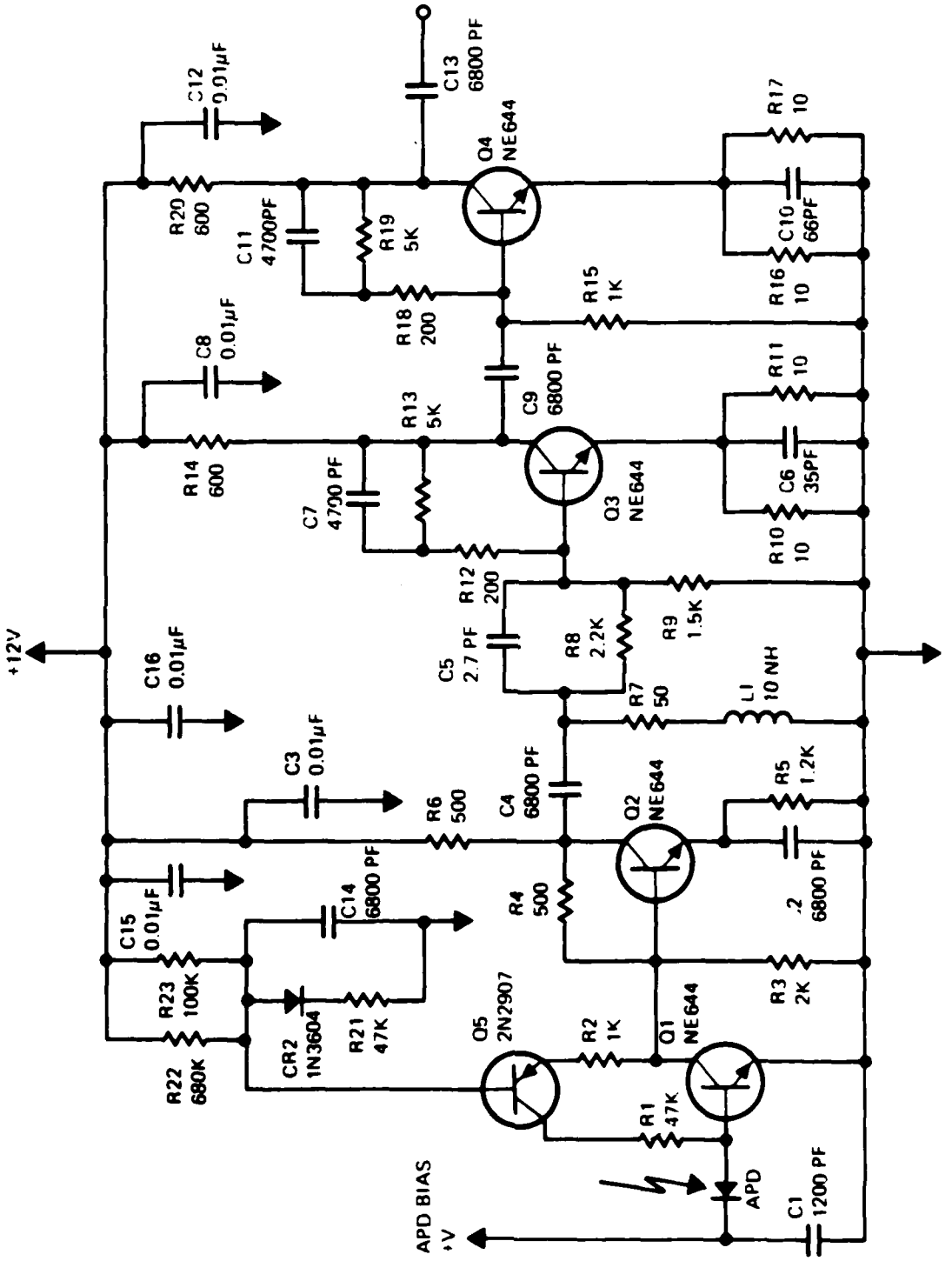


Figure 2.3. 830 nm APD/PREAMP Schematic

high bandwidth gain to achieve a 40 dB current gain overall. The APD and Q_1 are DC coupled in a high impedance front end configuration to minimize noise due to feedback elements. A temperature compensated active bias network consisting of Q_5 and CR_2 provides a temperature dependent Q_1 collector current which keeps the input pole frequency constant. Series equalization to cancel this pole is provided by C_5 and R_8, with the latter part being a laser trimmed thin film chip resistor. This single detector/preamp unit has a total gain of over 80 dB in a substrate 1.55" x .59". Total power dissipation is 200 mW.

The linear response of this 830 nm receiver is shown in Figure 2.4. A Hitachi HLP 3500 830 nm laser was used as the test source in this measurement, modulated at a 50% modulation depth up to 1300 MHz. An independent check on the HLP3500 frequency response was conducted using an AEG Telefunken BPW-28 avalanche photodiode as a reference detector. This showed a 2 dB laser resonance packing at 1300 MHz at the optimum output bias power of 1.5 mW into a graded index pigtail.

The 830 nm APD receiver is designed for a flat response to 800 MHz to preserve minimum noise operation in the NRZ data band. There is excess peaking in the frontend of the circuit at 1000 MHz, due to excessive parasitic inductance in the high voltage bias leads to the APD. A change in the bias lead layout on the hybrid substrate removes this problem in similar receiver circuits. Time constraints dictated a short term fix by relocating the bypass capacitor closer to the APD and replacing inductive conductors with passivating resistor elements.

Highly sensitive avalanche photodiodes are not presently available at 1300 nm, due to a combination of material physics and fabrication problems. The 1300 nm receiver uses a p-i-n photodiode instead of an APD. This is essentially the same receiver as was developed under a previous NRL program, contract number N0000014-82-C-2412 "1 GHz Bandwidth Recirculating Optical Analog Repeater." Figure 2.5 shows the schematic for the 1300 nm hybrid receiver, using a two stage feedback amplifier design. The transistors used are NEC64400 microwave transistor chips.

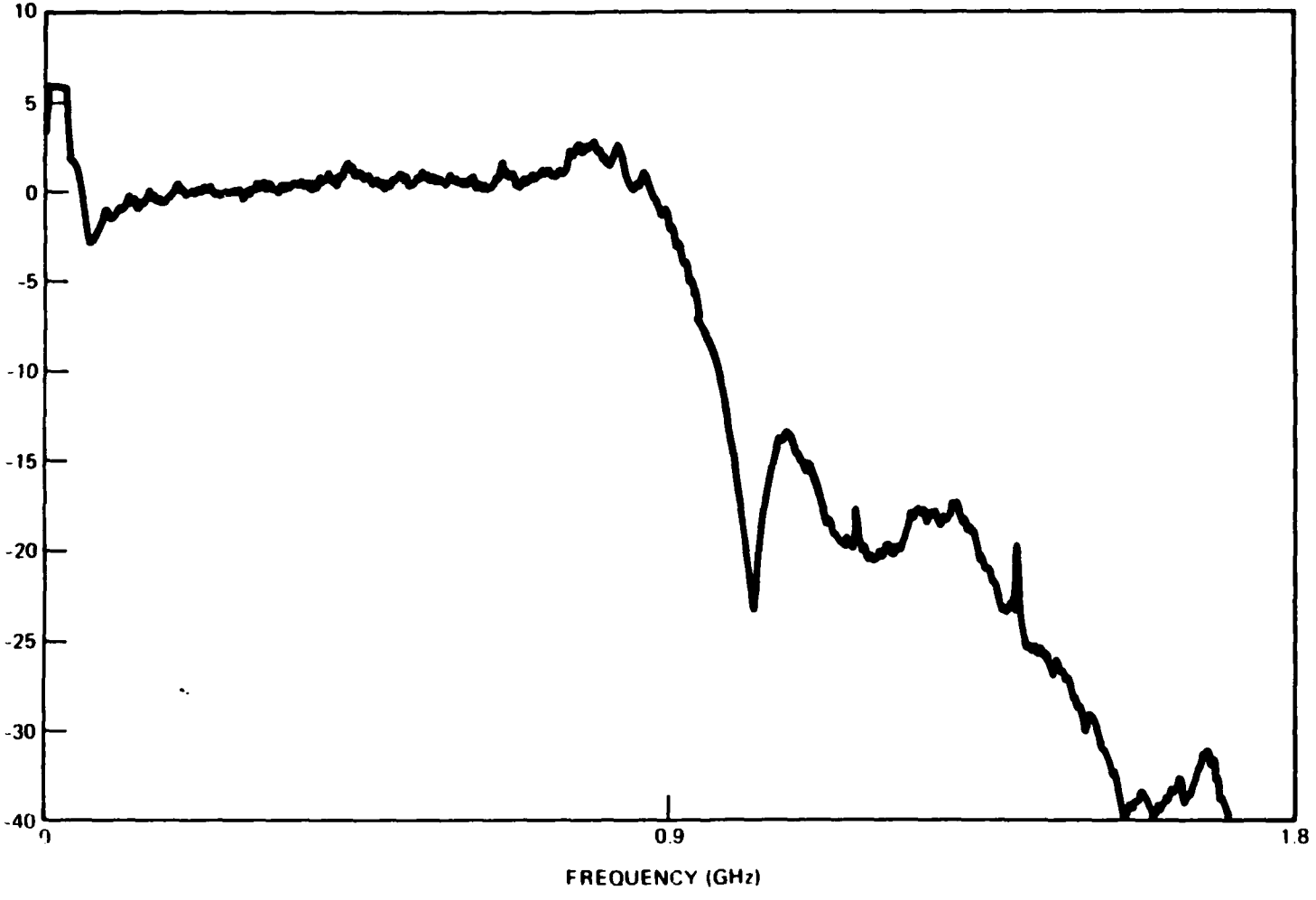


Figure 2.4. Frequency Response of Short Wavelength Optical Receiver

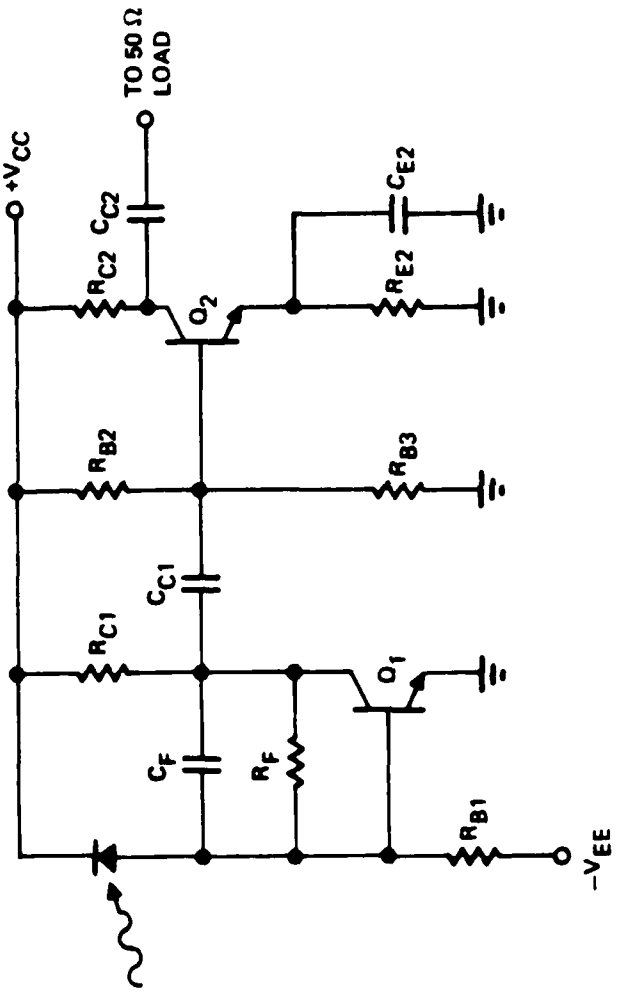


Figure 2.5. Schematic of 1300 nm Hybrid Receiver

Figure 2.6 shows a photograph of a completed hybrid, using thin film resistors, interdigitated trimming capacitors, and high reliability commercial construction procedures. Current gain for this two stage preamplifier is 10, or 20 dB. There is no APD gain, so the 1300 nm receiver requires an additional 60 dB of external gain which is not needed in the 830 nm version. Figure 2.7 shows the frequency response for one of the two deliverable units, as measured using a Hitachi HLP5500 transmitter and an HP Network Analyzer.

Both receiver types use 50 micrometer core fiber pigtails aligned to the respective detector varieties. Neither hybrid package is hermetically sealed, but all semiconductor chips are fully passivated and operable in a laboratory environment.

3. Electronic Components

The electronics section of the basic repeater is more complex than the optical components and interconnections section. There is a very large development effort in high speed digital circuits, for both government and commercial applications. We decided to take an approach which emphasizes rapid prototyping, easy trimming, and lower cost than other digital efforts using large scale custom integration or hybrid digital microcircuit fabrication. This approach used low cost discrete microwave transistors, chip passive components, and three layer printed circuit techniques to construct high speed linear and digital circuits. The device models and circuit topologies developed through several iterations at this level can then be moved to a more integrated technology with long development delays but better potential speed, reliability, and ease of use.

There were few standard electronic modules which we could use directly. Available emitter coupled logic circuits could not approach the 1.4 Gbit/s rates. High speed modular amplifiers are available for use to 1500 MHz, but they produce excessive low frequency phase distortion due to small coupling capacitor values. Some commercial

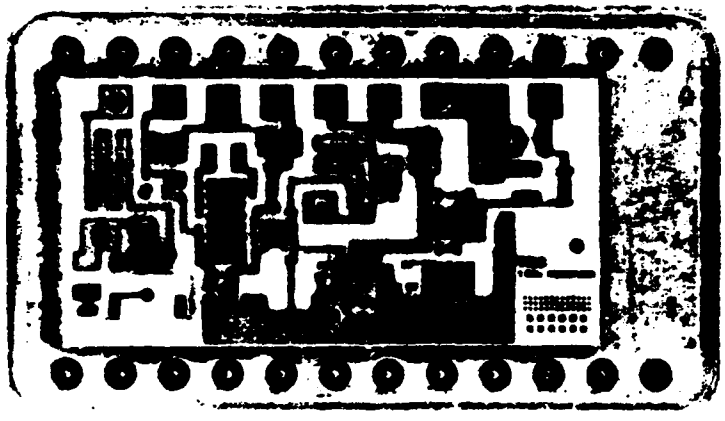


Figure 2.6. 1.3 μm Hybrid Receiver Amplifier

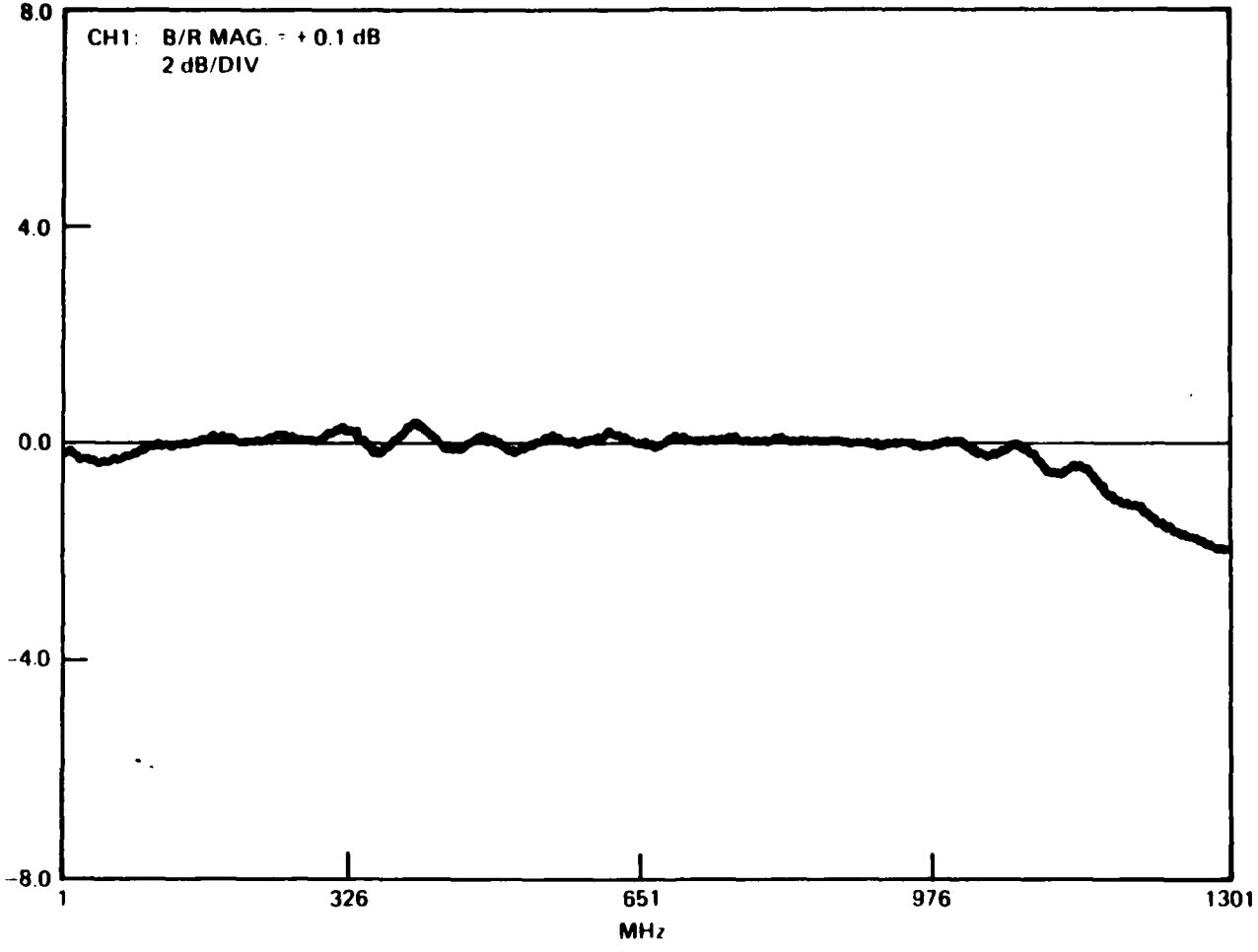


Figure 2.7. Frequency Response of Long Wavelength Optical Receiver

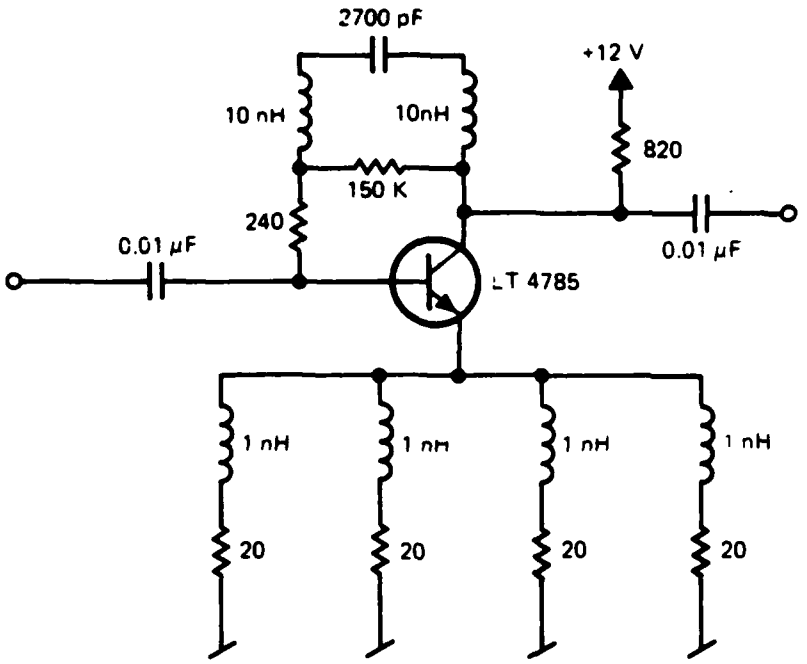
amplifier modules are used in the clock recovery module, where good low frequency response and multistage gain flatness are not needed.

3.1 Gain Stages

A repeater requires gain in numerous places. The repeaters under development need 50 dB in the long wavelength receiver electronics and 40 dB in the surface acoustic wave retiming circuitry. The unbalanced signalling format can have a large low frequency content requiring bandflatness from 1 MHz to beyond 1 GHz. Consideral trimming may be required to achieve the desired linear and nonlinear response.

Figure 3.1 shows the schematic and measured gain for the low power broadband amplifier developed. The stage was designed as a 50 ohm feedback amplifier using TRW LT4785 transistors. Modelling of the transistor, feedback transmission lines, and passive components used the COMPACT microwave analysis/CAD tool. Power consumption is 60 mW per stage. A similar circuit consuming 240 mW per stage was used as the output stage in several gain chains.

Linear amplifiers are excellent for low level signals, but they provide no waveform shaping or level restoration as is needed in digital applications. Fast transitions are necessary to minimize the effects of noise and data filtering. The signal should be quantized (0 or 1) at the transmitter, which implies a two state limiting amplifier. We developed a basic digital buffer stage for these applications, which uses two cascaded differential amplifiers. The same construction techniques are used in the digital buffer as in the linear gain stage, plus multilayer 50 ohm transmission line vias and resistive vias. Figure 3.2 shows the schematic for this basic digital element. The use of series coupling capacitors simplifies the design so long as input signals are present. Like standard logic, the stages are not stable with a DC input signal at the threshold voltage. This is not a problem in our continuous signal repeater application. Figure 3.3 shows the output waveforms for sinusoidal inputs of 100, 400, and 700 MHz. The



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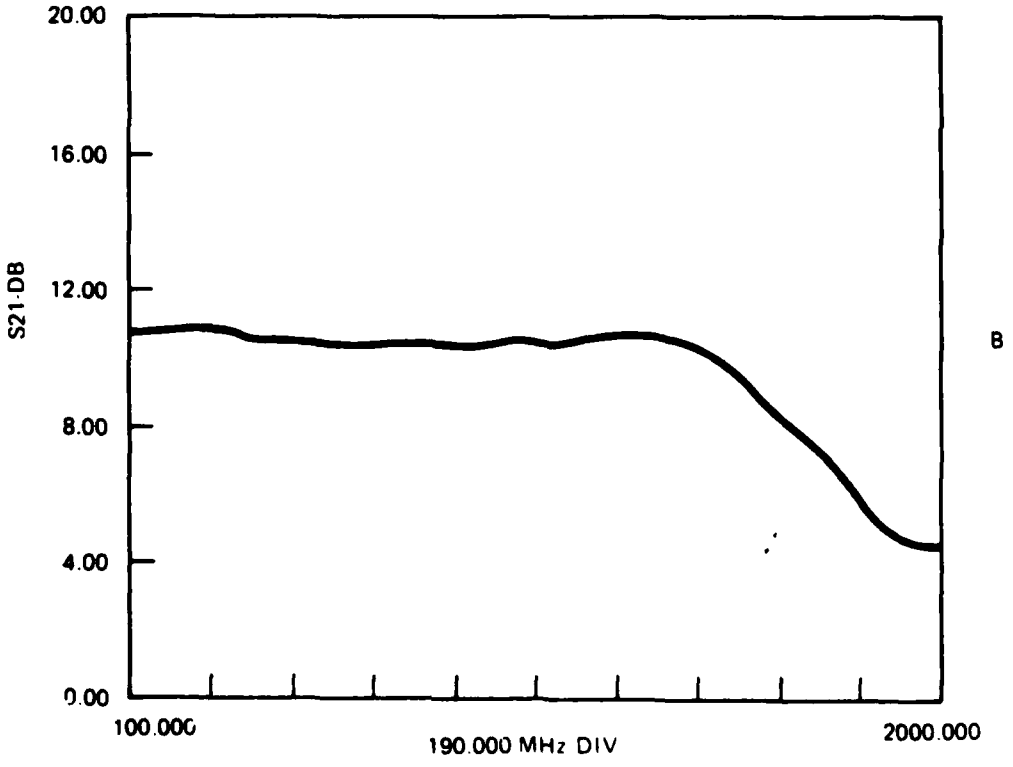

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Figure 3.1. Linear Gain Stage Schematic (A) And Response(B)

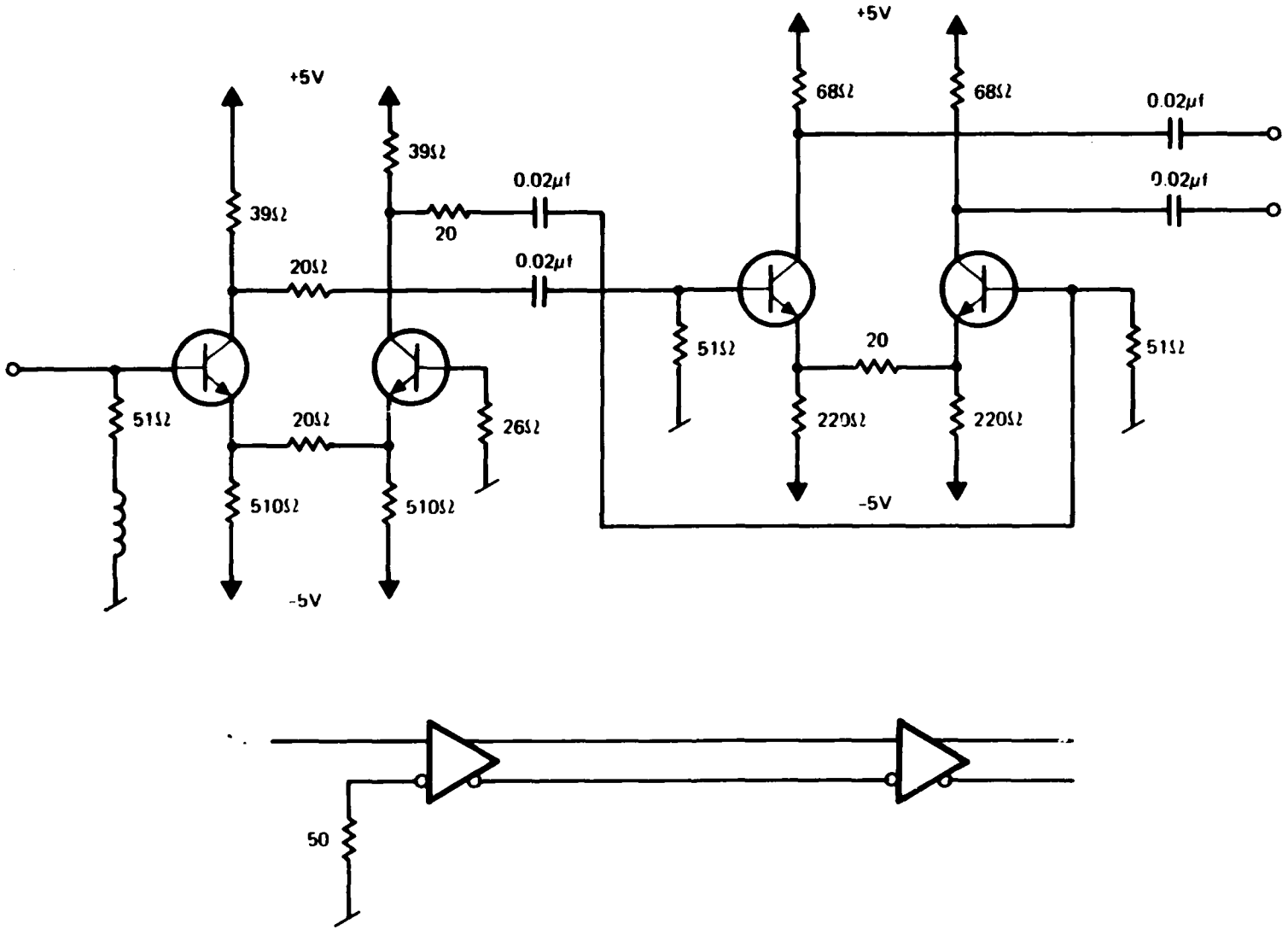
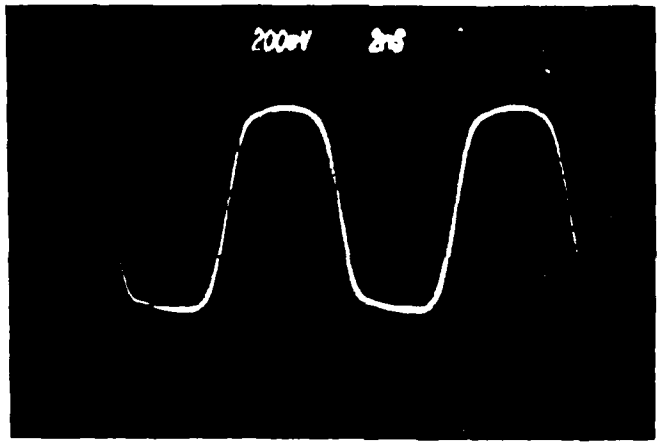
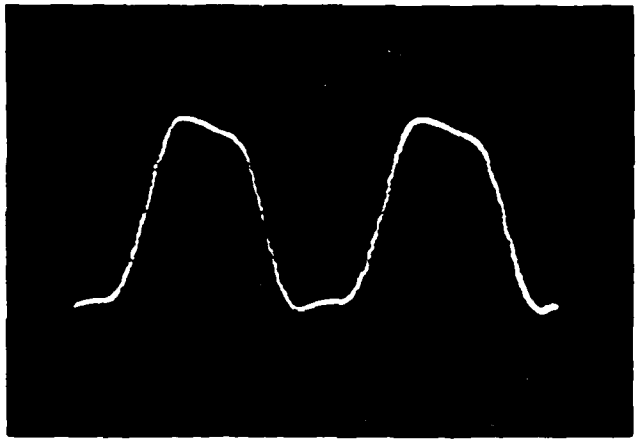


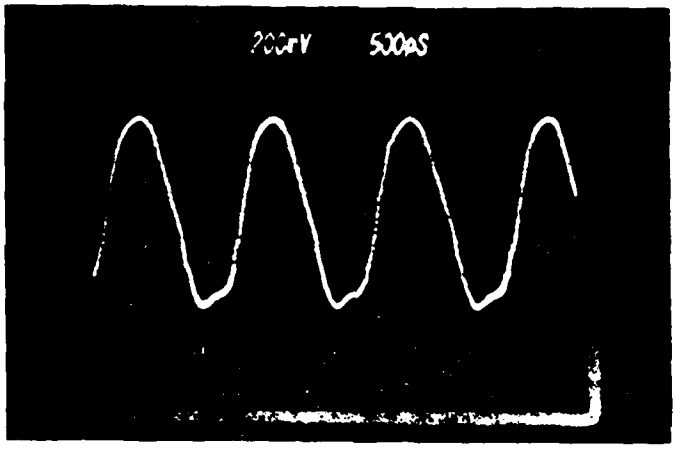
Figure 3.2. Digital Buffer Stage



100 MHZ



400 MHz



700 MHz

Figure 3.3: Digital Buffer Output Sinusoidal Input

risetime improvements over the sinusoidal input risetime indicate a limiting rise and fall time of 300 ps in operation with 1400 Mbit/s input.

Early versions of this circuit did not include the emitter passivating resistors. The emitter interconnection inductance made the circuits unstable at 2.3 GHz. The resistors provided sufficient loss at this frequency to assure stability. With these resistors, the low frequency voltage gain is approximately 4. Both inverted and noninverted output are simultaneously available. Output drive levels of 1.2Vpp into 50 ohms makes these circuits ideal as digital laser drivers.

3.2 Retiming Electronics

Figure 3.4 shows the block diagram for the retiming electronics. The transition detection element uses a half bit delay and multiplier circuit to produce a 1400 MHz clock frequency component from the input data stream. The NRZ data spectrum itself contains no energy at the clock frequency, making this nonlinearity essential. A microstrip high pass filter removes most of the residual data modulation before amplification and narrowband filtering to extract the clock frequency.

The Surface Acoustic Wave (SAW) filter is a linear phase bandpass filter with a Q of 100 and a 1400 MHz center frequency. Figure 3.5 shows the linear response of the filter. This filter averages the clock signal over a 100 bit period, providing a stable reference for the data decision circuit. Pseudo random data will have enough transitions to maintain the required clock amplitude. Non random data, with fixed patterns, may cause fluctuation and phase modulation of the recovered clock, making some sort of clock signal amplitude level control necessary.

The data decision circuit samples the filtered data stream once per bit as driven by the recovered clock. It is equivalent to a flip-flop or D type latch. The digital output of this flip-flop has a constant, 1

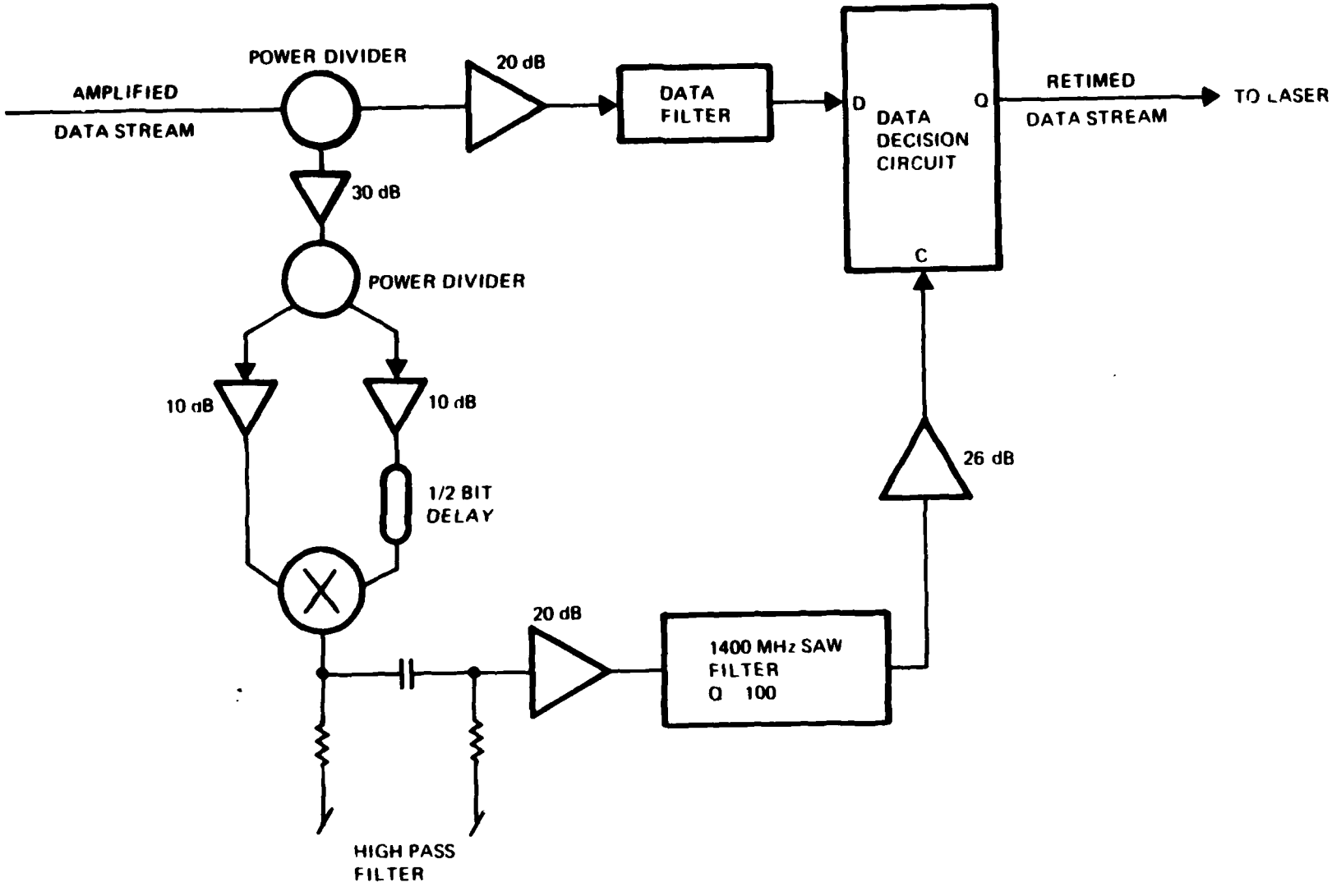


Figure 3.4. Retiming Electronics Block Diagram

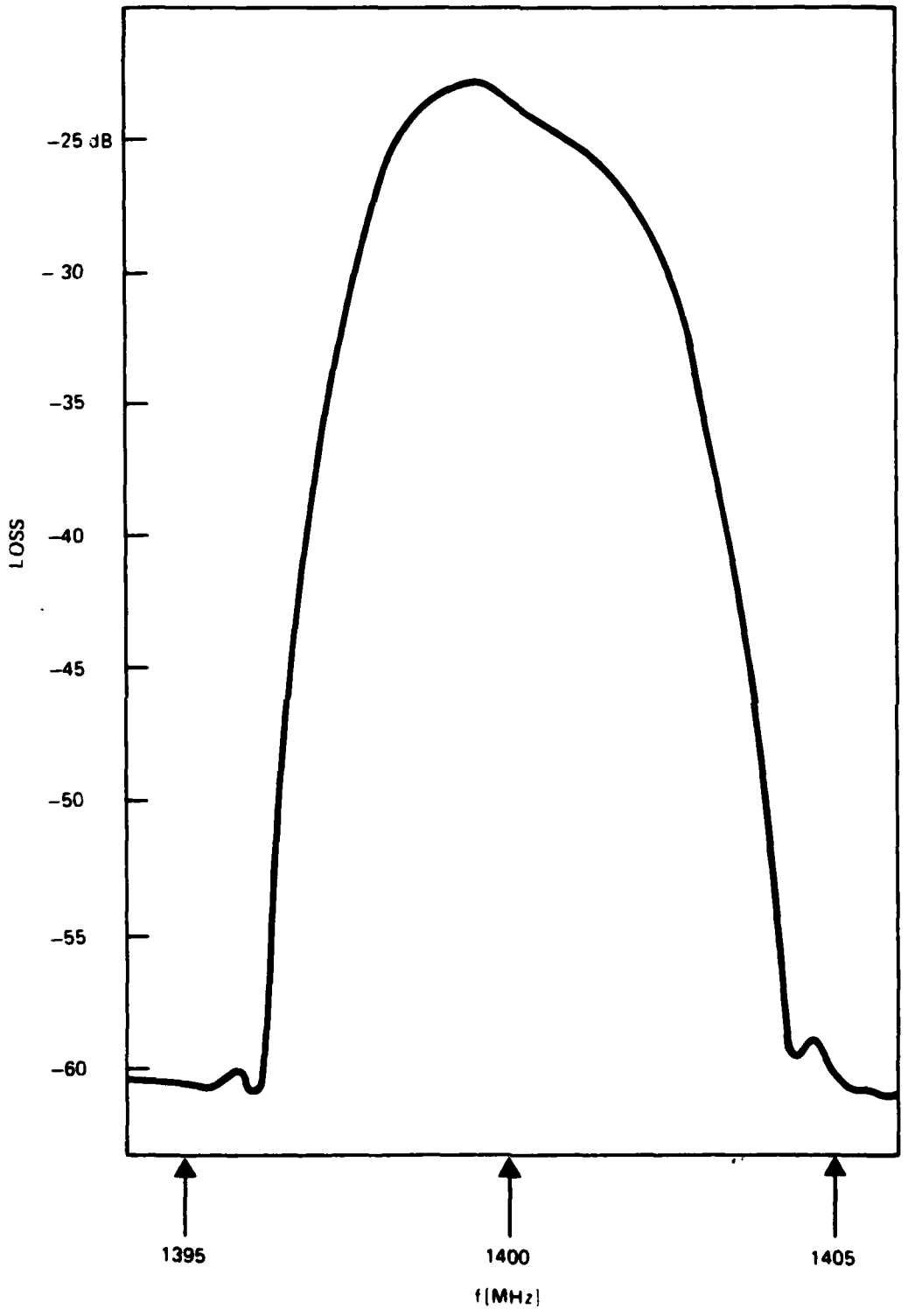


Figure 3.5. SAW Filter Insertion Loss Versus Frequency

bit duty cycle and improved transition times. It is ready for amplification in a digital buffer and delivery to the laser transmitter.

The surface acoustic wave filter has a propagation delay of several hundred bits. The delay of the entire clock recovery chain must be maintained at a constant value within ± 10 ps. The long delay is due to both the high filter Q and to propagation time effects in a SAW filter designed for high sideband rejection. The SAW filter is constructed on a quartz substrate instead of the more common lithium niobate, since the niobate substrate is much more temperature sensitive than the quartz and propagation time can vary excessively.

The SAW filter has an impact on one class of applications. The long delay through the filter chain means that the first few hundred bits in a new transmission are garbled; the clock signal is not present to sample the data. A data delay line is impractical due to the long delays and 1 MHz to 1 GHz bandwidth of the data signal. Normally, this is no problem in telecommunications repeaters, since each repeater receives the transmission of a single source with no interruption or phase discontinuity in the data or data clock. A packet network or recirculating digital memory would be a difficult case, since the clock and laser bias are not continuous across packet boundaries or at the end of each circuit of a recirculating packet. As a rule of thumb for use in systems planning, a user should expect to lose the 200 bits of data per repeater transit from the beginning of an interrupted data stream. Efficient, high speed clock recovery is a difficult problem in packet type communication systems, and a detailed requirements analysis would be necessary before an improved packet repeater could be designed.

The decision circuit shown in Figure 3.6 accomplishes three functions. It converts the sinusoidal clock input into a narrow strobe pulse. This pulse is used to sample the data stream once per bit period. The sampled return-to-zero pulses drive a Schmitt trigger latch as well as a shorted half-bit delay line. The shorted delay line provides 'reset' pulse for every 'set' pulse. This reset pulse follows

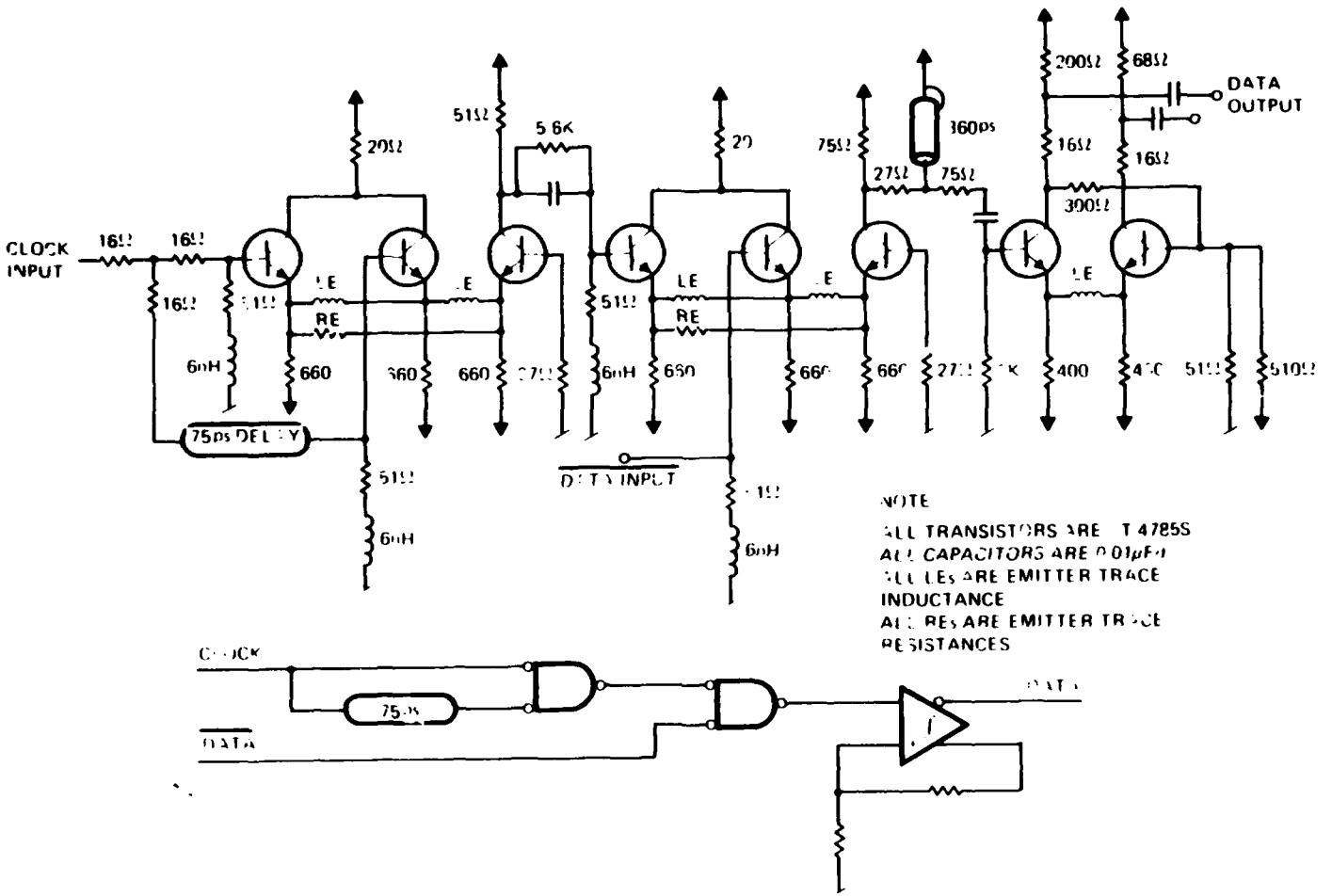


Figure 3.6. Decision Circuit Schematic and Functional Diagram

the set pulse by one bit period, so that all single a 'one' bits are a uniform length. A series of 'set' pulses leaves the latch in the 'one' state until one period after the last 'set' pulse, when the trailing 'reset' pulse restores the latch to a 'zero'. All intervening 'set' and 'reset' pulses cancel to leave the latch undisturbed.

The functional diagram and schematic show our implementation as a set of three discrete gates, each biased at 20 mA per gate. The first two are 'OR' gates, equivalent to NAND gates with inverting inputs. The first produces a 250 ps negative strobe pulse once per bit period. The second uses this strobe pulse to sample the inverted data stream and generate the 'set' pulse. Extra resistive loading is necessary in the Schmitt trigger latch to provide stability in the presence of positive feedback and reflections. Early testing of this unit at 250 Mbit/s (with a longer delay line) showed adequate speed of response but excessive instability at low frequencies. SPICE analysis indicated a change in series coupling capacitance and feedback values, which were used to achieve improved results.

3.3 Test Equipment

The proper test equipment for this repeater includes a bit error rate test set capable of operation of 1400 Mbit/s. This would permit full evaluation of all components for sensitivity, gain and phase distortion, and dynamic range. Anritsu makes such a device, the ME643A, capable of up to 2000 Mbit/s operation. This system is part of our capital plan for 1984 but is not now available to us.

The alternative test equipment developed was a 6 bit fixed pattern or word generator. This word generator exercises the system and components with a digital pattern of "010011". A sampling oscilloscope provides the diagnostic receiver function to compare the original transmitted signal with the signal recovered from the full repeater or subassembly. The word generator pattern gives the worst case combination of high and low frequency components in a pattern with three

one bits and three zero bits. The lower frequency parts of a full pseudo random NRZ spectrum are not attainable in such a word generator scheme.

Figure 3.7 shows the word generator block diagram and schematic. A synthesized 233.333 MHz oscillator (one sixth the data rate) is buffered and converted to a square wave and its complement. Both outputs are applied to a NOR gate after a one bit delay in the complemented signal. This produces a single pulse with a 714ps width every six bit periods. The pulse is split among three delay lines of length 0, 2, and 3 bits. The pulses are recombined, buffered, shaped, amplified, and inverted to produce the digital word shown in Figure 3.8. In the photograph each division corresponds to a single bit, clearly showing that the word is composed of three short pulses in a six bit field. A slight ringing at 2.3 GHz is out of the signal band and has no effect on the repeaters. The 1.2 Vpp output signal corresponds to a 24 mApp output drive, which is more than enough to drive any of the laser transmitters.

3.4 Test and Evaluation

The clock recovery circuit uses the word generator as a test driver. Figure 4.1a shows the power spectrum of the word generator output. The six bit pattern allows only a handful of frequency components, including a residual component at 1400 MHz. This component arises from the return-to-zero coding or with small lengthening of the bit pulse. Therefore it is not a suitable, stable reference for direct clock extraction.

The delay and multiply circuit produces a more stable 1400 MHz reference to use in retiming, one which is not so sensitive to pulse shape. This signal is amplified, prefiltered, and applied to the SAW resonator to give the power spectrum in Figure 4.1b. SAW filter insertion loss is 23 dB, and rejection of the nearest spurious signal is greater than 40 dB. We determined that these spurious signals are due

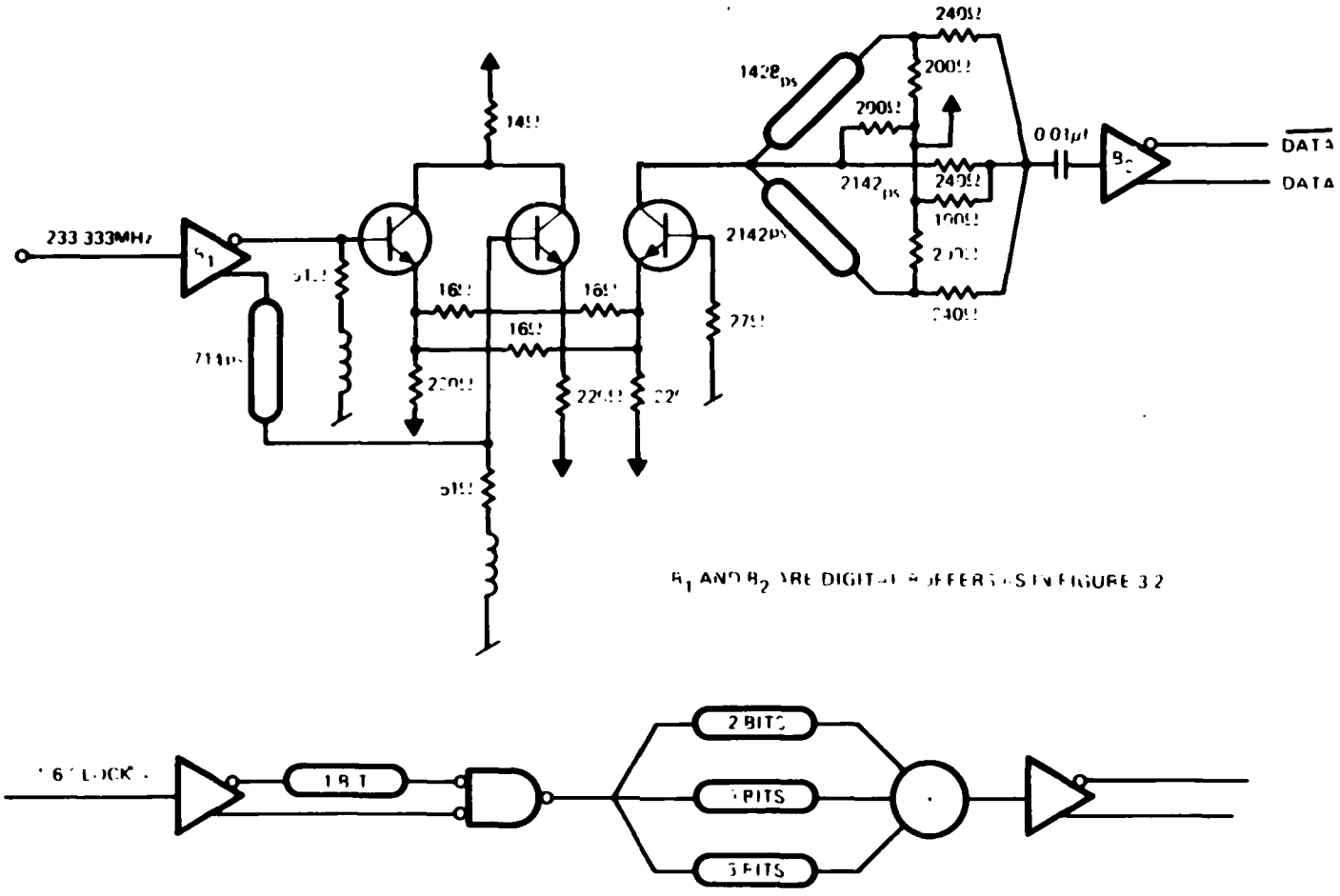


Figure 3.7 6 Bit Word Generator and Block Diagram

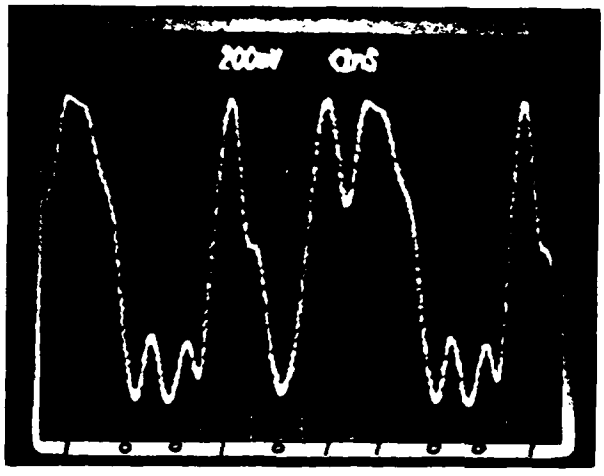


Figure 3.8. 6 Bit Word Generator Output. Horizontal Scale is 714pS 1 Division

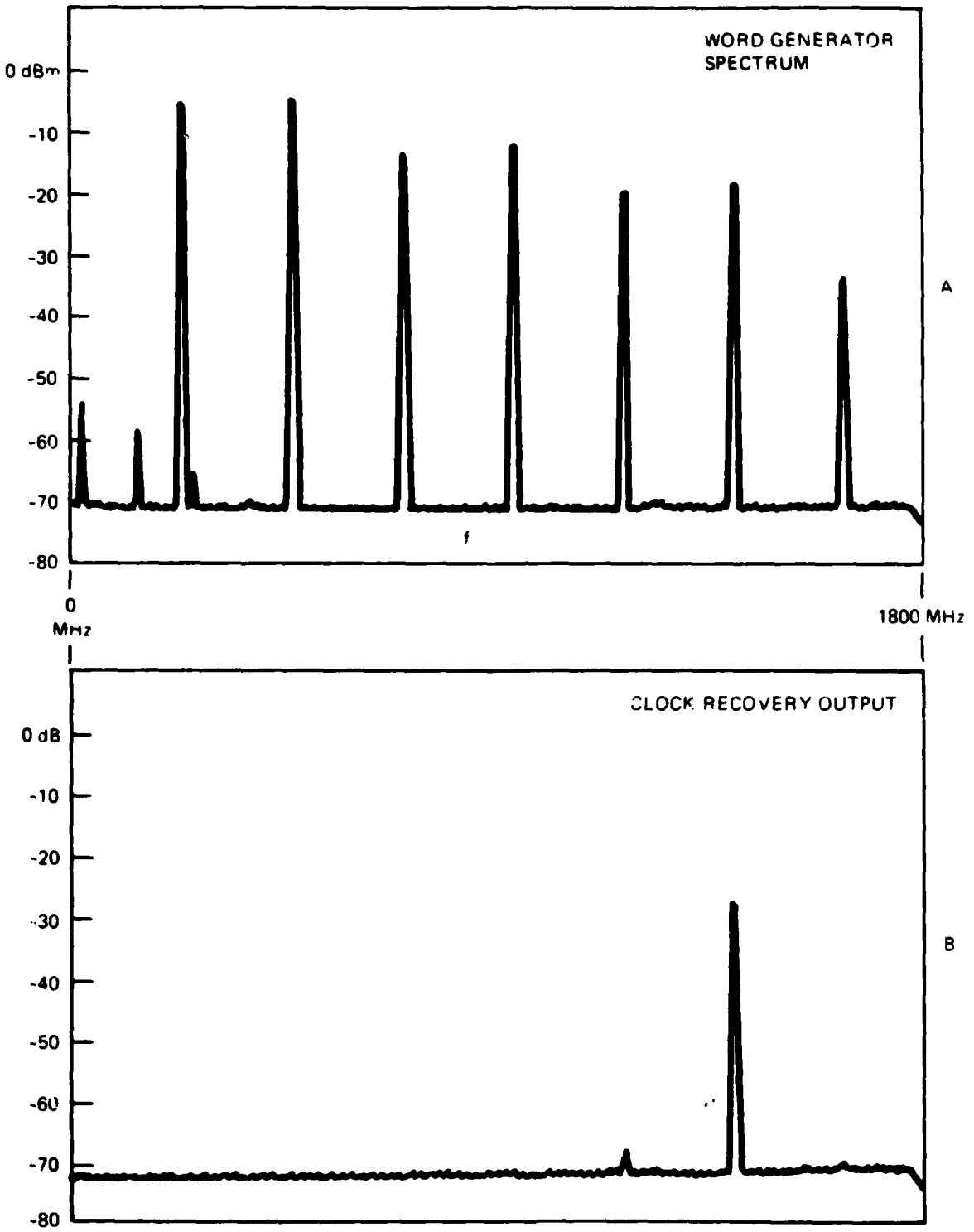
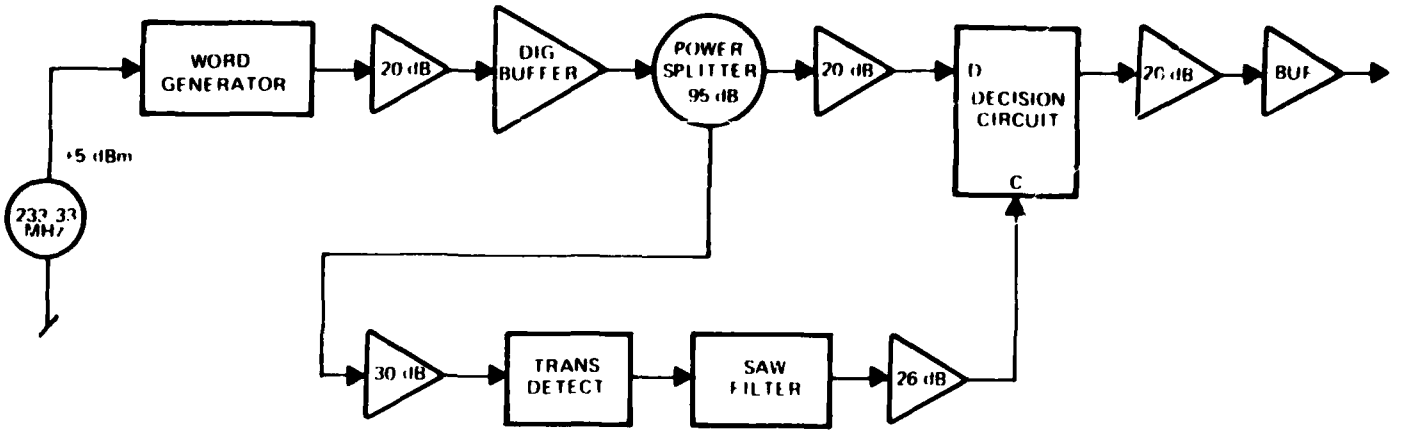


Figure 4.1. Digital Pattern Spectrum Before (A) And After (B) Clock Extraction

to direct RF coupling across the SAW filter contacts and input/output transmission lines. A 40 dB rejection is more than adequate to prevent a direct impact on retiming. Figure 4.2 shows the block diagram and output of the full electrical test of the retiming circuitry. The word generator output drives both the decision circuitry and the clock recovery circuitry through a resistive power divider. Cable delays are adjusted to provide the correct phasing of the clock and data streams at the decision circuit. The regenerated and retimed pattern is shown after linear and digital buffering. The time base is 714 ps/division with bit sampling at the major vertical boundaries.

Adding the 1300 nm transmitter and receiver combination yields the full long wavelength breadboard repeater. The regenerated waveform is shown in Figure 4.3. The long wavelength transmitter and receiver module has a linear gain curve as shown in Figure 2.7. The short wavelength performance was impaired due to inadequate bandwidth margin in the receiver (see Fig. 2.6) and excessive resonance enhancement in the MACOM laser diode. Phase errors above 900 MHz make the particular version of the receiver inadequate above 1000 Mbit/s. The problem is not a fundamental one, and could be resolved with a new hybrid layout and revised gain/bandwidth tradeoffs.

We have therefore designed, assembled and tested the critical technical elements for 1400 Mbit/s repeaters at both 830 and 1300 nm wavelength regions using single mode fiber coupled parts.



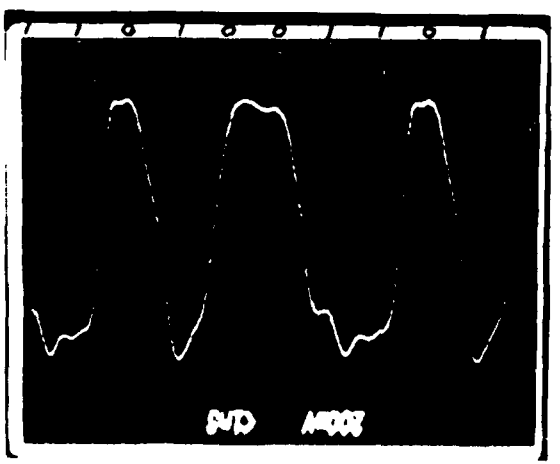


Figure 4.2. Regenerator Electrical Testing

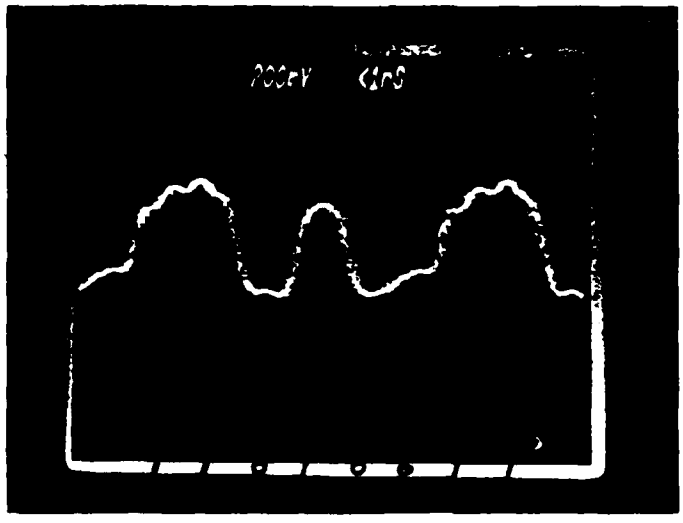
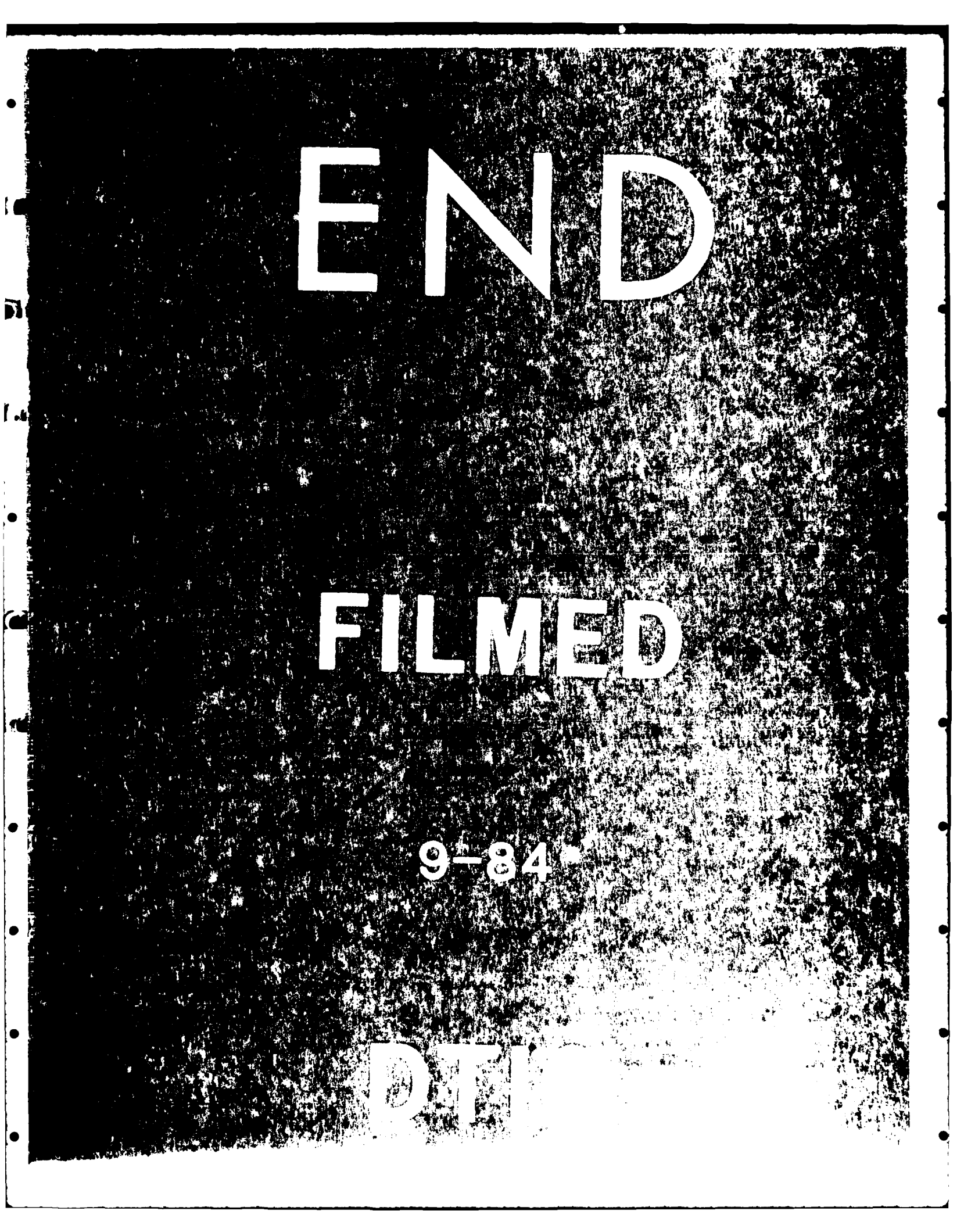


Figure 4.3. Regenerated Waveform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