ASD(ENA)-TR-82-5031
VOLUME I V

(2)

2nd AFSC STANDARDIZATION CONFERENCE

COMBINED PARTICIPATION BY:
DOD-ARMY-NAVY-AIR FORCE-NATO

30 NOVEMBER - 2 DECEMBER 1982
TUTORIALS: 29 NOVEMBER 1982

DAYTON CONVENTION CENTER
DAYTON, OHIO

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MIL-STD-1553
MULTIPLEX DATA BUS

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This technical report has been reviewed and is approved for publication.

Jeffery L Pesler

JEFFERY L. PESLER
Vice Chairman
2nd AFSC Standardization Conference

E. C. Gangl

ERWIN C. GANGL
Chief, Avionics Systems Division
Directorate of Avionics Engineering

FOR THE COMMANDER

Robert P Lavoie

ROBERT P. LAVOIE, COL, USAF
Director of Avionics Engineering
Deputy for Engineering

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This is a collection of UNCLASSIFIED papers to be distributed to the attendees of the Second AFSC Avionics Standardization Conference at the Convention Center, Dayton, Ohio. The scope of the Conference includes the complete range of DoD approved embedded computer hardware/software and related interface standards as well as standard subsystems used within the Tri-Service community and NATO. The theme of the conference is "Rational Standardization". Lessons learned as well as the pros and cons of standardization are highlighted.

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This is Volume 4

Volume 1	Proceedings pp. 1-560
Volume 2	Proceedings pp. 561-1131
Volume 3	Governing Documents
Volume 4	MIL-STD-1553 Tutorial
Volume 5	MIL-STD-1589 Tutorial
Volume 6	MIL-STD-1679 Tutorial
Volume 7	MIL-STD-1750 Tutorial
Volume 8	MIL-STD-1815 Tutorial
Volume 9	Navy Case Study Tutorial

PROCEEDINGS OF THE

2nd AFSC STANDARDIZATION CONFERENCE

30 NOVEMBER - 2 DECEMBER 1982

DAYTON CONVENTION CENTER
DAYTON, OHIO

Sponsored by:

Air Force Systems Command

Hosted by:

Aeronautical Systems Division

FOREWORD

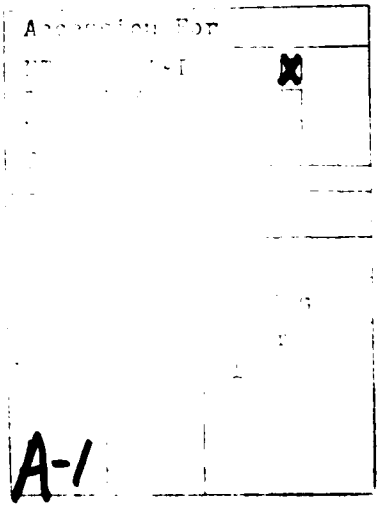
THE UNITED STATES AIR FORCE HAS COMMITTED ITSELF TO "STANDARDIZATION." THE THEME OF THIS YEAR'S CONFERENCE IS "RATIONAL STANDARDIZATION," AND WE HAVE EXPANDED THE SCOPE TO INCLUDE US ARMY, US NAVY AND NATO PERSPECTIVES ON ONGOING DOD INITIATIVES IN THIS IMPORTANT AREA.

WHY DOES THE AIR FORCE SYSTEMS COMMAND SPONSOR THESE CONFERENCES? BECAUSE WE BELIEVE THAT THE COMMUNICATIONS GENERATED BY THESE GET-TOGETHERS IMPROVE THE ACCEPTANCE OF OUR NEW STANDARDS AND FOSTERS EARLIER, SUCCESSFUL IMPLEMENTATION IN NUMEROUS APPLICATIONS. WE WANT ALL PARTIES AFFECTED BY THESE STANDARDS TO KNOW JUST WHAT IS AVAILABLE TO SUPPORT THEM: THE HARDWARE; THE COMPLIANCE TESTING; THE TOOLS NECESSARY TO FACILITATE DESIGN, ETC. WE ALSO BELIEVE THAT FEEDBACK FROM PEOPLE WHO HAVE USED THEM IS ESSENTIAL TO OUR CONTINUED EFFORTS TO IMPROVE OUR STANDARDIZATION PROCESS. WE HOPE TO LEARN FROM OUR SUCCESSES AND OUR FAILURES; BUT FIRST, WE MUST KNOW WHAT THESE ARE AND WE COUNT ON YOU TO TELL US.

AS WE DID IN 1980, WE ARE FOCUSING OUR PRESENTATIONS ON GOVERNMENT AND INDUSTRY EXECUTIVES, MANAGERS, AND ENGINEERS AND OUR GOAL IS TO EDUCATE RATHER THAN PRESENT DETAILED TECHNICAL MATERIAL. WE ARE STRIVING TO PRESENT, IN A SINGLE FORUM, THE TOTAL AFSC STANDARDIZATION PICTURE FROM POLICY TO IMPLEMENTATION. WE HOPE THIS INSIGHT WILL ENABLE ALL OF YOU TO BETTER UNDERSTAND THE "WHY'S AND WHEREFORE'S" OF OUR CURRENT EMPHASIS ON THIS SUBJECT.

MANY THANKS TO A DEDICATED TEAM FROM THE DIRECTORATE OF AVIONICS ENGINEERING FOR ORGANIZING THIS CONFERENCE; FROM THE OUTSTANDING TECHNICAL PROGRAM TO THE UNGLAMOROUS DETAILS NEEDED TO MAKE YOUR VISIT TO DAYTON, OHIO A PLEASANT ONE. THANKS ALSO TO ALL THE MODERATORS, SPEAKERS AND EXHIBITORS WHO RESPONDED IN SUCH A TIMELY MANNER TO ALL OF OUR PLEAS FOR ASSISTANCE.

ROBERT P. LAVOIE, COL, USAF
DIRECTOR OF AVIONICS ENGINEERING
DEPUTY FOR ENGINEERING



DEPARTMENT OF THE AIR FORCE

HEADQUARTERS AIR FORCE SYSTEMS COMMAND
ANDREWS AIR FORCE BASE, DC 20334

28 AUG 1982

REPLY TO ATTN OF: CV

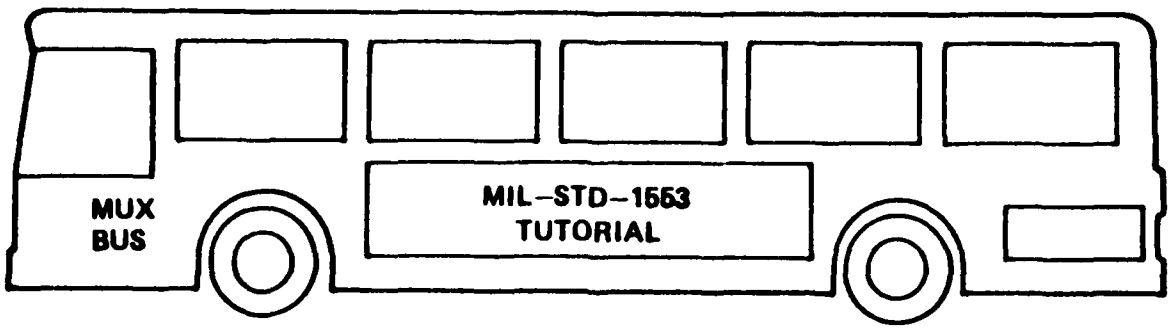
SUBJECT: Second AFSC Standardization Conference

TO: ASD/CC

1. Since the highly successful standardization conference hosted by ASD in 1980, significant technological advancements have occurred. Integration of the standards into weapon systems has become a reality. As a result, we have many "lessons learned" and cost/benefit analyses that should be shared within the tri-service community. Also, this would be a good opportunity to update current and potential "users." Therefore, I endorse the organization of the Second AFSC Standardization Conference.

2. This conference should cover the current accepted standards, results of recent congressional actions, and standards planned for the future. We should provide the latest information on policy, system applications, and lessons learned. The agenda should accommodate both government and industry inputs that criticize as well as support our efforts. Experts from the tri-service arena should be invited to present papers on the various topics. Our AFSC project officer, Maj David Hammond, HQ AFSC/ALR, AUTOVON 858-5731, is prepared to assist.

ROBERT M. BOND, Lt Gen, USAF
Vice Commander



2nd AFSC Standardization Conference

AL CROSSGROVE
BOEING

LEROY EARHART
TEST SYSTEMS

DON ELLIS
AEROSYSTEMS

DR. LEE SMITH
BOEING

Agenda

8:30	Introduction & System Design Issues
9:30	Hardware Design
10:10	Break
10:20	Test
11:00	Software Design
11:30	Panel Discussion

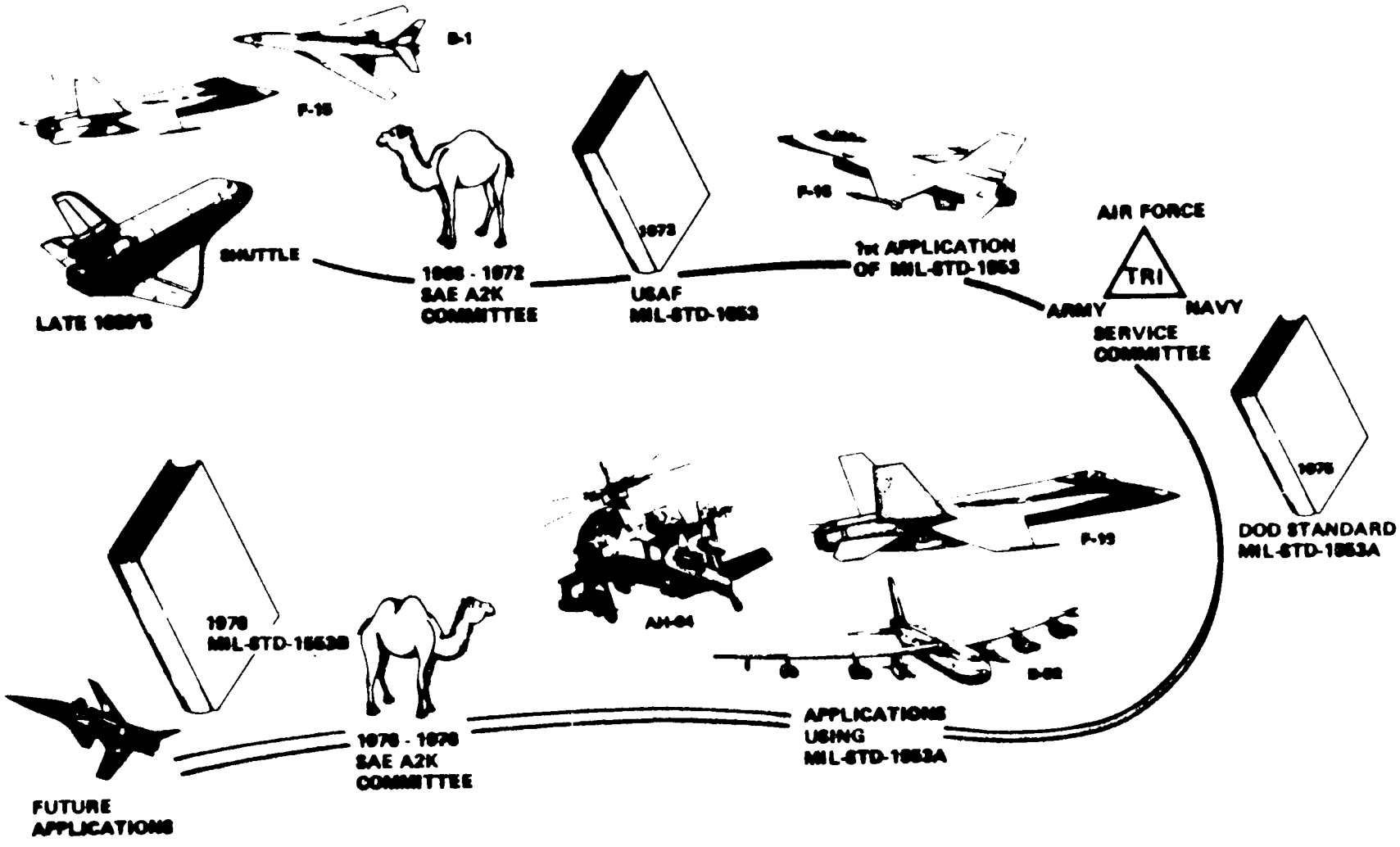
Introduction

and

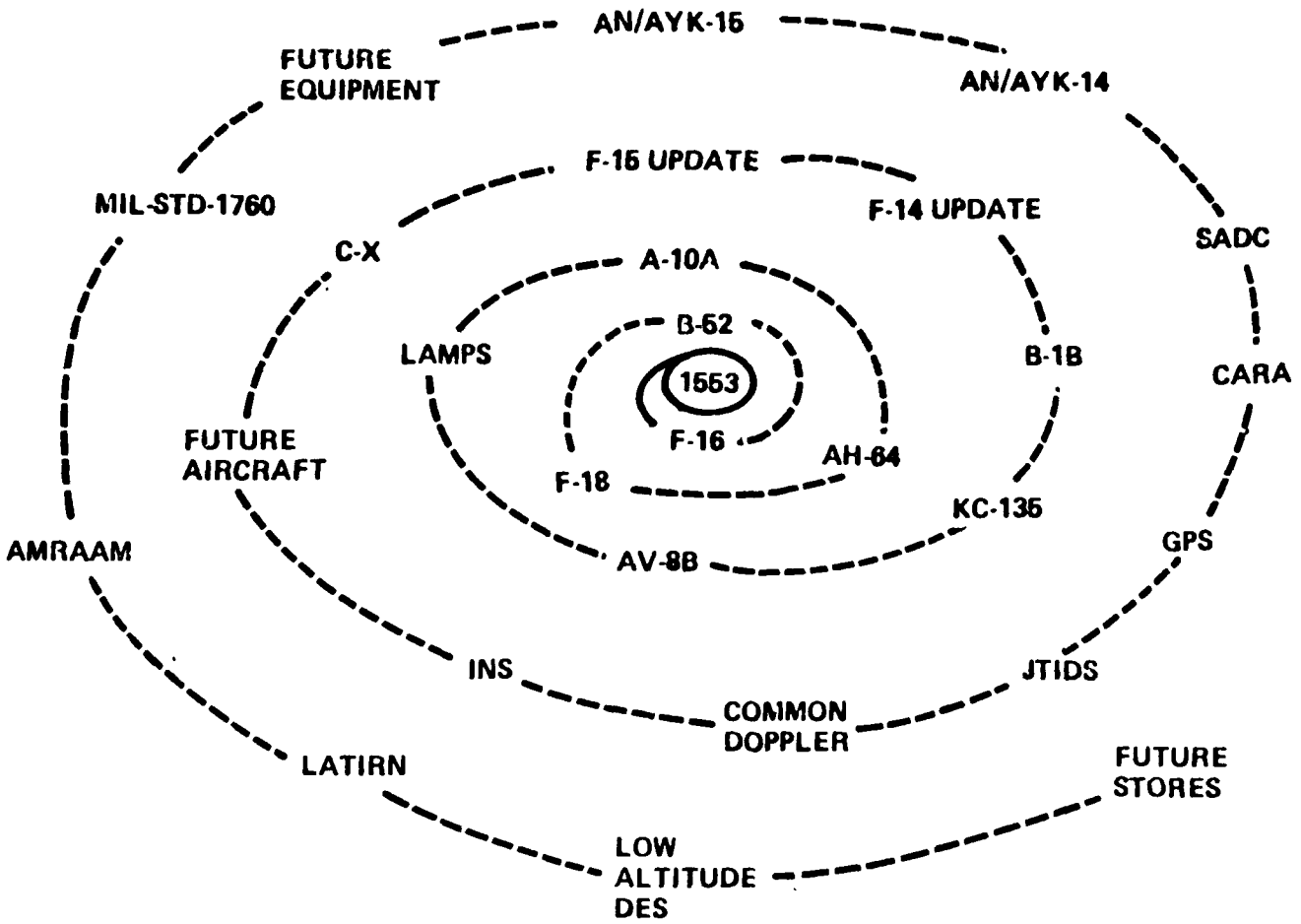
System Design

AL CROSSGROVE

History of the Standard

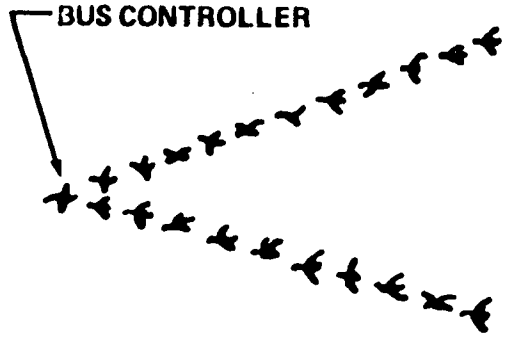


Mil-Std-1553 Applications



Why Multiplexing

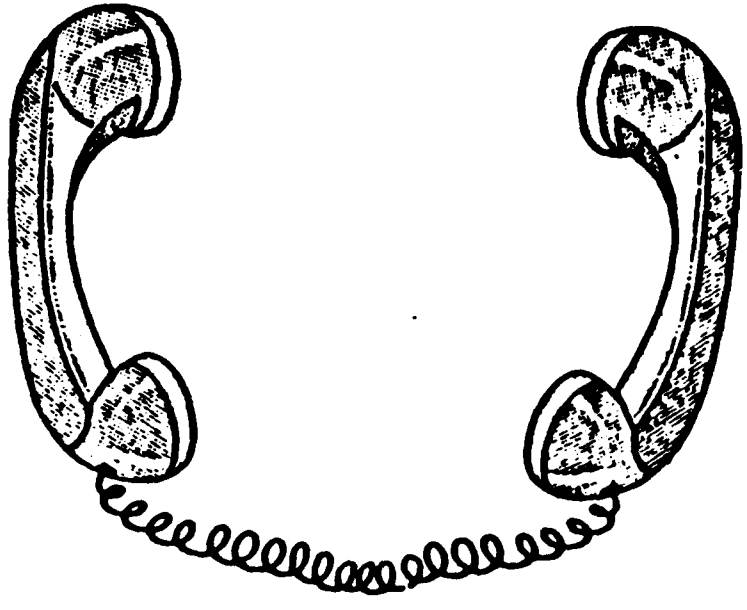
MIL-STD-1553 INTEGRATION



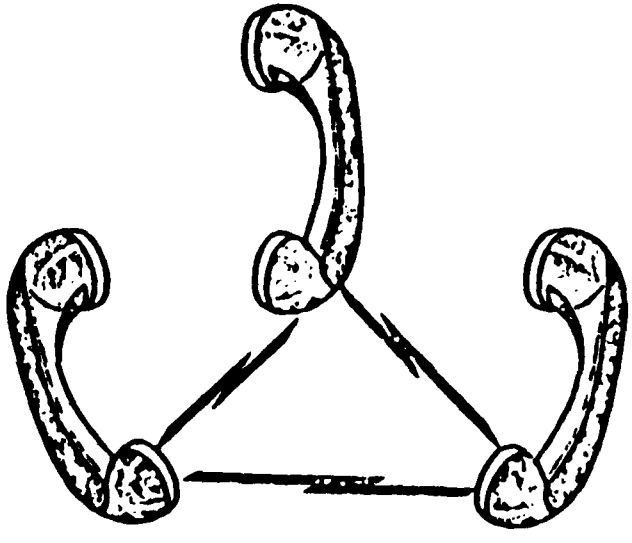
NON-MIL-STD-1553 INTEGRATION

Multiplexing

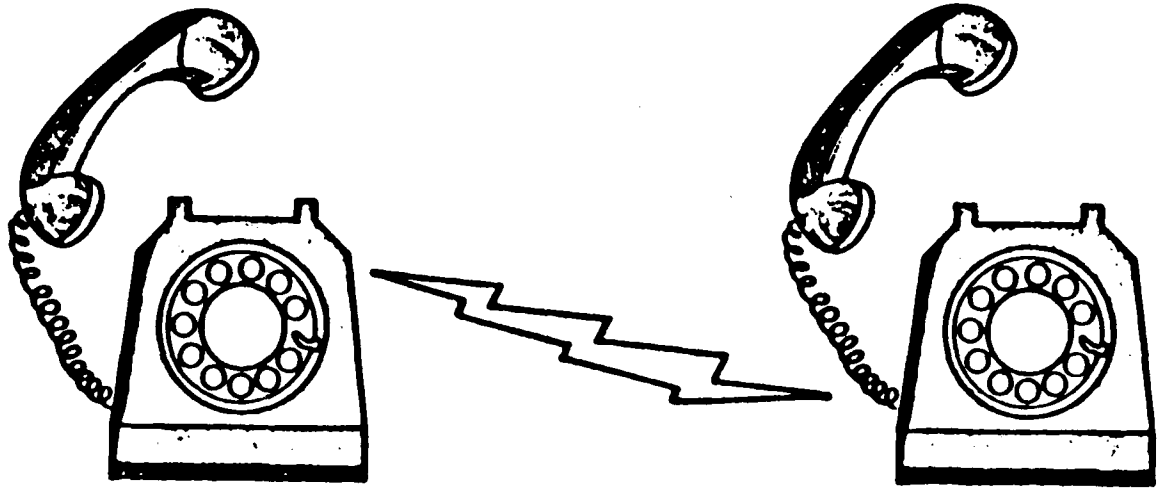
POINT TO POINT COMMUNICATION



PARTY LINE COMMUNICATIONS



Protocol

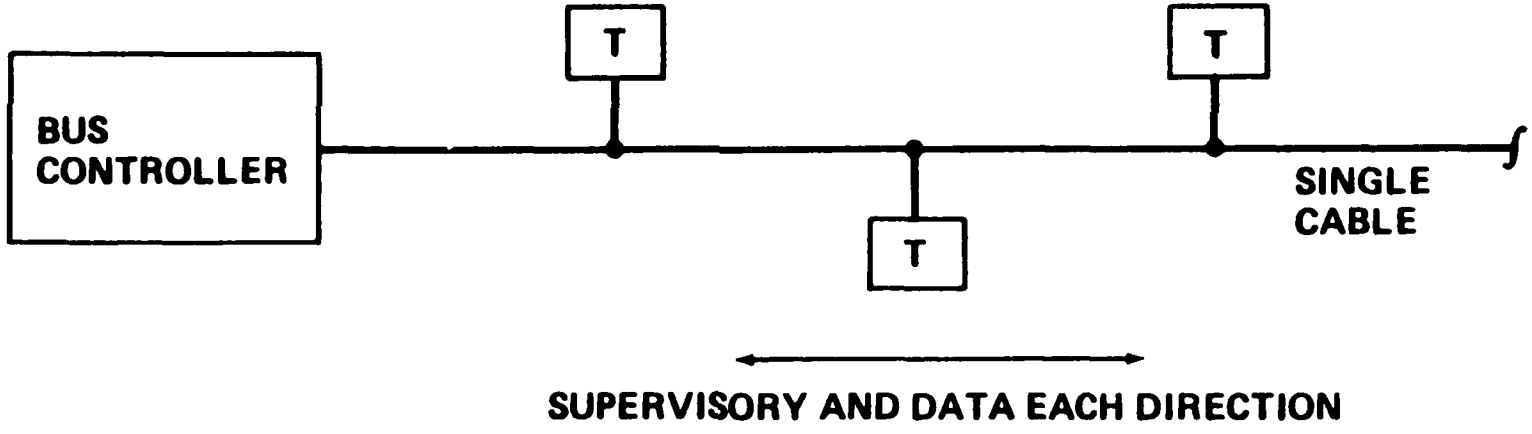


COMMAND/RESPONSE

HI, MY NAME IS _____
WOULD YOU SEND ME SOME
INFORMATION ?

YES! HERE IT COMES !

Bus Controller



Protocol Words

- COMMAND

  TRANSMITTED ONLY BY BUS CONTROLLER; CONTAINS ADDRESS OF ONE RECEIVING COMMAND

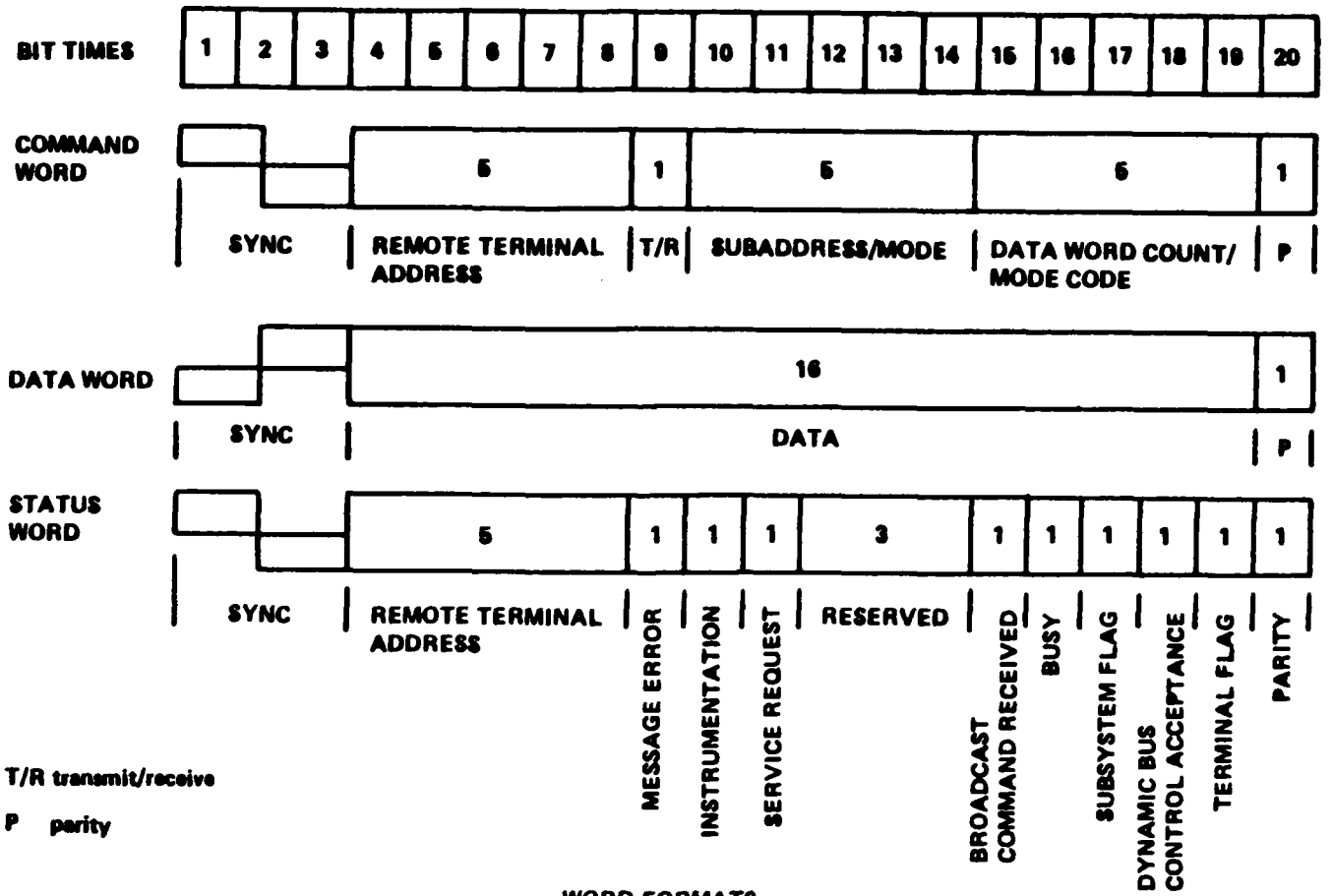
- STATUS

  TRANSMITTED ONLY BY REMOTE TERMINALS; CONTAINS THEIR OWN ADDRESS AND HEALTH INFORMATION

- DATA

  TRANSMITTED OR RECEIVED BY ANY UNIT

Protocol

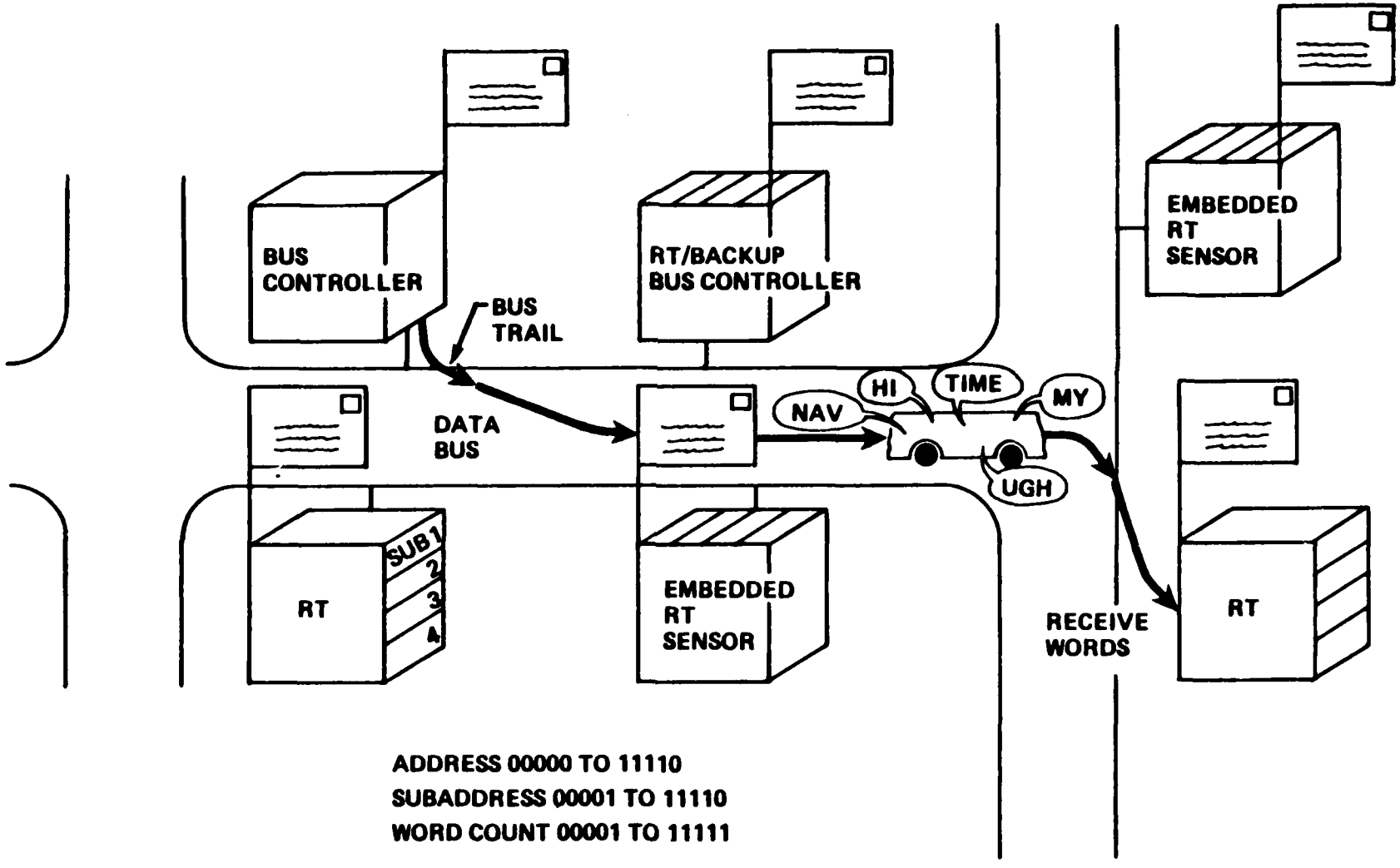


T/R transmit/receive

P parity

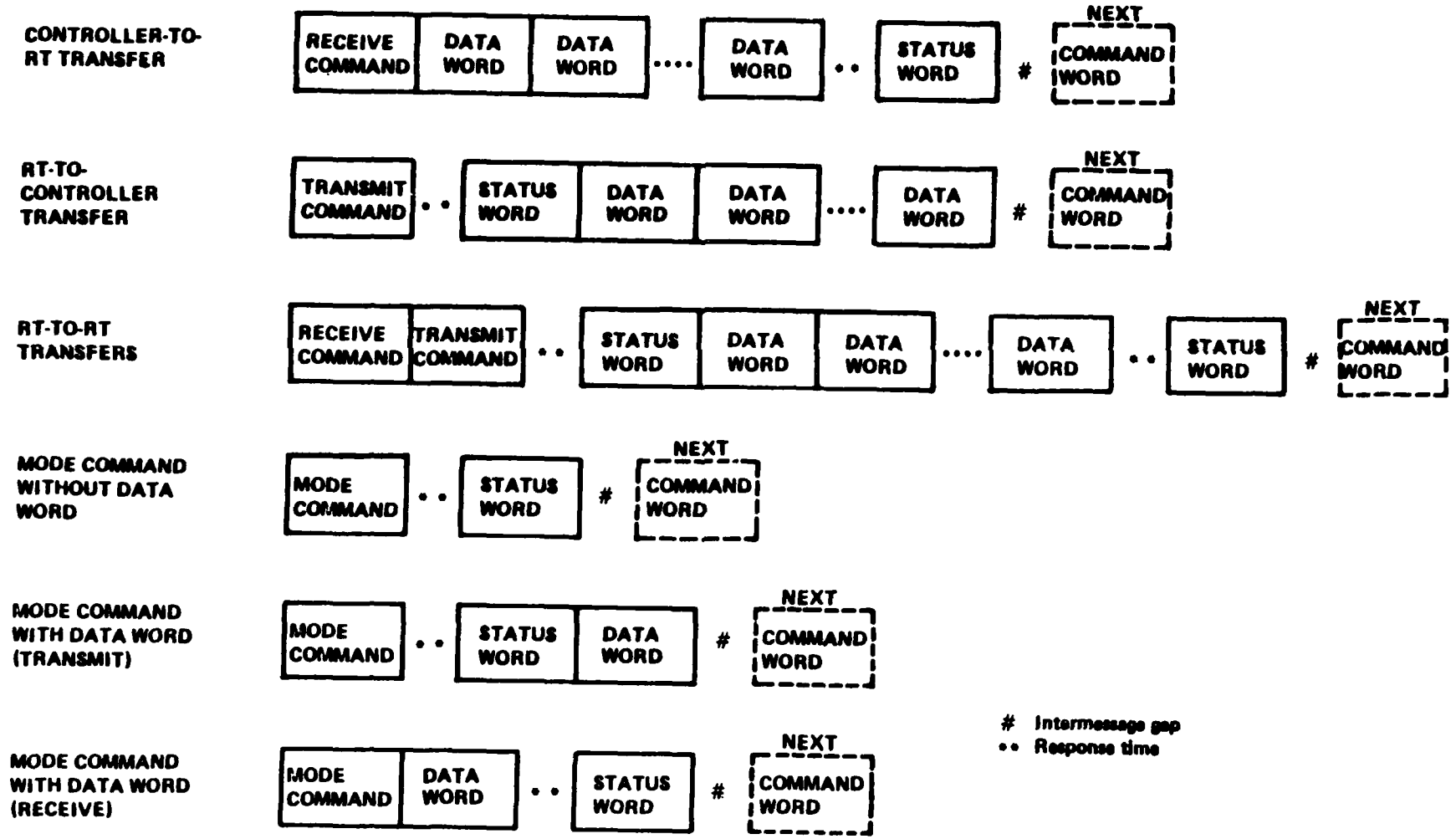
WORD FORMATS

Terminal Communication Method

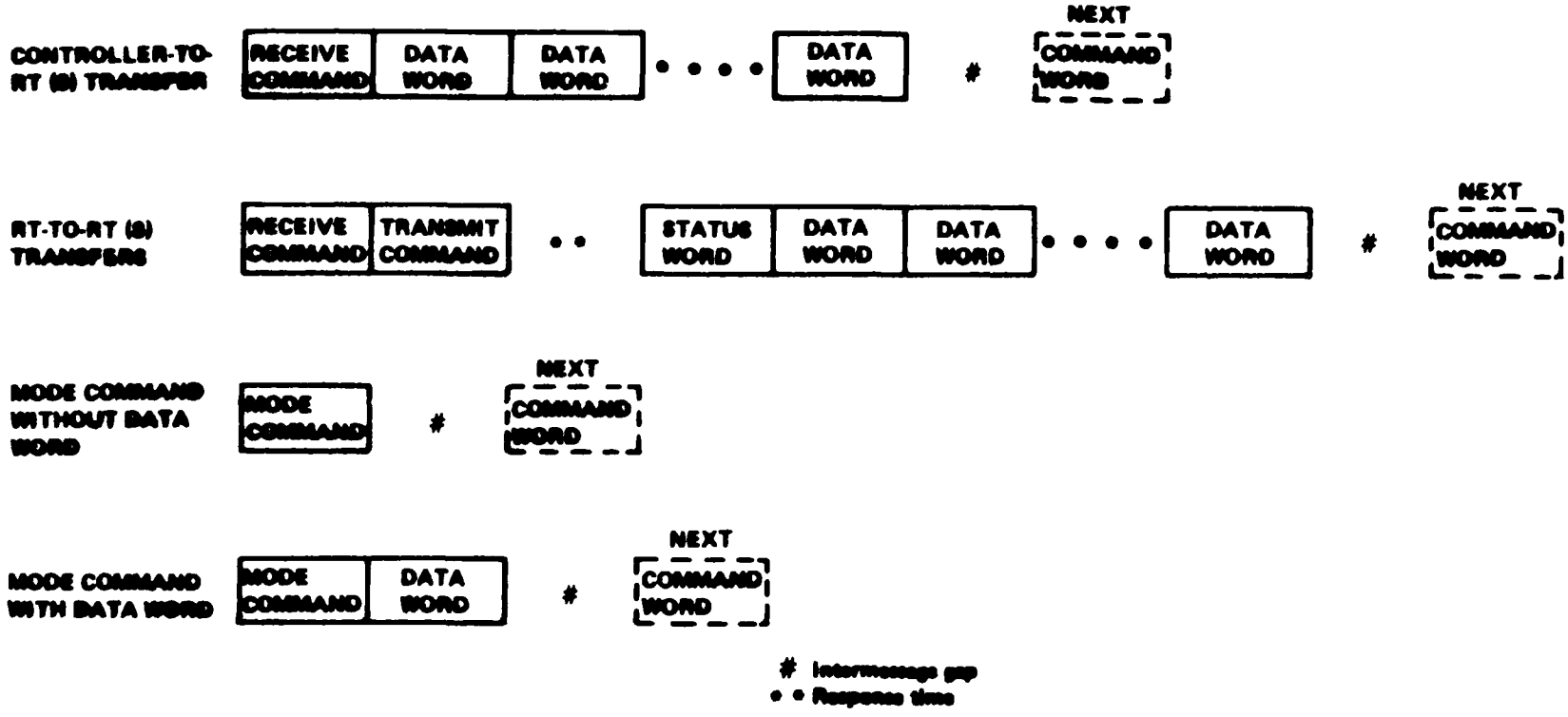


ADDRESS 00000 TO 11110
SUBADDRESS 00001 TO 11110
WORD COUNT 00001 TO 11111

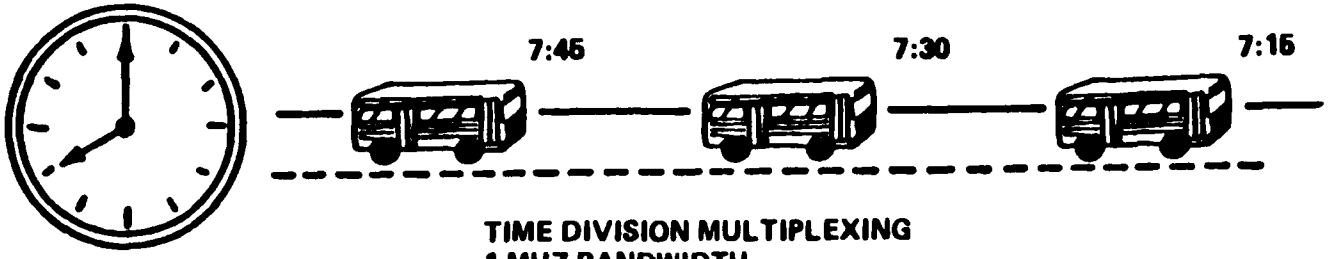
Message Formats



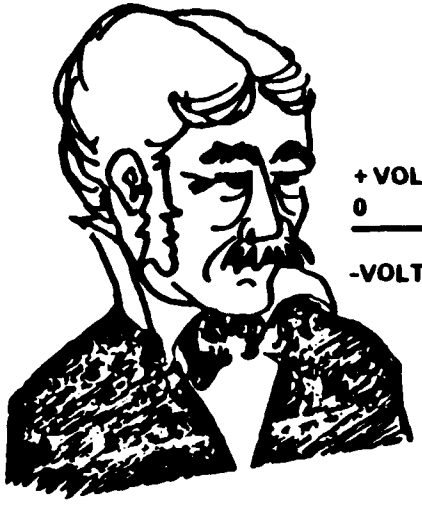
Message Formats



Coding Techniques

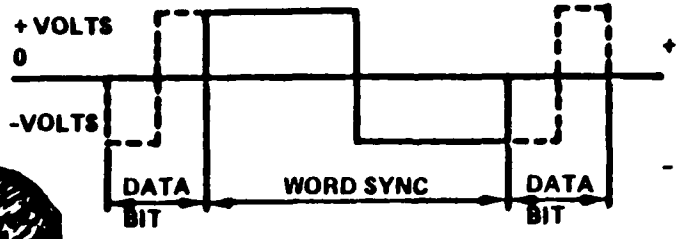


TIME DIVISION MULTIPLEXING
1 MHZ BANDWIDTH

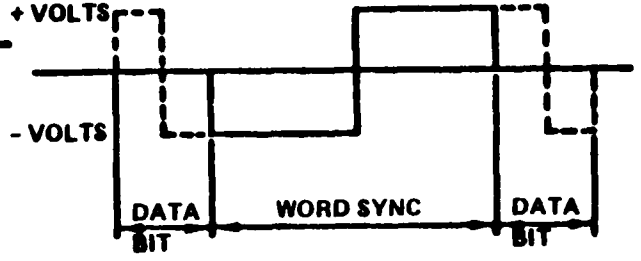


MR. MANCHESTER

MANCHESTER BI-PHASE LEVEL II

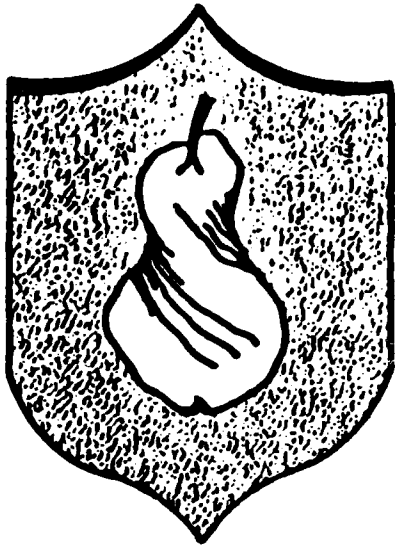


COMMAND AND STATUS SYNC

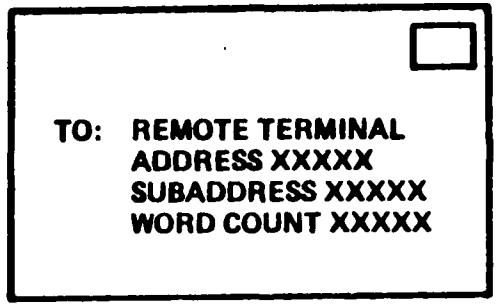


DATA SYNC

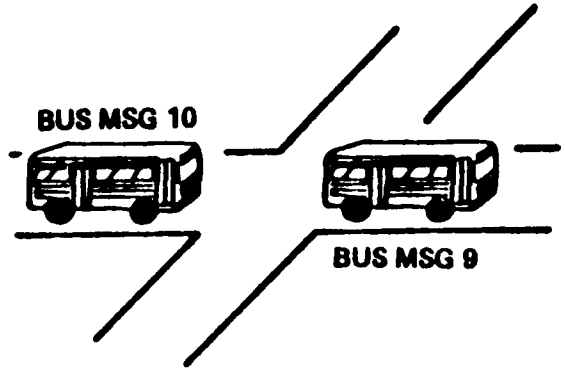
Message Integrity



TWISTED PAIR SHIELDED

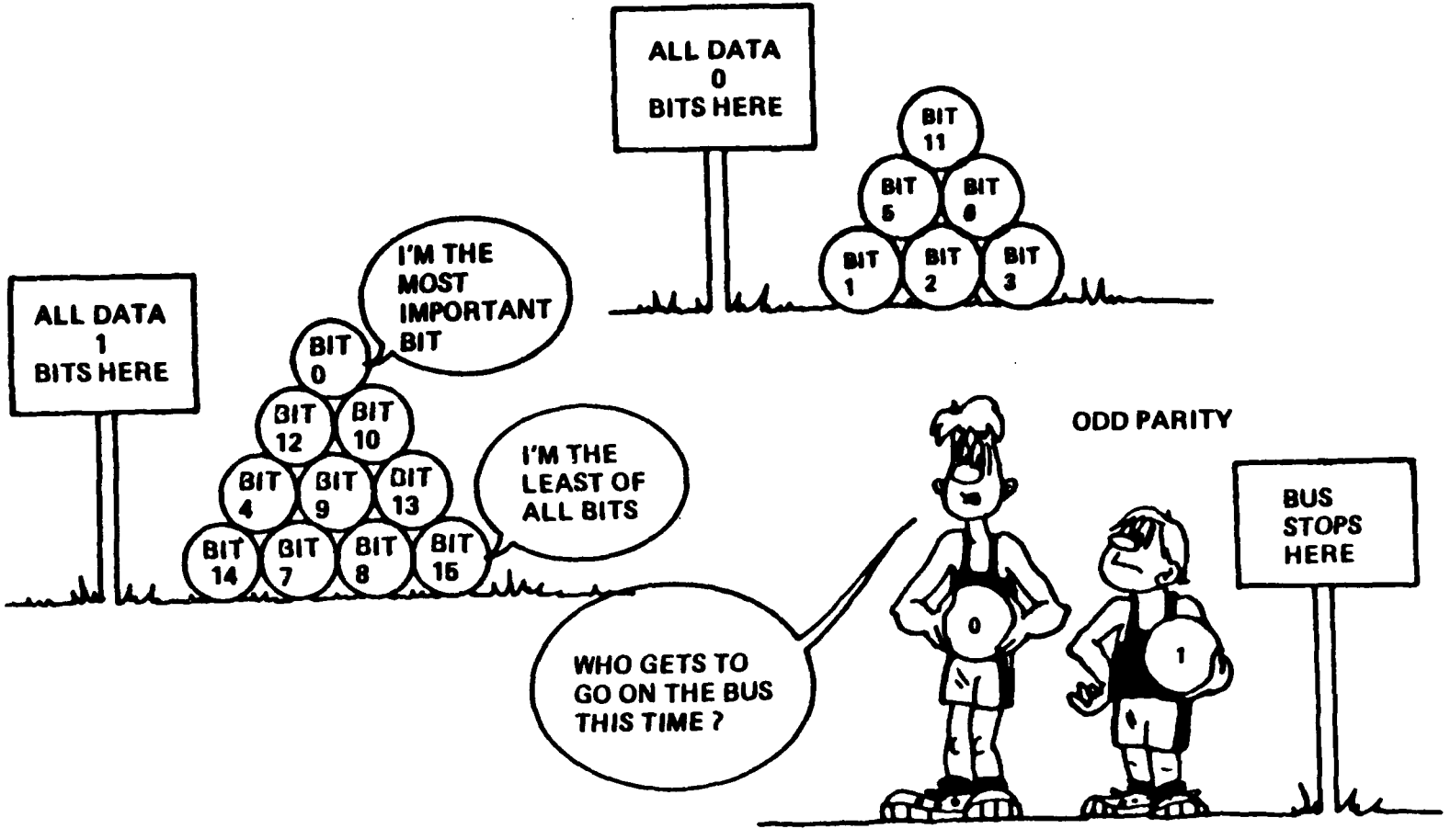


ADDRESS
SUBADDRESS
WORD COUNT

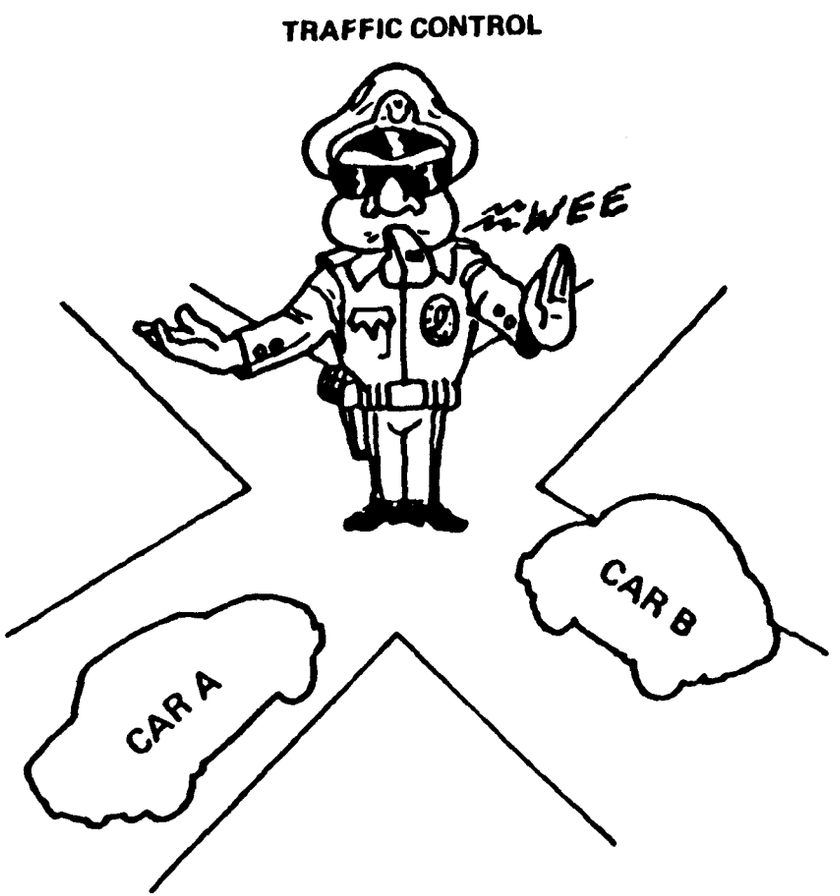


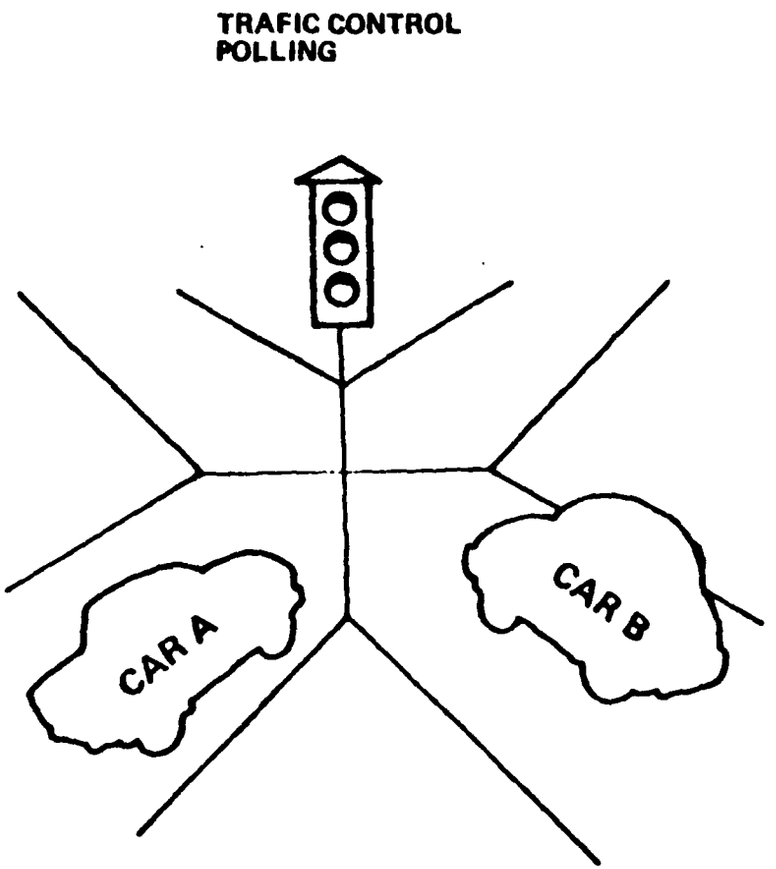
BUS MESSAGES
GAP TIMES
ISOLATION COUPLERS

Everyone Needs . . . Parity Today

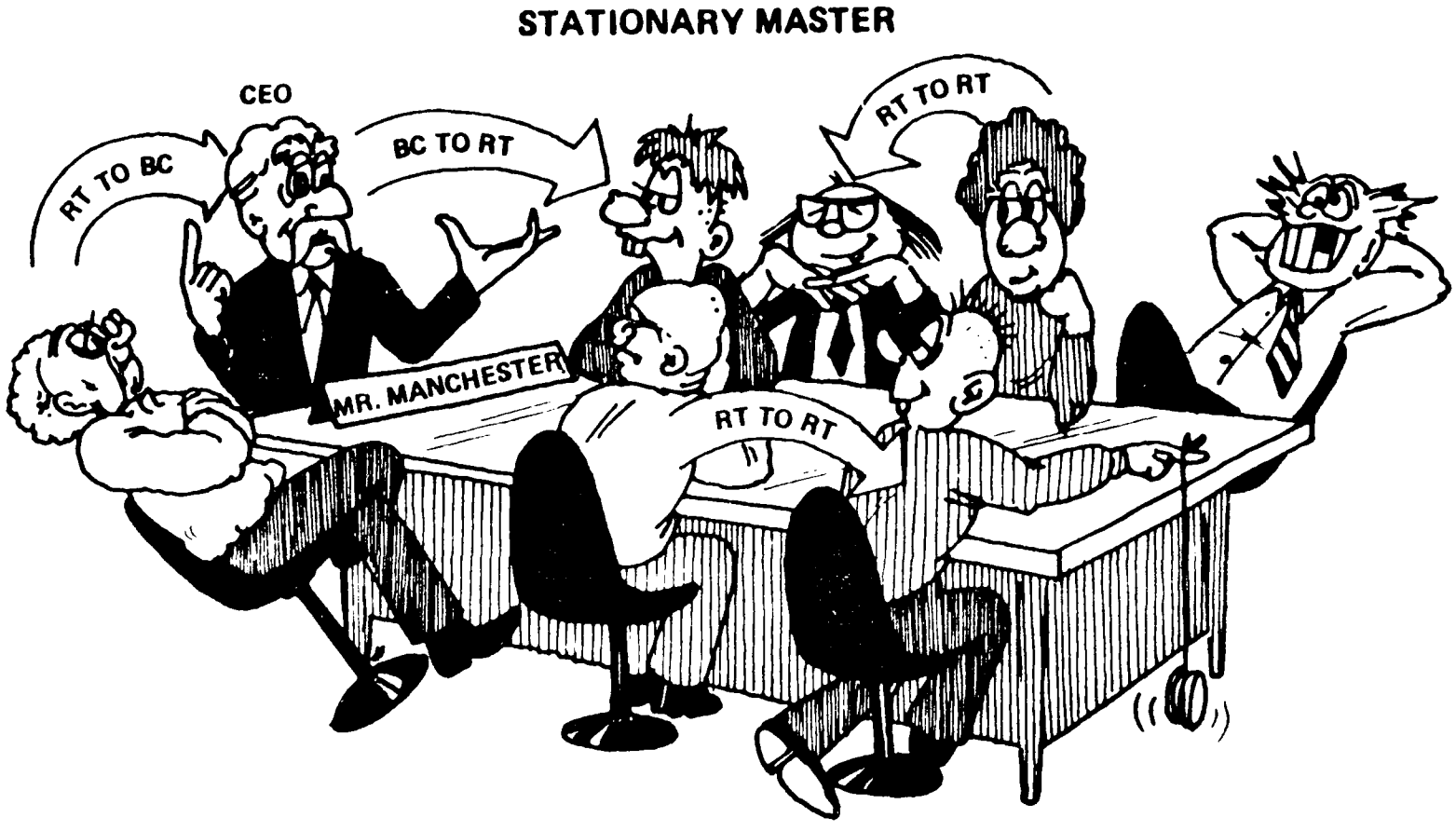


Stationary Master / Non-Stationary Master



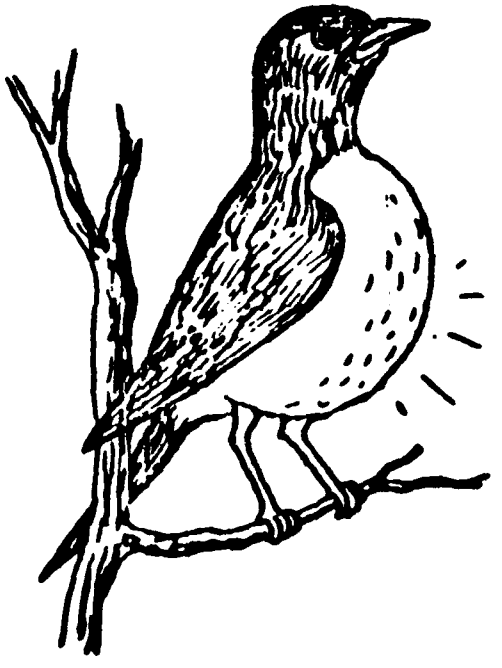


Bus Controller Approach

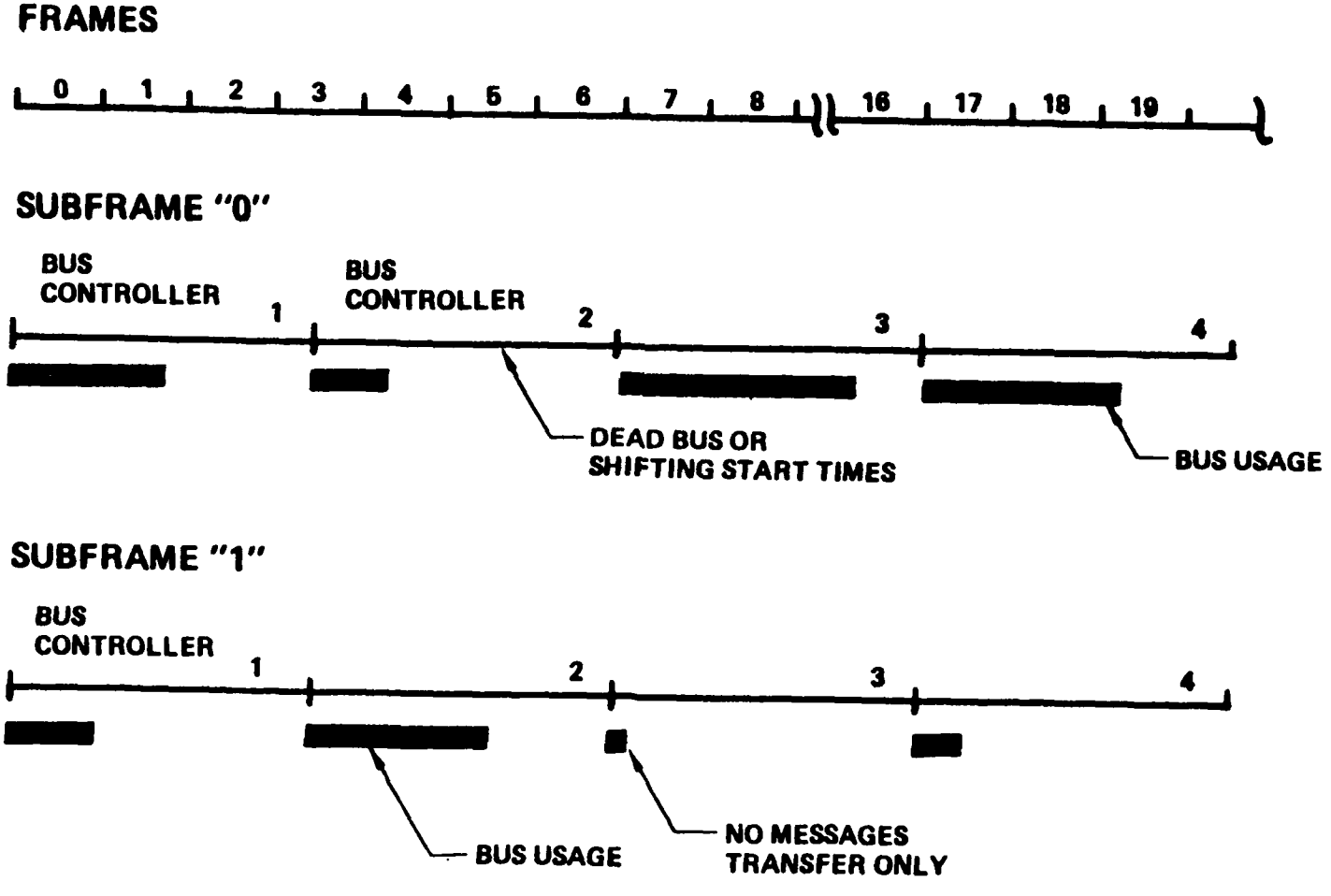


Bus Controller Approach

ROUND ROBIN **VS** **POLLING**



Bus Traffic Verses Bus Controller



Assigned Mode Codes

TRANSMIT RECEIVE BIT	MODE CODE	FUNCTION	ASSOCIATED DATA WORD	BROADCAST COMMAND ALLOWED
1	00000	DYNAMIC BUS CONTROL	NO	NO
1	00001	SYNCHRONIZE	NO	YES
1	00010	TRANSMIT STATUS WORD	NO	NO
1	00011	INITIATE SELF-TEST	NO	YES
1	00100	TRANSMITTER SHUTDOWN	NO	YES
1	00101	OVERRIDE TRANSMITTER SHUTDOWN	NO	YES
1	00110	INHIBIT TERMINAL FLAG BIT	NO	YES
1	00111	OVERRIDE INHIBIT TERMINAL FLAG BIT	NO	YES
1	01000	RESET REMOTE TERMINAL	NO	YES
1	01001	RESERVED	NO	TBD
↓	↓	↓	↓	↓
1	01111	RESERVED	NO	TBD
1	10000	TRANSMIT VECTOR WORD	YES	NO
0	10001	SYNCHRONIZE	YES	YES
1	10010	TRANSMIT LAST COMMAND	YES	NO
1	10011	TRANSMIT BIT WORD	YES	NO
0	10100	SELECTED TRANSMITTER SHUTDOWN	YES	YES
0	10101	OVERRIDE SELECTED TRANSMITTER SHUTDOWN	YES	YES
1 OR 0	10110	RESERVED	YES	TBD
↓	↓	↓	↓	↓
1 OR 0	11111	RESERVED	YES	TBD

NOTE: TBD -- TO BE DETERMINED.

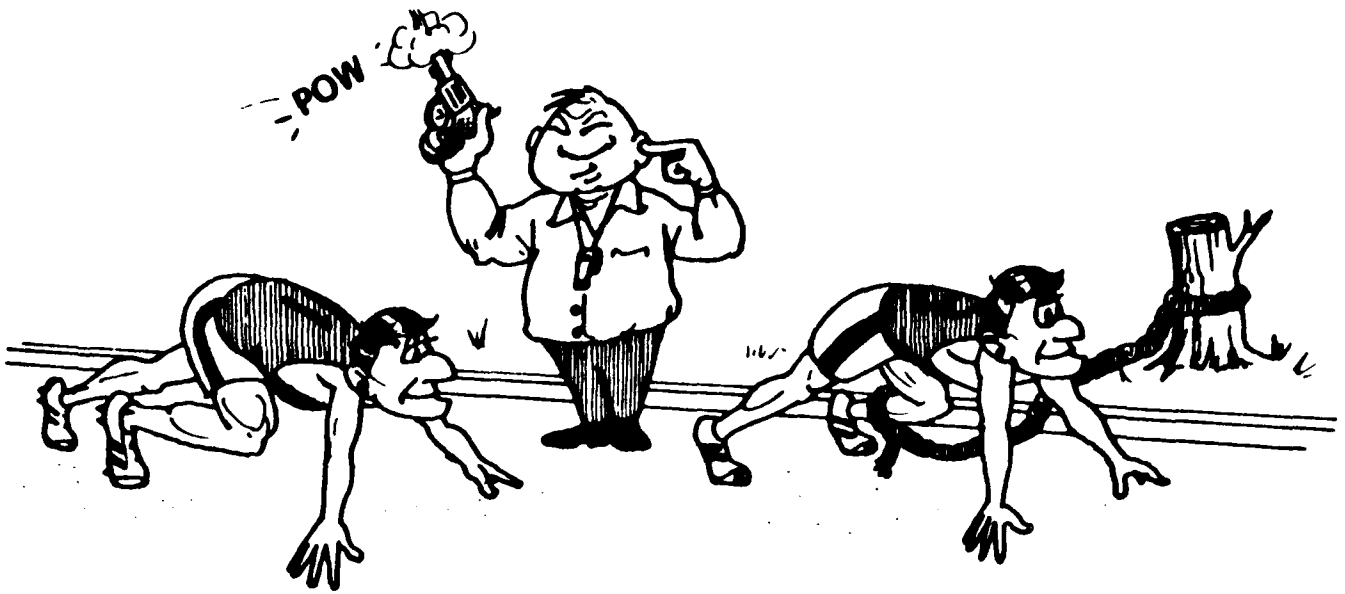
Mode Code Usage

	1553A	1553B	A-10	F-16	F-18	B-52	NOTICE 1 1553B
MODE COMMANDS							
WITHOUT DATA	N						
DYNAMIC BUS CONTROL		0			0		
SYNCHRONIZE	O	1		1			1
TRANSMIT STATUS		2		2-31		1	2
INITIATE SELF TEST	N	3				2	3
TRANSMITTER SHUTDOWN		4				3	4
OVERRIDE SHUTDOWN	E	5				4	5
INHIBIT T/F		6					
OVERRIDE INHIBIT T/F		7					
RESET RT		8					8
ONE DATA WORD FROM RT							
TRANSMIT VECTOR WORD		16					16
TRANSMIT LAST COMMAND		18					18
TRANSMIT BIT WORD		19					19
ONE DATA WORD TO RT							
SYNCHRONIZE		17					17
SELECTED SHUTDOWN		20					
SELECTED OVERRIDE		21					
ILLEGAL	N/A	9-15 22-31	ALL	NONE	1-31	0 5-31	0-17 9-15 20-31

SUBADDRESS (00000) FOR MODE DATA – ALL EXCEPT F-16

SUBADDRESS (11111) FOR MODE DATA – F-16, 1553B, NOTICE 1

Status Word Transmission



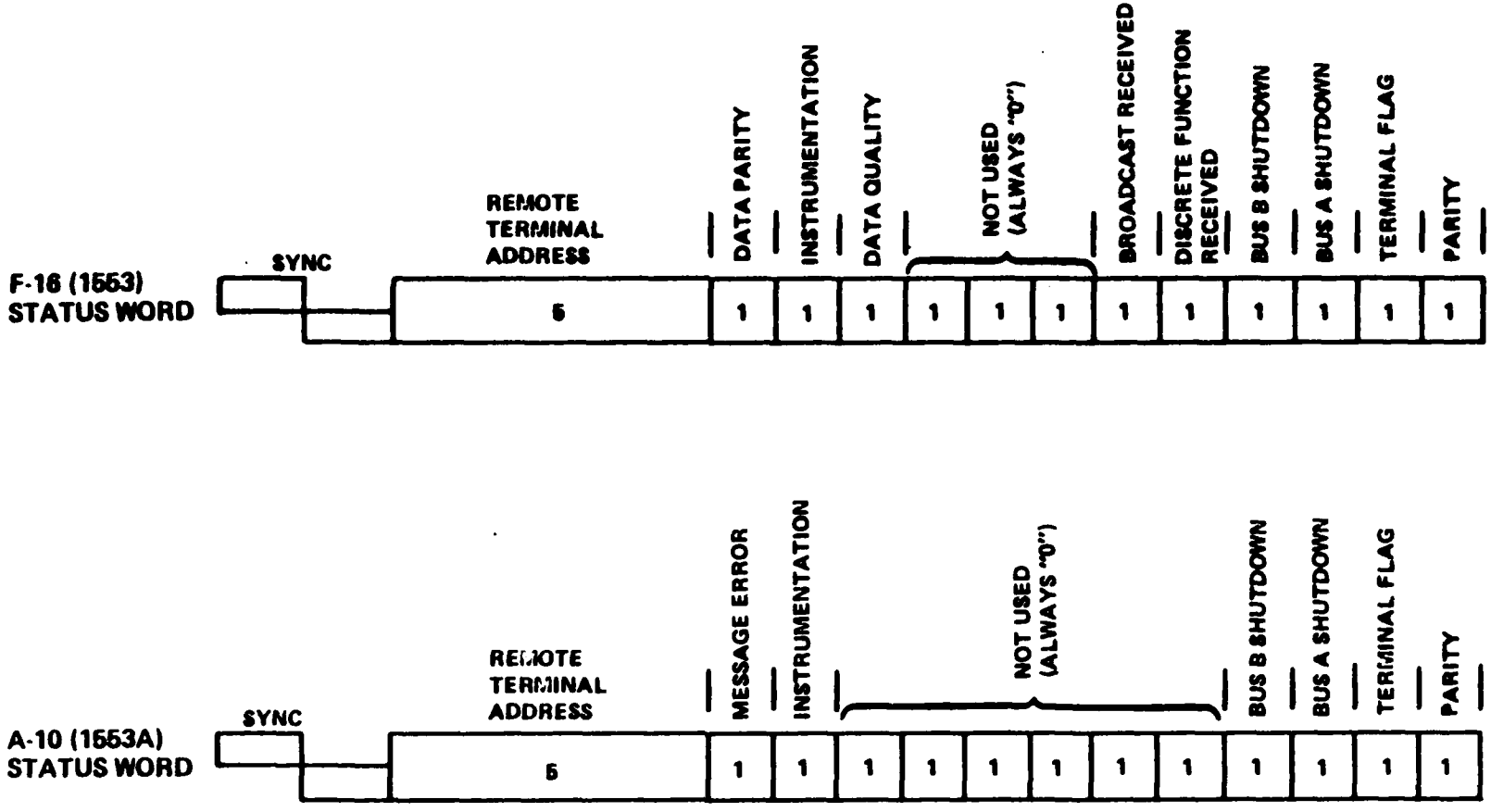
TRANSMIT STATUS

- NO ERRORS IN MESSAGE
- F-16, F-18, & A-10
  PARITY ERROR
  INVALID SYNC CODE
  BIT COUNT

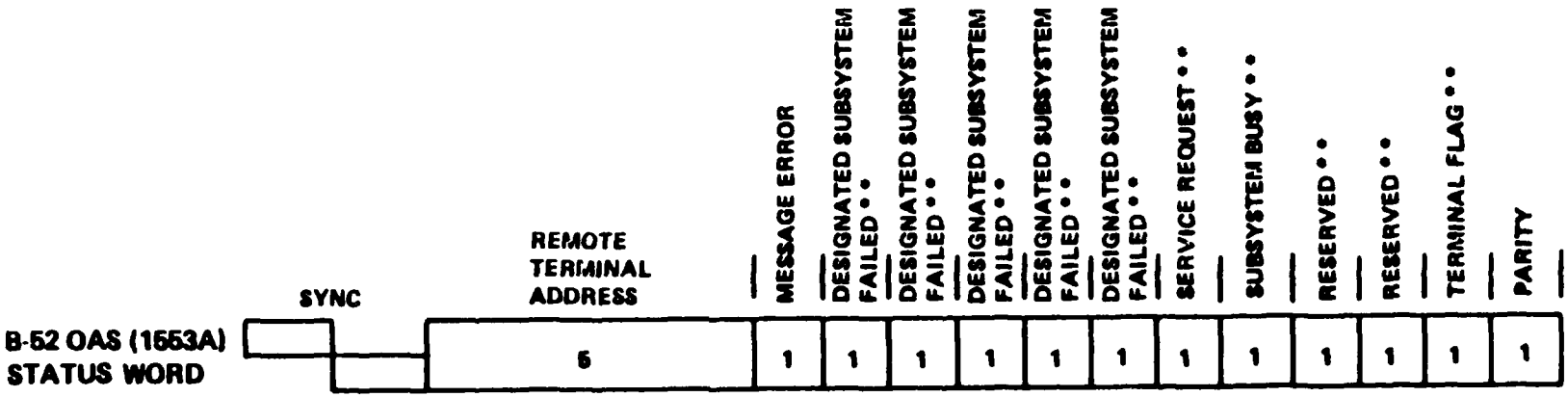
SUPPRESS STATUS

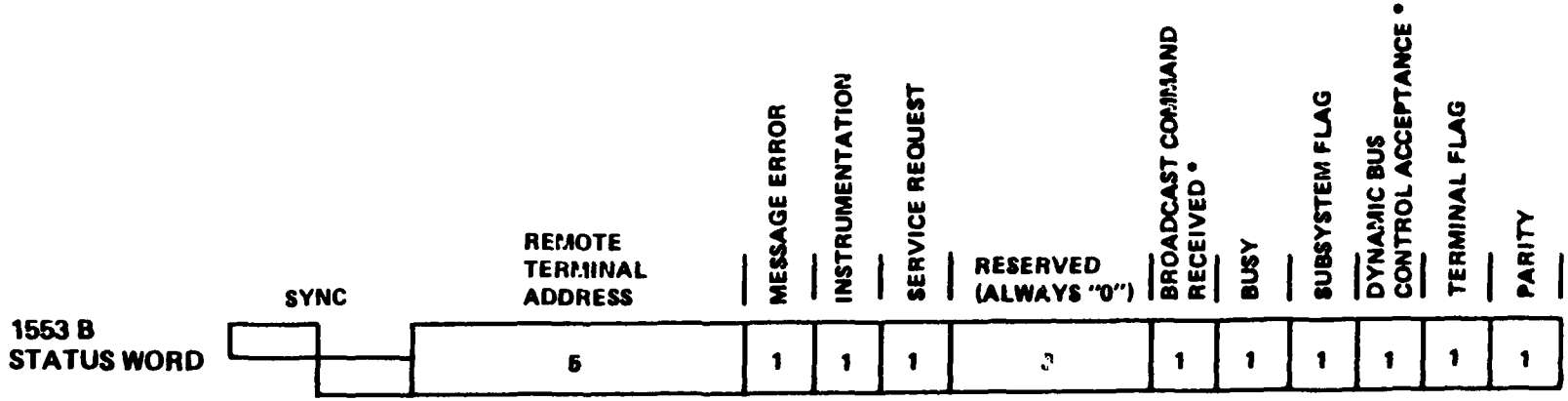
- BROADCAST MESSAGE
- NO DATA RECEIVED
- WORD ERROR
- B-52, 1553B, NOTICE I
  FOR MESSAGE ERROR

Status Word Definition



Status Word Definition

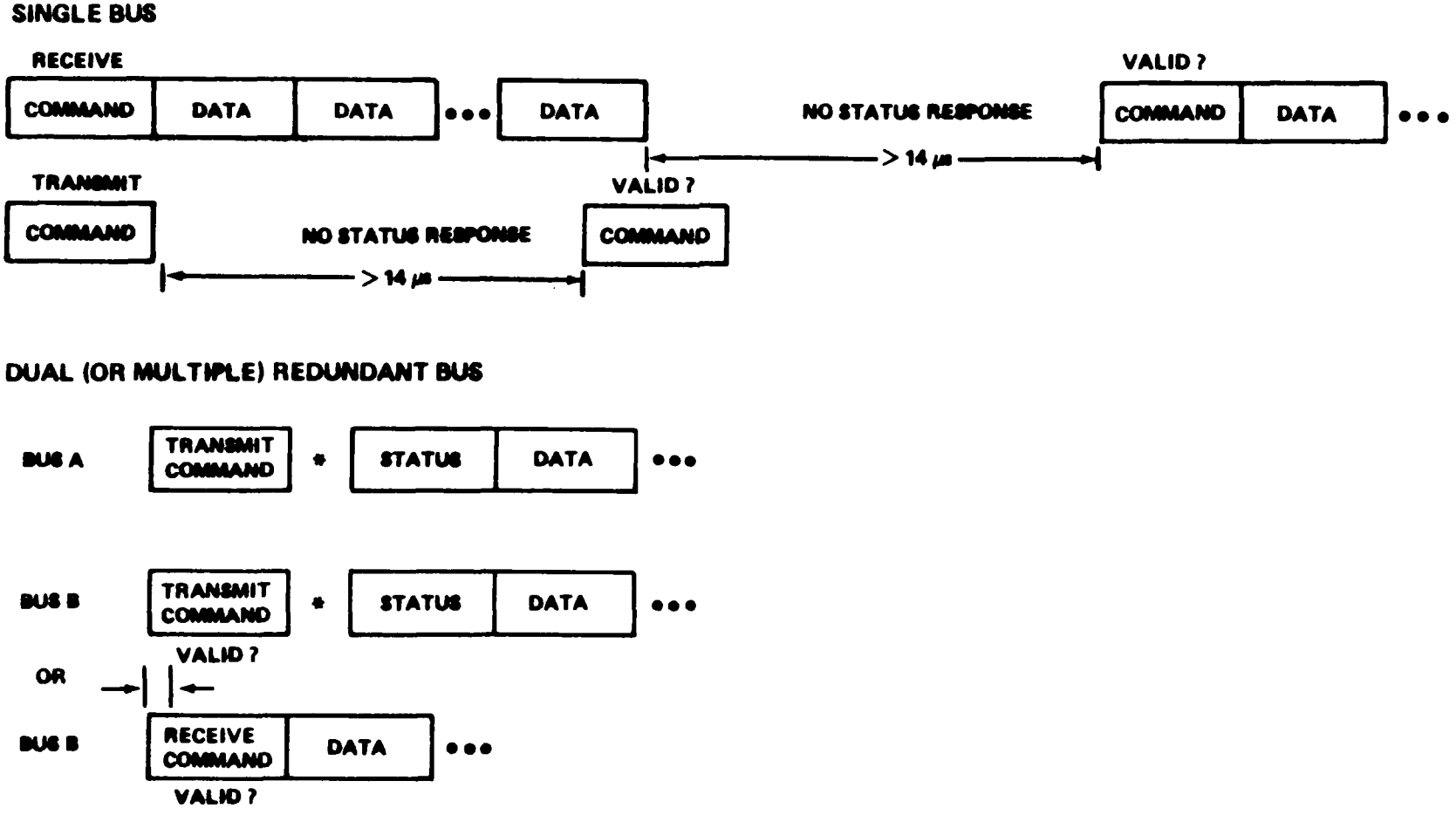




* SET TO ZERO FOR NOTICE 1

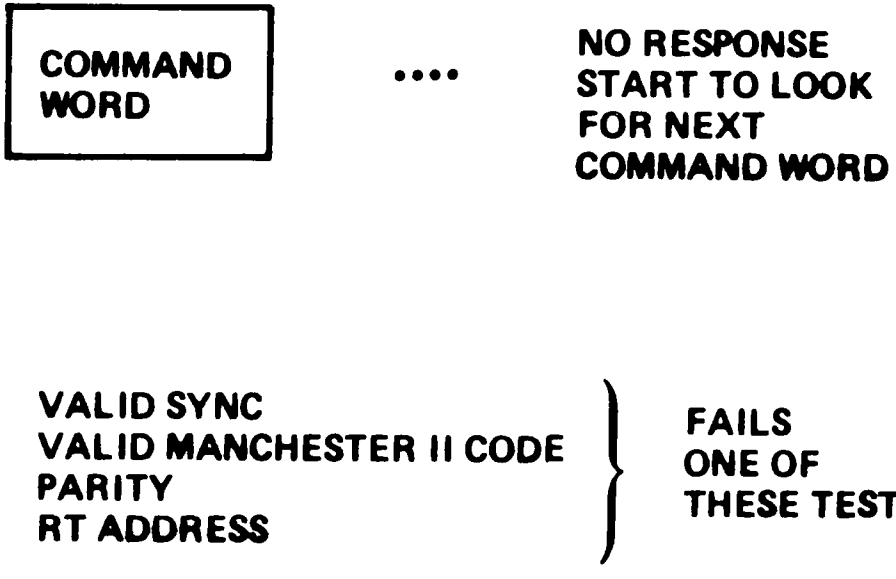
** F-18 USES FIELD FOR SERVICE REQUEST DATA

Superceding Valid Command



Invalid Command

A RT SHALL NOT RESPOND TO A COMMAND WORD WHICH FAILS TO MEET THE CRITERIA SPECIFIED FOR VALID COMMAND WORDS



Illegal Command

A VALID COMMAND WHERE

- SUBADDRESS/MODE FIELD
- DATA WORD COUNT/MODE CODE FIELD
- TRANSMIT/RECEIVE BIT

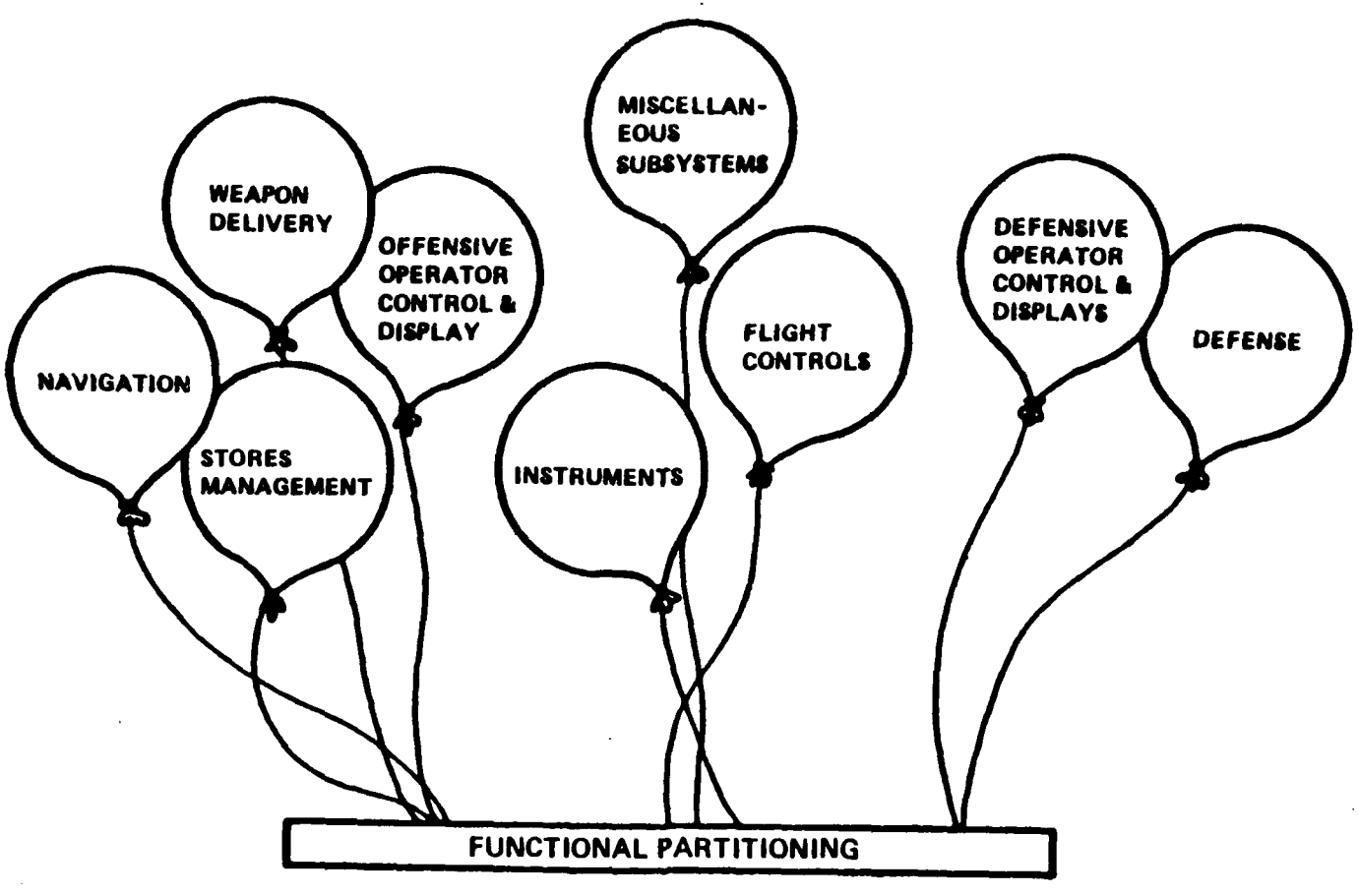
INDICATES A CONDITION WHICH HAS NOT BEEN IMPLEMENTED

1. BUS CONTROLLER SHALL NOT SEND OUT ILLEGAL COMMANDS
2. RT DESIGNERS OPTION:
   - MONITORING FOR ILLEGAL COMMANDS

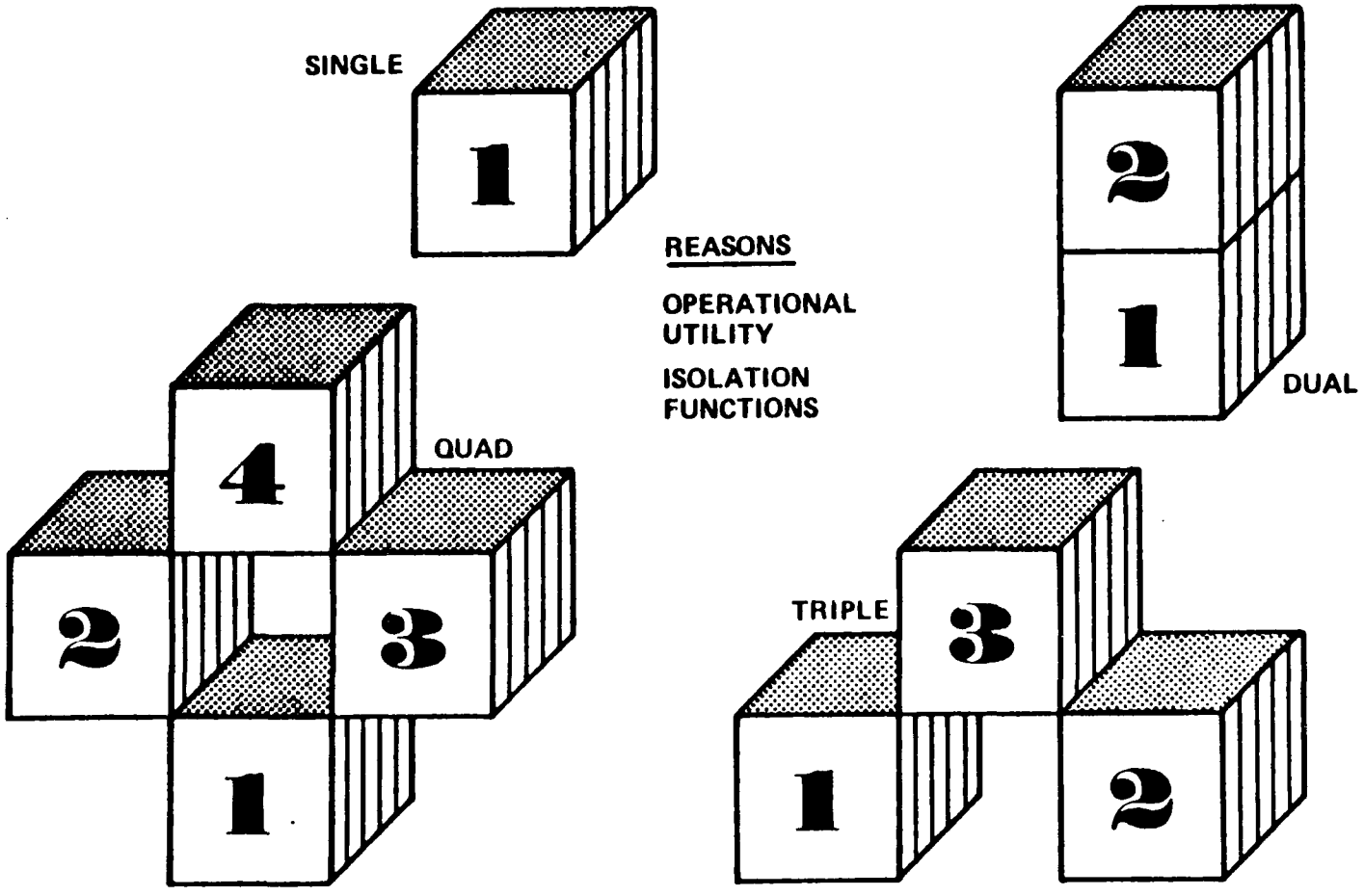
"IF" DESIGNED WITH OPTION RESPOND WITH STATUS WORD MESSAGE ERROR SET AND DO NOT USE THE DATA

System Design

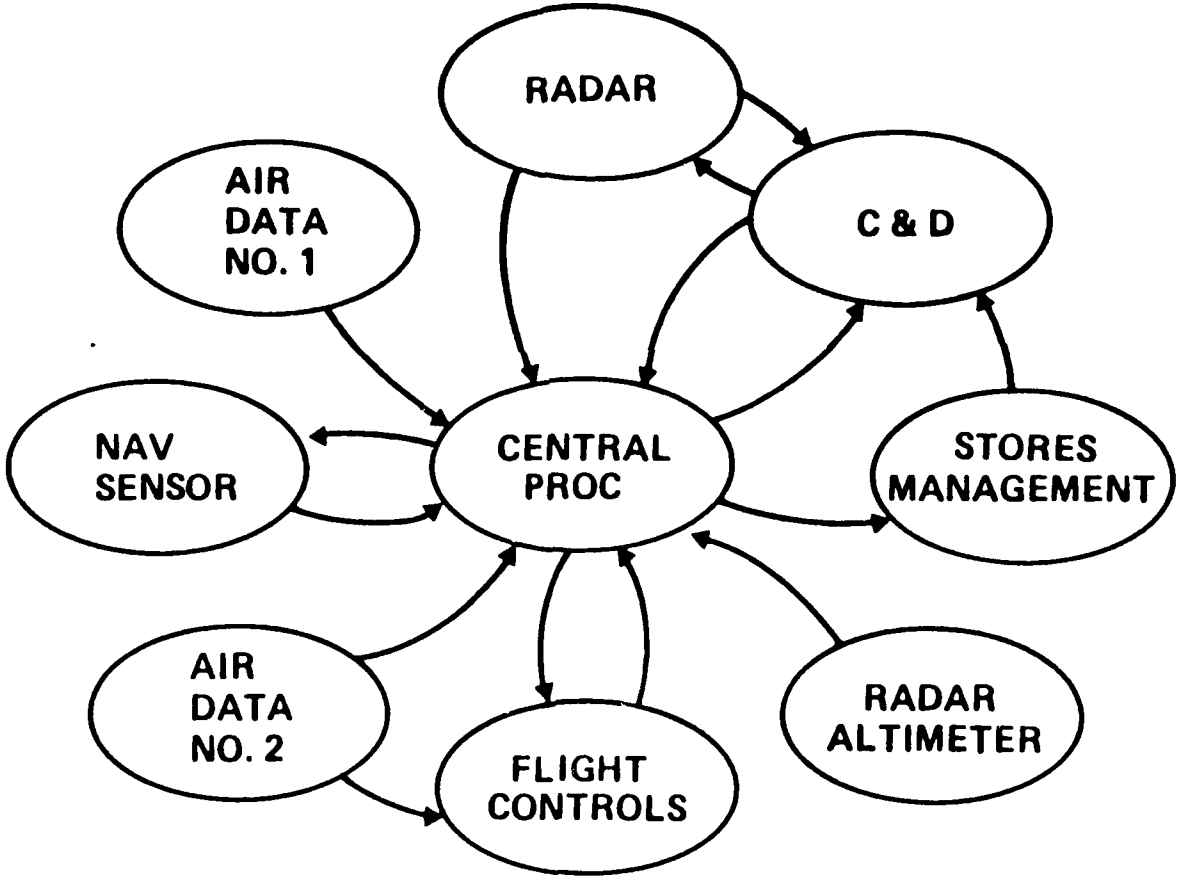
Functional Partitioning



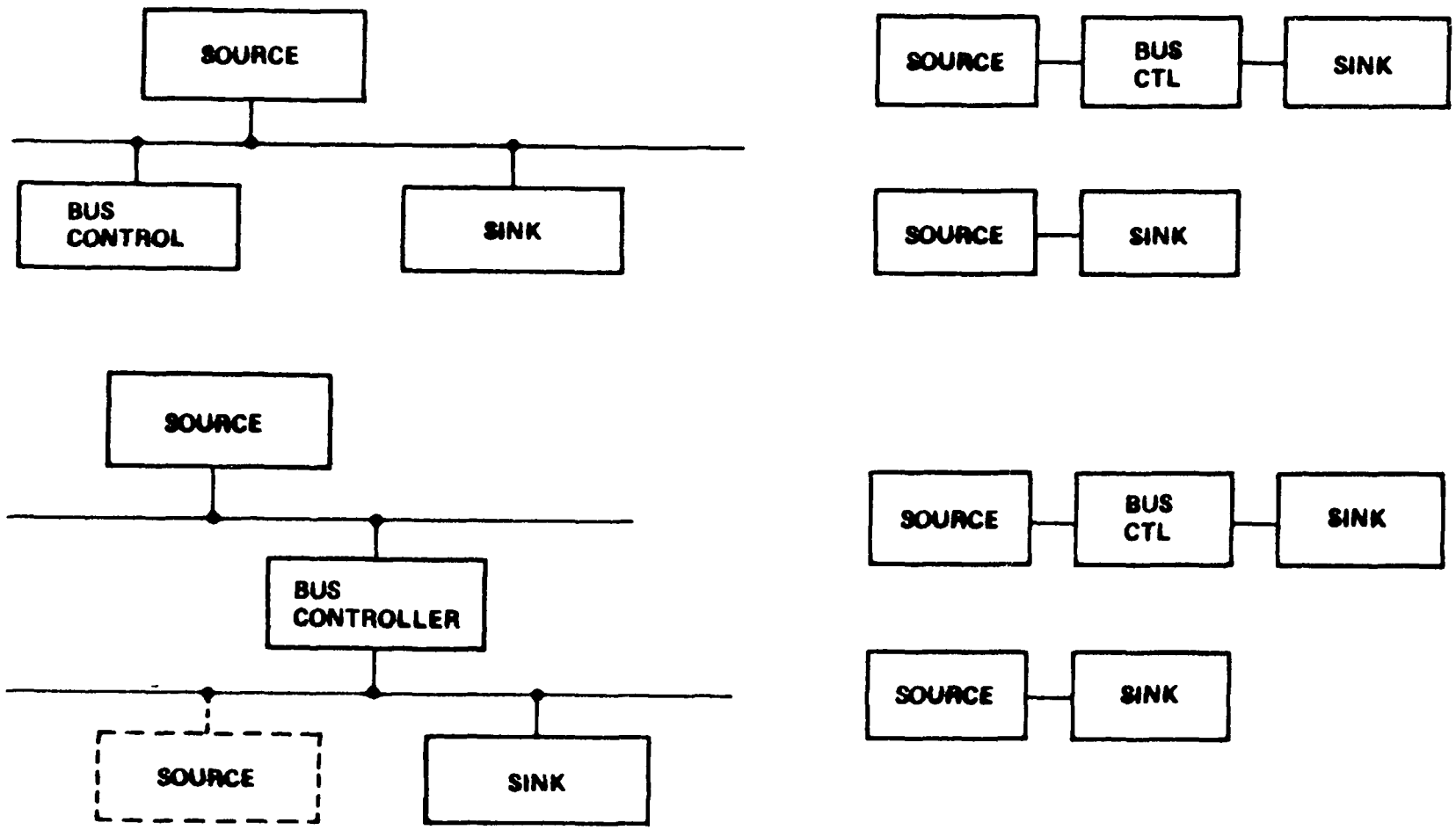
Redundancy Levels and Isolation



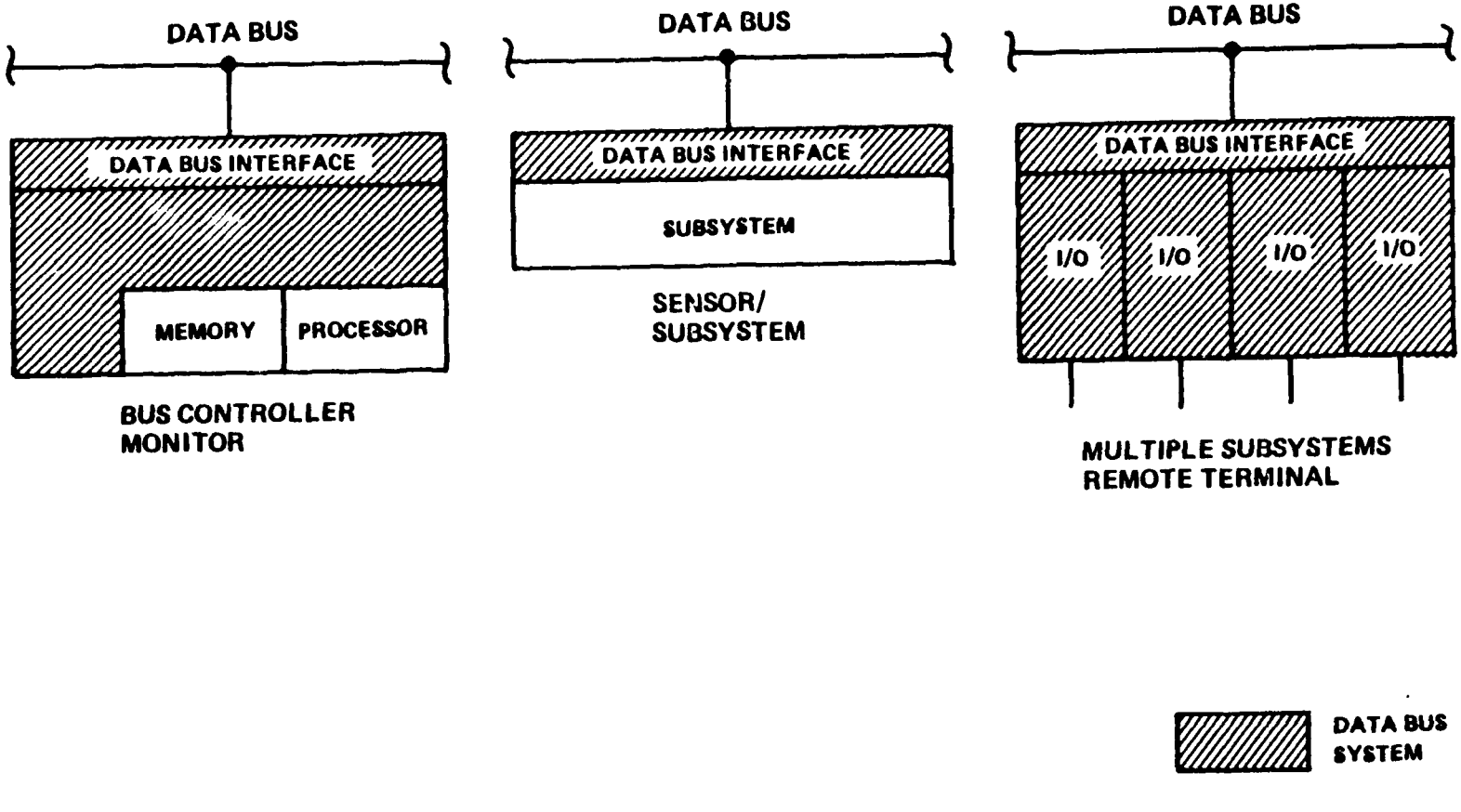
Functional Data Flow



Data Bus Traffic Flow



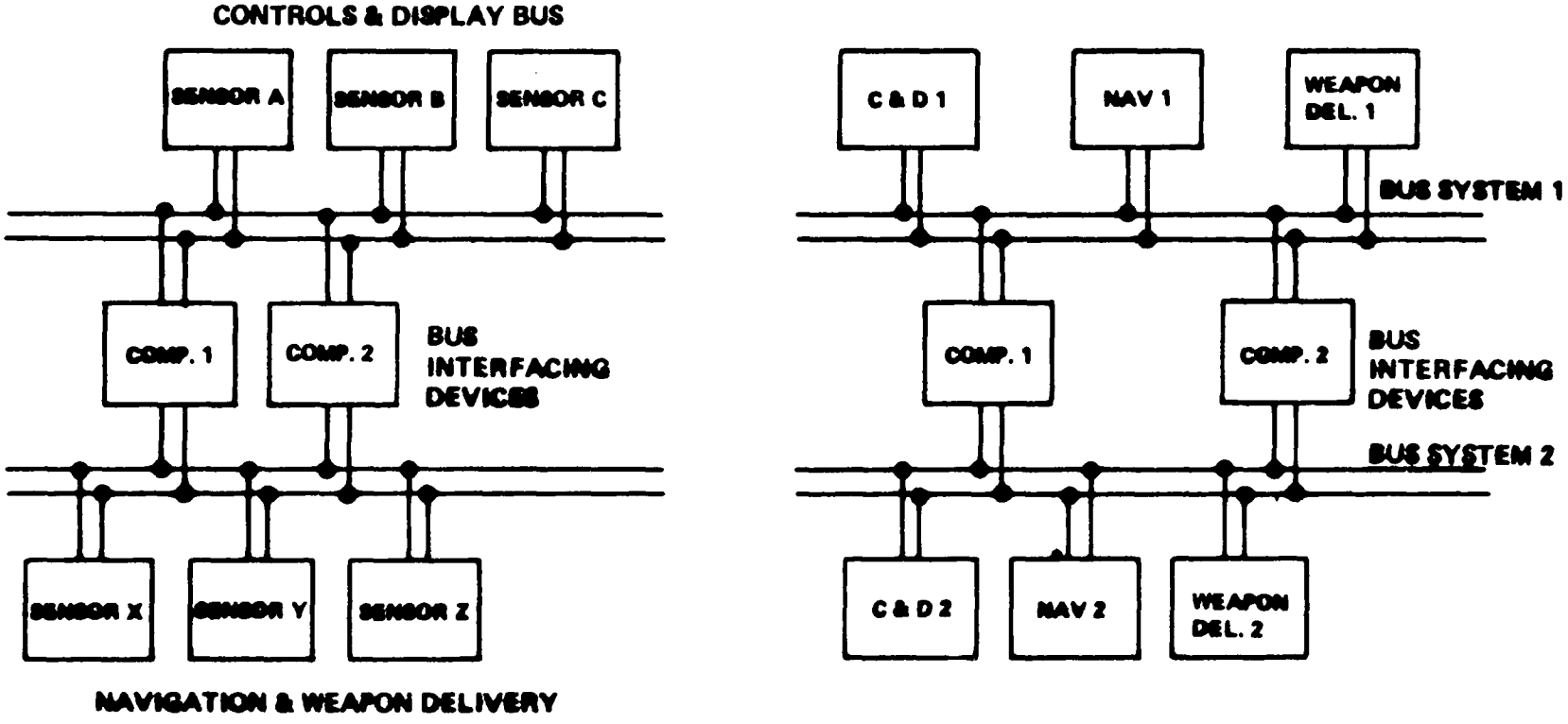
Key Mil-Std-1553 Elements



Bus Element Capabilities

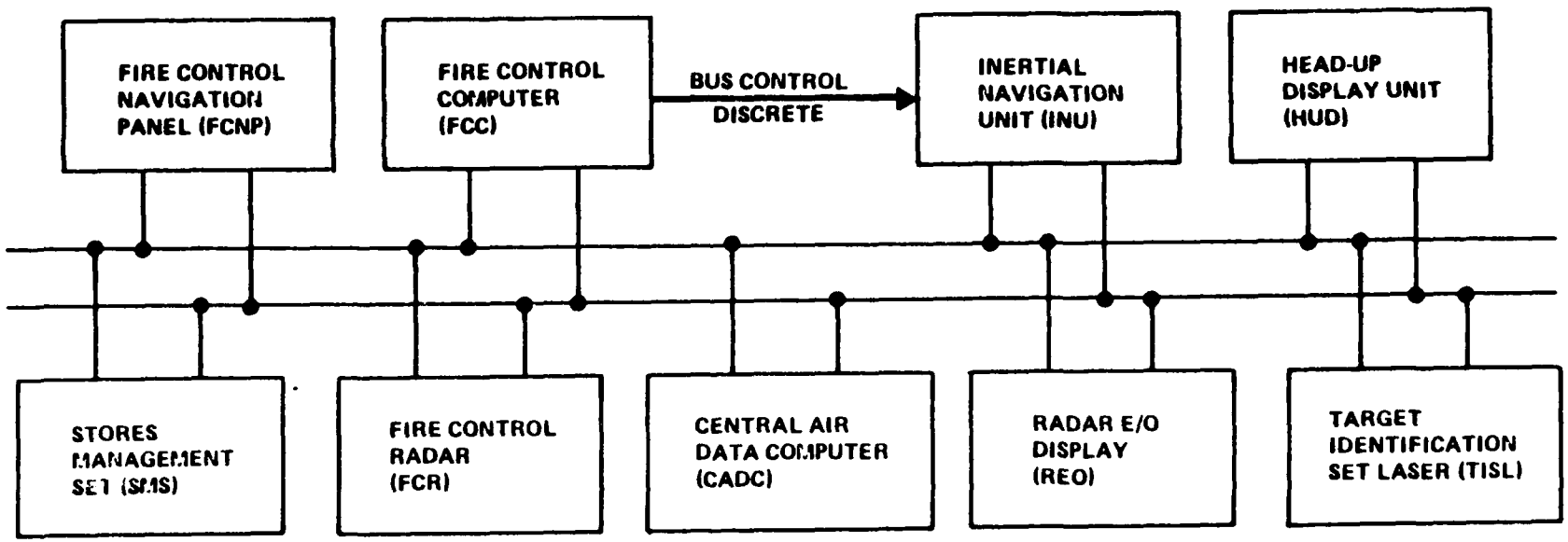
CAPABILITY	BUS CONTROLLER	MINIMUM STANDALONE RT (DUAL BUS)	STANDALONE RT (DUAL BUS)	STANDALONE RT (MULTIPLE BUS)	MINIMUM EMBEDDED (DUAL BUS)	EMBEDDED TERMINAL (DUAL BUS)	EMBEDDED TERMINAL (MULTIPLE BUS)	INTELLIGENT DEVICE:RT OR EMBEDDED (DUAL BUS)	INTELLIGENT DEVICE: RT OR EMBEDDED (MULTIPLE BUS)
1. INFORMATION TRANSFER FORMATS									
A. CONTROLLER TO REMOTE TERMINAL	X	X	X	X	X	X	X	X	X
B. REMOTE TERMINAL TO CONTROLLER	X	X	X	X	X	X	X	X	X
C. REMOTE TERMINAL TO REMOTE TERMINAL	X	X	X	X	X	X	X	X	X
D. MODE COMMAND WITHOUT DATA WORD	X		X	X		X	X	X	X
E. MODE COMMAND WITH DATA WORD (TRANSMIT)	X		X	X		X	X	X	X
F. MODE COMMAND WITH DATA WORD (RECEIVE)	X			X			X	X	X
2. BROADCAST INFORMATION TRANSFER FORMATS									
A. CONTROLLER TO RT(S) TRANSFER	X					X	X	X	X
B. RT TO RT(S) TRANSFER	X					X	X	X	X
C. MODE COMMAND WITHOUT DATA WORD	X		X	X		X	X	X	X
D. MODE COMMAND WITH DATA WORD	X		X	X			X	X	X
3. MODE CODES									
A. DYNAMIC BUS CONTROL	X								
B. SYNCHRONIZE	X		X	X					
C. TRANSMIT STATUS WORD	X	X	X	X	X	X	X	X	X
D. INITIATE SELF-TEST	X		X	X					
E. TRANSMITTER SHUTDOWN	X		X			X		X	
F. OVERRIDE TRANSMITTER SHUTDOWN	X		X			X		X	
G. INHIBIT TERMINAL FLAG BIT	X		X	X				X	X
H. OVERRIDE INHIBIT TERMINAL FLAG BIT	X		X	X				X	X
I. RESET REMOTE TERMINAL	X		X	X		X	X		X
J. TRANSMIT VECTOR WORD	X		X	X			X	X	X
K. SYNCHRONIZE	X							X	X
L. TRANSMIT LAST COMMAND	X		X	X		X	X	X	X
M. TRANSMIT BIT WORD	X		X	X			X		X
N. SELECTED TRANSMITTER SHUTDOWN	X			X					X
O. OVERRIDE SELECTED TRANSMITTER SHUTDOWN	X			X					X
4. STATUS BIT FIELD									
A. MESSAGE ERROR		X	X	X	X	X	X	X	X
B. INSTRUMENTATION (SET TO ZERO)									
C. SERVICE REQUEST			X	X			X	X	X
D. BROADCAST RECEIVED COMMAND			X	X	X	X	X	X	X
E. BUSY			X	X		X	X	X	X
F. SUBSYSTEM FLAG						X	X		
G. DYNAMIC BUS CONTROL ACCEPTANCE								X	X
H. TERMINAL FLAG			X	X				X	X

Functional Partitioning of Sensors

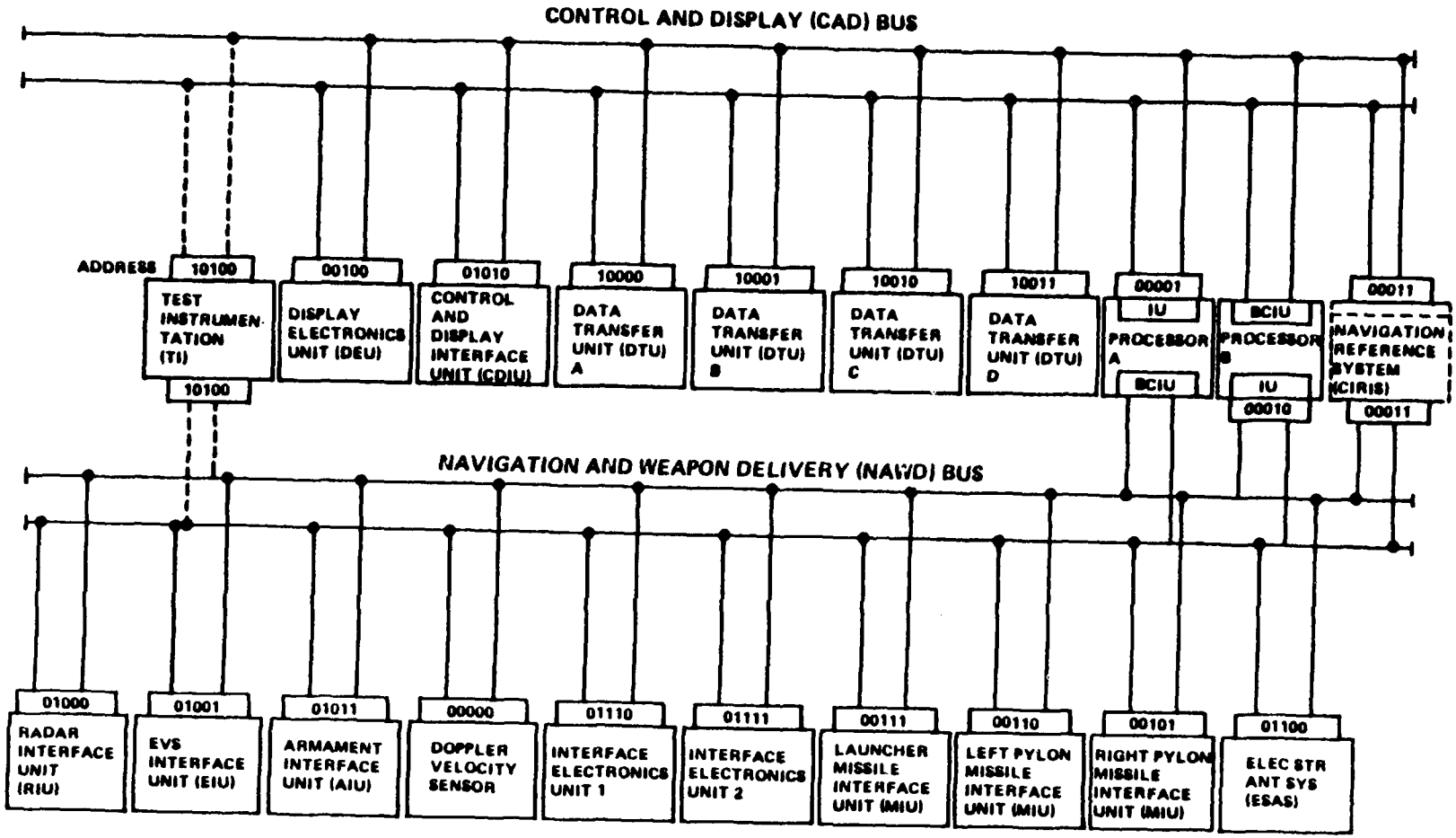


Single Level

F-16 Avionic System Architecture



B-52 OAS Multiplex System Architecture



Impact of Air Force Notice No. 1

- BROADCAST FORMAT INVALID
- LOSS OF CERTAIN MODE CODES
- DUAL STANDBY BUS FOR DUAL REDUNDANCY
- RESPONSE TIME GAP DIFFERENCES NOTED (1553A VERSES 1553B)
- DIFFERENCES IN DATA BUS COUPLERS NOTED (1553A VERSES 1553B)
- CABLE CHARACTERISTICS TIGHTENED (Z_o AND SHIELDING)

AEROSYSTEMS ASSOCIATES

MIL-STD-1553

HARDWARE DESIGN CONSIDERATIONS

D.H. ELLIS

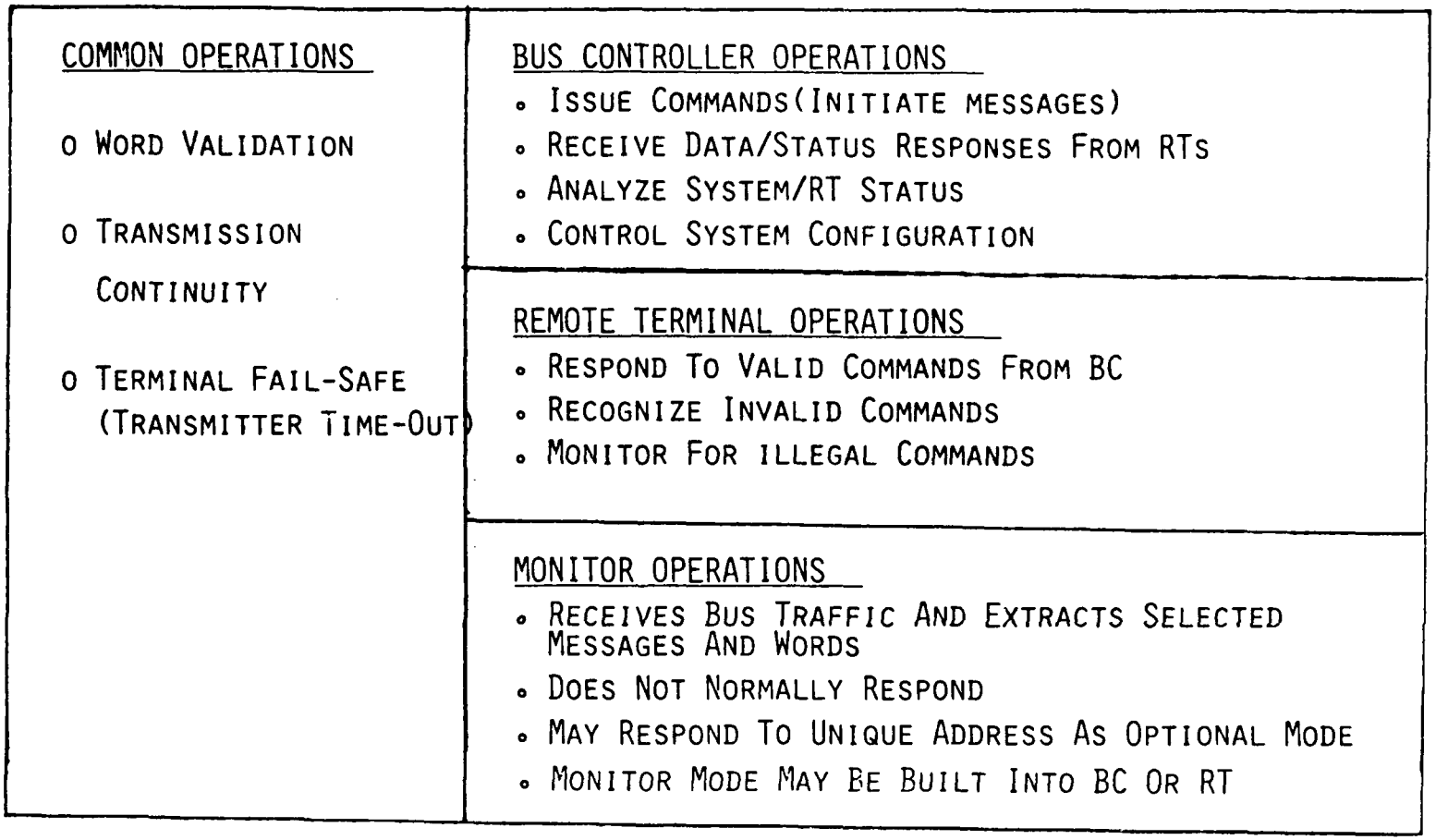
AEROSYSTEMS ASSOCIATES

HARDWARE DESIGN CONSIDERATIONS

- o 1553 DATA BUS DESIGN PHILOSOPHY
- o TERMINAL DEFINITIONS/OPERATIONS
- o GENERALIZED TERMINAL FUNCTIONS
- o BUS NETWORK AND TERMINAL INTERFACE
- o BUS COUPLER DESIGN CONSIDERATIONS
- o TERMINAL FUNCTIONAL DESCRIPTION
- o TERMINAL HARDWARE EXAMPLES
- o LSI/HYBRID DEVICES SUMMARY

SUMMARY MIL-STD-1553 CHARACTERISTICS

TRANSMISSION FORM	-	SERIAL DIGITAL
TRANSMISSION RATE	-	1 MBPS
TRANSMISSION MEDIA	-	TWISTED PAIR SHIELDED CABLE
COUPLING METHOD	-	TRANSFORMER(WITH STUBBING)
MODULATION TYPE	-	BASEBAND PCM
SYNCHRONIZATION	-	BIT ASYNCHRONOUS/WORD & MESSAGE SYNC
BUS CONTROL(PRIMARY)	-	CENTRALIZED(COMMAND-RESPONSE)
(OPTIONAL)	-	BROADCAST, DYNAMIC BUS ALLOCATION
WAVEFORM	-	BIPHASE(MANCHESTER II)
WORD TYPES	-	COMMAND, DATA, STATUS
WORD LENGTH	-	20 BITS(3-BIT SYNC, 1 PARITY)
DATA WORDS/MESSAGE	-	SELECTABLE(0-32)
TERMINAL TYPES	-	BUS CONTROLLER
	-	REMOTE TERMINAL
	-	MONITOR
NUMBER TERMINALS	-	BUS CONTROLLERS(1 ACTIVE + BACKUPS)
	-	REMOTE TERMINALS(1-31)
	-	MONITORS(AS REQUIRED)



TERMINAL OPERATIONS

GENERALIZED TERMINAL FUNCTIONS

WORD PROCESSOR

- o DATA BUS INTERFACE (COUPLING, RECEIVE AND TRANSMIT)
- o BIT/WORD PROCESSOR (ENCODING/DECODING)

MESSAGE PROCESSOR

- o WORD/MESSAGE PROCESSOR
- o SUBSYSTEM INTERFACE

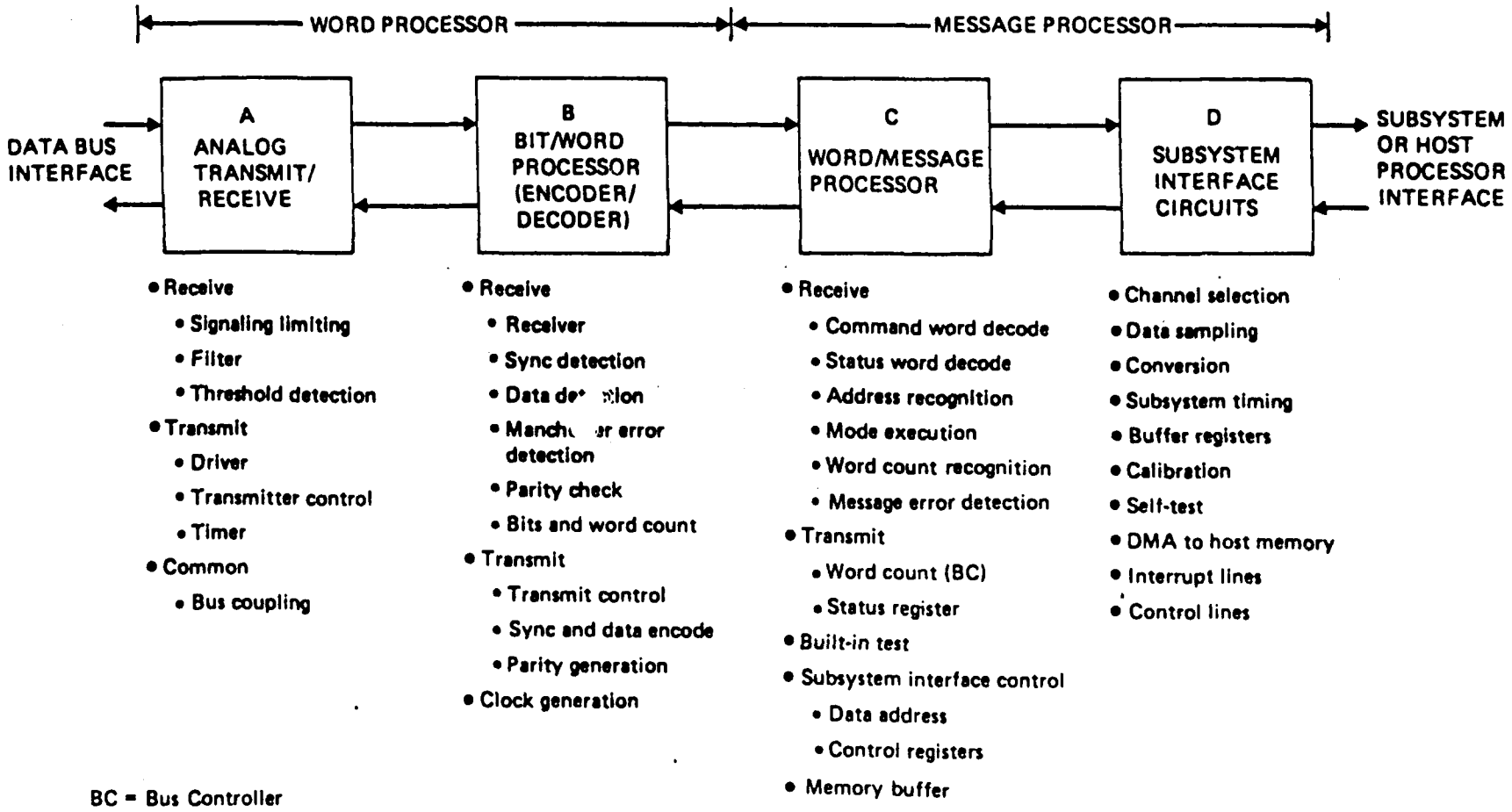


Figure 4.1-1. Generalized Terminal Functional Elements

BUS NETWORK DESIGN CONSIDERATIONS

- TRANSMISSION LINE CHARACTERISTICS
- NETWORK CONFIGURATION
- CABLE COUPLING

TRANSMISSION LINE CHARACTERISTICS

- Cable Type - Twisted Shielded Pair (TSP)
- Capacitance - 30 pfd./ft.,max.
- Characteristic Impedance (Z_0) - 70 to 85 ohms @ 1.0 MH_Z
- Attenuation - 1.5 db/100 Ft. @ 1.0 MH_Z,max.
- Bus Length (main bus) - Not Specified
- Stub Definition/Limits- Short Stub (less than 1 ft.)
  - Long Stub (1 to 20 Ft.)
- Termination - Two Ends Terminated With Resistors Equal To Z_0 ± 2 %
- Shielding - 75% Coverage, min.

NETWORK CONFIGURATION

- o BUS/STUB LENGTH
- o NUMBER OF STUBS
- o LENGTH OF STUBS (APPLICATION OF COUPLERS)
- o LOCATION OF STUBS
- o VERIFICATION OF SIGNAL INTEGRITY

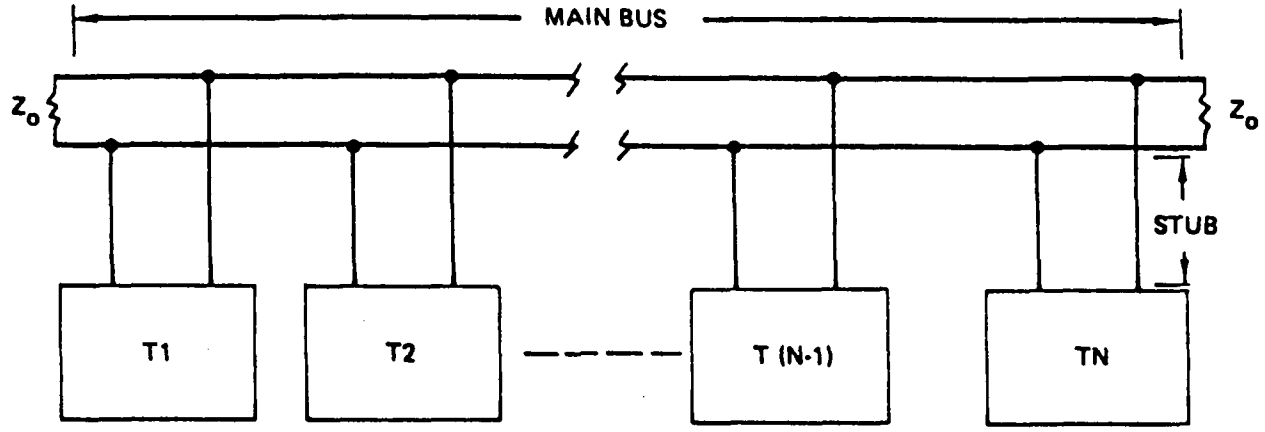


Figure 4.2-1. Bus Network Configuration

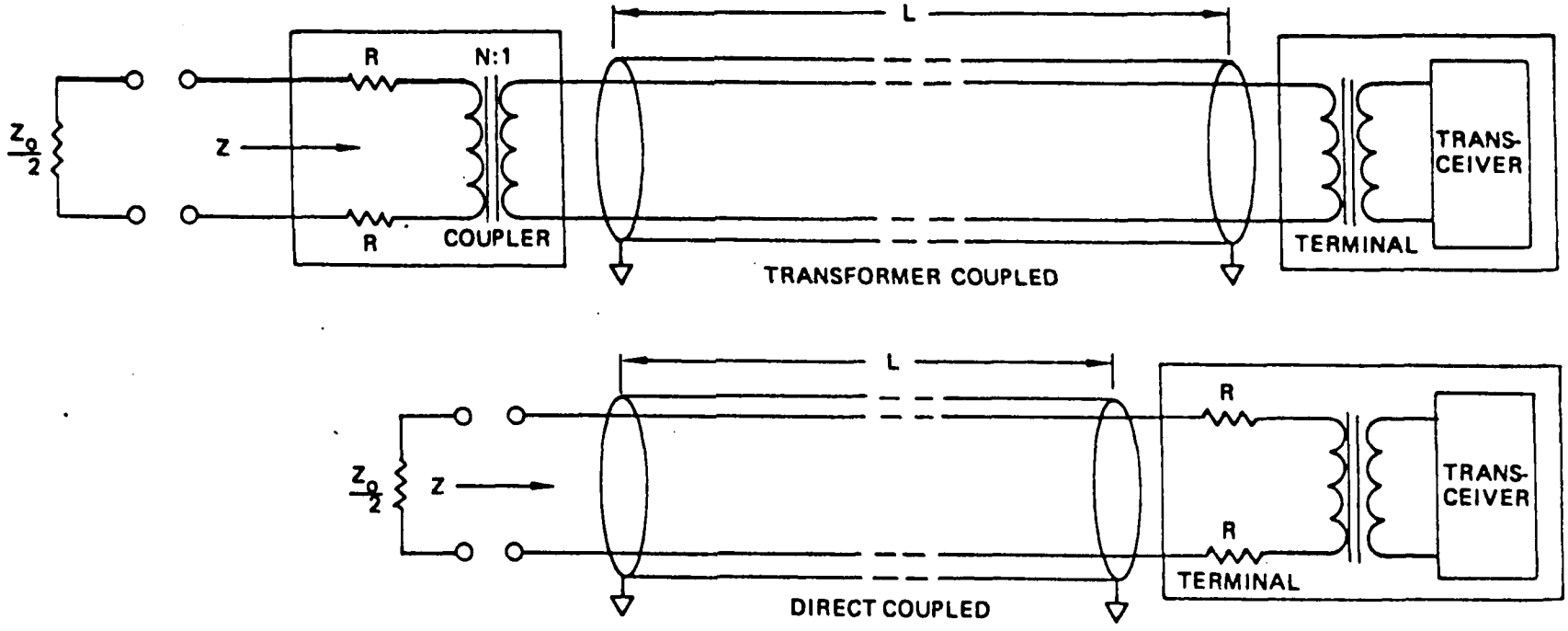
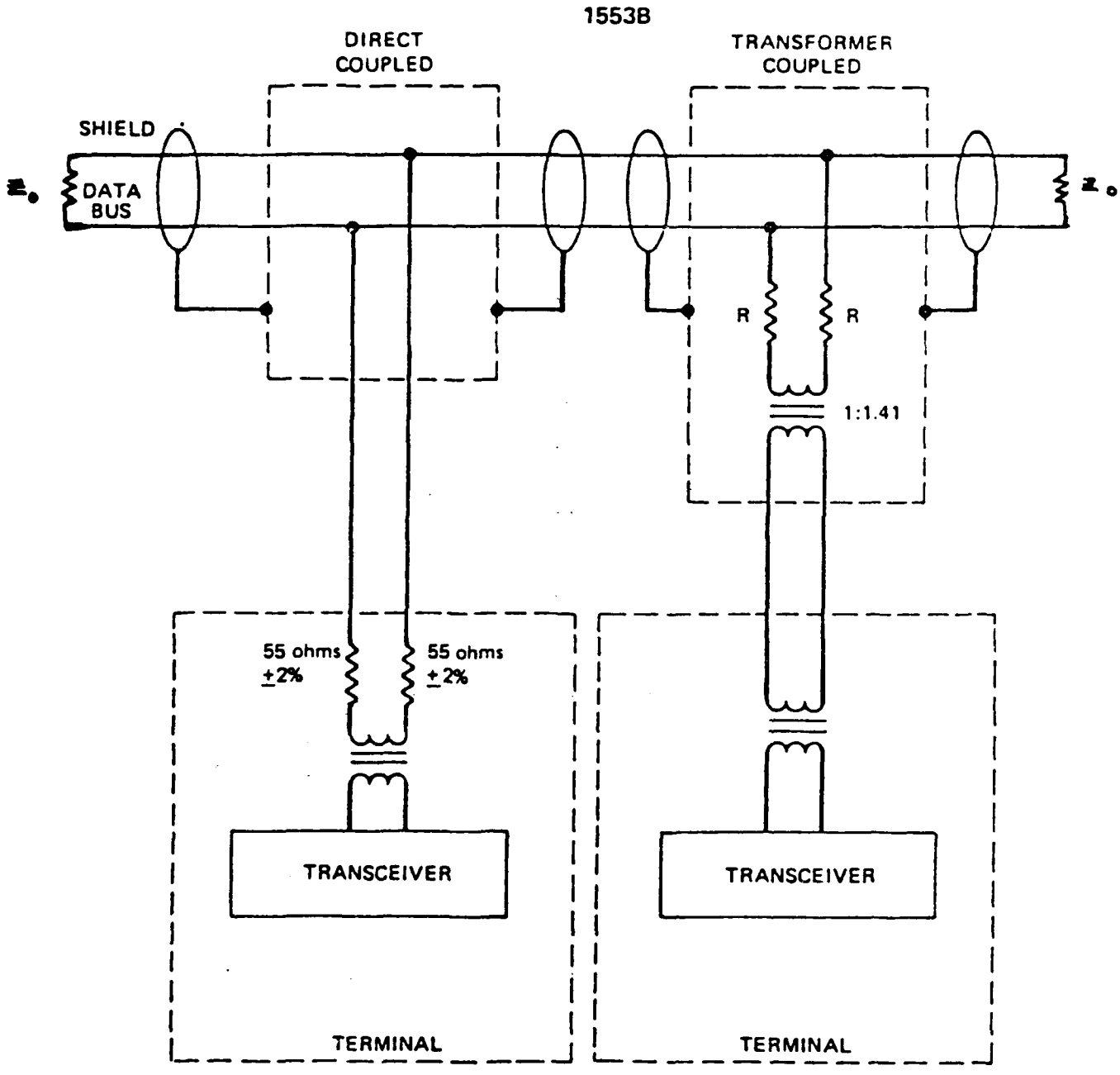


Figure 4.2-2. Transformer-Coupled and Direct-Coupled Stubs

BUS COUPLER CHARACTERISTICS

- o PASSIVE DEVICE FOR HIGH RELIABILITY
- o ISOLATION OF STUB FAULT CONDITIONS
- o REDUCTION OF MAIN BUS LOADING DUE TO STUB
- o COMMON MODE NOISE REJECTION (CMR)
- o TERMINATION OF STUB FOR TERMINAL TRANSMISSION



- Isolation resistors: R = 0.75 Z_o^* ±2%
- Isolation transformer: turns ratio 1:1.41 ±3%
  (1—terminal winding)
  (1.41—bus winding)

Z_{oc} > 3K at 75 kHz to 1 MHz
1V rms sine wave

Droop: < 20%
Overshoot/ringing: < ±1V } at 27 V P-P 250 kHz square wave
CMR: > 45 dB at 1 MHz

*Nominal characteristic impedance of bus cable: Z_o = 70 to 85 at 1 MHz

COUPLING TRANSFORMER DESIGN CONSIDERATIONS

- o TURNS RATIO (STEP-DOWN FROM MAIN BUS) PROVIDES TRANSFORMATION OF STUB IMPEDANCE
- o SELECTED TURNS RATIO TERMINATES STUB FOR TERMINAL TRANSMISSION
- o HIGH OPEN CIRCUIT IMPEDANCE AT LOW FREQUENCY
- o LOW SHUNT CAPACITANCE TO MAINTAIN HIGH INPUT IMPEDANCE AT HIGH FREQUENCIES
- o LIMIT INTERWINDING CAPACITANCE FOR CMR

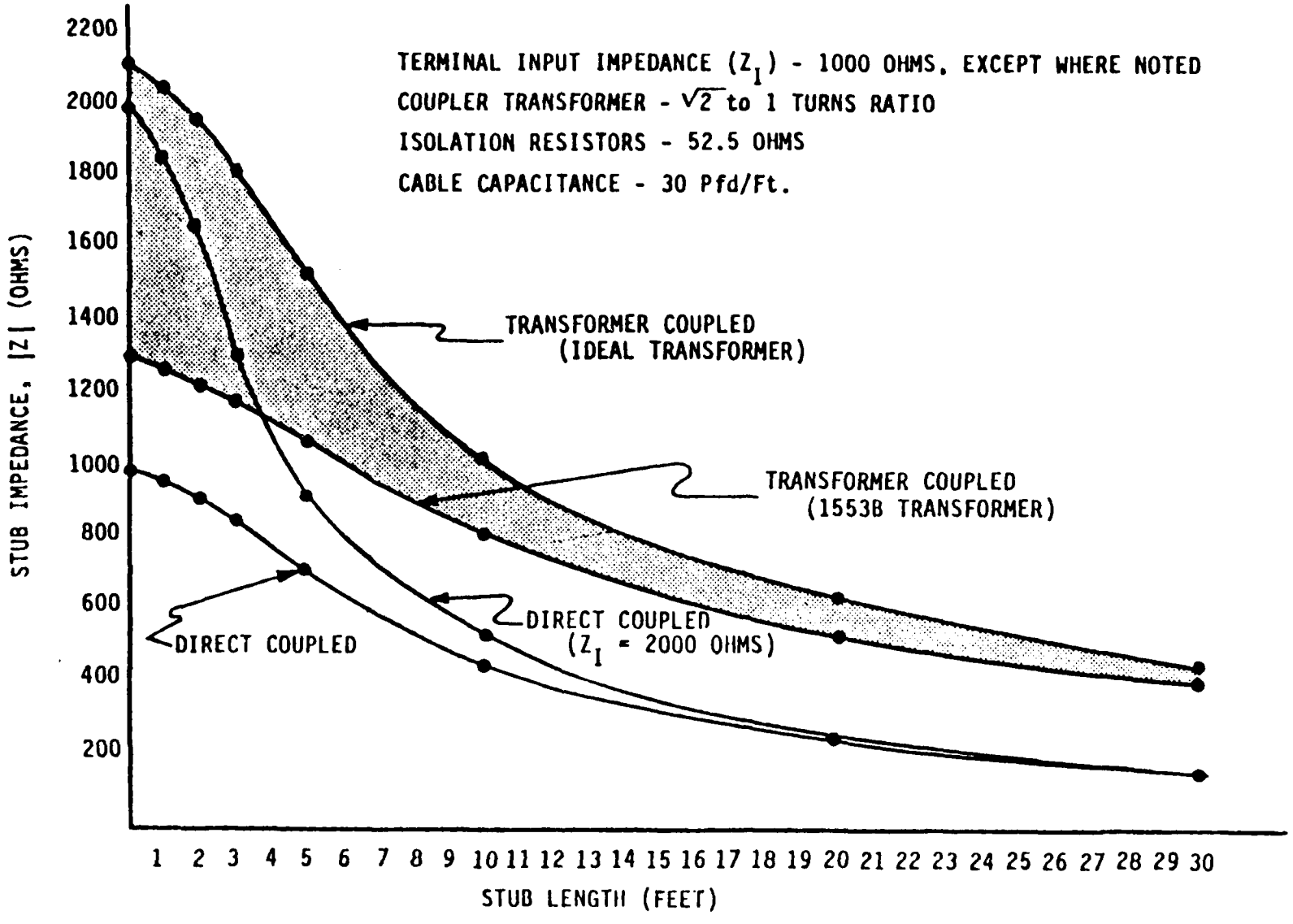


Figure 4.2-3 STUB IMPEDANCE vs. LENGTH

HARDWARE CHARACTERISTICS

TERMINAL INTERFACE

- o TRANSFORMER COUPLED (LONG STUB)
  - INPUT CHARACTERISTICS
  - OUTPUT CHARACTERISTICS
- o DIRECT COUPLED (SHORT STUB)
  - INPUT CHARACTERISTICS
  - OUTPUT CHARACTERISTICS

Table 4.2-2. Summary of Terminal and Data Bus Interface Requirements

Parameter	MIL-STD-1553A	MIL-STD-1553B
• Terminal output characteristics		
• Output voltage	±3.0V to ±10.0V, peak, l-l (6.0V to 20.0V, p-p, l-l) Point A, figure 4.2-4	18.0V to 27.0V, p-p, l-l (transformer coupled) Point A, figure 4.2-6B 6.0V to 9.0V, p-p, l-l (direct coupled) Point A, figure 4.2-6A
• Output waveform	Zero crossing deviation = ±25 ns; rise and fall time of waveform shall be ≥100 ns	Zero crossing deviation = ±25-ns maximum, measured with respect to previous crossing; rise and fall times are 100 to 300 ns Overshoot and ringing = ±900 mV, peak, maximum, l-l Point A, figure 4.2-6B (transformer-coupled stub) Zero crossing deviation and rise and fall times same as above overshoot and ringing; ±300-mV peak, maximum, l-l Point A, figure 4.2-6A (direct-coupled stub)

Table 4.2-2. Summary of Terminal and Data Bus Interface Requirements (Continued)

Parameter	MIL-STD-1553A	MIL-STD-1553B
• Output symmetry	Not specified	Voltage at 2.5 μs after midpoint of parity bit = ±250 mV, peak, maximum, l-l Point A, figure 4.2-6B (transformer-coupled stub) Voltage at 2.5 μs after midpoint of parity bit = ±90 mV, peak, maximum, l-l Point A, figure 4.2-6A (direct coupled stub)
• Output noise	10 mV, p-p, l-l Point A, figure 4.2-4	14.0 mV, rms, l-l Point A, figure 4.2-6B (transformer coupled) 5.0 mV, rms, l-l Point A, figure 4.2-6A (direct coupled)
• Terminal input characteristics		
• Input voltage	±0.5V to ±10.0V peak, l-l (1.0V to 20.0V, p-p, l-l) Point A, figure 4.2-4, terminal responds	0.86V to 14.0V, p-p, l-l, terminal response required; 0.0V to 0.2V, p-p, l-l, terminal no response (with transformer-coupled stubs) Point A, figure 4.2-5B 1.2V to 20.0V, p-p, l-l, terminal response required; 0.0V to 0.28V, p-p, l-l, terminal no response (with direct-coupled stubs) Point A, figure 4.2-5A

Table 4.2-2. Summary of Terminal and Data Bus Interface Requirements (Concluded)

Parameter	MIL-STD-1553A	MIL-STD-1553B
• Input impedance	2,000 ohms, minimum, from 100 kHz to 1.0 MHz Point C, figure 4.2-4	1,000 ohms, minimum, from 75 kHz to 1.0 MHz Point A, figure 4.2-5B (transformer-coupled stub) 2,000 ohms, minimum, from 75 kHz to 1.0 MHz, Point A, figure 4.2-5A (direct coupled)
• Noise rejection	BER = 1 in 10^{12}, maximum Incomplete message rate 1 in 10^{6} Test condition—bus controller connected to RT over 100-ft data bus using 20-ft stubs	Maximum word error rate of 1 in 10^{7} with AWG noise = 1.0 kHz to 4.0 MHz, 140 mV, rms level Signal level = 2.1V, p-p, l-l Point A, figure 4.2-5B (transformer-coupled stub) Maximum word error rate of 1 in 10^{7} with AWG noise = 1.0 kHz to 4.0 MHz, 200 mV, rms level Signal level is 3.0V, p-p, l-l Point A, figure 4.2-5A (direct-coupled stub)
• Common mode rejection	±10.0V peak, line to ground, dc to 2 MHz, shall not degrade performance Point A, figure 4.2-4	±10.0V peak, line to ground, dc to 2.0 MHz, shall not degrade performance of the receiver Point A, figure 4.2-5B (transformer-coupled stub) Same specification for direct-coupled stub Point A, figure 4.2-5A

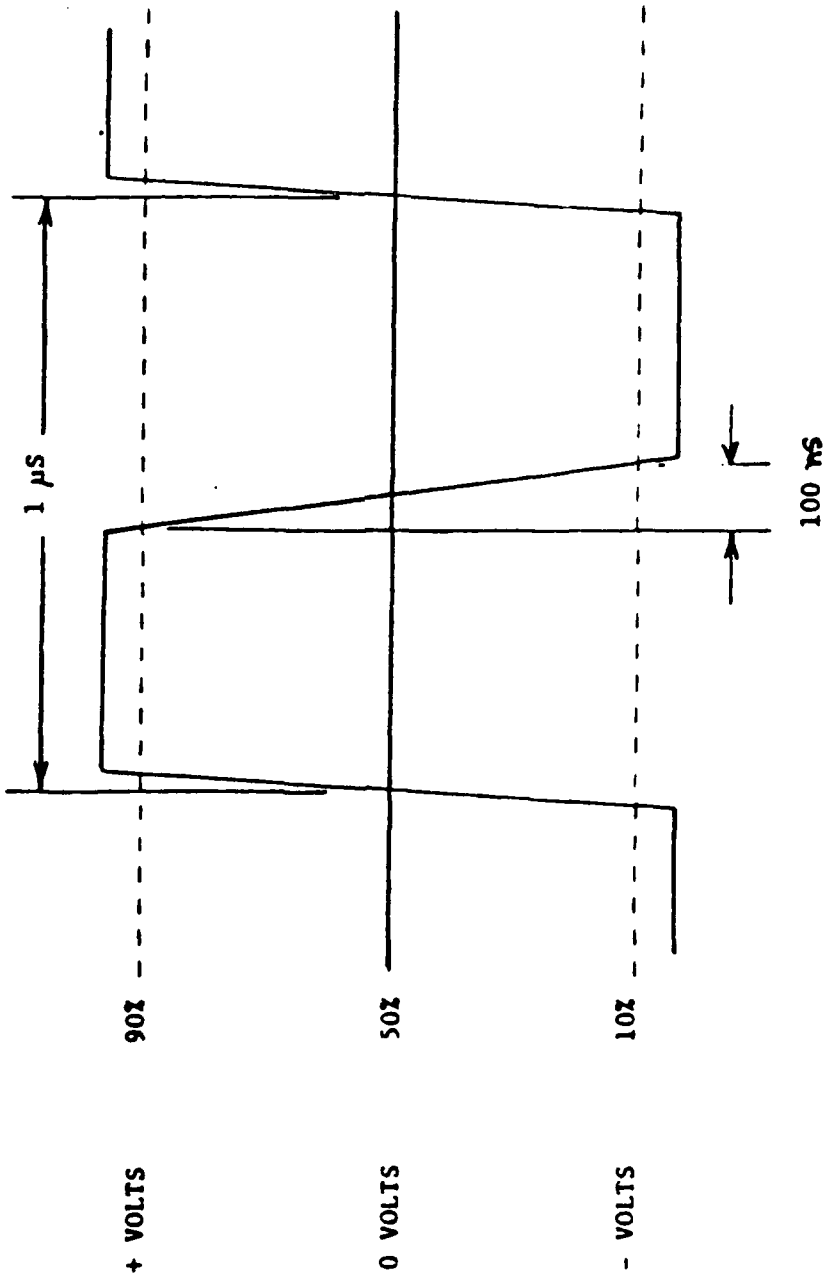


FIGURE 13. Output waveform.

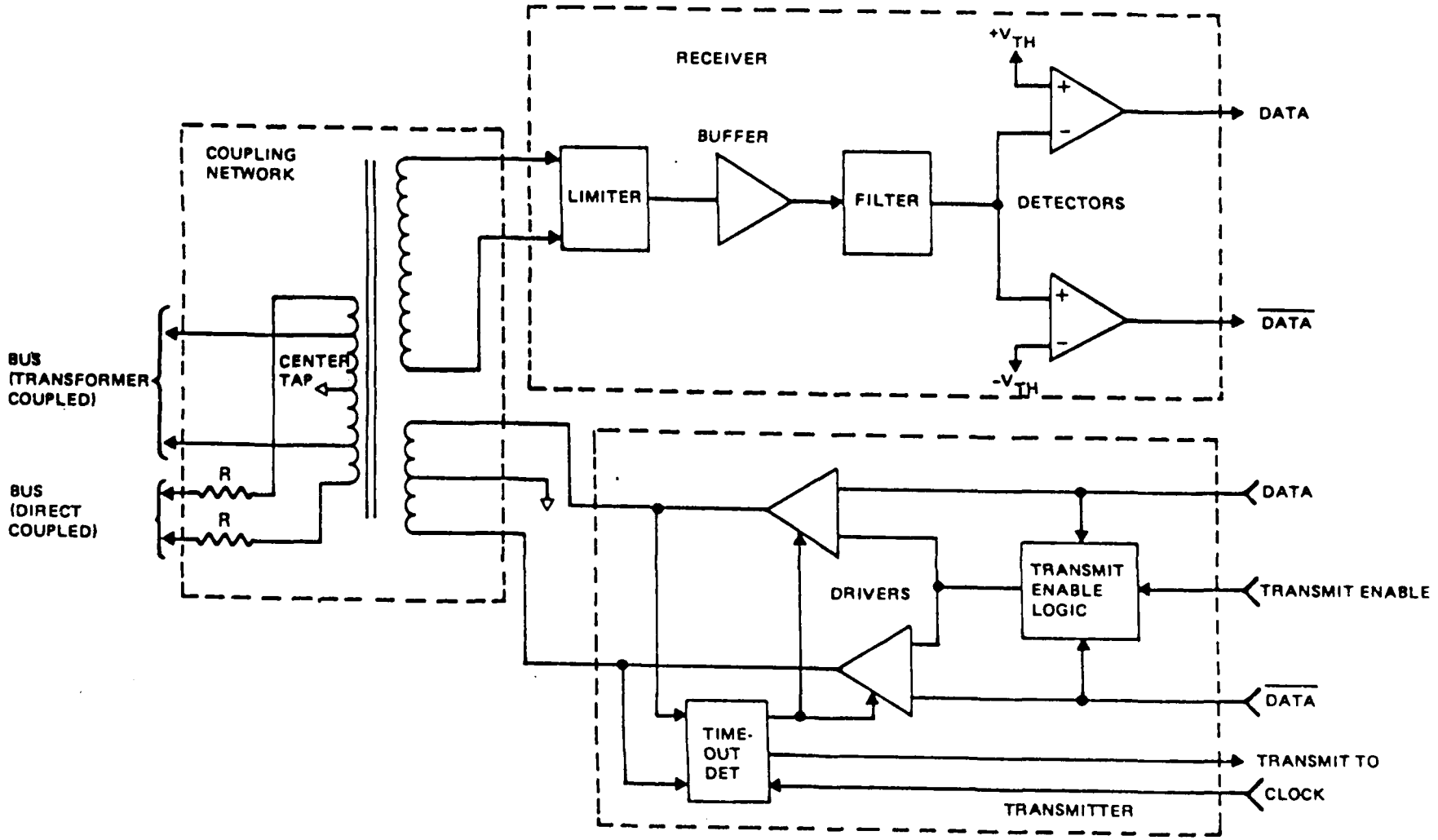


Figure 4.4-1. Typical Transceiver Circuit

REDUNDANT OPERATION

- ELECTRICAL ISOLATION
- SINGLE POINT FAILURE
- DUAL REDUNDANT BUS CONTROL

MIL-STD-1553 CIRCUIT AND COMPONENT SUPPLIERS

HYBRID/LSI

- AEROFLEX LABORATORIES, INC.
  - TRANSMITTER/RECEIVERS(HYBRID)
- CIRCUIT TECHNOLOGY, INC./MARCONI ELECTRONIC PRODUCTS, LTD.
  - TRANSMITTER/RECEIVERS(HYBRID)
  - DATA TERMINAL BIT PROCESSOR(HYBRID/LSI)
  - LSI CHIP SET(RTU/BCU)
  - REMOTE TERMINAL/BUS CONTROLLER INTERFACE MODULES(CUSTOM)
- DATA DEVICE CORPORATION/SMITH INDUSTRIES
  - TRANSMITTER/RECEIVERS(HYBRID/LSI)
  - ENCODER/DECODERS(HYBRID/LSI)
  - RTU INTERFACE MODULES(HYBRID/LSI)
  - PROTOCOL MODULES(HYBRID LSI)
  - LSI CHIP SET(RTU/BCU)
  - BUS CONTROLLER(HYBRID/LSI)
  - MEMORY BUFFERS(HYBRID/LSI)
  - RT/BC INTERFACE MODULES(CUSTOM)
- HARRIS SEMICONDUCTOR
  - ENCODER/DECODERS(LSI)
  - BUS INTERFACE UNIT(LSI)
- ITT CORPORATION(STC)
  - TRANSMITTERS/RECEIVERS
  - ENCODER/DECODERS
  - REMOTE TERMINAL UNITS

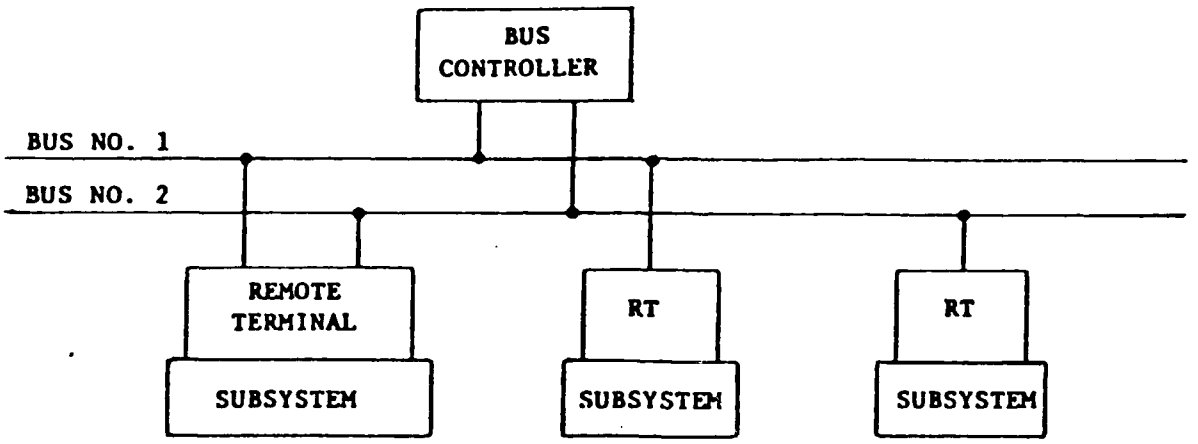


FIGURE 10.1. Illustration of possible redundancy.

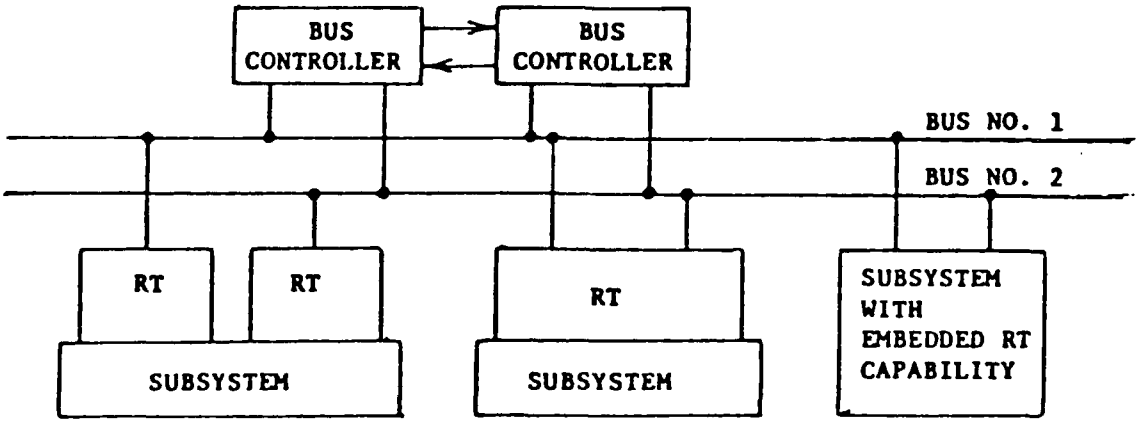


Figure 10.2

NOTE: RT - Remote Terminal

FIGURE 10.2. Illustration of possible redundancy.

MIL-STD-1553 CIRCUIT AND COMPONENT SUPPLIERS(CONT.)

HYBRID/LSI(CONT.)

- ROCKWELL/COLLINS
  - BUS INTERFACE UNIT(LSI)
- STANDARD MICROSYSTEMS CORPORATION/GRUMMAN AEROSPACE CORPORATION
  - BUS INTERFACE UNITS(FULL FUNCTION, SINGLE CHIP LSI)

BUS COUPLING TRANSFORMERS

- DATA DEVICE CORPORATION
- ITT CORPORATION(STC)
- TECHNITROL, INC.
- RAYCHEM CORPORATION(ALSO CUSTOM BUS NETWORK SYSTEMS)

BUS CONNECTORS

- AMPHENOL CORPORATION
- TROMPETER ELECTRONICS, INC.(ALSO SUPPLIES CABLE)
- RAYCHEM CORPORATION(ALSO SUPPLIES CABLE AND BUS SYSTEMS)

LSI BUS INTERFACE CHIP SETS

CIRCUIT TECHNOLOGY, INC./MARCONI ELECTRONIC PRODUCTS, LTD.

- CT 10894 DECODER(1 ADDITIONAL CHIP PROVIDES DUAL REDUNDANT OPERATION)
- CT 10895 ENCODER
- CT 10896 INTERFACE UNIT
- CT 10897 INTERNAL HIGHWAY CONTROL LOGIC

DATA DEVICE CORPORATION/SMITH INDUSTRIES

- MT-32008 ENCODER/DECODER(ADDITIONAL CHIP PROVIDES DUAL REDUNDANT OPER.)
- MT-32004 PROTOCOL SEQUENCER
- MT-32003 16x32 FIFO

HARRIS SEMICONDUCTOR

- HS-3273(BIU,TYPE 1)

ROCKWELL/COLLINS

- BIU-BIT/WORD PROCESSOR ONLY(ENCODER,(2) DECODERS, STATUS REGISTER,NO PROTOCOL SEQUENCER OR SUBSYSTEM INTERFACE)

STANDARD MICROSYSTEMS CORPORATION/GRUMMAN AEROSPACE CORPORATION

- COM1553A(LSI-DESIGNED FOR 1553A)
- COM1553B(SINGLE CHIP RTU OR BCU, WITH SUPPORTING LOGIC)

Table 1 Overall Comparison

GRUMMAN/SMC BIU CHIP	HARRIS BIU # 1 CHIP	SMITH BIU CHIP SET	MARCONI BIU CHIP SET
PROVIDES 16-BIT PARALLEL INTERFACE TO THE SUB-SYSTEM	8-BIT/16-BIT	16-BIT	8-BIT
ALLOWS FOR SETTING OF RESERVED STATUS BITS	NO	NO	NO
CONTAINS DOUBLE-BUFFERED I/O, 4 DOUBLE-BUFFERED STATUS BITS	SAME AS GRUMMAN/SMC	FIFO-BUFFERED I/O 4 DOUBLE-BUFFERED STATUS BITS	DOUBLE-BUFFERED I/O, 4 DOUBLE-BUFFERED STATUS BITS
PROVIDES DMA HANDSHAKE CONTROL ASYNCHRONOUS DATA TRANSFER	SAME AS GRUMMAN/SMC	SYNCHRONOUS TRANS-FER CONTROL	DMA HANDSHAKE CONTROL SYNCHRONOUS DATA TRANSFER
HANDLES RT-RT COMMANDS	YES	YES	YES
HANDLES BROADCAST	YES	YES	YES
NO	PROVISIONS FOR OP-ERATING AT DIFFERENT BIT RATES	NO	NO
CAPABLE OF READING LAST COMMAND, ERROR, OR DATA REGISTERS	CAN ONLY READ ERROR - AUTOMATICALLY CHECKS OWN TRANSMISSION	CAN ONLY READ ERROR	CAN ONLY READ ERROR
ABOVE REGISTERS AUTO-MATICALLY DMAED INTO MEMORY AT END OF RT MESSAGES	NO	NO	NO
40-PIN SINGLE CHIP	40-PIN SINGLE CHIP	48-PIN ENCODER/DE-CODER - UART 40-PIN FIFO 53-PIN PROTOCOL SEQUENCER	40-PIN RECEIVER 40-PIN TRANSMITTER 48-PIN INTERFACE UNIT 40-PIN INTERNAL HIGHWAY CONTROL LOGIC
FOUR REGISTER CHIPS THREE LOGIC CHIPS TRANSCEIVER/TRANS-FORMER AND OSCILLATOR IS SUPPORTING CIRCUITRY FOR SIMPLE RT APPLICATION	SIMILAR TO GRUMMAN/ SMC	SLIGHTLY LESS THAN GRUMMAN/SMC	SLIGHTLY LESS THAN GRUMMAN/SMC
ADDITIONAL BIU NEEDED FOR REDUNDANCY	SAME AS GRUMMAN/SMC	ADDITION ENCODER/ DECODER-UART	ADDITIONAL RECEIVER
HANDLES: DYNAMIC BUS CONTROL TRANSMIT STATUS WORD INHIBIT T/F BIT OVERRIDE INHIBIT T/F BIT TRANSMIT LAST COM-MAND CODE CODES AUTOMATICALLY	SAME AS GRUMMAN/SMC	HANDLES ALL MODE CODES AUTOMATICALLY	HANDLES ALL MODE CODES AUTOMATICALLY
PROVIDES FOR READING OF SOFTWARE LOADED RT - ADDRESS	NO	HARDWIRED WITH PARITY BIT	HARDWIRED WITH PARITY BIT
NMOS	JUNCTION - ISOLATED CMOS	CMOS	METAL GATE CMOS
APPROX $250	APPROX $500	>$1,000	>$1,000

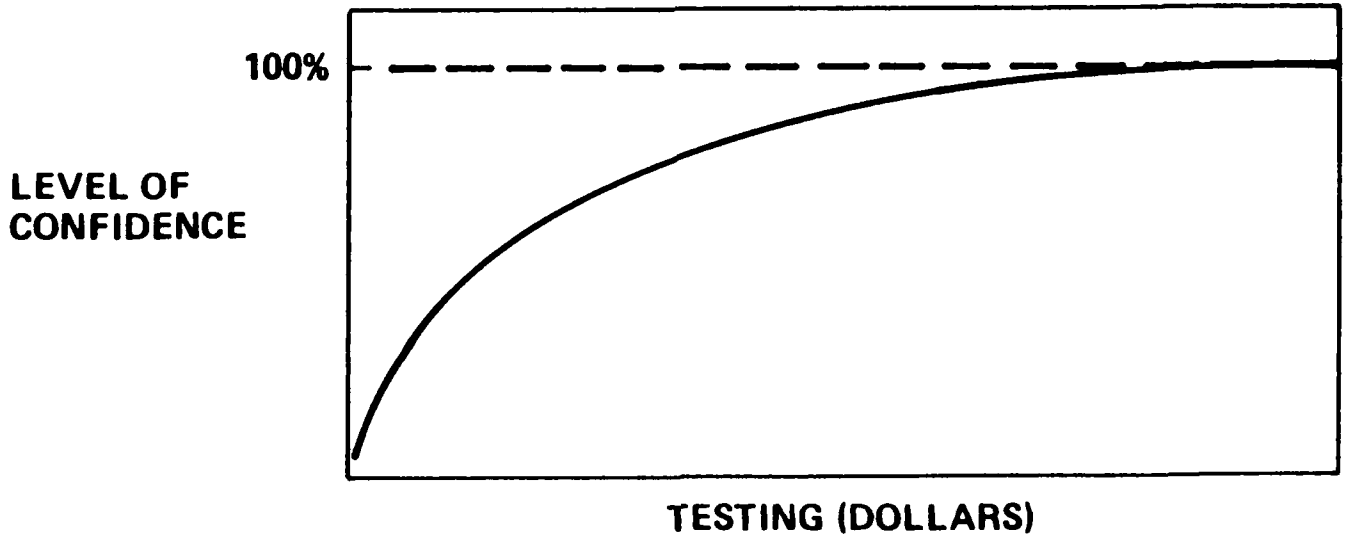
1806-007P

Testing and Test Equipment

Leroy Earhart
Test Systems, Inc.
217 W. Palmaire
Phoenix, Arizona
(602) 861-1010

Amount of Testing Is A Compromise

TEST TO PROVIDE A SPECIFIED
LEVEL OF CONFIDENCE THAT
THE UUT FUNCTIONS PROPERLY



TESTING AND TEST EQUIPMENT

- PHASES OF TESTING
- TEST REQUIREMENTS
- FUNCTIONAL REQUIREMENTS FOR TEST EQUIPMENT
- OVERVIEW OF AVAILABLE TEST EQUIPMENT

PHASES OF TESTING

- o DEVELOPMENT TESTS
- o DESIGN VERIFICATION
- o SYSTEM TESTS
- o PRODUCTION TESTING
- o FIELD TESTING

TESTING

- ALL PHASES OF TESTING REQUIRE ERROR INJECTION TO VERIFY THE OPERATION OF THE MESSAGE VALIDATION AND ERROR DETECTION CIRCUITS.

TEST REQUIREMENTS

- ELECTRICAL INTERFACE TESTS
  - INPUT TESTS
  - OUTPUT TESTS
  - ISOLATION BETWEEN REDUNDANT BUSES

- TERMINAL PROTOCOL TESTS
  - REMOTE TERMINAL TESTS
  - BUS CONTROLLER TESTS

INPUT TESTS

- POLARITY
- AMPLITUDE VARIATION
  - RESPONSE
  - NO RESPONSE
- INPUT IMPEDANCE
- COMMON MODE REJECTION (CMR)
- ZERO CROSSING DEVIATION
- TRANSMISSION RATE
- NOISE REJECTION/ERROR RATE

Connections To The Data Bus

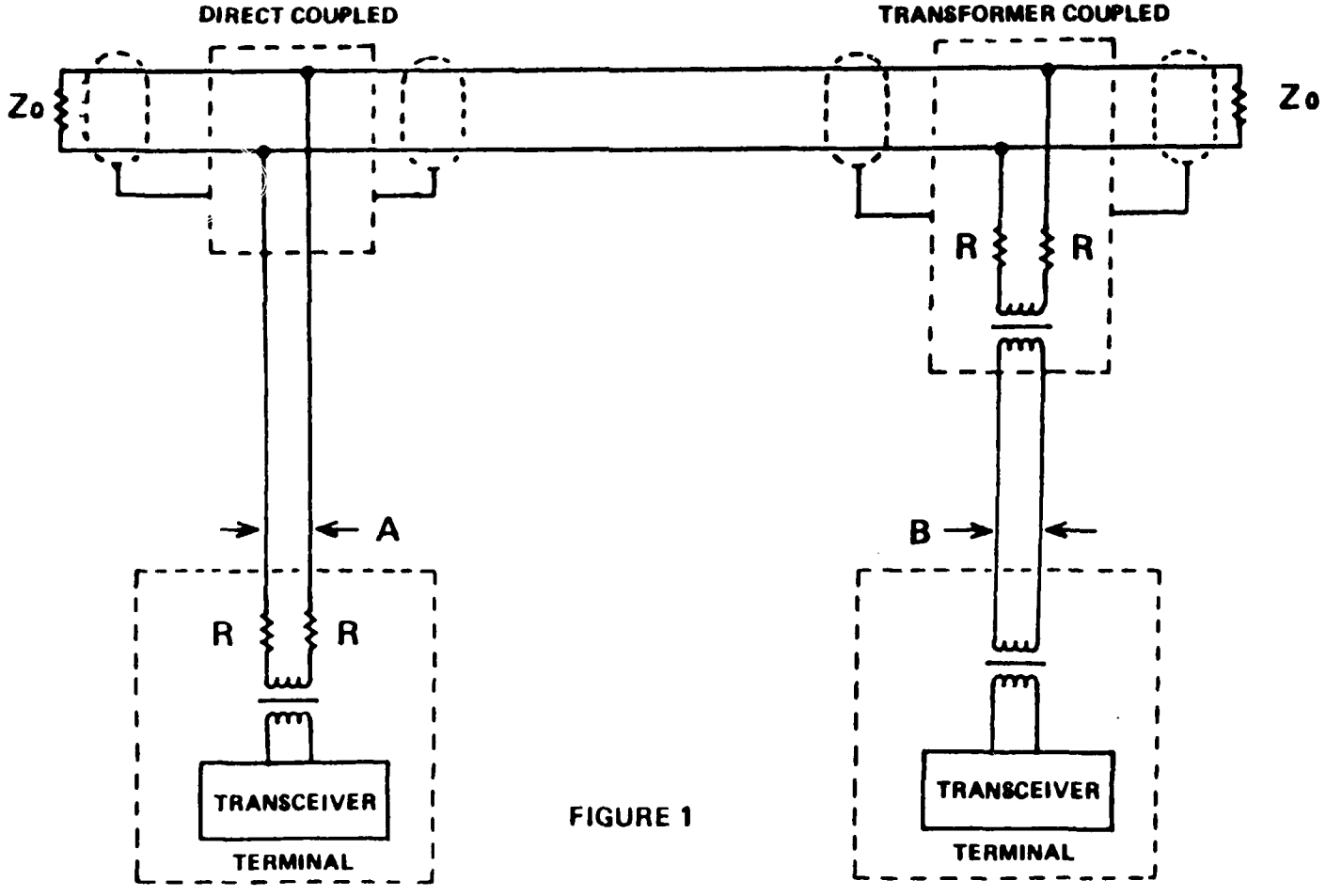


FIGURE 1

Configuration For Testing Common Mode Rejection

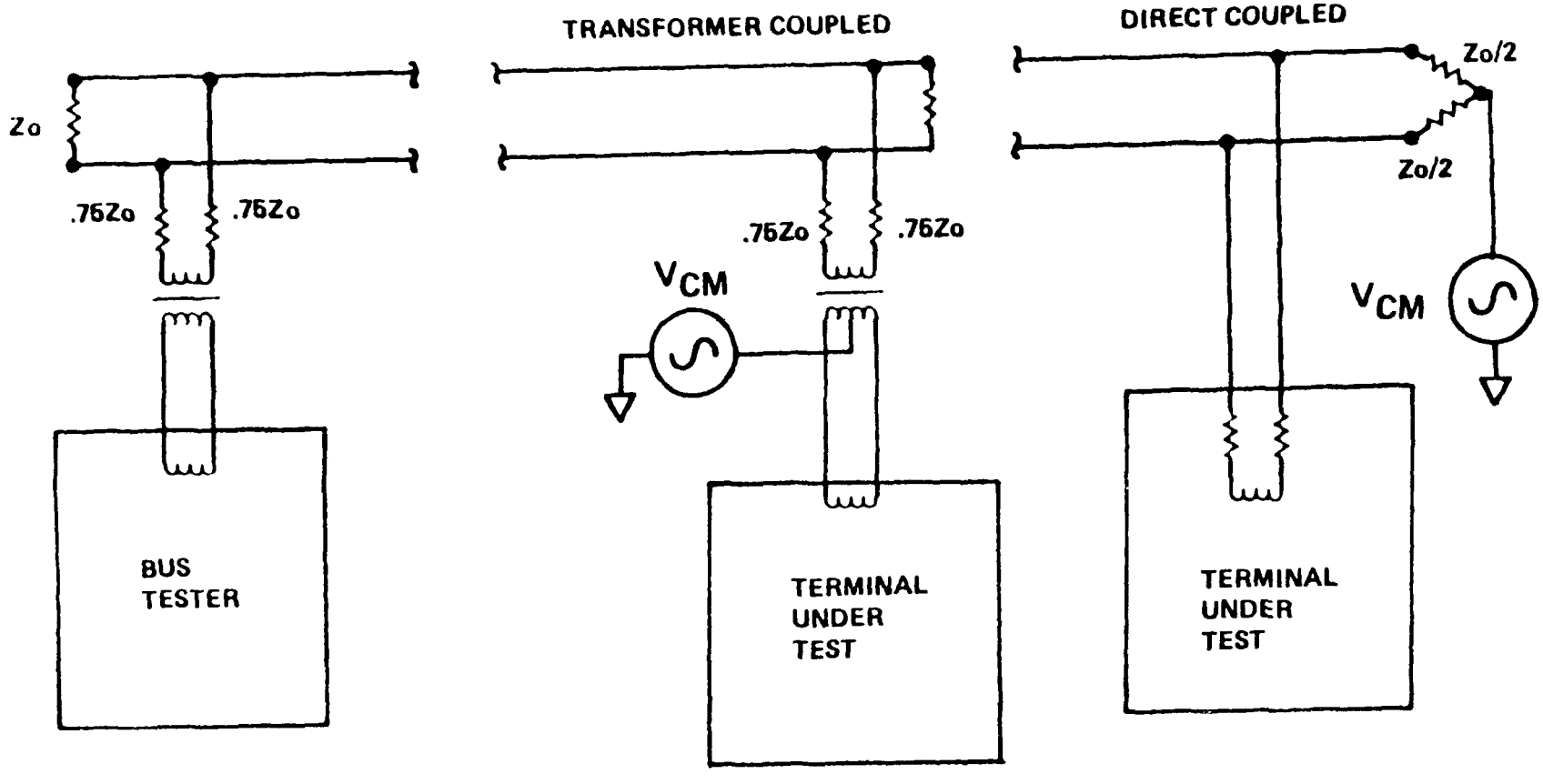


FIGURE 2

Typical Set-Up For Noise Rejection Test

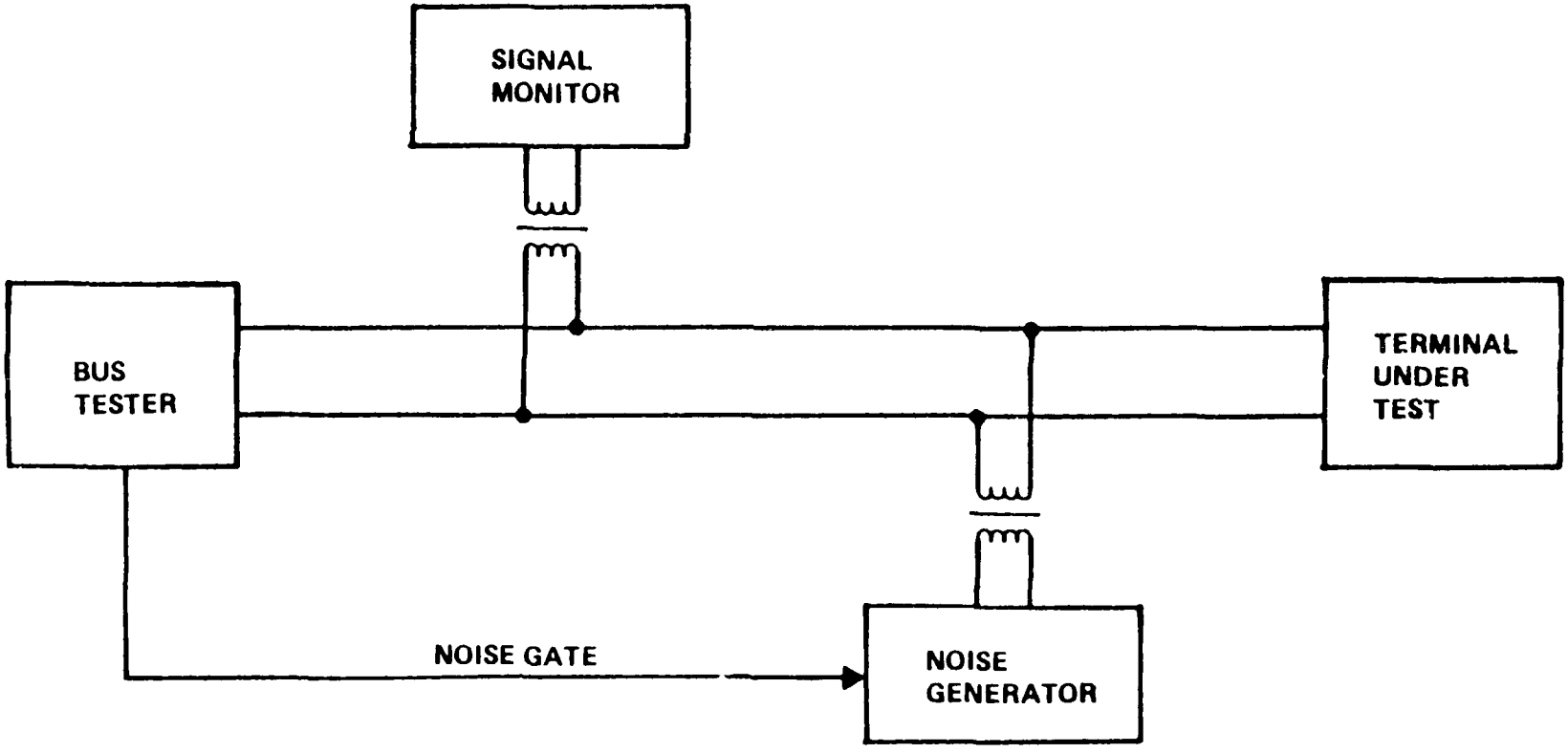
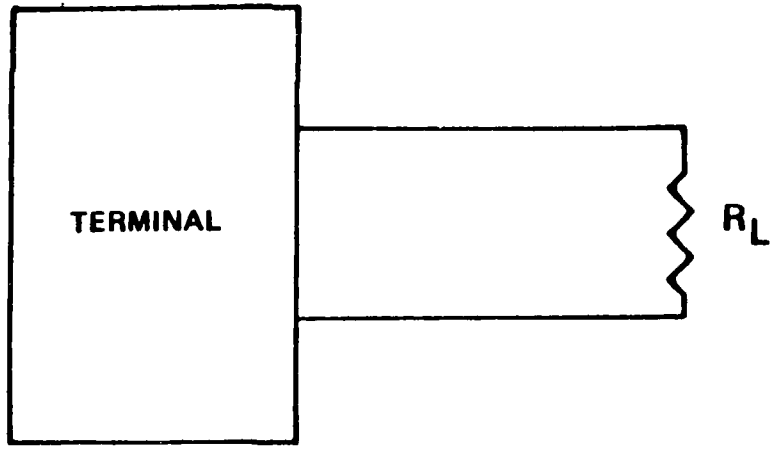


FIGURE 3

OUTPUT TESTS

- POLARITY
- AMPLITUDE
- RISE/FALL TIMES
- WORD LENGTH
- TRANSMISSION BIT RATE (CLOCK STABILITY)
- WORD SYNC AND BIT ENCODING
- ZERO CROSSING STABILITY
- OVERSHOOT AND RINGING
- OUTPUT SYMMETRY
- OUTPUT NOISE

Configuration For Terminal Output Tests



- TRANSFORMER COUPLED: R_L = 70 OHMS
- DIRECT COUPLED: R_L = 35 OHMS

FIGURE 4

ISOLATION BETWEEN REDUNDANT BUSES

- SPECIFICATION - 45 DB MINIMUM
- CROSSTALK (COUPLING)
  - NOISE
  - INTERNAL BUS ROUTING

REMOTE TERMINAL TESTS

- LEGAL (VALID) INFORMATION TRANSFER FORMATS
- UNIQUE TERMINAL ADDRESS
- RESPONSE TIME
- RESPONSE TO SUPERCEDING COMMANDS
- ILLEGAL COMMANDS
- INVALID COMMANDS
- VALID COMMANDS WITH INVALID DATA
- MESSAGE LENGTH VALIDITY
- MESSAGE CONTINUITY
- REDUNDANT BUS OPERATION

BUS CONTROLLER TESTS

- VALID COMMAND AND DATA FORMATS
- PROCESSING NORMAL RT RESPONSES
- PROCESSING ABNORMAL RT RESPONSES
- CHECK-OUT SOFTWARE
  - MULTIPLEX CONTROL
  - AVIONIC SYSTEM CONTROL

TEST EQUIPMENT FUNCTIONAL REQUIREMENTS

- COMMON REQUIREMENTS
- REMOTE TERMINAL TESTERS
- BUS CONTROLLER TESTERS
- BUS MONITORS

REMOTE TERMINAL TESTER

- FORMAT COMMANDS AND DATA
- RECEIVES AND STORES RESPONSES
- CONTROLLED ERRORS GENERATED
  - SYNC ERROR (INVERTED OR SHIFTED MID TRANSITION)
  - BIT ENCODING ERROR
  - PARITY ERROR
  - BIT COUNT ERROR (TOO FEW/TOO MANY)
  - DISCONTIGUOUS DATA (GAP)
  - WORD COUNT ERROR (TOO FEW/TOO MANY)
  - MIXED BUS TRANSMISSION IN MESSAGE
  - INCOMPLETE MESSAGE WITH SUBSEQUENT COMMAND

REMOTE TERMINAL TESTER CONTINUED

- CONTROLLED VARIATIONS
  - TRANSMISSION BIT RATE
  - ZERO CROSSING DEVIATION
  - INTER MESSAGE GAP

- VALIDATION CHECKS
  - RESPONSE TIME
  - BIT ENCODING
  - BIT COUNT
  - ODD PARITY
  - TRANSMISSION CONTINUITY
  - WORD COUNT
  - SIMULTANEOUS BUS ACTIVITY

BUS CONTROLLER TESTER

- PROCESSES COMMANDS AND DATA
- FORMATS STATUS AND DATA
- CONTROLLED ERRORS GENERATED
  - SYNC ERROR (INVERTED OR SHIFTED MID TRANSITION)
  - BIT ENCODING ERROR
  - PARITY ERROR
  - BIT COUNT ERROR (TOO MANY/TOO FEW)
  - DISCONTIGUOUS DATA (GAP)
  - WORD COUNT ERROR (TOO MANY/TOO FEW)
  - NO RESPONSE (FAILED BUS)
  - WRONG TERMINAL ADDRESS IN STATUS
  - ERROR FLAGS IN STATUS
  - RESPONSE ON WRONG BUS

BUS CONTROLLER TESTER CONTINUED

- CONTROLLED VARIATIONS
  - TRANSMISSION BIT RATE
  - ZERO CROSSING DEVIATION
  - RESPONSE TIME

- VALIDATION CHECKS
  - INTER MESSAGE GAP TIME
  - BIT ENCODING
  - BIT COUNT
  - ODD PARITY
  - TRANASMISSION CONTINUITY
  - WORD COUNT
  - SIMULTANEOUS BUS ACTIVITY

BUS MONITOR

- RECEIVE DATA BUS TRAFFIC
- EXTRACT SELECTED INFORMATION
- STATISTICAL ANALYSIS FUNCTION
  - STORE AND TABULATE INFORMATION
    - ACTIVE TERMINALS BY ADDRESS AND DATA BUS
    - UNIQUE COMMANDS
    - ERROR CONDITIONS
- LOGIC ANALYZER TYPE FUNCTION
  - EVENT TRIGGER CONDITIONS
  - STORE DATA BUS TRAFFIC
    - PRECEEDING TRIGGER CONDITION
    - CENTERED ABOUT TRIGGER CONDITION
    - FOLLOWING TRIGGER CONDITION
  - TRIGGER OUTPUT

Comparison of Test Equipment

1/4	TEST SYSTEMS INC BCM	TEST SYSTEMS INC MTS	FAIRCHILD DBMC	LORAL SBA 100	SCI SYSTEMS BST 1100	SPECTRAL MODEL 20
PRIMARY FUNCTIONS RT TESTER	YES	NO	YES	YES	YES	YES
BC TESTER	NO	YES 0-32 RTs	YES 1RT	YES 0-32 RTs	YES 0-31 RTs	YES *
BUS MONITOR	YES	YES VIA GPC	YES	YES	YES	YES
BUS ACTIVITY SIM.	YES	NO	YES	YES	NO	NO
MANUAL INTERFACE	SWITCHES & LED DISPLAY	SWITCHES & LED DISPLAY	KEY PAD, LIGHT PEN & CRT	KEY PAD, KEY BOARD & CRT	KEY BOARD & CRT	KEY PAD & CRT
COMPUTER INTERFACE HIGH SPEED PARALLEL	YES	YES	NO	NO	NO	NO
IEEE 488	NO	NO	NO	YES	OPTIONAL	YES
RS 232	NO	NO	YES	YES	YES	YES
TAPE TRANSPORT	NO	NO	OPTION	YES	YES	NO
BUS INTERFACE DUAL REDUNDANT	YES	YES	YES	YES	YES	YES *
DIRECT COUPLED	YES } SWITCH	YES } SWITCH	YES } SWITCH	YES } OPER	YES } INT	YES * } OPER.
TRANSFORMER COUPLED	YES } SEL.	YES } SEL.	YES } SEL.	YES } SEL.	YES } JUMPERS	YES } SEL.
AMPLITUDE CONTROL	0.1-20Vp-p	0.1-20Vp-p	0.5-30Vp-p	0-27Vp-p	0.5-15Vp-p	0-27Vp-p
CONNECTOR	SPLIT	SPLIT	CONCENTRIC	CONCENTRIC	CONCENTRIC	CONCENTRIC

* : QUALIFIED CAPABILITY
GPC: GENERAL PURPOSE COMPUTER

Comparison of Test Equipment (Continued)

2/4	TEST SYSTEMS INC BCM	TEST SYSTEMS INC MTS	FAIRCHILD DBMC	LORAL SBA 100	SCI SYSTEMS BST 1100	SPECTRAL MODEL 20
RT TESTER						
TRANSMIT CMD & DATA	128 WDS	---	128 MSG; 8 DATA TBLS; RANDOM DATA	32 MSG. MIN 1024 WDS MIN	64 MSG.	1 MSG.
RESPONSE STATUS & DATA	128 WDS	---	MONITOR, 1000 WDS	MONITOR, 2048 WDS	64 MSG.	1 MSG.
SIMULATE OTHER RT TRAFFIC	YES	---	YES	YES	NO	LIMITED
ADAPTIVE POLLING	NO	---	YES	YES	NO	NO
BC TESTER						
TERMINALS SIMULATED	---	0-32 TERM. ADD	1 TERM. ADD.	32 INDEP. MSG.	0-31 TERM. ADD.	1 MSG
MEMORY FOR TX DATA	---	4096 SHARED	8 DATA TBLS RANDOM DATA	32 MSG.	1024 WDS	1 MSG.
MEMORY FOR REC DATA	---	3072 SHARED	MONITOR, 1000 WDS	MONITOR, 2048 WDS	1024 WDS	256 WDS
TRANSMIT REC DATA	---	YES	YES	YES	YES	NO
BUS MONITOR						
STATISTICAL ANALYSIS	VIA GPC	VIA GPC	YES	YES	---	NO
LOGIC ANALYZER TYPE	YES	VIA GPC	YES	YES	---	YES
MEMORY SIZE	256 WDS	---	1000 WDS	2048 WDS	1024 WDS	256 WDS

• : QUALIFIED CAPABILITY
GPC: GENERAL PURPOSE COMPUTER

Comparison of Test Equipment (Continued)

3/4	TEST SYSTEMS INC BCM	TEST SYSTEMS INC MTS	FAIRCHILD DBMC	LORAL SBA 100	SCI SYSTEMS BST 1100	SPECTRAL MODEL 20
NOISE GATE	YES	YES	NO	YES	NO	YES
GENERATED ERRORS	(NOTE 1)	(NOTE 1)	(NOTE 2)	(NOTE 3)	(NOTE 4)	(NOTE 1)
SYNC ERROR-INVERT	YES	NO	YES	NO	YES	YES
SYNC ERROR-SHIFT	YES	YES	NO	YES	NO	NO *
BIT ENCODING ERROR	YES	YES	NO	YES	NO	YES
PARITY ERROR	YES	YES	YES	YES	YES	YES
BIT COUNT ERROR	NO	NO	± 1 BIT	+ 1 TO 9 - 1 TO 3	NO	1-99 BITS
DISCONTIGUOUS DATA	2, 8, 14 μs	1 μs	NO	1-6.5 μs	NO	1-99 μs
WORD COUNT ERROR	YES	± 1 WD	± 1 - 33	+ 1 TO 4 - 1 TO 32	NO	YES
NO RESPONSE	---	YES	YES	YES	YES	YES
WRONG TA IN STATUS	---	NO	YES	YES	NO	YES
STATUS BITS	---	YES	YES	YES	YES	YES
RSP ON WRONG BUS	---	NO	YES	YES	NO	YES

NOTE 1: ERRORS GENERATED IN ANY WORD.
NOTE 2: ERRORS GENERATED IN THE COMMAND WORD OR THE LAST DATA WORD OF THE SELECTED MESSAGE.
NOTE 3: ERRORS GENERATED ONE AT A TIME IN A MESSAGE EITHER FIXED TO A SELECTED POSITION OR RIPPLING THROUGH ALL THE POSITIONS.
NOTE 4: ERRORS GENERATED IN CONTROLLER MODE ONLY. INVERTED SYNC IS PUT IN ALL WORDS. PARITY ERROR IN CMD OR ALL DATA WORDS.

* : QUALIFIED CAPABILITY
GPC: GENERAL PURPOSE COMPUTER

Comparison of Test Equipment (Concluded)

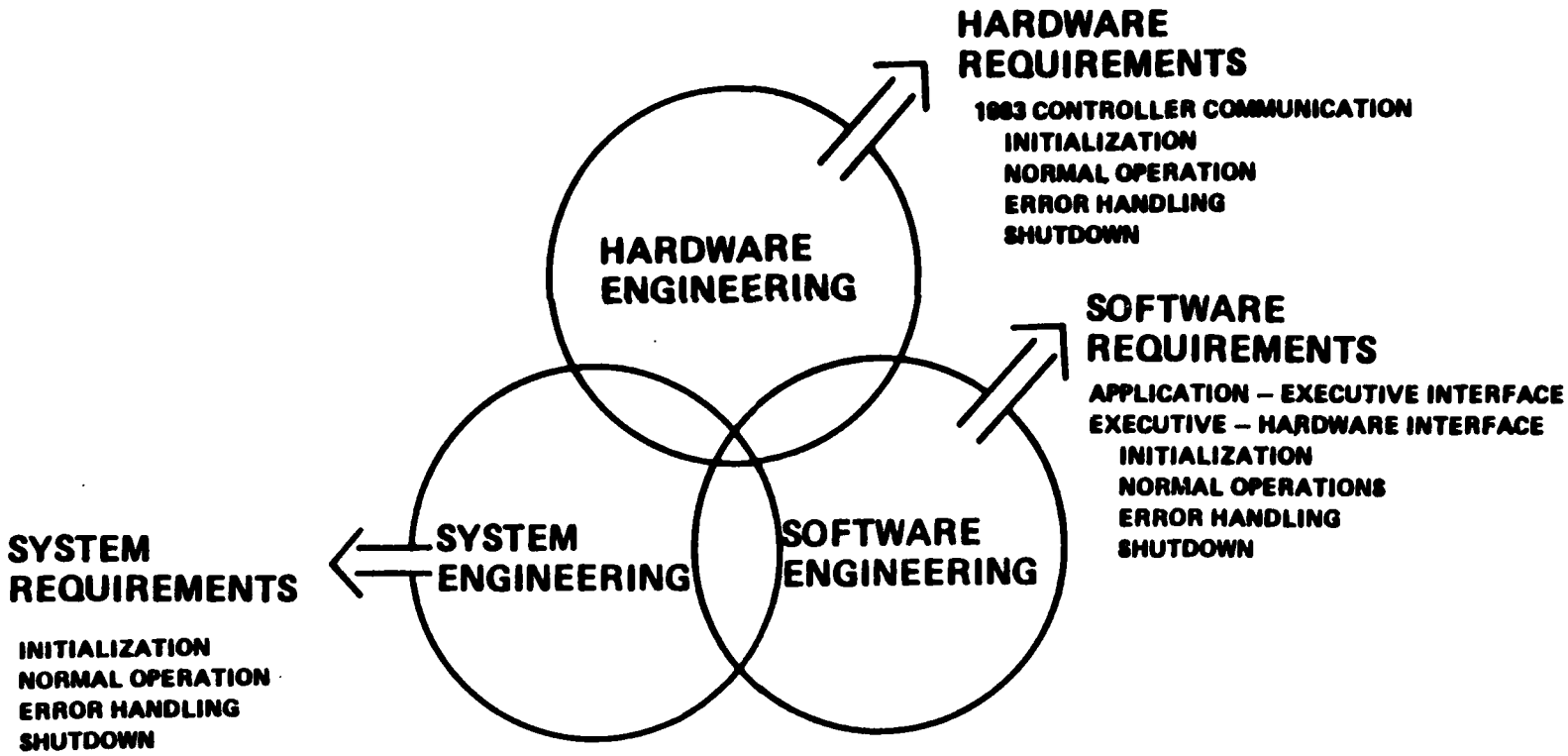
4/4	TEST SYSTEMS INC BCM	TEST SYSTEMS INC MTS	FAIRCHILD DBMC	LORAL SBA 100	SCI SYSTEMS BST 1100	SPECTRAL MODEL 20
VARIABLES						
TRANSMISSION BIT RATE	NO	NO	NO	YES ± 100 Hz ± 1000 Hz	NO	NO
ZERO CROSSING DEVIATION	± 0-200 ns	NO	NO	± 150, ± 200 ns	NO	± 0-375 ns
INTERMESSAGE GAP	YES	——	YES	YES	YES	NO
TERMINAL RESPONSE	——	NO	NO	2-32 μs	NO	YES
VALIDATION CHECKS						
BIT COUNT	YES •	YES •	YES	YES	YES (LOW)	YES
BIT ENCODING	YES	YES	YES	YES	YES	YES
ODD PARITY	YES	YES	YES	YES	YES	YES
TRANSMISSION CONTINUITY	0.5 μs	0.5 μs	1.0 μs	0.5 μs	YES	0.5 μs
WORD COUNT	YES	NO	YES	YES	YES	INDIRECTLY
TERMINAL RESPONSE TIME	YES (15 μs)	——	YES	YES (5/10/12/17 (50 μs)	YES (20 μs)	YES
INTERMESSAGE GAP TIME	NO	NO	YES	YES	NO	YES
SIMULTANEOUS BUS ACTIVITY	NO	NO	YES	YES	NO	NO

• : QUALIFIED CAPABILITY
GPC: GENERAL PURPOSE COMPUTER

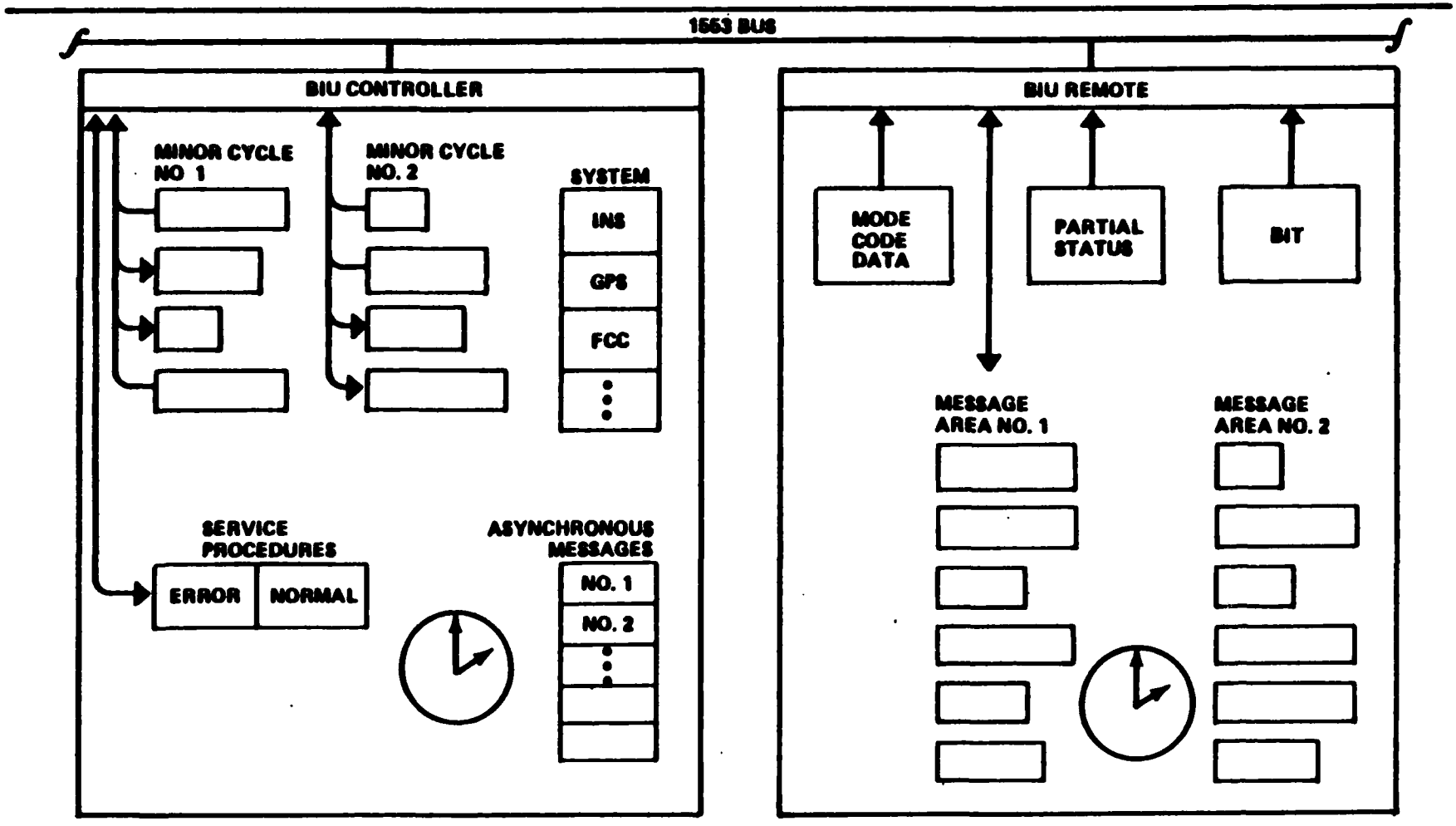
SOFTWARE DESIGN

DR. LEROY A. SMITH

Purpose of Course

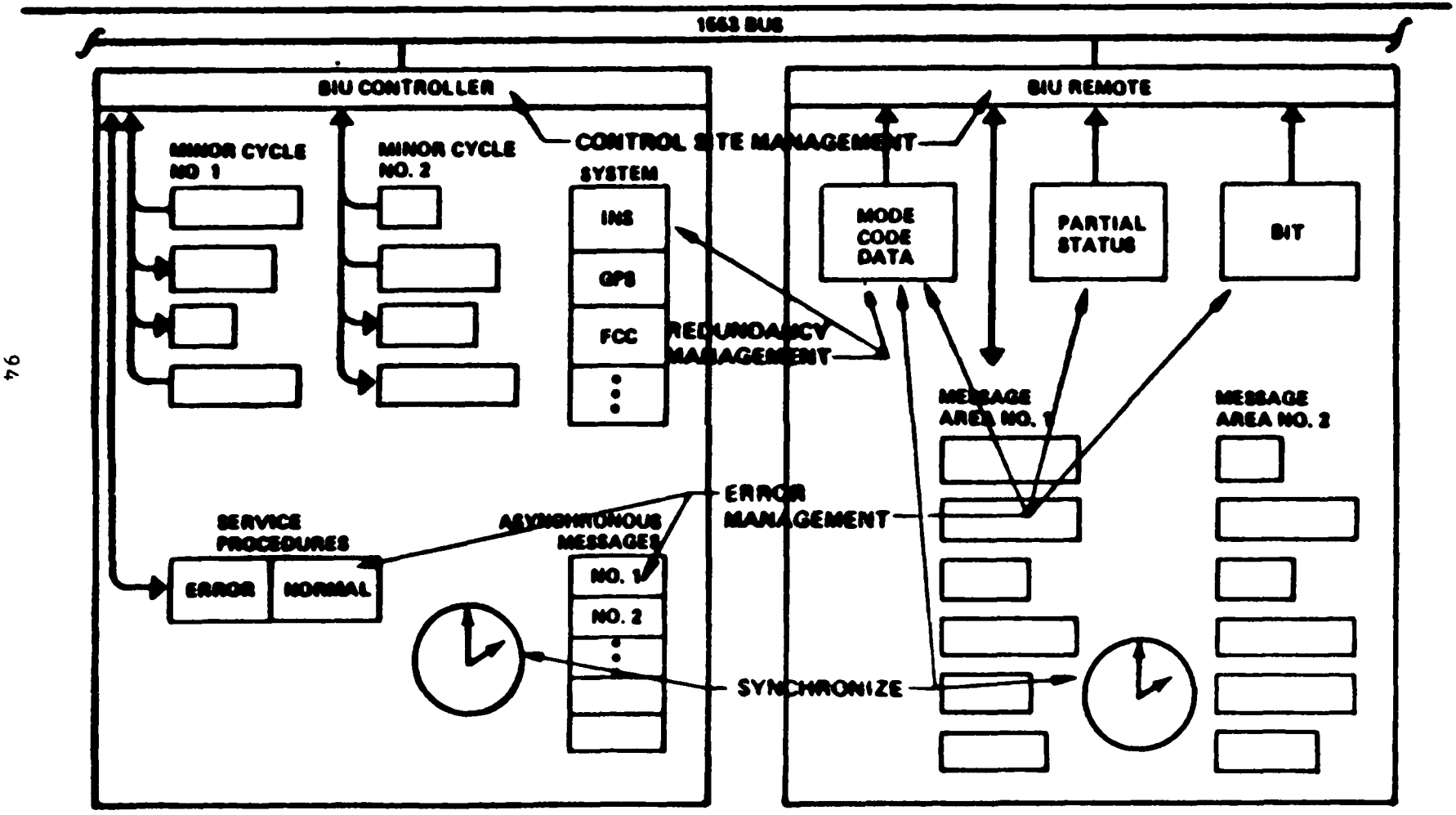


Bus Control Software



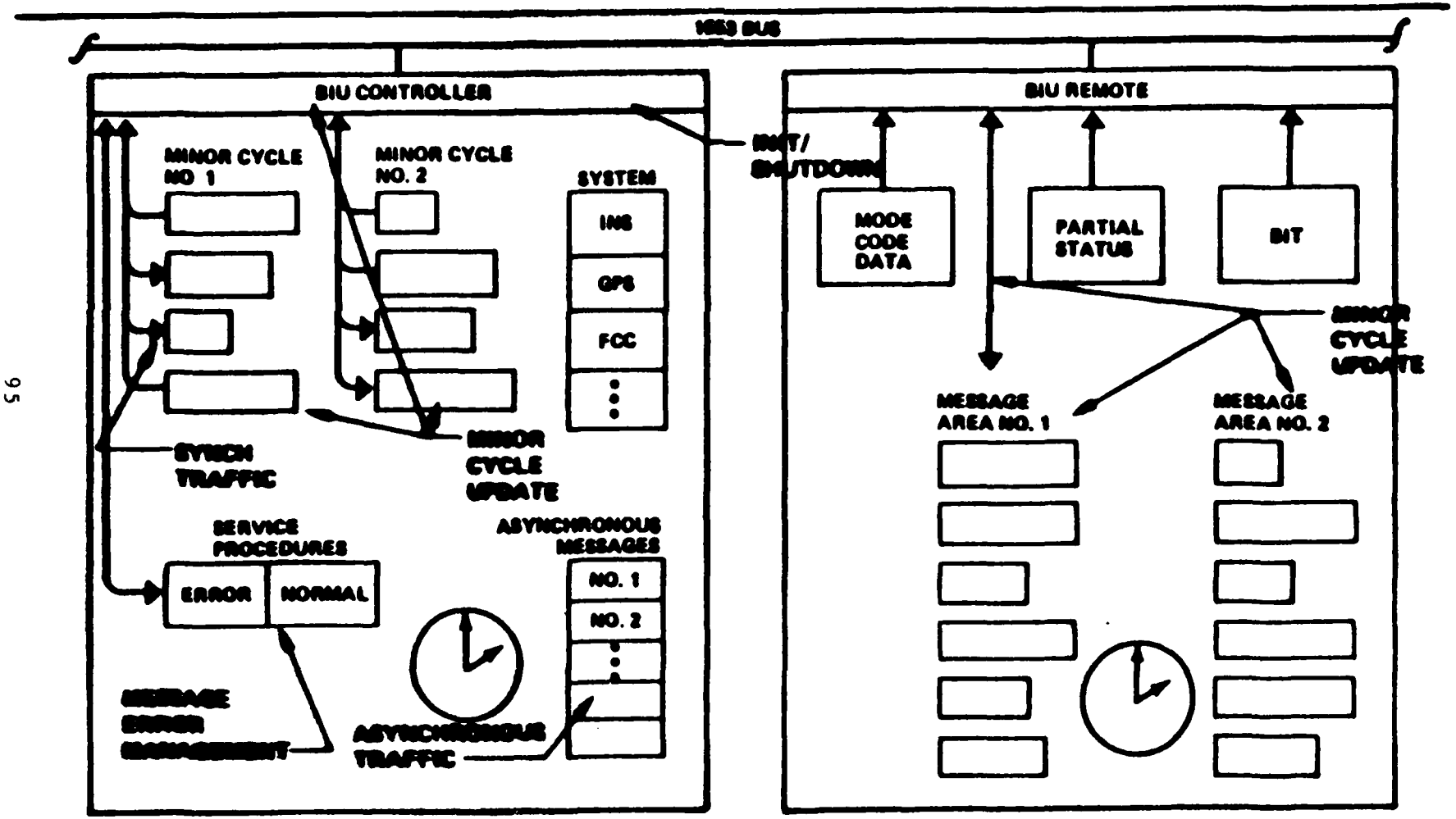
Bus Control Software

System Control Functions



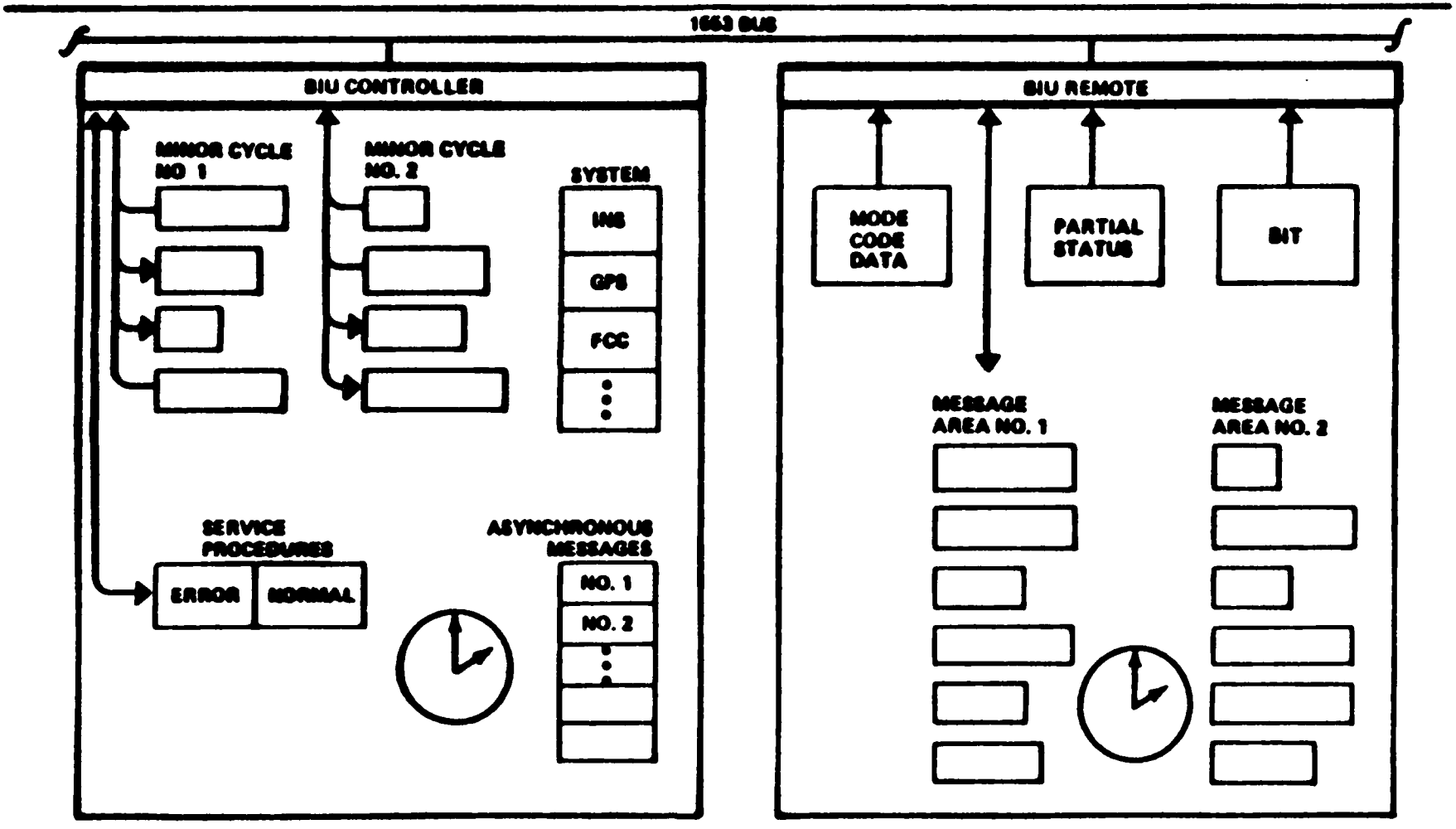
Bus Control Software

Message Control Function

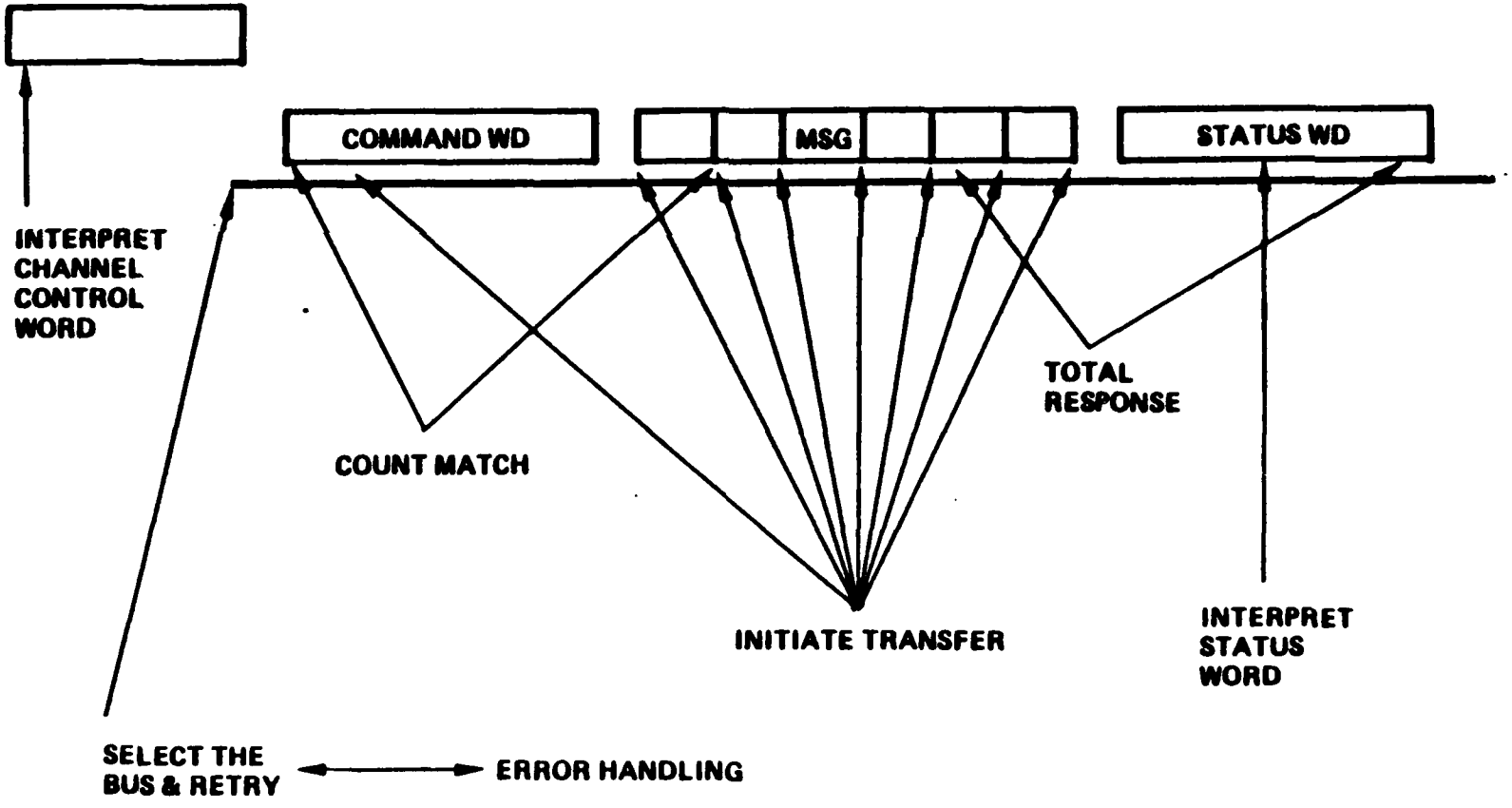


Bus Control Software

BIU Physical Interface Control Functions



BIU Physical Interface Control Functions



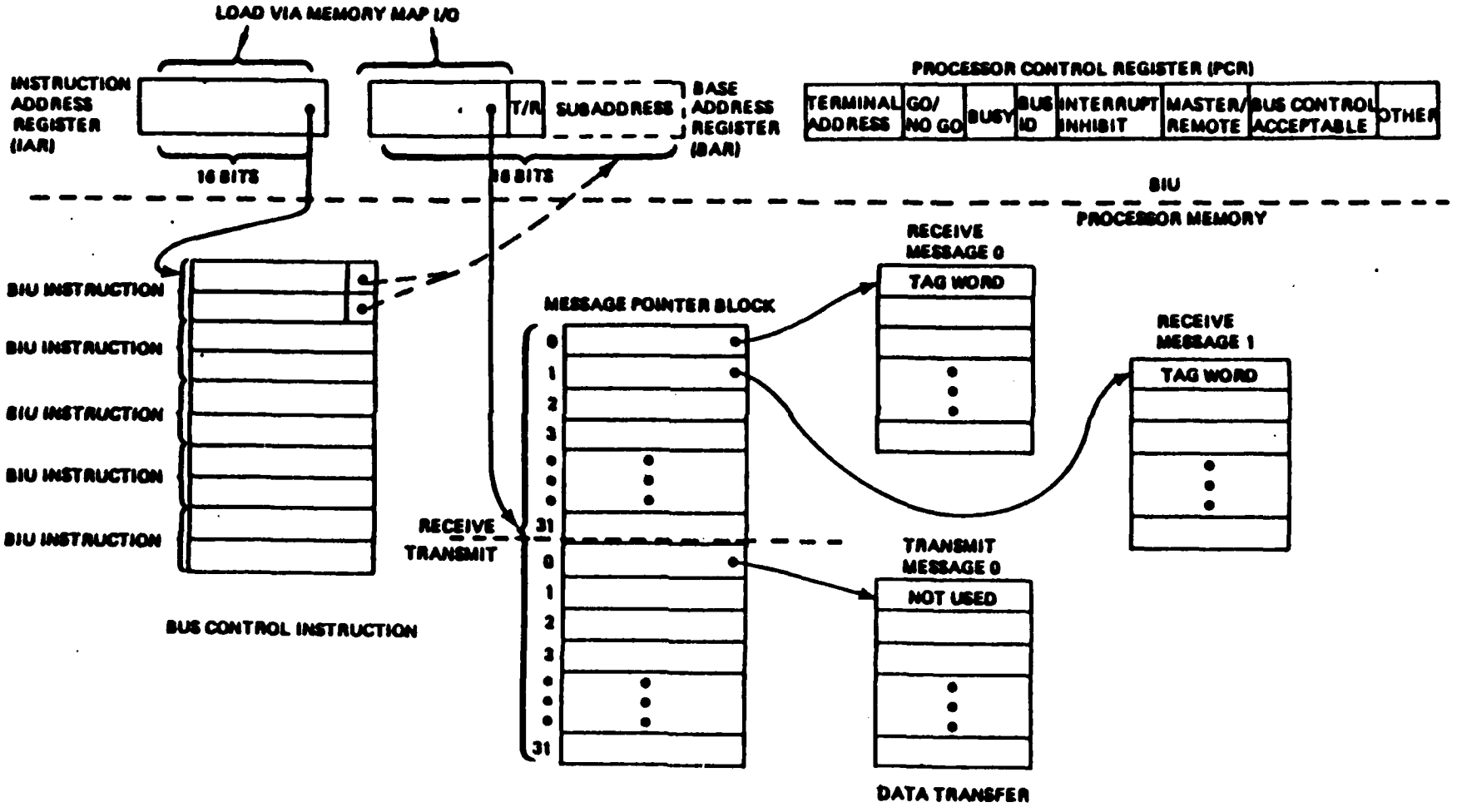


Figure 5.5-1. BIU/Processor Interface

SYSTEM CONTROL PHILOSOPHY

INITIALIZATION

- USE ADDRESS IDENTIFICATION DISCRETES TO IDENTIFY POSITION
- INDIVIDUAL POWER CONTROL OVER SUBSYSTEMS CAN BE USED
- BACKUP PROCESSOR CONTENDS FOR BUS CONTROLLER
- MASS MEMORY OVER THE BUS SHOULD BE USED SPARINGLY

NORMAL OPERATION

- DON'T USE DYNAMIC BUS ALLOCATION
- SYNCHRONIZE ALL BUSES TOGETHER, INCLUDING HIERARCHICAL
- SYNCHRONIZE USING COMMON CLOCKS FOR EXACT TIMING
- SYNCHRONIZE USING MODE CODES FOR CLOSE TIMING
- USE CHAINED CHANNEL CONTROL WORDS
- USE COMMON COMPUTERS

SYSTEM CONTROL PHILOSOPHY

ERROR MANAGEMENT

- o USE PASSIVE FAILURE MODE
- o USE CONTROL DISCRETES FOR ACTIVE/STANDBY PROCESSORS
- o CHANGE RT ADDRESS IF IT CHANGES IDENTITY

SHUTDOWN

- o COORDINATE TO AVOID RECONFIGURATION
- o SYSTEMS SHUTDOWN SUBSYSTEMS

BUS CONTROL SOFTWARE PHILOSOPHY

INITIALIZATION

- o USE DISCRETES TO DETERMINE IDENTITY (NEED TO ESTABLISH ADDRESS)
- o USE SELF TEST TO DETERMINE VALIDITY OF TERMINALS
- o MAKE CERTAIN LOAD MATCHES IDENTITY
- o USE MEMORY CHECKSUM TO DETERMINE COMPLETE LOAD

NORMAL OPERATION

- o ADJUST MESSAGE POINTER TABLES BASED ON MINOR CYCLE RECEIPT
- o USE CYCLIC COMMUNICATIONS
- o USE CHAINED CHANNEL CONTROL WORDS
- o DISPATCH TASKS BASED UPON MINOR CYCLE RECEIPT
- o POSTPONE ASYNCHRONOUS MESSAGES UNTIL AFTER NORMAL TRAFFIC
- o USE A SUBADDRESS FOR SYSTEM COMMUNICATION WHICH CAN INTERRUPT PROCESSOR

BUS CONTROL SOFTWARE PHILOSOPHY

ERROR MANAGEMENT

- o BUS ERROR -
  - RETRY OPPOSITE BUS ONCE
  - TALLEY FAILURE
  - STAY WITH BEST BUS

- o DEVICE ERROR
  - DETECT FAILURE
  - DEFER TO (USER DEFINED) SYSTEM MANAGEMENT FOR RESOLUTION
  - ELIMINATE FROM COMMUNICATION LISTS
  - PERIODICALLY TEST COMMUNICATION
  - RESTORE AFTER LONG PERIOD OF VALIDITY (MAYBE)

SYSTEM SHUTDOWN

- o BUS CONTROLLER IS LAST TO SHUTDOWN

BIU CONTROL PHILOSOPHY
OR
"LET THE HARDWARE DO THE WORK"

INITIALIZATION

- o USE BIU'S THAT HAVE CHANGEABLE ADDRESSES
- o USE CAPABILITY TO LISTEN TO BUS
- o USE BIU TO BIU TIME COMMUNICATION

NORMAL OPERATION

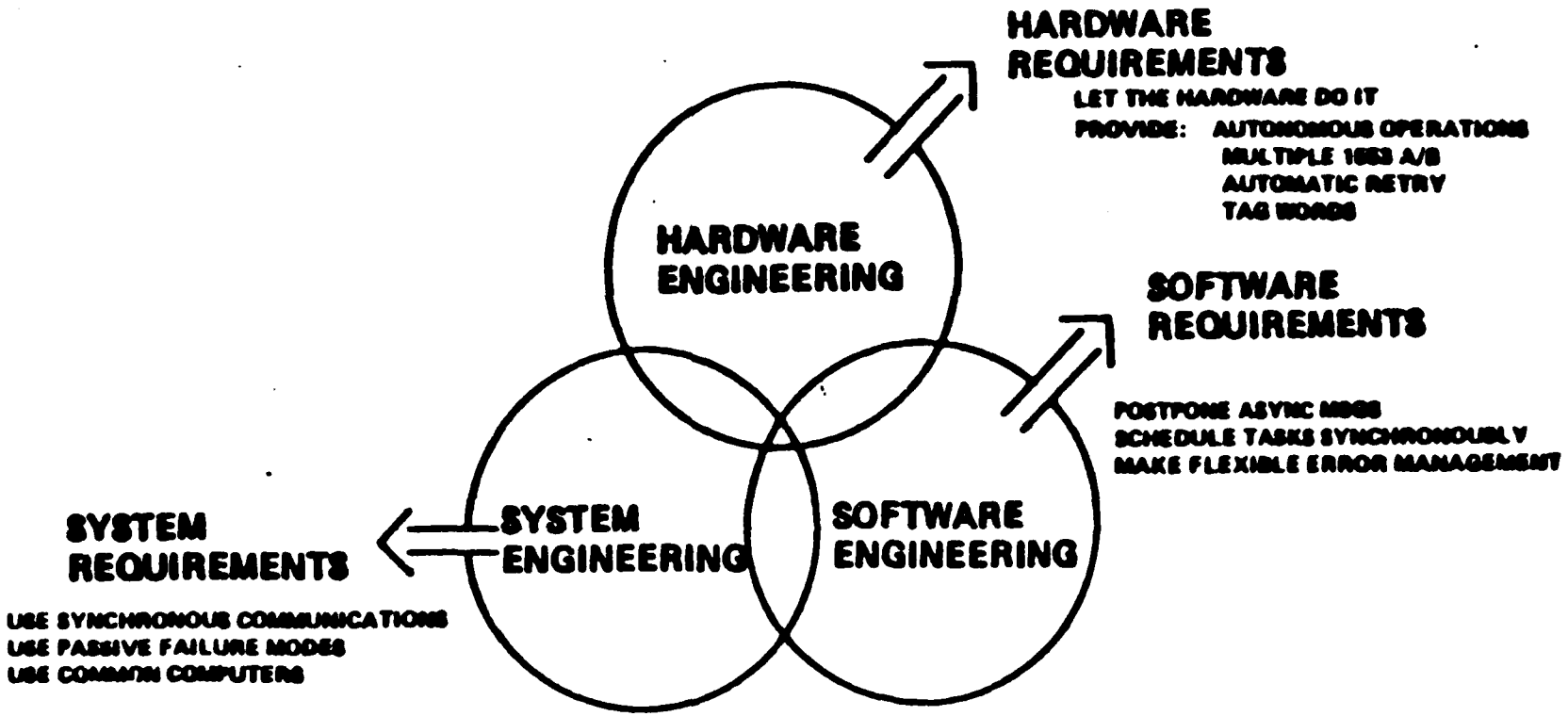
- o USE CHAINED I/O
- o USE MULTIPLE 1553A/B CONTROL IF APPLICABLE
- o PROVIDE TAG WORDS INDICATING VADILITY, TIME
- o PROVIDE FOR PRIORITY ASYNCHRONOUS MESSAGES
- o PROVIDE A WINDOW INTO WHERE THE BIU IS EXECUTING
- o PROVIDE FOR MULTIPLE BUFFERING AND CHANGE OF SUBADDRESS MEANING

BIU CONTROL PHILOSOPHY

ERROR MANAGEMENT

- PROVIDE AUTOMATIC RETRY ON SAME OR ALTERNATE BUS
- PROVIDE A MEANS OF MASKING OUT FAILURES AND INTERRUPTS
- PROVIDE A MEANS OF ELIMINATING COMMUNICATION WITH RT's
- PROVIDE EXCEPTION CHAIN CAPABILITY

Conclusion


HARDWARE REQUIREMENTS
LET THE HARDWARE DO IT
PROVIDE: AUTONOMOUS OPERATIONS
MULTIPLE 1553 A/B
AUTOMATIC RETRY
TAG WORDS
HARDWARE ENGINEERING
SOFTWARE REQUIREMENTS
POSTPONE ASYNC MSGS
SCHEDULE TASKS SYNCHRONOUSLY
MAKE FLEXIBLE ERROR MANAGEMENT
SYSTEM REQUIREMENTS
USE SYNCHRONOUS COMMUNICATIONS
USE PASSIVE FAILURE MODES
USE COMMON COMPUTERS
SYSTEM ENGINEERING
SOFTWARE ENGINEERING