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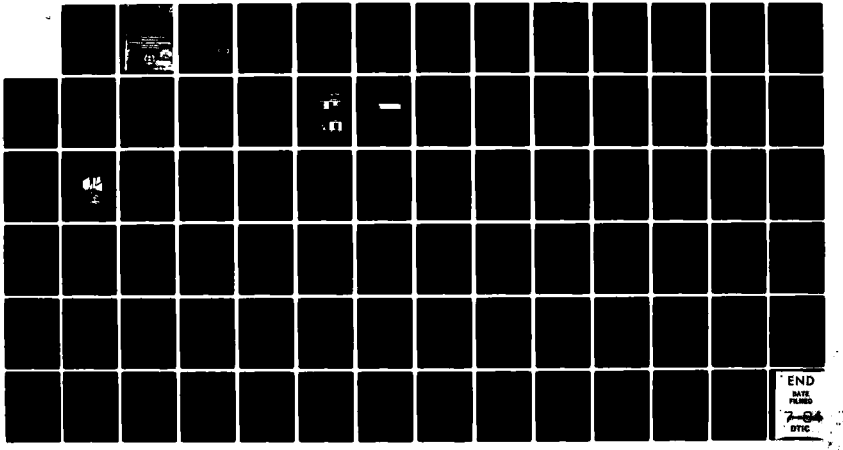

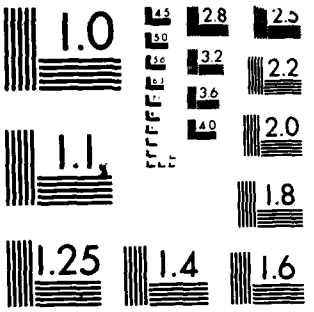

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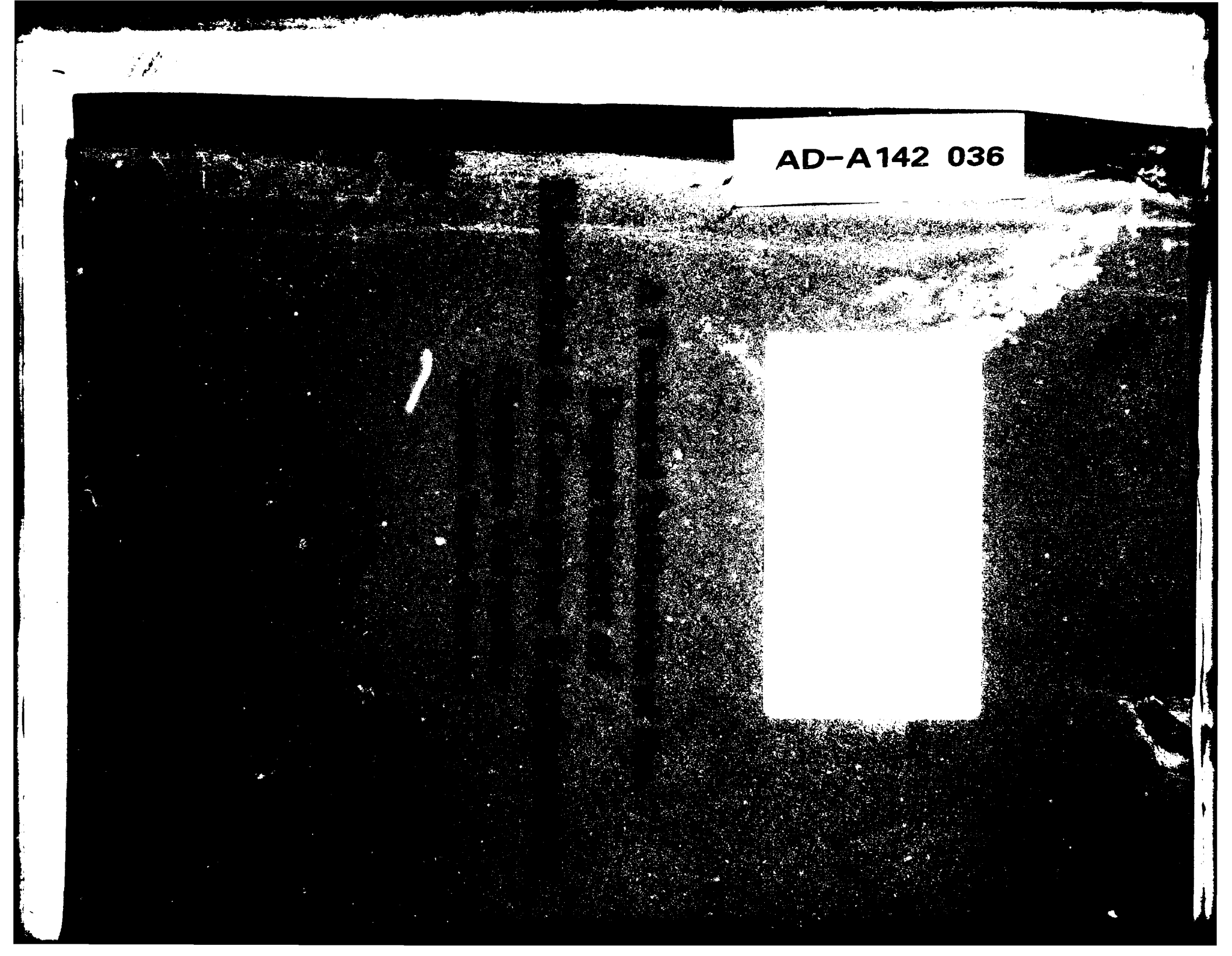

BALLISTIC TRANSPORT IN SUBMICRON SILICON MOSFETS

D. J. Dumin

Performed on Contract
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Office of Naval Research

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Recent improvements in the manufacturing of MOSFETs have reduced the minimum feature size and brought transistors with submicron geometries into being. For certain materials such as GaAs, gate lengths on the order of 0.2um are not comparable in length to the mean free path of the electrons in the channel at room temperature. It has been suggested that these electrons could cross the channel without suffering a collision, a

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phenomenon referred to as ballistic transport. For silicon devices the ballistic transport phenomenon might occur at cryogenic temperatures (4.2K) where decreased scattering results in high low-field mobilities.

We characterized submicron silicon MOSFET's down to 4.2K in the subthreshold, linear and saturation regimes. A 500um MOSFET was used as a comparison device. The measurements indicated that the effective channel mobility was inversely proportional to the ambient temperature, longitudinal field and transverse field. The channel mobility of a 500um MOSFET was measured to have a mobility as high as 25,000 $cm^2/V\text{-}s$ at 4.2K with Vds = 0.01 v. The mobilities of submicron transistors have been measured to be 800 and 1700 $cm^2/V\text{-}s$ at 4.2K for 0.2 and 0.7um MOSFET's respectively with Vds = 0.1 v. The operation of submicron MOSFET's with longitudinal fields on the order of those that were used in our 500um long MOSFET would require impractically small supply voltages. For example, a 0.2um device would require a drain-to-source voltage on the order of a few microvolts to operate with the same longitudinal field as a 500um device with Vds = 0.01 v. Voltages of this magnitude would not be compatible with existing technology due to noise margin limitations in digital circuits. Our experimental results indicated that ballistic transport cannot appear in silicon transistors operating at normal DC supply voltages due to scattering induced by high drain fields. Even in high mobility materials such as GaAs the high electric fields in submicron devices will keep the mean free path of the charge carriers shorter than the effective channel length. Therefore, ballistic transport should not have a large effect on the I-V characteristics of silicon or even GaAs MOS devices operating at DC voltages above a few tenths of a volt.

BALLISTIC TRANSPORT IN SUBMICRON SILICON MOSFETS

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Preface

This final report prepared by Clemson University under contract No. N00014-81-K-0347, describes research performed in the Department of Electrical and Computer Engineering, Dr. A. Wayne Bennett, department head.

The principal investigator was Dr. David J. Dumin. The graduate student working on the project was Mr. Perry J. Robertson. Transistors were manufactured by Dr. S. M. Sze and Mr. E. Labate at Bell Laboratories, Dr. Pallab K. Chatterjee at Texas Instruments, Mr. A. Ipri at RCA Laboratories and Nelson Saks at the Naval Research Laboratory. We also wish to thank Dr. Walter Kester at Analog Devices and Mr. Ron Waters at Harris Corp. for their assistance in bonding our chips. The assistance provided by these engineers is acknowledged and greatly appreciated.

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SECTION I

ABSTRACT

Recent improvements in the manufacturing of MOSFETs have reduced the minimum feature size and brought transistors with submicron geometries into being. For certain materials such as GaAs, gate lengths on the order of 0.2 um are now comparable in length to the mean free path of the electrons in the channel at room temperature. It has been suggested that these electrons could cross the channel without suffering a collision, a phenomenon referred to as ballistic transport. For silicon devices the ballistic transport phenomenon might occur at cryogenic temperatures (4.2K) where decreased scattering results in high low-field mobilities.

We characterized submicron silicon MOSFET's down to 4.2K in the subthreshold, linear and saturation regimes. A 500 um MOSFET was used as a comparison device. The measurements indicated that the effective channel mobility was inversely proportional to the ambient temperature, longitudinal field and transverse field. The channel mobility of a 500 um MOSFET was measured to have a mobility as high as 25,000 cm^2/V-s at 4.2K with Vds = 0.01 v. The mobilities of submicron transistors have been measured to be 800 and 1700 cm^2/V-s at 4.2K for 0.2 and 0.7 um MOSFETs respectively with Vds = 0.1 v. The operation of submicron MOSFETs with longitudinal fields on the order of those that were used in our 500 um long MOSFET would require impractically small supply voltages. For example, a 0.2 um device would require a drain-to-source voltage on the order of a few microvolts to operate with the same longitudinal field as a 500 um device with Vds = 0.01 v. Voltages of this magnitude would not be

compatible with existing technology due to noise margin limitations in digital circuits. Our experimental results indicated that ballistic transport cannot appear in silicon transistors operating at normal DC supply voltages due to scattering induced by high drain fields. Even in high mobility materials such as GaAs the high electric fields in submicron devices will keep the mean free path of the charge carriers shorter than the effective channel length. Therefore, ballistic transport should not have a large affect on the I-V characteristics of silicon or even GaAs MOS devices operating at DC voltages above a few tenths of a volt.

SECTION II

INTRODUCTION

Ballistic transport of electrons in submicron semiconductor devices has been the subject of many technical articles for several years. In these papers, considerable speculation concerning the possibility of observing ballistic transport in such devices. The majority of the theoretical models predict ballistic transport if a small device is operated at sufficiently low fields. Very little has been published concerning any experimentation that has been performed to determine if the ballistic effect can be observed either at room temperature or at very low temperatures (77K to 4.2K). At low temperatures charge scattering will be reduced, thus increasing the channel mobility and enhancing any ballistic characteristic(1). We have attempted to provide an experimental base of knowledge with which we may determine if ballistic effects appear in the silicon device characteristics at low temperatures. Our velocity-field data indicates that observation of ballistic transport in field effect transistors made on nominally high mobility materials such as GaAs will only be observable at impractically low drain voltages.

SECTION III

BALLISTIC TRANSPORT

In the past few years there has been a marked reduction in the minimum line definition achieved in the microelectronic industry. This has brought the minimum size of MOS transistors down below the 0.1 um limit. Line widths of 25.0 nm are now possible due to the development of direct write-on-wafer e-beam technology coupled with better fine definition photo resist polymers(2). Modifications in the photo resist process and structure have resulted in even smaller line widths(3).

As the device sizes shrank, it was suggested by Shur and Eastman that the effective channel length of these new submicron transistors might approach a size comparable to the mean free path of the charge carriers in the channel(4). This would bring the transit time of these carriers down to the limit of the time between collisions. Thus, there would be the possibility that electrons could be accelerated across the channel and be collected at the drain without suffering a collision event. Such an event has been termed "Ballistic Transport".

Ballistic transport has become the subject of many technical papers especially for those authors interested in the operation of GaAs devices. Because of its band structure and high mobility at room temperature, GaAs has long been considered the material which holds the most promise in which to observe ballistic transport.

Many theories have been developed to explain how ballistic transport might affect the operation of submicron devices. Motion of electrons through a semiconductor in the presence of a uniform field and in the absence of any collisions would be governed by(5)

$$Vs = \frac{q\ E\ t}{m^*}$$

where

Vs = effective velocity (cm/s)

q = electron charge

E = magnitude of the electric field (v/cm)

t = transit time

m^* = effective mass.

This equation of operation has been used along with statistical methods to develop many models to simulate the operation of a ballistic device. Most of these methods involve a Monte Carlo simulation of the ballistic process using various device structures and doping densities(6-12). But very little information has been published describing the results of experimental work performed in this area. Most of this work has been performed using two-terminal GaAs diode structures(4)(13-15). Very little has been published relating to the possible occurrence of ballistic transport in silicon MOSFET devices either at room temperature or at cryogenic temperatures. Part of the purpose if this paper is to extend the information available in this area especially considering the dominance of silicon devices in the industry

SECTION IV

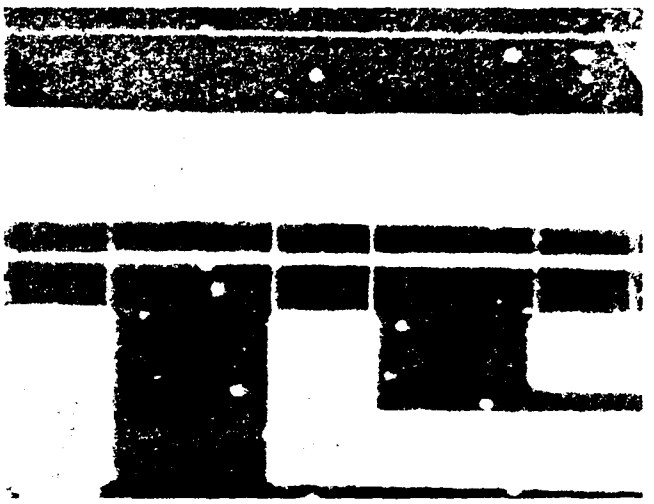
TRANSISTOR DESCRIPTIONS

Several sets of NMOS transistors were used as test devices in this project. They were chosen for their availability, submicron size and device type. We used some of the smallest experimental transistors presently available. All were silicon, NMOS transistors of various configurations.

BTL Transistors

The smallest and most useful devices were the transistors manufactured by Bell Telephone Laboratories (BTL) and made available to us by Mr. E. Labate and Dr. S. M. Sze of the Advanced LSI Development Laboratory in Murray Hill, New Jersey. Micrographs of the BTL transistors are shown in Figures 1 and 2. We concentrated our testing on these transistors because each die contained several different devices of differing gate lengths on the same die. In addition, the other devices (from RCA and TI) were experimental and lacked the uniformity we have observed in the BTL devices. The BTL devices we tested were manufactured using the modified NMOS process reported by W. Fichtner et al(16)(17).

The BTL transistors were N-channel, enhancement mode devices with channel dopings of approximately $1X10^{7}$ cm^{-3}. The gate oxide thickness was measured to be 28.0 nm. These devices were configured with



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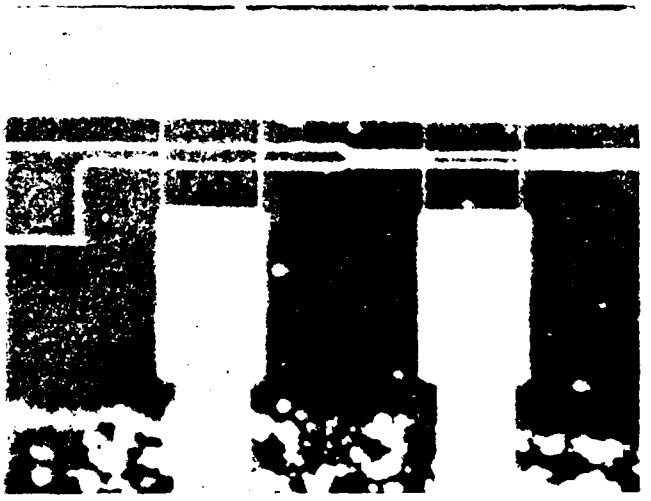

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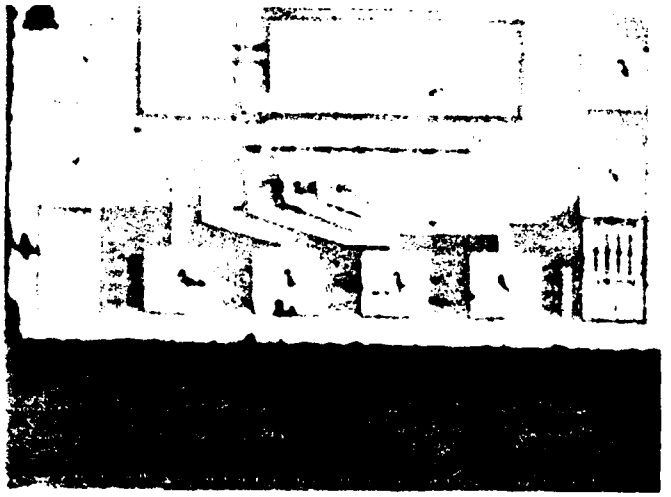
Figure 1. 500X Micrograph of BTL 0.2, 0.7, 1.2 and 1.7um Transistors.



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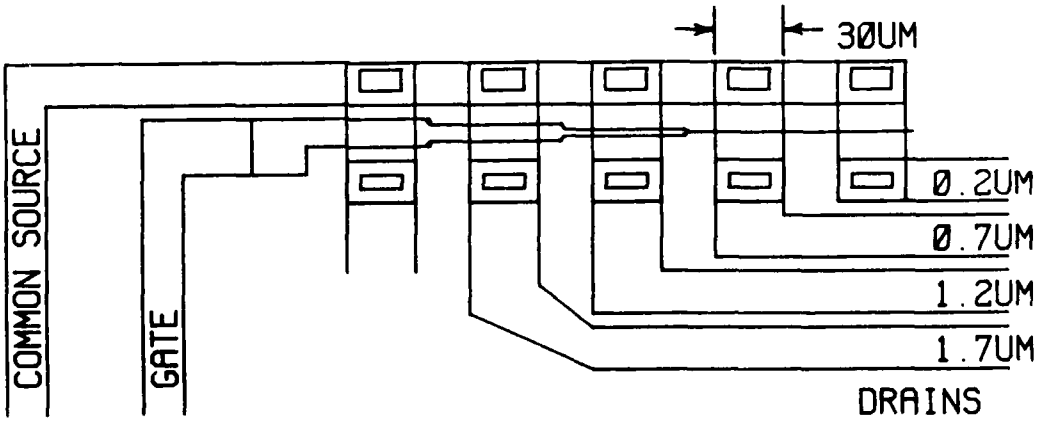


(b)

Figure 2. a) 40X Micrograph of the BTL Chip. b) BTL Transistor Geometry.

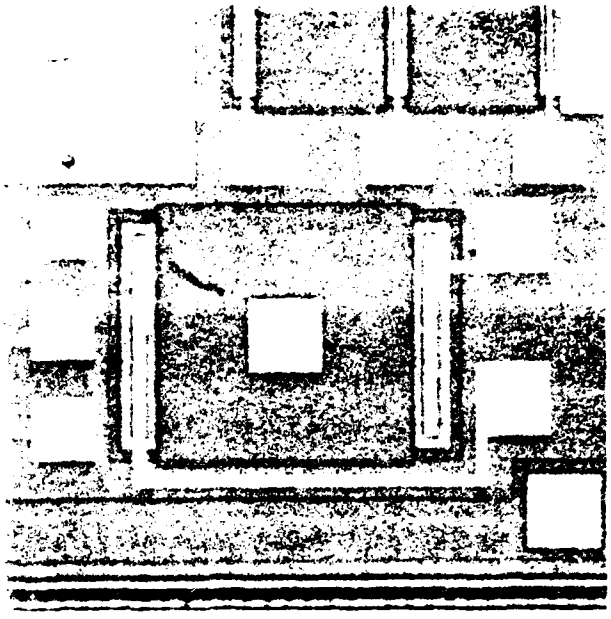
a common source and common gate and a separate drain for each device. Direct write e-beam lithography was used to define gate lengths varying from 1.0 um to 30 um. Each transistor was 30 um wide. The effective gate lengths for each device were found to be 0.8 um less than the actual lithographic gate lengths by using the method described by John G. J. Chern et al 1980(18). The effective gate lengths used for characterization were 0.2, 0.7, 1.2 and 1.7 um respectively.

Eight of the chips received from BTL were bonded into 18 pin DIPs by R. S. Waters, Director of CMOS Design, Harris Corp., Melborne, Fla. Of the original eight die, three survived bonding in good enough condition to be tested. These transistors are referred to in this report as BTL#1, BTL#2 and BTL#4.

The modified NMOS process used to manufacture the BTL transistors was developed to produce transistors with gate lengths approaching 0.15 um which would retain an electrically long channel characteristic(19), that is, they did not suffer from traditional short channel effects as described by S. M. Sze(20, pp. 469-486). None of the transistors used in this project exhibited short channel characteristics.

Long Channel Comparison Device

A 500 by 500 square um, long channel, NMOS, silicon transistor was provided by Nelson Saks of the Naval Research Laboratories (NRL). The sample, designated as CCD 4-5/1-H6, was produced on a P-type, 15 ohm-cm silicon substrate. It had a phosphorus doped, polysilicon gate



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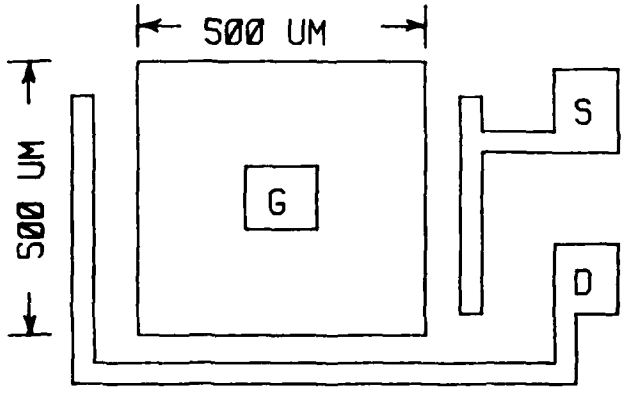


(b)

Figure 3. a) Micrograph and b) Geometry of the T500X500 Transistor.

grown over and 85 nm gate oxide. The gate was not self aligned. This transistor is referred to as T500X500 in this report. The geometry of this transistor is shown in Figure 3.

This long channel, wide transistor was used as a comparison device. It proved to be a very interesting device having very high effective mobilities, especially at lower temperatures.

Tests of a similar 500 X 500 um transistor referred to as T500X500/I5 were performed by Nelson Saks at NRL. The results of his tests were used, with his permission, for comparison with our tests at low temperatures.

Other Transistors Tested

Two other sets of transistors were intitially tested for use in this project. We have not concentrated on analyzing the results of these tests due to the erratic nature of the data.

One transistor was a silicon-on-sapphire, NMOS device manufactured by RCA and provided by A. Ipri of RCA Labs, Princeton, New Jersey. This transistor had a gate oxide 8.0 nm thick and a channel doping of $3X10^{17}$ cm^{-3}. It was manufactured on a ⟨100⟩ silicon substrate and came from lot number 4752. We tested the transistor designated as DC3. In this report, this device is referred to as RCA 4752.

The last two transistors were provided by Dr. Pallab K. Chatterjee, Manager of VLSI Design, Texas Instruments, Inc. These transistors had a gate length of approximately 0.3 um and a gate oxide 8.0 nm thick. These devices were 2.0 um wide. The channel was doped at $1.2X10^{17}$ cm^{-3}. The two transistors used from this lot are referred to as TI 34-8/C9 R3 and TI 34-8/C8 R3.

SECTION V

DEWAR DESIGN AND CONSTRUCTION

A. Overview

A double walled, two-stage helium dewar was constructed in order to make measurements on the test transistors at temperatures down to and including 4.2K. The equipment had to be configured to allow the progressive insertion and removal of the transistor under test while providing electrical connections to the device. At the same time the opening of the dewar had to be closed to insure the integrity of the temperature gradient within the inner helium dewar and to prevent ice formation on the device. An automatic drive mechanism was used to provide computer control over the insertion and removal of the device under test. Problems with the measurement of very small currents using the ISAAC A/D converter caused us to scrap the automatic test environment. It should be mentioned, however, that the drive mechanism, circuitry and computer control worked very well.

In order to insure an accurate measurement of the device's ambient temperature a custom designed circuit using a resistance temperature detector (RTD) was developed. This circuit could accurately measure the ambient temperature down to 77K, the temperature of liquid nitrogen. Tests made at 4.2K were performed with the device submerged in liquid helium at atmospheric pressure. No measurements were made between 77K and 4.2K therefore it was not necessary to know the exact temperature between these two points. We were able to use the ISAAC A/D and the Apple computer to read and record the test temperatures.

A vacuum pump was provided to draw a moderate vacuum on the space between the inner and outer walls of the helium dewar. This greatly reduced the heat flow to the liquid helium inside leaving the surface of the helium quiescent.

B. Helium Dewar

The helium dewar consisted of two, double-walled dewars, one inside the other as shown in Figure 4. The outside, nitrogen dewar was placed inside a plywood frame for protection and support. A slot in one side provided for viewing of the liquid levels within both dewars. The entire inside of both dewars was silvered with the exception of opposing slits which ran the length of the dewars. Large holes drilled on the back side of the plywood support allowed light to be shined into the dewars for better viewing. A picture of the support is shown in Figure 5. The plywood support was 10 inches square. The outer nitrogen dewar was 7 inches in diameter and the inner helium dewar was 4 inches in diameter. The top of the platform stood approximately 40 inches off the floor.

The inner helium dewar was attached via six bolts and a locking ring to a square, quarter-inch thick brass plate, 12 inches on a side. This plate was mounted to a plywood board which was mounted atop the plywood support. This left the inner dewar suspended within the outer dewar within about two inches of its bottom. The brass plate served as a mounting plate for other parts of the test apparatus.

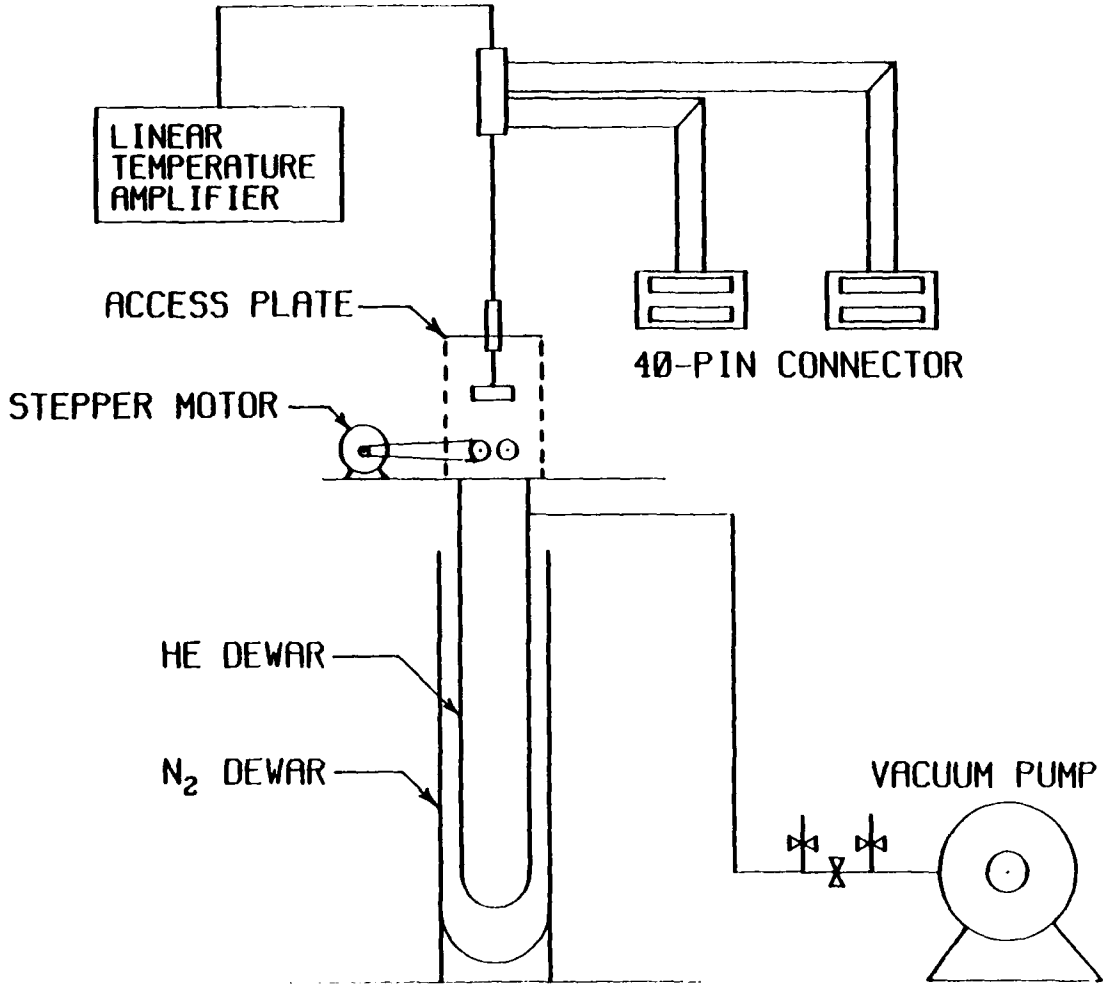


Figure 4. Double Dewar Low Temperature Test Apparatus.

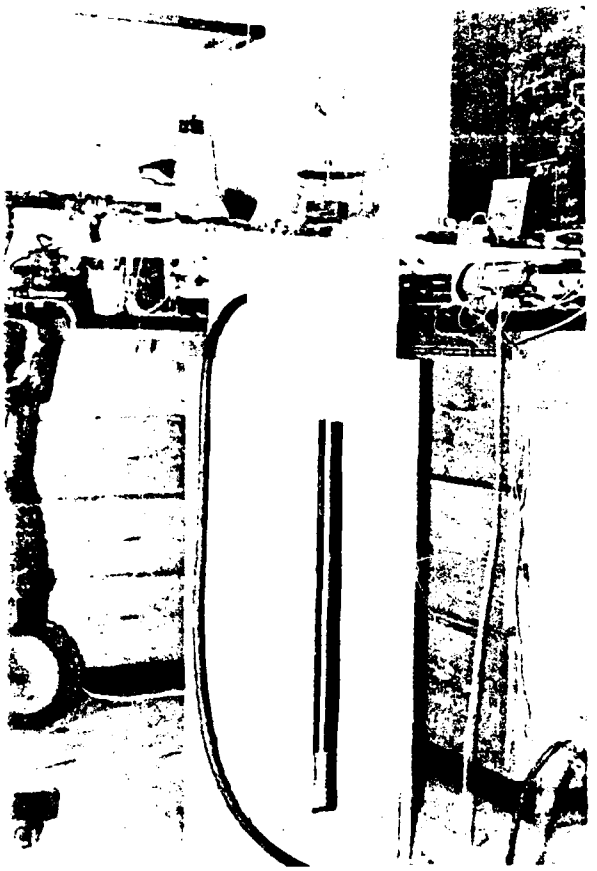


Figure 5. Plywood Support for Nitrogen and Helium Dewars.

A small square hole cut in the plate provided access to the dewar. The space between the inner and outer dewars was filled with liquid nitrogen. A square hole cut in the wooden support provided both a place to pump in the nitrogen and to attach the vacuum line to the inner dewar.

Vacuum Pump

It was necessary to draw a vacuum on the space between the inner and outer walls of the inner helium dewar to reduce helium boiloff during testing. Three valves allowed selective venting of the vacuum pump and the helium dewar to the atmosphere. A thick-walled rubber hose connected the dewar to the value assembly.

C. Access Plate Assembly

A round, 1/4-inch thick brass plate, 3/4 inch in diameter was used to cover the opening of the helium dewar. Four mounting holes allowed the plate to be mounted over four 1/4-inch studs and to be securely attached to the large plate. Figure 6 shows the access plate assembly and brass mounting plate. Note that the studs are not in place in this picture. A Swaglock fitting allowed a 4-foot long, 3/8-inch diameter thin-walled stainless steel tube to pass through the plate. The tubing carried 40, 30-gauge solid copper wires between the upper connector and the DIP socket mounted to the end of the tube. The DIP socket was arranged to allow testing of devices mounted in DIPs either 0.3 inches or 0.6 inches wide having up to 40 pins.

Figure 6. Access Plate Assembly and Brass Mounting Plate. Forty-pin Connector is Under the Brass Plate.

In addition to the other wires already mentioned, a twisted pair of copper wires were run down the tube to connect the RTD to the amplifier for temperature measurement. Electrical connections between the connectors at the top of the stainless steel tube and the 40 screw terminals were made using two, 20-conductor flat cables.

D. Stepper Motor

A stepper motor, drive circuitry and drive wheel were mounted to the large brass plate so that the process of lowering and raising of the device under test could be automated. The high torque stepper motor is powered from a 5-volt, 3-Ampere power supply and controlled by a K33505 controller board. Both were manufactured by Airpax. The stepper motor was used to control the depth of the device carrier when connected to a computer D/A converter such as the Apple/ISAAC system. Switches were provided for manual operation.

E. Temperature Measurement

The ambient temperature of the device under test was measured using a circuit especially designed by us for use with this system. The temperature was determined by the change in resistance of a 100 ohm, platinum Resistance Temperature Detector (RTD) manufactured by Omega Engineering. When used with a linear amplifier, the temperature could be accurately measured from 77K to 400K.

The gain and offset of the amplifier were adjusted so that 4.5 volts at the output corresponded to 77K and 0 volts corresponded to 237.14K as shown in Figure 7. Linearity over this range of temperature was very good.

Measurements at 4.2K were made with the test device completely submerged in liquid helium at atmospheric pressure. No measurements were made between 4.2K and 77K where the accuracy of the temperature measurement could not be insured.

A twisted pair of wires connected the RTD to the amplifier. This pair was routed down the inside of the 3/8 inch stainless steel tube. The RTD was mounted under, and in intimate contact with, the device under test. In this way, a close measure of the device's temperature could be maintained.

The output voltage of the amplifier was displayed on a HP 34703A Multimeter and the temperature was calculated using the formula

$$T = -43.6\ V + 273.14$$

where V is the output voltage from the amplifier. A program was written to allow this measurement and calculation to be performed automatically using the Apple/ISAAC A/D converter.

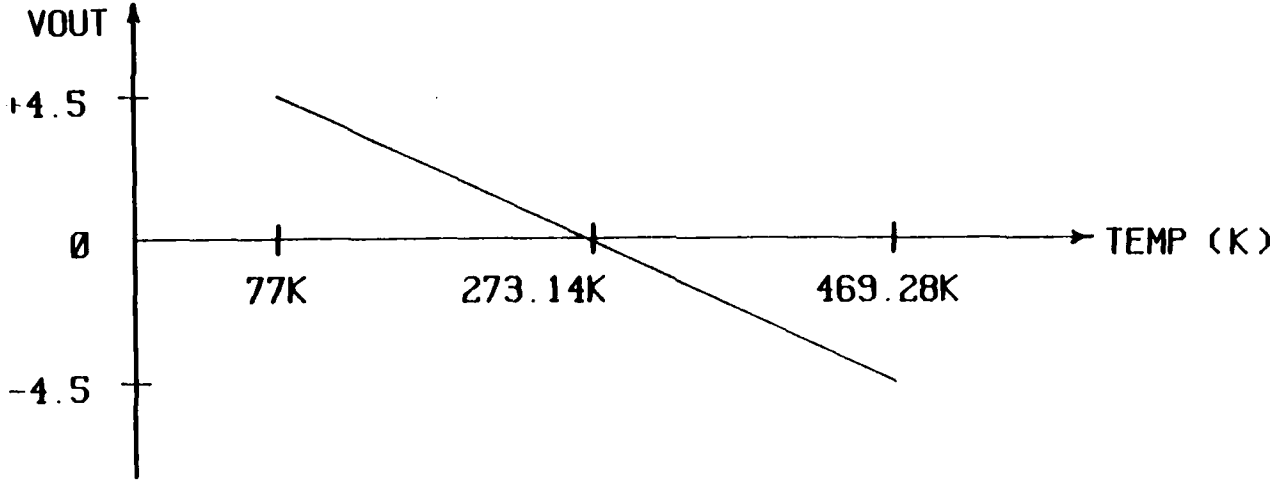


Figure 7. Output Voltage Vs. Input Temperature for Linear Temperature Amplifier.

F. Liquid Nitrogen and Liquid Helium

For tests at temperatures down to 77K, liquid nitrogen was pumped from a 30-liter tank. The inner dewar was filled to about 1/2 full capacity. The outside dewar was then filled with liquid nitrogen.

At first, liquid nitrogen was put in the inner dewar alone and no vacuum was pulled on the inner dewar. This condition lead to considerable nitrogen boil-off. The boil-off was reduced greatly by applying a vacuum to the inner dewar and filling the space between the inner and outer dewar with liquid nitrogen.

For tests down to 4.2K, liquid nitrogen was placed between the inner and outer dewars and a vacuum was pulled on the inner dewar. Liquid helium was pumped from a 100-liter storage tank through a vacuum transfer tube into the inner dewar. The transfer continued until the dewar was about half full. Once the inner dewar was filled, the access plate was locked in place to reduce the condensation of air within the dewar.

SECTION VI

TRANSISTOR MEASUREMENTS

A. Automatic Test Environment

At the outset of the project, we realized that the extensive testing that would be required to measure the subthreshold, linear and saturation characteristics of many transistors over a temperature range from 300K to 4.2K would be very labor intensive. The wait periods between temperature measurements would be especially time consuming. These delays were necessary to allow the temperature of the device to settle to an equilibrium value. In addition, we thought that the large amount of data generated in these tests could be best handled if it were automatically stored on floppy disk at the time it was acquired. These two overriding factors, time and data, lead us to develope an automatic test environment which consisted of an Apple II+ computer interfaced to an ISAAC A/D and D/A data acquisition system. This combination allowed the tests to run with minimal human intervention.

Extensive effort was put into development of computer programs at the beginning of the project. This was during the time that the helium dewar was being built and the transistors were being readied for testing. One program was designed to perform the tests. The other program was used to analyze the data. Both of these programs were highly successful. The problems that caused us to drop the automatic testing were hardware related.

The major problem accured when trying to use the ISAAC A/D converter to measure very small currents. The ISAAC system has a 12-bit A/D converter with a stated accuracy of plus or minus 2.5

millivolts. Actual measurements indicated that this accuracy was closer to plus or minus 10.0 millivolts. This was not small enough to insure measurement accuracy of currents on the order of a few micramperes.

In addition, The ISAAC A/D converter only measures voltage. Therefore, any measurement of current had to be a measurement of the voltage drop this current caused as it passed through a known resistance. Many problems occurred while trying to measure the voltage across a resistor in the drain leg of a MOSFET. If the power supply was not adjusted as the drain current (Ids) increased, the drain-to-source voltage (Vds) would decrease ruining the measurement. Many circuits were designed in an attempt to avoid this problem but they all suffered from measurement accuracy due to the A/D converter problems mentioned before.

Log Amplifiers

Measurement of subthreshold currents was especially difficult because of the small currents involved (1 nA to 1 mA). These currents varied over several decades, where as the ISAAC A/D converter inputs are limited to a rather narrow -5.0 volt to +5.0 volt range.

We attempted to measure the subthreshold currents by interfacing an Analog Devices 755N Logarithmic Amplifier to the ISAAC A/D converter as shown in Figure 8. Using the log amplifier, we could effectively compress the current range into the required voltage range by taking the log of the current and find the actual current magnitude using the inverse log relationship.

Implimentation of the log amplifier was not completely successful for two reasons. First, the amplifier was not linear over the required 6 decades. Second, ground loop problems prevented accurate measurement of the output voltage by the ISAAC A/D converter.

Test Equipment

With the automatic test environment rejected, we proceeded to make the required measurements using the most accurate ammeter and voltmeter we had available. Additional measurements made in the linear region were performed using a Tektronix 576 Curve Tracer. Current and voltage measurements were made using a Keithley 614 Electrometer. The electrometer was used to make current measurements in the subthreshold region in the range from 1 nA to 1 mA. The HP 3468A Multimeter was used to make current measurements in the linear and saturation region down to 10 uA.

When the curve tracer was used to record the linear characteristics of our transistors, Ids vs. Vgs measurements were made using a photograph of the Ids vs. Vds family of curves for the device in the linear regime.

B. Subthreshold Regime

Measurements of the subthreshold characteristics of our test transistors were made using the circuit shown in Figure 9. The gate voltage was measured using the HP 3468A Multimeter. The drain-to-source current was measured using the Keithley 614 Electrometer.

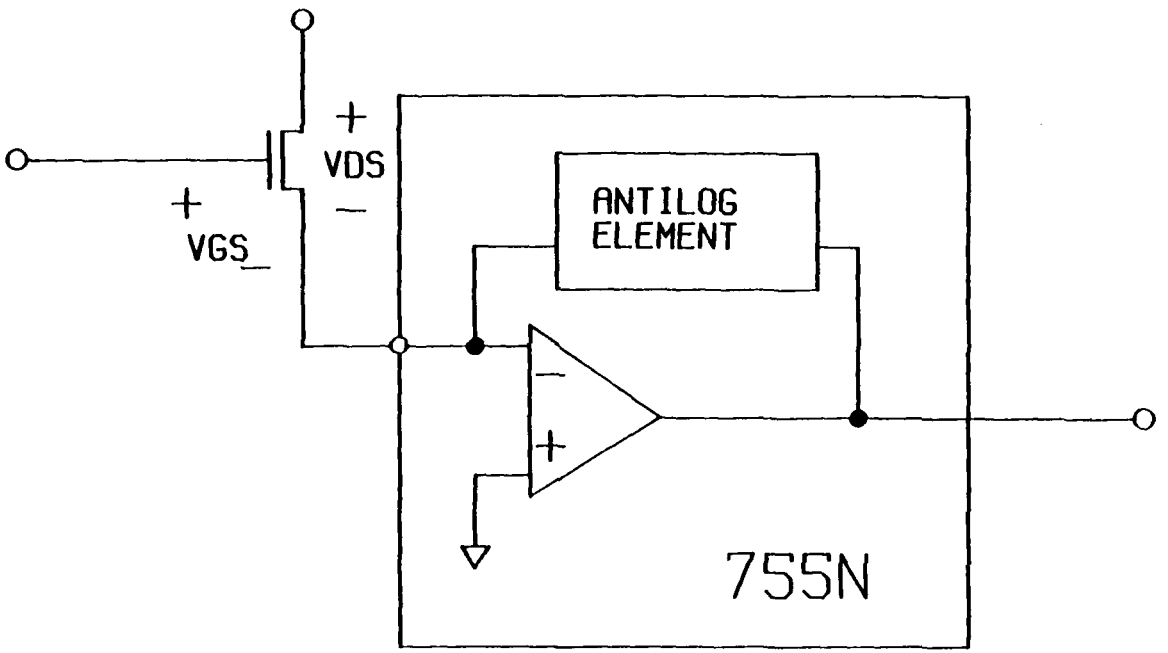


Figure 8. Test Circuit for Subthreshold Test Using an Analog Devices 755N Log Amplifier.

Test Procedure

At each test temperature, with the device turned on (Vgs = 3.0 volts), the drain supply was adjusted to set the drain-to-source voltage (Vds) to 0.01 volts. Vgs was then changed from 0.0 volts to 5.0 volts while the drain-to-source current, (Ids), was measured at each point. This data was used to produce a graph of Log(Ids) vs. Vgs for each transistor. This curve is sometimes referred to as the turn-on characteristic of the device.

C. Linear Regime

Measurements of the drain characteristics of the test devices in the linear regime were performed in one of two ways; either the data was taken directly from the curve tracer as shown in Figure 10(b) or measurements were made using the circuit shown in Figure 9.

Curve Tracer

When the Tektronix 576 curve tracer was used, data was taken from a photograph of the curve tracer display. The data must be read from a family of curves as shown in Figure 10(a). The circles indicate the data points that would be used to produce a plot of Ids vs. Vgs for Vds = 0.1 volts.

The circuit for making curve tracer measurements is shown in Figure 10(b). The leads from the screw terminals attached to the device under test in the dewar were plugged into the appropriate terminals on the curve tracer. The horizontal scale was set to 0.05 volts/cm. The gate voltage step control was set to 2X step rate, 0.5

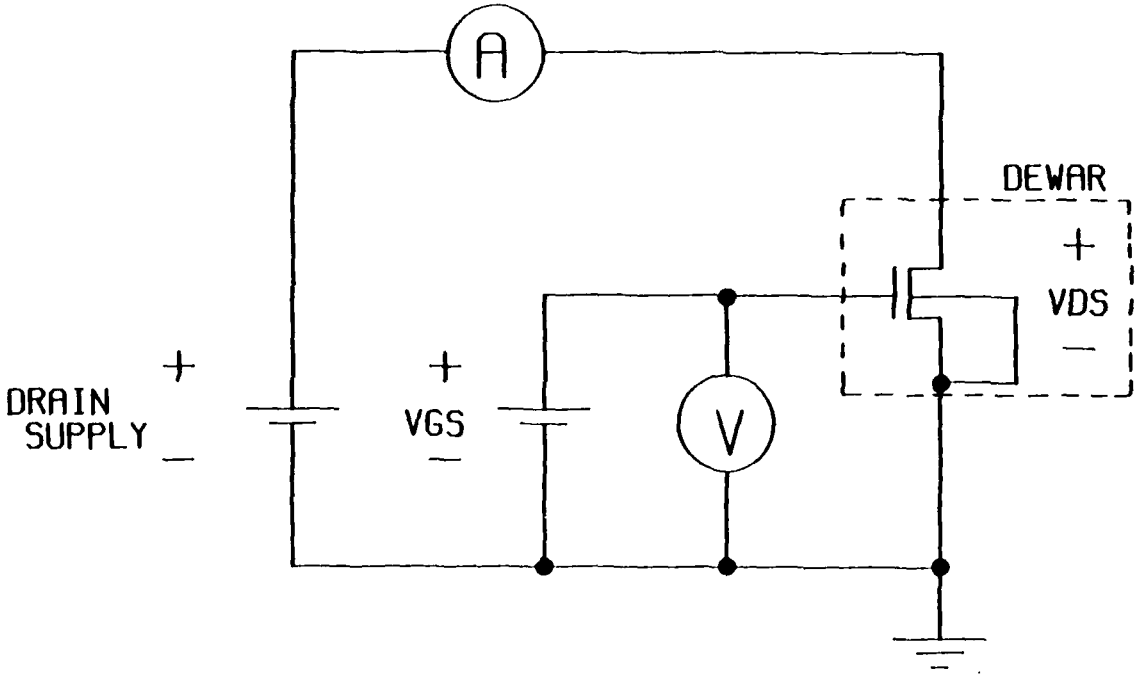


Figure 9. Test Circuit for Measurement of Ids Vs. Vgs for a Given Vds.

volts/step and ten steps. Thus, measurements were made for gate voltages from 0 to 5.0 volts at one half volt increments. The vertical current scale was set so that the entire family of gate voltage curves could be observed on the screen. Again, all linear measurements were made with Vds = 0.1 volts or Vds = 0.25 volts. Saturation and subthreshold measurements were not performed using the curve tracer.

Multimeter Test Circuit

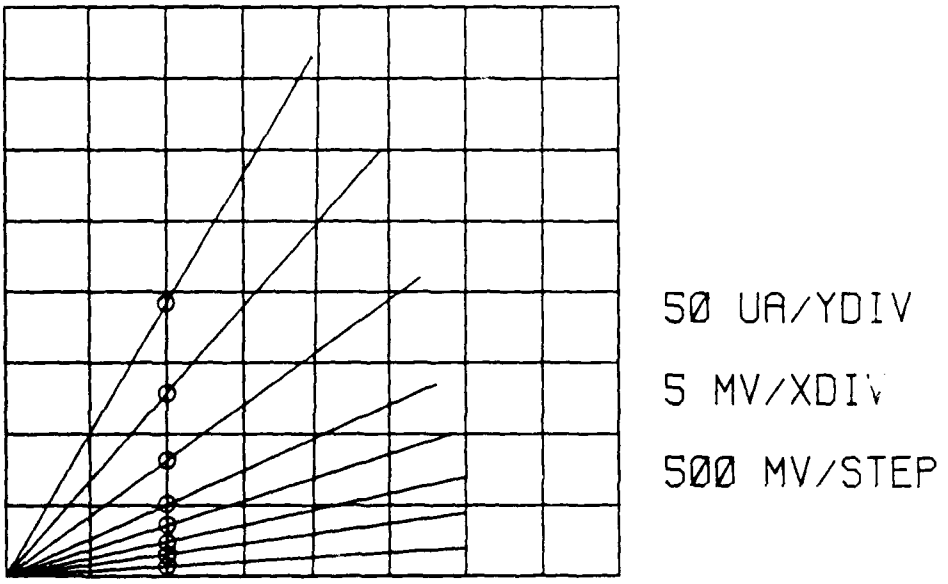
Some measurements in the linear regime were made using the circuit in Figure 9. The gate voltage was measured using the Keithley 614 Electrometer. The drain-to-source current was measured using the HP 3468A Multimeter.

In this configuration and with the transistor turned on (Vgs = 3.0 volts) the drain supply was adjusted until Vds equaled 0.1 volts. The gate voltage, Vgs, was adjusted from 0.0 volts to 5.0 volts while Ids was measured at each data point.

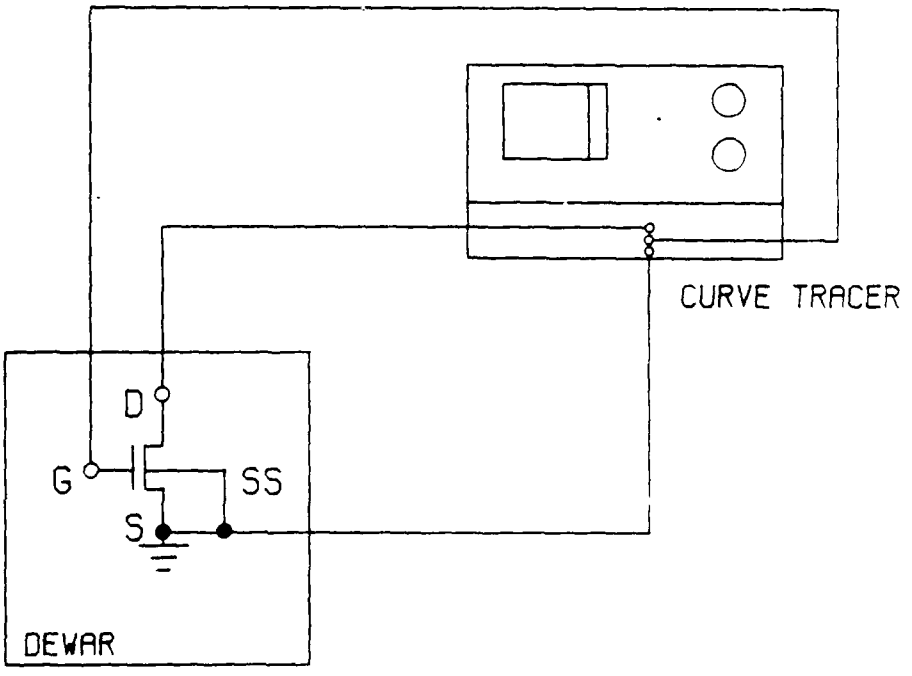
D. Saturation Regime

Measurements of the drain current characteristics in the saturation regime were made using the circuit shown in Figure 9. The gate voltage was measured using the Keithley 614 Electrometer. Drain-to-source currents were measured using the HP 3468A Multimeter in order to take advantage of its auto-ranging capabilities.

With the gate voltage set to 5.0 volts, the drain supply was adjusted until the drain-to-source voltage reached its test value (2.0 to 3.5 volts depending on the device under test). The gate voltage was then adjusted from 0.0 volts to 5.0 volts while the drain-to-source current was measured at each data point.



(a)



(b)

Figure 10. a) Curve Tracer Screen and b) Circuit for Measurements in the Linear Regime.

SECTION VII

RESULTS AND DISCUSSION

A. Subthreshold Characteristics

The subthreshold characteristics of our transistors were measured over a temperature range from 300K to 4.2K. Plots of Ids vs. Vgs are shown in Figures 11-18. The subthreshold (turn-on) characteristic is described by the subthreshold swing, S(mV/dec). Subthreshold swings for our transistors have been compiled in Table 1.

The subthreshold swing, S, increased with decreasing channel length for BTL#2 devices. Just the opposite characteristic appeared in the BTL#1 and BTL#4 devices. The subthreshold swing decreased in all devices as the temperature decreased. This leads to faster switching times and has led some authors to advocate the operation of devices at 77K especially for low power applications(21). For comparison, A. Kamgar reported a subthreshold swing of 92, 22 and 5 mV/dec for 300K, 77K and 4.2K respectively(22) in devices with a channel length of 8.0 um. These values compared favorably to our transistors at 300K and 77K but our devices had a much higher subthreshold swing at 4.2K. This is probably due to the fact that we did not take data at current values low enough to see the small subthreshold swing. Other authors have reported a saturation of the subthreshold swing for short channel transistors. Kamgar(23) reported subthreshold swings at 4.2K on the order of 10 mV/decade, still an order of magnitude larger than the calculated values.

Table 1. Subthreshold Swing of Tested Devices with Vds = 0.01 Volts.

Transistor	S(mV/dec) 300K	200K	77K	4.2K
T500x500		23	34	35
BTL#2 1.7um	70	33		21
BTL#2 1.2um	64	37		23
BTL#2 0.7um	72	41		36
BTL#2 0.2um	143	78		12
BTL#1 0.7um	82		33	
BTL#1 1.2um	140		20	
BTL#4 0.7um	137		23	
BTL#4 0.2um	70		22	

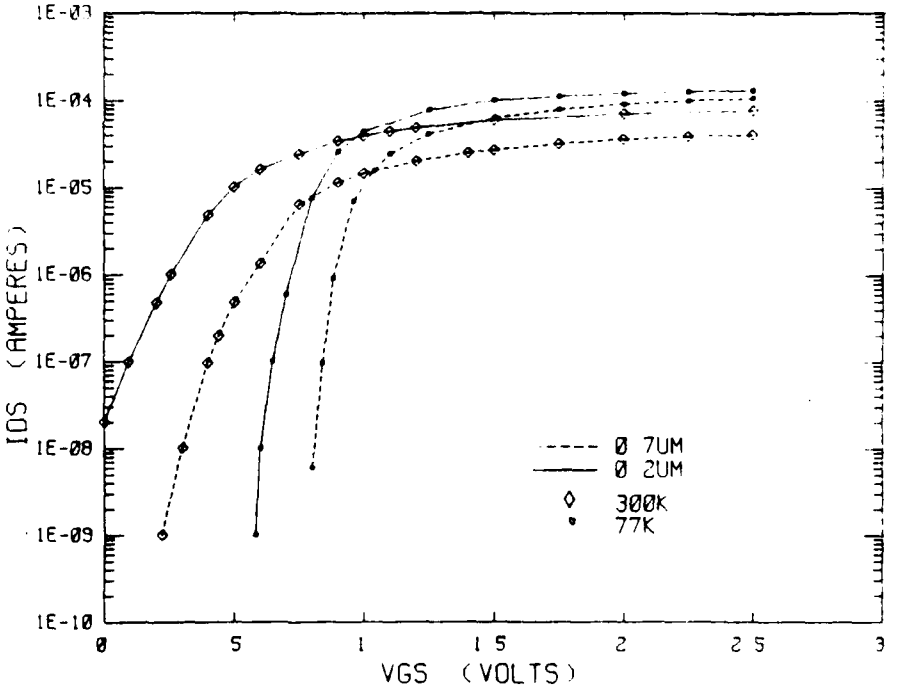


Figure 11. Subthreshold Characteristics for BTL#1 0.7um and 0.2um Transistors.

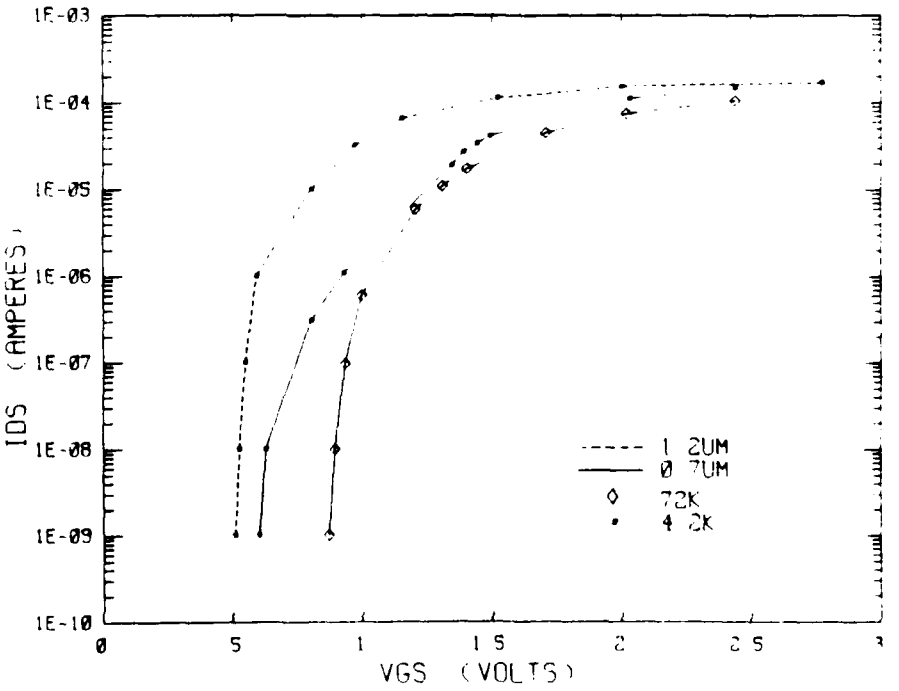


Figure 12. Subthreshold Characteristics for BTL#1 0.7um and 1.2um Transistors.

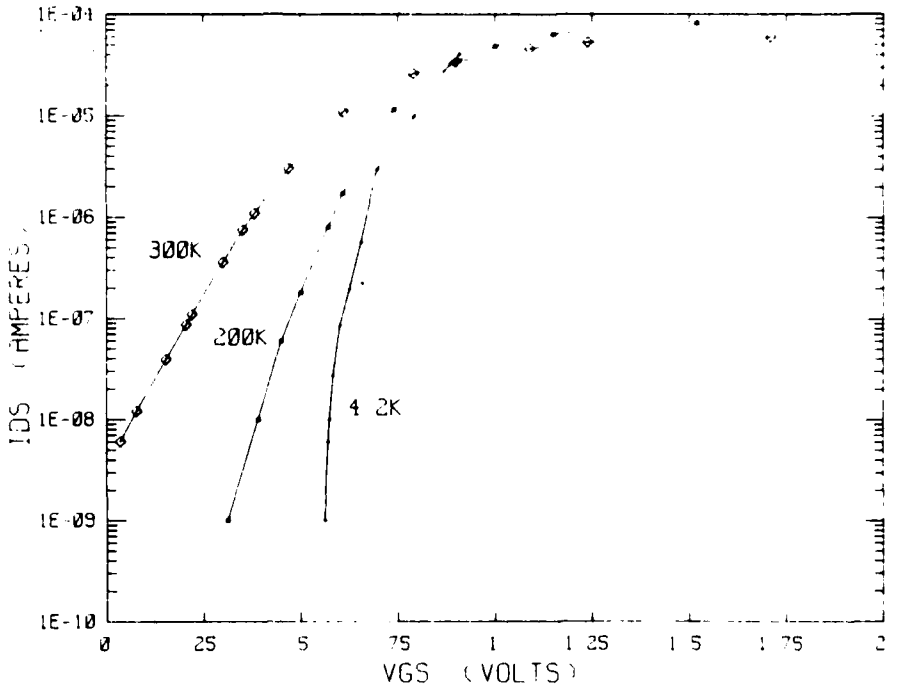


Figure 13. Subthreshold Characteristics for BTL#2 0.2um Transistor to 4.2K.

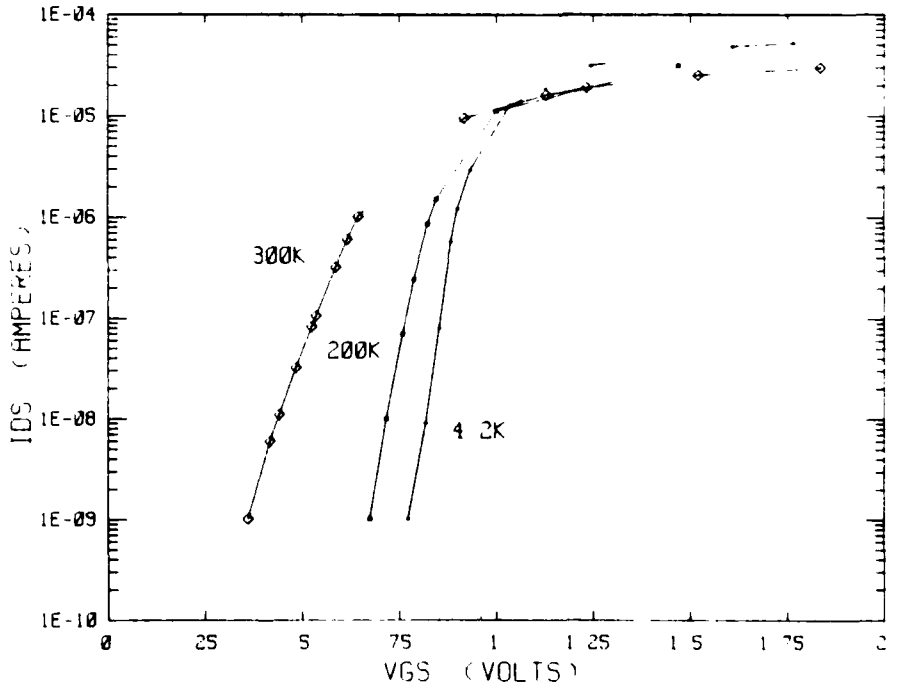


Figure 14. Subthreshold Characteristics for BTL#2 0.7um Transistor to 4.2K.

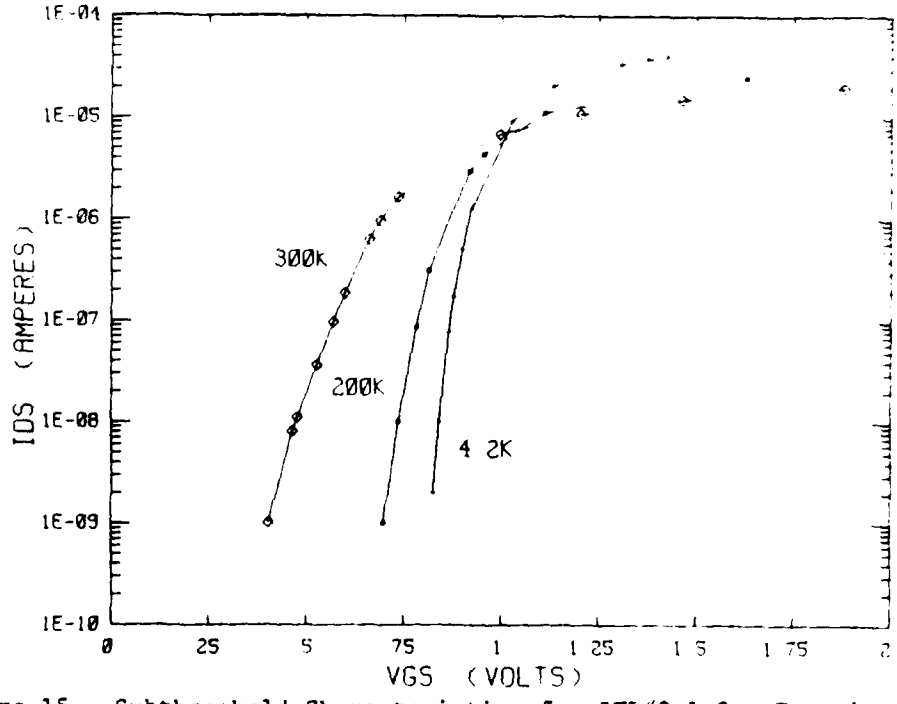


Figure 15. Subthreshold Characteristics for BTL#2 1.2um Transistor to 4.2K.

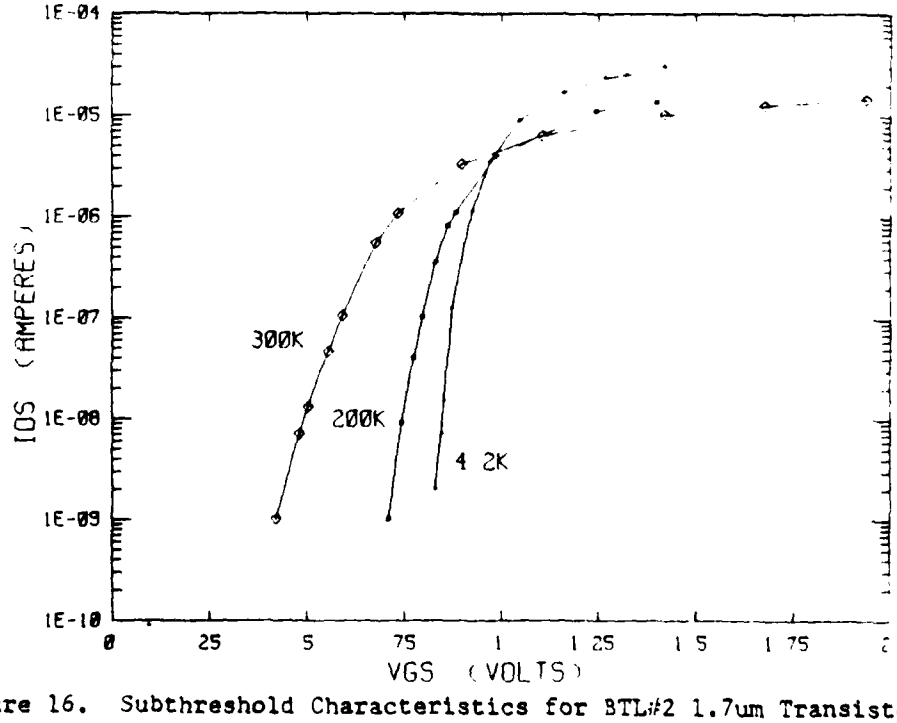


Figure 16. Subthreshold Characteristics for BTL#2 1.7um Transistor to 4.2K.

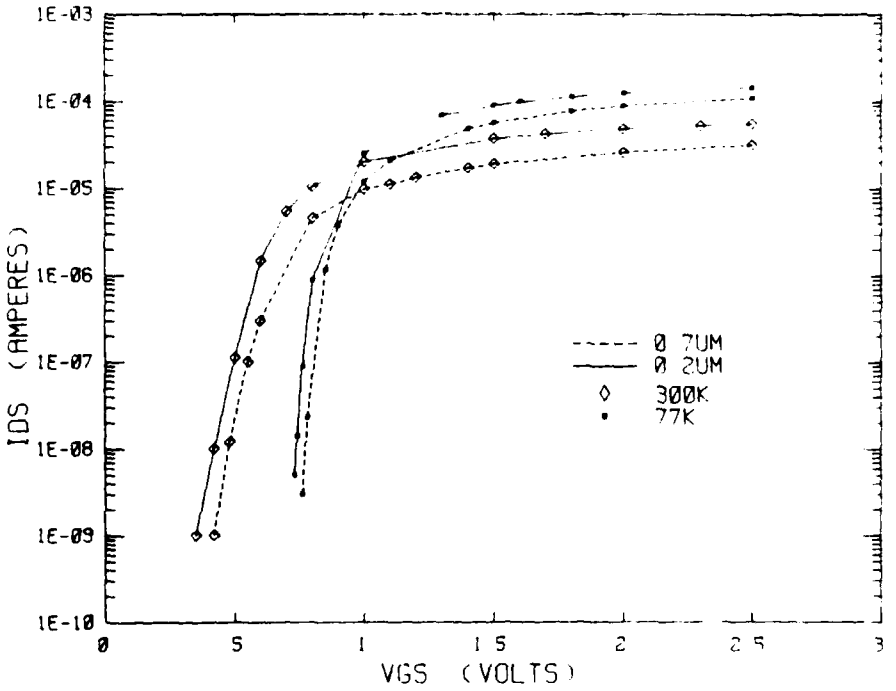


Figure 17. Subthreshold Characteristics for BTL#4 0.7um and 0.2um Transistors.

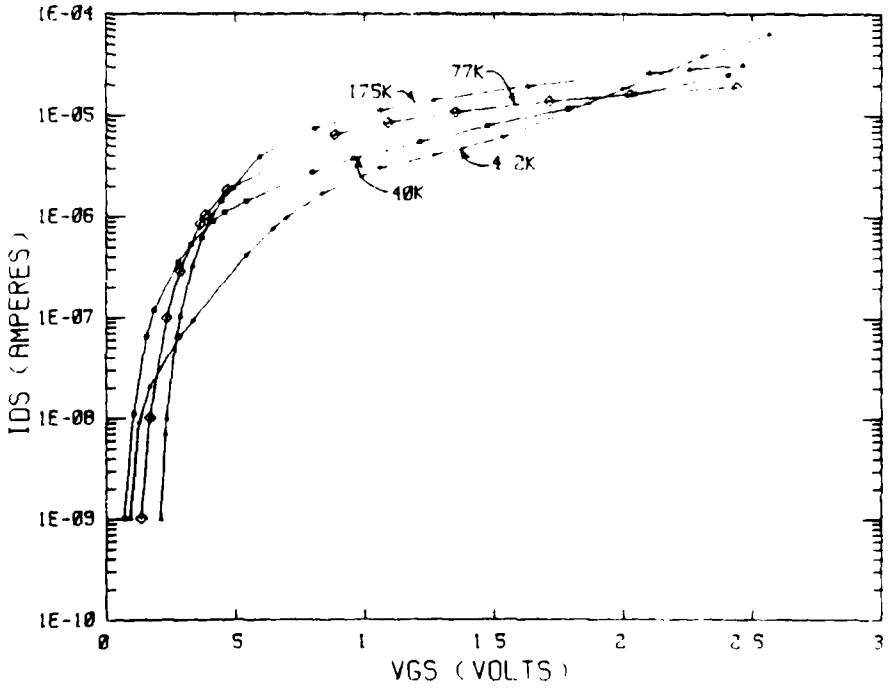


Figure 18. Subthreshold Characteristics for T500X500 Transistor to 4.2K.

B. Mobility Vs. Transverse Electric Field

Mobility in the Linear Regime

We have plotted the effective mobility vs. the transverse electric field for transistors operating in the linear regime in Figures 19-28. In the linear regime, the mobility was found to decrease as the transverse field increased. Above about Ex = 500 KV/cm, the mobility fell off logarithmically as the gate field approached 2000 KV/cm to a saturation value that was dependent on the effective gate length. Saturation values are listed in Table 2. We also saw that the mobility increased as the temperature decreased giving us a family of curves for each transistor.

Table 2. Saturation Mobility at High Transverse Field as a Function of Channel Length.

Channel Length (um)	Saturation Mobility ($cm^2/V-s$)
0.2	100
0.7	200
1.2	300
1.7	400

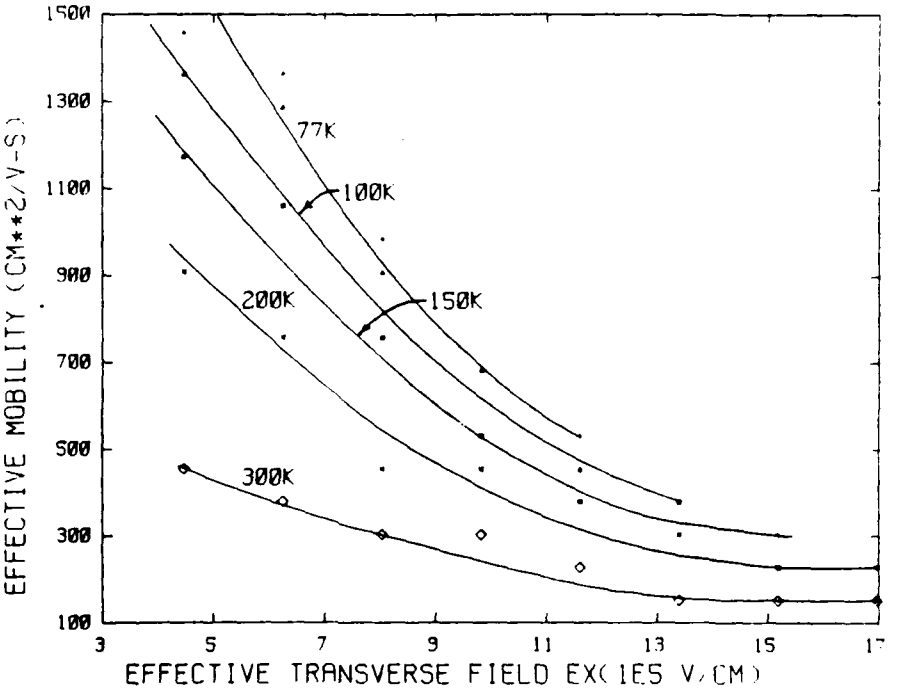


Figure 19. Effective Electron Mobility Vs. Transverse Electric Field for BTL#1 0.7um Transistor in the Linear Regime.

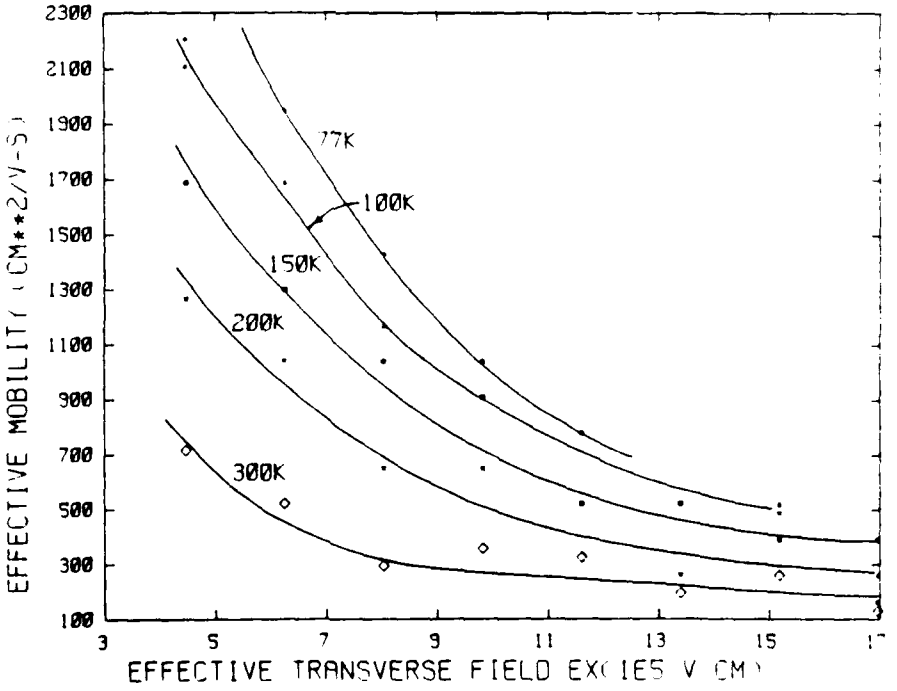


Figure 20. Effective Electron Mobility Vs. Transverse Electric Field for BTL#1 1.2um Transistor in the Linear Regime.

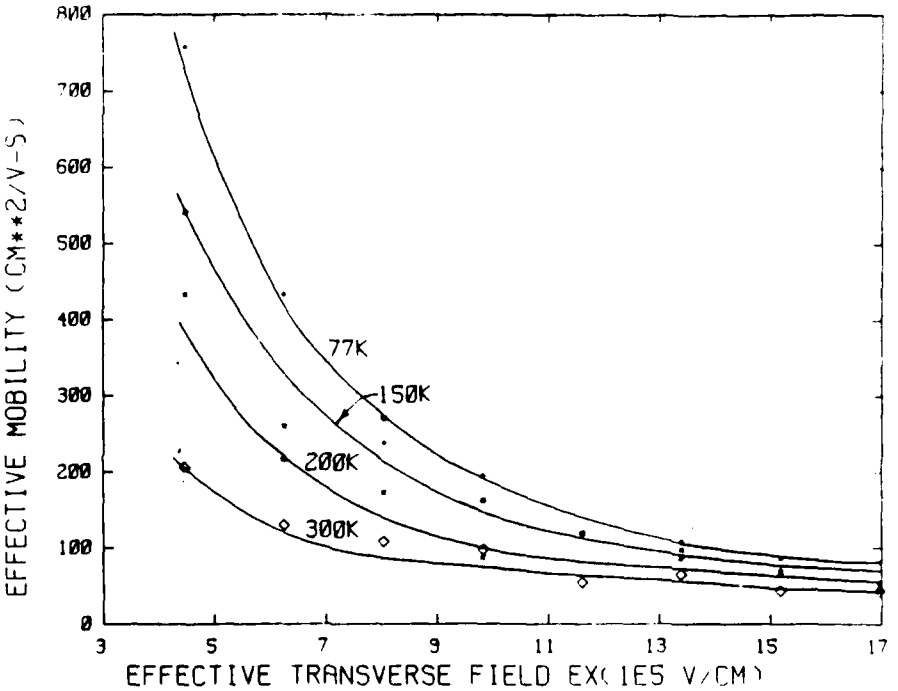


Figure 21. Effective Electron Mobility Vs. Transverse Electric Field for BTL#4 0.2um Transistor in the Linear Regime.

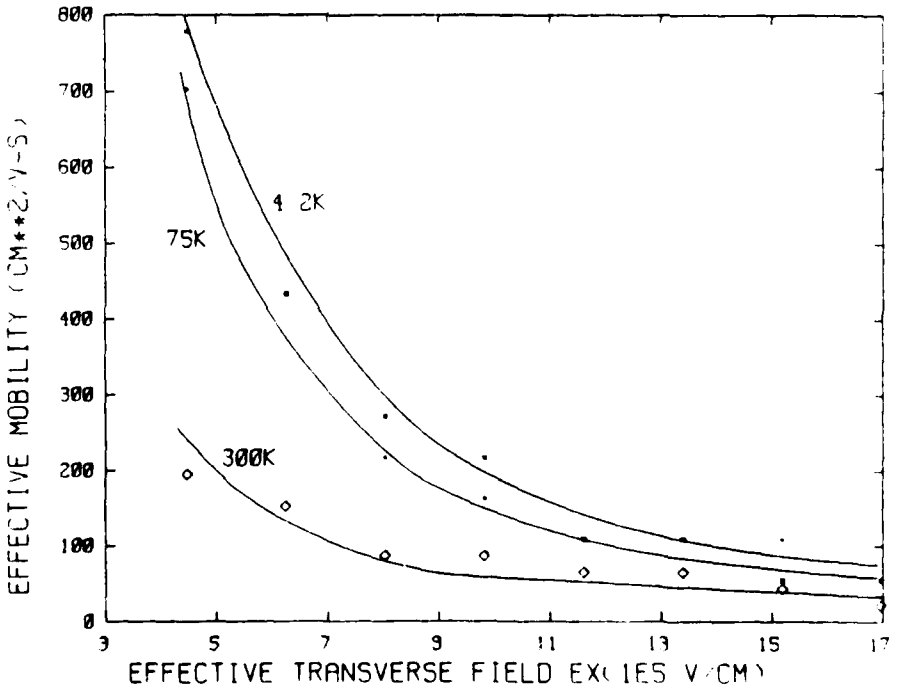


Figure 22. Effective Electron Mobility Vs. Transverse Electric Field for BTL#4 0.2um Transistor in the Linear Regime to 4.2K.

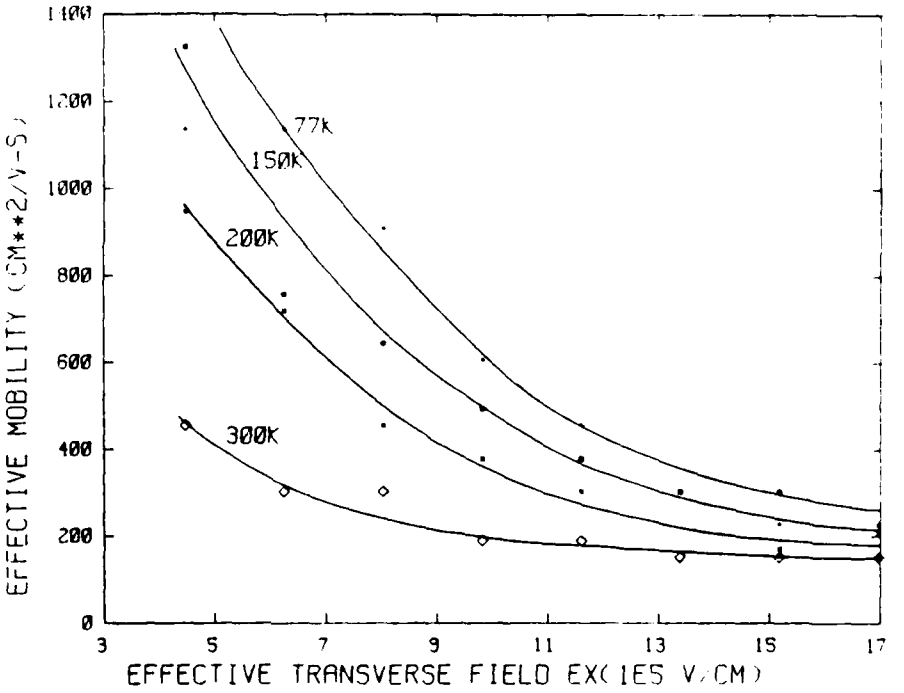


Figure 23. Effective Electron Mobility Vs. Transverse Electric Field for BTL#4 0.7um Transistor in the Linear Regime.

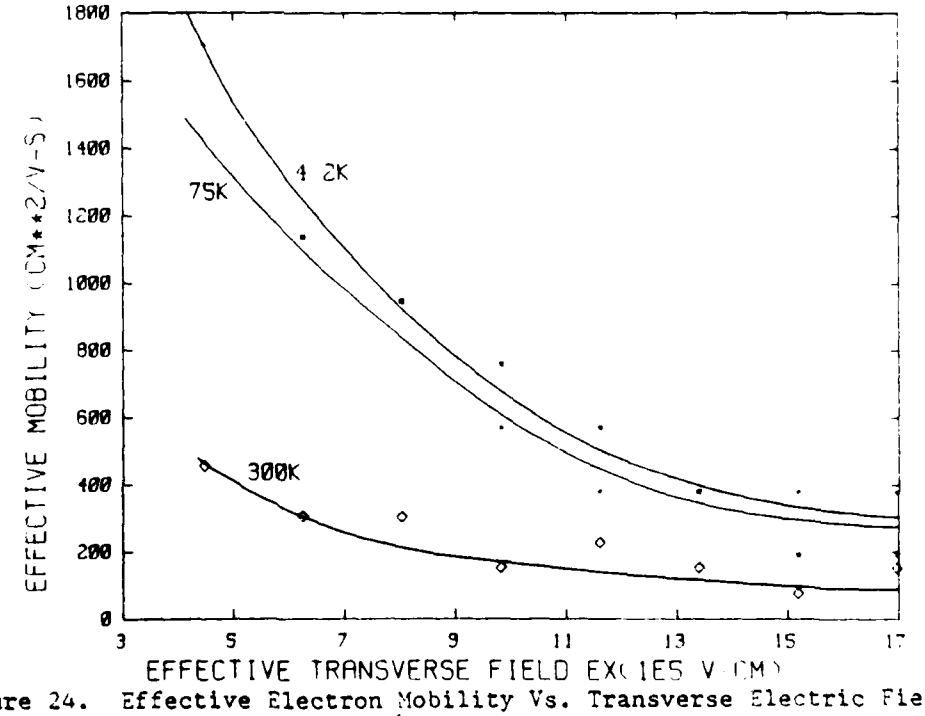


Figure 24. Effective Electron Mobility Vs. Transverse Electric Field for BTL#4 0.7um Transistor in the Linear Regime to 4.2K.

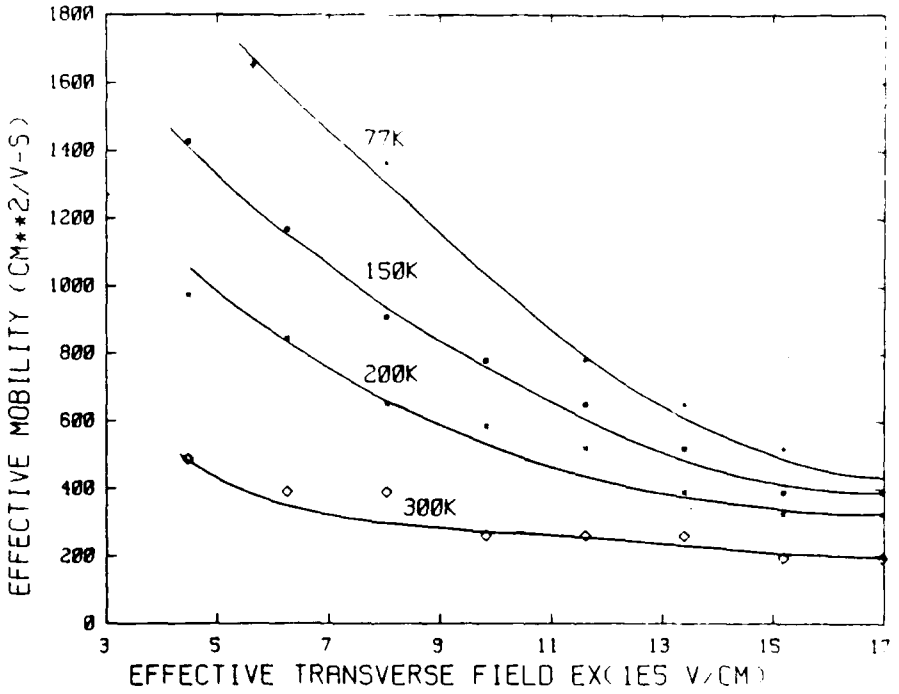


Figure 25. Effective Electron Mobility Vs. Transverse Electric Field for BTL#4 1.2um Transistor in the Linear Regime.

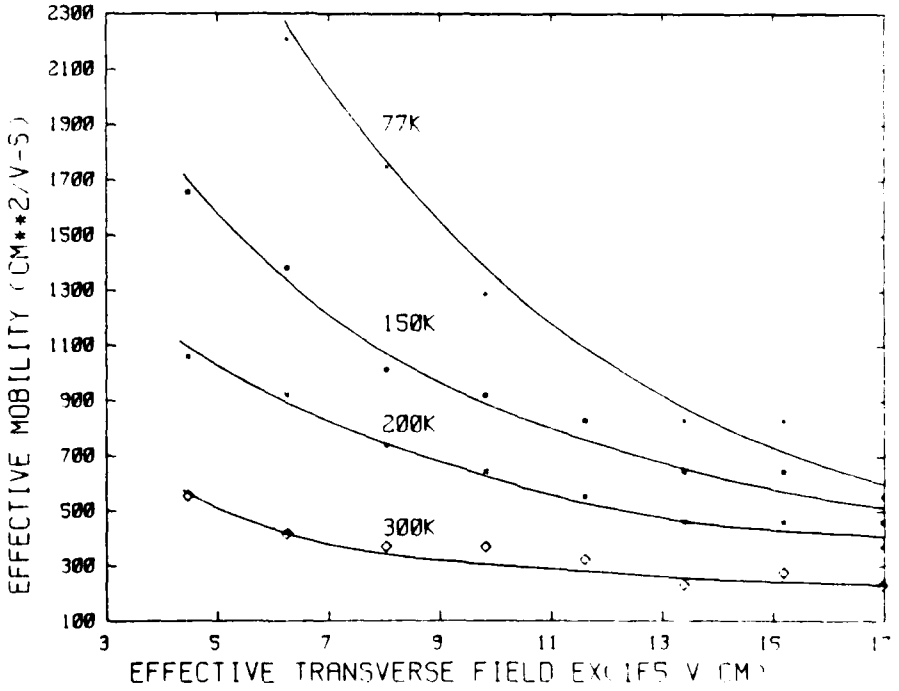


Figure 26. Effective Electron Mobility Vs. Transverse Electric Field for BTL#4 1.7um Transistor in the Linear Regime.

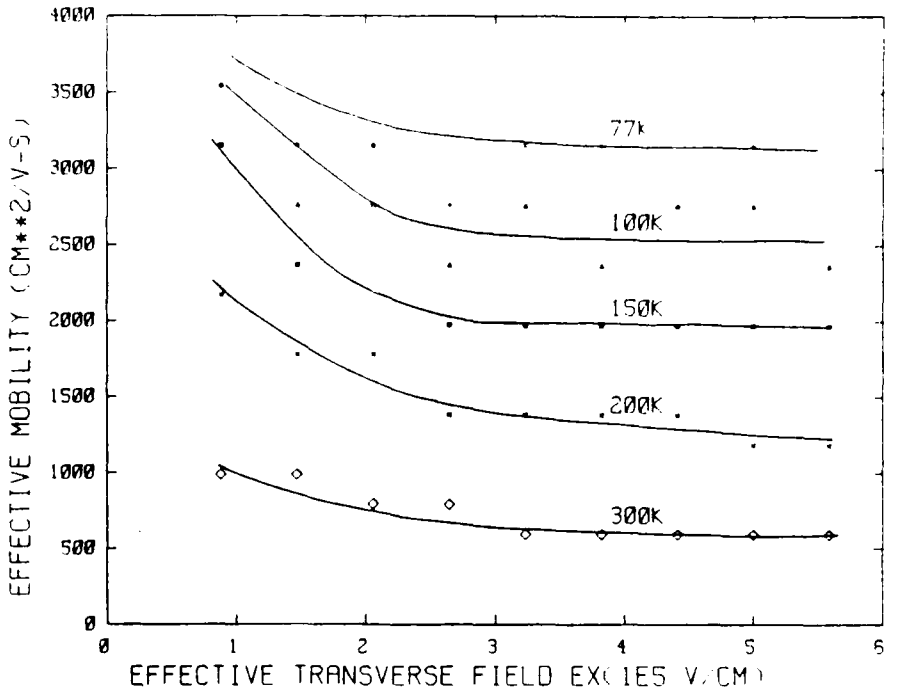


Figure 27. Effective Electron Mobility Vs. Transverse Electric Field for T500X500 Transistor in the Linear Regime.

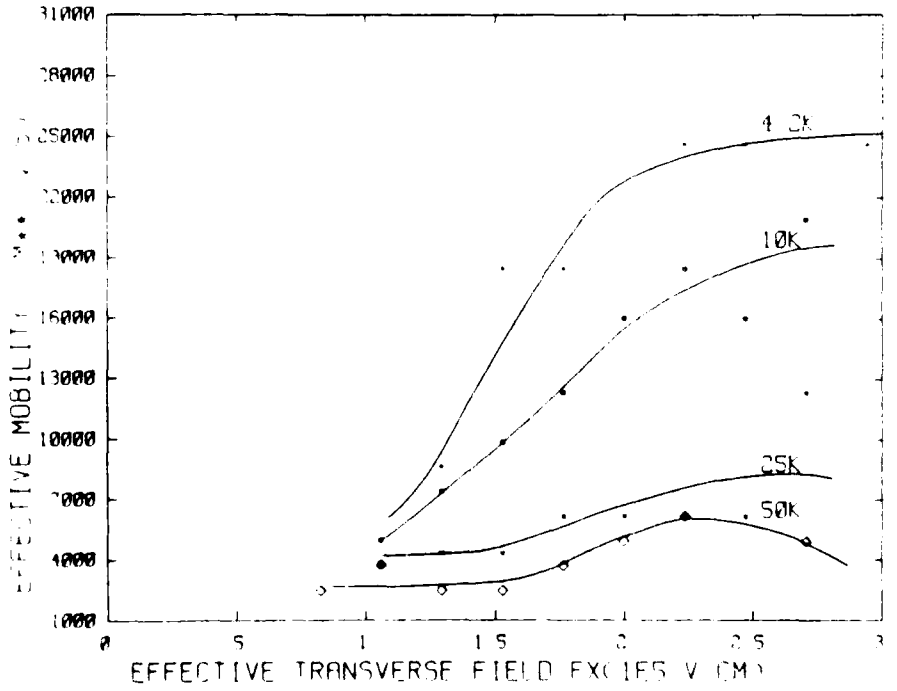


Figure 28. Effective Electron Mobility Vs. Transverse Electric Field for T500X500/I5 Transistor in the Linear Regime.

The mobility at very low temperatures was determined from data taken on the BTL#2 transistors. The mobiity increased linearly with the transverse field until about 500 KV/cm. Above 500 KV/cm the mobility fell to its saturation value. This characteristic was especially prominent in the 0.2 um transistor curves. The peak mobility occured at a slightly lower transverse field at 4.2K. At 4.2K the maximum mobility appeard at about 300 KV/cm.

In each transistor, we saw an increase in mobility as the effective channel length increased. This was probably due to the higher longitudinal fields that appeared in the smaller transistors. All data for these mobility measurements were taken with the drain-to-source voltage set to 0.1 volts. Thus, there were proportionally higher drain fields in the smaller devices.

Mobility in the Saturation Regime

In Figures 29-34 we have plotted the effective mobility as a function of electric field for transistors operating in the saturation regime. The drain voltages were on the order of 2.0 volts which gave us longitudinal electric fields around 100 KV/cm in the 0.2 um devices. With such high longitudinal fields applied to the device, we found that the effective mobility peaked at a value of transverse electric fie. of around 400 KV/cm for temperatures above 77K. Above 400 KV/cm, the effective mobility fell off logrithamically to a field dependent saturation value just as observed in the linear regime. At 4.2K, the effective mobility reached a maximum at a transverse field of around 200 KV/cm. This characteristic was also observed in the linear regime.

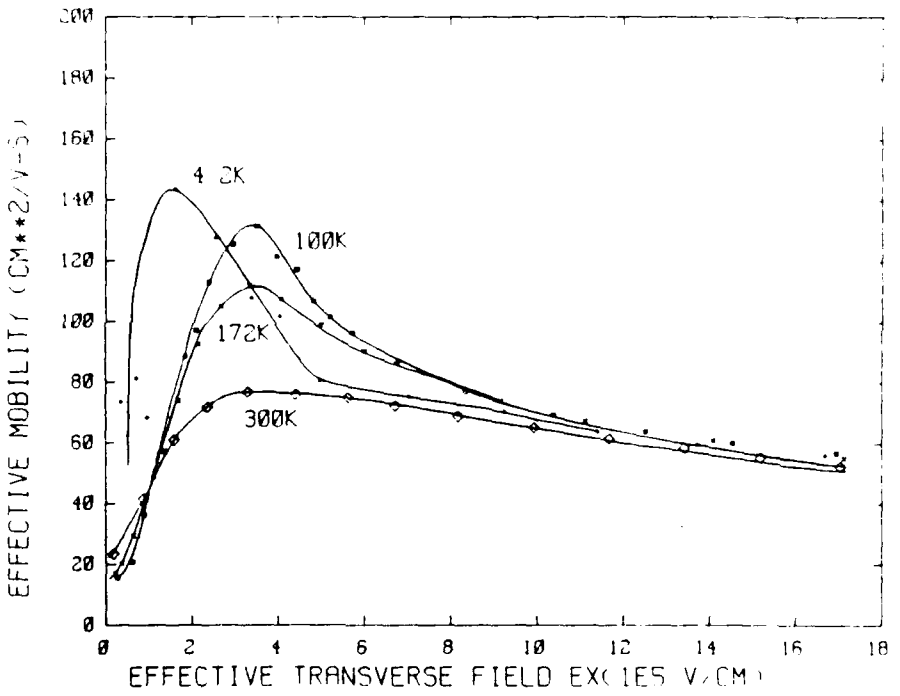


Figure 29. Effective Mobility Vs. Transverse Electric Field for BTL#2 0.2um Transistor in the Saturation Regime.

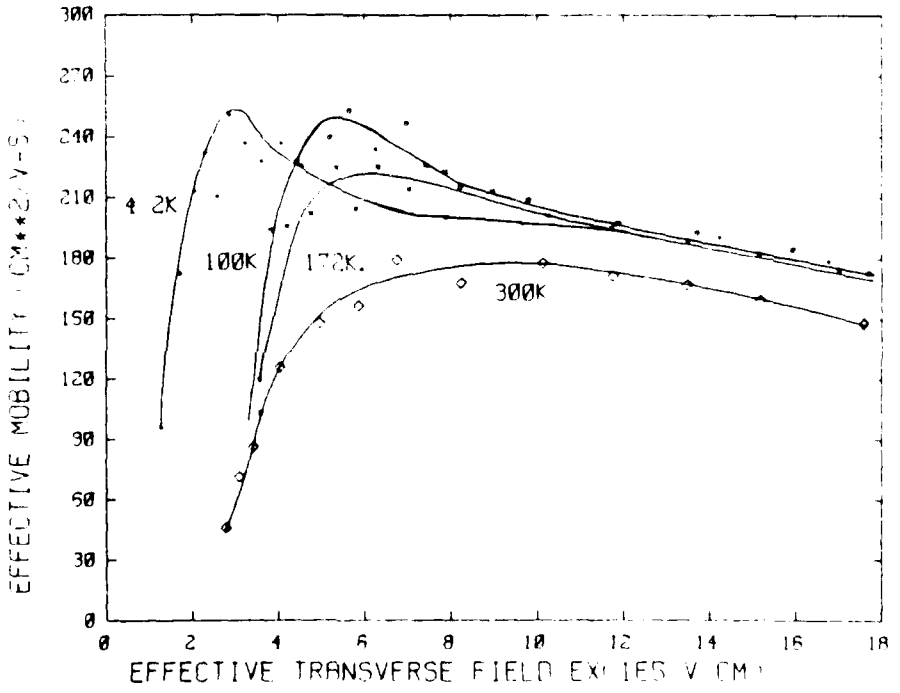


Figure 30. Effective Mobility Vs. Transverse Electric Field for BTL#2 0.7um Transistor in the Saturation Regime.

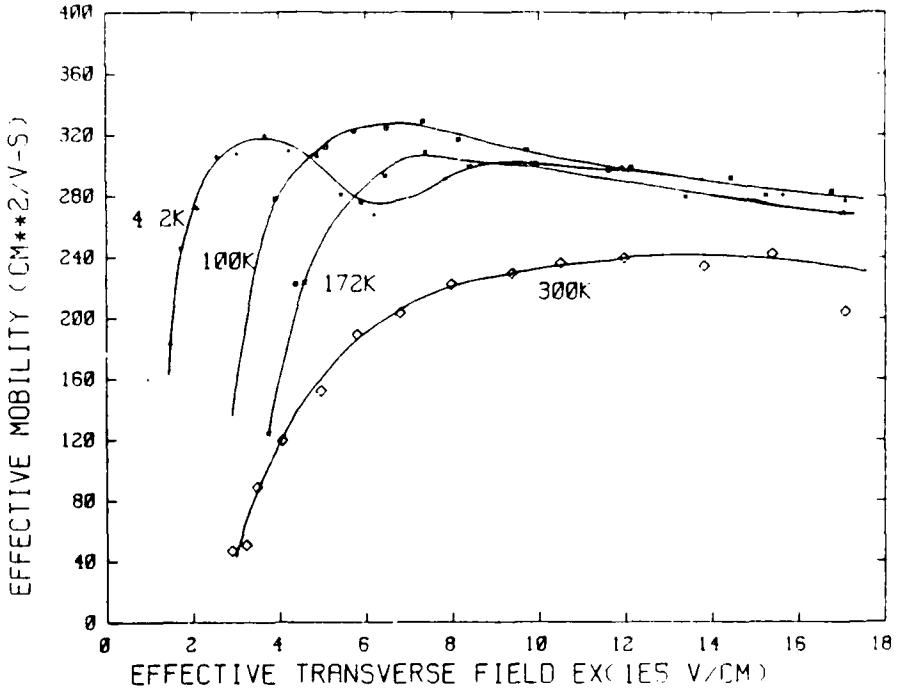


Figure 31. Effective Mobility Vs. Transverse Electric Field for BTL#2 1.2um Transistor in the Saturation Regime.

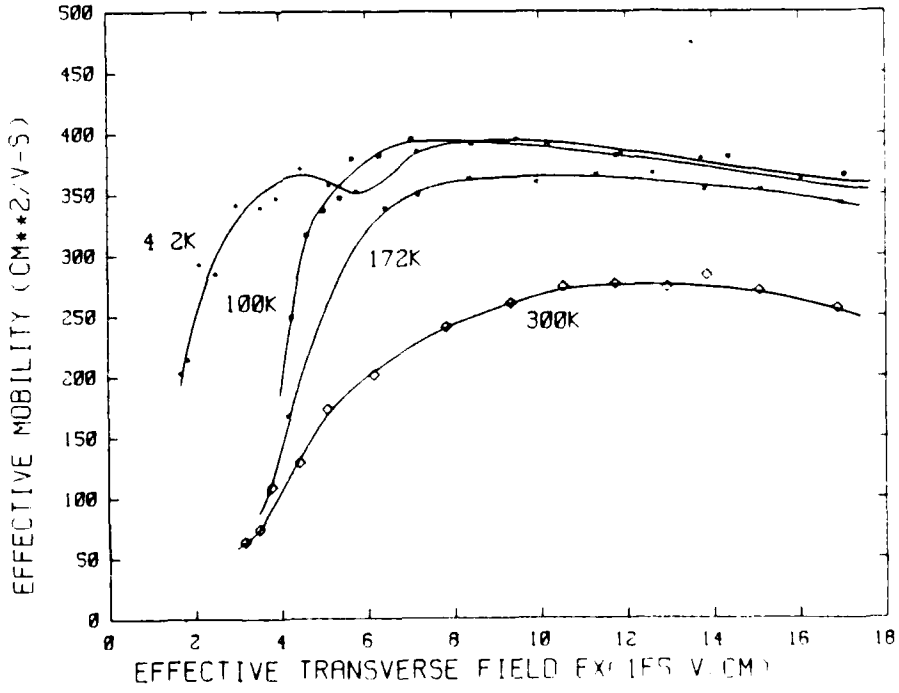


Figure 32. Effective Mobility Vs. Transverse Electric Field for BTL#2 1.7um Transistor in the Saturation Regime.

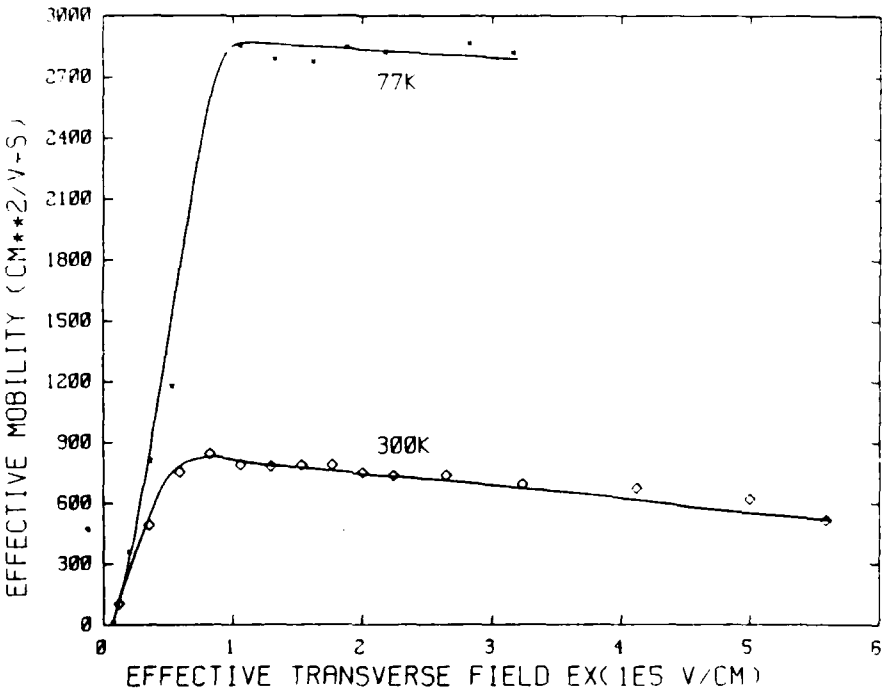


Figure 33. Effective Mobility Vs. Transverse Electric Field for T500X500 Transistor in the Saturation Regime.

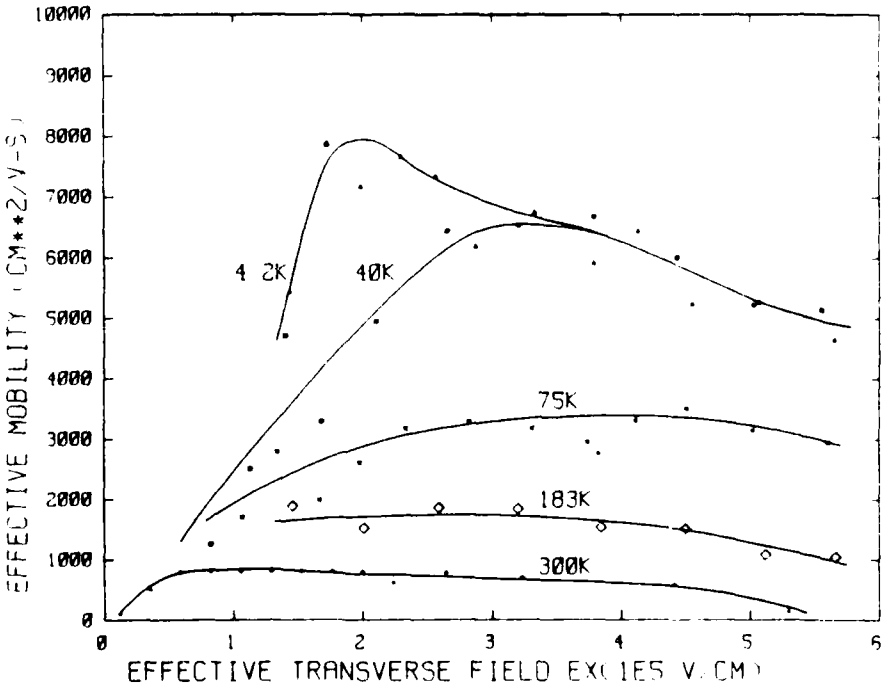


Figure 34. Effective Mobility Vs. Transverse Electric Field for T500X500 Transistor in the Saturation Regime to 4.2K.

Mobility as a Function of Temperature

A comparison of the respective mobilities at 300K and 77K showed that there was an increase in the mobility by approximately a factor of 4 over this temperature range. This data was tabulated in Table 3. These results were in good agreement with published results for long channel transistors(24).

Discussion

The effect of temperature on the mobility may be observed by plotting the effective electron mobility vs. temperature as shown in Figure 35. There were two things evident from this graph. First, the mobility decreased with increasing longitudinal field. Secondly, mobility increased with decreasing temperature approaching a maximum value at 4.2K. This behavior is not as predicted by S. M. Sze and others(20, p. 30)(25). They show the mobility falling off below about 77K due to increased impurity scattering. The impurity scattering is greater below 77K because of the greater scattering angle of electrons at lower thermal energies. This effect did not appear in our mobility data. Rather, the mobility of our transistors continued to increase below 77K.

Table 3. Increase in Mobility from 300K to 77K at Ex = 500 KV/cm for the BTL#4 Transistor Data.

Channel Length (um)	Mobility at (K) 300	77	Increase Factor
0.2	200	750	3.75
0.7	450	1700	3.8
1.2	500	2300	4.6
1.7	600	2700	4.5

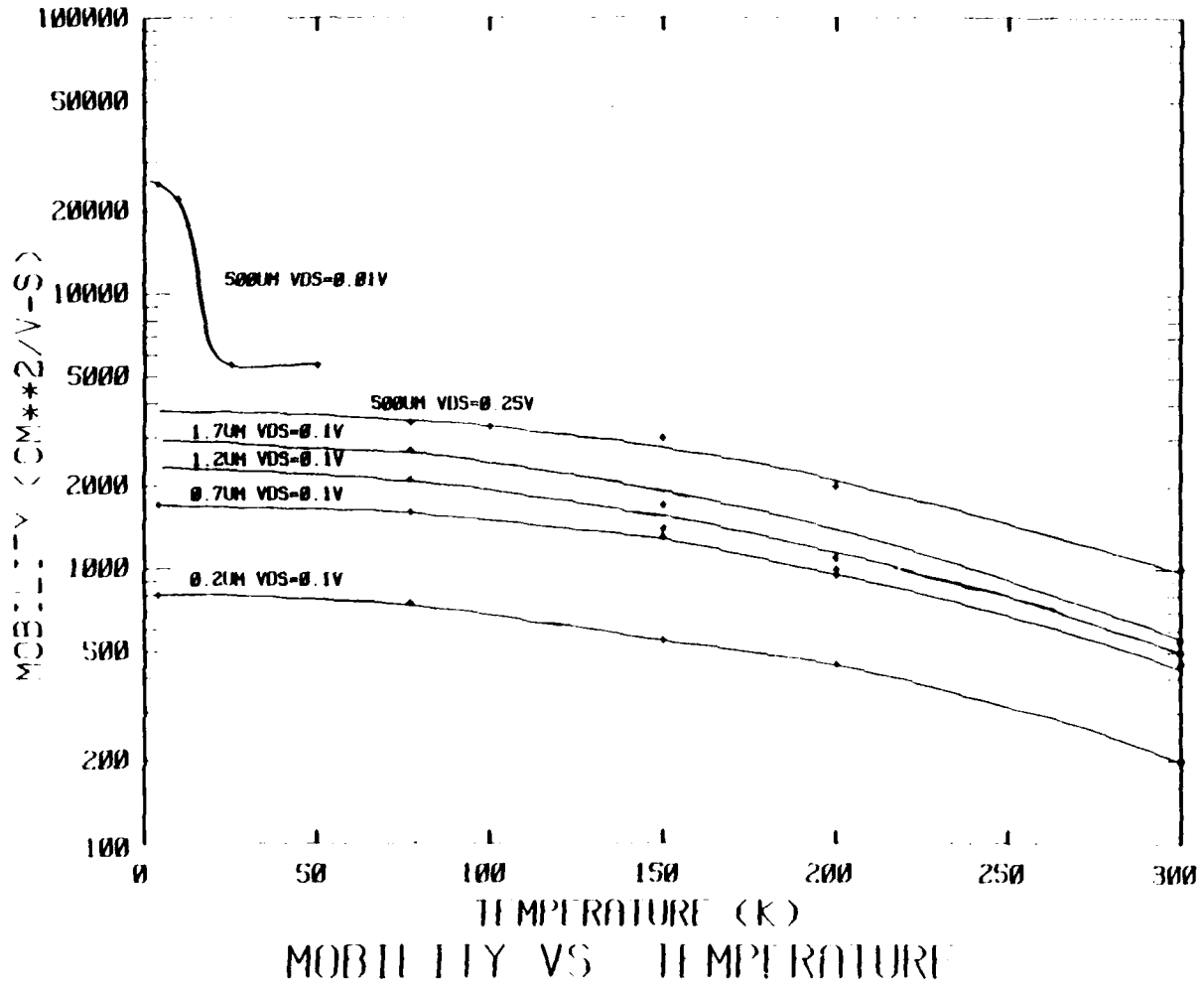


Figure 35. Mobility for Submicron and Long Channel MOS Transistors from 300K to 4.2K.

C. Electron Drift Velocity Vs. Longitudinal Electric Field

Mobility has been defined as the constant relating the electric field to the carrier velocity. For the carriers in the channel of a MOSFET, the drain-to-source voltage (Vds) creates the electric field that accelerates the charges to the drain. This accelerating field is referred to as the longitudinal field, Ey (volts/cm). The relationship between Ey and the drift velocity, Vs, then becomes

$$Vs = Un\ Ey$$

where Un is the effective electron mobility. The transverse field, Ex, is perpendicular to Ey and is created by the gate-to-substrate voltage, Vgs. The transverse field is responsible for creating the depletion region under the gate and the surface inversion region.

For each of our transistors we have taken Ids vs. Vgs data in the linear regime and used it to find a mobility and carrier velocity at several different temperatures. We then plotted low field mobility vs. transverse electric field for each transistor as shown in Figures 19-28. We used the low field mobility at Ex = 500 KV/cm for different temperatures and compiled a table of mobilities vs. Ey where

$$Ey = Vds / L \quad (v/cm)$$

and

Vds = drain-to-source voltage (volts)

L = effective channel length (cm).

These values are compiled in Table 4. This data was then plotted in Figure 36. In this graph, we have used the scattered data points to draw equithermal lines at 300K, 200K, 150K, 100K, 77K and 4.2K, respectively.

There are several important features in Figure 36. First, the relationship between the drift velocity and the longitudinal field is linear for the low field region below 1 KV/cm. This corresponds well to previous data as compiled by S. M. Sze(20, p. 46). Secondly, the slope of lines are parallel down to 77K. We see an increase in the slope at 4.2K. We may examine the slopes, S, quantitatively as

$$S = \frac{(\text{Log } V1 - \text{Log } V2)}{(\text{Log } E1 - \text{Log } E2)}$$

where (E1, V1) and (E2, V2) are two points in the linear region along the lines shown in Figure 36. The slope, S, then becomes

$$S = \frac{\text{Log}(V1/V2)}{\text{Log}(E1/E2)}.$$

Table 4. Longitudinal Electric Field Ey(KV/cm) Vs. Effective Carrier Velocity ($1X10^4$ cm/sec) to 4.2K Taken from Plots of Mobility Vs. Transverse Electric Field for Ex = 500 KV/cm. This data has been plotted in Figure 36.

Longitudinal Field (KV/cm)	Effective Carrier Velocity ($1X10^4$ cm/sec) Temperature (K)					
	300	200	150	100	77	4.2
0.0002					0.1	0.5
0.005	0.5	1.0	1.5	1.65	1.7	
0.07	4.9	10.5			21	49
0.588	32.4	65	100		160	
0.833	41.7	83	117		175	
0.833	50	94	125	163	192	
1.429	64.3	140	186		230	
1.429	64.3	121	164	200	240	
5.0	100	225	275		375	
12.0	330	420		460		460
17.0	400	500		534		534
29.0	460	600		690		710
100.0	750	1100		1300		1450

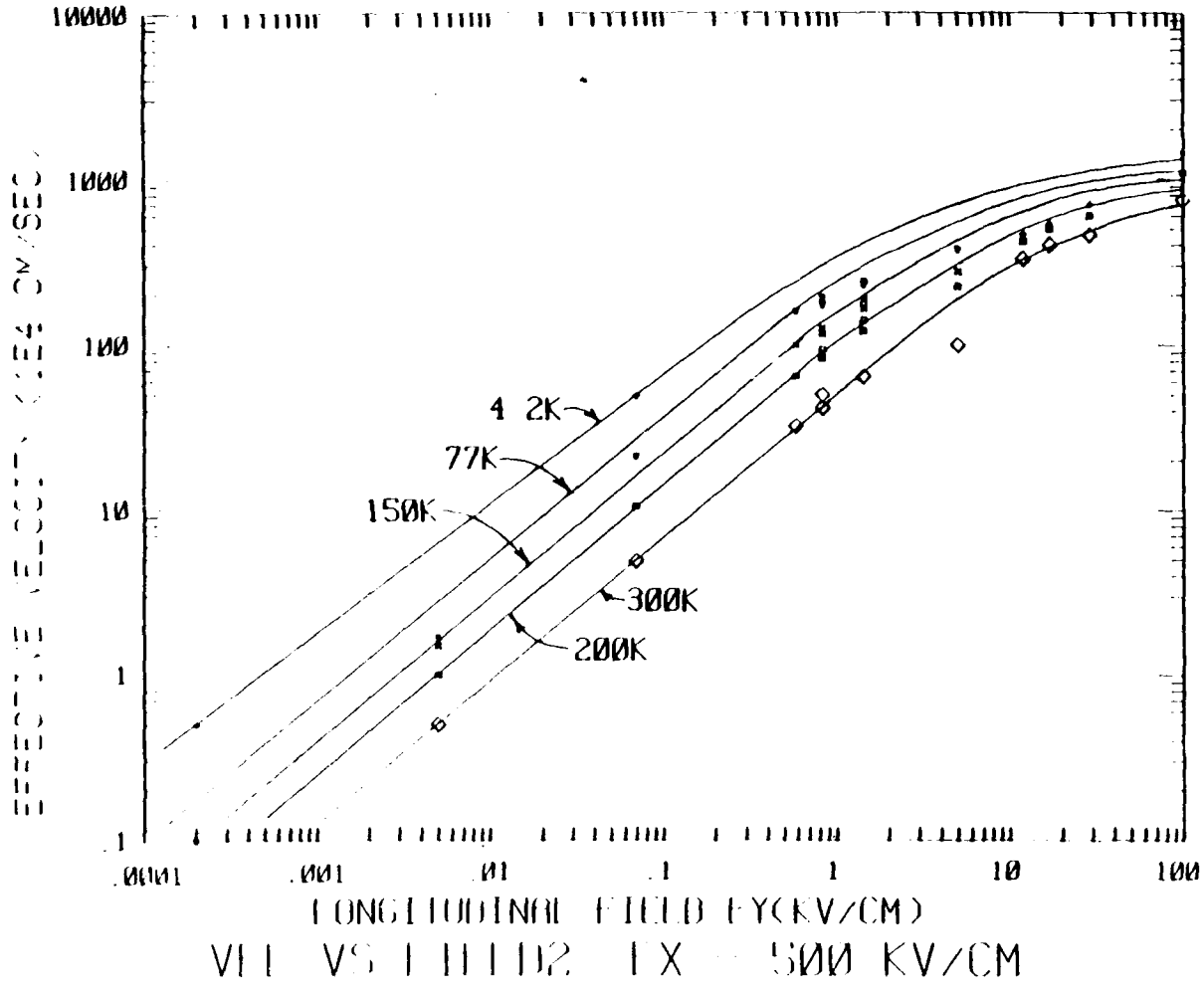


Figure 36. Effective Electron Velocity Vs. Longitudinal Electric Field for Temperatures 300K to 4.2K.

We may then find the power relationship between the longitudinal electric field and the effective electron velocity by examining the slope of the curves in the linear region.

Using the above relationship, S(300K) = 1.14, S(77K) = 1.19 and S(4.2K) = 1.26 from Figure 36. In comparison, a value of S(300k) = .99 was taken from the graph of effective velocity vs. longitudinal electric field in Sze(20, p. 46).

Using the linear relationship for carrier velocity, Vs, the electron mobility may be derived from Figure 36 as the linear approximation to the lines in the low field region. These values at 300K, 77K and 4.2K are respectively 1000, 4300 and 10,000 cm^2/V-s. In comparison, the 300K value in Sze is 1200 cm^2/V-s. We see that the effective electron mobilities are similar at 300K.

The constant mobility in the low field region is due to the constant transverse field which keeps the thickness of the inversion layer constant. Thus, the cross section area that an electron entering the channel sees remains relatively constant. The mobility increases dramatically as we lower the temperature due to decreasing scattering mechanisms. The effective electron mobility increases with decreasing temperature all the way down to 4.2K. This corresponds to the data presented by C. Jacoboni down to 77K(25). Our values for mobility vs. temperature at Ex = 10 KV/cm have been compliled in Table 5.

Below 77K, the mobility data presented by Jacoboni falls off due to the dominance of ionized impurity scattering over this region. Our data showed no such characteristic. Our data would be the result of an asymptotic extention of his data above 77K to the 10,000 cm^2/V-s line

Table 5. Mobility Vs. Temperature from the Velocity Vs. Longitudinal Electric Field Curves.

Temperature (K)	Mobility (cm^2/V-s)
300	1000
200	2000
150	3100
77	4300
4.2	10,000

for temperatures below 77K. In our data we do not see the effects of ionized impurity scattering below 77K which would usually lead to a decrease in mobility below about 50K according to(20, p. 28)

$$U_i = (m^*)^{-1/2} \quad N_i^{-1} \quad T^{3/2}$$

where

U_i = mobility due to ionized impurities

N_i = ionized impurity density

T = temperature

m^* = effective electron mass.

Above about 50K carrier scattering is dominated by acoustic phonon scattering whose mobility term is U_l. This mobility is given in Sze as(20, p. 28)

$$U_l = (m^*)^{-5/2} \; T^{-3/2}$$

where m^* and T are defined as before.

The mobilities are combined according to

$$U = (1/U_l + 1/U_i + \ldots)^{-1}$$

so that the smallest mobility term will dominate the scattering process. If we assume that the two scattering processes mentioned above are the two dominant mechanisms, we see that below about 50K, the two terms are nearly equal.

Saturation Velocity

Above 1 KV/cm, the velocity of the carriers in the channel begin to saturate and the carriers approach their thermal velocity at the respective temperatures. There is a slight increase in the saturation velocity as the temperature decreases as predicted by Sze(20,p. 46). The saturation velocity, Vs, tends to follow the relationship

$$Vs = \frac{2.4 \times 10^7}{1 + 0.8 \exp(T/600K)} \quad (cm/s)$$

where T is the temperature of the silicon sample. The drift velocities in Figure 36 approach $1X10^7$ cm/s in the saturation region. We see no deviation in the standard behavior of the MOSFETs even for very short channel devices at low temperatures.

The mobility, derived from the linear slope of the velocity vs. longitudinal field curves, decreased as the field increased. As we decreased the channel length (while keeping the supply voltages relatively constant) the fields inside the devices increased proportionally lowering the effective mobility of the carriers in the channel. Thus we see a lower mobility for shorter channel transistors. We can not achieve high effective electron mobilities in submicron devices operating at nominal supply voltages even at very low temperatures.

The new generation of submicron devices will have to operate at lower supply voltages if there are to be high carrier velocities and ballistic transport in the channel. There is a lower limit to the size of operating voltages due to noise margin considerations.

SECTION VIII

CONCLUSIONS

We have measured the I-V characteristics of submicron silicon MOSFETs to 4.2K in the subthreshold, linear and saturation regimes. We have obtained the mobility vs. transverse electric field for submicron devices in the linear and saturation regimes. We used data from devices with gate lengths of 0.2, 0.7, 1.2, 1.7 and 500 um to determine the effective electron velocity vs. the longitudinal electric field.

We found mobilities in 500 um silicon devices that were as high as 25,000 $cm^2/V\text{-}s$ at 4.2K. This was in the low field regime with Vds = 0.01 v. Mobilities of this magnitude could lead to ballistic transport in submicron devices. But the mobilities in 0.2 um devices with Vds = 0.1 v. were only about 800 $cm^2/V\text{-}s$ at 4.2K. We saw that the shorter channel lengths lead to proportionally higher longitudinal electric fields which reduced the electron mobility. Therefore, the drain-to-source voltage would have to be reduced to a few microvolts to achieve mobilites high enough to observe ballistic transport in submicron devices.

We found that the effective electron velocity is linearly proportional to the longitudinal electric field for fields below 1000 V/cm. Above 1000 V/cm the velocty begins to saturate at about Vs = $1X10^7$ cm/s. The saturation velocity was slightly higher for lower temperatures. In the linear region, Ex = 10 KV/cm, we found that the mobility varied from 1000 and 4300 $cm^2/V\text{-}s$ at 300K and 77K to 10,000 $cm^2/V\text{-}s$ at 4.2K.

APPENDICIES

APPENDIX A

DERIVATION OF MOBILITY AND CARRIER VELOCITY FROM DEVICE TEST DATA

The drain current in an MOS transistor is given by(20, p. 440)

$$Ids = \frac{Z}{L} Un\ Ci \left\{ (Vgs - 2Vb - \frac{Vds}{2})\ Vds - \frac{2}{3} \frac{2\ Es\ q\ Na}{Ci} \left[(Vds + 2Vb)^{2/3} - (2Vb)^{2/3} \right] \right\} \qquad (A\text{-}1)$$

where

Z = gate width

Un = effective electron mobility

Ci = gate capacitance per unit area

L = gate length

Vgs = gate-to-source voltage

Vb = built-in voltage

Vds = drain-to-source voltage

Es = permitivity of silicon

Na = channel doping

q = electron charge.

The idealized characteristics are defined by:

1) Gate structure is an ideal diode, i.e. no interface traps fixed oxide charge or work function differential;
2) Consider only drift component of drain current;
3) Carrier mobility in the inversion layer is constant;
4) Uniform channel doping;
5) Reverse leakage current negligibly small;
6) Transverse field is much greater than the longitudinal field, i.e. the gradual channel approximation.

This equation may be simplified depending on the region in which the device is operating. For our purposes we define three regions as linear, velocity saturation, and pinchoff saturation. This will lead to three equations from which we may derive the carrier mobility and velocity in each case.

Linear Case

When the drain voltage is small, this equation reduces to

$$Ids = \frac{Z\ Un\ Ci}{L} (Vgs - Vt)\ Vds \qquad (A-2)$$

for $Vds \ll (Vgs-Vt)$ where Vt = Threshold voltage.

By rearranging terms, we can get

$$Ids = \left(\frac{Z\ Un\ Ci\ Vds}{L}\right) Vgs - \left(\frac{Z\ Un\ Ci\ Vds}{L}\right) Vt$$

where

$$Ci = Es\ /\ d$$

and

$$Es = 1.1 \times 10^{-12}\ F/cm$$

d = thickness of the gate oxide.

Equation (A-2) is the slope-intercept form of a line plotted on a Ids vs. Vgs graph for constant Vds as shown in Figure A-1.

Given a graph of the experimental results, as in Figure A-1, we may use the slope of the line to find the mobility. Given the device characteristics and the slope, M, at a given temperature,

$$Un = \frac{M\ L}{Z\ Ci\ Vds} \quad (cm^2/V\text{-}s) \qquad (A\text{-}3)$$

and the carrier velocity, Vs, is given by the equation

$$Vs = \frac{Un\ Vds}{L} \quad (cm/sec). \qquad (A\text{-}4)$$

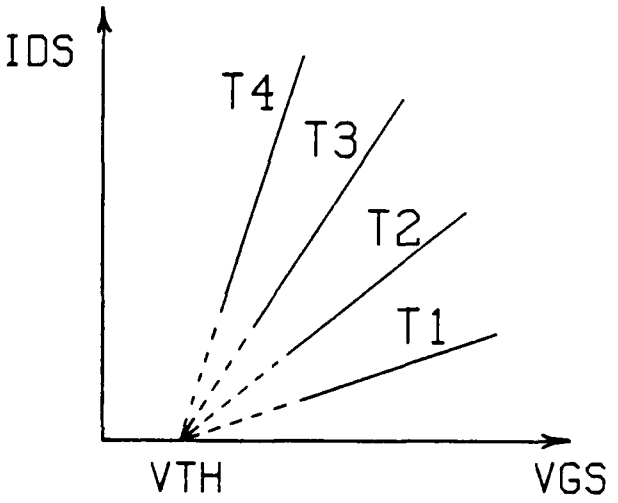


Figure A-1. Example of Ids Vs. Vgs Plotted Data for Linear and Velocity Saturation Curves.

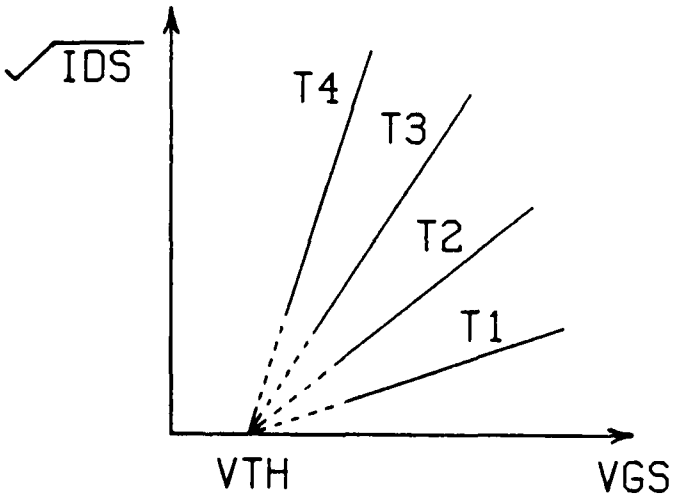


Figure A-2. Example of Square Root of Ids Vs. Vgs Plotted Data for Pinchoff Saturation Curve of a Long Channel Transistor.

Velocity Saturation

When the drain voltage becomes large, Vds (Vgs - Vt), and the device under test has a short channel (L = 1 um) the high longitudinal field causes the carrier velocities to approach their saturation value ($1X10^7$ cm/s in silicon). This velocity saturation has the effect of limiting the saturation current in the device before normal pinchoff saturation occurs(20, p. 442). Under these conditions, the saturation current is linearly dependent on the gate voltage and is given in Sze as(20, p. 450)

$$Ids = Z\ Ci\ (Vgs - Vt)\ Vs \qquad (A-5)$$

where Vs is the carrier velocity in the channel.

Just as we did in the linear case, we may rearrange terms in Equation (A-5) and get

$$Ids = (Z\ Ci\ Vs)\ Vgs - (Z\ Ci\ Vs)\ Vt.$$

From the slope, M, of the Ids vs. Vgs curve shown in Figure A-1, we may derive an expression for the carrier velocity, namely

$$Vs = \frac{M\ d}{Z\ Es} \quad (cm/sec). \qquad (A-6)$$

Rearranging the terms in Equation (A-4) we get the expression for effective mobility

$$Un = \frac{2\ Vs}{Vds} \qquad (cm^2/V\text{-}s). \tag{A-7}$$

Pinchoff Saturation

In the normal long channel transistor, as the drain voltage is raised, the charge in the inversion layer at the drain becomes zero. This is the pinchoff point(20, p. 440). Above this point, increases in Vds no longer lead to increases in drain current Ids so this region is usually referred to as the saturation region. In this region, Equation (A-1) reduces to

$$Ids = \frac{Z\ Un\ Ci}{2L} (Vgs - Vt)^2. \tag{A-8}$$

If we take the square root of both sides of Equation (A-8) and rearrange terms, we get

$$(Ids)^{1/2} = [Z\ Un\ Ci/(2L)]^{1/2} (Vgs - Vt). \tag{A-9}$$

Notice that this is the slope intercept form of a line plotted on a graph of the square root of Ids vs. Vgs as shown in Figure A-2.

Given the slope, M, of a line in Figure A-2, the effective mobility becomes

$$Un = \frac{2\ M^2\ L\ d}{Z\ Es}. \qquad (cm^2\ /V\text{-}s). \qquad (A\text{-}10)$$

The carrier velocity may be found using Equation (A-4).

For the purposes of this report, a program was written which uses the above equations to create a graph of carrier velocity vs. transverse electric field given either the Ids vs. Vgs or square root of Ids vs. Vgs curves. Experimental data was taken at descrete points along these curves and stored on floppy disks using the Strobe Graphics plotter software. The program we wrote retrieved this data from the disk file and calculated the slope of the curves using a linear approximation between consecutive data points. The slope of the line was used to determine the mobility between these two data points. This mobility was then associated with the transverse electric field for the gate voltage midway between the original two data points. The mobility vs. transverse electric field data was stored on floppy disk for later plotting.

APPENDIX B

DETERMINATION OF EFFECTIVE CHANNEL LENGTH

As the gate definition approaches submicron lengths, lateral diffusions can drastically reduce the effective channel length from the mask size. Therefore we need an accurate method to determine what the actual channel length is after the MOSFET is manufactured(26).

The method we chose was both convient and nondestructive. The only requirement is that you have at least two transistors on the chip with different gate lengths. In our case, we used transistors with gate lengths of 1.0, 2.0, 3.0 and 6.0 um.

We made Ids vs Vgs measurements of these transistors for several gate voltages in order to find the measured channel resistance, R_m,

$$R_m = \frac{Vds}{Ids} = R_{ext} + R_{channel}$$

and

$$R_m = R_{ext} - A(L_{mask} - DL)$$

where

$$A = [Un\ C_{ox}\ W_{eff}\ (Vgs - Vt - Vds/2)]^{-1}$$

and

R_m = measured resistance

R_{ext} = external contact resistance

$R_{channel}$ = channel resistance

L_{mask} = mask length of the gate

DL = difference in effective length and mask length

W_{eff} = effective width of the depletion layer

C_{ox} = gate oxide capacitance.

For a fixed Vds, if we plot R_m versus L_{mask} we will get a set of straight lines that intersect at the point (R_{ext}, DL). Thus we may find the external resistance in our test circuit R_{ext} and the difference between the mask length, L_{mask}, and the effective channel length L_{eff} which is

$$L_{eff} = L_{mask} - DL$$

The data for our transistors has been plotted in Figure B-1. Here we can see that the R_{ext} = 55 ohms and L = 0.8 um.

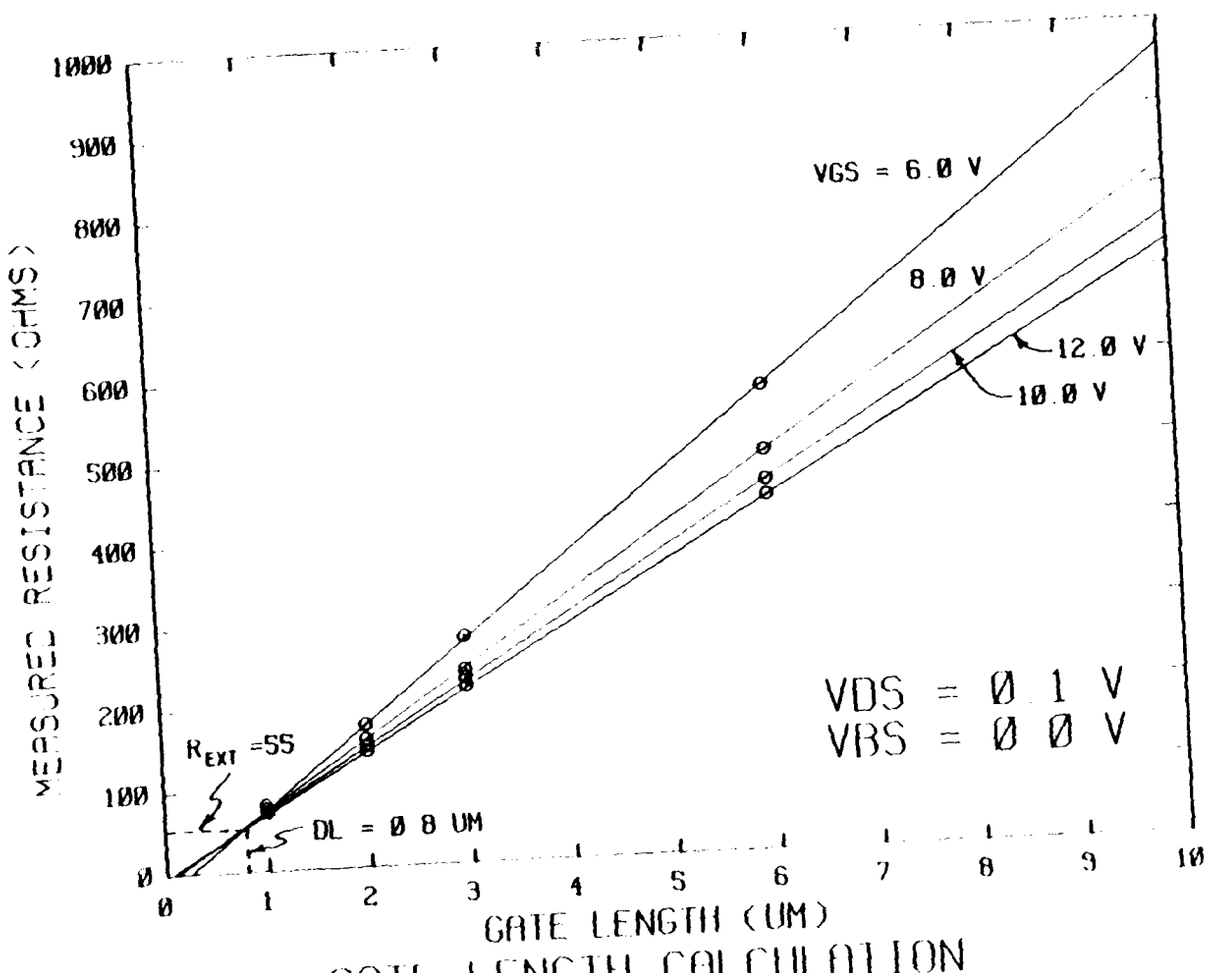


Figure B-1. Measured Resistance Vs. Gate Length Used to Determine the Effective Gate Length of Our Submicron Silicon Transistors.

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