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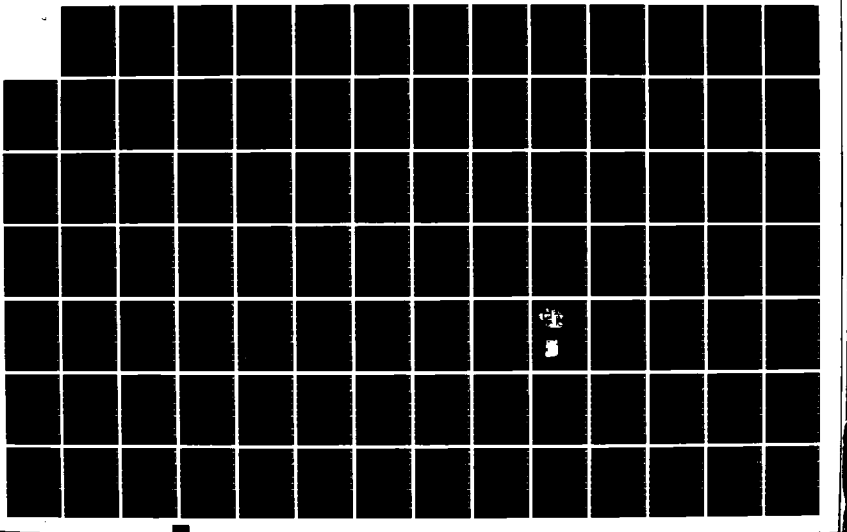

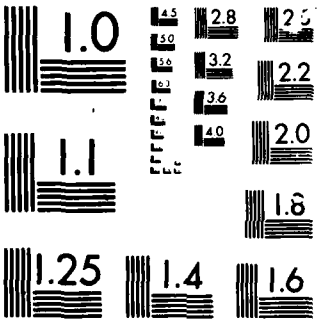
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A Dedicated Microprocessor Controller for a Bound Document Scanner

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Final Report - February 1984

A thesis submitted to Massachusetts Institute of Technology, Cambridge, Massachusetts in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

A DEDICATED MICROPROCESSOR CONTROLLER FOR A BOUND DOCUMENT SCANNER

by

EDWARD CHARLES SHAFFER

Captain, United States Army

B.S., United States Military Academy (1975)

Submitted to the

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

in partial fulfillment of the requirements

FOR THE DEGREE OF

MASTER OF SCIENCE

at the

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J.F. Reintjes, Thesis Supervisor

Accepted by _____
Chairman, Departmental Committee on Graduate Students

ABSTRACT

Research was carried out on an electro-optical bound document scanner which used a general purpose F-8 microcomputer as the scanner controller. The goal was to replace the F-8 with a dedicated controller by replicating essential features of the system which provided the scanner/controller interface. A microprocessor-based configuration was considered to be the most promising approach. A detailed analysis of the existing hardware and software interface between the F-8 and the scanner was conducted to establish the feasibility of using a microprocessor and to develop controller design criteria. Features of a number of microprocessors were examined and compared against one another to determine the best architecture for this application.

A microprocessor-based controller was designed using the MOSTEK MK38P70 microprocessor. Integral to the design were two Intel 8255A Programmable Peripheral Interface (PPI) chips which allowed the four 8-bit I/O ports of the MK38P70 to perform all the functions previously handled by nine F-8 I/O ports. A 2Kx8-bit EPROM holds the control program MEOSC. MEOSC is a modified version of the F-8 controller program, EOPS2. The F-8 was able to be used as a versatile system development and debug tool for the dedicated controller since the MK38P70 uses F-8 assembly language. A threshold monitor and adjust circuit was developed in conjunction with the controller in order to provide the operator a means to control the black-to-white transitions of CCD pixel data derived from the scanner.

System performance using the controller has been excellent. Printer and CRT copies of scanned documents obtained from the system using the MK38P70 controller are indistinguishable from those obtained using the F-8 controller under similar conditions. All control functions have been consolidated onto the scanner front panel. A significant reduction of system space requirements has been achieved, and the F-8 has been released for more general purpose work.

Thesis Supervisor: Dr. J.F. Reintjes

Title: Professor Emeritus, Electrical Engineering

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BIOGRAPHICAL NOTE

Ed Shaffer, a Captain in the United States Army Signal Corps, is a 1975 graduate of the United States Military Academy. As an undergraduate, he concentrated in Electrical Engineering and participated in research to develop camouflaged tactical radio antennas. He has completed the Signal Officer Basic and Advance Courses at Fort Gordon, Georgia and was Distinguished Graduate of his Communications-Electronics Staff Officer Course at Fort Sill, Oklahoma. His first permanent duty station was at Fort Lewis, Washington, from 1976 through 1979. There he served with the 9th Infantry Division as a C-E Staff Officer for the 3rd Battalion, 60th Infantry; Platoon Leader of the Division Main Signal Center Platoon, A Company, 9th Signal Battalion, where he was responsible for supervising installation of communications for the division tactical command post; and C-E Staff Officer of the 1st Battalion, 84th Field Artillery. He was subsequently assigned to Germany where he commanded the 165th Signal Company, which provided tactical communications support to the 59th Ordnance Brigade, from 1979 to 1981. He then became Systems Control Officer for the 44th Signal Battalion (Army Area), 7th Signal Brigade, from 1981 to 1982 where he was responsible for supervising crucial SHF and UHF multichannel communications systems linking major U.S. Army Europe headquarters and planning and supervising a very effective mission evaluation of subordinate Army Area Signal Companies. Captain Shaffer anticipates further responsibilities as both a tactical communicator and as a communications-electronics engineer in his subsequent assignments.

CHAPTER 1

INTRODUCTION

A. PROBLEM STATEMENT

The bound document scanner project currently underway within the Laboratory for Information and Decision Systems uses a Fairchild F-8 Formulator Mark III programmable microcomputer as the controller for the scanner/printer system. The goal of this research is to develop an achievable architecture for a dedicated stand-alone controller and to evaluate system performance using this controller. The approach that was taken in pursuing this goal was to replicate essential features of the F-8 controller, including the hardware interface and control software, in a dedicated real-time controller consisting of a microprocessor and auxiliary circuitry.

B. SUMMARY OF THE RESEARCH GOAL

The scope of the research was constrained so that the general architecture of the existing scanner system could be retained. The control element of the system only was to be redesigned, using as simple an implementation as possible while conforming with system parameters. The system was to be transparent to the new controller in that the scanner had to continue to produce the same quality copy as obtained with the F-8 controller. A microprocessor based configuration was considered as the most promising approach toward realizing a dedicated controller. Design criteria for a microprocessor controller were drawn up after reviewing functional requirements. Essential features were delineated to ensure that the controller would at least

(1) properly interface to the scanner system, (2) be able to be removed from and replaced into the system in a modular manner to support further scanner research, (3) handle all control processes at least as quickly as the F-8 controller, (4) be able to use an EPROM memory to hold the control program, and (5) respond to operator control. Some additional features which were considered desirable, but not essential, included: (1) low component count and low cost, (2) provision for more than minimum operator control of scanning, and (3) an architecture compatible with ongoing efforts to incorporate data compression into the scanner system. Initially, the abilty of a microprocessor to meet these requirements was uncertain. Hence, a detailed analysis of the role of the existing controller and a comparative analysis of available microprocessors was necessary.

C. BACKGROUND

The bound document scanner project seeks to improve interlibrary resource sharing through use of a solid state, near real-time, facsimile facility. Requests for materials not available at one library but on hand at another are currently filled by lending-borrowing arrangements involving physical movement of documents or photocopies from one library to the other. An electronic delivery system would decrease handling times for material transfer from days or weeks to the order of hours or less; but to be viable, the system must be economically attractive. Current digital facsimile systems cannot copy pages from bound volumes or are prohibitively costly for libraries. The bound document scanner under development attempts to meet the requirements for a relatively economic, document friendly, electronic delivery system. Figure 1.1 outlines the basic

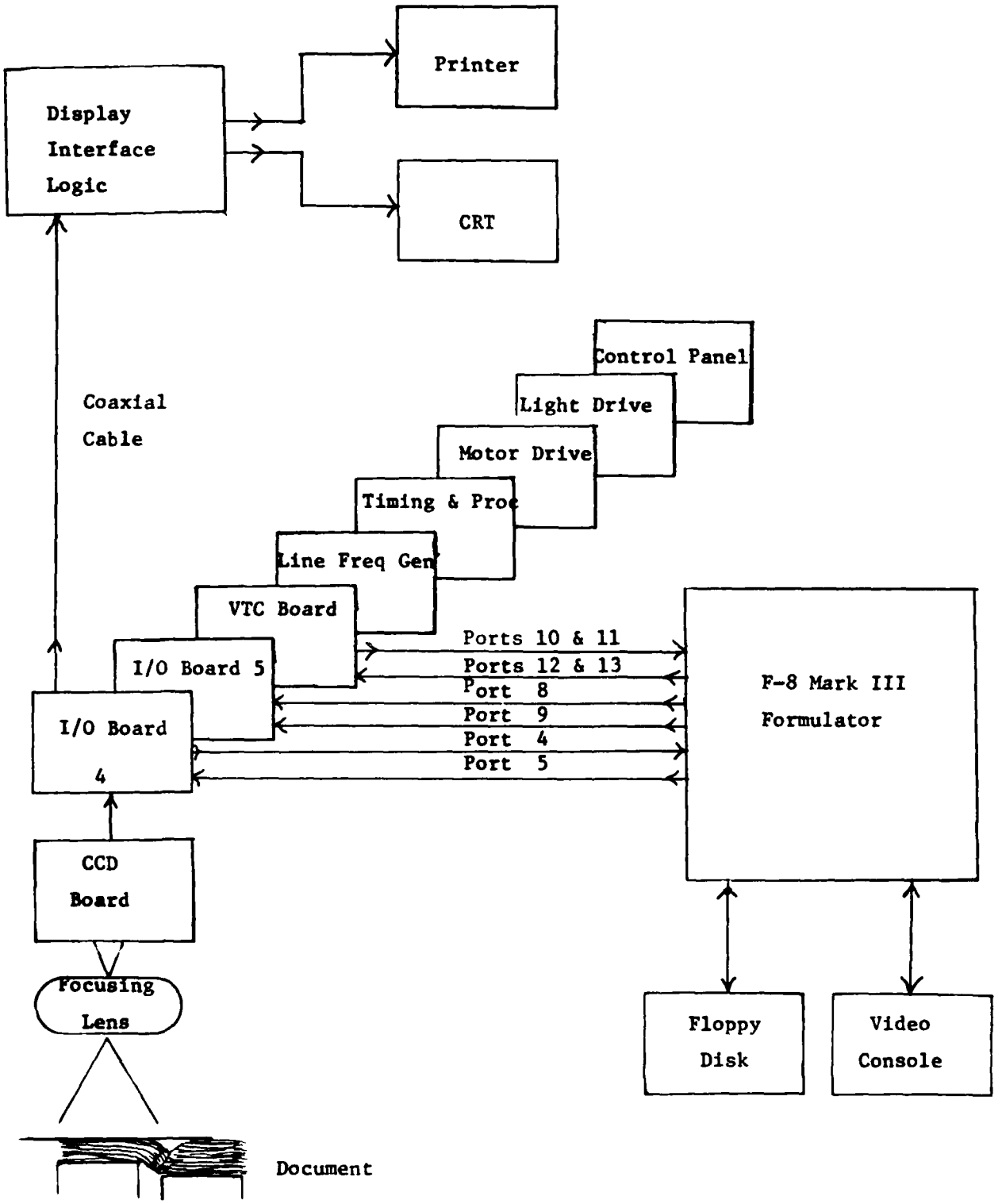


Fig. 1.1 Bound Document Scanner System

elements of the scanner system. The controller consists of the F-8 Formulator with floppy disk and video console. The controller interfaces with the scanner hardware via eight I/O ports. Images from the scanned page are focused onto the CCD which converts the image into 2048 pixels. After the pixel data are processed by the scanner hardware, they are sent to the display logic and coverted into an image on the CRT or printer.

The salient features of the scanner have been documented in several theses (see bibliography). The key component that is relevant to this research is the F-8 microcomputer. It is now being used as the system controller and has also been used as a development tool for the bound document scanner system. The F-8 Mark III Formulator consisting of a CPU Board, Console with Console Control and Console Memory Boards, a 4K PSU (F-8 ROM) Board, four 4K RAM Boards, a Parallel Interface Board, and a Quad I/O Board (Figure 1.2b) was expanded into a versatile software development station by Medley (6). By adding more I/O ports and communications interface to the F-8, he enabled addition of a Zenith-19 video terminal, modem access, and utilization of dual 8 inch floppy disk drives and a teletype terminal (Figure 1.2a). This configuration allows for rapid writing and execution of F-8 programs, such as the scanner control program, "EOPS2" (Electro-Optical Scanner Version 2). Flexible program analysis is possible using the debug capability of the F-8. Once program modules are written and debugged, they can be assembled and linked into executable programs. Programs can then be stored on disk and loaded into RAM for execution. The Disk Operating System, Version 4 (DOS4) is bootstrapped into the F-8 before commands or programs can be loaded and executed.

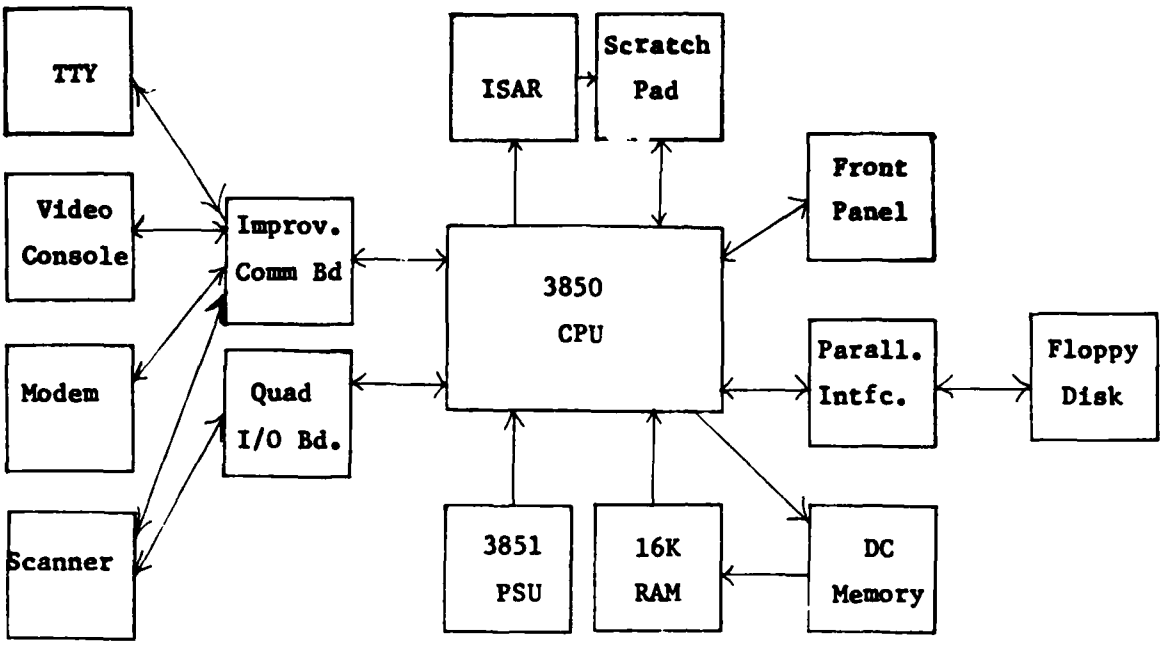


Fig 1.2a F-8 Formulator Functional Configuration

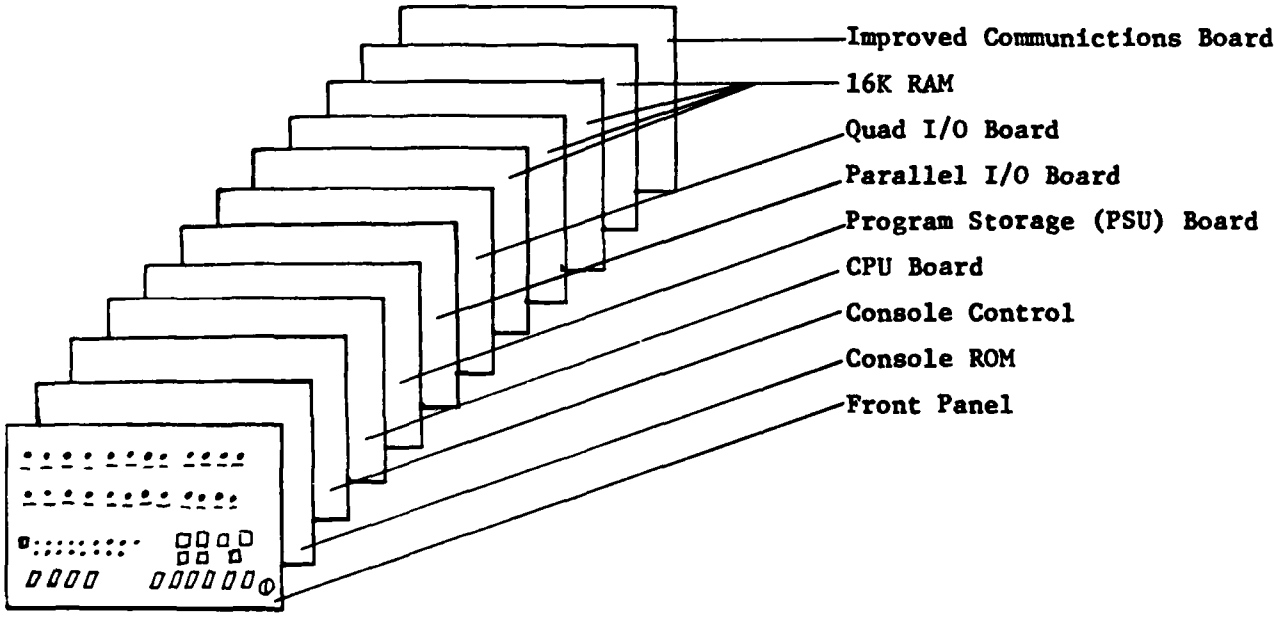


Fig 1.2b F-8 Formulator Physical Configuration

Following is a brief description of how the scanner system operates. To initiate scanning, EOPS2 is loaded after DOS4 is running. Scanning begins by pushing a start button. EOPS2 automatically starts the scanner motor, flourescent lights, and printer pumps or CRT screen erase. EOPS2 then starts the scanner moving horizontally across the page, sets the CCD pixel data threshold voltage level, and sends the CCD pixel signals to the printer or CRT for local copy. After a page scan EOPS2 reinitializes all devices.

D. RESEARCH PLAN

Thesis research comprising development of the dedicated controller included the following tasks:

1. A thorough anlaysis of the interface between the scanner hardware and EOPS2 software was conducted to identify the existing control sequence.

2. The general requirements for controller design were identified and reviewed with respect to the general capabilities of microprocessors.

3. A number of microprocessors were examined to compare features relevant to the controller application.

4. The most consuming task consisted of the design and implementation of the controller circuit. This included necessary hardware modifications and interface specifications for the scanner; software modifications to EOPS2; phased testing of the interface hardware and software; and test and evaluation of the final controller.

The important aspects of control interface, controller design, software modifications, and operating instructions are documented in

this report.

E. SUMMARY OF RESULTS

A microprocessor based controller was designed and implemented using the MOSTEK MK38P70 microprocessor. The controller meets all design criteria and has an architecture superior to other possible configurations for this application in that it has a simple memory interface, low chip count, and uses F-8 assembly language. Two support chips, Intel 8255A Progammble Peripheral Interfaces (PPIs), provide a simple yet effective interface between the MK38P70 and the scanner. A 2Kx8 bit Erasable Programmable Read-Only-Memory (EPROM) holds the controller program MEOSC (Microprocessor Electro-Optical Scanner Control) which is a modified version of EOPS2. The controller circuit was incorporated into existing scanner hardware along with a threshold monitor and adjust circuit which permits precise control of CCD pixel data thresholding.

System performance using the MK38P70 controller has been excellent. The scanner continues to provide quality hard (printer) and soft (CRT) copy with the new controller. The scanner system is much more streamlined with the dedicated controller in place, and the F-8 Formulator has been released for more general purpose work.

F. OVERVIEW OF FOLLOWING CHAPTERS

Chapter 2 presents the F-8/scanner control interface analysis. This information is needed for implementation of the control function and is used to develop controller requirements and the scanner interface. Chapter 3 discusses the relative merits of the microprocessors considered for the controller and the basis for a final choice among them. A practical design is presented in Chapter 4;

it includes necessary hardware, software, and scanner modifications. Chapter 5 is devoted to a discussion of the testing and evaluation of controller performance. Results, conclusions and recommendations for further research are included in Chapter 6.

CHAPTER 2

SCANNER/F-8 INTERFACE ANALYSIS

A. INTRODUCTION

The primary goal of the research is to replicate the functions of the current F-8 controller in a stand-alone dedicated microprocessor; it is not the intention of the project to overhaul the software and over-all system design. As a means of understanding the requirements for the dedicated microprocessor controller, there is presented in this chapter a detailed analysis of the hardware and software features incorporated into the current F-8/scanner/display system.

The bound document scanner is controlled by the interfaces between logic hardware that is part of the scanner and display circuitry, and F-8 program instructions, EOPS2. Eight F-8 input/output (I/O) ports and one front panel port (internal to the F-8) provide the logical and physical connections between the F-8 Central Processing Unit (CPU) and the scanner and display hardware. The analysis to follow focuses on the interplay between hardware and software as they relate to scanner control rather than on a detailed explanation of each logic component or program instruction. Included is a functional description of the control scheme for the F-8/scanner/display system.

A number of conventions will be used in the descriptions of circuit and software operation. A signal which is active when driven to a low voltage level (-0.3 to 0.8 volts d.c.), that is, "LO", will be designated in capital letters with an overbar across the top of the

designation. For example, $\overline{\text{SEND}}$ is a low going pulse generated by the F-8 which enables data transmission between the scanner and the display logic. A signal which is normally active when at a high voltage level (2.4 to 5.8 volts d.c.), that is, "HI", will simply be designated in capital letters. Occasionally, program subroutines will also be referred to in mnemonic form, also in capital letters; for example FSTLN is an EOPS2 subroutine which returns after detecting the first line of valid CCD data. The F-8 uses inverted logic, that is, logic 0 is HI and logic 1 is LO. For convenience, reference is often made to data in hexadecimal notation, or HEX. The first character in the HEX notation corresponds to the four most significant bits of an 8-bit data word (bits 7,6,5, and 4); the second character corresponds to the four least significant bits (bits 3,2,1, and 0).

B. SOFTWARE DESCRIPTION

As previously explained, the F-8 scanner control program is named EOPS2 (Electro-Optical Scanner Program, Version 2). EOPS2 uses three F-8 I/O ports as input ports (Ports 4, 10, and 11), five F-8 I/O ports as output ports (Ports 5, 8, 9, 12, and 13), and one port normally internal to the F-8 (Port 0). EOPS2 has two main functions: (1) Finding and setting an optimum threshold level for digitizing CCD pixel data, and (2) generating commands for control of the local printer and CRT and ensuring proper transmittal of commands and CCD data over the coaxial cable connecting the scanner to the display logic. Detailed flow charts of the EOPS2 functions are contained in Appendix A and a complete program listing can be found in Stanton's thesis (10). This chapter focuses on the salient features of EOPS2; a summary flowchart is included for reference (Figure 2.1). The general

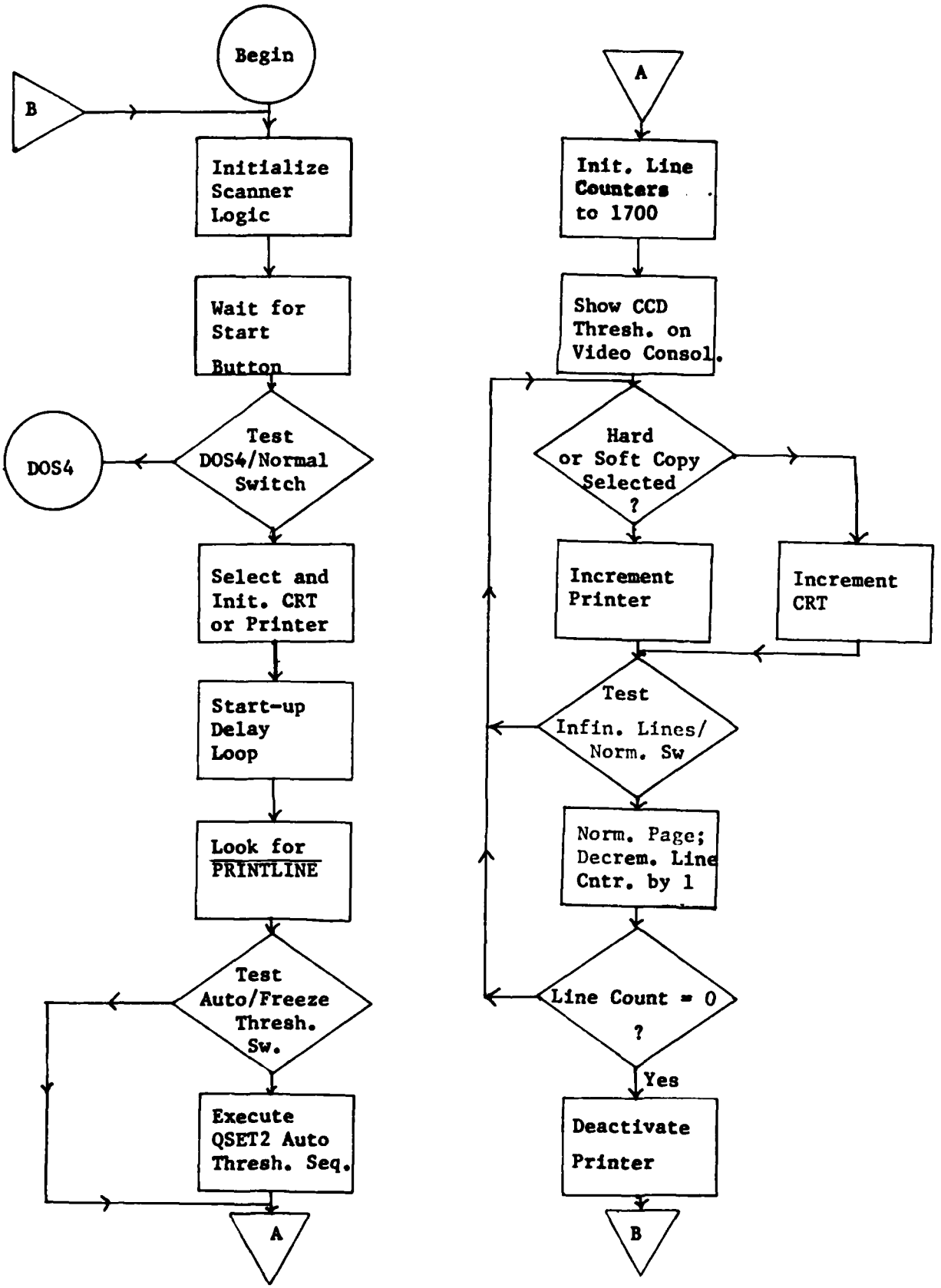


Fig. 2.1 EOPS2 Summary Flowchart

sequence of events is as follows:

1. Once EOPS2 has been loaded into memory by the user, program execution begins. All logic on the scanner and display logic circuitry is then initialized or reset. The program next goes into a "wait loop" until the operator positions a document on the scanner and pushes the start button on the scanner control panel. A corresponding $\overline{\text{START}}$ signal is detected via input Port 4, which then allows the program to leave the wait loop.

2. EOPS2 polls two sense switches located on the front panel of the F-8 which are tied to Port 0. The "Return to DOS4 (Disk Operating System)/Normal" switch, tied to bit 4 of Port 0, must be down (logic 0) for EOPS2 to continue; otherwise, EOPS2 execution is aborted. The "Hard/Soft Copy" switch, tied to bit 7, selects the printer or CRT as the destination of scanner copy. The chosen display is then initialized by the XMITS subroutine.

3. A start-up delay loop allows the scanner flourescent lights to preheat, and the phase-lock-loop-controlled motor's speed to stabilize. CCD pixel data is ignored until the subroutine FSTLN returns a signal called $\overline{\text{PRINTLINE}}$, which indicates the detection of images from the scanned document.The presence of $\overline{\text{PRINTLINE}}$ is detected by input Port 4.

4. The "Automatic/Freeze Threshold" switch on the front panel of the F-8 (bit 6 of Port 0) is polled, and an automatic thresholding algorithm, subroutine QSET2, is either executed or skipped. QSET2 samples a calibration pattern superimposed over the left margin of the document page. This calibration pattern allows QSET2 to establish the maximum black-to-white pixel transition count observed during the

first 28 scan lines. This maximum transition count sets an optimum level for digitizing CCD pixels into either zeroes or ones, corresponding to white or black. In general, the maximum count is obtained by comparing the transition count for the current line to that of the preceding line; the larger count is retained for comparison with the count obtained on the next scan. The transition count is detected by counters on the Video Thresholding Circuit (VTC) board and passed to the F-8 by Ports 10 and 11. The final maximum count is converted to a voltage level corresponding to a voltage threshold setting on the VTC board. QSET2 concludes after this level has been found by the F-8 and the setting has been passed to the VTC board by Ports 12 and 13. Ten signal lines are needed, eight from Port 12 and two from Port 13, to send the voltage threshold setting from the F-8 to the VTC board; the state of these lines (HI or LO) corresponds to three HEX characters. During this time, the HEX notation is converted to AASCI code for transmission to the Zenith console. The console displays a message denoting the current threshold level. While QSET2 is executing, no data are sent to the displays.

5. Once the optimum threshold has been locked in, either as a result of QSET2 or the previous threshold value (FREEZE), line counters are initialized to begin counting down 1700 lines of CCD data. This count corresponds to a page width of 8.5 inches (200 lines per inch). The printer or CRT displays each scan line of digitized CCD data in real time after the data on each of the 2048 pixel elements has been transferred out of the device. Display-control commands and digitized CCD data are transmitted over coaxial cable by I/O Board 4 to the display logic. Output Port 5 is connected to I/O Board 4 and

controls the switching of CCD data and commands over the coaxial cable. Display-control commands are presented to I/O Board 5 by Output Ports 8 and 9 which are activated by the subroutine XMITS. Display commands consist of a device address and command (such as Hard Left Margin Justify) which are converted into a serial format by I/O Board 5 for transmission. Appropriate commands enable and increment the displays after each line of CCD data is received by the display logic. The subroutine ENDLN senses the end of a CCD line via Input Port 4 in order to initiate command generation.

6. After the 1700 lines comprising a page have been counted down and printed, EOPS2 checks the "Normal/Infinite Lines" switch (bit 5 of Port 0). If normal operation is selected, the printer is shut off and the F-8 software resets to await another push of the start button. The scanner carriage mechanically returns to its starting position at the left side of the document. The choice of infinite lines allows a constant stream of CCD data and increment display commands to be sent to the displays while the scanner carriage is held stationary in order to make tests and adjustments.

There are several timing critical features of EOPS2 which merit highlighting:

1. Delay loops are needed for start-up of the scanner flourescent lights and motor and for printer/CRT start up. The approximately 1.5 seconds allocated is adequate to initialize all devices.

2. The subroutine QSET2 must read the black-to-white transition count in a CCD line and write a current threshold level to the VTC Board within a 900-microsecond idle time between CCD lines.

Figure 2.2 shows that during a clockout period, the CCD pixels produce an analog waveform which takes up only about 2.6 milliseconds of the 3.5 millisecond period. QSET2 currently uses about 300 microseconds to perform thresholding between each of the first 28 scan lines.

3. Display commands must also be generated, transmitted, and received by the display logic during the 900-microsecond idle time between CCD lines. An 18-microsecond delay has been allocated as a buffer after transmittal of commands in order to give the display logic, printer and CRT time to process and respond to the command. Approximately 400 microseconds are used between lines for soft copy (CRT) and approximately 600 microseconds are used for hard copy (printer) in processing commands.

4. Analog CCD data is valid for approximately 2.6 milliseconds, as shown in Figure 2.2. The signal PRINTLINE is detected by subroutines FSTLN and ENDLN to correspond to the period when CCD pixel data are present. Proper timing of the PRINTLINE signal is crucial since it is this signal which is sensed by Port 4 which, in turn, triggers alternation of CCD and command data over the transmission line.

The point to be emphasized about timing is that any program modifications must be executable during the 900-microsecond idle time between CCD lines. Modifications must allow for equipment delays where appropriate and they must fit into the page scan time of approximately 6 seconds.

C. HARDWARE DESCRIPTION

The hardware interface between the scanner and the F-8 is contained on three circuit boards located on the scanner. These are

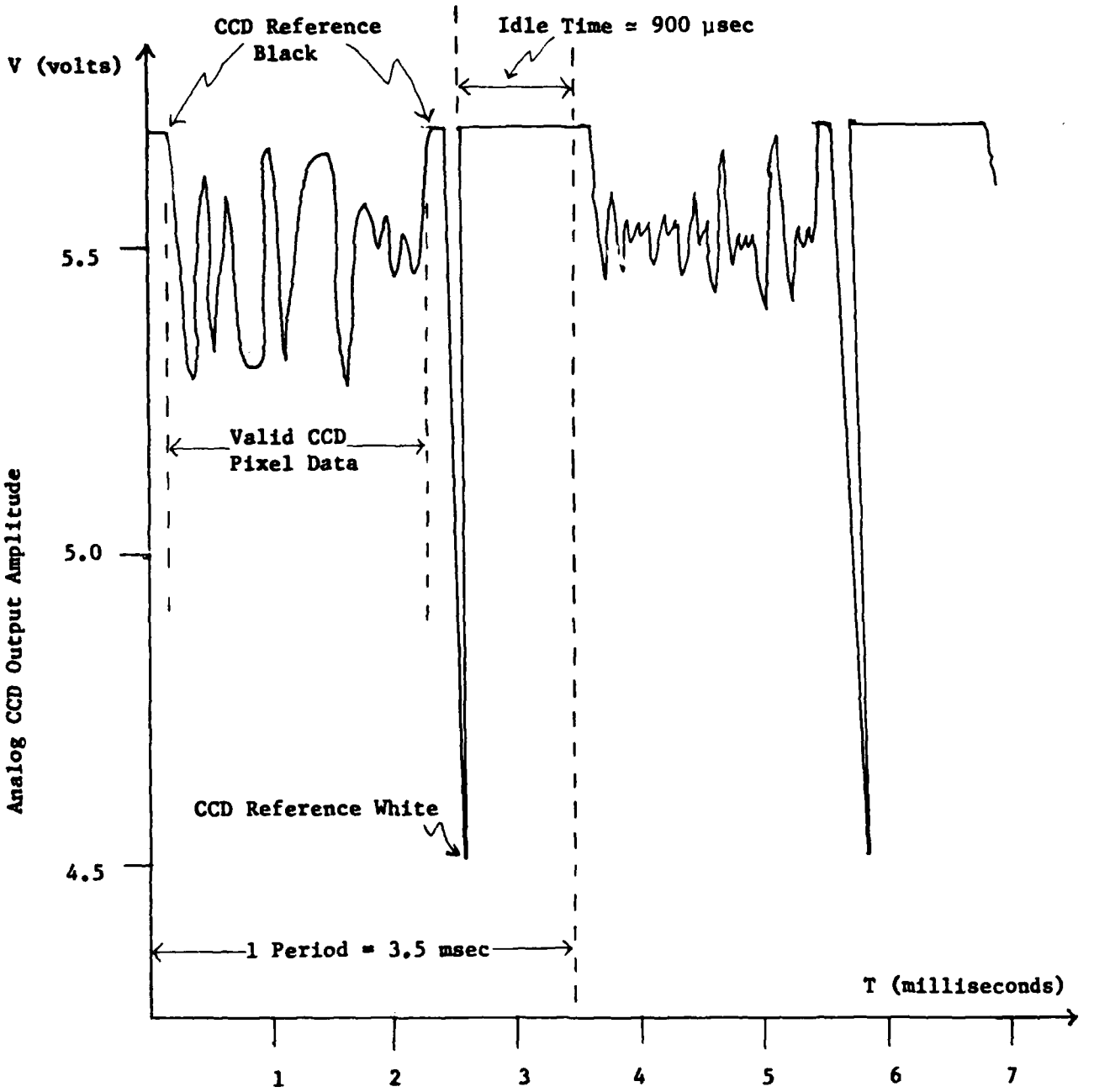


Fig. 2.2 Analog Representation of CCD Output

named I/O Board 4, I/O Board 5, and the VTC (Video Thresholding Circuit) Board. Block diagrams of these boards are shown in Figures 2.3, 2.4, and 2.5, respectively. This section briefly describes the functions of these boards as they relate to scanner control.

1. I/O Board 4 is the transmission line driver and CCD interface board. Its function is to send CCD line data and display commands over the coaxial cable to the display logic, and to sense the signals $\overline{\text{START}}$ and $\overline{\text{PRINTLINE}}$. At any given time, the board will perform only one of three functions; these functions are initiated by the F-8 over Port 5 (Output). The three most significant bits of Port 5 are connected to a 3-to-8 decoder on the board. A HEX value sent by the F-8 pulls one or more of the three lines LO (logic 1) in order to select one of the output lines of the decoder for enabling the chosen function. Only 3 of the 8 output lines of the 3-to-8 decoder are required by the current scanner; the remainder of the 8 lines were used in a previous application. The HEX values sent by the F-8 are:

a. H'00': Enable Command Transmit (ENCMD). This value opens the transmission line to display commands. Display commands are generated by I/O Board 5. They are coupled to the coaxial cable by line drivers on I/O Board 4.

b. H'20': Enable CCD Transmit (ENCCD). This value closes the transmission line to display commands and allows the digitized CCD line data to be transmitted.

c. H'40': Enable Port 4 Sensing (ENSENS). This value allows F-8 Port 4 to poll I/O Board 4 for the presence of $\overline{\text{START}}$ and $\overline{\text{PRINTLINE}}$. The four least significant bits of Port 4 are connected to NAND gates on I/O Board 4 which are enabled while ENSENS is active.

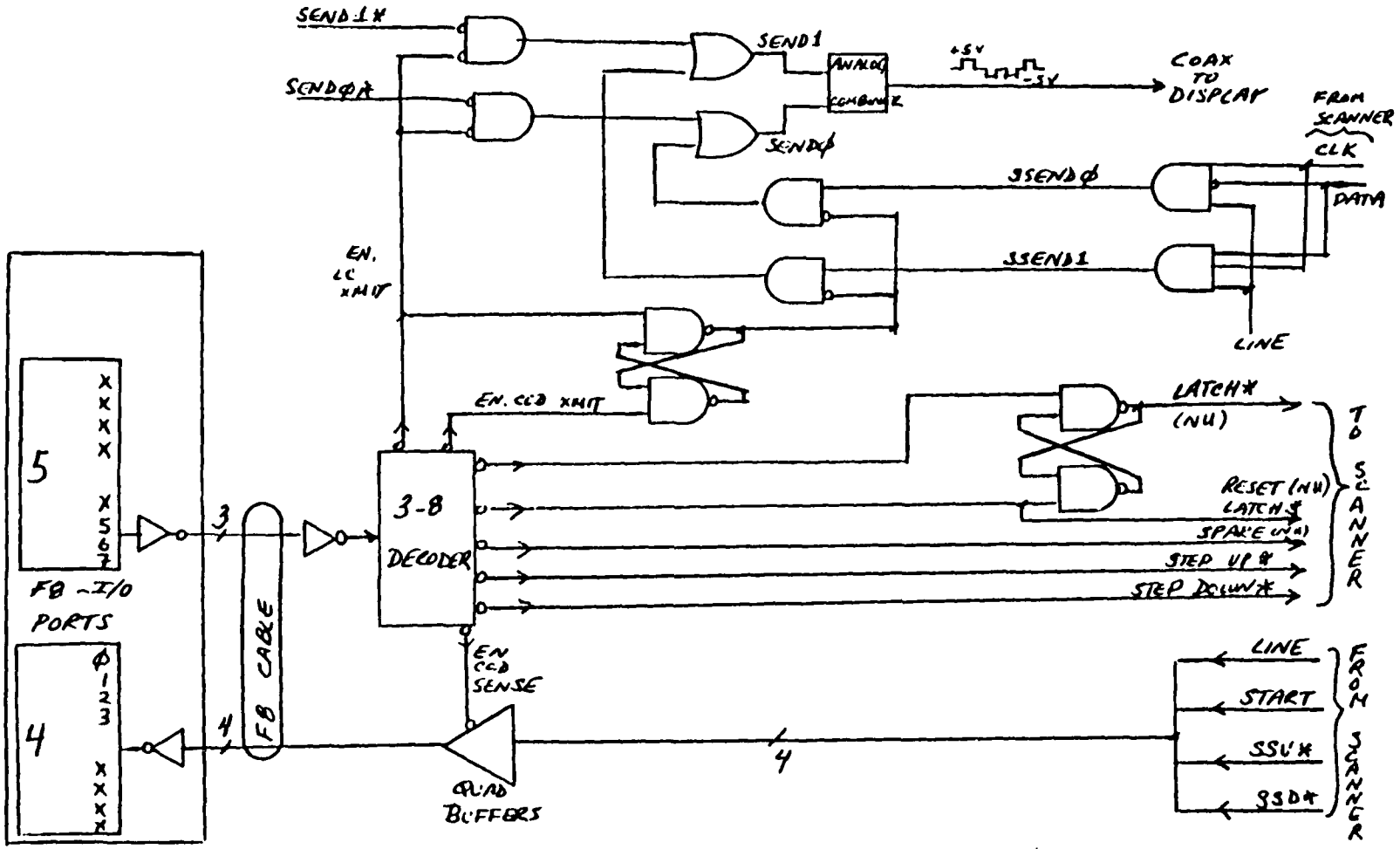


Figure 2.3 F8 - I/O BOARD 4 LOGIC DIAGRAM *

Board 4 buffers input and output lines to the scanner electronics and switches image data and commands onto the display channel.

* **Extracted from Keverian (4).**

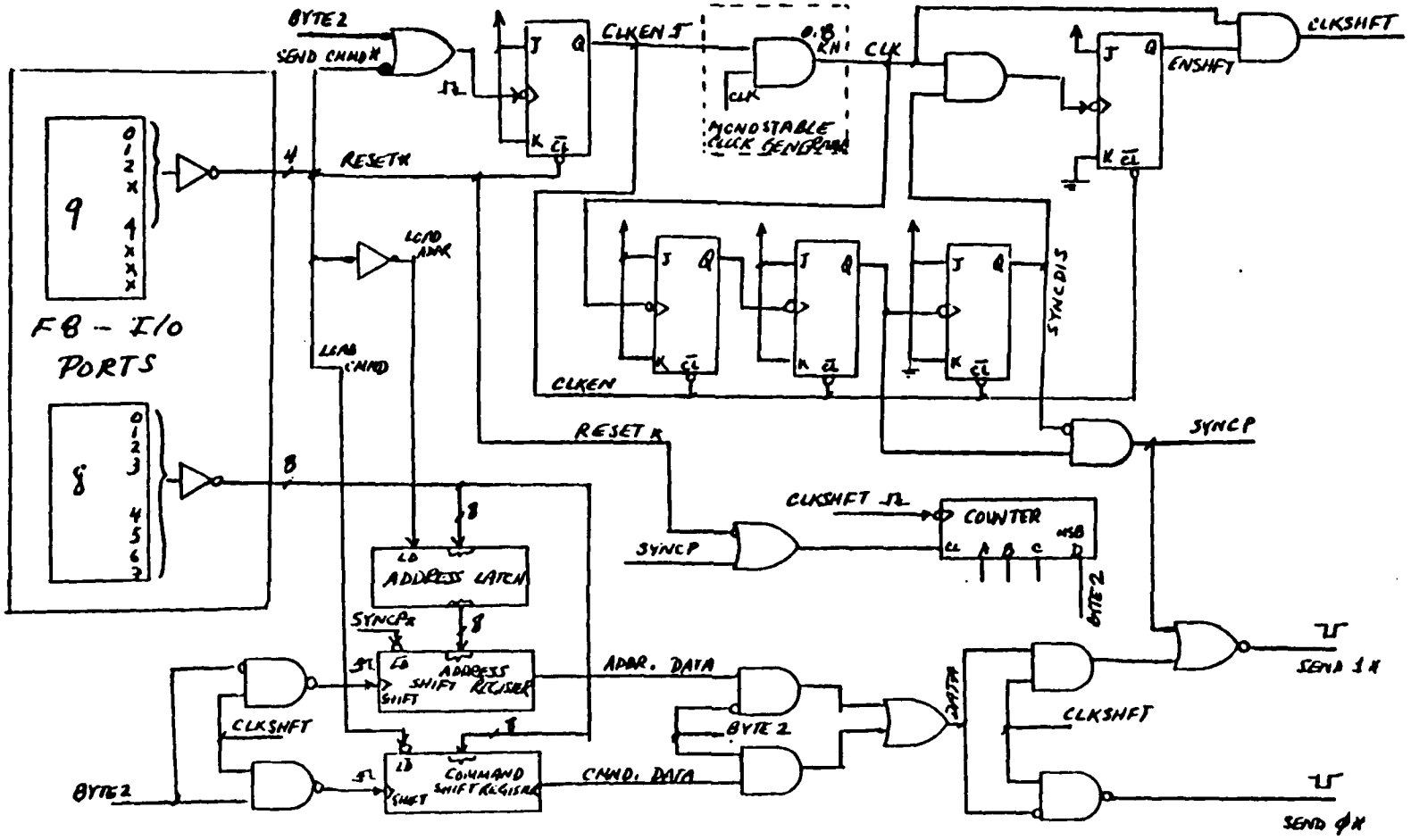


Figure 2.4 F8-I/O BOARD 5 LOGIC DIAGRAM *

Board 5 performs most of the encoding of the parallel data from the F8 into the serial communications protocol of the display channel.

* **Extracted from Keverian (4).**

Only two of the four input lines to these gates are used in the scanner application. $\overline{\text{PRINTLINE}}$ is tied to the gate connected to bit 0 of Port 4; $\overline{\text{START}}$ is tied to the gate connected to bit 1 of Port 4.

Note that I/O Board 4 is relatively simple; it contains only the 3-to-8 decoder, line driver, AND gates and inverters as its major components. A number of additional gates and inverters are contained on the board but they are not required for the present scanner configuration.

2. I/O Board 5 is the synchronization/display address/display command generation board. Its sole purpose is to generate control characters in the proper sequence for display control. The synchronization pulse, display address, and display command are combined into a serial bit stream. Port 8 (Output) first places the display address from the F-8 onto input pins of the address latches. Port 9 sends a "Load Address" signal ($\overline{\text{LDADDR}}$ = H'08'), which is tied to the address latches, in order to load the address into the latches. Port 8 next presents an appropriate display command to the inputs of the command shift register. (A latch is not used since Port 8 will maintain the display command levels at the shift register until another output operation occurs at Port 8.) Port 9 then loads the command shift register with the "Load Command" signal ($\overline{\text{LDCMD}}$ = H'10'). Finally the signal $\overline{\text{SEND}}$ (H'02') is given by Port 9 to generate a 2.4 microsecond synchronization pulse. $\overline{\text{SEND}}$ also activates the shift clock and transmit clock which clock out the display address and command serially from the address and command shift registers. A $\overline{\text{RESET}}$ signal (H'01') sent by Port 9 resets all logic on the board to await

the next command initiation. The zero bits are physically separated from the one bits by several gates and an inverter when they leave I/O Board 5 so that they can be combined by the I/O Board 4 line driver. A summary of the logic signals sent to I/O Board 5 is shown below:

a. Port 8:

(1) Display Addresses:

H'01' $\overline{\text{ADHARD}}$ Printer

H'08' $\overline{\text{ADSOFT}}$ CRT

(2) Display Commands:

(a) Printer:

H'08' $\overline{\text{HARDLMJ}}$ Start printer

H'00' $\overline{\text{HARDFIL}}$ Fill line with blanks

H'03' $\overline{\text{HARDADV}}$ Advance paper one line

H'0F' $\overline{\text{HARDCUT}}$ Cut paper

H'37' $\overline{\text{HARDOFF}}$ Clear/shut-off printer

(b) CRT:

H'06' $\overline{\text{SOFTEN}}$ Enable CRT

H'03' $\overline{\text{SOFTDSB}}$ Disable CRT

H'01' $\overline{\text{SOFTERS}}$ Erase CRT

H'02' $\overline{\text{SOFTRSY}}$ Reset Y axis counter

H'04' $\overline{\text{SOFTINY}}$ Increment Y axis

b. Port 9:

H'01' $\overline{\text{RESET}}$ Resets logic on board

H'02' $\overline{\text{SEND}}$ Generates synch. and bit stream

H'10' $\overline{\text{LDCMD}}$ Loads display command

H'08' $\overline{\text{LDADDR}}$ Loads display address

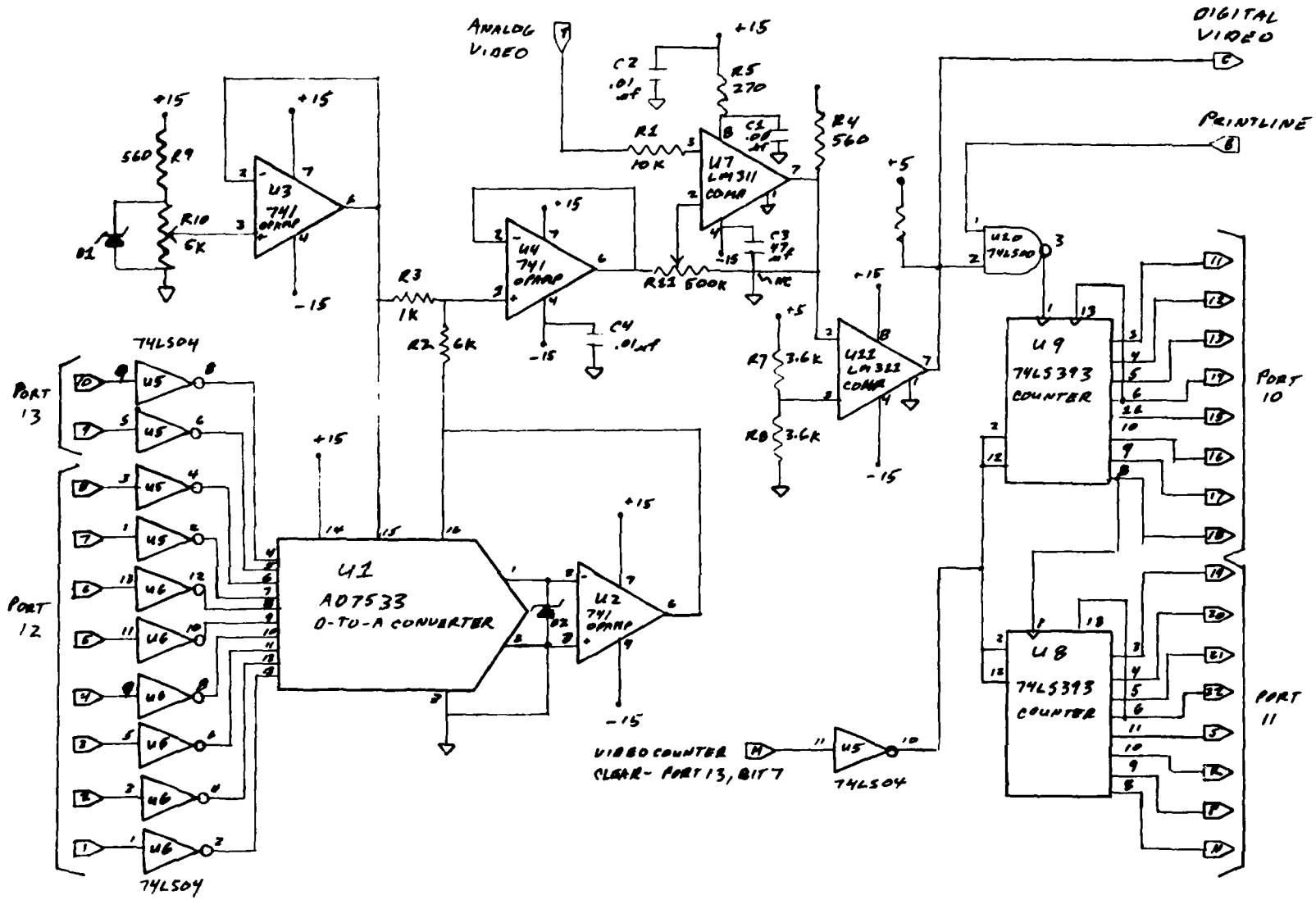


Fig. 2.5 Video Detection and Thresholding Circuit (VTC Board) *

* Adapted from Stanton (10).

Proper generation of the serial bit stream requires a precise timing sequence, which is controlled by the clocks on this board. A detailed discussion of this timing can be found in Keverian's thesis (4).

3. The VTC Board selects and sets the optimum voltage threshold level for digitizing CCD pixel content into either black or white. QSET2 passes an initial level via Ports 12 and 13 to a digital-to-analog converter. The converter, in conjunction with three OPAMPS, converts the level to a scaled value in the range of 5.14 to 6.16 volts in increments of 1 millivolt per digital step. Two comparators convert the CCD pixel content to logic 1 or 0 (black or white) depending on the threshold voltage applied to the comparators. The number of black-to-white transitions in a CCD line at the current threshold level are counted by two digital counters. This count is sent to the F-8 by Ports 10 and 11. QSET2 compares this transition count to the current maximum. After 28 CCD scan lines are checked, the threshold level is fixed and the function of the board is complete. The transition counters are reset by bit 7 of Port 13 while the correct threshold level is maintained for the remainder of a scanned page by all eight bits of Port 12 and bits 0 and 1 of Port 13.

D. PORT UTILIZATION

The scanner application requires the use of eight F-8 I/O Ports (and one internal F-8 Port). This requirement calls for careful consideration in moving from an F-8 controlled system to a microprocessor controlled system, since most microprocessors cannot provide this capability without a number of support chips. The purpose of this section is to delineate the current port utilization scheme and to discuss options for combining the functions of these ports as a

Table 2.1 - Summary of I/O Port Control Transactions Between F-8 and Scanner

SEQUENCE OF PORT OPERATIONS IN SCANNER CONTROL

ACTION	PORT
Reset display command generator logic on I/O Board 5	9 (Out)
Enable transmission of display commands through I/O Board 4	5 (Out)
Enable Port 4 to sense logic on I/O Board 4	5 (Out)
Look for push of start button	4 (In)
Check "Normal/DOS4" switch for normal operation	0 (Int)
Check for release of start button	4 (In)
Check "Hard/Soft" switch for selecting display	0 (Int)
Put display address on I/O Board 5	8 (Out)
Load address into latches and shift register on I/O Board 5	9 (Out)
Put display command on command shift register on I/O Board 5	8 (Out)
Load display command into shift register on I/O Board 5	9 (Out)
Generate SEND to transmit synchronization pulse, display address, and display command serially	9 (Out)
Look for beginning, then end, of a CCD line via I/O Board 4	4 (In)
Check "Automatic/Freeze Threshold" switch and start subroutine QSET2	0 (Int)
Clear black-to-white transition counters on VTC Board	13 (Out)
Put current threshold level on VTC Board	12 and 13 (Out)

Table 2.1 - Summary of I/O Port Control Transactions Between F-8 and Scanner (Cont.)

Input transition count from CCD line and compare against current maximum	10 and 11 (In)
Set final threshold level on VTC Board	12 and 13 (Out)
Open transmission line to display commands via I/O Board 4	5 (Out)
Start printer or CRT using XMITS subroutine	8 and 9 (Out)
Open transmission line to CCD line data via I/O Board 4	5 (Out)
Enable Port 4 to sense logic on I/O Board 4	5 (Out)
Look for end of CCD line (PRINTLINE) in order to stop printing	4 (In)
Close transmission line to CCD data and open it to display command	5 (Out)
Advance display by one line using XMITS subroutine	8 and 9 (Out)
Check "Infinite/Normal Lines" switch for normal operation	0 (Int)
Shut off printer/CRT after 1700 CCD lines using XMITS subroutine; program then resets	8 and 9 (Out)

basis for a more efficient controller architecture. Table 2.1 provides a summary of the logic functions performed by the F-8 ports for scanner operation as discussed in the previous sections.

The F-8 Ports are connected to the scanner hardware on a bit-by-bit basis. F-8 port lines are non-tri-state, bidirectional in nature which makes it impractical to tie both output and input lines to the same bit directly. This lack of buffering of input from output is part of the reason why so many ports are used in the scanner application. As mentioned previously, some of the ports are not used to their capacity; for example I/O Board 4 uses only three out of eight bits from Port 5 and only two out of eight bits from Port 4. A more efficient allocation would be to break the port into two 4-bit ports; however, this cannot be accomplished without additional external components since an input or output instruction affects all eight bits of the port. Table 2.2 breaks out the F-8 ports used by the scanner. As it stands, this table indicates that an arrangement consisting of five 4-bit ports and four 8-bit ports would be more efficient in terms of bits used compared to bits allocated.

Table 2.2 - F-8 Port Allocation for Scanner Application

PORT AND USE	NUMBER OF BITS USED	CONNECTED TO
0 (Input)	4	F-8 Front Panel (Internal)
4 (Input)	2	I/O Board 4
5 (Output)	3	I/O Board 4

8 (Output)	8	I/O Board 5
9 (Output)	4	I/O Board 5
10 (Input)	8	VTC Board
11 (Input)	8	VTC Board
12 (Output)	8	VTC Board
13 (Output)	3	VTC Board

TOTAL PORTS USED	TOTAL BITS USED	OUTPUT BITS	INPUT BITS
9	48	26	22

A number of options are available for a more efficient port scheme. Before any particular microprocessor was considered for use in the dedicated controller, some port reduction possibilities were studied that were compatible with the F-8 architecture. Each alternative was evaluated in terms of the hardware and software complexity it would add to the scanner system. The results are presented below.

1. Use of a Programmable Interface. A programmable interface device can be used to combine ports. A number of programmable interface devices are available from different manufacturers; some can only be used with a computer of similar architecture, while others are universal in application. A programmable interface normally has some type of a data bus and control signals as interface to the computer and several ports which can be used as inputs or outputs or both. For example, if such a device were used with the F-8, one F-8 8-bit port

would provide data transfer by connecting it to the device data bus, while several pins of another F-8 port would provide control. In this manner, three or four ports (depending on the device) are achievable by using only two ports. This is illustrated in Figure 2.6. Here three ports are used, one for control and two for data transfer, to obtain six ports. Some programmable interfaces also have 4-bit port options. In using a peripheral interface additional software must be used, as compared to a direct port interface, in order to tell the device which interface port to write data to or read data from.

2. Expanding Outputs. One method of expanding output ports is shown in Figure 2.7. Dual 4-bit latches are tied to the bits of a data transfer port. Another port is used to select and enable the appropriate latch. As shown, up to 28 output lines can be realized by using two ports; more output lines can be realized by additional hardware. As with the previous scheme, additional instructions are needed by the control port, and output port instructions must be modified into latch instructions. All required output bits (26) needed for the scanner can be obtained in this manner; i.e., the functions of F-8 Ports 5, 8, 9, 12, and 13 could be combined into two ports. Additionally, the latches can be used as either 4-bit or 8-bit output ports.

3. Combining Inputs. All input lines of the scanner can be combined into two ports in a manner complementary to expanding outputs. Again, only a control port and data transfer port are required. Instead of latches, input multiplexers are used. Eight 16-input line multiplexers can provide eight 8-bit input ports.

4. Simultaneous Expansion/Combining of Outputs/Inputs. This

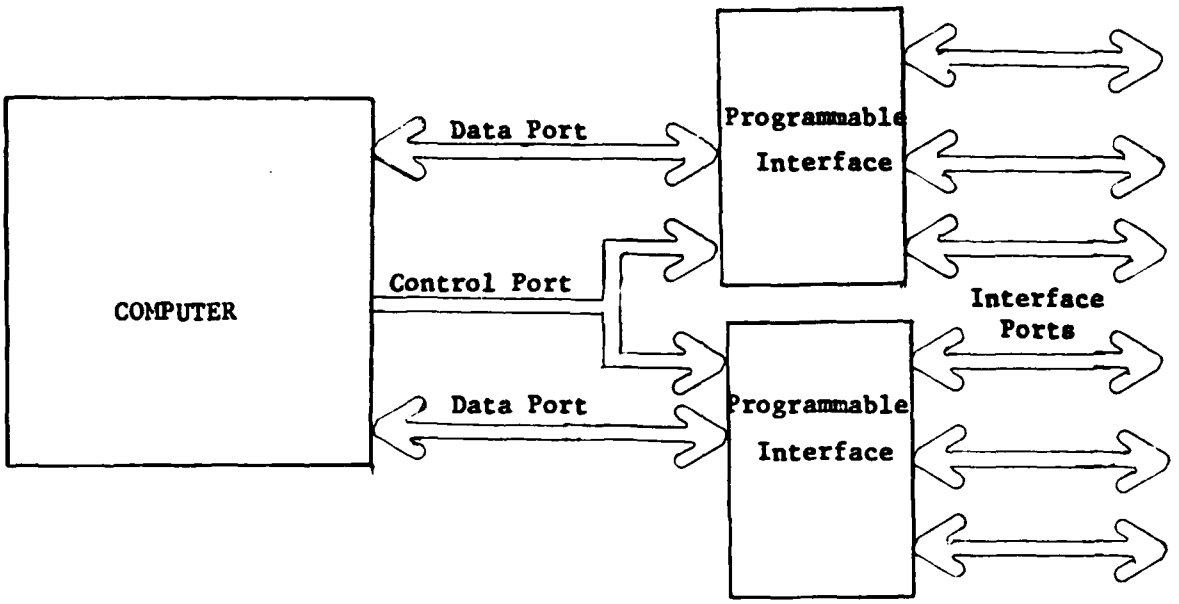


Fig. 2.6 Use of a Programmable Interface

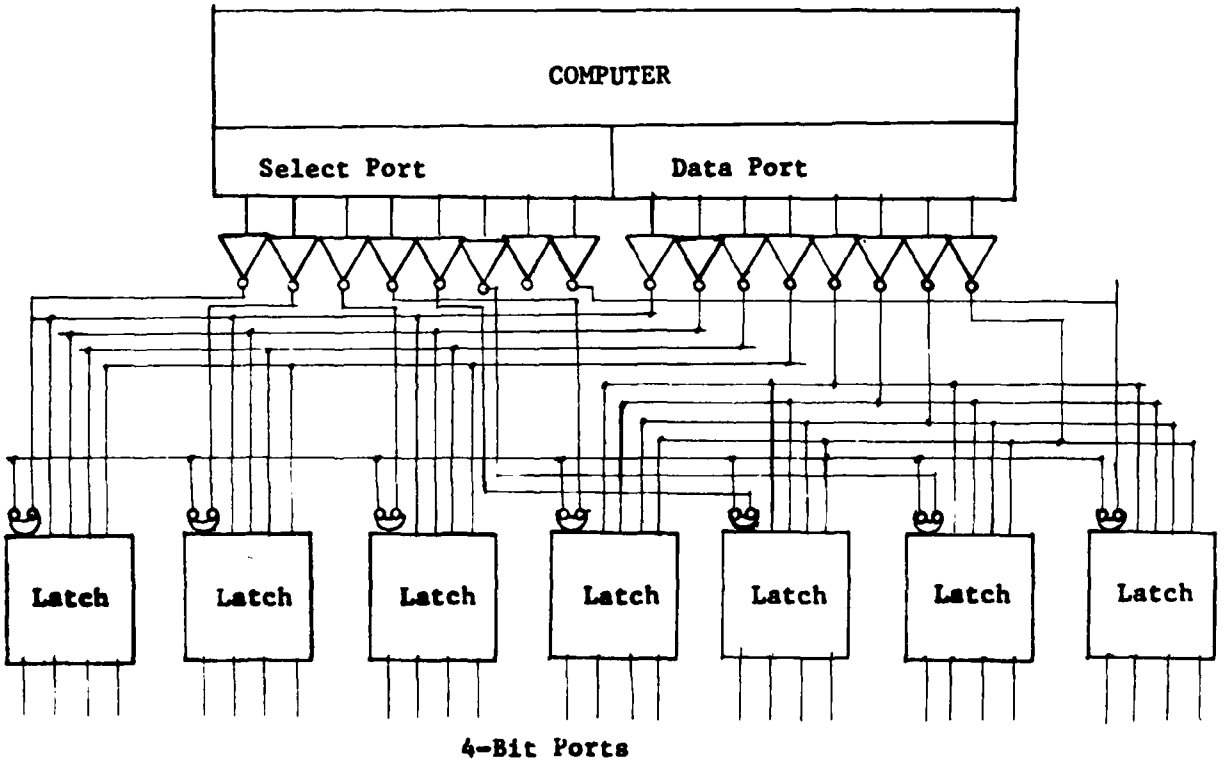


Fig. 2.7 Expanding Outputs

alternative uses tri-state buffers for input/output. As before, a data transfer and control port are needed to select appropriate buffers and control direction of data flow. Although it uses less hardware than options 2 or 3, software modifications required are more complex.

Of the above four port combination alternatives investigated, the use of a programmable interface appeared most promising. Only two chips are needed to combine all F-8 ports into a four F-8 port arrangement for the scanner application. The hardware interfacing and addition of control instructions can be straightforward with the proper device. Additionally, this number of ports (4) is on the order of those available with microprocessors. The following chapters pursue the implications of scanner interfacing in greater detail.

CHAPTER 3

MICROPROCESSOR ANALYSIS

A. GENERAL

The concept of substituting a dedicated controller in lieu of the F-8 in the scanner application required an investigation of options. A microprocessor-based configuration was quickly chosen over a strict hardware (transistor-transistor logic) configuration, primarily because a microprocessor has programming flexibility, lower chip count, and simpler connections. Choice of an appropriate microprocessor required a further investigation of features available in light of the dedicated controller requirements. Trade-offs among various microprocessors were also considered. This analysis was made before a detailed design was attempted. At the outset, the scope of possible choices was narrowed to 8-bit devices since the F-8 is an 8-bit machine and it was clear that an 8-bit chip was capable of doing the job. Also the characteristics and applications of 8-bit devices are well documented, and support chips are widely available. The microprocessors evaluated here were considered either because of their compatibility with, or similarity to, the F-8 architecture, or their popularity and availability. Although ultimately, any of the microprocessors discussed here probably could be used, the final choice resulted in an architecture which allowed a straightforward transition from the F-8 to the dedicated controller.

B. CONTROLLER CRITERIA

Some of the salient considerations in the controller design

were outlined in Chapter 1. To reiterate, the main goal was to find a simple design, that is, an ability to transfer the essence of the F-8/scanner interface into a dedicated controller with minimum system reconfiguration. This goal, when considered along with the results of the F-8/scanner interface analysis (Chapter 2), led to the following list of essential and desirable features which served as criteria against which microprocessors could be judged.

1. Essential Features:

a. The microprocessor and supporting chips must combine the functions of the nine ports (eight I/O and one internal) used by the F-8 into a lesser number of ports consistent with the port capacity of the given microprocessor.

b. A clear-cut method had to be devised for switching back and forth between the dedicated controller and F-8 in order to support further research with the scanner. This represented a special constraint associated with the laboratory environment.

c. The microprocesor had to be capable of executing instructions within time constraints, as outlined in Chapter 2. In particular, automatic thresholding and the sequence of display commands had to execute within the 900-microsecond idle time between clockout of CCD lines.

d. An EPROM (Erasable Programmable Read-Only Memory) based memory for the controller was considered to be an essential feature in order to accommodate future program improvements in the laboratory setting. EOPS2 requires about 800x8-bits of memory; hence, a standard 2Kx8-bit EPROM was considered to be more than adequate for holding the dedicated controller program.

e. As a minimum, an interface between the controller and operator was needed with the capability to start and stop the control program, to choose between automatic or frozen thresholding of the CCD line data, and to choose between hard or soft display.

2. Desirable Features:

a. A need for a relatively low chip count derived from a desire for a relatively simple port interface and simple circuit connections.

b. Low cost was considered desirable, but not the most important criterion. The goal was to keep the total cost of the microprocessor, support chips, and additional hardware needed for the controller and scanner modifications on the order of several hundred dollars.

c. A requirement existed for consideration of data compression schemes. Two proposed schemes are being studied for implementation at a later date. This requirement translated into an expansion capability as well as some flexibility for incorporating compression into the dedicated controller/scanner system in the future.

d. Additional operator interface features were needed. Involved here are a capability for threshold monitoring, manual threshold loading, and choice of normal page or infinite CCD lines (for scanner adjustment).

These criteria provided a suitable point of departure for comparing and judging the microprocessors analyzed below.

C. DESCRIPTION OF MICROPROCESSORS

The following microprocessor series were candidates for use in

the controller: the Fairchild F-8 series; the MOSTEK 3870 series; the Intel 8085 series and 8048 series; and Zilog Z80 series. The Fairchild and MOSTEK series were candidates because of their instruction compatability with the F-8. The Intel 8048 series was considered since it has an architecture similar to the F-8 series. The Intel 8085 and Zilog series were attractive because of their versatility and the wide availability of support chips. The subsequent discussion focuses on the distinguishing features of each, with emphasis on those items which are relevant to the controller application.

1. The Fairchild F-8 Series. An appropriate microprocessor series to start with is the Fairchild F-8 series. Previously, the F-8 Mark III Formulator microcomputer used in the laboratory has been referred to simply as "the F-8". Theoretically, it is possible to pull apart the F-8 Formulator and reconfigure the components to yield a compact, dedicated F-8 controller. In practice, it would be necessary to replicate only those features necessary for scanner control.

The heart of the F-8 series is the 3850 Central Processing Unit (CPU). The 3850 includes an arithmetic and logic unit (ALU), control unit and instruction register, bus interface logic, and accumulator registers. The F-8 logic is not functionally distributed among CPU and support chips, but rather, various functions are integrated within each chip to minimize support chip count. Any memory addressing logic must be performed by the memory or a memory interface chip rather than in the CPU. This eliminates the need for address lines on the 3850 CPU and instead allows for two 8-bit I/O ports. The arrangement also permits a 64-byte read/write memory (RAM) rather than requiring that addressing logic be contained on the chip. However,

this scheme also prevents connection of the 3850 CPU directly to a standard memory device; hence, a 3853 Static Memory Interface (SMI) device is needed between the 3850 and a standard read-only memory (ROM) or EPROM, whereas a 3852 Dynamic Memory Interface (DMI) is needed between the 3850 and any off-chip standard read/write memory (RAM).

Instead of a standard ROM or EPROM, the 3850 CPU is normally used with the 3851 Program Storage Unit (PSU). The 3851 PSU provides a 1Kx8-bit read-only memory, two 8-bit I/O ports, a timer, and interrupt logic. It has its own memory addressing and processing logic which can interrupt five control lines called ROMC states which are generated by the 3850. The 3851 PSUs are factory mask programmable only; if several are used, or if one is used with other F-8 peripheral devices, each must have a specific memory addressing mask to avoid possible memory contention problems.

Of the remaining support devices, another that is relevant to a controller application is the 3861 Parallel I/O device (PIO). The 3861 has the two 8-bit I/O ports, programmable timer, and interrupt logic of the 3851 PSU. However, unlike the 3851, the 3861 has no masked memory.

Some additional features of the 3850 are outlined in Table 3.1. Section D compares the F-8 series against other devices in a controller application.

2. The MOSTEK 3870 Series. The MOSTEK 3870 series is derived from the Fairchild F-8 series. Essentially, the MK3870 microprocessor is an enhanced version of the Fairchild 3850 CPU and 3851 PSU, combined on a single chip. It uses the F-8 instruction set.

Table 3.1 Microprocessor Comparison Chart

	Fairchild F-8 (3850)	MOSTEK 3870	Intel 8048	Intel 8085	Zilog Z80
Technology	N Channel Isoplanar MOS	N Channel Ion	N Channel Sil Gate MOS	N Channnel Sil Gate MOS	N Channel Sil Gate Depl Load
Clock	1000-2000 nsec.	500-1000 nsec.	500 nsec.	320 nsec.	166-500 nsec.
Instruction Execution	2-13 usec.	1-6.5 usec.	2.5 usec. cycle	1.3 usec. cycle	1 usec. or less
RAM	64 bytes	64 bytes	64 bytes	N/A	N/A
Parallel I/O	Two 8-bit Ports	Four 8-bit Ports	Three 8-bit Ports	16 Bits Addr.& Data Bus	24 Bits Addr.& Data Bus
Type I/O	Non-buffer. Bidirect.	True Bi-direction.	True Bi-direction.	Tri-State	Tri-State
Expandable	Yes	Limited	Limited	Yes	Yes
Assembly Language	F-8	F-8	Intel 8048	Intel 8080A 8080A	Z80 & Intel
EPROM Version	No	Yes 38P70	Yes 8749	No	No
Power	+5 V	+5 V	+5 V	+5 V	+5 V
Cost	$10.00	$44.00	$6.00	$5.75	$3.75

Memory-addressing logic is included on the chip. Pertinent features of the 3870 are shown in Table 3.1. A serial port version of the MK3870 is available, the MK3873. EPROM versions of both the MK3870 and MK3873 are also available; they are the MK38P70 an MK38P73, respectively, and can accommodate up to 4Kx8-bit standard EPROMs. The MK3870 and MK38P70 have four truly bidirectional 8-bit parallel I/O ports; the MK3873 and MK38P73 have three 8-bit parallel I/O ports, one 5-bit parallel I/O port, and a serial port. A 64-byte scratchpad RAM is included on each. The 3870 series does not include support devices; however it is possible to use some support devices from other microprocessors.

3. The Intel 8048 Series. The Intel 8048 series is Intel's approach to providing an F-8 series-like, expandable, low end, low cost, limited application microprocessor series. The series has its own specific support chips and a different assembly language from the other microprocessors discussed. The 8048 series is intended for use in low chip count applications; a 2Kx8-bit version, the 8749, is available. The 8048 has a 64-byte on chip RAM and three parallel 8-bit I/O ports, one of which (called the bus port) is truly bidirectional. A support device worth mentioning is the 8243 Input/Output Expander, which can expand the low-order 4 bits (least significant) of the bus port into four individually addressable 4-bit I/O ports. The 8048 can operate in several modes: Internal Execution Mode - the microprocessor cannot access external memory - this is the normal mode for operating in a self contained configuration; Debug Mode - allows single stepping through programs; and Programming and Verify Modes - used for programming EPROMs in EPROM versions of the chip and for verifying memory content. Some additional characteristics of the series are

shown in Table 3.1.

4. The Intel 8085 Series. The Intel 8085 series represents Intel's enhancement of the Intel 8080A series; the 8080A is probably the most widely known 8-bit microprocessor. More support devices are available for the Intel 8080A/8085 series than for any other microprocessor series. The 8085 incorporates clock logic and bus interface logic onto the chip and has a single +5 volt d.c. power supply. All input, output, read, and write functions are performed using data bus/address bus lines and control signals connected to peripheral devices. The 8085 series uses the 8080A instruction set with minor exceptions.

Some useful peripheral chips exist in the 8080A/8085 series for the controller application. The 8255A Programmable Peripheral Interface (PPI) gives a capability for achieving three 8-bit I/O ports, or two 8-bit I/O ports and two 4-bit I/O ports, from an 8-bit data port and some control lines from a microprocessor. The 8755A 2Kx8-bit EPROM with two 8-bit I/O ports combines an EPROM and port expansion capability into a single chip. Also, a device with two 8-bit I/O ports and one 6-bit I/O port and timer along with 256 bytes of static read/write memory (RAM) is available, the 8155.

5. The Zilog Z80 Series. The Zilog Z80 microprocessor represents Zilog's enhancement of the Intel 8080A. In some respects, it is similar to the Intel 8085. It includes all 8080A instructions as a subset of its more powerful instruction set. The Z80 can use the same support devices as the Intel 8080A and 8085 series; like the 8085, the Z80 has bus and clock logic incorporated into one chip.

Versions of the Z80 can operate at speeds much higher than most other microprocesors. Like the 8080A, all I/O and read/write functions are executed using 16 address lines, 8 data-bus lines, and control signals. The Z80 series has a few support chips, including the Z80A-PIO Parallel I/O device, which can be used to interface the Z80 with devices not having the 8080A/8085/Z80 architecture; and the Z80A-DMA direct memory access controller, which can be used to convert serial data to parallel data and vice versa. Other characteristics of the Z80 are shown in Table 3.1.

D. COMPARATIVE ARCHITECTURES

Theoretically, it is feasible to physically implement the dedicated controller using any of the five microprocessors listed in the previous section. This section proposes one possible controller architecture for each microprocessor type. Although other potential configurations can be found, those described here reflect an attempt to meet the general system requirements for memory and port interface. Configurations which use the F-8 series, MK3870 series, Intel 8048 series, Intel 8085 series, and Z80 series microprocessors in the scanner application are shown in Figures 3.1 through 3.5, respectively, and will be described below. These figures only show general functional interfaces between the microprocessors and the scanner, but not specific connections. The figures do not show specific port utilizations but rather attempt to show how an acceptable port capacity can be attained (in terms of scanner control requirements) with available support chips. A brief discussion and some comparative advantages/disadvantages of each scheme follows.

1. The F-8 Series Based Configuration (Fig. 3.1). This

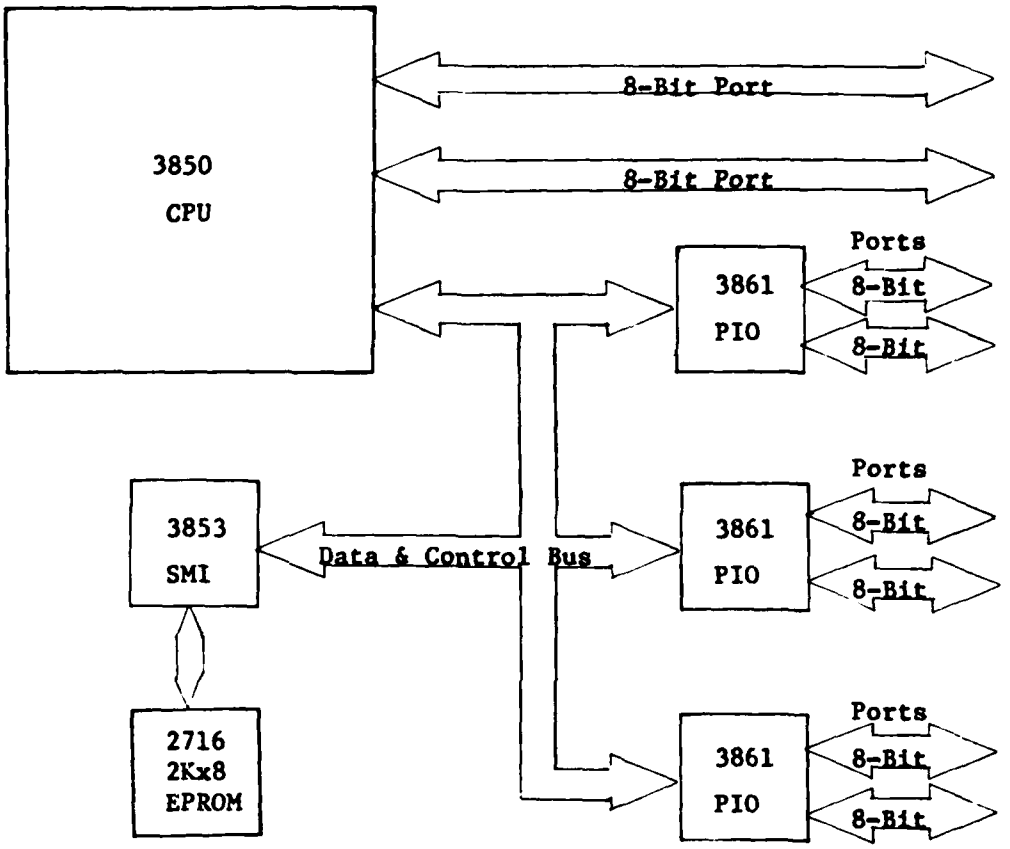


Fig. 3.1 Controller Configuration Based on F-8 Series Microprocessor

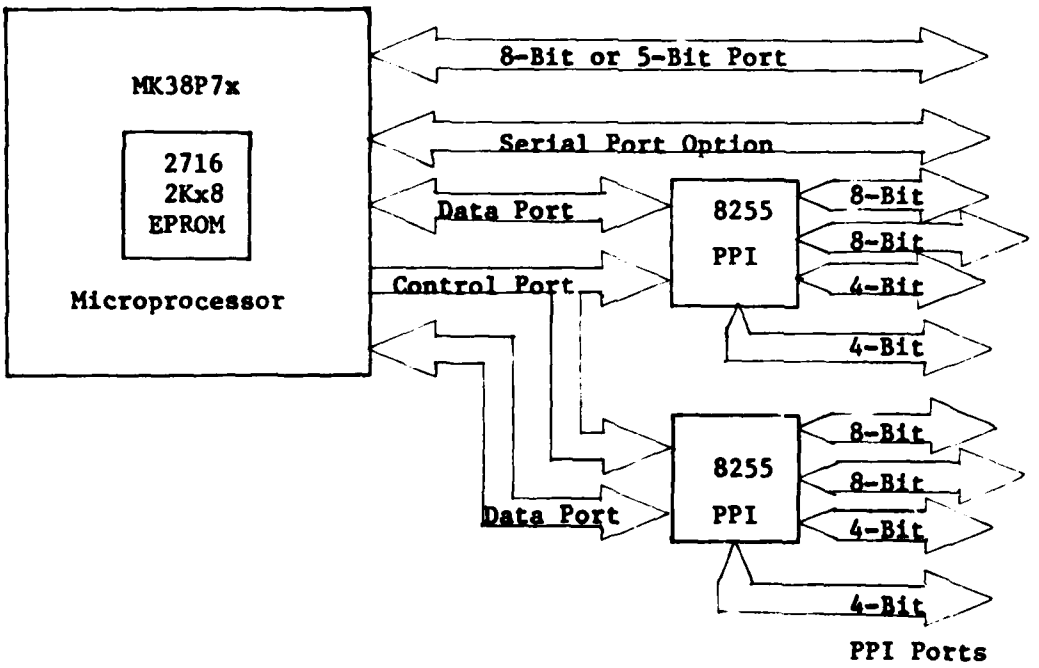


Fig. 3.2 Controller Configuration Using MK3870 Series Microprocessor

scheme uses the 3850 CPU to achieve two 8-bit I/O ports and three 3861 PIOs to obtain six additional 8-bit I/O ports. Memory consists of a standard 2716 2Kx8-bit EPROM and a 64-byte RAM on the 3850. A 3853 SMI is needed to interface the EPROM to the CPU. Additional port capacity can be achieved by adding more 3861s or other peripheral devices. The primary advantages offered by this scheme over the other microprocessor configurations are:

a. The EOPS2 control program can be transferred essentially intact into the EPROM for implementation. Only minor program changes are required in going from the F-8 Formulator hardware to the dedicated controller.

b. The 3850 architecture can support additional functions readily. Functional expansion capability is invaluable for any significant changes or additions to the scanner system.

Some disavantages of this scheme, compared to the four others, include:

a. It is the only configuration requiring an additional chip (3853 SMI) for interfacing the EPROM to the CPU.

b. The 3850 CPU is slower than the other microprocessors, which limits its use in expanded applications.

2. The MOSTEK 3870 Series Configuration (Fig. 3.2). An MK38P70 is used together with two Intel 8255A PPIs to achieve five 8-bit I/O ports and four 4-bit I/O ports; two 8-bit ports of the 38P70 are used for data transfer to the PPIs and one 8-bit port of the 38P70 is used to control I/O transfers between the 38P70 and the PPIs. Memory consists of a standard 2Kx8-bit 2716 EPROM mounted directly on the 38P70 and a 64-byte on chip RAM. This concept has the following

advantages over the other schemes:

a. Again, the EOPS2 program can be used essentially intact. The 38P70 uses F-8 assembly language; however, use of the PPIs requires additional instructions as compared to the F-8 configuration above.

b. Use of the PPIs gives a more efficient matching to the scanner port interface requirements than some of the other schemes because of the 4-bit port capability of the PPIs.

c. A lower chip count is achieved as compared to the F-8 and Z80 configurations.

d. The EPROM is conveniently mounted on the MK38P70, which reduces circuit connections.

e. A serial port capability can be realized by substituting a MK38P73 for the MK38P70.

A few disadvantages are:

a. Expansion capability, as compared to the F-8, 8085, and Z80 series, is limited.

b. Only 64 bytes of RAM are avilable, with no possibility for expansion.

c. The cost of the MK38P70 is much higher than that of the other microprocessors.

3. The Intel 8048 Series (Fig 3.3). An 8749 (2Kx8-bit EPROM version of the 8048) microprocessor is used with an 8255A PPI and 8243 I/O Expander to achieve four 8-bit I/O ports and four 4-bit I/O ports (one less than required). Memory consists of a 2716 2Kx8-bit EPROM mounted on the 8749 and a 64-byte on-chip RAM. This configuration is very similar to the MK38P70 one disussed above. Some advantages of

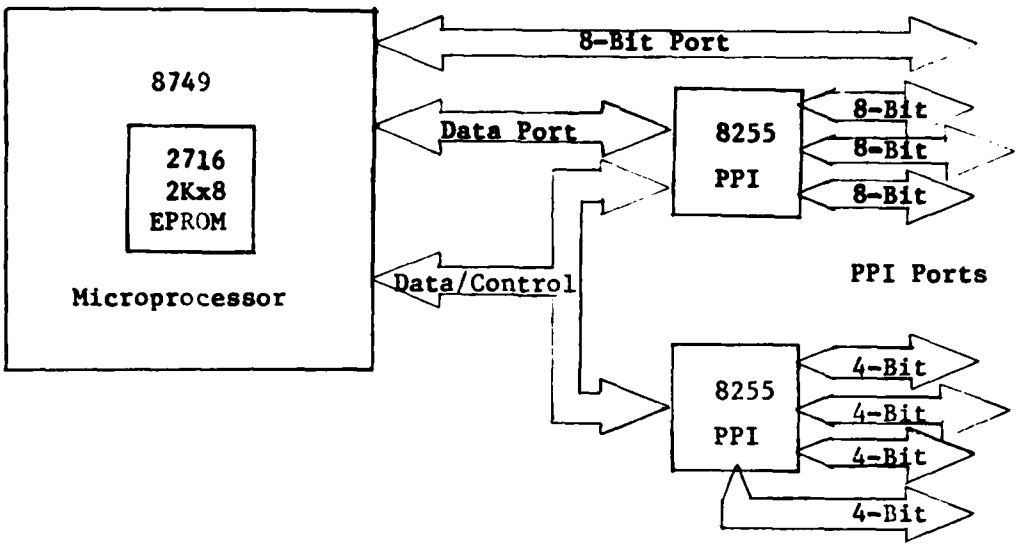


Fig. 3.3 Controller Configuration Using Intel 8048 Series Microprocessor

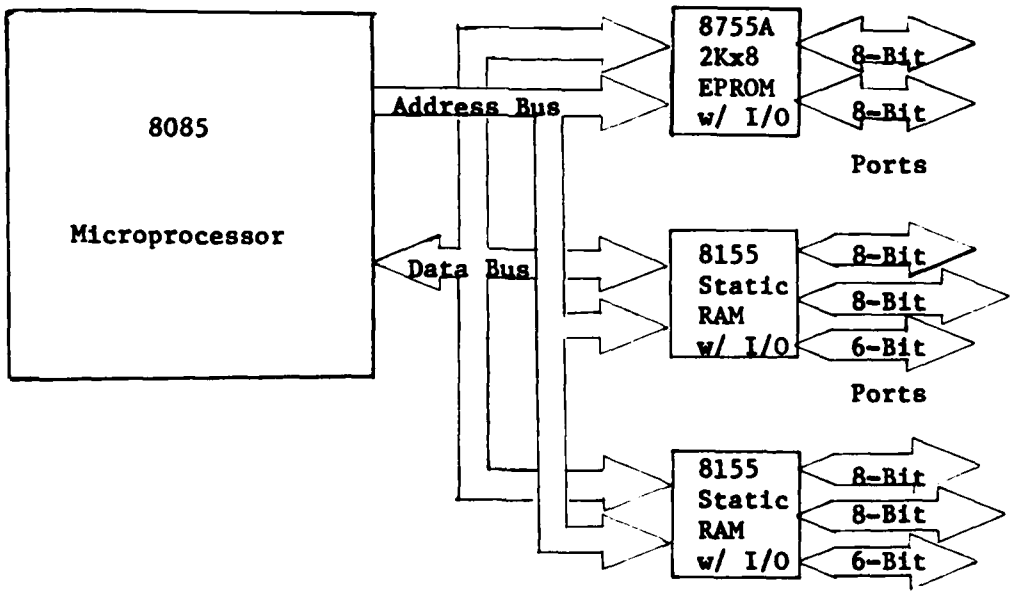


Fig. 3.4 Controller Configuration Using Intel 8085 Series Microprocessor

this scheme include:

a. The multiple operating modes of the 8749 give greater flexibility in programming and testing the controller as compared to any of the other schemes.

b. Complex addressing is not required, and on-chip RAM is available, so chip count is low, as with the MK38P70 and F-8 schemes. This is the main advantage over the 8085 and Z80 series.

Some disadvantages include:

a. The non-standard instruction set requires special consideration. Software development would require acquisition of programming tools not presently available in the laboratory.

b. As shown, the port interface requirement is not met. Three 8255As are needed to meet the port requirements in lieu of the 8243 and 8255A shown. Otherwise, a hardware modification to the scanner is needed in order to use the 8243.

4. The Intel 8085 Configuration (Fig 3.4). This configuration uses the 8085 CPU with some peripherals capable of providing both memory and I/O capability. The 8755A 2Kx8-bit EPROM with I/O and two 8155 Static RAM with I/O give six 8-bit I/O ports and two 6-bit I/O ports and provide for all memory requirements. Separate data and address buses are required. Advantages of using this architecture over the other four are:

a. The 8755A is a self contained device. This results in lower chip count since a separate EPROM is not needed. Also, use of a separate EPROM programmng circuit is not required.

b. All devices have tri-state I/O lines which eliminates the need to buffer input and output connections to ports.

This suggests that inputs and outputs might be combined on the same bit, thus further reducing the chip count shown to yield the lowest chip count of any configuration.

c. The configuration is readily expandable.

The disadvantages of using this chip as opposed to the others include:

a. A non-F-8 assembly language is used, which requires attention to timing considerations when writing the control program.

b. Separate data and address lines are used, requiring more connections and a different programming approach as compared to the F-8-like architectures.

c. There is no significant RAM residing on the CPU.

5. The Zilog Z80 Configuration (Fig 3.6). The Z80 also requires separate address and data lines. Three 8255A PPIs are needed to achieve six 8-bit I/O ports and six 4-bit I/O ports. A standard 2716 2Kx8 bit EPROM provides program memory; however, a separate chip is needed for RAM. Advantages of using this Z80 configuration as opposed to the others are:

a. The Z80 has the most powerful and versatile instruction set. More programming flexibility is available compared to the other microprocessors, which would be significant if additional functions are ever incorporated into the controller.

b. Instruction execution using the Z80 is faster than that of the other microprocessors.

c. The Z80 configuration is readily expandable.

Among the disadvantages, compared to the other schemes, are:

a. A separate RAM chip is needed.

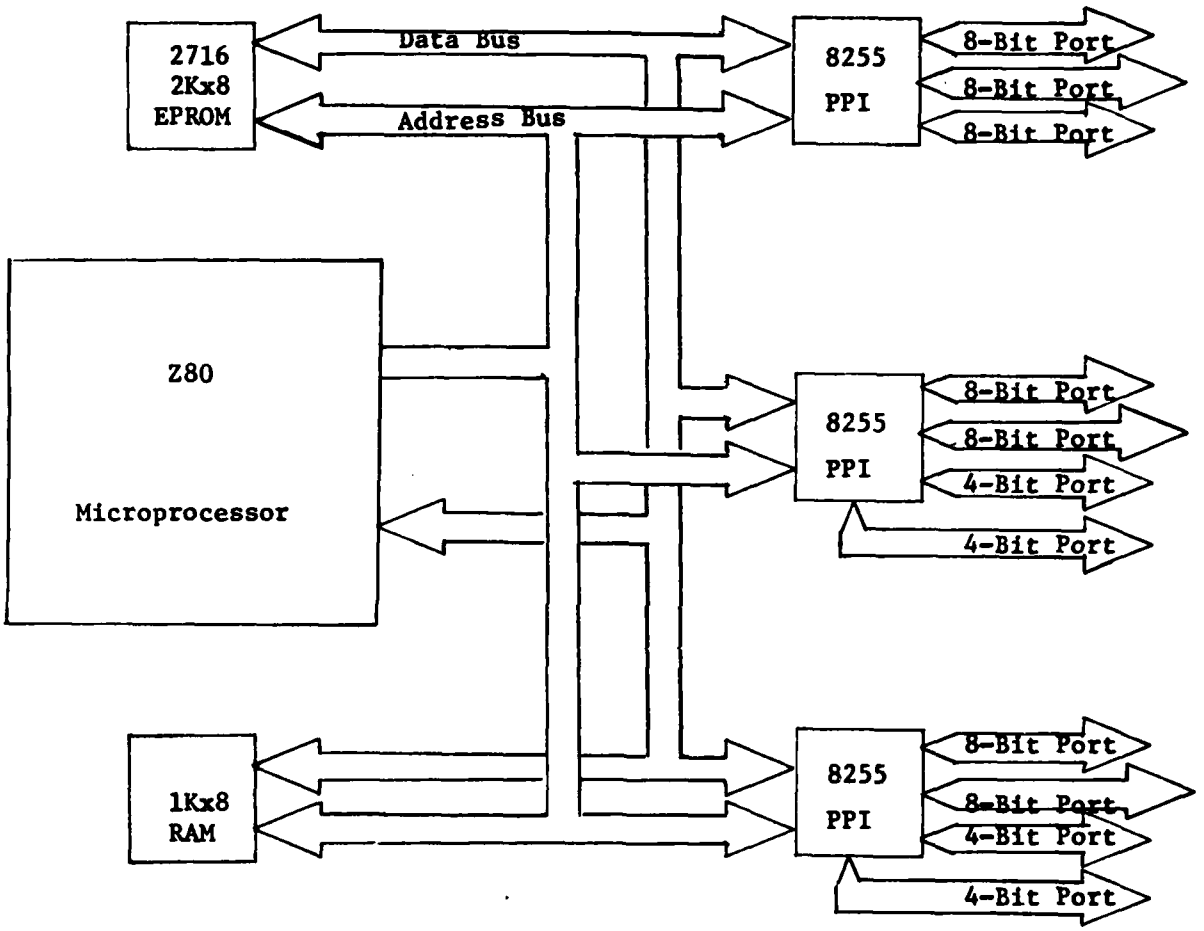


Fig. 3.5 Controller Configuration Using Zilog Z80 Series Microprocessor

b. A higher chip count is required than some of the other configurations.

c. Separate address and data lines are used, as in the 8085 scheme.

E. FINAL SELECTION

The preceding sections outlined some of the features and capabilities of five microprocessor types and suggested possible controller architectures using each type. The architectures provided a basis for comparing the types against one another for use in the controller application. After the advantages and disadvantages of each configuration were weighed against each other and against the requirements for the controller, one configuration, the MK38P70, was chosen as the basis for final design. The MK38P70 was selected over the others for the following reasons:

1. Available laboratory facilities made possible the immediate development, testing, and implementation of the controller. The F-8 assembly language used by the 38P70 suggested that the F-8 Formulator would be a useful means to emulate and test the controller configuration. This would also be true for the F-8 (3850) configuration; however, some additional advantages of the MK38P70 over the F-8, to reiterate, are:

a. A memory interface chip is not needed.

b. The convenience of an on-chip EPROM socket and capability to interface with a readily available support chip (8255A PPI) provide a "better fit" than the 3850 for the controller architecture.

c. The MK38P70 can be made to operate faster than the

3850, and a serial port can be obtained by substituting an MK38P73 for the MK38P70. These options may prove more useful in accommodating future system modifications than would be possible with the 3850 architecture.

2. The configuration offered an optimal port interface in terms of numbers of 8-bit and 4-bit ports while leaving a very limited expansion capability.

3. The control program could be written in the F-8 assembly language.

4. Separate data and address lines were not needed, which simplified connections.

At the outset of this research, it was recognized that using any microprocessor with an EPROM memory required a language compatible programming capability. A programming circuit was not available for F-8 assembly language as required by the MK38P70. Fortunately, Lin (5) devised an EPROM programmer that works directly from the F-8 Formulator. In addition, he wrote an 8080A/8085/Z80 assembler program that allowed 8080A/8085/Z80 assembly program instructions to be written using the F-8 Formulator and converted into correct source code. These developments permitted program writing and EPROM programming for all series of devices analyzed above, with the exception of the Intel 8048 series.

In summary, the MOSTEK 38P70 microprocessor was judged to be the most attractive for meeting the system criteria and was the one selected for the design. The next chapter describes the detailed design of the MK38P70-based controller.

CHAPTER 4

CONTROLLER DESIGN

A. GENERAL

This chapter describes the details of the circuitry and software used in the implementation of the dedicated microprocessor controller. A general description of the controller and its interfaces to the rest of the scanner system is given first as an overview, followed by a detailed discussion of the port interface used. The threshold monitor and adjust circuit is discussed separately, since that circuit is modular, that is, it can be added or removed without affecting basic scanner functions. A brief discussion of some required scanner modifications is followed by an inquiry into data compression requirements as a basis for future research. A detailed listing of the microprocessor software (MEOSC - Microprocessor Electro-Optical Scanner Control Program) is given in Appendix B, and Manufacturer's Data for hardware is contained in Appendix C.

B. CONTROLLER DESCRIPTION

Figure 4.1 shows the MK38P70 based scanner system. In a comparison of this system with the F-8 Formulator based system (Fig. 1.1), several differences are obvious. The peripherals associated with the F-8 (video console and floppy disk) are not used. However, a threshold monitor and adjust circuit board has been inserted in the MK38P70 version as a separate package from the controller circuit board. A new port numbering scheme is used with the MK38P70 system because of the nature of the port interface. From the Figures 1.1 and

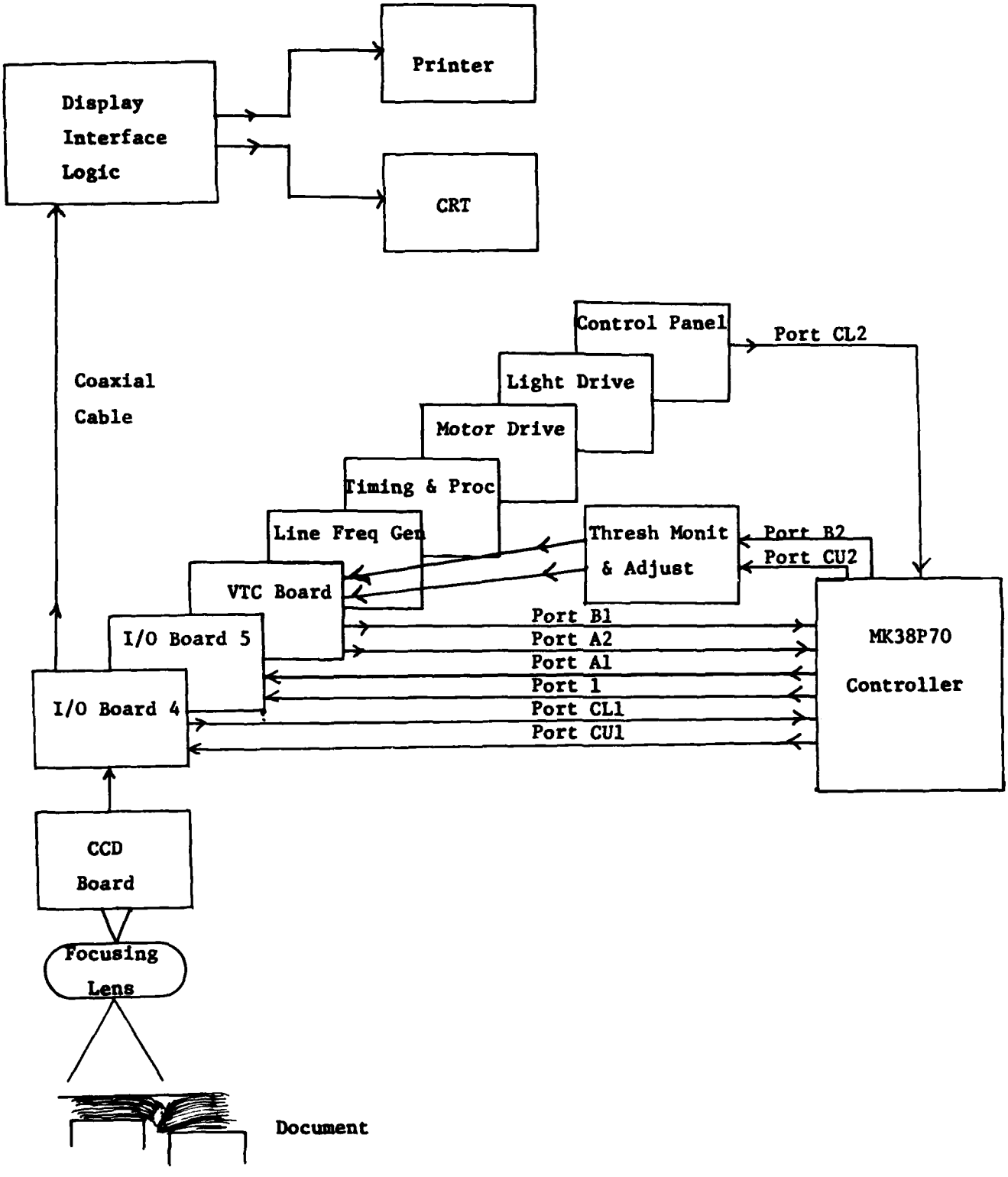


Fig. 4.1 Bound Document Scanner with MK38P70 Controller

4.1 it is apparent that the essential structure of the scanner system has been preserved in implementing microprocessor control. Nevertheless, a subtle difference, not shown explicitly, exists. In the F-8 system, operator controls and threshold monitoring are distributed among the video console, Formulator front panel, and scanner control panel. In the MK38P70 based system all operator functions are consolidated onto the scanner control panel.

A block diagram of the MK38P70 controller board is shown in Figure 4.2. The scanner control program resides on the 2716 2Kx8-bit EPROM (IC #4), which is mounted directly on the MK38P70 (IC #1). A 2.0 MHz crystal provides a 1.0 MHz internal clock for the CPU after a divide-by-two operation. The MK38P70 has four 8-bit I/O ports which have been numbered by the manufacturer as Ports 0, 1, 4, and 5. Port 4 is used to control the I/O data transfers between the MK38P70 and the 8255A Programmable Peripheral Interface (PPI) devices (ICs #2 and #3). Ports 0 and 5 of the MK38P70 are used to transfer data both to and from the 8255As. Basically, Port 4 selects a PPI and a port on the PPI and tells the PPI whether an input or output operation is to take place. During input, data are read in from the selected PPI port pins, through the PPI, through the MK38P70 Port 0 or 5 pins, and into the microprocessor. During output, data are written from the MK38P70, through the data port (0 or 5) and PPI, to the selected PPI port. The 8255A PPIs have been configured such that each provides two 8-bit ports, Ports A and B, and two 4-bit ports, Port C Lower (CL) and C Upper (CU). The PPI is programmed for Mode 0, which means that each PPI port can only be used as an input or an output port, not both.

It is possible to rearrange MK38P70 and PPI ports to derive a

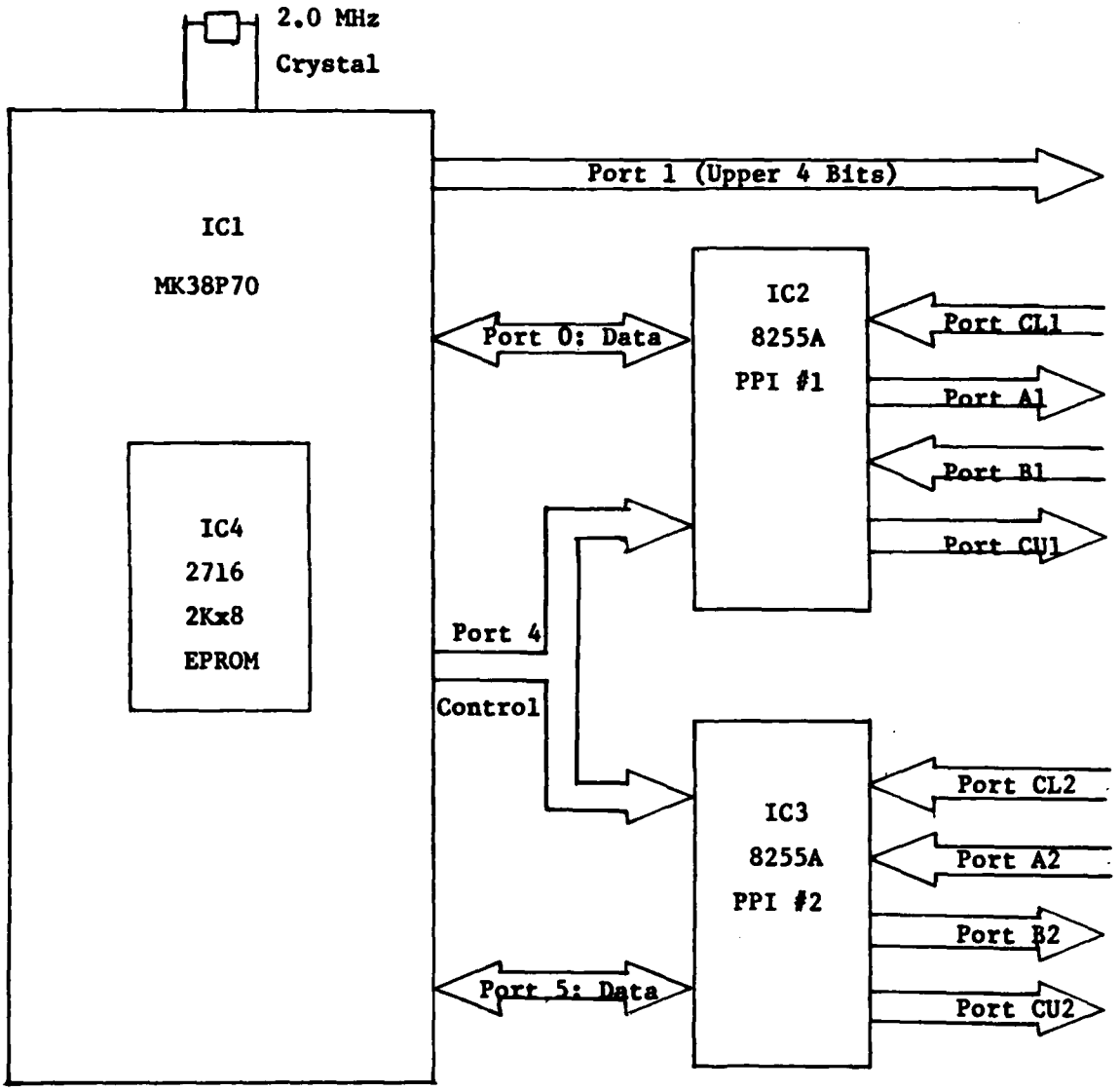


Fig. 4.2 MK38P70 Controller Block Diagram

different interface arrangement. Although this implies that the connections are arbitrary, in reality, several factors were involved in arriving at the arrangement depicted in Figure 4.2:

1. Use of 4-bit PPI ports was sufficient to replace Ports 4, 5, and 13 of the F-8 controller, as well as the internal F-8 port (Port 0 - F-8 panel sense switches).

2. Interchangeablity was sought between the F-8 and the MK38P70 controllers. This meant only that similar ports were substituted, i.e., 8-bit ports for 8-bit ports and 4-bit ports for smaller ports. The port connections were arranged so that the two 44-pin connectors that interfaced the scanner to the F-8 could be used to interface the scanner to the microprocessor controller. Some rearrangement of port bits was required; this factor had no significant effect on the port arrangement but required some minor software modifications.

3. During testing, it was found that using a PPI port in lieu of F-8 Port 9 did not meet the timing requirements. The reason is that I/O operations using the PPI ports require additional program instructions. Therefore, the MK38P70 Port 1 (upper four bits) had to be used to replace F-8 Port 9.

4. Future modifications or additions to the controller may require a serial port capability. If so, a serial port capability could be achieved by substituting an MK38P73 for the MK38P70. The only difference between the two devices is that the serial port of the MK38P73 uses three pins which are in the three least sigificant bit positions of the MK38P70 Port 1. Therefore, the lower four bits of the MK38P70 are not used but are reserved in order to enhance substitution

of the microprocessors. Appendix C shows the pin assignments for both microprocessors.

Photographs of the MK38P70 based scanner system and the MK38P70 controller circuit board are shown in Figures 4.3 and 4.4, respectively. These pictures indicate the physical arrangement of the components discussed above. The F-8 and the video console, which are not required in the MK38P70 configuration, are visible at the right-hand side of Figure 4.3. The MK38P70 controller was placed on two circuit boards in order to facilitate interchangeability with the F-8 by means of the 44-pin connectors. The controller circuit and threshold monitor and adjust circuit are both mounted in the circuit board rack behind the scanner control panel.

C. CONTROLLER SOFTWARE CONSIDERATIONS AND THE 8255A PPI

Crucial to a workable interface between the MK38P70 and the scanner was the need to devise a scheme to control the flow of I/O operations through the two 8255A PPIs. This section includes a functional description of the 8255A and the scheme that was used to translate 8255A commands into the additional program instructions needed to transform the F-8 EOPS2 control program into the MK38P70 control program (MEOSC).

The 8255A PPI is a general purpose I/O device that provides 24 I/O pins. The I/O pins may be configured to operate in several modes; mode 0 was chosen since this is the only mode in which Port C can be used as two distinct 4-bit ports. Mode 0, then, provides for two 8-bit ports (A and B) and two 4-bit ports (CL and CU). Figure 4.5 shows the decode logic of the PPI and Figure 4.6 shows the signals and pin assignments. The decode logic diagram shows that the device select

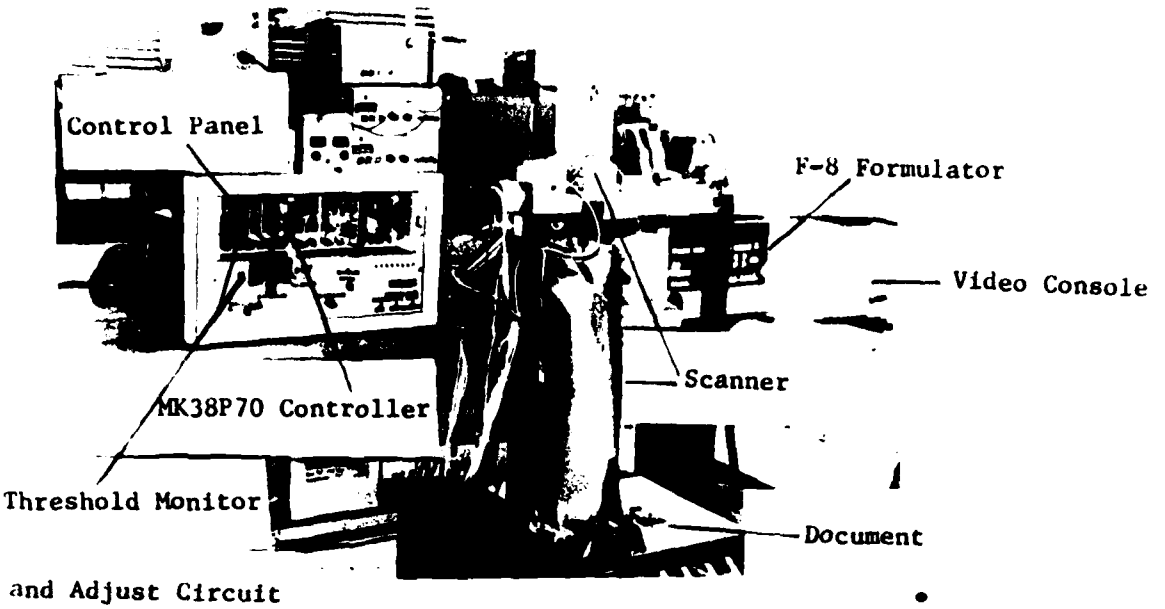


Fig. 4.3 Physical Arrangement of MK38P70/Scanner System

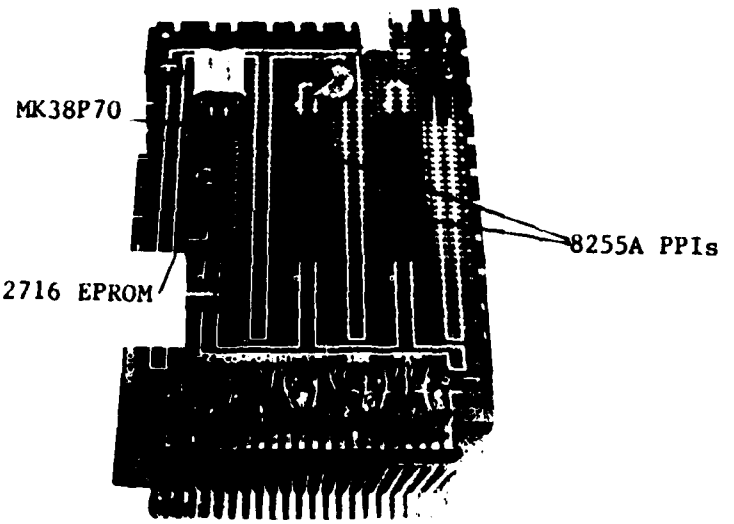
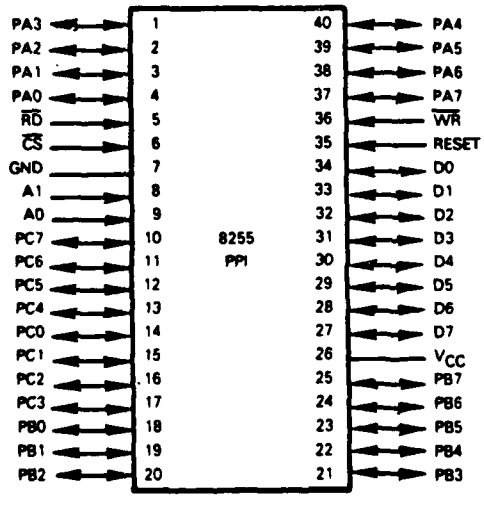


Fig. 4.4 Physical Layout of MK38P70 Controller Circuit

$\overline{CS}$	A1	A0	Selected
0	0	0	I/O Port A
0	0	1	I/O Port B
0	1	0	I/O Port C
0	1	1	A Control, write-only buffer
1	X	X	8255 not selected

Fig. 4.5 8255A PPI Decode Logic



PIN NAME	DESCRIPTION	TYPE
D0 - D7	Bidirectional Data Bus	Bidirectional
PA0 - PA7	Eight I/O pins, designated as Port A	Bidirectional
PB0 - PB7	Eight I/O pins, designated as Port B	Bidirectional
PC0 - PC7	Eight I/O pins, designated as Port C upper and Port C lower	Bidirectional
$\overline{RD}$	Read from device control	Input
$\overline{WR}$	Write to device control	Input
RESET	System reset	Input
$\overline{CS}$	Device select	Input
A0,A1	I/O port select	Input
V_{CC},GND	Power and Ground	

Fig. 4.6 8255A PPI Signals and Pin Assignments

line of the PPI, $\overline{CS}$, must be a logic 0 (LO) in order for the device to operate; the logic states of pins A1 and A0 determine which port is to be selected (A, B, CL, or CU); or, in the case where A1 and A0 are both logic 1 (HI), that a program control word is to be passed to the PPI. Figure 4.6 shows pins D0 through D7, the bidirectional data bus; these lines are connected to Port 0 (8255A #1) and Port 5 (8255A #2) of the MK38P70. The PPI port pins (PA0 - PA7, PB0 - PB7, PC0 - PC7) are connected to the scanner hardware by means of the two 44-pin connectors (refer to Figure 4.2). The remaining pins (except Vcc and GND) are tied to control signals. Putting RESET HI resets the 8255A; pulling $\overline{RD}$ LO inputs data from the selected PPI port to the data bus; pulling $\overline{WR}$ LO outputs data from the data bus to the selected port. Before any I/O operations can occur, the mode and port scheme (for example, Port A = Output, Port B = Input, Port CL = Input, Port CU = Output) must be programmed into the PPI. A PPI port will remain either as an input or an output port (not both) until the PPI is RESET and reprogrammed.

The $\overline{CS}$, A0, A1, $\overline{RD}$, $\overline{WR}$, and RESET lines of both PPIs are connected to Port 4 (control port) of the MK38P70. The bit assignments are:

MK38P70 Port 4 Bit #:	7	6	5	4	3	2	1	0
PPI Control Signal:	N/A	RESET	$\overline{CS}$#2	$\overline{CS}$#1	$\overline{RD}$	$\overline{WR}$	A1	A0

In order to RESET the PPIs, the MK38P70 outputs H'00' over its Port 4; since the MK38P70 uses inverted logic (1 = LO, 0 = HI), this pulls all pins HI. Next, it is necessary to tell each PPI which ports are to be used for input or output. PPI "control" must be written to, <u>not</u> a port. Control addresses are generated over Port 4 as follows:

MK38P70 Port 4 Bit#:	7	6	5	4	3	2	1	0
PPI Control Signal:	N/A	RESET	CS#2	CS#1	RD	WR	A1	A0
8255A #1 Control=H'50':	HI	LO	HI	LO	HI	HI	HI	HI
8255A #2 Control=H'60':	HI	LO	LO	HI	HI	HI	HI	HI

In order to perform an output operation, $\overline{WR}$ must be LO while the data desired is present on the data bus (Port 0 or 5). In the case of initialization, the data consists of an 8-bit word which contains the mode and port designation. The control word used for 8255A #1 is H'7C', and for 8255A #2, H'6E'. (More detail concerning control words can be found in the Manufacturer's Data, Appendix C.) These control words are output on MK38P70 Ports 0 and 5, respectively. The $\overline{WR}$ must be pulled HI again to complete the output operation. After the control word is written, further I/O operations may be performed. In summary, the sequence of commands to initialize the PPIs, in F-8 assembly language, is:

```
F-8 Assemby
Language          Remarks

LI      H'00'     RESET both 8255As
OUTS    4
LI      H'54'     Initialize 8255A #1
OUTS    4         (WR pin LO)
LI      H'7C'     (I/O Program word)
OUTS    0         (Data bus #1)
LI      H'50'
OUTS    4         (WR pin pulled HI)
LI      H'64'     Initialize 8255A #2
OUTS    4         (WR pin LO)
LI      H'6E'     (I/O Program word)
OUTS    5         (Data bus #2)
LI      H'60'
OUTS    4         (WR pin pulled HI)
```

Instructions are given for other I/O operations in a manner similar to that outlined above. The following two examples illustrate

the input and output operations:

1. An input operation using Port B of 8255A #1:

```
LI      H'5A'   Bit#:  7  6   5   4   3  2  1  0
OUTS    4       Signal NA RS CS2 CS1 RD WR A1 A0
INS     0       H'5A'= HI LO  HI  LO  LO HI LO HI
```

Data will be read into the MK38P70 Port 0 as long as 8255A #1 Port B remains selected and the $\overline{RD}$ pin is held LO.

2. An output operation using Port B of 8255A #2:

```
LI      H'66'   Bit#:  7  6   5   4   3  2  1  0
OUTS    4       Signal:NA RS  CS2 CS1 RD WR A1 A0
LI      H'42'   H'66'= HI LO  LO  HI  HI LO LO HI
OUTS    5
LI      H'62'   H'62'= HI LO  LO  HI  HI HI LO HI
OUTS    4
```

The above features illustrate the additional instructions required for I/O operations using the PPI. An output operation requires six instructions, compared to two if the operation were executed directly from an MK38P70 port. Also, only two additional instructions are required for an input operation; however, to maintain the integrity of the input data, the data bus is cleared of previous data before an input operation, which represents another instruction, for a total of three additional instructions. With the exception of output operations made directly from MK38P70 Port 1, all controller circuit I/O operations require these additional instructions. A PPI output operation can take up to 39 microseconds to execute, whereas a Port 1 output operation only needs 9 microseconds. However, a PPI input operation takes up to 23 microseconds, whereas an input directly from an MK38P70 port consumes up to 18 microseconds.

The most significant difference between EOPS2 and the scanner

control program for the MK38P70 controller is the inclusion of these additional PPI instructions. Also, portions of EOPS2 specific to the peripherals of the F-8 Formulator, such as a jump to DOS4 and console display of the threshold level, were omitted. A detailed listing of the MK38P70 scanner control program (MEOSC) is contained in Appendix B.

D. THE MK38P70 CONTROLLER CIRCUIT

The major components of the MK38P70 controller circuit are the MK38P70 microprocessor, the two 8255A PPIs, and the 2716 EPROM. The function of the PPIs has been detailed in Section C above. This section focuses on the role of the microprocessor and EPROM and the physical connections used in the circuit.

The salient features of the MK38P70 were presented in Chapter 3. A functional block diagram of the MK38P70 is shown in Figure 4.7 and the pin and signal assignments are shown in Figure 4.8. Connections XTL1 and XTL2 are used for an external time base. The microprocessor can operate with an external clock in the range of 2 to 4 MHz which results in an internal clock operating at half that speed (1 to 2 MHz). In order to obtain replication of the F-8 Formulator controller instruction execution times, the same external time base of 2.0 MHz was used for the MK38P70 controller. Replication of instruction execution times was desirable in order for the MK38P70 controller operation to parallel as closely as possible the F-8 controller operation, and it also allowed use of the F-8 Formulator as an emulator of the MK38P70 in order to test and debug program instructions using the PPI interface (discussed further in Chapter 5). The port connections are labeled $\overline{\text{P0-0}}$ through $\overline{\text{P0-7}}$ (Port 0), $\overline{\text{P1-0}}$

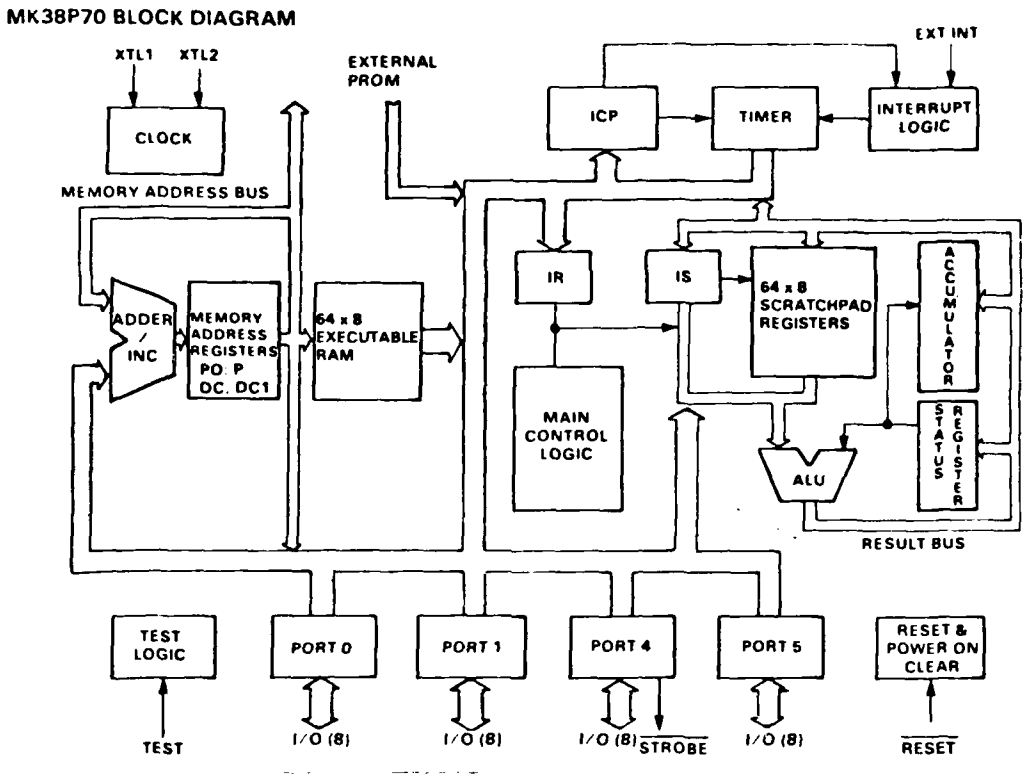


Fig. 4.7 MK38P70 Functional Block Diagram

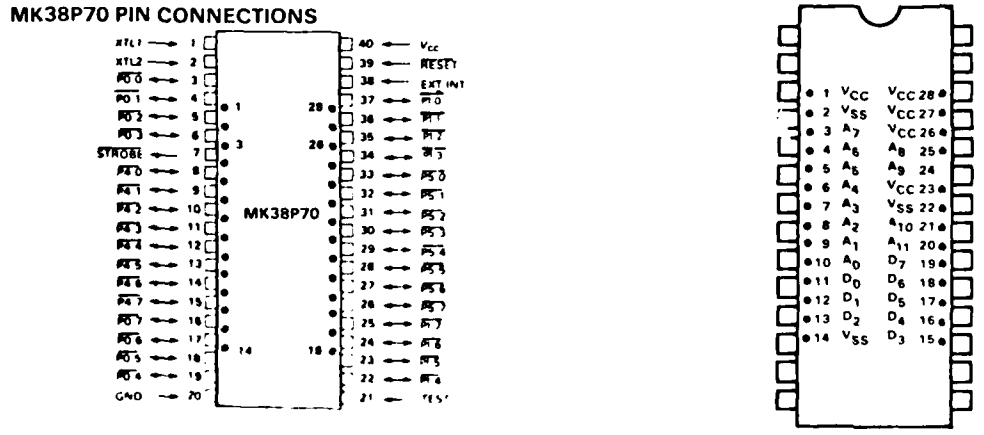


Fig. 4.8 MK38P70 and EPROM Socket Pin Assignments

through $\overline{P1\text{-}7}$ (Port 1), $\overline{P4\text{-}0}$ through $\overline{P4\text{-}7}$ (Port 4), and $\overline{P5\text{-}0}$ through $\overline{P5\text{-}7}$ (Port 5). These ports are normally in a HI state (F-8 logic 0). Port 0 is connected to the data bus of 8255A #1, Port 1 (upper four bits) is conected to I/O Board 5, Port 4 is the control port for the PPIs, and Port 5 is connected to the data bus of 8255A #2. $\overline{STROBE}$ is a ready strobe associated with Port 4 which provides a LO pulse when data are written onto Port 4; it is not used in this application. $\overline{RESET}$ is used as an external reset for the microprocessor; when pulled LO the microprocessor resets; when allowed to return HI program execution begins at location H'000'. The MK38P70 also resets to H'000' following power up by means of an internal power-on-reset circuit. An R-C network recommended by MOSTEK was used for $\overline{RESET}$ (see Figure 4.11). EXT INT (External Interrupt) allows for external (hardware) or internal (software) program interrupt and can be used with the timer for pulse width measurement and event counting. TEST is only used for testing the operation of the MK38P70 and is normally grounded. EXT INT and TEST are not used in the controller application.

The EPROM connections are located on top of the MK38P70 and are shown in Figure 4.8. Comparing these connections to those shown in Figure 4.9, EPROM pin assignment and block diagram, it can be seen that Pin 1 of the 2716 corresponds to Pin 3 of the MK38P70 EPROM socket. The 2716 is an ultra-violet-light-erasable-programmable read-only-memory. A program can be written into the EPROM using an EPROM programming circuit which provides required voltage levels and timing parameters. As previously stated, Lin (5) designed and implemented such a circuit which programs EPROMs using the F-8. A ten minute exposure to ultra-violet light erases the program for reuse of

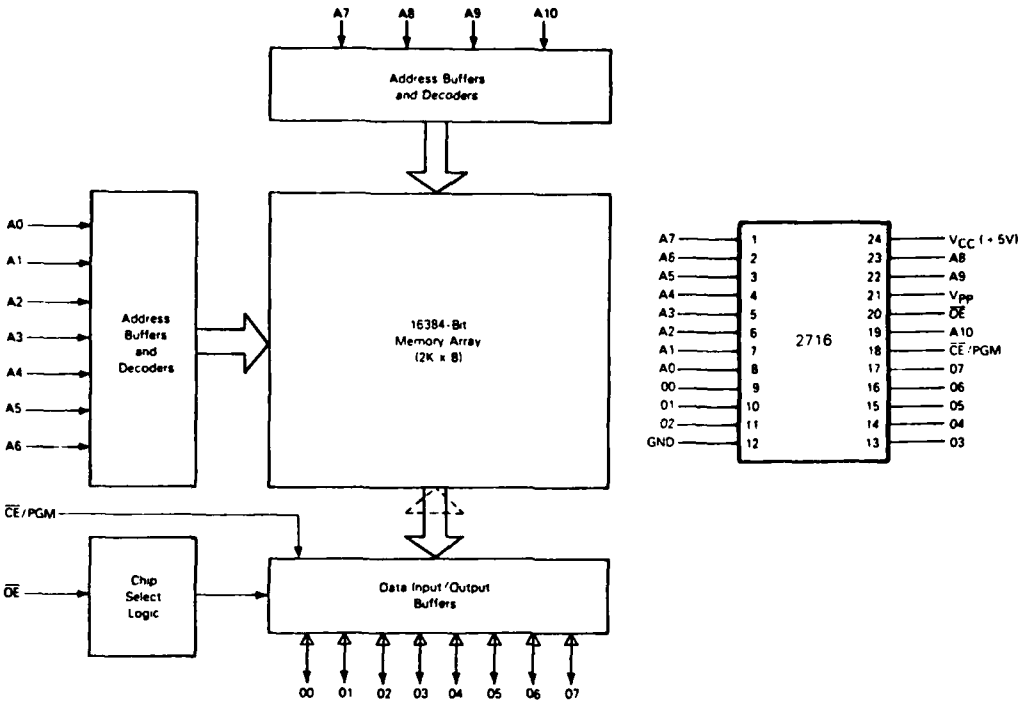
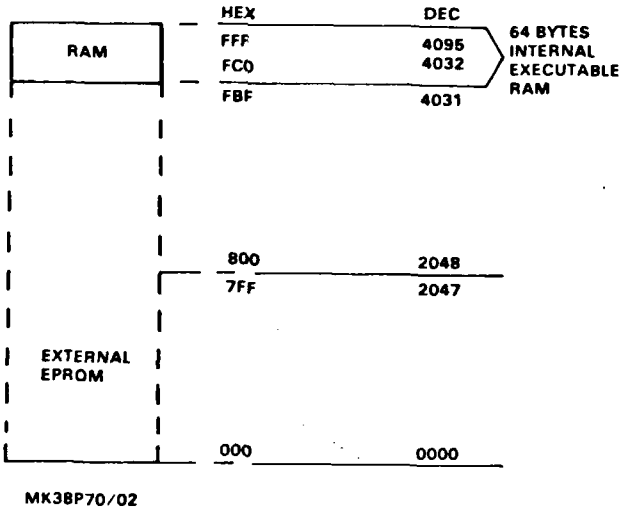


Fig. 4.9 2716 EPROM Block Diagram and Pin Assignment



Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK38P70/02	64 bytes	12 bits	0 bytes	64 bytes

Fig. 4.10 MK38P70 Main Memory Map

the EPROM. Eleven address pins (A0 - A10) and eight data pins (O0-O7) access each of 16384 bits (2Kx8 bits); each bit is programmed with a logic 0 or 1 and will remain in that state until the current program residing on the chip is erased. Pin $\overline{OE}$ (Vss on the MK38P70) is a chip select and is normally LO when the 2716 is in operation. Vcc is the +5 volt d.c. supply, whereas Vpp requires +25 volts d.c. only while the program is being burned into the EPROM. $\overline{CE}$/PGM performs the dual functions of power down control and program pulse input used during programming. Figure 4.10 shows that 2716 EPROM mounted on the MK38P70 will occupy up to the first 2048 bytes of memory (0000 - 2047 or H'000' - H'7FF'), while the RAM on the MK38P70 occupies higher memory locations.

The components are integrated into the MK38P70 controller as indicated in the circuit diagram, Figure 4.11. Two 22-pin card connectors are used for interchangeability with the F-8; these connectors are designated as CN1 and CN2. A 6-pin mylar connector is also used (CN3). CN1 provides all connections to I/O Boards 4 and 5. CN2 provides all connections to the VTC Board, and CN3 provides power (+5 volts d.c.), GND, $\overline{RESET}$ and three sense switch connections. The $\overline{RESET}$ button and sense switches are located on the scanner control panel. R1, D1, and C2 comprise the R-C reset circuit. C3 is a high frequency decoupling capacitor which suppresses noise on the Vcc line; C1 is an additional filter capacitor. IC5 is a 7805 +5 volt d.c. regulator. Notice that the total number of components for the circuit is very small. Circuit board layout is shown in Figure 4.12 (note that one vector board is used only for its 22-pin connector). The controller has been rack mounted and currently uses a +8 volt d.c.

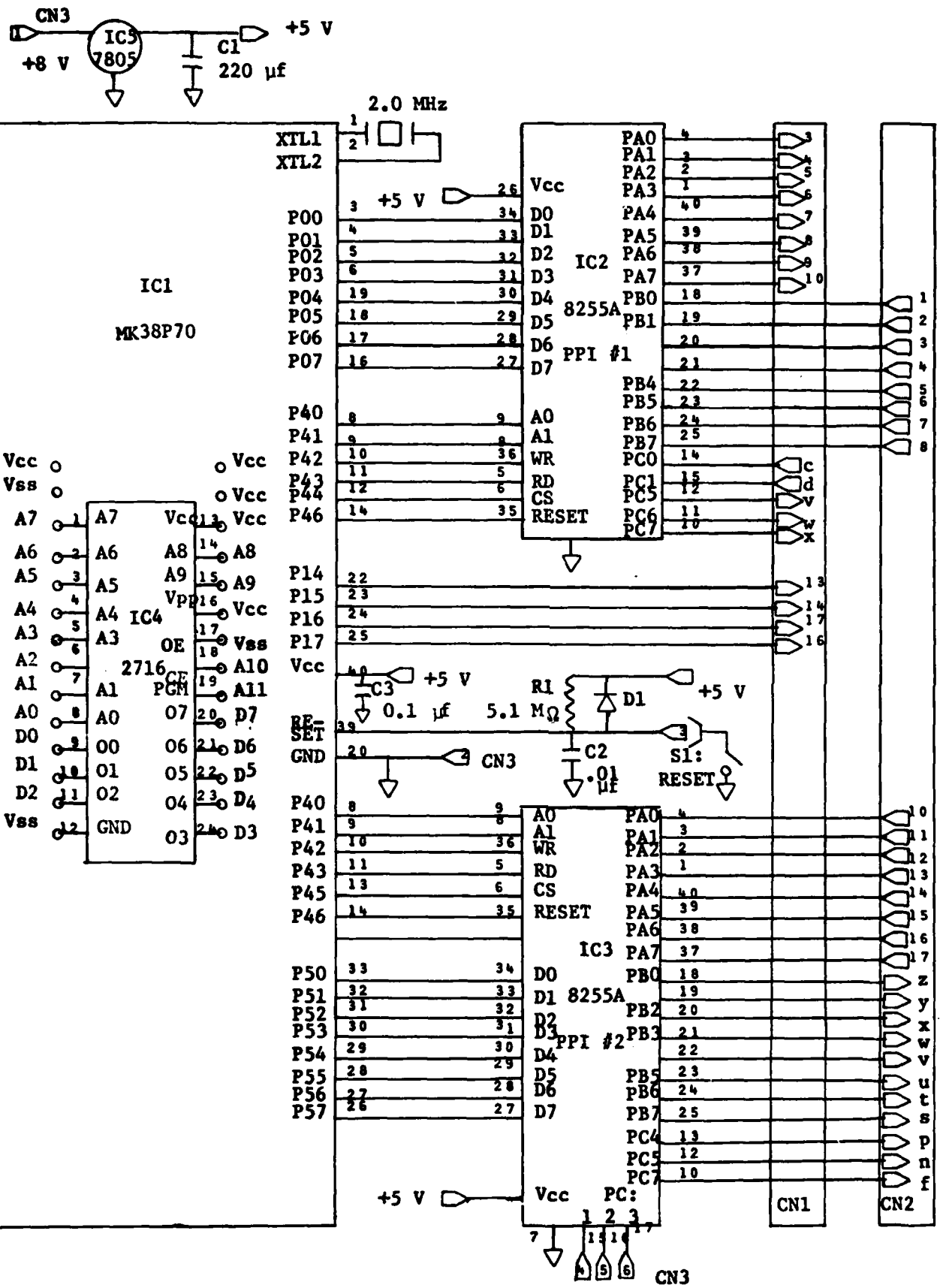
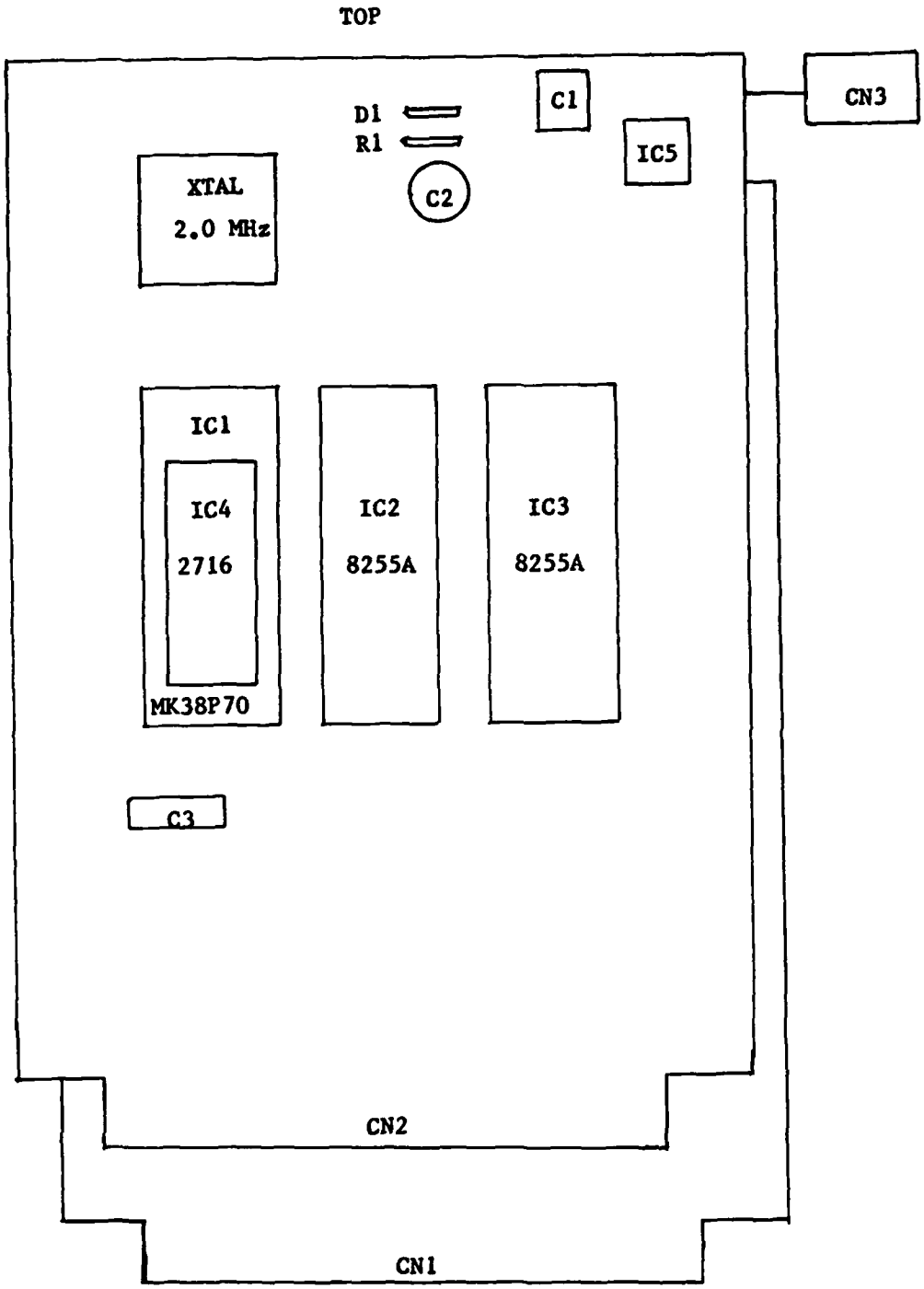


Fig. 4.11 MK38P70 Controller Circuit Diagram



IC5: 7805 +5 V Reg.
C1: 220µf
C2: .01µf
C3: 0.1µf
R1: 5.1MΩ
D1: IN914

Fig. 4.12 MK38P70 Controller Circuit Board Layout

external power supply.

E. THRESHOLD MONITOR AND ADJUST CIRCUIT

The scanner system with F-8 controller had a means of monitoring the HEX value corresponding to the voltage threshold level. This level determined whether a given CCD pixel would be designated black or white. A sequence of program instructions called SHOW in EOPS2 passed the HEX threshold value to the Zenith console for display.

An alternative display method was needed for the MK38P70 controller. Besides merely displaying the threshold level, it was desirable to be able to manually load the threshold level. Previous experiments showed that a manual threshold adjust would in some instances result in a more aesthetically pleasing hard copy of the scanned document. This section describes the circuit that was devised to accomplish both threshold display and threshold adjust.

The circuit is essentially "in line" with Ports B2 and CU2 from the controller (Figure 4.1). During an automatic or frozen thresholding scan, thresholding is under software control, and the ten lines of Ports B2 and CU2 (corresponding to three HEX characters) feed HI or LO levels from the controller through this circuit unaltered. Choosing manual thresholding, however, cuts off the levels from the controller and instead inserts manually selected levels into the ten lines down to the VTC board. Figure 4.13 is the threshold monitor and adjust circuit diagram. S1 is a DPDT switch which selects manual or software thresholding. For software thresholding, AND gates 1, 2, and 3 are enabled and the levels from the controller pass through these gates and through OR gates 6, 7, and 8. During manual thresholding,

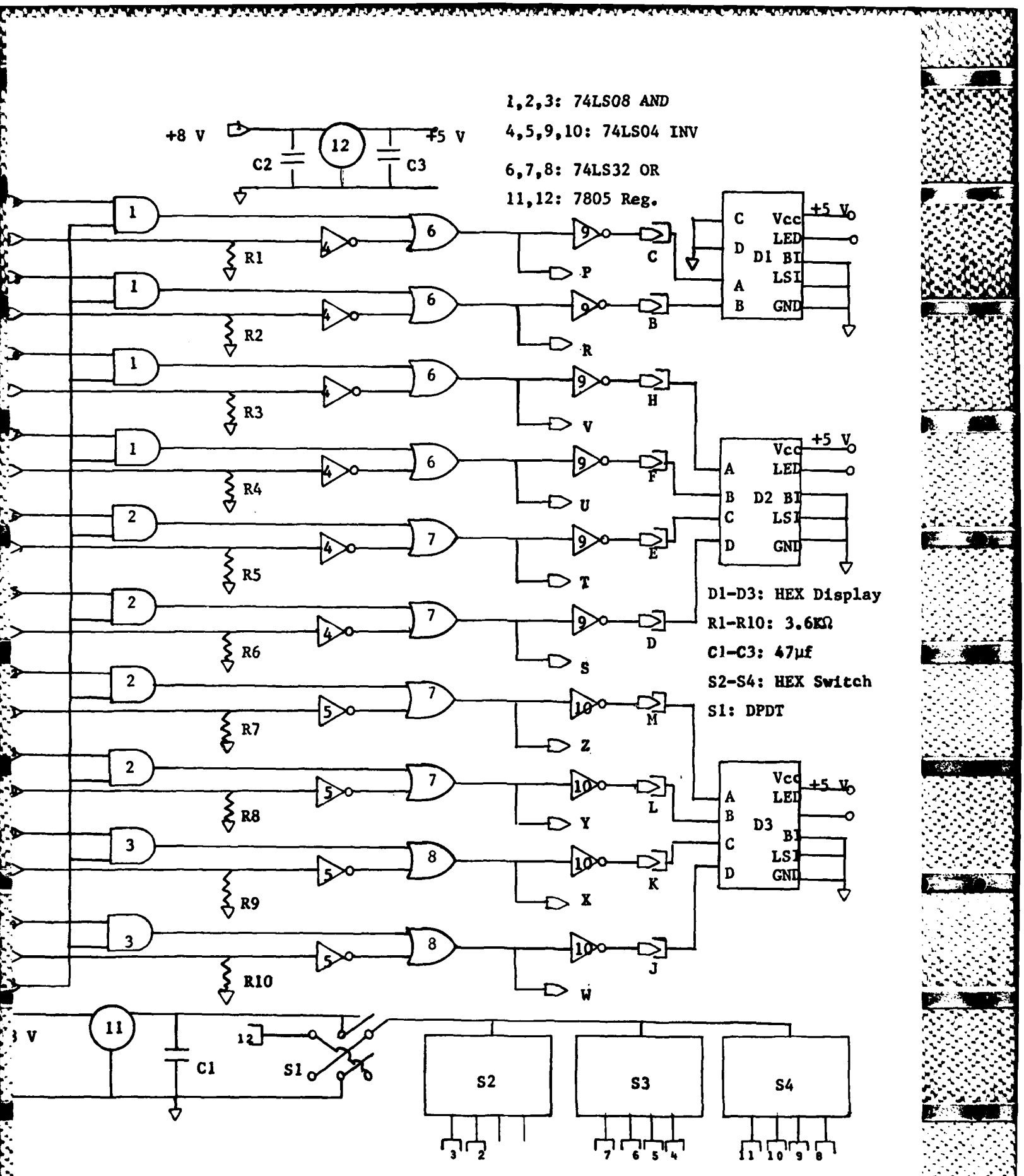


Fig. 4. Threshold Monitor and Adjust Circuit Diagram

the AND gates are disabled and the levels are fed through the OR gates by means of hexadecimal switches S2, S3, and S4. Inverters 4 and 5 are needed to invert the HEX switch logic (0 = LO, 1 = HI) to F-8 (inverted) logic (0 = HI, 1 = LO). In either case, the levels output by the OR gates are displayed by means of the hexadecimal displays D1, D2, and D3. Again inverters (9 and 10) are needed to change inverted logic into the non-inverted logic used by the displays. These displays have been configured so that they will always follow whatever levels are on line by grounding the latch strobe inputs (LSI) and blanking inputs (BI) (see Appendix C). The +5 volt d.c. 7805 regulator (11), filter capacitor C1, switches S1, S2, S3, and S4, and displays D1, D2, and D3, are located on the scanner control panel. All other components are mounted on the circuit board (Figure 4.14).

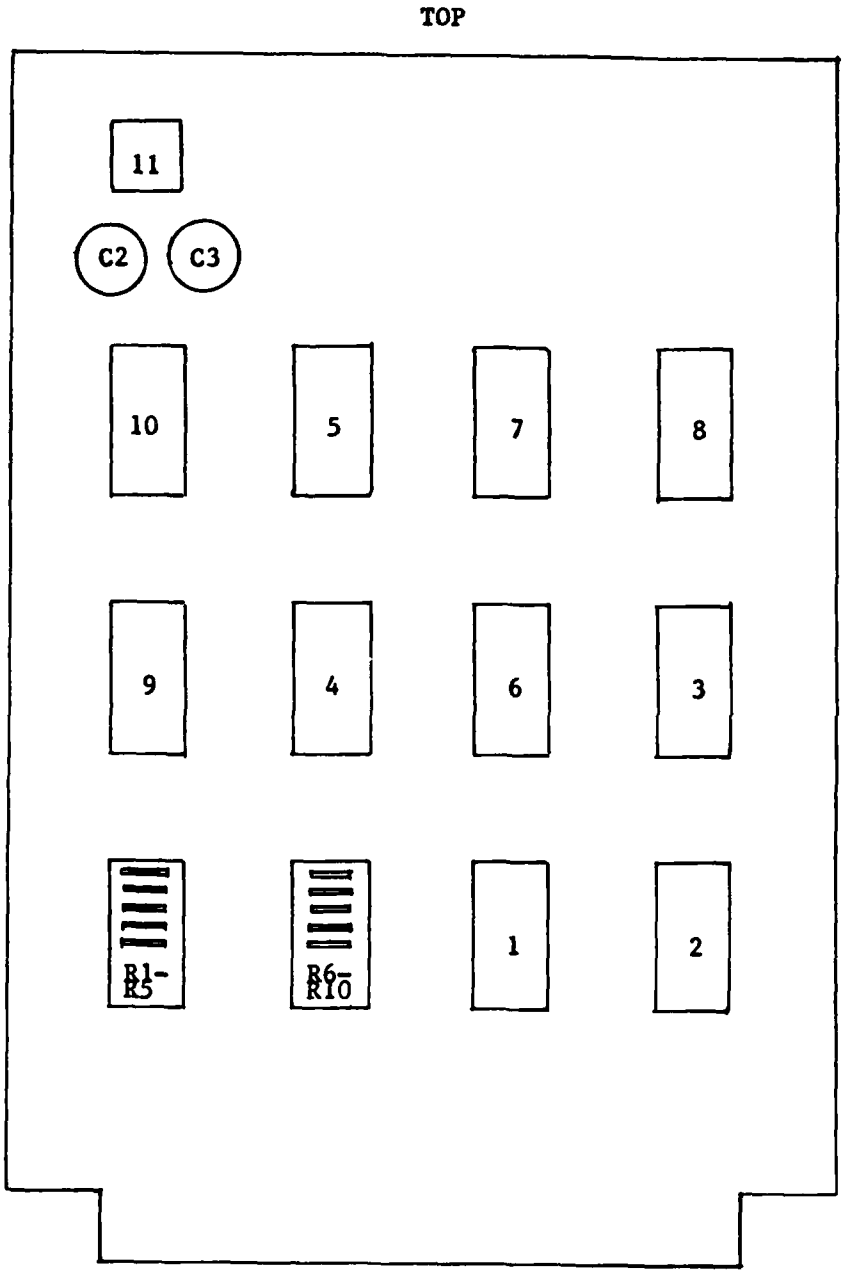
F. SCANNER MODIFICATIONS

Several minor modifications were made to the scanner to accommodate the MK38P70 controller:

1. Resistors were placed on I/O Board 4 between the inputs to inverters (connected between Port CU1 and the 3-to-8 decoder) and ground. These were required since open collector type inverters had been used which could not be properly driven by the 8255A PPI.

2. The scanner motor speed required adjustment. Speed had to be reduced from approximately 425 RPM to 410 RPM. A slower speed was necessary since an interval slightly greater than 900 microseconds between CCD lines was needed in order to process added program instructions. (This point will be further discussed in Chapter 5.)

3. The cable containing Port B2 and CU2 lines was cut for insertion of the threshold monitor and adjust circuit. Connectors were



1,2,3: 74LS08 AND
6,7,8: 74LS32 OR
4,5,9,10: 74LS04 INV

R1-R10: 3.6KΩ
C2,C3: 47μf
11: 7805 +5 Reg.

Fig. 4.14 Threshold Monitor and Adjust Circuit Board Layout

added such that the cable can be reconnected to bypass the circuit. This arrangement permits complete reversion to the original F-8 controller system.

4. Additional components were added to the scanner control panel. All operator controls are now located here, including three of the four sense switches originally located on the F-8 Formulator front panel.

Thus far, all changes made to implement the controller have been straightforward. Hardware differences between the MK38P70 and F-8 controllers amounted to elimination of the F-8 Formulator and its peripherals, incorporation of two additional circuit boards into scanner hardware, additions to the control panel, and the other minor modifications listed immediately above. Software changes consisted of elimination of F-8 peripheral peculiar portions of EOPS2 and addition of I/O instructions needed for the PPIs. Everything to this point has been fully implemented; testing and evaluation of this implementation is the subject of Chapter 5. The following section of this chapter, however, outlines some considerations for future implementation of data compression schemes.

G. DATA COMPRESSION CONSIDERATIONS

The scanner system is a local operation, set up for experimental purposes in the laboratory. A coaxial cable connects the scanner to the display interface logic; the data handling capacity of this line permits near real time operation of the scanner/printer system. The CCD data bits comprising a scanned line are clocked out serially at 800 kilobits per second over the coaxial cable. Previous research has indicated that a practical and cost effective

transmission system should utilize a 56 kilobit per second leased telephone line (references 2 and 11). Preserving a reasonable throughput rate in the system using such a line requires a data compression-decompression scheme.

Of interest here is the impact, if any, that inclusion of data compression would have on the microprocessor controller design. Thus far, two compression-decompression schemes have been proposed by other members of the research group, one by Dishop (2), and another by Lin (5). Dishop's method uses hardware logic to achieve compression using the B-1 data compression code. CCD data, as well as display commands, are compressed and decompressed using this scheme. Lin, on the other hand, uses a software based scheme capable of using several data compression codes, but he does not encode display commands. Further research may indicate additional schemes or modifications to the two already proposed. In any event, a final compression-decompression scheme for use with the scanner has not been settled upon. This precludes a detailed analysis for inclusion of data compression into the controller. However, Appendix E pursues the influence of the two proposed schemes on controller design, in the event one or the other scheme is chosen for final compressor-decompressor design.

The main question in considering the controller along with data compression is whether the MK38P70 controller would have to be scrapped. The primary functions now handled by the controller include automatic thresholding and generation of the display control commands. If the compression-decompression scheme chosen allows for a functionally distributed scanner architecture, all or parts of these functions can continue to reside on one or more MK38P70s using

appropriate interfaces. In this case, the MK38P70 would not have to be removed but additional hardware might be necessary in order to perform functions associated with compression and decompression. Data compression functions cannot be directly superimposed onto the controller; this is because the MK38P70 cannot read in data at a rate of 800 kilobits per second for processing.

CHAPTER 5

TESTS AND EVALUATION

A. GENERAL

Implementation of the controller designed in Chapter 4 required an ongoing evaluation of the ability of the circuit to perform at least as well as the F-8 controller. Several types of tests were performed during the course of the research. They were: (1) tests needed to establish the ability of certain elements to meet specifications, (2) tests to verify the software programs, and (3) performance tests of the dedicated microprocessor-based system itself. The role of these tests in microprocessor design is the subject of this chapter.

B. PORT INTERFACE TESTING

Prior to an attempt to use the MK38P70 as the scanner control element, it was necessary to establish the practicality of using the 8255As for the port interface. One way to test the PPIs was to configure the F-8 Formulator as an emulator of the MK38P70. The PPI port interface was constructed on a wirewrap circuit board and connected to the F-8 Quad I/O board in a piggyback fashion. As shown in Figure 5.1, the four F-8 ports of the Quad I/O board were used to simulate the four 8-bit ports of the MK38P70. The PPI port were connected to the scanner hardware. The EOPS2 program was rewritten to include the additional instructions required for PPI I/O operations.

There were several reasons for using this test:

1. The ability of the PPIs to effect a reduction of F-8 ports

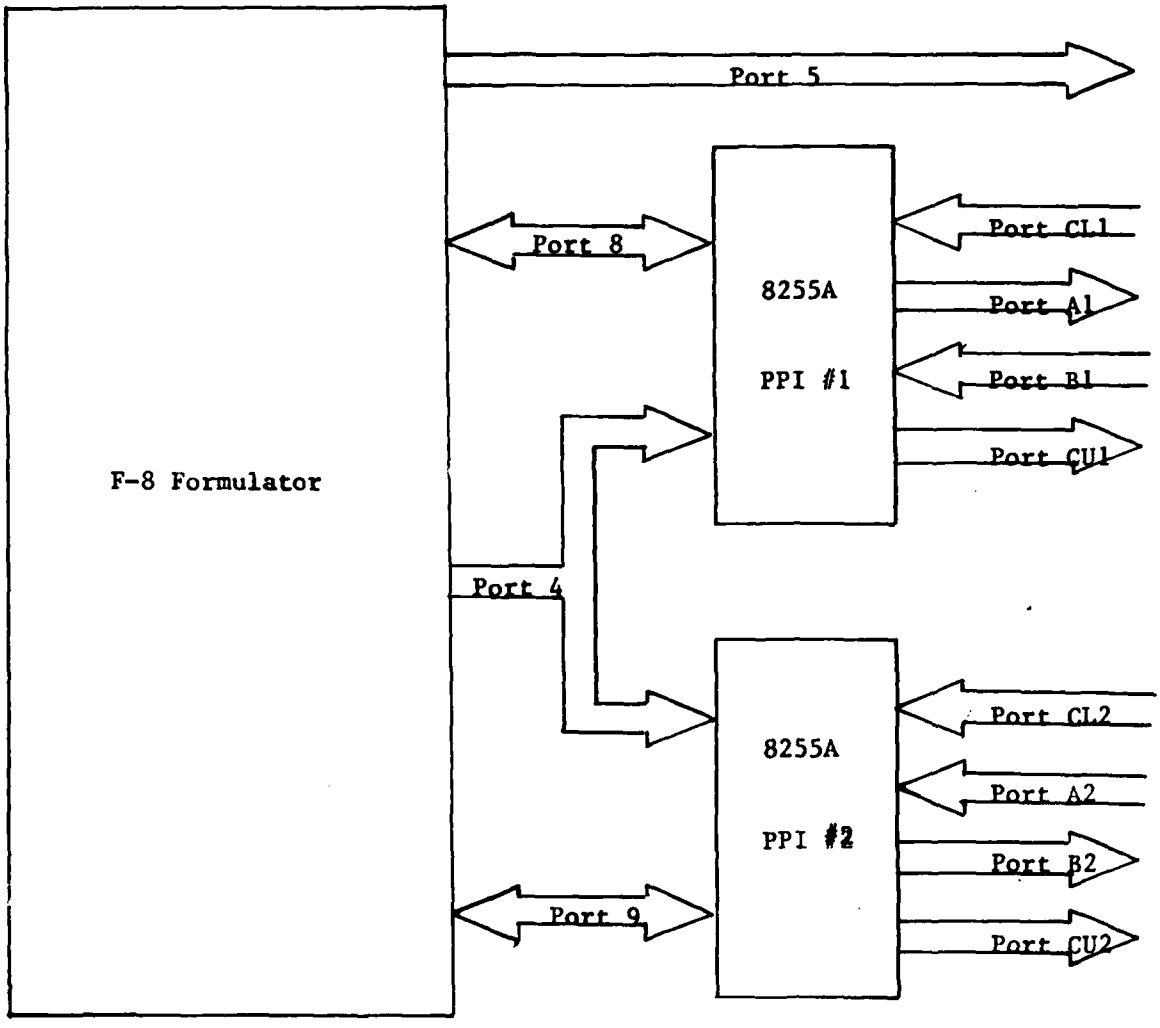


Fig. 5.1 F-8 Formulator Used as MK38P70 Emulator

could be evaluated.

2. Assuming the interface performed adequately, the modified EOPS2 program could be tried and scanner performance could be evaluated using the interface.

3. If the modified scanner program worked using the interface, the modified program could be transferred essentially intact to the MK38P70. The only major change would be a renumbering from the F-8 Quad I/O port numbers to the MK38P70 port numbers.

4. The F-8 Formulator had a debug program which could be used to stop and check the control program at any program step. The debug feature would permit the logic states of the scanner hardware to be checked at each stage of program execution.

Initially, a slightly different interface was used from that shown in Figure 5.1. Port CU2 was tied to the four pins of I/O Board 5 which control assembly and transmission of display commands. Debugging revealed all logic transactions were occurring in proper sequence but that CCD line data and display commands were not being transmitted correctly over the coaxial cable to the display logic. Eventually it was discovered that additional PPI instructions in the XMITS subroutine resulted in an improperly timed $\overline{\text{SEND}}$ pulse. (The $\overline{\text{SEND}}$ pulse controls transmission of display commands.) To correct the problem the four pins of I/O Board 5 were connected directly to F-8 Port 5. The original timing for the $\overline{\text{SEND}}$ pulse was restored, and after some additional debugging, the configuration of Figure 5.1 performed all scanner control functions as well as the original F-8 configuration.

Correct functioning of the port interface represented a significant milestone in development of the controller. The following

baseline was then established for further work:

1. The functions of nine F-8 ports were successfully combined into four 8-bit I/O ports. This proved that a microprocessor based configuration was feasible.

2. Both soft and hard display copy using the interface were qualitatively equivalent to that obtained in absence of the interface.

3. The port interface was completely transparent to the scanner operator. EOPS2 was loaded and scanner controls functioned in the same manner as in the original system.

C. TESTS SUPPORTING SOFTWARE DEVELOPMENT

The MEOSC program eventually derived for the MK38P70 evolved from successive program changes to EOPS2. Once the modified EOPS2 program functioned correctly using the F-8 emulating the MK38P70, there remained the tasks of renumbering ports, burning the program into an EPROM, and debugging and evaluating program performance in the controller circuit.

The four F-8 Quad I/O ports are slightly different from the four MK38P70 ports. Two of the MK38P70 ports, Ports 0 and 1, are "fast" ports, that is, input and output instructions execute in half the time required by the other MK38P70 ports as well as the F-8 Quad I/O ports (4, 5, 8, and 9). Ports 0 and 1 of the MK38P70 were used to replace the F-8 emulator Ports 8 and 5, respectively, whereas MK38P70 Ports 4 and 5 were used to replace emulator Ports 4 and 9, respectively. Some initial program testing again showed that the only critical problem with the new scheme was proper generation of the $\overline{\text{SEND}}$ pulse. Since MK38P70 Port 1 was used, the $\overline{\text{SEND}}$ pulse was only being generated for half of its required duration. The problem was corrected

by using some duplicate program instructions in the XMITS subroutine.

Initially, there was no way to stop program execution in the microprocessor for testing purposes. This dilemma was resolved by creation of a software debug tool consisting of a wait loop. The wait loop instructions were inserted into a desired location in the control program and the program was then burned into an EPROM. (The F-8 Formulator was used to write the microprocessor control program and, together with the EPROM programming circuit, burn the program into the EPROM.) Successive application of the wait loop in different program locations burned into different EPROMs enabled verification of the status of interface logic and identification and correction of hardware and software faults.

Some additional remarks regarding testing are relevant here. During this testing stage, the microprocessor was mounted on the same wirewrap circuit board that had been used for port interface testing. This arrangement facilitated making required corrections. Once the wait loop had been used to verify all logic and correct the $\overline{\text{SEND}}$ pulse, display copy was scrutinized. At first, severely distorted images were obtained which no amount of program debugging could resolve. A timing analysis suggested the possibility that control sequences were exceeding the 900 microsecond limit between CCD lines. This possibility was eventually validated by retarding the motor speed, which in turn slightly slowed the clockout rate of CCD lines and lengthened the processing interval for control sequences. It is theorized that machine dependent characteristics of the MK38P70 resulted in program execution cycles exceeding the 900 microsecond interval, resulting in CCD pixels corresponding to some lines being

printed, while those corresponding to other lines were not. It should also be possible to obtain good copy by slightly increasing the external time base speed of the MK38P70 instead of slowing the motor.

Once the prototype controller circuit and program had demonstrated consistent and repeatable performance in terms of acceptable hard and soft copy, the controller circuit was constructed on a printed circuit board as described in Chapter 4. The final product of the testing described here is the MEOSC program (Appendix B). Section D below compares the performance of the MK38P70 controller to that of the F-8 controller.

D. SYSTEM TESTING

System testing of the MK38P70 controller was deferred until the threshold monitor and adjust circuit was operational. This circuit was tested on a breadboard and then permanently constructed on a wirewrap board, as described in Chapter 4. The only testing of this circuit that was conducted was verification of all gate logic and proper functioning of the HEX displays. The circuit was then placed in the circuit rack along with the MK38P70 controller circuit to obtain the final system configuration.

The final testing of the MK38P70 basically boiled down to a GO/NO-GO performance criterion: does the MK38P70 controlled system produce both hard and soft display copy comparable to that obtained with the F-8 controlled system? Several approaches were taken in this test. Hard and soft copies were taken of an IEEE standard facsimile test chart under various thresholding and lighting conditions using both controllers. Next, a number of documents with different print characteristics were scanned under similar thresholding conditions.

Some copies of printer samples from these tests are contained in Appendix D.

No significant visible differences were found in comparisons of MK38P70 controlled scanner copy to F-8 controlled scanner copy. This was true for both hard and soft copy under various threshold conditions using the standard facsimile chart as well as different documents. The MK38P70 controller performance was therefore rated as a GO.

CHAPTER 6

CONCLUSION

A. SUMMARY OF RESULTS

The goal of implementing a real-time, dedicated microprocessor controller for the scanner system was attained through use of the MK38P70-based controller. This implementation proved the technical feasibility of employing a dedicated microprocessor as the control element of the essentially closed-loop scanner system used in the laboratory. The performance of the controller was highly satisfactory. It fulfilled its required function, namely, it produced satisfactory reproducibility of scanned documents on a consistent basis.

The MK38P70 microprocessor, the key component of the controller, proved acceptable for meeting design criteria. It was chosen over more versatile microprocessors primarily for the following reasons:

1. The instruction set was F-8 compatible. Compatibility greatly enhanced implementation, since the F-8 Formulator microcomputer being replaced was able to be used as an invaluable system development tool in the laboratory setting. Debugging and testing were accomplished rapidly because of this capability.

2. The port capacity of the MK38P70 was sufficient to meet system requirements. The architecture gave the possibility of substituting an MK38P73 in order to accommodate future add-ons.

3. The 2716 EPROM chosen for this application proved to be adequate. The MK38P70 had relatively simple physical and logical EPROM

interface features.

It can be concluded that these factors made the MK38P70 the best device for this application, considering the scope of control functions it had to perform and the given laboratory constraints.

Devising a good port interface was a crucial point in system development. The final choice for the interface consisted of utilizing two 8255A PPI devices. The PPIs were used in lieu of other options because they: (1) were general purpose, machine independent, programmable chips which were readily adaptable to the application; (2) provided the proper number of required 4-bit and 8-bit port combinations in order to obtain an interface with few chips; and (3) were inexpensive and readily available. Other options considered but rejected included expanding outputs, combining inputs, simultaneously expanding outputs and combining inputs, and using other peripheral interfacing devices.

During debugging and testing, several observations were made about the MK38P70 based system. Timing was critical in the logic transactions between the controller and the portion of I/O Board 5 which generated display commands. Proper generation of the $\overline{\text{SEND}}$ pulse in the XMITS subroutine necessitated using MK38P70 Port 1 to interface with I/O Board 5 instead of using a PPI port. No other interfaces proved to be as time critical, and PPI ports were used successfully. However, the final controller circuit operated slightly more slowly than expected, which necessitated a slight downward adjustment of the scanner motor speed.

Implementation of the MK38P70 controller resulted in some improvements in the over-all scanner system. Elimination of the F-8

Formulator and its peripherals resulted in a dramatic decrease in space requirements and eventual cost of the system. All control functions were consolidated onto the scanner control panel. A threshold monitor and adjust capability was added so that the current threshold level can be shown without need for the video console. This feature provides a capability to precisely control the voltage threshold level used to digitize CCD pixels.

B. AREAS FOR FURTHER RESEARCH

1. Data Compression. Data compression was considered as a peripheral issue in controller design. Appendix E outlines possibilities for implementing two potential compression schemes. These schemes do not negate using the MK38P70 controller; however, additional considerations may enter once a scheme has been chosen for implementation. Therefore, more research may be warranted regarding interfacing the chosen data compressor-decompressor to the scanner system and the role of the MK38P70 in such a system.

2. Controller speed. Replacing the 2.0 MHz crystal with a slightly faster time base for the MK38P70 should be considered. Experimenting with a faster time base should allow the motor to be readjusted back to its original speed. Also, adjusting the time base may provide additional insight into machine-dependent operating characteristics of the MK38P70 as compared to the F-8.

3. Serial Port. A serial port capability can be achieved by substituting an MK38P73 for the MK38P70. The serial port permits an interface capability with some add-on devices which cannot be achieved with the existing controller configuration. If additional features are to be added to the scanner system, use of a serial port should be

considered. Use of the serial port will require a study of programming requirements peculiar to the MK38P73.

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APPENDIX A

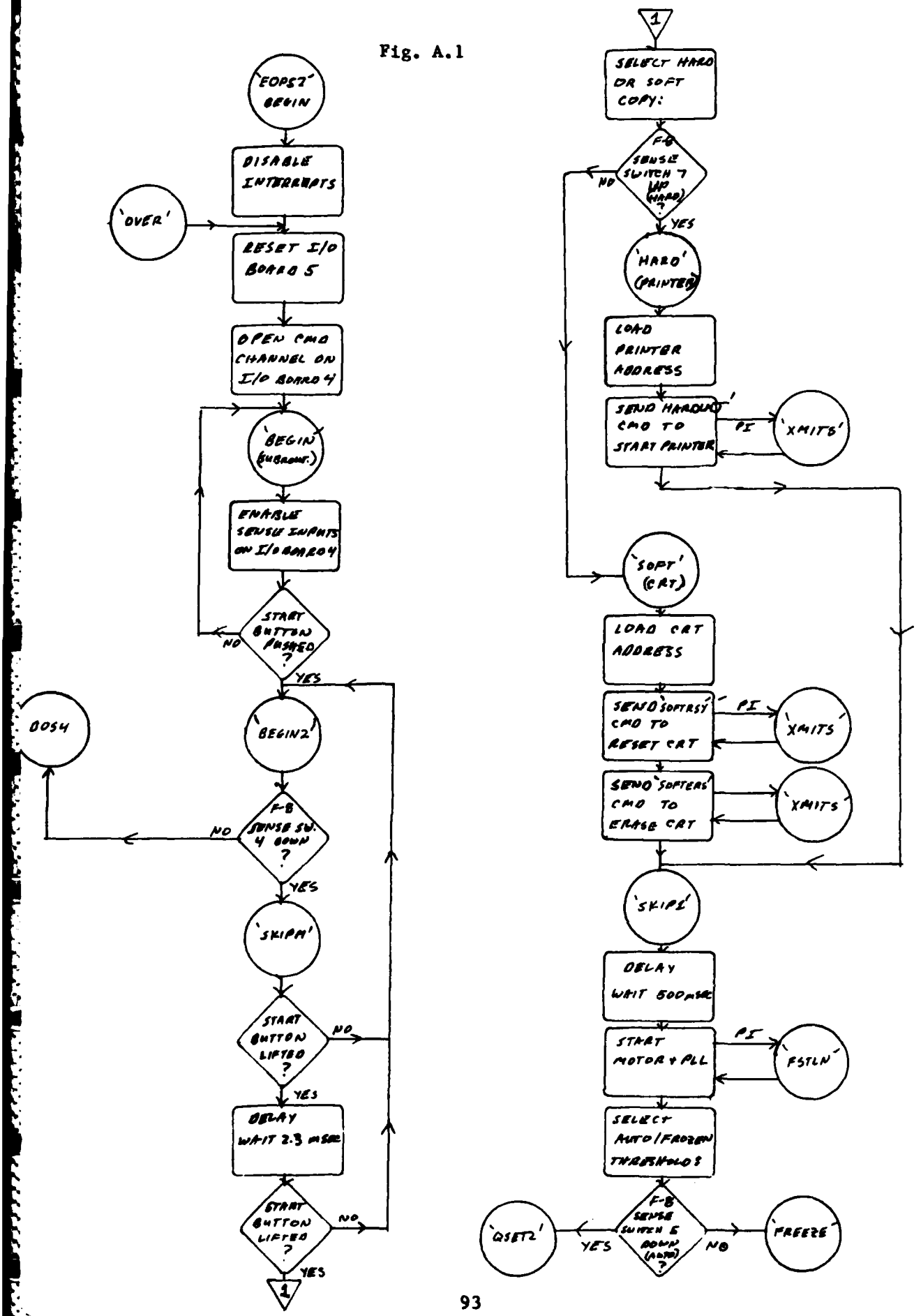
EOPS2 FLOWCHARTS

EOPS2 is the bound document scanner control software for the F-8 Formulator. This appendix contains flowcharts outlining the functions performed by EOPS2. A complete program listing of EOPS2 can be found in Stanton's thesis (10). The flowcharts are also useful for understanding MEOSC, the MK38P70 controller software, which is a modified version of EOPS2.

The flowcharts are arranged as follows (refer to EOPS2 program to find the subroutines and portions of the main calling program listed below):

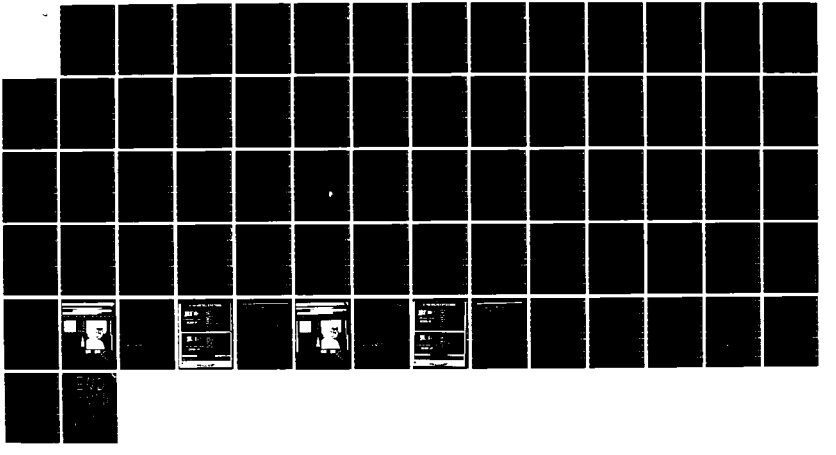
Fig. A.1 - Begin MAIN4; scanner initialization.
Fig. A.2 - Subroutine QSET2 (automatic thresholding).
Fig. A.3 - MAIN4 segments SHOW (display threshold level) and FREEZE (frozen thresholding).
Fig. A.4 - MAIN4 segments BJA (display CCD data) and ENDCHK (end of page check)
Fig. A.5 - MAIN4 segment NORMCNT (finalization - normal page); subroutine ENDLN (end of CCD line)
Fig. A.6 - Subroutines FSTLN (beginning of CCD data) and XMITS (transmit display commands)

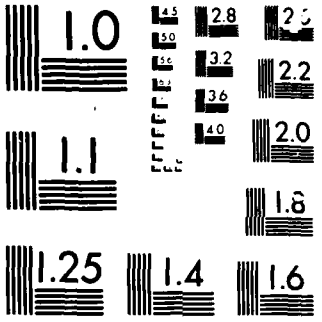
Fig. A.1


'EOPS2' BEGIN
DISABLE INTERRUPTS
'OVER'
RESET I/O BOARD 5
OPEN CMD CHANNEL ON I/O BOARD 4
'BEGIN' (SUBROUT.)
ENABLE SENSE INPUTS ON I/O BOARD 4
START BUTTON PUSHED ?
NO
YES
'BEGIN2'
F-B SENSE SW. 4 DOWN ?
NO
YES
'SKIPA'
START BUTTON LIFTED ?
NO
YES
DELAY WAIT 2.3 MSEC
START BUTTON LIFTED ?
NO
YES
1
0054
1
SELECT HARD OR SOFT COPY:
F-B SENSE SWITCH 7 UP (HARD) ?
NO
YES
'HARD' (PRINTER)
LOAD PRINTER ADDRESS
SEND 'HARDOUT' CMD TO START PRINTER
PI
'XMITB'
'SOFT' (CRT)
LOAD CRT ADDRESS
SEND 'SOFTRST' CMD TO RESET CRT
PI
'XMITS'
SEND 'SOFTERS' CMD TO ERASE CRT
'XMITS'
'SKIPI'
DELAY WAIT 500 MSEC
START MOTOR + PLL
PI
'FSTLN'
SELECT AUTO/FROZEN THRESHOLDS
F-B SENSE SWITCH 6 DOWN (AUTO) ?
YES
NO
'QSET2'
'FREEZE'

AD-A141 525 A DEDICATED MICROPROCESSOR CONTROLLER FOR A BOUND DOCUMENT SCANNER(U) ARMY MILITARY PERSONNEL CENTER ALEXANDRIA VA E C SHAFFER JUN 84 2/2

UNCLASSIFIED F/G 14/5 NL





MICROCOPY CHART

Fig. A.2

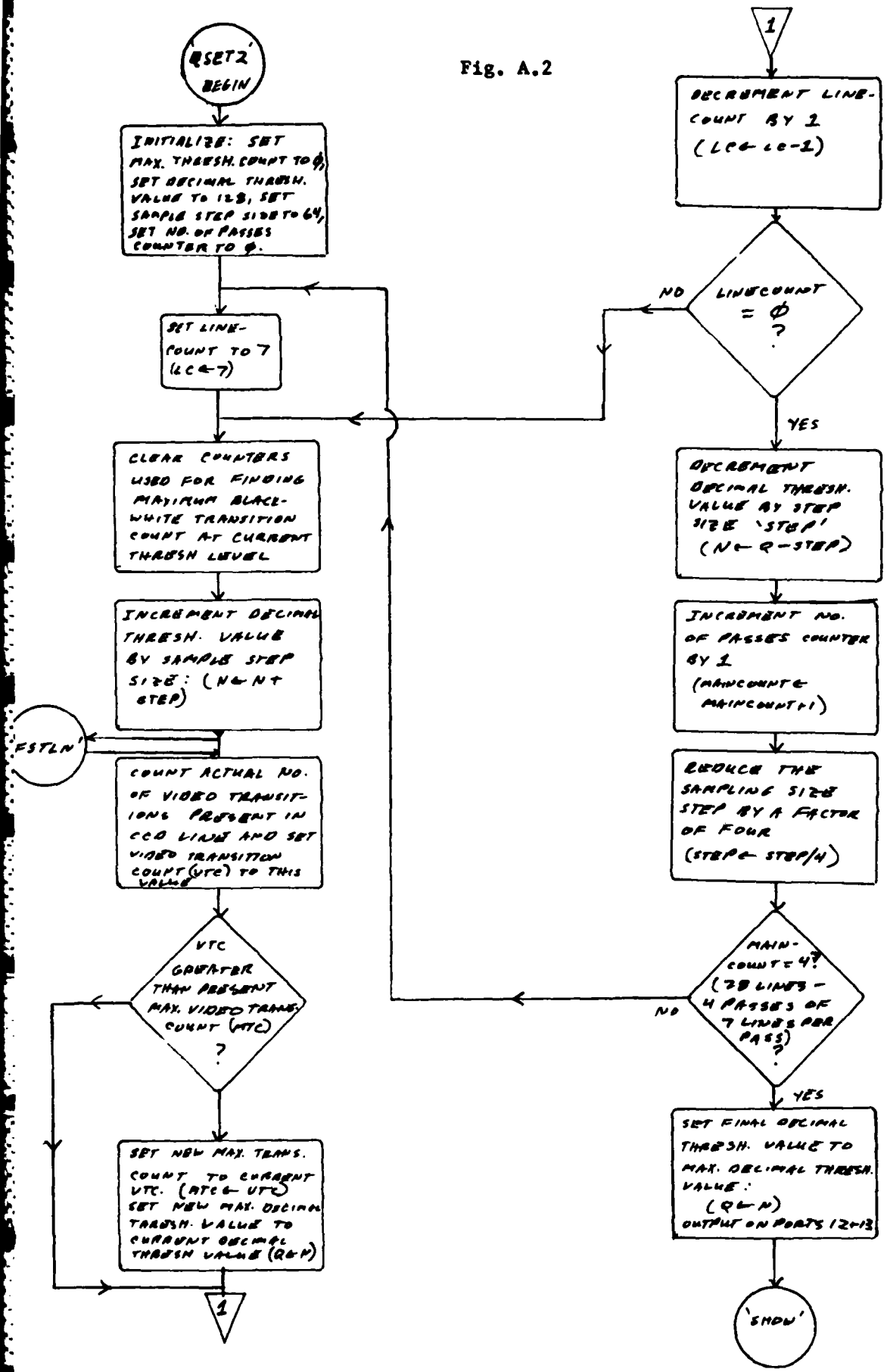

'RSET2' BEGIN
INITIALIZE: SET MAX. THRESH. COUNT TO Ø, SET DECIMAL THRESH. VALUE TO 128, SET SAMPLE STEP SIZE TO 64, SET NO. OF PASSES COUNTER TO Ø.
SET LINE-COUNT TO 7 (LC ← 7)
CLEAR COUNTERS USED FOR FINDING MAXIMUM BLACK-WHITE TRANSITION COUNT AT CURRENT THRESH LEVEL
INCREMENT DECIMAL THRESH. VALUE BY SAMPLE STEP SIZE: (N ← N + STEP)
'STLN'
COUNT ACTUAL NO. OF VIDEO TRANSITIONS PRESENT IN CCD LINE AND SET VIDEO TRANSITION COUNT (VTC) TO THIS VALUE
VTC GREATER THAN PRESENT MAX. VIDEO TRANS. COUNT (MTC) ?
SET NEW MAX. TRANS. COUNT TO CURRENT VTC. (MTC ← VTC) SET NEW MAX. DECIMAL THRESH. VALUE TO CURRENT DECIMAL THRESH VALUE (Q ← N)
1
1
DECREMENT LINE-COUNT BY 1 (LC ← LC-1)
LINECOUNT = Ø ?
NO
YES
DECREMENT DECIMAL THRESH. VALUE BY STEP SIZE 'STEP' (N ← Q-STEP)
INCREMENT NO. OF PASSES COUNTER BY 1 (MAINCOUNT ← MAINCOUNT+1)
REDUCE THE SAMPLING SIZE STEP BY A FACTOR OF FOUR (STEP ← STEP/4)
MAIN-COUNT = 4? (28 LINES - 4 PASSES OF 7 LINES PER PASS) ?
NO
YES
SET FINAL DECIMAL THRESH. VALUE TO MAX. DECIMAL THRESH. VALUE: (Q ← N) OUTPUT ON PORTS 12+13
'SHOW'

Fig. A.3

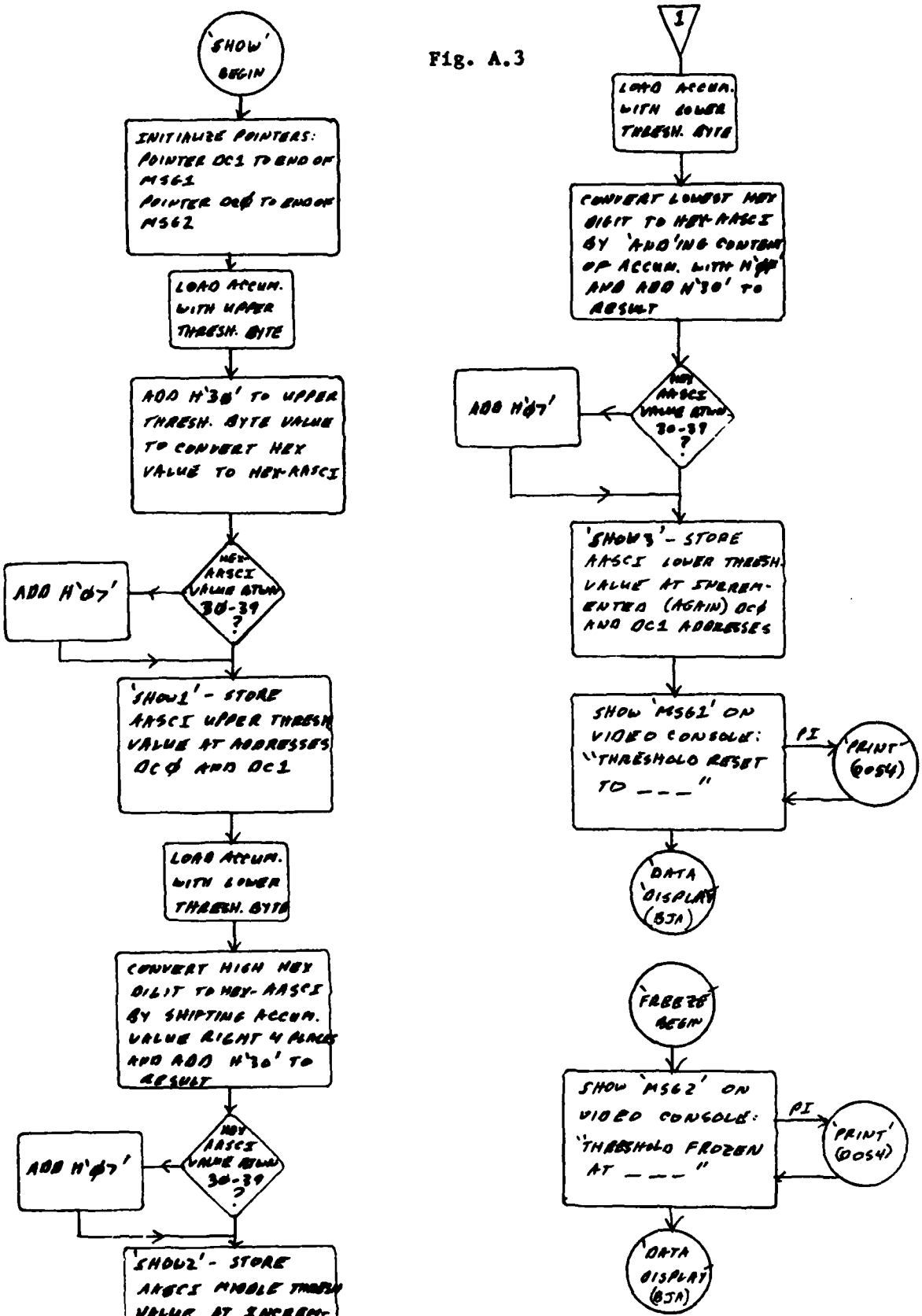

'SHOW' BEGIN
INITIALIZE POINTERS: POINTER OC1 TO END OF MSG1 POINTER OCØ TO END OF MSG2
LOAD ACCUM. WITH UPPER THRESH. BYTE
ADD H'3Ø' TO UPPER THRESH. BYTE VALUE TO CONVERT HEX VALUE TO HEX-ASCI
HEX-ASCI VALUE RTNG 3Ø-39 ?
ADD H'Ø7'
'SHOW1' - STORE ASCI UPPER THRESH VALUE AT ADDRESSES OCØ AND OC1
LOAD ACCUM. WITH LOWER THRESH. BYTE
CONVERT HIGH HEX DIGIT TO HEX-ASCI BY SHIFTING ACCUM. VALUE RIGHT 4 PLACES AND ADD H'3Ø' TO RESULT
HEX ASCI VALUE RTNG 3Ø-39 ?
ADD H'Ø7'
'SHOW2' - STORE ASCI MIDDLE THRESH VALUE AT INCREMENTED OCØ AND OC1 ADDRESSES
1
1
LOAD ACCUM. WITH LOWER THRESH. BYTE
CONVERT LOWEST HEX DIGIT TO HEX-ASCI BY 'AND'ING CONTENT OF ACCUM. WITH H'ØF' AND ADD H'3Ø' TO RESULT
HEX ASCI VALUE RTNG 3Ø-39 ?
ADD H'Ø7'
'SHOW3' - STORE ASCI LOWER THRESH VALUE AT UNINCREMENTED (AGAIN) OCØ AND OC1 ADDRESSES
SHOW 'MSG2' ON VIDEO CONSOLE: "THRESHOLD RESET TO ___"
PI
PRINT (DOS4)
DATA DISPLAY (BJA)
FREEZE BEGIN
SHOW 'MSG2' ON VIDEO CONSOLE: "THRESHOLD FROZEN AT ___"
PI
PRINT (DOS4)
DATA DISPLAY (BJA)

Fig. A.4

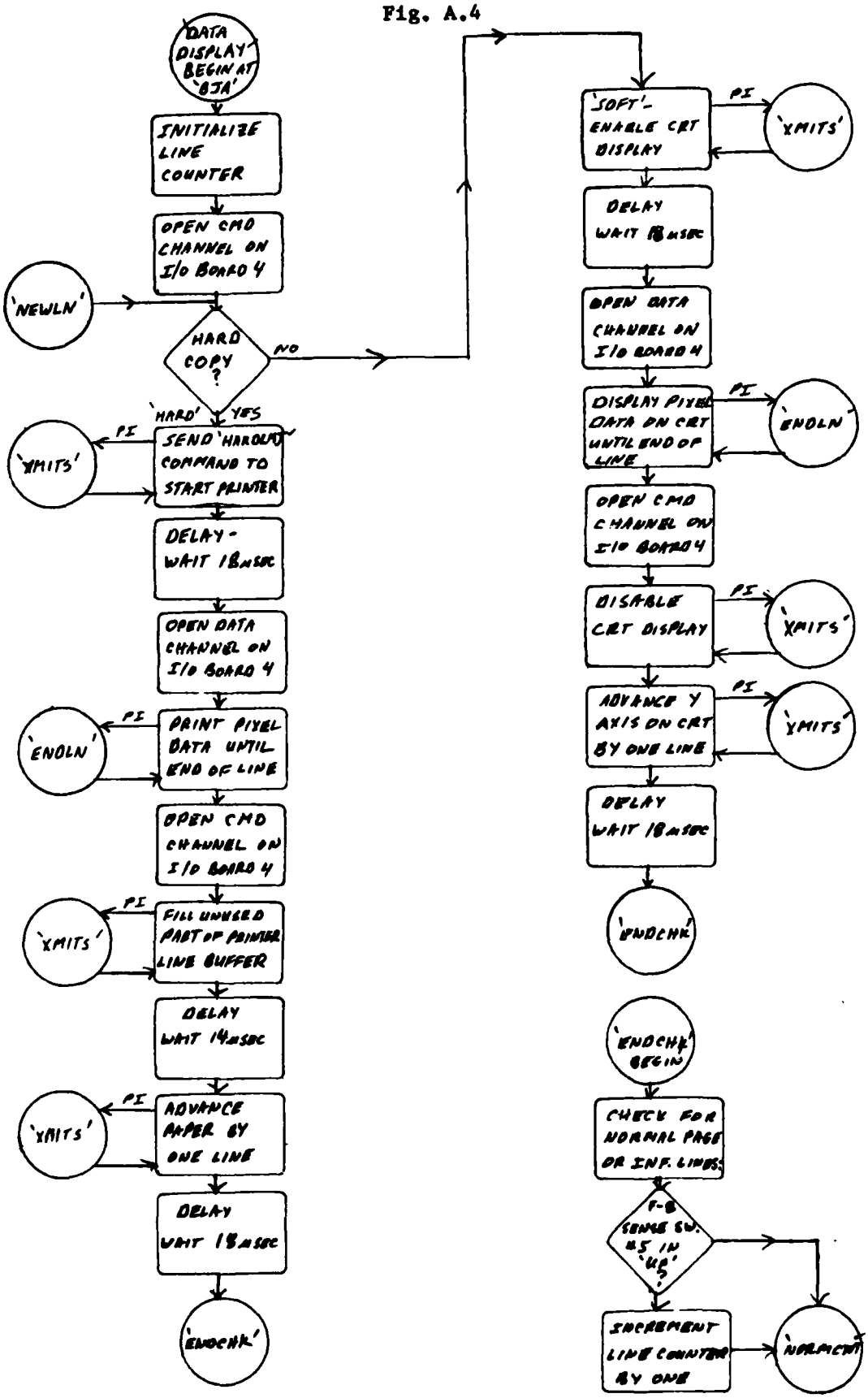
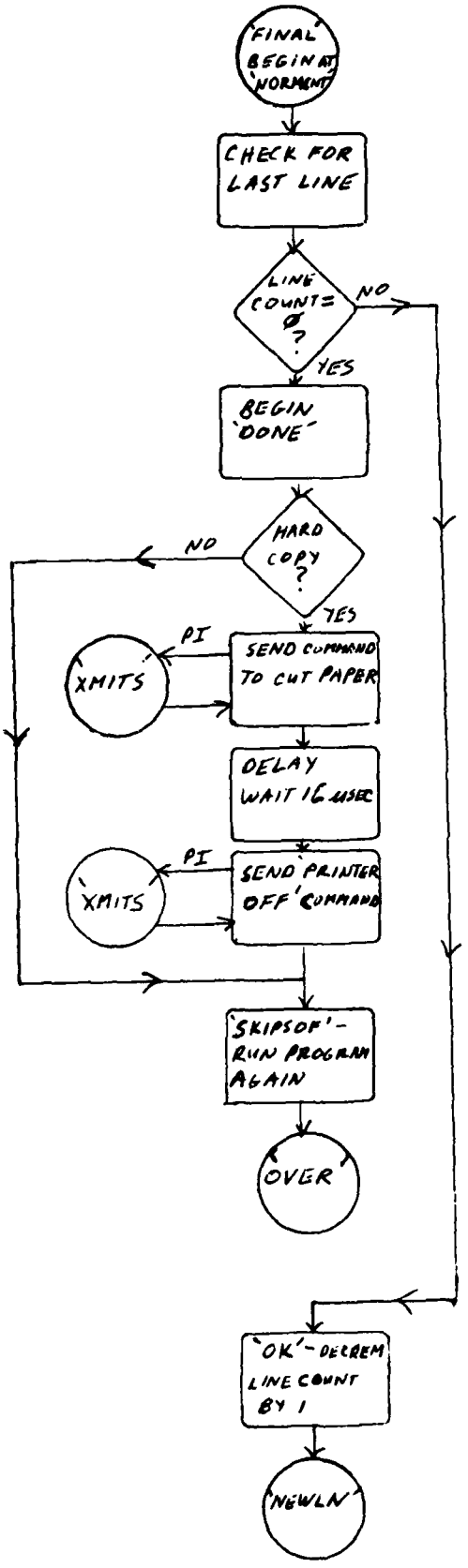

DATA DISPLAY BEGIN AT 'BJA'
INITIALIZE LINE COUNTER
OPEN CMD CHANNEL ON I/O BOARD 4
'NEWLN'
HARD COPY ?
NO
'HARD'
YES
'XMITS'
PI
SEND 'HARDCOPY' COMMAND TO START PRINTER
DELAY - WAIT 18msec
OPEN DATA CHANNEL ON I/O BOARD 4
'ENDLN'
PRINT PIXEL DATA UNTIL END OF LINE
OPEN CMD CHANNEL ON I/O BOARD 4
FILL UNUSED PART OF PRINTER LINE BUFFER
DELAY WAIT 14msec
ADVANCE PAPER BY ONE LINE
DELAY WAIT 18msec
'ENDCHK'
'SOFT' - ENABLE CRT DISPLAY
DELAY WAIT 18msec
OPEN DATA CHANNEL ON I/O BOARD 4
DISPLAY PIXEL DATA ON CRT UNTIL END OF LINE
OPEN CMD CHANNEL ON I/O BOARD 4
DISABLE CRT DISPLAY
ADVANCE Y AXIS ON CRT BY ONE LINE
DELAY WAIT 18msec
'ENDCHK'
'ENDCHK' BEGIN
CHECK FOR NORMAL PAGE OR INF. LINES
F-8 SENSE SW. #5 IN 'UP' ?
INCREMENT LINE COUNTER BY ONE
'NORMCNT'

Fig. A.5


'FINAL' BEGIN AT 'NORMENT'
CHECK FOR LAST LINE
LINE COUNT = Ø ?
NO
YES
BEGIN 'DONE'
HARD COPY ?
NO
YES
PI
XMITS
SEND COMMAND TO CUT PAPER
DELAY WAIT IC USEC
PI
XMITS
SEND PRINTER OFF 'COMMAND
'SKIPSOF' - RUN PROGRAM AGAIN
'OVER'
'OK' - DECREM LINE COUNT BY 1
'NEWLN'

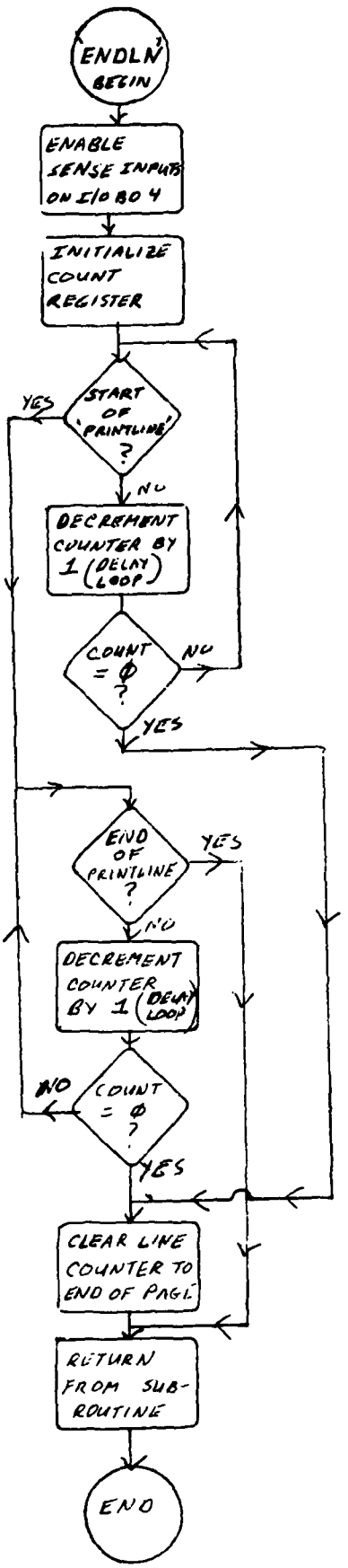
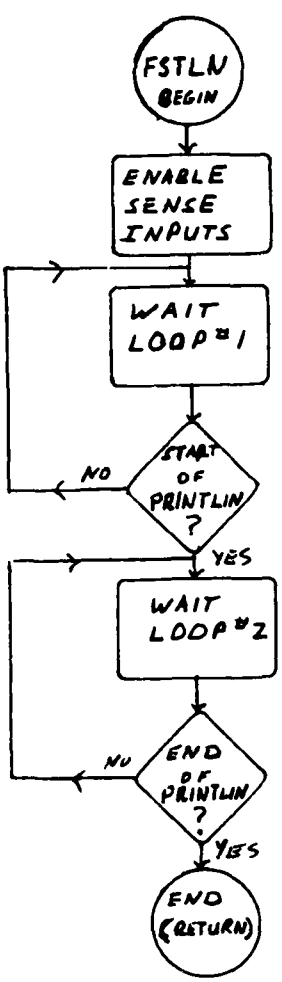
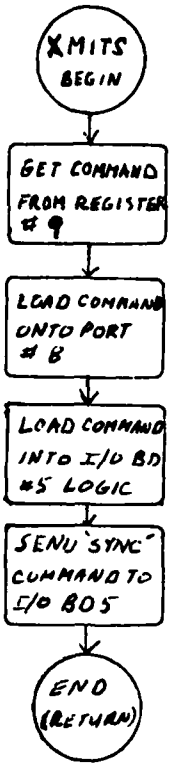

'ENDLN' BEGIN
ENABLE SENSE INPUTS ON I/O BD 4
INITIALIZE COUNT REGISTER
YES
START OF 'PRINTLINE' ?
NO
DECREMENT COUNTER BY 1 (DELAY LOOP)
COUNT = Ø ?
NO
YES
YES
END OF PRINTLINE ?
NO
DECREMENT COUNTER BY 1 (DELAY LOOP)
NO
COUNT = Ø ?
YES
CLEAR LINE COUNTER TO END OF PAGE
RETURN FROM SUB-ROUTINE
END

Fig. A.6


FSTLN
BEGIN
ENABLE
SENSE
INPUTS
WAIT
LOOP #1
START
OF
PRINTLIN
?
NO
YES
WAIT
LOOP #2
END
OF
PRINTLIN
?
NO
YES
END
(RETURN)


XMITS
BEGIN
GET COMMAND
FROM REGISTER
#9
LOAD COMMAND
ONTO PORT
#8
LOAD COMMAND
INTO I/O BD
#5 LOGIC
SEND 'SYNC'
COMMAND TO
I/O BD5
END
(RETURN)

APPENDIX B

MEOSC: MK38P70 CONTROLLER SOFTWARE

This appendix contains the program listing of MEOSC (Microprocessor Electro-Optical Scanner Control). MEOSC consists of a main calling program and several relocatable modules which have been assembled, linked, and loaded into a 2716 EPROM located on the MK38P70. A complete copy of this program is stored on floppy disk; the disk HELP file describing the software package has been included to serve as an overview.

```
+-----------------------------------------------------+
  THIS IS THE MAIN DESCRIPTOR FILE FOR THIS DISK.
  IT DESCRIBES THE PROGRAMS ON IT AND HOW TO USE THEM.
+-----------------------------------------------------+
```

PROGRAMS MODIFIED AND DEBUGGED
BY
CPT ED SHAFFER, JULY 83.

***** USER INFORMATION *****

THE MK38P70 CONTROLLER PROVIDES THRESHOLD AND PRINTER CONTROL FOR THE BOUND DOCUMENT SCANNER. SOFTWARE IS IN A VARIETY OF FORMS DESIGNATED BY THE FILE ATTRIBUTE:

'00' IS A TEXT FILE SUCH AS THIS ONE OR ONE CONTAINING UNASSEMBLED SOURCE CODE.

'10' IS AN OBJECT CODE FILE THAT CAN BE LOADED AND/OR LIKED, DEPENDING ON THE SOFTWARE.

'30' IS A CORE IMAGE FILE THAT (WHEN LOCATED ON DISK DRIVE 0) IS LOADED AND EXECUTED AS A SYSTEM-LEVEL COMMAND WHEN THE FILENAME IS ENTERED.

'40' IS AN EXECUTIVE FILE FOR FACILITATING VARIOUS FILE OPERATIONS.

THE FILE MEOSC,30:1 (MICROPROCESSOR ELECTRO-OPTICAL SCANNER CONTROL) IS A COMPLETE SOFTWARE PACKAGE. IT CURRENTLY USES THRESHOLD SAMPLING ALGORITHM QSET2 BUT CAN BE ALTERED TO USE THE QSET1 SAMPLING ALGORITHM. QSET1 HAS AN INITIAL STEP SIZE (S1) OF 128 AND SAMPLES THE ENTIRE RANGE OF N (0 TO 1024). QSET2 HAS AN INITIAL STEP SIZE OF 64 AND SAMPLES THE RANGE OF N (128 TO 640). THE PROGRAM MEOSC RESIDES ON THE 2716 EPROM MOUNTED ON THE MK38P70. TO INITIATE SCANNING, ALL THAT IS REQUIRED IS APPLICATION OF POWER TO THE CONTROLLER CIRCUIT. IF AT ANY TIME PROGRAM EXECUTION IS IN ERROR, MEOSC CAN BE REINITIALIZED BY PUSHING THE RESET BUTTON ON THE SCANNER CONTROL PANEL.
ONCE THE SOFTWARE IS LOADED AND RUNNING, USER CONTROL IS PROVIDED THROUGH THE 'SENSE' SWITCHES ON THE SCANNER CONTROL PANEL. THE SWITCH FUNCTIONS ARE, FROM RIGHT TO LEFT:

SENSE #	DOWN	UP
1	NORMAL PAGE	INFINITE LINES
2	AUTOMATIC THRESHOLD	THRESHOLD FREEZE
3	SOFT COPY	HARD COPY

SENSE 1 IS USED FOR CALIBRATION AND CAUSES THE LINE COUNTER TO BE DISABLED SO THAT, WITH THE SCANNER IN 'FREEZE MODE' THE SOFTWARE WILL CONTINUE TO ACCEPT AN

INFINITE STREAM OF LINES WITHOUT ENDING THE PAGE. WHEN SENSE 1 IS RETURNED TO THE DOWN POSITION THE SOFTWARE IMMEDIATELY EXECUTES THE END OF PAGE SEQUENCE AND RESETS.

SENSE 2 IS USED FOR CONTROL OF THE AUTOMATIC THRESHOLD FEATURE. IN AUTOMATIC THRESHOLD MODE, 28 LINES OF THE LEADING MARGIN CONTAINING THE TEST PATTERN ARE SAMPLED TO OBTAIN THE THRESHOLD FOR EXISTING CONDITIONS. THE VALUE OF THE SELECTED THRESHOLD IS DISPLAYED ON THE PANEL IN HEX. IN THRESHOLD FREEZE MODES, THE LAST THRESHOLD SET BY THE SOFTWARE IS RETAINED AND DISPLAYED ON THE PANEL. NOTE: IF THE THRESHOLD IS ALTERED BY USING THE MANUAL ADJUST, THE MANUALLY LOADED VALUE WILL APPEAR ON THE PANEL DISPLAYS.

SENSE 3 SELECTS PRINTER OR CRT DOCUMENT DISPLAY.

MEOSC IS IN TURN COMPOSED OF SMALLER LINKABLE SOFTWARE PACKAGES. THESE MODULES ARE DESCRIBED BELOW:

MAIN4 ------ MAIN CALLING PROGRAM, VERSION 4

THIS MODULE CONTAINS THE MAINLINE ROUTINES OF MEOSC AND THEREFORE MUST BE AT THE BEGINNING LINK. IT CONTAINS ALL INITIALIZATIONS, SENSE SWITCH CONTROLS, LINE COUNTERS, COMMAND TRANSMISSIONS, CRT SCREEN PROMPTS, AND ATC CALLS. IT ALSO INITIALIZES THE SAMPLING ALGORITHM, QSET, THEREBY CONTROLLING SAMPLING RANGE AND INITIAL STEP SIZE (S1).

FSTLN ----- FIRST LINE

THIS SUBROUTINE POLLS THE SIGNAL CALLED 'PRINTLINE' WHICH IS PRESENT ON INPUT PORT CL1 IN THE LEAST SIGNIFICANT BIT POSITION. THE PROGRAM IS DESIGNED TO DETECT A RISING TRANSITION OF THE INPUT SIGNAL. THIS IS ACCOMPLISHED BY LOOPING UNTIL THE SIGNAL IS FALSE AND THEN LOOPING UNTIL IT IS TRUE. WHEN THIS PROGRAM RETURNS, THE TRANSITION WILL HAVE JUST OCCURRED. THE SOFTWARE IS DESIGNED TO TAKE INTO ACCOUNT THE INVERSION THAT TAKES PLACE THROUGH THE I/O PORT. THEREFORE THIS MODULE ACTUALLY SENSES A DOWNWARD TRANSITION OF THE SIGNAL 'PRINTLINE' IN THE SCANNER. THE GOAL IS TO CATCH THIS DOWNWARD TRANSITION WHICH SIGNALS THE END OF A LINE OF CCD DATA.

ENDLN ----- END OF LINE

THIS SUBROUTINE IS A SLIGHTLY MORE COMPLEX VERSION OF FSTLN. IT ALSO DETECTS A FALLING TRANSITION OF 'PRINTLINE' HOWEVER, IT IS DESIGNED TO WAIT FOR THIS TRANSISTION FOR 10 MS. THIS FEATURE WAS INCLUDED TO PREVENT THE SOFTWARE FROM GETTING HUNG UP AND OUT OF SYNC IF THE SCANNER SHOULD EITHER STOP IN MIDPAGE OR PRODUCE A FALSE START. IN THE

EVENT THAT THIS SUBROUTINE MUST WAIT MORE THAN 10 MS, IT SETS THE LINE COUNTER TO THE LAST LINE SO THAT WHEN THE RETURN TO THE MAIN PROGRAM OCCURS, THE LAST LINE CONDITION WILL BE INVOKED AND THE SOFTWARE WILL BE RESET. SHOULD IT BE NECESSARY TO HAVE THE SCANNER FROZEN IN MIDPAGE AND STILL HAVE THE SOFTWARE OPERATING SYNCRONOUSLY WITH THE SCANNER (FOR ALIGNMENT ETC.), SENSE SWITCH 1 SHOULD BE USED.

XMITS ----- TRANSMIT COMMAND

THIS IS THE SIMPLEST OF ALL THE SUBROUTINES. IT IS THE ONE WHICH ACTUALLY SENDS THE COMMANDS TO THE PRINTER OR CRT DISPLAY. IT EXPECTS THE COMMAND CHANNEL IN I/O BOARD 4 TO HAVE ALREADY BEEN OPENED AND THE COMMAND FOR TRANSMISSION TO BE STORED IN REGISTER 9.

QSET ----- QUICK THRESHOLD SAMPLING ALGORITHM

THIS MODULE SAMPLES THE RANGE OF THRESHOLD VALUES BY USING PROGRESSIVELY SMALLER AND SMALLER STEP SIZES. EACH TIME QSET IS CALLED, THE EXISTING STEP SIZE WILL BE USED FOR SEVEN SAMPLES AND WILL THEN BE DIVIDED BY FOUR BEFORE CONTROL IS RETURNED TO THE MAIN CALLING PROGRAM. WITH EACH VALUE OF N, VTC IS COMPARED TO THE PREVIOUS MAXIMUM VTC (MTC). THE VALUE OF N PRODUCING THE OVERALL MAXIMUM VALUE OF VTC IS STORED FOR EITHER THE NEXT INVOCATION OF QSET OR FOR THE MAIN CALLING PROGRAM TO LOAD INTO PORTS B2 AND CU2 AS THE OPTIMUM THRESHOLD VALUE FOR THE PAGE TO BE SCANNED.

********** EXAMPLES **********

SHOULD IT BE NECESSARY TO REASSEMBLE, RELINK, AND RELOAD THE MEOSC PACKAGE, THE FOLLOWING SEQUENCE OF COMMANDS WILL PRODUCE THIS RESULT:

```
ASM MAINM,00:1 TO MAIN4,10:1 NOLIST ERRS
ASM FSTLM,00:1 TO FSTLN,10:1 NOLIST ERRS
ASM ENDLM,00:1 TO ENDLN,10:1 NOLIST ERRS
ASM XMITM,00:1 TO XMITS,10:1 NOLIST ERRS
ASM QSETM,00:1 TO QSET ,10:1 NOLIST ERRS

LINK 1 CLEAR ORG 0 MAIN4,10:1
LINK 1 FSTLN,10:1
LINK 1 ENDLN,10:1
LINK 1 XMITS,10:1
LINK 1 QSET ,10:1
```

THE SOFTWARE IS NOW LOADED IN RAM. THE FILE MUST NEXT BE PLACED INTO A SINGLE FILE FOR LOADING INTO THE EPROM:

```
ASS DO WDISK FILENAME,10:1
DUMP 0000-0255
```

THIS PACKAGE WILL BE STORED ON DISK, AND CAN BE LOADED INTO RAM AT ANY TIME FOR EPROM PROGRAMMING BY THE COMMAND:

LOAD FILENAME,10:1

ONCE MEOSC HAS BEEN ASSEMBLED INTO A SINGLE FILE, IT IS READY TO BE BURNED INTO AN EPROM. THE EPROM PROGRAMMING CIRCUIT MUST BE MOUNTED ON THE F-8 CPU BOARD AND CONNECTED TO A +25 VOLT D.C. SUPPLY PER INSTRUCTIONS FOR THE EPROM PROGRAMMER. THE COMMAND 'EPROM' IS ENTERED ON THE F-8 AND THE EPROM IS CHECKED TO ENSURE IT HAS BEEN INITIALIZED BY ENTERING OPTION 'D'. THE 2716 CAN THEN BE PROGRAMMED AS FOLLOWS:

ENTER OPTION 'Q' WITHIN THE 'EPROM' PROGRAM
ENTER COMMAND 'LOAD FILENAME,10:1' ON THE F-8
ENTER COMMAND 'DUMP 0000-0255' ON THE F-8
ENTER COMMAND 'EPROM' ON THE F-8
ENTER OPTION 'P' WITHIN THE PROGRAM 'EPROM'
FOLLOW INSTUCTIONS IN 'EPROM' FOR CHANGING VOLTAGES

THIS LAST COMMAND PLACES A COPY OF THE MEOSC SOURCE CODE ON THE EPROM STARTING AT LOCATION 0000, WHICH IS WHERE PROGRAM EXECUTION BEGINS USING THE MK38P70. THE 2716 EPROM CAN THEN BE PLACED ON THE MK38P70, AND IF THE PROGRAM IS CORRECT, THE CONTROLLER WILL OPERATE.

IT MUST BE NOTED THAT THESE COMMANDS TO CREATE NEW COPIES OF THE OPERATING PROGRAMS MUST BE EXECUTED IMMEDIATELY FOLLOWING THE LINKING OPERATION SINCE SOME OF THE OTHER FDOS PROGRAMS (LIKE THE ASSEMBLER AND THE EDITOR) OBSCURE THE LOWER ADDRESSES OF THE MEMORY WHERE THE SCANNER PROGRAMS ARE LOADED.

ON THIS DISK ARE FILES DESIGNATED FILENAME,30:1 WHICH ARE AUTOMATIC LOAD-AND-EXECUTE FILES WHICH CAN BE COPIED TO A DISK IN DRIVE 0 FOR IMMEDIATE USE. A PREASSEMBLED MEOSC,10:1 FILE IS ALSO PRESENT WHICH CAN BE LOADED DIRECTLY INTO AN EPROM.

FOR FURTHER INFORMATION CONCERNING THE OPERATION OF THE F8 AND ITS OPERATING SYSTEM FDOS, CONSULT THE USERS MANUALS SUPPLIED WITH THE SYSTEM.

```
MAIN4    RORG   0
*
         TITLE 'MAIN CALLING PROGRAM-VERSN 4'
*
* REVISED FOR THE MK38P70 CONTROLLER PROGRAM
* MEOSC BY CPT ED SHAFFER, JULY 1983.
* WRITTEN AND EDITED BY CPT B.J. STANTON.
* THIS IS THE MAIN CALLING PROGRAM FOR THE
* ELECTRO-OPTICAL PAGE SCANNER.  IT MUST BE
* LINKED FIRST WHEN BUILDING THE SOFTWARE
* PACKAGE  'MEOSC'.
*
* THE USE OF THE SCANNER CONTROL PANEL SENSE
* SWITCHES, FROM RIGHT TO LEFT:
*
* #        DOWN                    UP
*-----------------------------------------
* 1    NORMAL PAGE              INFINITE LINES
* 2    AUTOMATIC THRESHOLD      THRESHOLD FREEZE
* 3    SOFT COPY                HARD COPY
*-----------------------------------------
*
*
LINEU    EQU    6          LINE CNTR HIGH BYTE
LINEL    EQU    164        LINE CNTR LOW BYTE
*
* CODES FOR THE 3-TO-8 DECODER ON I/O BOARD 4:
*
ENCMD    EQU    H'00'      CODE FOR CMD CHANNEL
ENCCD    EQU    H'20'      CCD CHANNEL CMS
ENSENS   EQU    H'40'      CONN INP SW TO PRT4
*
* DISPLAY ADDRESSES FOR I/O BOARD 5:
*
ADHARD   EQU    H'01'      ADDRESS OF PRINTER
ADSOFT   EQU    H'08'      ADDR OF TEK. DISPL
*
* DISPLAY CONTROL FOR I/O BOARD 5:
*
LDADDR   EQU    H'80'      ADDR LOAD CODE
*
* DISPLAY COMMANDS SENT THRU I/O BOARD 5:
*
HARDLMJ  EQU    H'0B'      LEFT MARG JUSTIFY
HARDFIL  EQU    H'00'      FILL,PRT LINE BUFF
HARDADV  EQU    H'03'      ADVANCE ONE LINE
HARDCUT  EQU    H'0F'      CUT PAPER
HARDOFF  EQU    H'37'      SHUT OFF PTR (PUMPS)
SOFTEN   EQU    H'06'      ENBLE SOFTCOPY DISPL
SOFTDSB  EQU    H'03'      DSBL SOFTCOPY DISPL
SOFTERS  EQU    H'01'      ERASE SOFTCOPY DISPL
SOFTRSY  EQU    H'02'      RESET Y COUNTER
SOFTINY  EQU    H'04'      INCREMENT Y COUNTER
*
*
* LINKING INFO
```

```
          EXTRN ENDLN,FSTLN,XMITS,QSET
*
*
*
          DI                  DISABLE INTERRUPTS
          LI     H'00'
          OUTS   4           INITIALIZE PORTS
          OUTS   0
          OUTS   5
          LI     H'54'       SET 8255 #1
          OUTS   4
          LI     H'7C'
          OUTS   0
          LI     H'50'
          OUTS   4
          LI     H'64'       SET 8255 #2
          OUTS   4
          LI     H'6E'
          OUTS   5
          LI     H'60'
          OUTS   4
          LI     H'57'       SET OUTPUT PORTS HI
          OUTS   4           PORT 8 (1A)
          LI     H'00'
          OUTS   0
          LI     H'53'
          OUTS   4
          LI     H'55'       PORT 5 (1C UP)
          OUTS   4
          LI     H'51'
          OUTS   4
          LI     H'66'       PORT 12 (2B)
          OUTS   4
          LI     H'C0'
          OUTS   5
          LI     H'62'
          OUTS   4
          LI     H'65'       PORT 13 (2C)
          OUTS   4
          LI     H'61'
          OUTS   4
          LI     H'10'       RESET INTERFACE
          OUTS   1
          CLR
          OUTS   1
OVER      LI     ENCMD            SET FOR CML XMIT
          OUTS   0
          LI     H'55'
          OUTS   4
          LI     H'51'
          OUTS   4
*
*----------------------DATA CHANNEL CLOSED
*
BEGIN     LI     ENSENS      ENABLE SCANNER INPUT
```

```
          OUTS   0
          LI     H'55'
          OUTS   4
          LI     H'51'
          OUTS   4
          CLR
          OUTS   0
          LI     H'59'          LOOP TILL
          OUTS   4              INIT = 0
          INS    0
          NI     H'02'          INIT = BIT 2
          BNZ    BEGIN
*
SKIPM     CLR                   LOOP TILL
          OUTS   0              INIT = 1
          LI     H'59'
          OUTS   4
          INS    0
          NI     H'02'          INIT = BIT 2
          BZ     SKIPM
*
*****DELAY LOOP*****
*
          CLR                   WAIT 2.3 MS
DLI       INC
          BNZ    DLI
*
*****END DELAY******
*
          CLR
          OUTS   0
          LI     H'59'          CHECK START AGAIN
          OUTS   4
          INS    0
          NI     H'02'
          BZ     SKIPM
*
          CLR                   GET F8 SENSE 7
          OUTS   5              FOR HARD/SOFT OUTPUT
          LI     H'69'
          OUTS   4
          INS    5
          SL     4
          NI     H'80'
          LR     8,A
*
          LR     A,8            USE REG8 FOR HDR/SFT
          CI     H'00'
          BZ     SOFT
*
HARD      LI     ADHARD         SETUP FOR PRINTER
          OUTS   0
          LI     H'57'
          OUTS   4
          LI     H'53'
          OUTS   4
```

```
          LI    H'80'       STORE PRINTER ADDR
          OUTS  1
          CLR
          OUTS  1
          LI    HARDLMJ     START PUMPS IN PRTR
          LR    9,A
          PI    XMITS
          BR    SKIP1
*
SOFT      LI    ADSOFT      SETUP FOR TEK-DISPL
          OUTS  0
          LI    H'57'
          OUTS  4
          LI    H'53'
          OUTS  4
          LI    LDADDR      STORE TEK ADDR
          OUTS  1
          CLR
          OUTS  1
          LI    SOFTRSY     INITIALIZE TEK-DISPL
          LR    9,A
          PI    XMITS
          LI    SOFTERS     ERASE SCREEN
          LR    9,A
          PI    XMITS
*
*****DELAY LOOPS******************
*
SKIP1     LI    D'250'      DELAY FOR PUMPS OR
          LR    2,A           SCREEN ERASE
LOOP0     LI    D'200'
          LR    3,A
LOOP1     DS    3
          BNZ   LOOP1
          DS    2
          BNZ   LOOP0
*
*****END DELAY***************
*
          PI    FSTLN       WAIT FOR FIRST LINE
*
* CHECK FOR AUTO THRESHOLD DISABLE----------
*
          CLR
          OUTS  5
          LI    H'69'
          OUTS  4
          INS   5
          SL    4
          NI    H'40'
          BNZ   FRZ
*
*****
* BEGIN AUTOMATIC THRESHOLD SETTING SEQUENCE
*****
          CLR               MAX DIGITAL VIDEO
```

```
         LR     6,A         (MTC) INITIALIZED
         LR     7,A         TO ZERO
*
*  INITIALIZE FOR THRESHOLD SAMPLING----------
*
*###############      NOTE!!!   ################
*
*  AS IT STANDS NOW, QSET IS INITIALIZED TO
*  SAMPLE THE RANGE 128 TO 640 WITH AN
*  INITIAL STEP SIZE OF 64 AS DOCUMENTED FOR
*  THE SOFTWARE PACKAGE, 'EOPS2'.
*
*  TO SAMPLE THE ENTIRE RANGE OF N (0 TO 1024),
*  SCRATCH REGISTER 5 MUST BE LOADED WITH ZERO,
*  AND SCRATCH REGISTER 3 MUST BE LOADED WITH
*  128.
*
*###############################################
*
*
         LR     4,A         THRESHOLD SET TO
         LI     128         START AT 128
         LR     5,A
         LI     64          STEP SIZE INITIALIZED
         LR     3,A         TO 64
*
* TAKE FOUR PASSES (AT 7 LINES PER PASS)-------
*
         PI     QSET
         PI     QSET
         PI     QSET
         PI     QSET
*
* LOAD OPTIMUM THRESHOLD---------------------
*
         LR     A,QU
         SL     4
         OUTS   5
         LI     H'65'
         OUTS   4
         LI     H'61'
         OUTS   4
         LR     A,QL
         OUTS   5
         LI     H'66'
         OUTS   4
         LI     H'62'
         OUTS   4
*
FRZ      LI     LINEU       INITIALIZE LINE CTR
         LR     0,A         SO IS HIGH BYTE
         LI     LINEL
         LR     1,A         S1 IS LOW BYTE
*
         LI     ENCMD       OPEN UP CMD CHANNEL
         OUTS   0
```

```
          LI     H'55'
          OUTS   4
          LI     H'51'
          OUTS   4
NEWLN     LR     A,8
          CI     H'00'
*
          BZ     NLSOFT
*
NLHARD    LI     HARDLMJ    SEND LMJ
          LR     9,A
          PI     XMITS
*
*****DELAY******
*
          LI     254        WAIT 18 US
DL1       INC
          BNZ    DL1
*
******END DELAY******
*
          LI     ENCCD      OPEN DATA CHAN
*------------------DATA CHANNEL OPEN
          OUTS   0
          LI     H'55'
          OUTS   4
          LI     H'51'
          OUTS   4
*
          PI     ENDLN      WAIT FOR END OF LINE
*
          LI     ENCMD      OPEN CMD CHANNEL
*----DATA CHANNEL CLOSED ----------------------
          OUTS   0
          LI     H'55'
          OUTS   4
          LI     H'51'
          OUTS   4
*
          LI     HARDFIL    SEND FILL CMD
          LR     9,A
          PI     XMITS
*
*****DELAY*******
*
          LI     240        WAIT 144 US
DL2       INC
          BNZ    DL2
*
*****END DELAY*****
*
          LI     HARDADV    ADVANCE PAPER
          LR     9,A
          PI     XMITS
*
******DELAY******
```

```
*         LI    254         WAIT 18 US
DL3       INC
          BNZ   DL3
*
******END DELAY*****
*
          JMP   ENDCHK      CHECK FOR LAST LINE
*
*
*
NLSOFT    LI    SOFTEN      ENABLE TEK DISPLAY
          LR    9,A
          PI    XMITS
*
******DELAY******
*
          LI    254         WAIT 18 US
DL4       INC
          BNZ   DL4
*
******END DELAY******
*
          LI    ENCCD       OPEN DATA CHAN
*--------------------DATA CHANNEL OPEN
          OUTS  0
          LI    H'55'
          OUTS  4
          LI    H'51'
          OUTS  4
*
          PI    ENDLN       WAIT FOR EOL SIG
*
          LI    ENCMD       OPEN CMD CHANNEL
*-------------------DATA CHANNEL CLOSED
          OUTS  0
          LI    H'55'
          OUTS  4
          LI    H'51'
          OUTS  4
*
          LI    SOFTDSB     DISABLE TEK-DISPLAY
          LR    9,A
          PI    XMITS
*
          LI    SOFTINY     SEND INCREMENT Y CMD
          LR    9,A
          PI    XMITS
*
******DELAY******
*
          LI    254         WAIT 18 US
DL5       INC
          BNZ   DL5
*
******END DELAY******
*
```

```
          JMP    ENDCHK
***********************************
ENDCHK    CLR               IF F8 SENSE 5
          OUTS   5          =1 THEN LOOP
          LI     H'69'
          OUTS   4
          INS    5          UNTIL F8 SENSE
          SL     4
          NI     H'20'      =0
          CI     H'00'
          BZ     NORMCNT
          LI     H'01'
          LR     1,A
          LI     H'00'
          LR     0,A
NORMCNT   LR     A,1
          AI     0          CHECK FOR LAST LINE
          BNZ    OK
          LR     A,0
          AI     0
          BZ     DONE
          DS     0
OK        DS     1
          JMP    NEWLN
DONE      LR     A,8
          CI     H'00'
          BZ     SKIPSOF
*
*PRINTER FINAL SECTION--------------------
*
          LI     HARDCUT    SEND CUT CMD
          LR     9,A
          PI     XMITS
*
********DELAY
*
          LI     246
CDL       INC               WAIT FOR CUT/
          BNZ    CDL
*
********END DELAY
*
          LI     HARDOFF    SEND PRINTER OFF CMD
          LR     9,A
          PI     XMITS
*
*
*
SKIPSOF   JMP    OVER       RUN PROGRAM AGAIN
*
*
*
          END
```

```
FSTLN    RORG  0
         TITLE 'FSTLN'
*
* WRITTEN BY RALPH L. VINCIGUERRA 12/80
* REVISED BY CPT ED SHAFFER 7/82 FOR
* USE IN MK38P70 CONTROLLER
*
* THIS IS A SUBR WHICH WAITS FOR THE
* SIGNAL CALLED PRINTLINE TO MAKE A
* RISING TRANSITION SIGNALLING THE
* END OF A SCAN LINE, AND TIME TO
* SEND COMMANDS.
* DUE TO AN INVERSION IN THE
* INTERFACE THE ACTUAL LINE IN THE
* SCANNER MAKES A FALLING TRANSITION.
*
*
ENSENS   EQU   H'40'
*
*
         LI    ENSENS     ENABLE SENSE INPUTS
         OUTS  0
         LI    H'55'
         OUTS  4
         LI    H'51'
         OUTS  4
*
LP1      CLR              LOOP UNTIL FALSE
         OUTS  0
         LI    H'59'
         OUTS  4
         INS   0
         SL    4
         SR    4
         NI    H'01'
         BNZ   LP1
LP2      CLR              LOOP UNTIL TRUE
         OUTS  0
         LI    H'59'
         OUTS  4
         INS   0
         SL    4
         SR    4
         NI    H'01'
         BZ    LP2
         POP
         END
```

```
ENDLN    RORG  0
         TITLE 'ENDLN'
*
* WRITTEN BY RALPH L. VINCIGUERRA 12/80
* REVISED BY CPT ED SHAFFER 7/83
* FOR USE IN MK38P70 CONTROLLER
*
* THIS IS A SUBR WHICH WAITS FOR THE
* SIGNAL CALLED PRINTLINE TO MAKE A
* RISING TRANSITION SIGNALLING THE
* END OF A SCAN LINE, AND TIME TO
* SEND COMMANDS.
* DUE TO AN INVERSION IN THE
* INTERFACE THE ACTUAL LINE IN THE
* SCANNER MAKES A FALLING TRANSITION.
*
*
* THIS SUBR ALSO WILL ONLY WAIT
* ABOUT 10MS FOR THE
* TRANSITION TO OCCUR. IF THE TRANSITION
* TAKES MORE THE LINE COUNTER IS SET
* THE THE END OF THE PAGE AND THE
* MAIN PROGRAM CONCLUDES.
*
ENSENS   EQU   H'40'
*
         LI    ENSENS     ENABLE SENSE INPUTS
         OUTS  0
         LI    H'55'
         OUTS  4
         LI    H'51'
         OUTS  4
*
         LI    D'255'
         LR    9,A        INITIALIZE CNT REG
*
LP1      CLR              LOOP UNTIL FALSE
         OUTS  0
         LI    H'59'
         OUTS  4
         INS   0
         SL    4
         SR    4
         NI    H'01'
         BZ    RDY
         DS    9
         BZ    DUMPOUT
         BR    LP1
*
RDY      LI    D'255'
         LR    9,A
LP2      CLR              LOOP UNTIL TRUE
         OUTS  0
         LI    H'59'
         OUTS  4
         INS   0
```

```
            SL      4
            SR      4
            NI      H'01'
            BNZ     GO
            DS      9
            BNZ     LP2
DUMPOUT     LI      L'0C'
            LR      0,A
            LR      1,A
GO          POP
            END
```

```
XMITS    RORG  0
*
         TITLE 'XMITS'
*
* WRITTEN BY RALPH L. VINCIGUERRA 12/80
* REVISED BY CPT ED SHAFFER 7/82 FOR
* USE IN MK38P70 CONTROLLER
*
* THIS SUBR IS USED TO SEND THE COMMANDS
* TO THE PRINTER OR THE TEK DISPLAY.
* IT EXPECTS THAT THE COMMAND CHANNEL
* HAS ALREADY BEEN OPENED ON BOARD 4
* AND THAT THE COMMAND TO BE SENT IS
* WAITING IN REGISTER 9 TO BE SENT TO
* BOARD 5.
*
         LR    A,9         PUT CMD ON BOARD 5
         OUTS  0
         LI    H'57'
         OUTS  4
         LI    H'53'
         OUTS  4
         LI    H'40'       LOAD CMD INTO LOGIC
         OUTS  1           ON BOARD 5
         CLR
         OUTS  1
         LI    H'20'       SEND SYNC PULSE
         OUTS  1
         OUTS  1
         CLR
         OUTS  1
         OUTS  1
*
         POP               POP RET ADDR
         END
```

```
QSET     RORG  0
         TITLE 'QUICK THRESHOLD SAMPLER,V6'
*
*  THIS IS THE NEXT GENERATION OF QSET
*  MODIFIED TO BE A RELOCATABLE MODULE.
*
*  INTENDED TO BE LINKED WITH THE MAIN
*  CALLING PROGRAM OF THE ELECTRO-OPTICAL
*  PAGE SCANNER.
*
*  INITIALIZING IS ACCOMPLISHED IN THE
*  MAIN CALLING PROGRAM.  STARTING VALUE
*  OF N AND STEP SIZE (SI) ARE DETERMINED
*  AT THAT TIME.
*
*  WRITTEN BY CAPT B.J. STANTON, 9 JUN 82
*  DEBUGGED FROM QSET3, 21 JUN 82
*  EDITED FROM QSET5, 21 JULY 82
*
*  REVISED BY CPT ED SHAFFER JUL 83
*  FOR USE IN MK38P70 CONTROLLER
*
VCRSET   EQU   H'80'      DIG VIDEO CNT RESET
CNT      EQU   2          SAMPLE PGM COUNTER
STEP     EQU   3          THRESHOLD STEP SIZE
NU       EQU   4          THRESHOLD HIGH BYTE
NL       EQU   5          THRESHOLD LOW  BYTE
MTCU     EQU   6          MAX DIG VIDEO HI BYT
MTCL     EQU   7          MAX DIG VIDEO LO BYT
MINU     EQU   10         MINUEND HIGH BYTE
MINL     EQU   11         MINUEND LOW  BYTE
ENSENS   EQU   H'40'
*
*
* ----------SUBROUTINE SAMPLE---------------
*
* THIS SUBROUTINE HAS PROVISIONS FOR A VAR-
* IABLE THRESHOLD STEP SIZE LOADED IN R3
* (STEP).  IT EXPECTS THE STARTING THRESHOLD
* VALUE TO BE LOADED IN R4,R5 (NU, NL)
*
         LIS   7          INITIALIZE
         LR    CNT,A      COUNTER
*
RVC      LI    H'FC'      RESET
         OUTS  5          VIDEO
         LI    H'64'      COUNTERS
         OUTS  4
         LI    H'60'
         OUTS  4
         LI    H'F1'
         OUTS  5
         LI    H'64'
         OUTS  4
         LI    H'60'
         OUTS  4
```

```
          LI     H'F0'
          OUTS   5
          LI     H'64'
          OUTS   4
          LI     H'60'
          OUTS   4
*
          LR     A,NL        INCREMENT
          AS     STEP        THRESHOLD N
          LR     NL,A        VALUE ONE
          OUTS   5
          LI     H'66'
          OUTS   4
          LI     H'62'
          OUTS   4
          LR     A,NU        STEP
          LNK
          LR     NU,A
          SL     4
          OUTS   5
          LI     H'65'
          OUTS   4
          LI     H'61'
          OUTS   4
*
* TEST FOR END OF PRINTLINE------------------
*
          LI     ENSENS
          OUTS   0
          LI     H'55'
          OUTS   4
          LI     H'51'
          OUTS   4
PL1       CLR                LOOP UNTIL FALSE
          OUTS   0
          LI     H'59'
          OUTS   4
          INS    0
          SL     4
          SR     4
          NI     H'01'
          BNZ    PL1
PL2       CLR                LOOP UNTIL TRUE
          OUTS   0
          LI     H'59'
          OUTS   4
          INS    0
          SL     4
          SR     4
          NI     H'01'
          BZ     PL2
*
* STORE NEW VTC IN SUBTRAHEND (K)------------
*
          CLR
          OUTS   5
```

```
         LI     H'6B'
         OUTS   4
         INS    5
         COM
         LR     KU,A
         CLR
         OUTS   0
         LI     H'5A'
         OUTS   4
         INS    0
         COM
         LR     KL,A
*
* LOAD MINUEND WITH MAX VTC (MTC)-----------
*
         LR     A,MTCU
         LR     MINU,A
         LR     A,MTCL
         LR     MINL,A
*
* SUBTRACT FOR SIGN OF RESULT---------------
*
         LR     A,KL        LOAD SUBLOW AND
         COM                COMPLEMENT
         AS     MINL        SUBLOW + MINLOW
         LR     MINL,A      STORE IN MINLOW
         LR     A,MINU      CARRY TO
         LNK                MINHI
         LR     MINU,A
         LR     A,MINL      ADD 1 TO MAKE
         INC                2'S COMPLEMENT
         LR     A,MINU      CARRY TO
         LNK                MINHI
         LR     MINU,A
         LR     A,KU        LOAD SUBHI AND
         COM                COMPLEMENT
         AS     MINU        SUBHI + MINHI
*
* END OF SUBTRACT FOR SIGN------------------
*
         BC     SKIP
         LR     A,KU        REPLACE MTC
         LR     MTCU,A      WITH NEW MAXIMUM
         LR     A,KL        VTC
         LR     MTCL,A
*
         LR     A,NU        STORE NEW
         LR     QU,A        THRESHOLD VALUE
         LR     A,NL        N GIVING MTC
         LR     QL,A
*
SKIP     DS     CNT
         BNZ    RVC
*
* END OF SUBROUTINE SAMPLE------------------
*
```

```
* DETERMINE STARTING VALUE OF NEW RANGE OF
* N TO BE SAMPLED
*
* SUBROUTINE SUBTRACT-----------------
* LOADS:
* MINUEND     IN R10, R11 (H)
* SUBTRAHEND  IN R12, R13 (K)
* RESULT      IN R10, R11 (K)
*
* FIRST LOAD VALUES-------------------
*
          LR     A,QU       LOAD
          LR     MINU,A     MINUEND
          LR     A,QL       IN
          LR     MINL,A     MINUEND
*
          LR     A,STEP     LOAD STEP
          LR     KL,A       IN
          CLR               SUBTRAHEND
          LR     KU,A
*
* THEN SUBTRACT-------------------------
*
          LR     A,KL       LOAD SUBLOW AND
          COM               COMPLEMENT
          AS     11         SUBLOW + MINLOW
          LR     11,A       STORE IN MINLOW
          BNC    SB1        IF CARRY THEN
          LR     A,10       INCREMENT
          INC               MINHI
          LR     10,A
*
SB1       LR     A,11       ADD 1 TO MAKE
          INC               2'S COMPLEMENT
          LR     11,A
          BNC    SB2        IF CARRY THEN
          LR     A,10       INCREMENT
          INC               MINHI
          LR     10,A
*
SB2       LR     A,KU       LOAD SUBHI AND
          COM               COMPLEMENT
          AS     10         SUBHI + MINHI
          LR     10,A       STORE IN MINHI
*
* FINALLY STORE NEW STARTING THRESHOLD-------
*
*
          LR     A,MINU
          LR     NU,A
          LR     A,MINL
          LR     NL,A
*
* ALTER STEP SIZE-----------------------------
*
          LR     A,STEP     DIVIDE STEP
```

```
          SR     1           SIZE BY 4
          SR     1
          LR     STEP,A
          POP
*
* END OF SUBROUTINE SAMPLE-----------------
*
          END
```

APPENDIX C

MANUFACTURER'S TECHNICAL DATA

This appendix contains technical data extracts of pertinent items and components used to implement the MK38P70 controller circuit and threshold adjust and display circuit. It is included for convenience to clarify the main text of this report and does not constitute a complete set of data. More detailed information is available in the manufacturers' publications.

MOSTEK

3870 SINGLE CHIP MICRO FAMILY

MK3870 and MK38P70

MK3870 FEATURES

- Available with 1K, 2K, 3K, or 4K bytes of mask programmable ROM memory
- 64 bytes scratchpad RAM
- Available with 64 bytes executable RAM
- 32 bits (4 ports) TTL compatible I/O
- Programmable binary timer
  - Interval timer mode
  - Pulse width measurement mode
  - Event counter mode
- External interrupt input
- Crystal, LC, RC, or external time base options
- Low power (275 mW typ.)
- Single +5 volt supply

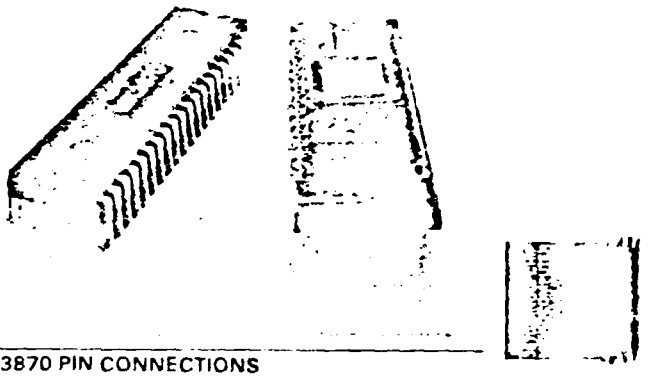
MK38P70 FEATURES

- EPROM version of MK3870
- Piggyback PROM (P-PROM)™ package
- Accepts 24 pin or 28 pin EPROM memories
- Identical pinout as MK3870
- In-Socket emulation of MK3870

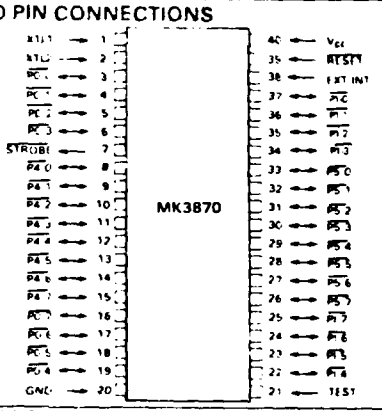
GENERAL DESCRIPTION

The MK3870 is a complete 8-bit microcomputer on a single MOS integrated circuit. The MK3870 can execute a set of more than 70 instructions, and is completely software compatible with the rest of the devices in the 3870 family. The MK3870 features 1-4K bytes of ROM and optional additional executable RAM depending on the specific part type designated by a slash number suffix. The MK3870 also features 64 bytes of scratchpad RAM, a programmable binary timer, and 32 bits of I/O.

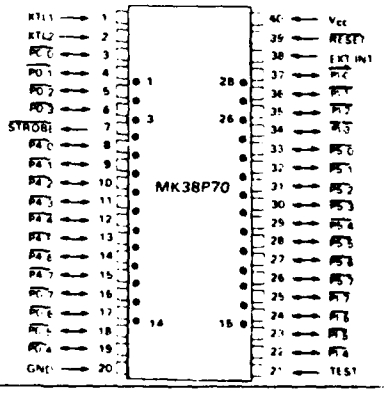
The programmable binary timer operates by itself in the interval timer mode or in conjunction with the external interrupt input in the pulse width measurement and the



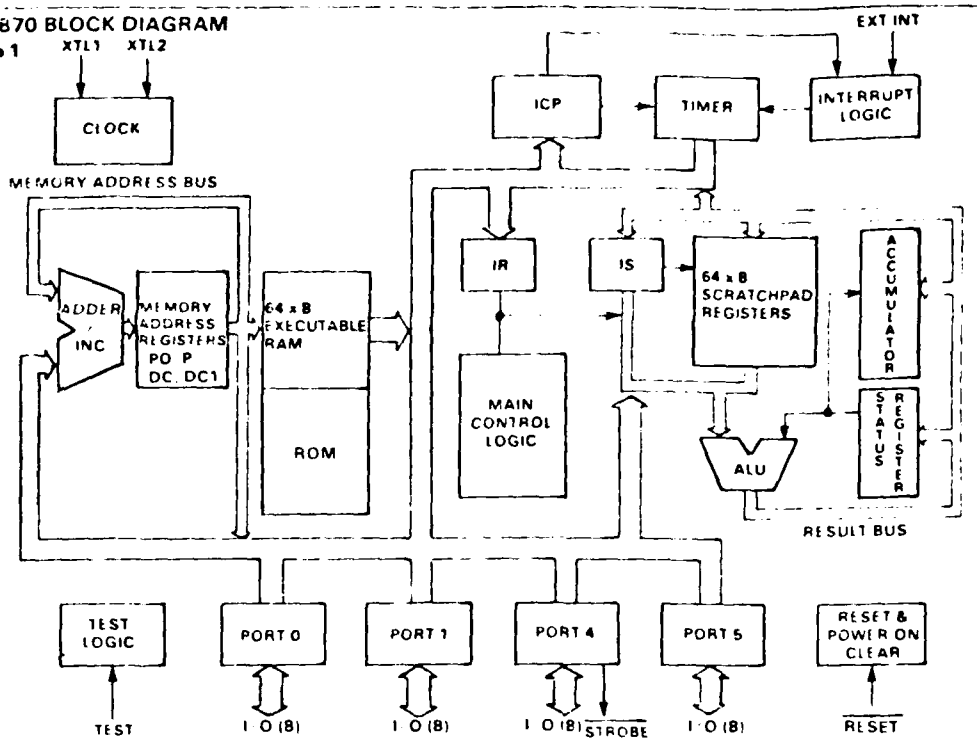
MK3870 PIN CONNECTIONS



MK38P70 PIN CONNECTIONS



MK3870 BLOCK DIAGRAM
Figure 1



event counter modes of operation. Two sources of vectored, prioritized interrupt are provided with the binary timer and the external interrupt input. The user has the option of specifying one of four clock sources for the MK3870 and MK38P70: Crystal, LC, RC, or external clock. In addition, the user can specify either a ±10% power supply tolerance or a ±5% power supply tolerance.

The MK38P70 microcomputer is the PROM based version of the MK3870. It is called the piggyback PROM (P-PROM)™ because of its packaging concept. This concept allows a standard 24-pin or 28 pin EPROM to be mounted directly on top of the microcomputer itself. The EPROM can be removed and reprogrammed as required with a standard PROM programmer. The MK38P70 retains exactly the same pinout and architectural features as other members of the 3870 family. The MK38P70 is discussed in more detail in a later section.

PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}0}$ -- $\overline{P0\text{-}7}$	I/O Port 0	Bidirectional
$\overline{P1\text{-}0}$ -- $\overline{P1\text{-}7}$	I/O Port 1	Bidirectional
$\overline{P4\text{-}0}$ -- $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ -- $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}0}$-- $\overline{P0\text{-}7}$, $\overline{P1\text{-}0}$-$\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$-$\overline{P4\text{-}7}$, and $\overline{P5\text{-}0}$-$\overline{P5\text{-}7}$ are 32 lines which can be individually used as either TTL compatible inputs or as latched outputs.

$\overline{STROBE}$ is a ready strobe associated with I/O Port 4. This pin, which is normally high, provides a single low pulse after valid data is present on the $\overline{P4\text{-}0}$-$\overline{P4\text{-}7}$ pins during an output instruction.

$\overline{RESET}$ may be used to externally reset the MK3870. When pulled low the MK3870 will reset. When then allowed to go high the MK3870 will begin program execution at program location H '000'.

EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.

XTL 1 and XTL 2 are the time base inputs to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering a mask ROM MK3870. The MK38P70 will operate with any of the four configurations.

TEST is an input, used only in testing the MK3870. For normal circuit functionality this pin may be left

unconnected, but it is recommended that TEST be grounded

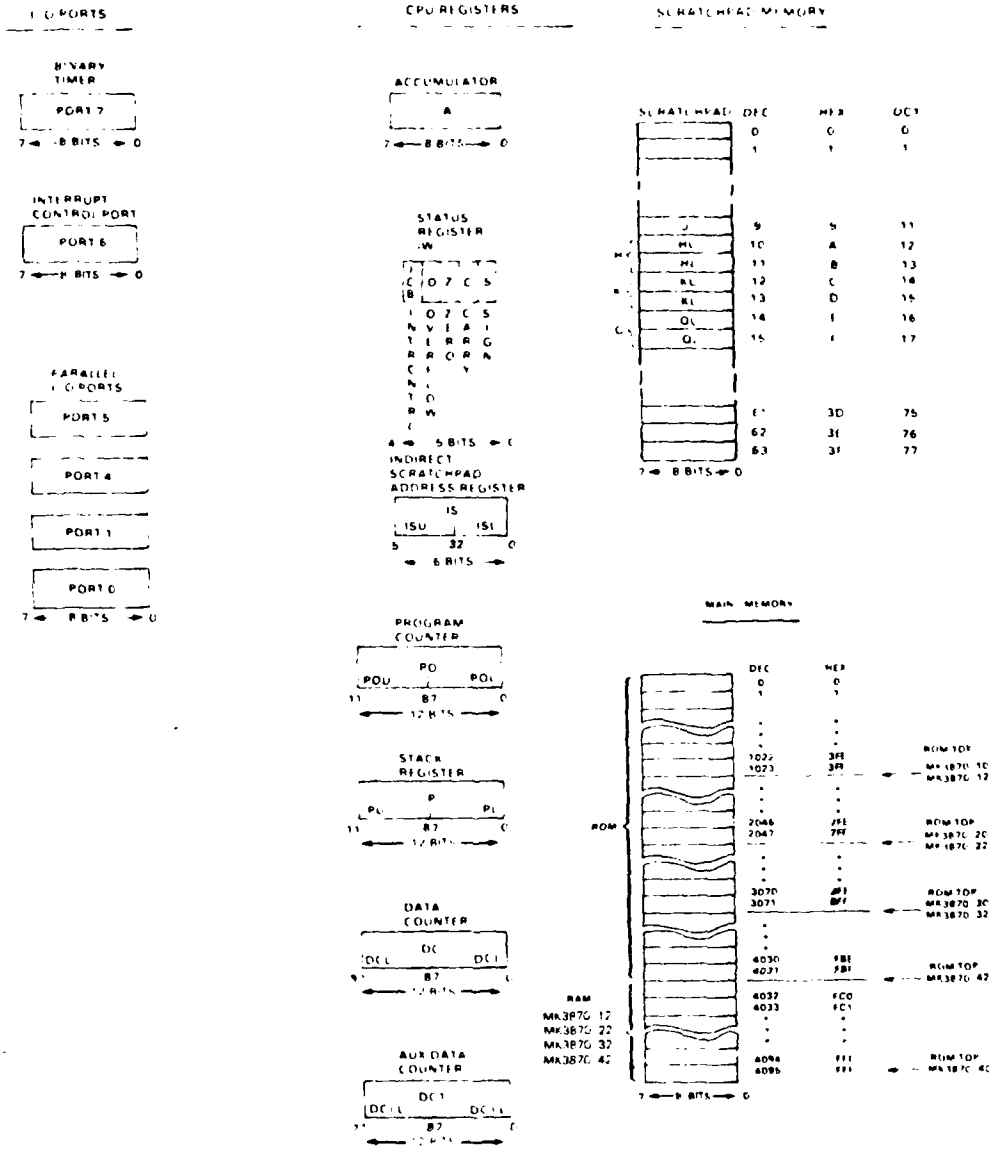
V_{CC} is the power supply input (single +5v)

MK3870 ARCHITECTURE

The basic functional elements of the MK3870 are shown in Figure 1. A programming model is shown in Figure 2. The architecture is common to all members of the 3870 family. All 3870 devices are instruction set compatible and differ only in amount and type of ROM, RAM, and I/O. The unique features of the MK3870 are discussed in the following sections. The user is referred to the *3870 Family Technical Manual* for a thorough discussion of the architecture, instruction set, and other features which are common to all 3870 family devices.

MK3870 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 2



MK3870 MAIN MEMORY

There are four address registers used to access main memory. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions or immediate operands. The Stack Register is used to save the contents of the Program Counter during an interrupt or subroutine call. Thus, the Stack Register contains the return address at which processing is to resume upon completion of the subroutine or interrupt routine. The Data Counter is used to address data tables. This register is auto-incrementing. Of the two data counters only Data Counter (DC), can access the ROM. However, the XDC instruction allows the Data Counter and Auxiliary Data Counter to be exchanged.

The graph in Figure 3 shows the amounts of ROM and executable RAM for every available slash number in the MK3870 pin configuration.

EXECUTABLE RAM

The upper bytes of the address space in some of the MK3870 devices is RAM memory. As with the ROM memory, the RAM may be addressed by the PO and the DC address registers. The executable RAM may be addressed by all MK3870 instructions which address Main Memory. Additionally, the MK3870 may execute an instruction sequence which resides in the executable RAM. Note this cannot be done with the scratchpad RAM memory, which is the reason the term "executable RAM" is given to this additional memory.

I/O PORTS

The MK3870 provides four, 8 bit bidirectional Input/Output ports. These are ports 0, 1, 4, 5. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pin are covered in the 3870 Family Technical Manual. The schematic of an I/O pin and available output drive options are shown in Figure 4.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MK3870 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. $\overline{\text{STROBE}}$ may also be used as an input strobe to Port 4 after completing the input operation.

MK38P70 GENERAL DESCRIPTION

The MK38P70 is the EPROM version of the MK3870. It retains an identical pinout with the MK3870, which is documented in the section of this data sheet entitled "FUNCTIONAL PIN DESCRIPTION". The MK38P70 is housed in the "R" package which incorporates a 28 pin socket located directly on top of the package. A number of standard EPROMs may be plugged into this socket.

The MK38P70 can act as an emulator for the purpose of exact verification of user code prior to the ordering of mask ROM MK3870 devices. Thus, the MK38P70 eliminates the need for emulator board products. In addition, several MK38P70s can be used in prototype systems in order to test design concepts in field service before committing to high-volume production with mask ROM MK3870s. The compact size of the MK38P70 EPROM combination allows the packaging of such prototype systems to be the same as that used in production. Finally, in low-volume applications, the MK38P70 can be used as the actual production device.

Most of the material which has been presented for the MK3870 in this document applies to the MK38P70. This includes the description of the pin configuration, architecture, programming model and I/O ports. Additional information is presented in the following sections.

MK38P70 MAIN MEMORY

As can be seen from the block diagram in Figure 5, the MK38P70 contains executable RAM in the main memory map. The MK38P70 contains no on-chip ROM. Instead, the memory address lines are brought out to the 28 pin socket located directly on top of the 40 pin package, so the external EPROM memory is addressed as main memory.

There is one memory version of the [redacted] and it is designated as the MK38P70/02 [redacted]8P70/02 contains 64 bytes of on-chip exec[redacted]AM. The MK38P70/02 can emulate the followi[redacted]ces:

MK3870/10
MK3870/12
MK3870/20
MK3870/22
MK3870/30
MK3870/32
MK3870/42

MK38P70
Figure 5

MEM

The MK38F
because o
mapped int
space. The
locations

Addressing
accomplis
Figure 6 f
register siz

MK38P70

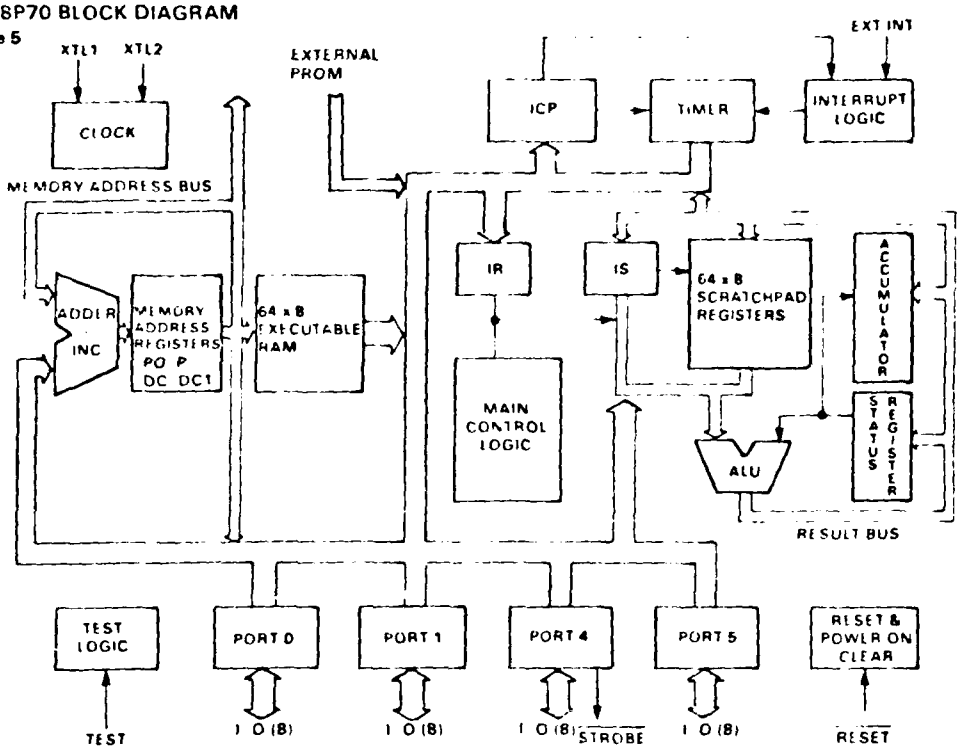
A 28 pin EF
"R" packag
are shown
the 28 pin s
memory de
memory sh

The 28 pir
24 pin ar
differences
by providir

Initially th
is availabl
28 pin me

MK38P70 BLOCK DIAGRAM

Figure 5



The MK38P70 02 cannot exactly emulate the MK3870 40 because of the 64 bytes of executable RAM which are mapped into the upper 64 bytes of addressable main memory space The MK3870/40 contains ROM memory in these locations

Addressing of main memory on the MK38P70 is accomplished in the same way as it is for the MK3870 See Figure 6 for main memory addresses and for address register size in the MK38P70

MK38P70 EPROM SOCKET

A 28 pin EPROM socket is located on top of the MK38P70 "R" package The socket and compatible EPROM memories are shown in Figure 7 When 24 pin memories are used in the 28 pin socket, they should be inserted so that pin 1 of the memory device is plugged into pin 3 of the socket (the 24 pin memory should be lower justified in the 28-pin socket)

The 28-pin socket has been provided to allow use of both 24-pin and 28-pin memory devices Minor pin-out differences in the memory devices must be accommodated by providing different versions of the MK38P70

Initially, the MK38P70 that is compatible with the MK2716 is available The MK38P70 designed to accomodate the 28-pin memory devices will be available at a later date

MK38P70 I/O PORTS

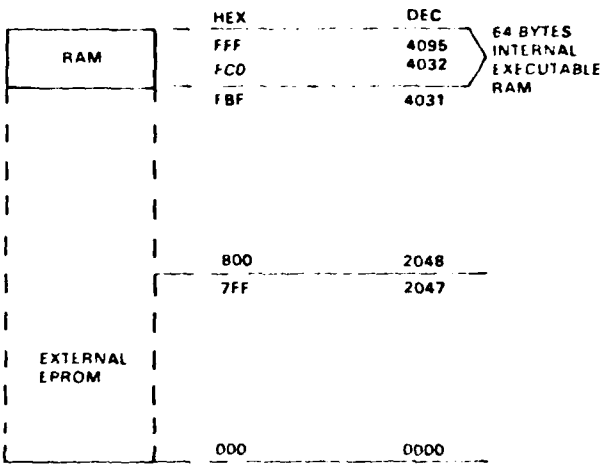
The MK38P70 is offered with two types of output buffer options on Ports 4 and 5. These are the open drain output buffer and the standard output buffer which are pictured in Figure 4 The open drain version of the MK38P70 is provided so that user-selected open drain port pins on the MK3870 can be emulated prior to ordering those mask ROM devices Figure 7 lists which version(s) of the MK38P70 has open drain output buffers and which has standard output buffers in parentheses following the specified MK38P70 part ordering number (MK97XXX).

MEMORY ACCESS TIMING

A timing diagram depicting the memory access timing of the MK38P70 is shown in the next table The Φ clock signal is derived internally in the MK38P70 by dividing the time base frequency by two and is used to establish all timing frequencies The WRITE signal is another internal signal to the MK38P70 which corresponds to a machine cycle, during which time a memory access may be performed Each machine cycle is either 4 Φ clock periods or 6 Φ clock periods long These machine cycles are termed short cycles and long cycles, respectively The worst case memory cycle is the short cycle, during which time an op code fetch is performed This is the cycle which is pictured in the timing

MK38P70 MAIN MEMORY MAP

Figure 6



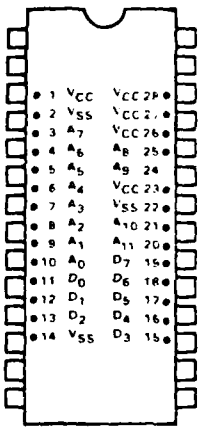
MK38P70 02

Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK38P70/02	64 bytes	12 bits	0 bytes	64 bytes

diagram. After a delay from the falling edge of the WRITE clock, the address lines become stable. Data must be valid at the data out lines of the PROM for a setup time prior to the next falling edge of the WRITE pulse. The total access time available for the MK38P70 version is shown as t_{aas} or the time when address is stable until data must be valid on the data bus lines. The equation for calculating available memory access time along with some calculated access times based on the listed time base frequencies is shown in Figure 8.

MK38P70 "R" PACKAGE SOCKET PINOUT

Figure 7



MK97400 (Standard Outputs) Compatible Memories	MK97410 (Open Drain) Compatible Memories
2758	2758
MK2716	MK2716
2516	2516
2532	2532

ELECTRICAL SPECIFICATIONS
MK3870, MK38P70

OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temprature T_A
-00	+5V ± 10%	0°C - 70°C
-05	+5V ± 5%	0°C - 70°C
-10	+5V ± 10%	-40°C - +85°C
-15	+5V ± 5%	-40°C - +85°C

See Ordering Information for explanation of part numbers

ABSOLUTE MAXIMUM RATINGS*

	-00, -05	-10, -15
Temperature Under Bias	-20°C to +85°C	-50°C to +100°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0V to +7V	-1.0V to +7V
Voltage on TEST with Respect to Ground	-1.0V to +9V	-1.0V to +9V
Voltage on Open Drain Pins With Respect to Ground	-1.0V to +13.5V	-1.0V to +13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin	60mW	60mW
Power Dissipation by all I/O pins	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS
T_A, V_{CC} within specified operating range
I/O power dissipation ≤ 100mW (Note 2)

SIGNAL	SYM	PARAMETER	-00,-05 MIN	-00,-05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
XTL1 XTL2	t_ϕ	Time Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_\phi$		$2t_\phi$			
WRITE	t_W	Internal WRITE Clock period	$4t\Phi$ $6t\Phi$		$4t\Phi$ $6t\Phi$			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
STROBE	$t_{I/O-s}$	Output valid to STROBE delay	$3t\Phi$ -1000	$3t\Phi$ +250	$3t\Phi$ -1200	$3t\Phi$ +300	ns	I/O load = 50pF + 1 TTL load
	t_{sL}	STROBE low time	$8t\Phi$ -250	$12t\Phi$ +250	$8t\Phi$ -300	$12t\Phi$ +300	ns	STROBE load 50pF + 3TTL loads
RESET	t_{RH}	RESET hold time, low	$6t\Phi$ -750		$6t\Phi$ -1000		ns	
	t_{RPOC}	RESET hold time, low for power clear	[illegible]		[illegible]		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	$6t\Phi$ -750		$6t\Phi$ -1000		ns	To trigger interrupt
			$2t\Phi$		$2t\Phi$		ns	To trigger timer

AC CHARACTERISTICS FOR MK38P70

(Signals brought out at socket)
T_A V_{CC} within specified operating range
I/O Power Dissipation < 100 mW (Note 2)

SYMBOL	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	CONDITION
t_{acc}*	Access time from Address A_{11} A_0 stable until data must be valid at D_7 D_0	650		650		ns	ϕ 2.0 MHz

*See Table in Figure 8

CAPACITANCE

T_A = 25°C
All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance		10	pF	Unmeasured Pins Grounded
C_{XTL}	Input capacitance XTL1 XTL2	2.5	2.5	pF	

DC CHARACTERISTICS

T_A V_{CC} within specified operating range
I/O power dissipation < 100mW (Note 2)

SYMBOL	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	DEVICE
I_{CC}	Average Power Supply Current		85		110	mA	MK3870/10 Outputs Open
			94		125	mA	MK3870/12 Outputs Open
			85		110	mA	MK3870/20 Outputs Open
			94		125	mA	MK3870/22 Outputs Open
			100		130	mA	MK3870/30 Outputs Open
			100		130	mA	MK3870/32 Outputs Open
			100		130	mA	MK3870/40 Outputs Open
			100		130	mA	MK3870/42 Outputs Open

DC CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	DEVICE
I_{CC}	Average Power Supply Current		125		150	mA	MK38P70/02 No EPROM, Outputs Open
P_D	Power Dissipation		400		525	mW	MK3870-10 Outputs Open
			440		575	mW	MK3870/12 Outputs Open
			400		525	mW	MK3870/20 Outputs Open
			440		575	mW	MK3870/22 Outputs Open
			475		620	mW	MK3870/30 Outputs Open
			475		620	mW	MK3870/32 Outputs Open
			475		620	mW	MK3870/40 Outputs Open
			475		620	mW	MK3870/42 Outputs Open
			600		750	mW	MK38P70/02 No EPROM, Outputs Open

DC C
T_A, V_C

SYM
V_{IHE}
$V_{IL E}$
I_{IHE}
$I_{IL EX}$
V_{IHI}
V_{IHF}
V_{IHE}
V_{IL}
I_{IL}
I_L
I_{OH}
I_{OH}
I_{OH}
I_{OL}
I_{OL}

DC CHARACTERISTICS (cont.)

T_A, V_{CC} within specified operating range, I/O power dissipation = 100mW (Note 2)

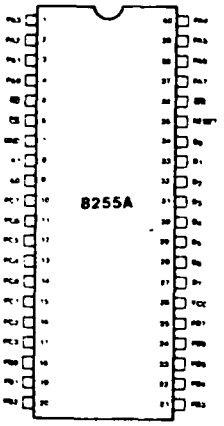
SYM	PARAMETER	-00,-05 MIN	-00,-05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	CONDITIONS
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	V_{IHEX} V_{CC}
I_{ILEX}	External Clock input low current		-100		-130	μA	V_{ILEX} V_{SS}
$V_{IHI/O}$	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard pull-up
		2.0	13.2	2.0	13.2	V	Open drain (1)
V_{IHR}	Input high level, $\overline{RESET}$	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IL}	Input low level	-.3	.8	-.3	.7	V	(1)
I_{IL}	Input low current, all pins with standard pull-up resistor		-1.6		-1.9	mA	V_{IN}=0.4V
I_L	Input leakage current, open drain pins, and inputs with no pull-up resistor		+10 -5		+18 -8	μA μA	V_{IN}=13.2V V_{IN}=0.0V
I_{OH}	Output high current pins with standard pull-up resistor	-100 -30		-89 -25		μA μA	V_{OH}=2.4V V_{OH}=3.9V
I_{OHDD}	Output high current, direct drive pins	-100 -1.5	 -8.5	-80 -1.3	 -11	μA mA mA	V_{OH}=2.4V V_{OH}=1.5V V_{OH}=0.7V
I_{OHS}	$\overline{STROBE}$ Output High current	-300		-270		μA	V_{OH} = 2.4V
I_{OL}	Output low current	1.8		1.65		mA	V_{OL}=0.4V
I_{OLS}	$\overline{STROBE}$ Output Low current	5.0		4.5		mA	V_{OL}=0.4V

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

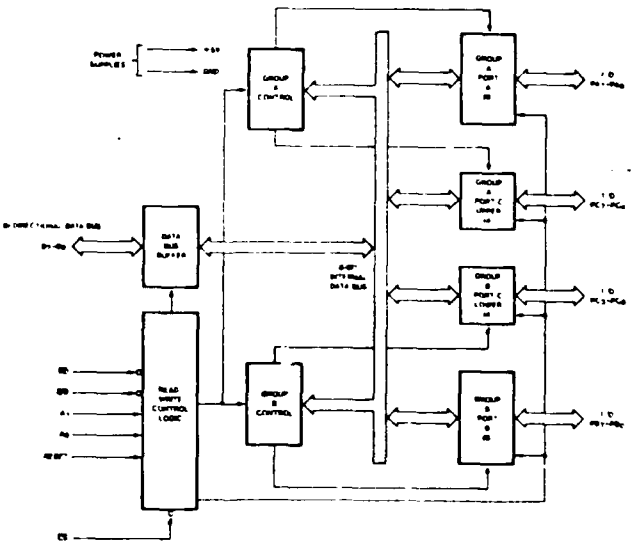
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255A BLOCK DIAGRAM



5A FUNCTIONAL DESCRIPTION

eral

3255A is a programmable peripheral interface (PPI) e designed for use in Intel® microcomputer ms. Its function is that of a general purpose I/O ponent to interface peripheral equipment to the ocomputer system bus. The functional configura- of the 8255A is programmed by the system software hat normally no external logic is necessary to inter- peripheral devices or structures.

Bus Buffer

3-state bidirectional 8-bit buffer is used to interface 3255A to the system data bus. Data is transmitted or ived by the buffer upon execution of input or output ructions by the CPU. Control words and status infor- ion are also transferred through the data bus buffer.

d/Write and Control Logic

function of this block is to manage all of the internal external transfers of both Data and Control or Status ds. It accepts inputs from the CPU Address and Con- busses and in turn, issues commands to both of the trol Groups.

)

p Select. A "low" on this input pin enables the com- niction between the 8255A and the CPU.

(RD)

Read. A "low" on this input pin enables the CPU to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to read from the 8255A.

(WR)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS → 3-STATE

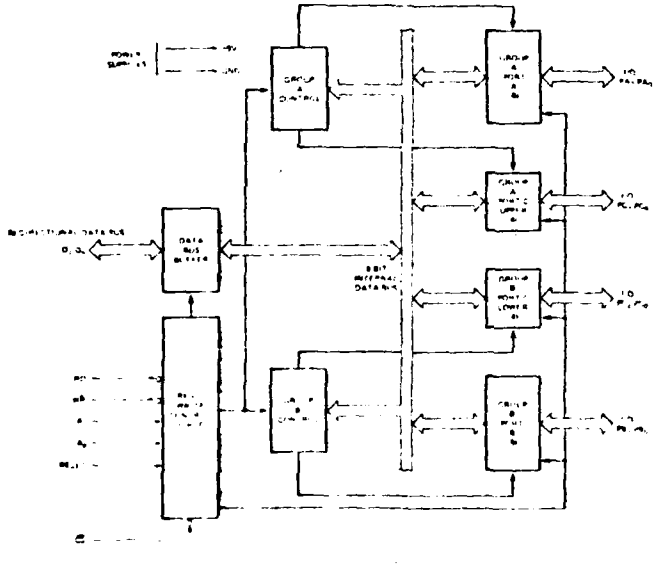


Figure 1. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

00744A

A and Group B Controls

functional configuration of e by the systems software. In e a control word to the 8255A. information such as "mode" that initializes the functiona

the Control blocks (Group A commands" from the Read/Write words" from the internal commands to its associated p

Group A – Port A and P Group B – Port B and Po

Control Word Register can On operation of the Control Wo

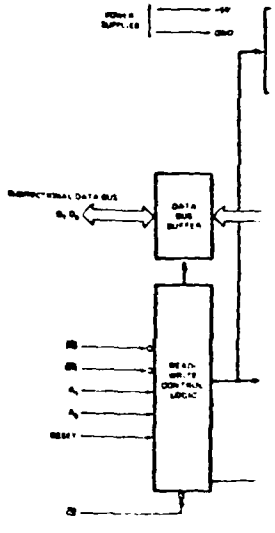


Figure 2. 8225A Block Diagram Group B Control Fun

8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel® microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communiction between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A – DATA BUS
0	1	0	1	0	PORT B – DATA BUS
1	0	0	1	0	PORT C – DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS – PORT A
0	1	1	0	0	DATA BUS – PORT B
1	0	1	0	0	DATA BUS – PORT C
1	1	1	0	0	DATA BUS – CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS – 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS – 3-STATE

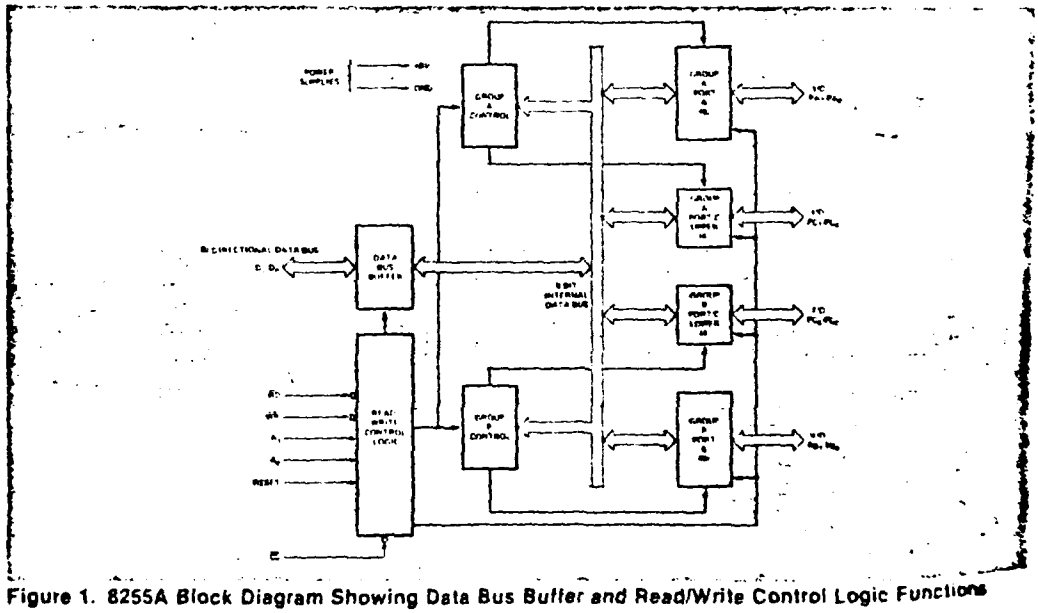


Figure 1. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

(RESET)

Reset. A "high on this input clears the control register and all ports (A, C, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

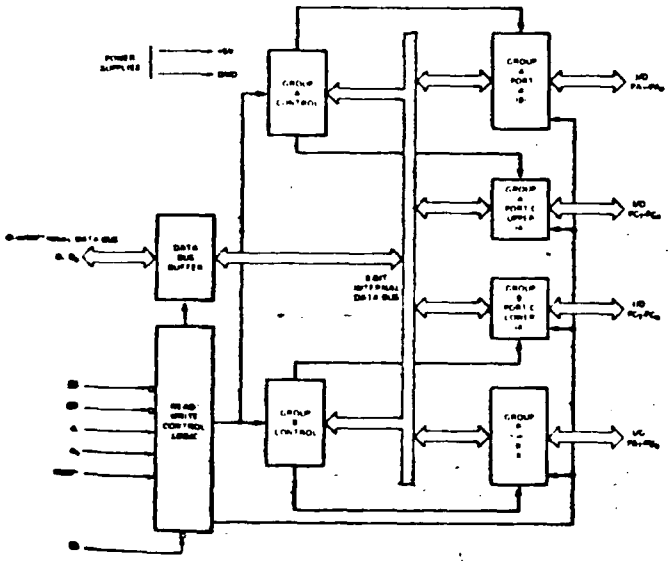
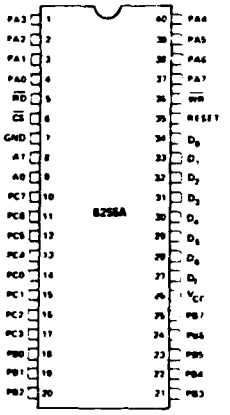


Figure 1. 8255A Block Diagram Showing Group A and Group B Control Functions

PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 - Basic Input/Output
Mode 1 - Strobed Input/Output
Mode 2 - Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

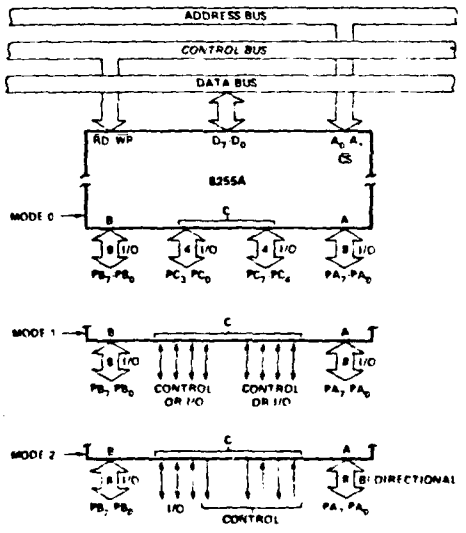


Figure 3. Basic Mode Definitions and Bus Interface

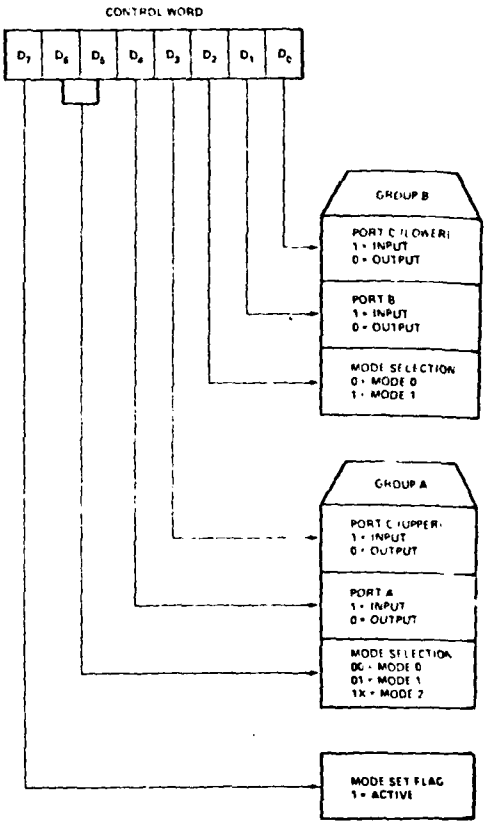


Figure 4. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

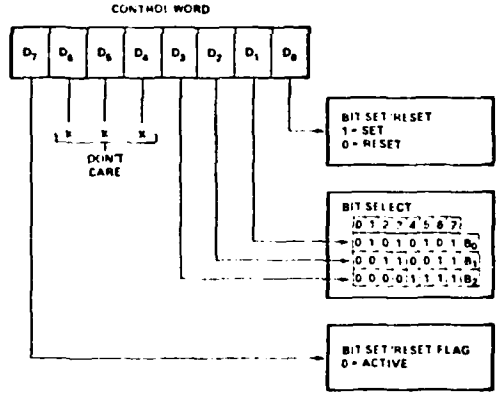


Figure 5. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) – INTE is SET – Interrupt enable
(BIT-RESET) – INTE is RESET – Interrupt disable

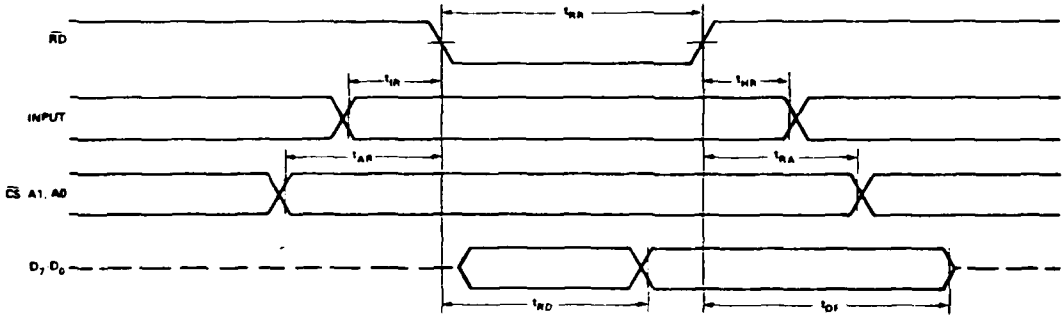
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

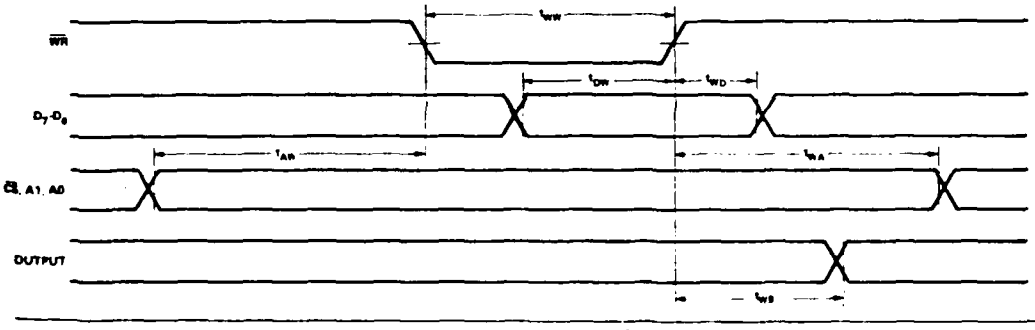
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



MODE 0 (Basic Input)



MODE 0 (Basic Output)

00744A

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, GND = 0V

NOTE:
The 8255A-5 specifications are not final. Some parametric limits are subject to change

Bus Parameters

Read:

SYMBOL	PARAMETER	8255A		8255A-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{AR}	Address Stable Before READ	0		0		ns
t_{RA}	Address Stable After READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid From READ[1]		250		200	ns
t_{DF}	Data Float After READ	10	150	10	100	ns
t_{RV}	Time Between READs and/or WRITEs	850		850		ns

Write:

SYMBOL	PARAMETER	8255A		8255A-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{AW}	Address Stable Before WRITE	0		0		ns
t_{WA}	Address Stable After WRITE	20		20		ns
t_{WW}	WRITE Pulse Width	400		300		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
t_{WD}	Data Valid After WRITE	30		30		ns

Other Timings:

SYMBOL	PARAMETER	8255A		8255A-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WB}	WR = 1 to Output[1]		350		350	ns
t_{IR}	Peripheral Data Before RD	0		0		ns
t_{HR}	Peripheral Data After RD	0		0		ns
t_{AK}	ACK Pulse Width	300		300		ns
t_{ST}	STB Pulse Width	500		500		ns
t_{PS}	Per. Data Before T.E. of STB	0		0		ns
t_{PH}	Per. Data After T.E. of STB	180		180		ns
t_{AD}	ACK = 0 to Output[1]		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	ns
t_{WOB}	WR = 1 to OBF = 0[1]		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1[1]		350		350	ns
t_{SIB}	STB = 0 to IBF = 1[1]		300		300	ns
t_{RIB}	RD = 1 to IBF = 0[1]		300		300	ns
t_{RIT}	RD = 0 to INTR = 0[1]		400		400	ns
t_{SIT}	STB = 1 to INTR = 1[1]		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1[1]		350		350	ns
t_{WIT}	WR = 0 to INTR = 0[1]		850		850	ns

Notes: 1. Test Conditions 8255A C_L = 100pF, 8255A-5 C_L = 150pF
2. Period of Reset pulse must be at least 50μs during or after power on. Subsequent Reset pulse can be 500 ns min.

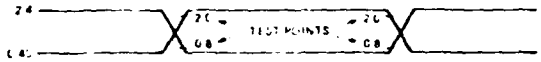


Figure 25. Input Waveforms for A.C. Tests

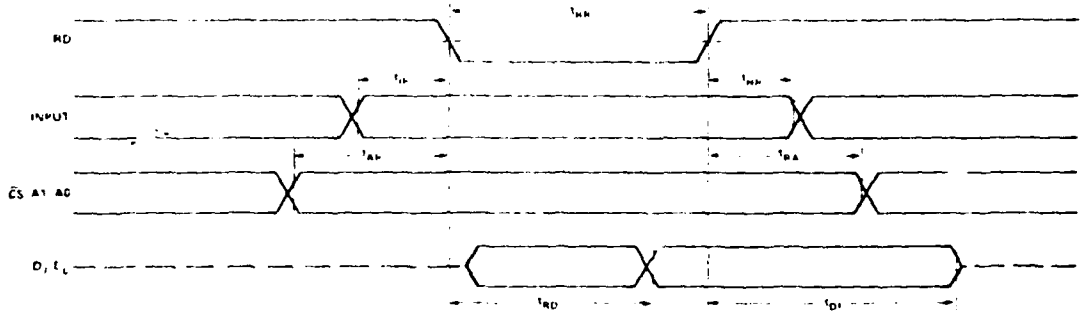


Figure 26. MODE 0 (Basic Input)

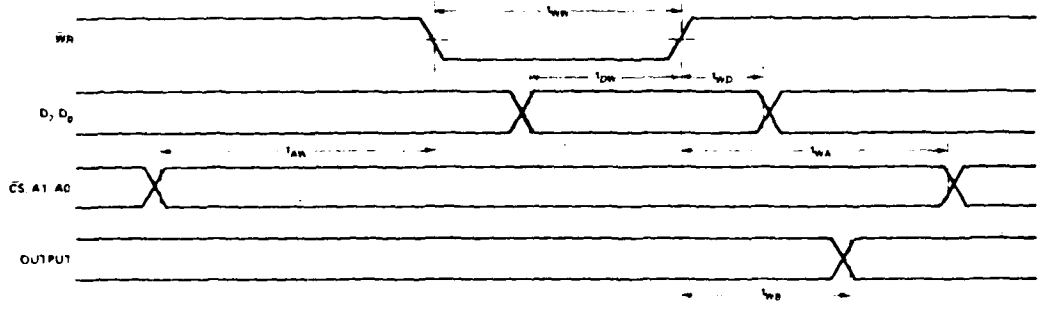


Figure 27. MODE 0 (Basic Output)

intel

2716
16K (2K x 8) UV ERASABLE PROM

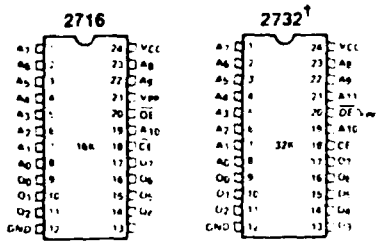
- Fast Access Time
  - 350 ns Max. 2716-1
  - 390 ns Max. 2716-2
  - 450 ns Max. 2716
  - 490 ns Max. 2716-5
  - 650 ns Max. 2716-6
- Single +5V Power Supply
- Low Power Dissipation
  - 525 mW Max. Active Power
  - 132 mW Max. Standby Power
- Pin Compatible to Intel® 2732 EPROM
- Simple Programming Requirements
  - Single Location Programming
  - Programs with One 50 ms Pulse
- Inputs and Outputs TTL Compatible during Read and Program
- Completely Static

The Intel® 2716 is a 16,384 bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5 volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. A selected 2716-5 and 2716-6 is available for slower speed applications. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



†Refer to 2732 data sheet for specifications

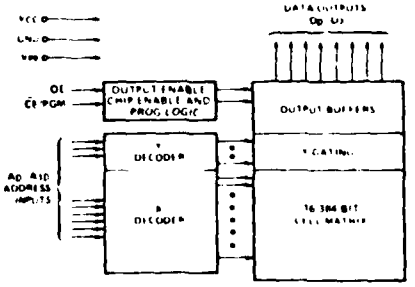
MODE SELECTION

MODE \ PINS	$\overline{CE}/PGM$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

PIN NAMES

A_0–A_{10}	ADDRESSES
$\overline{CE}/PGM$	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
All Input or Output Voltages with Respect to Ground . . . . . +6V to -0.3V
V_{PP} Supply Voltage with Respect to Ground During Program . . . . . +26.5V to -0.3V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Conditions During Read

	2716	2716-1	2716-2	2716-5	2716-6
Temperature Range	0°C – 70°C	0°C – 70°C	0°C – 70°C	0°C – 70°C	0°C – 70°C
V_{CC} Power Supply[1,2]	5V ±5%	5V ±10%	5V ±5%	5V ±5%	5V ±5%
V_{PP} Power Supply[2]	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

READ OPERATION

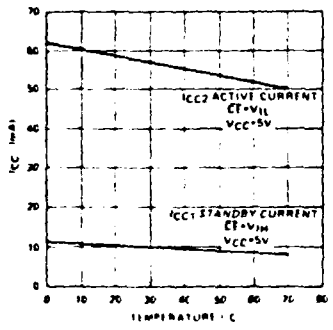
D.C. and Operating Characteristics

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[3]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.25V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

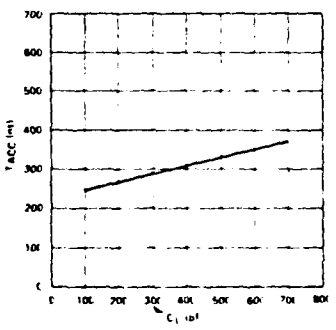
NOTES 1 V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2 V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3 Typical values are for T_A = 25°C and nominal supply voltages.
4 This parameter is only sampled and is not 100% tested.

Typical Characteristics

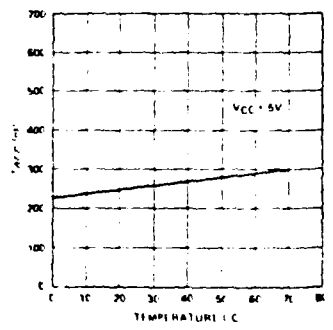
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



A.C. Characteristics

Symbol	Parameter	Limits (ns) 2716 Min.	2716 Max.	2716-1 Min.	2716-1 Max.	2716-2 Min.	2716-2 Max.	2716-5 Min.	2716-5 Max.	2716-6 Min.	2716-6 Max.	Test Conditions
t_{ACC}	Address to Output Delay		450		350		390		450		450	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		450		350		390		490		650	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay		120		120		120		160		200	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0	100	0	100	0	100	0	100	0	100	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

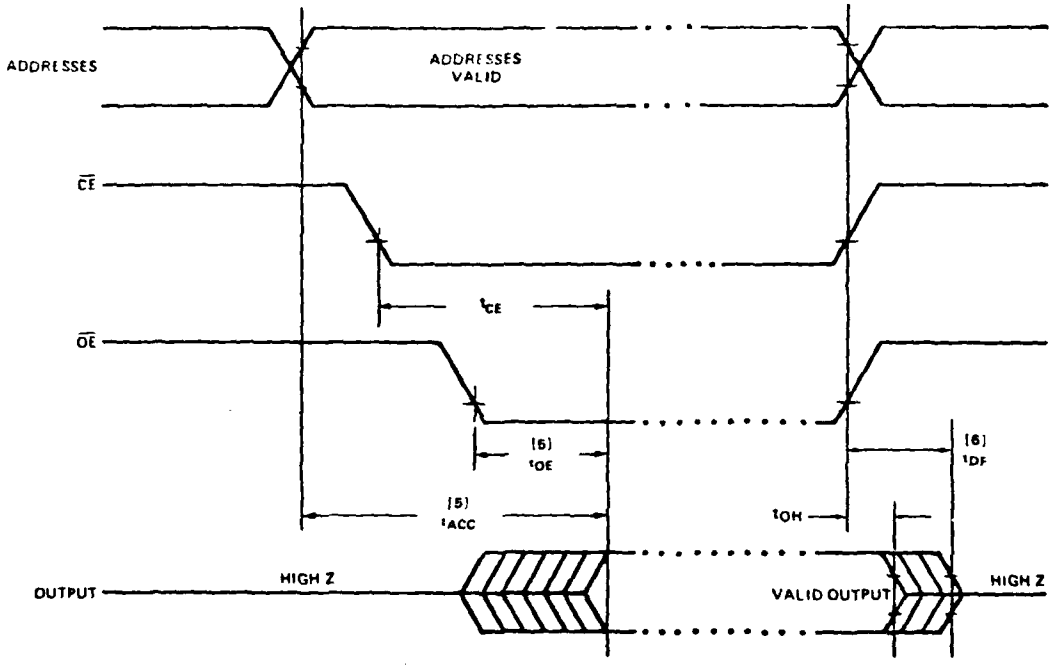
Capacitance [4] $T_A = 25°C$, $f = 1$ MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A. C. Waveforms [1]



NOTE
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. OE may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of CE without impact on t_{ACC}.
6. t_{DF} is specified from OE or CE, whichever occurs first.

ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog PROM/ROM Programming Instruction Section) for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2716 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

TABLE I. MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedence state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because 2716's are usually used in larger memory arrays, Intel has provided a 2 line control function that accomodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time – either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled 2716s.

PROGRAM INHIBIT

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that 2716. A low level $\overline{CE}$/PGM input inhibits the other 2716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

intel

- Fast Acce
  - 450 ns
  - 550 ns
- Single +5
- Output Er
  MCS-86™
- Low Powe
  150mA M
  30mA Ma

The Intel® 2732
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faster, easier, an

An important 27
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AP-72 is availab

The 2732 has a s
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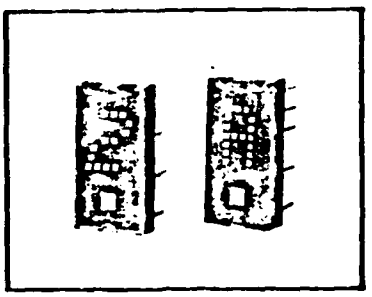
applying a TTL-

PI

R141525



745-0007

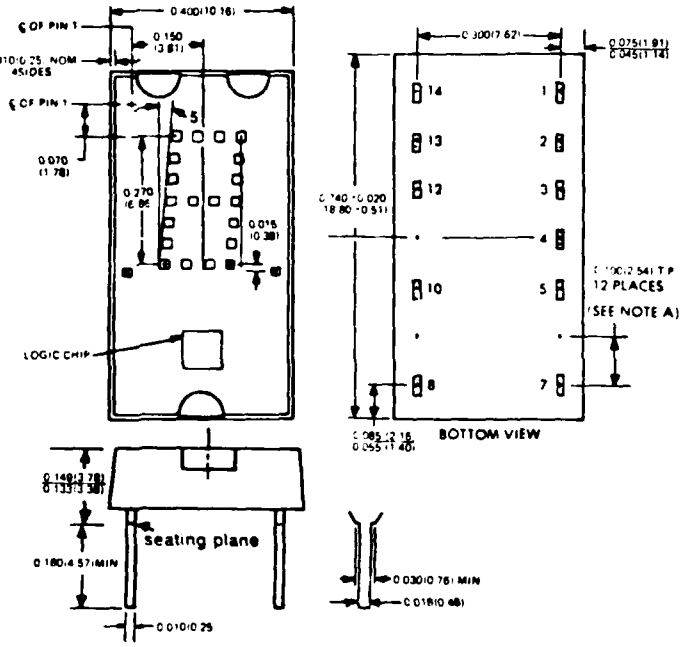
DIODE-LITE® Hexadecimal Display

with Integral TTL MSI Circuit Chip

character height: .270"

The display and TTL MSI chip are mounted on a lead-frame assembly which is then cast within an electrically nonconductive, transparent epoxy. Multiple displays may be mounted on 0.450 inch centers.

mechanical data



NOTES:

A. The true position pin spacing is 0.100 between centerlines. Each pin centerlines is located within ±0.010 of its true longitudinal position relative to pins 1 and 14.

B. Lead dimensions are not controlled above the seating plane.

C. Dimensions associated with position of LED's are between centerlines and are nominal.

D. All dimensions are in inches unless otherwise specified.

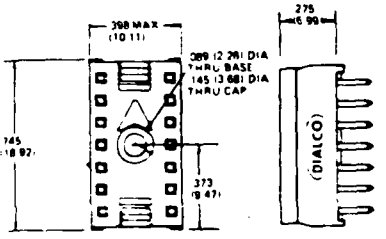
PIN 1 LED SUPPLY VOLTAGE
PIN 2 LATCH DATA INPUT B
PIN 3 LATCH DATA INPUT A
PIN 4 LEFT DECIMAL POINT CATHODE
PIN 5 LATCH STROBE INPUT
PIN 6 OMITTED
PIN 7 COMMON GROUND
PIN 8 BLANKING INPUT
PIN 9 OMITTED
PIN 10 RIGHT DECIMAL POINT CATHODE
PIN 11 OMITTED
PIN 12 LATCH DATA INPUT D
PIN 13 LATCH DATA INPUT C
PIN 14 LOGIC SUPPLY VOLTAGE, VCC

( ) Metric dimension in mm.

Solid-State Visible Hexadecimal Display With Integral TTL Circuit To Accept, Store, And Display 4-Bit Binary Data

- 0.270-Inch-High Character
- High Brightness
- Left-and-Right-Hand Decimals
- Separate LED and Logic Power Supplies May Be Used
- Easy System Interface
- Single-Plane Wide-Angle Visibility
- Internal TTL MSI Chip with Latch, Decoder, and Driver
- Operates from 5-Volt or 6-Volt Supply
- Constant-Current Drive for Hexadecimal Characters

connector 501-0701-009



For use with 745-0007 display.

DIALIGHT
A NORTH AMERICAN PHILIPS COMPANY
203 HARRISON PLACE • BROOKLYN, N.Y. 11237 • 212 497 7600 • TWX: 710-584-5487

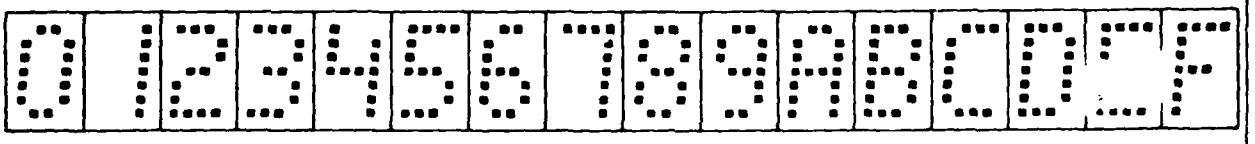
description 745-0007

This hexadecimal display contains a four-bit latch, decoder, driver, and 4x7 light-emitting-diode (LED) character with two externally-driven decimal points in a 14-pin package. A description of the functions of the inputs of this device follows.

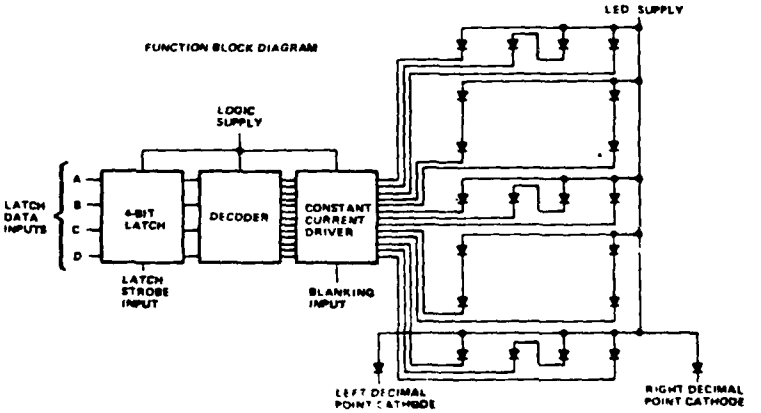
	PIN NO.	DESCRIPTION
LATCH STROBE INPUT	5	When low, the data in the latches follow the data on the latch data inputs. When high, the data in the latches will not change. If the display is blanked and then restored while the enable input is high, the previous character will again be displayed.
BLANKING INPUT	8	When high, the display is blanked regardless of the levels of the inputs. When low, a character is displayed as determined by the data in the latches. The blanking input may be pulsed for intensity modulation.
LATCH DATA INPUTS (A, B, C, D)	9, 2, 13, 12	Data on these inputs are entered into the latches when the enable input is low. The binary weights of these inputs are A = 1, B = 2, C = 4, D = 8.
DECIMAL POINT CATHODES	4, 10	These LEDs are not connected to the logic chip. If a decimal point is used, an external resistor or other current-limiting mechanism must be connected in series with it.
LED SUPPLY	1	This connection permits the user to save on regulated V_{CC} current by using a separate LED supply, or it may be externally connected to the logic supply (V_{CC}).
LOGIC SUPPLY (V_{CC})	14	Separate V_{CC} connection for the logic chip.
COMMON GROUND	7	This is the negative terminal for all logic and LED currents except for the decimal points.

The LED driver outputs are designed to maintain a relatively constant on-level current of approximately five milliamperes through each of the LED's forming the hexadecimal character. This current is virtually independent of the LED supply voltage within the recommended operating conditions. Drive current varies with changes in logic supply voltage resulting in a change in luminous intensity as shown in Figure 2. The decimal point anodes are connected to the LED supply; the cathodes are connected to external pins. Since there is no current limiting built into the decimal point circuits, this must be provided externally if the decimal points are used.

The resultant displays for the values of the binary data in the latches are as shown below.



0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15



description 745-0007

absolute maximum ratings over operating ambient-air temperature range (unless otherwise noted)

Logic Supply Voltage, V_{CC} (See Note 1)	7V
LED Supply Voltage (See Note 1)	7V
Input Voltage (Pins 2, 3, 5, 8, 12, 13, See Note 1)	5.5V
Decimal Point Current	20 mA
Operating Ambient-Air Temperature Range	0°C to 70°C
Storage Temperature Range	-55°C to 100°C

NOTE 1: Voltage values are with respect to common ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Logic Supply Voltage, V_{CC}	4.5	5	6.5	V
LED Supply Voltage, V_{LED}	4	5	7	V
Decimal Point Current, $I_{F(DP)}$		5		mA
Latch Strobe Pulse Width, t_w	40			ns
Setup Time, t_{setup} (See Note 2)	50			ns
Hold Time, t_{hold} (See Note 3)	40			ns

NOTES: 2 Setup time is the interval immediately preceding the positive-going transition of the latch strobe input during which interval the data to be displayed must be maintained at the latch data inputs to ensure its recognition.

3 Hold time is the interval immediately following the positive-going transition of the latch strobe input during which interval the data to be displayed must be maintained at the latch data inputs to ensure its continued recognition.

operating characteristics at 25°C ambient-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_V	Luminous Intensity (See Note 4)	Average Per Character LED	V_{CC} = 5V, V_{LED} = 5 V See Note 5	35	100		µcd
		Each decimal	$I_{F(DP)}$ = 5 mA	35	100		µcd
λ_p	Wavelength at Peak Emission		V_{CC} = 5 V, V_{LED} = 5 V $I_{F(DP)}$ = 5 mA, See Note 6	640	660	680	nm
B	Spectral Bandwidth between Half-Power Points				20		nm
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage		V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = 5.5 V, V_I = 5.5V			1	mA
I_{IH}	High-Level Input Current		V_{CC} = 5.5 V, V_I = 2.4V			40	µA
I_{IL}	Low-Level Input Current		V_{CC} = 5.5 V, V_I = 0.4 V			−1.6	mA
I_{CC}	Logic Supply Current		V_{CC} = 5.5 V, V_{LED} = 5.5 V, $I_{F(DP)}$ = 5 mA, All inputs at 0V		60	90	mA
I_{LED}	LED Supply Current				45	90	mA

NOTES: 4 Luminous intensity is measured with a solar cell and filter combination which approximates the CIE (International Commision on Illumination) eye-response curve.

5 This parameter is measured with 8 displayed, then again with E displayed.

6 These parameters are measured with .8. displayed.

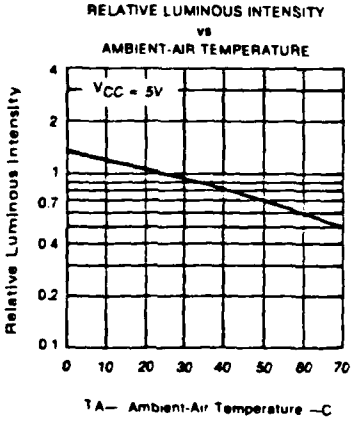


FIGURE 1

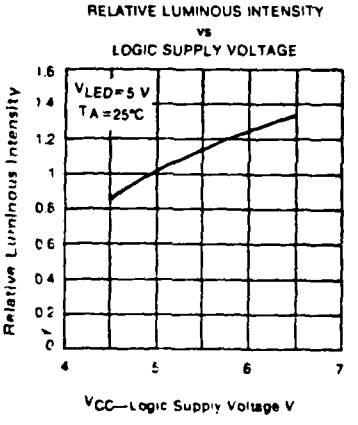


FIGURE 2

NO. ANDOVER, MA 01845
(617) 685-4371

ALCOSWITCH

GOLD CONTACTS STANDARD

SMC SERIES • MINI BI-DIRECTIONAL

SMC SERIES HAS LARGER VISIBLE READOUT CHARACTERS despite its small size. Many of the advantages of miniaturization found in the PICO Series are offered along with a greater number of output code options. This popular family is used in measurement and test instruments for range setting, data programming and count controlling; and in communications equipment for digital tuning. The simple, reliable bi-directional pushbutton mechanism permits rapid changes to either higher or lower numerical settings. Instrument-grade performance and long service life are enhanced by the heavy gold clad wiping contacts. Large readout characters are protected by dust-sealed window. Snap-together grouping and snap-in panel mounting minimize installation time and cost.

SPECIFICATIONS

Contact Rating: 0.4 VA @ 20 VDC or Peak AC.

Contact Circuit Resistance: 0.12 ohms max. (Total internal ckt. res.)

Mechanical Life: More than 10^6 operations.

Operating Temperature: -10°C to +60°C.

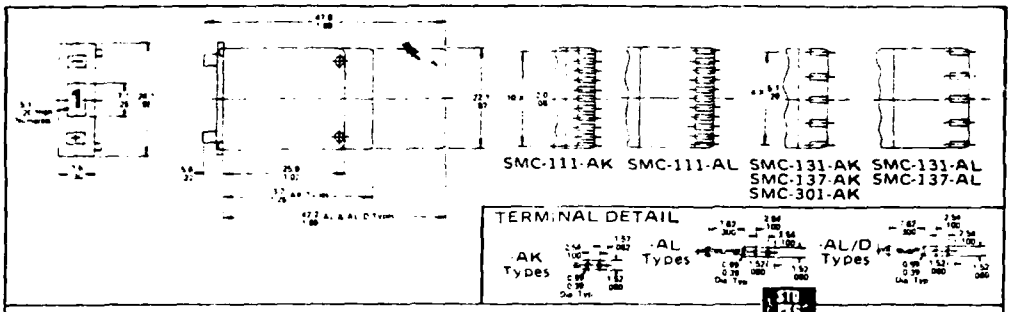
Housing: Black, matte finish. Material: Noryl SE1

PC Board: Glass epoxy type, G10.

PC Terminals Spacing: SMC-11: .079", SMC-141,-161: .100"
All Others: .200"

Character Height/Color: .200" (except -301 & -SG-558: .140"; SG-557: .120"). White on black background.

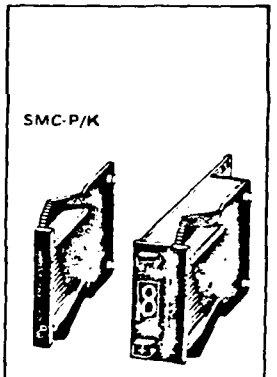
Contacts Gold Plating Thickness: Wiping: .0004" (10 microns)
Code Pattern: .00012" (3 microns)



Model	Code Pg. 86	Description	Characters	One-9	10-19	11-19	20-99	100-249
SMC-111-AK	111	Decimal Code, (1-of-10)	0-9	6.10	4.88	5.49	4.88	4.58
SMC-111-AK/01	111	Decimal Code, Repeating Readout	0&1	6.35	5.08	5.72	5.08	4.76
SMC-111-AK/05	111	Decimal Code, Repeating Readout	0&5	6.35	5.08	5.72	5.08	4.76
SMC-111-AK/+ —	111	Decimal Code, Repeating Readout	+&—	6.35	5.08	5.72	5.08	4.76
SMC-111-AL	111	Decimal Code, Extended PC Board	0-9	6.75	5.40	6.08	5.40	5.06
SMC-111-AL/+ —	111	Decimal Code, Extended PC Board	+&—	7.00	5.60	6.30	5.60	5.25
SMC-131-AK	131	1-2-4-8 BCD Code	0-9	6.10	4.88	5.49	4.88	4.58
SMC-131-AL/D	131	BCD, Extended PCB for diodes	0-9	6.75	5.40	6.08	5.40	5.06
SMC-137-AK	137	1-2-4-8 BCD Complement Code	0-9	6.10	4.88	5.49	4.88	4.58
SMC-137-AL/D	137	BCD, Complement, EXT. PCB for diodes	0-9	6.75	5.40	6.08	5.40	5.06
SMC-141-AK	141	BCD & BCD Complement Codes	0-9	6.75	5.40	6.08	5.40	5.06
SMC-301-AK	301	Hexadecimal (16 Positions)	0-9 & A-F	7.40	5.92	6.66	5.92	5.55
SMC-SG-557	301	Hexadecimal (16 Positions)	0-15	7.40	5.92	6.66	5.92	5.55
SMC-SG-558	301	Binary Coded Octal (8 Positions)	0-7	7.40	5.92	6.66	5.92	5.55
SMC-524-AK	524	Complement of 9's Complement	0-9	8.90	7.12	8.01	7.12	6.68
SMC-400-AK	400	SPDT 2-Position Repeating	+&—	5.90	4.72	5.31	4.72	4.43
†SMC-DS/09	—	Dummy Switch	0-9	5.25	4.20	4.73	4.20	3.94
SMC-WD5/1	WD5/1	1-2-4-4 Resistance Decade	0-9	6.75	5.40	6.08	5.40	5.06
*SMC-P/K (Pr.)		End Mounting Plates, Molded Clip		.95	.76	.86	.76	.71
SMC-BG		.300" Spacer Section		.95	.76	.86	.76	.71
SMC-A		.100" Spacer, with Mounting Clips		.50	.40	.45	.40	.38
SMC-A/DP		.100" Spacer, with Decimal Point		.95	.76	.86	.76	.71
B9L		Connector, 9 contacts, Solder Lugs		2.25	1.80	2.03	1.80	1.69
B9LS		Connector, 9 contacts, PC Terminals		2.25	1.80	2.03	1.80	1.69
B11LS		Connector, 11 contacts, PC Terminals		2.50	2.00	2.25	2.00	1.88

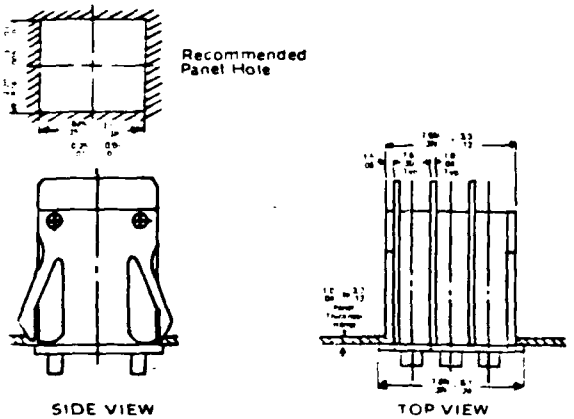
*Sold in pairs only †Mechanically operable, no electrical function

SMC



ADDITIONAL RECOMMENDED DIMENSIONS

Dimensions are given in inches. N=the number of switch modules. Panel opening width must be adjusted when using spacer; Add .300" for each SMC-BG used; add .100" for each SMC-A used.



MODULE ASSEMBLY METHOD

SMC bi-directional code switches may be easily assembled into groups of any number. The tabs or pins of one decade section press fit into the holes in the adjacent section. Spacers and end mounting plates may be included in the same manner, as desired. Assembly requires no additional hardware, no tools. This method requires little time and minimizes the cost in installation.

Groups of SMC switches with end plates snap into panel holes of the recommended size and are retained by metal clips. Again, tools and additional hardware items are not required.

CUSTOM SWITCHES

Contact factory for information concerning the feasibility, pricing and delivery of special switches, including non-standard codes, limit stopping, special wheel markings, optional colors and PC terminals.

FACTORY ASSEMBLED GROUPS

Special type numbers will be assigned for customers requiring delivery of assembled groups of code switches. Ready-to-mount assemblies are shipped individually packaged and identified. Contact factory for details

APPENDIX D

SCANNER PRINTOUTS

The bound document scanner is capable of providing printouts of documents up to 8 1/2" by 11" in size. This appendix shows some sample printouts obtained using the MK38P70 as well as the F-8 controller. Note that both controllers provide comparable copy. The copies were obtained under the following conditions:

Figures D.1 through D.4: F-8 controller
Figures D.5 through D.8: MK38P70 controller

These figures show that there are no discernible differences between copies obtained with the MK38P70 and those obtained using the F-8. The copies shown were made using manual thresholding in an attempt to obtain the most pleasing reproduction of the subject document. This involved making some choice between dark copy or high resolution; the IEEE facsimile charts best illustrate the trade-off. The other documents show the flexibility of the scanner in that it can give good reproduction of a variety of subjects. Note, however, that gray tones must be translated into either black or white pixels.

The printouts were made with all conditions remaining the same except different light bulbs were used for each controller, which resulted in a small difference in light non-uniformity compensation. Some ghosting and smearing is apparent on the copies; these problems are attributable to the printer electronics and toner dispenser on the printer, respectively.

Fig. D.1


NMA MICROFONT QJKLPYZ
68S12GH5D4X7U3W8V9E
PQR45DE4UV670FG8STHIJNOW•ABYZ
3KLM12C
ABCDEFGHIJKLMNOPQRS
TUVWXYZ 0123456789
'-{}%¢$YH ASA OCR-A
ABCDEFGHIJKLMNOPQRSTUV
WXYZabcdefghijklmnopqr
stuvwxyz1234567890PICA
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890 Elite
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890 Spartan Medium 8 pt
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890 Spartan Medium 10 pt
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890 Spartan Medium 12 pt
IEEE Std 167A-1975
FACSIMILE TEST CHART
Prepared by the IEEE Facsimile Subcommittee and printed by Eastman Kodak Company. Use in accordance with IEEE Std 167 1966, Test Procedure for Facsimile. Copyright 1975, Institute of Electrical and Electronics Engineers

Fig. D.2

3910
September, 1983

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science
Graduate Office - Room 38-444

APPLICATION FORM FOR ORAL QUALIFYING EXAMINATION

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The examining committee will consist of three faculty members. Two of these are selected by the Area Committee from the faculty in that Area. The third is selected by the Committee on Graduate Students from outside the Area. In order that the third member will have interests in common with you, you are asked to suggest three faculty members whose research interests seem appropriate. Consult the list of "Reserch Interests of Faculty Members Who Supervise Theses" available from the Graduate Office. If it is not possible to assign one of the three to your committee a faculty member with similar interests will be chosen.

The Department Committee on Graduate Students will consider the results of the oral examination and all other evidence available in deciding whether you are qualified for the doctoral program. You will be informed of the Committee's decision before the end of the term in which the examination was taken. If you are not considered qualified, you may apply to repeat the examination after consultation with your Graduate Counselor. A student who has not taken the Oral Qualifying Examination by the end of the fourth regular term will be allowed to continue in the doctoral program only with the explicit permission of the Committee on Graduate Students.

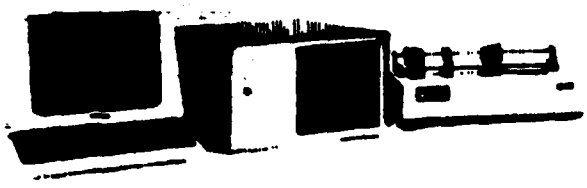
Submission of this form satisfies the requirement for filing a plan of graduate study as explained in Memo 3800. Changes in plans following submission of this form should be reported to the Graduate Office through the Graduate Counselor.

You should submit this form to the Graduate Office, Room 38-444, and give a copy to your Graduate Counselor.

Ask for Memo 3800.

Fig. D.3

S-100 MICRO-SYSTEMS



QT Maxi-System Package

$5395.00

List $7995.00 Save $2600.00

Includes:

- **MAINFRAME** - QTC-MF+DD8 Desk Top or Rack Mount Mainframe (11"h x 17"w x 20"d)
- **TERMINAL** - Televideo 925C w/detachable keybd.
- **PRINTER** - Your choice of Toshiba P-1350 (Letter [illegible] 100 cps) or OKI-DATA 84A (200 cps)
- **MOTHERBOARD** - 8 slot standard & 12 slot optional
- **CPU** - Systemaster single bd. computer (4Mhz)
- **MEMORY** - 64K RAM standard Expandable to 256K
- **FLOPPY DISK CONTROLLER** - Supports 5¼ or 8" drives
- **DISK DRIVES** - 2 megabytes on line • Double side double density 8" drives
- **I/O PORTS** - 2 Serial + 1 parallel port
- **MISCELLANEOUS FEATURES** - Key lock switch • 2 AC outlets for printer + terminal • Filtered fan • 15 ea DB25 cutouts
- Cables • Documentation
- **SOFTWARE** - CPM® Standard • 8 slot motherbd. (12 slots optional)

QT Maxi-Mini System Package

$3495.00

Includes:

- **MAINFRAME** - QTC-IMF+DD6 Desk Top Mainframe (11"h x 11"w x 20"d)
- **TERMINAL** - Televideo 925C w/detachable keybd.
- **PRINTER** - OKI-DATA 82A (200 cps)
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- **CPU** - Systemaster single bd. computer (4Mhz)
- **MEMORY** - 64K RAM standard Expandable to 256K
- **FLOPPY DISK CONTROLLER** - Supports 5¼ or 8" drives
- **DISK DRIVES** - 2 megabytes on line • Thinline double side double density 8" drives
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- Cables • Documentation
- **SOFTWARE** - CPM® Standard • 8 slot motherbd. (12 slots optional)

Maxi in capacity (2, 4 MG)
• Mini in price and size (11"h×11"w×20"d)

[illegible]

[illegible]

SOLDER TYPE		FLAT RIBBON TYPE	
DB25P	2.50	IDC25P	5.00
DB25S	3.50	IDC25S	5.00
DB25 Hood	1.00	IDC25 Hood	1.00

[illegible]

QTC-DDC5V cabinet with SA1004 - 10 MG Hard Disk
Only $1999.00

Retail Showroom
[illegible]
[illegible]

The Great Salt Lake Computer Company, Inc.

Mail Orders
[illegible]
[illegible]

CIRCLE 208 ON READER SERVICE CARD

Fig. D.4

Five Star Club Winners

We are pleased to announce the following names of AFCEANs who are new members of the Five Star Club. Members of the Club have recruited five or more new members into the Association.

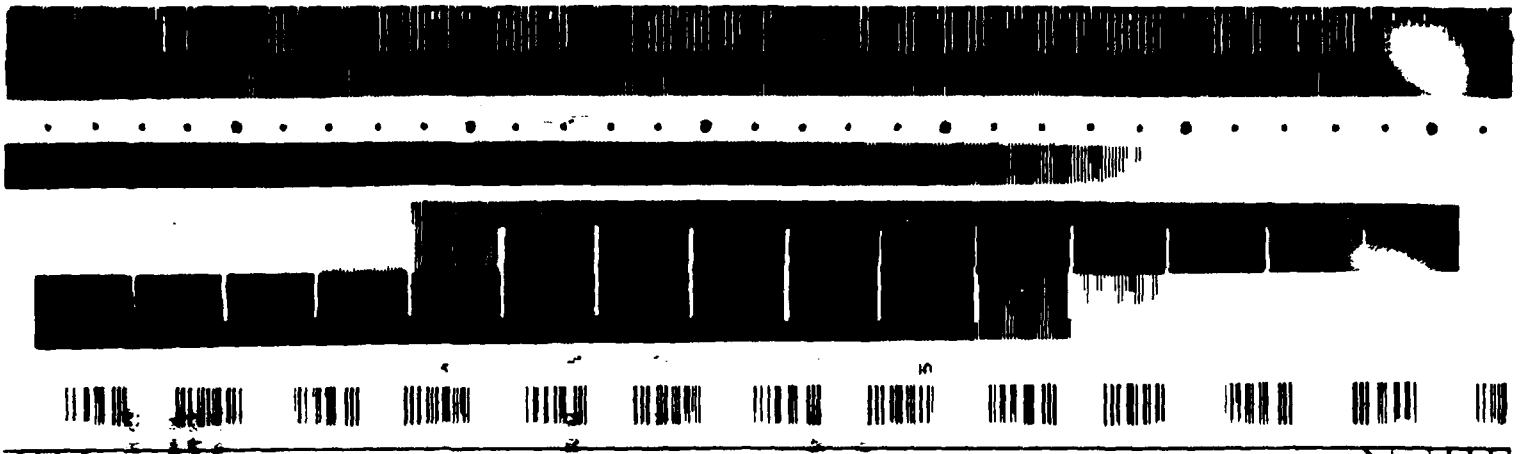
CWO-2 T. R. Armstrong
E. R. Ates
LTC Tommy H. Berggren
Lt. Don Carmichael
C. F. Chicarelli
LTC G. L. Coady
Anderson Cox
Jeff Ewell
Barbara A. Fischer
Capt. R. M. Fisher
Gerald F. Gaa
LTC Thomas Gallagher
Capt. G. Ray Gibson
1Lt. David Gruber
LTC Ronald Hall
Capt. Scott A. Hammell
George B. Hanson
Maj. Mike Harris
Lt. Robert Kahlo
Col. W. S. Kromer
Marie Langford
Bud J. Longfellow
1Lt. Alan S. McCoy
2Lt. Michael D. McDonald
K. H. Metcalfe
Kathleen A. Mihlbauer
LTC Danny C. Miller
J. Murphy
G. T. Pothier
2Lt. Donald M. Roberts

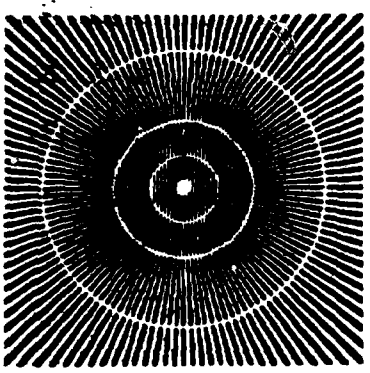
Top Twenty Club

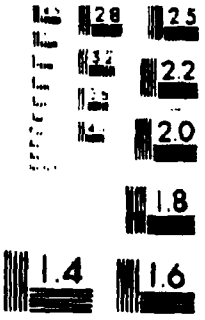
AFCEA members who have taken a three year Association membership automatically qualify for the Top Twenty Club. Listed below are those who have joined between April 1, 1983 and April 30, 1983.

Patrick G. Agnew
Robert R. Altenhof
Ekkehard Antz
Capt. Bruce S. Barrett
Albert E. Bennett
2Lt. Christopher P. Benoit
L. Berckmans
Harry P. Bimburant
Ray J. Blisard
Capt. Frank W. Bost
2Lt. Leighton K. Boyd
LTC John I. Brennecke
Ramon P. Britt
Capt. Ronald T. Broderick
Roger Burton
Thomas D. Clark
MSgt. Martin Collett, Jr.
Patrick J. Conley
Marvin B. Crouch
L. Daniel Crowley
Col. Milton Dawsen
Donald P. Devriend
GYSgt. Eddie L. Dunn
LTC Donald A. Durant
Harry G. Eberhardt, Jr.
O. R. Frederiksen
Maj. Richard G. Galloway
Gerald N. Galstan
Ralph E. Grant
LTC Allan J. Hansen, Jr.
Edwin W. Harris
Eleanor S. Harris
Elwood W. Hertzog
Maj. Ronald Hinkle
Michael Honey
Russell D. Housley
LTC Jay D. Huttenhow
Maj. Mon'd Izzat
Col. Larry E. Jarman
Gerald D. Jones
Paul P. Kays
Paul J. Kirzow
Daniel J. Knauf
1Lt. Frederic D. Knight
Robert H. Krumpe
Maj. Wilfred J. Lefresne
Donald E. Lively
Douglas Lockie
John R. Looney
James W. Loughran
Capt. Donna G. Mailhot
Capt. James A. Mailhot
James Malone
Elliott N. Meyer
Harry T. Morris
Sgt. Kenneth G. Park
Richard L. Pellican
Michael A. Pizzuti
Leonard Plotkin
Clifford A. Purcell
LTC Stephen R. Rose
Joseph A. Shahoud
George Shimabuku
Col. Harold W. Sidebottom
Nicholas V. Slondsky
Capt. Linda R. Smith
Larry Spice
George F. States
Guy B. Stephenson, Jr.
Herbert J. Stoklasek
Heinz G. Stroebel
LTC Gerald Swinarsky
Maj. Sidney L. Taylor
Capt. Ann M. Testa
Maj. Kenneth L. Thomas
George D. Thompson
CW2 John C. Ullian
Mark Vanderzwiep
John G. Vlahos
Capt. L. A. Wade
William J. Watts
Col. Harry M. York
Capt. Vickie A. Young
Cdr. Donald K. Youngblood

Fig. D.5







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'-{}%*$¥H ASA OCR-A

ABCDEFGHIJKLMNOPQRSTUV
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abcdefghijklmnopqrstuvwxyz
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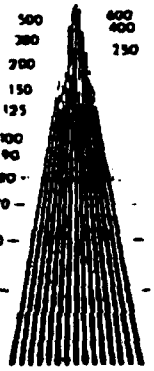

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1234567890 Spartan Medium 8 pt

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890 Spartan Medium 10 pt

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890 Spartan Medium 12 pt

IEEE Std 167A-1975

FACSIMILE TEST CHART

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Fig. D.6

S910
September, 1983
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science
Graduate Office - Room 38-444

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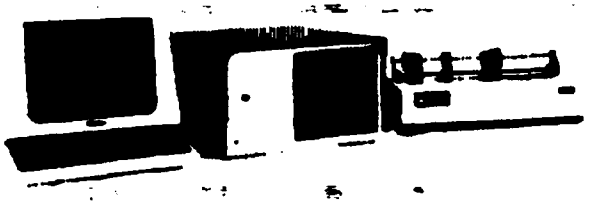
S-100 MICRO-SYSTEMS



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$5395.00

List $7995.00 Save $2600.00

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[illegible] CONNECTOR CORNER

RS232 Connectors

SOLDER TYPE		FLAT RIBBON TYPE	
DB25P	2.50	IDC25P	[illegible]
DB25S	3.00	IDC25S	6.00
DB25 Hood	1.00	IDC25 Hood	1.00

HARD DISK SUB ASSEMBLY

QTC-DDC6V cabinet with SA 1004 - 10 MG Hard Disk

Only $1695.00

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1Lt. David Gruber
LTC Ronald Hall
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George B. Hanson
Maj. Mike Harris
Lt. Robert Kahlo
Col. W. S. Kromer
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1Lt. Alan S. McCoy
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LTC Donald A. Durant
Harry G. Eberhardt, Jr.
O. R. Frederiksen
Maj. Richard G. Galloway
Gerald N. Galstan
Ralph E. Grant
LTC Allan J. Hansen, Jr.
Edwin W. Harris
Eleanor S. Harris
Elwood W. Hertzog
Maj. Ronald Hinkle
Michael Honey
Russell D. Housley
LTC Jay D. Huttenhow
Maj. Mon'd Izzat
Col. Larry E. Jarman
Gerald D. Jones
Paul P. Keys
Paul J. Kirzow
Daniel J. Knauf
1Lt. Frederic D. Knight
Robert H. Krumpe
Maj. Wilfred J. Lefresne
Donald E. Lively
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James W. Loughran
Capt. Donna G. Mailhot
Capt. James A. Mailhot
James Malone
Elliott N. Meyer
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Sgt. Kenneth G. Park
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Joseph A. Shahoud
George Shimabuku
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Nicholas V. Slonsky
Capt. Linda R. Smith
Larry Spice
George F. States
Guy B. Stephenson, Jr.
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Heinz G. Stroebel
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Maj. Sidney L. Taylor
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Capt. L. A. Wade
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Capt. Vickie A. Young
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APPENDIX E

DATA COMPRESSION CONSIDERATIONS

As stated in Chapter 4, two data compression schemes have been proposed thus far for incorporation into the bound document scanner. Both schemes essentially seek to compress CCD image data clocked out at 800 kilobits per second into a format that can be accommodated by a 56 kilobit per second leased telephone line. Lin's scheme (5) uses a Z80 microprocessor and support chips and implements data compression encoding and decoding in software, whereas Dishop (2) uses a strict hardware approach to encoding and decoding. Lin's scheme can utilize a number of encoding algorithms; Dishop uses only the B-1 encoding algorithm. Both compression and decompression have been implemented by Lin whereas only the compressor part of Dishop's scheme has been tested.

A point-to-point document transmission system (full duplex) utilizing data compression is shown in the block diagram of Figure E.1. A compressor, decompressor, and transmission line interface are the major components which need to be added to the existing scanner system. Note that the system must accurately transmit digitized and compressed CCD lines to the receiver and that display control command data must either be transmitted between CCD lines or generated at the receiving end. Dishop's scheme permits transmission of display control commands whereas Lin's scheme requires the receiving controller to generate display commands.

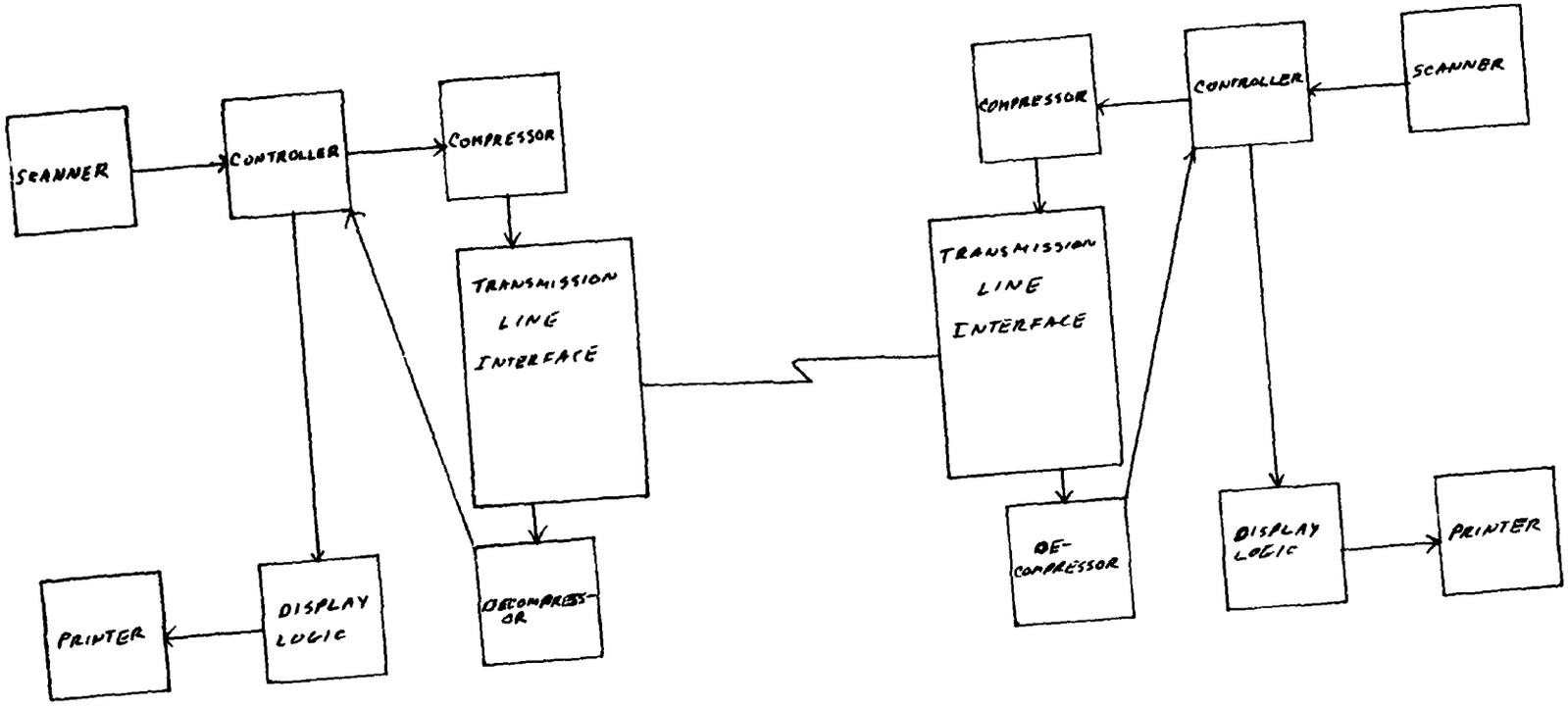

Fig. E.1 Document Transmission System Using Data Compression

Dishop's scheme essentially requires controller action only on the transmission side of the system. The controller must make three lines available with the signals $\overline{\text{START}}$, $\overline{\text{FSTLN}}$, and $\overline{\text{LSTLN}}$ generated on these lines by the control software. ($\overline{\text{START}}$ is generated by software sensing of the scanner $\overline{\text{START}}$ signal on I/O Board 4; $\overline{\text{FSTLN}}$ and $\overline{\text{LSTLN}}$ are generated by software sensing of the scanner $\overline{\text{PRINTLINE}}$ signal on I/O Board 4.) Figure E.2a is a block diagram of Dishop's compressor and Figure E.2b is a block diagram of Dishop's decompressor. The compressor diagram shows $\overline{\text{START}}$, $\overline{\text{FSTLN}}$, and $\overline{\text{ENDLN}}$, as well as DATA, LINE, F1* and EXTCLK which are extracted from the scanner hardware. Assuming that the sequence of commands and CCD lines is properly reconstructed by the decompressor at the receiving end, data can be passed directly to the display circuitry without intervention by the controller. The MK38P70 controller can therefore be used essentially as is, with the exception of providing the three additional signal lines. Port bits can be made available for these lines by minor modifications to the controller circuit.

Lin's scheme requires controller action at both the transmitting and receiving sides of the system. For transmission, the controller must, as a minimum, accomplish thresholding and send scan data to the compressor in 1700 line blocks (one page). On the receiving end, the controller must be able to detect the beginning and end of each line and beginning and end of each page, generate required display commands, and send commands and CCD data to the display logic. Assuming correct decompression, the receiving controller can be a scaled down version of the existing MK38P70 controller, with interfaces only to the logic now contained on I/O Boards 4 and 5. Two

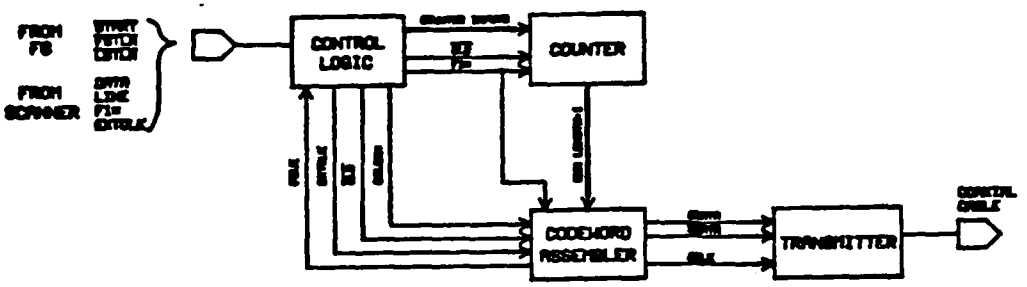

Fig. E.2a Dishop Compressor Block Diagram *

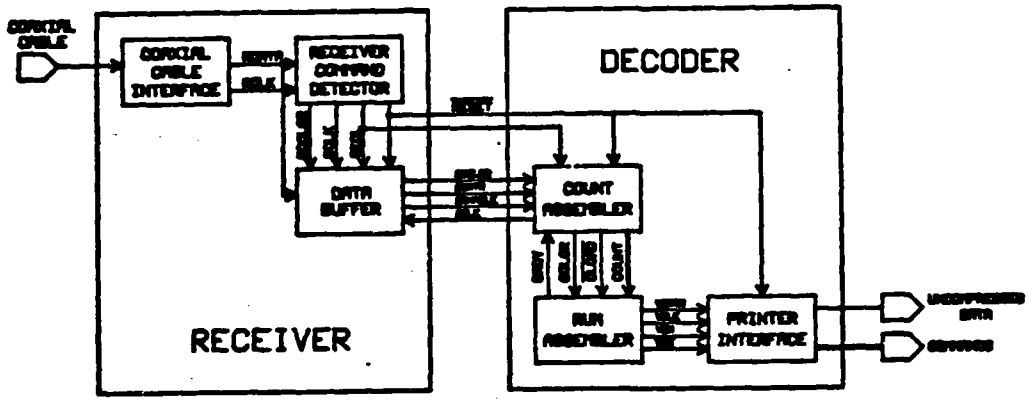

Fig E.2b Dishop Decompressor Block Diagram *

* Extracted from Dishop (2)

controllers, then, would be needed at each end of a point-to-point full duplex system if simultaneous transmission and reception are desired. The separation of functions would yield a simpler scanner interface for each controller. Port capacity would also be freed up to provide the Beginning of Page (BOP) and End of Page (EOP) control signals needed for Lin's compressor. As suggested by Lin, a Z80-DMA (Direct Memory Access) could be used to read in the 800 kilobit per second CCD data. An MK38P73 (serial port version) controller could not be used to perform this function since this device can only process data up to a rate of 9.6 kilobits per second. The DMA, however, can convert the 2048 serial bits corresponding to a scan line to the 256 8-bit bytes required by the compressor input queues. An inverse arrangement could be used at the receiving end, with the DMA combining parallel data (256x8 bytes) back into a serial bit stream. Figure E.3 shows a block diagram of Lin's scheme using two MK38P70 controllers and DMAs. Note that the DMA is a physical and logical peripheral of the Z80 microprocessor and its use would require either modifications to the Z80-based compressor-decompressor or a separate Z80 chip.

In summary, it appears that the MK38P70 controller can continue to be used in a scanner system utilizing either of these compression schemes. It is likely that the functions presently performed by the controller will still exist in a transmission system, and parts or all of these functions can be handled by one or more MK38P70s in a functionally distributed system. It seems unlikely that all control functions, compression, decompression, and any processing on the CCD data needed could be accomplished with a single general purpose microprocesor at this time.

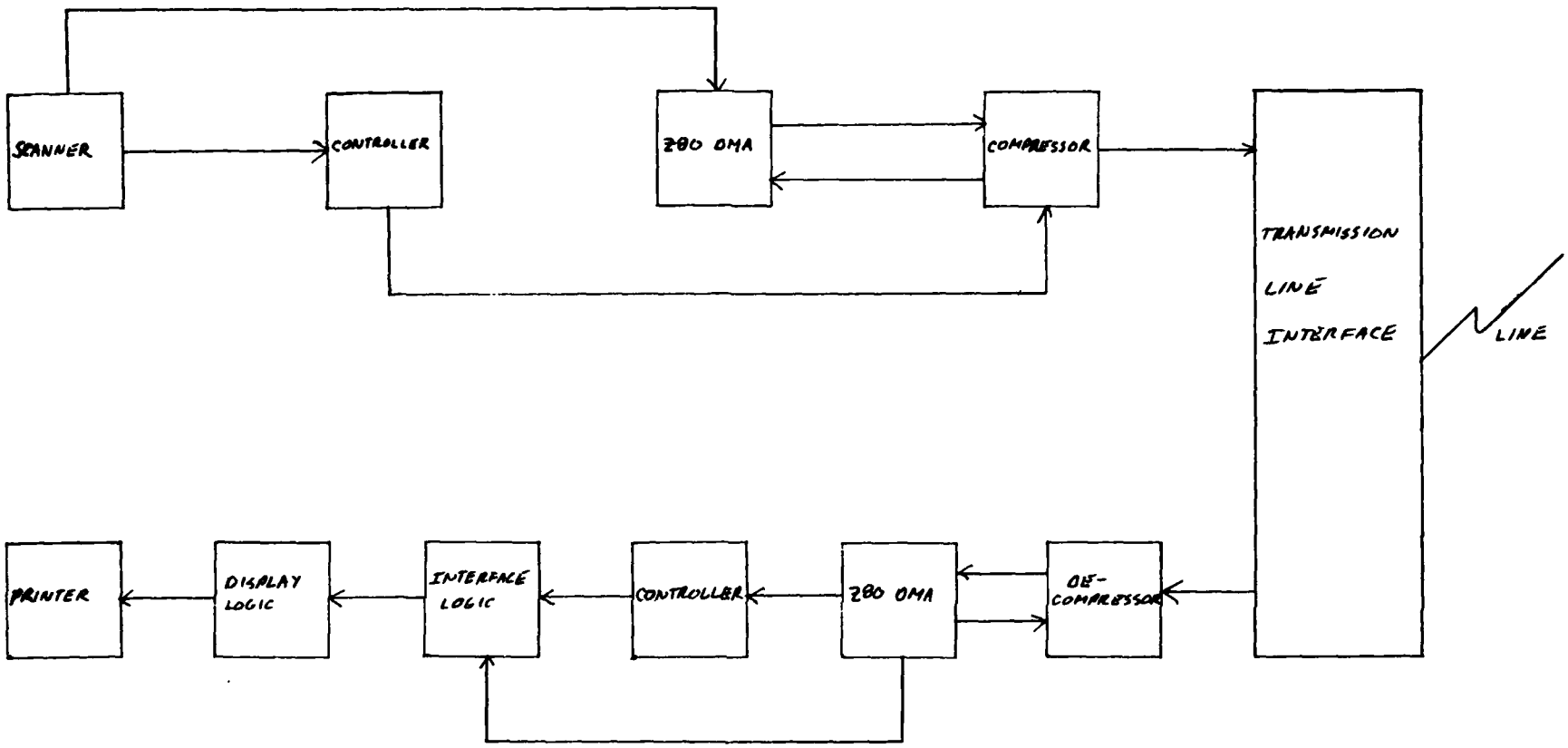

Fig. E.3 Scanner System Using Lin's Compression/Decompression Scheme

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