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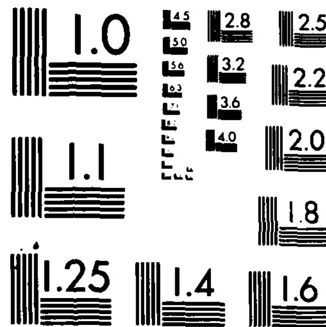

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Progress Report on

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LAYERED STRUCTURES PREPARED BY

MOLECULAR BEAM EPITAXY"

Covering the period of

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by

Hadis Morkoç

University of Illinois

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The research on modulation doped AlGaAs/GaAs FETs (MODFETs) and on AlGaAs buffer GaAs MESFETs has continued with substantial progress. Current-voltage collapse observed in the drain characteristics of MODFETs in dark at 77K have for the first time been eliminated. The responsible mechanisms were found to relate to the defect concentration in AlGaAs and also to the gate recess width relative to the gate. Microwave S-parameter measurements were also made to deduce the device equivalent circuit parameters and compared to conventional GaAs MESFETs. The results are compared qualitatively to predictions.

In GaAs FETs with high resistivity AlGaAs buffer layers it was found that no improvement (relative to GaAs buffer FETs) but degradation can result if the AlGaAs buffer GaAs active layer interface is not of high quality. The only way high quality can be assured has been found to be via the use of a thin superlattice at the heterointerface. Both optical and electrical properties of the GaAs layer grown on this superlattice is of sufficiently (over)

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Chief, Technical Information Division

I. INTRODUCTION

Great technological advances coupled with a strong motivation for high speed data handling capability have in the past few years led to substantial advances to be made in high speed devices. For devices to operate at high frequencies the transit time through the device and parasitics or susceptibility of the device to parasitics, must be minimized. The transit time can be reduced by decreasing the path length, e.g. gate length in FETs, and/or by increasing the carrier velocity. There is no universal recipe to reduce the influence of all parasitics but proper measures, such as improved ohmic contacts, metal conductors and small geometrics are useful.

In digital circuit applications in addition to fast intrinsic switching time, the device must be able to drive the device, line and parasitic capacitances. This calls for large current levels leading to the requirement that both the carrier concentrations and carrier velocity and mobility must be high. To maintain a low power consumption, the digital switching device should be a normally-off type which implies that the channel must be very thin since the compound semiconductor gate technology is based on Schottky gates. Achievement of non-leaky gates put an upper limit on the doping level at about 10^{18} cm^{-3}. The channel must then be made thin enough to be depleted by the gate built-in voltage. Such large doping levels degrade the electron mobility and to a lesser extent the electron velocity.

Modulation doped structure can meet the very requirement mentioned above while providing enhanced electron mobility and velocity. In very high speed switching applications the device is driven from off to on and back to off conditions very rapidly. This being the case the turn-on and turn-off

characteristics become very important and enhanced mobility plays an important role as well. Naturally the parasitic resistance components such as the source resistance is also lowered due to increased mobility and velocity.

The heterojunction FETs go by various names, e.g. MODFET for modulation doped FET, SDHT for selectively doped heterojunction FET, HEMT for high electron mobility transistor and FEGFET for two dimensional electron gas FET. In this text we will refer to this device as "MODFET ."

II. HOW MODULATION DOPING WORKS

Modulation doping relies on selective doping of a semiconductor layer adjacent to undoped smaller bandgap semiconductor layer. Theoretically as long as long as the donor energy (acceptor in p-type case) is larger than the conduction band energy of the smaller bandgap material the electrons diffuse into the smaller bandgap material. The details of these kind of structures and properties can be found in Chapter.. The two most commonly studied systems so far have been GaAs/AlGaAs[1] and $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$[2] lattice matched systems. Systems such as $In_{0.53}Ga_{0.47}As/InP$[3] have also been investigated. In this text we will concentrate on the GaAs/AlGaAs heterojunction systems with which the vast majority of the devices and the only device with high speed data have been fabricated.

Fig. 1 shows the schematical cross-section of a single heterointerface modulation doped structure. The structure is grown typically by molecular beam epitaxy generally at a growth rate of 1μm/hr and at a substrate temperatures of 580-620°c. Following the growth of an undoped buffer layer, typically 1μm thick, the AlGaAs layer part of which is left undoped at the heterointerface to reduce the coulombic interaction between donors and

electrons[4,5] is grown. A thin surface layer of GaAs either doped or undoped is optional. For structures intended for very high electron mobilities, the undoped layer thickness is quite large, $\geq \sim 200$ Å, and for them to be used in FETs, thin layer is quite this, about 30 Å. The latter is to obtain large transconductances which lead to improved device performance.

Although predicted in the late sixties, the first experimental realization of modulation doing came out of independent research at AT and T Bell Laboratories in the late seventies. Improved transport obtained has quickly transformed into a worldwide effort to use this structure for high speed devices.[7-11]

III. FET FABRICATION

The first step in device fabrication is generally the device isolation which in most cases is done by chemically etching mesas down to the undoped GaAs layer or to the semi-insulating substrate, or by an isolating implant. The source and drain areas are then defined in positive photoresist and typically AuGe/Ni/Au metallization is evaporated. Following the lift-off, the sorce-drain metallization is alloyed at or above 400°C for a short time (~ 1 min.) to obtain ohmic contacts. During this process Ge alloys down past the heterointerface, thus making contact to the sheet of electrons as shown in Figure 2.

The gate is then defied and a very small amount of recessing is done by either chemical etching, reactive ion etching, or ion milling. The extent of the recess is dependent upon whether depletion or enhancement mode devices are desired. In depletion mode devices, the remaining doped layer should be just the thickness to be depleted by the gate Schottky barrier. In enhancement

mode devices, the remaining doped AlGaAs is much thinner and thus the Schottky barrier depletes the electron gas as well. In test circuits composed of ring oscillators, the switches are of enhancement mode which conduct current when a positive voltage is applied to the gate and the loads are of depletin type. Figure 3 shows the top view of a MODFET with a gate dimension of 1 μm x 300 μm intended for microwave applications. For logic circuits, the gate width is typically 20 μm.

In the long run, more advanced fabrication procedures for reducing the access resistors must be employed (will be described later). In addition the structures must be designed to allow reproducible gate recess. This can be achieved by placing a very thin GaAs layer, a specific distance away from the interface, determined by the desired device characteristic. The recessing preferably done by dry processing can be stopped selectively at the GaAs surface which also makes possible the deposition of the gate on the more stable GaAs as opposed to AlGaAs.

IV. PRINCIPLES OF HETEROJUNCTION FET

IV.a. General

Since the electron moving parallel to the heterointerface encounter reduced scattering by ionized donors located in AlGaAs layer, the current conducting channel must be parallel to the heterointerface. Modulation of the channel current is done by a third terminal, gate, placed on the doped AlGaAs layer. Since the transport properties of the AlGaAs is much inferior to even the bulk GaAs, care should be exercised to make certain that the AlGaAs layer is entirely depleted by the gate and hetero-interface fields. Only then the

current is carried entirely by the two dimensional electron gas having enhanced properties.

In discrete devices, the power consumed can be dissipated rather easily allowing the use of normally-on devices. In this case with no external gate bias only the AlGaAs layer is depleted and the device conducts the maximum amount of current. When a negative gate bias is applied with respect to the source, the channel (two dimensional electron gas) is depleted pinching off the device. In intergrated circuits, however, the device density is very high and power consumption of normally on devices prohibits their use. The doped AlGaAs layer under the gate in then made thinner such that the gate with no external bias depletes the electron gas as well. The current flows only when a positive voltage is applied to the gate.

The device operation is to some extent analogous to that of the Si/SiO_2 MOSFET. While the basic principles of operation are similar, material systems and the details of device physics are different. The most striking difference, however, is the lack of appreciable interface states in this heterojunction system. Where the gate metal and the channel are separated by only about 400Å. This, coupled with the large dielectric constant of $Al_xGa_{1-x}As$ as compared to SiO_2 gives rise to extremely large transconductances. In addition, large electron densities, about $10^{12} cm^{-2}$, and higher electron velocities and mobilities can be achieved at the interface which lead to high current levels. The effective mass of electrons in GaAs is much smaller than in Si and therefore electron concentrations under consideration raise the Fermi level up into the conduction band, which is not the case for Si MOSFETs. It is therefore necessary to develop a new model for this device as has been attempted by the Thomson CSF group[12] and by the team at the University of Minnesota and Illi-

nois.[13] In order to calculate the current voltage characteristics, we must first determine the two dimensional electron gas concentration.

IV.b. Electron gas concentration

As indicated earlier, the electrons diffuse from the doped $Al_xGa_{1-x}As$ to the GaAs where they are confined by the energy barrier and form a two dimensional electron gas. This was verified by the Shubnikov de Hass osci''ations and their dependence on the angle between the magnetic field and the rmal of the sample.[14] The wave vector for such a system is quantized in the rection perpendicular to but not parallel to the interface.

The electric field set up by the charge separation causes a severe band bending in the GaAs layer with a resultant triangular potential barrier where the allowed states are no longer continuous in energy, but discrete. As a result, quantized sub-bands are formed and a new two dimensional model is needed to calculate the electron concentration. In most cases the ground sub-band is filled with the first excited sub-band being partially empty. Since the the wave functions or the electron concentration is distributed slightly in direction perpendicular to the heterointerface we will refer to the areal density of the electron gas from now on.

To determine the electron concentration we must first relate it to the sub-band energies. The rigorous approach is to solve for the sub-band energies self-consistently with the solution for the potential derived from the electric charge distribution. This has been done by Stern and Howard[15] for the silicon-silicon dioxide system in the sixties, and more recently by Ando[16] for the GaAs-AlGaAs system. A workable approximation is to assume that the potential well is perfectly triangular, and that only the ground and first

sub-bands need be considered. Using the experimentally obtained sub-band populations, adjustments in the parameters can be made to account for he non-constant electric field and non-parabolicity in the conduction band. Solving Poisson's equation in AlGaAs and GaAs layers and using Gauss' law, one can obtain another expression for the sheet electron concentration in terms of structural parameters, e.g., the doping level in AlGaAs, doped and undoped AlGaAs layer thicknesses, and the magnitude of conduction band energy discontinuity or the AlAs mole fraction in AlGaAs.[13]

Analysis of the Fermi level shows[13] that it is a linear function of the sheet carrier concentration, n_s, for $n_s \geq 5 \times 10^{11} cm^{-2}$. Taking this into account one can eliminate the iteration process because analytical expressions become available. Another feature that must be considered in the model is the necessity of using the Fermi-Dirac as opposed to the commonly used Maxwell-Boltzmann statistics.[17] This term is particularly import·.nt at room temperature because of larger thermal energy energy. In the case of Si/SiO_2 MOSFET's, three dimensional analyses work quite well because the Fermi level is not as high; but they fail for this heterojunction FET. This will be explained in detail next.

The interface density of the 2DEG, n_s, is determined as

$$n_s = \int_{E_c}^{\infty} f(E)g(E)\, dE \tag{1}$$

where E_c is the bottom of the conduction band, g(E) is the density of states and

$$f(E) = \frac{1}{1 + \exp[(E - E_F)/kT]} \tag{2}$$

is the Fermi-Dirac distribution. In Si MOSFET's the integral in eq. (1) may be evaluated using the following assumptions:

i) the Maxwell-Boltzmann (rather than the Fermi-Dirac) distribution function may be used,

ii) the density of states in the potential well near the interface is continuous.

Both of these assumptions are justified for Si MOSFET's but are <u>not</u> justified for modulation doped structures. This is illustrated by Fig. 4 where interface carrier densities for intrinsic Si and GaAs are plotted as functions of the Fermi level using the three dimensional Joyce-Dixon approximation[18] (dashed line) and a more accurate "two dimensional" formula proposed in reference[12]. This two dimensional model is based on considering the quantized energy levels in the potential well near the interface. It is also shown that a simple linear approximation for the n_s vs. E_F curve which may be used in analytical calculations[19] for interface densities greater than about 5 x 10^{11} cm^{-2}. Due to a large effective electron mass in Si (m^*/m_o = 0.3 for one ellipsoid in the (100) direction) and six ellipsoids included in the density of states effective mass, there are many levels in the potential well so that a "three dimensional" theory works quite well. The Maxwell-Boltzmann distribution function may be used because the position of the Fermi level (for realistic interface densities) is about 0.1 eV or so below the bottom of the potential well. In GaAs the Fermi Level is in the potential well, necessitating the use of the Fermi-Dirac distribution therefore, the discrepancy between the three-dimensional and two-dimensional models is quite large in GaAs. The theory of modulation doped structures should also account for the fact that the position of the Fermi level in Si is much less sensitive to the interface carrier density n_s as compared to GaAs.

For $n_s > 5 \times 10^{11}$ cm^{-2} the linearized relationship between n_s and E_F (Fig. 4) can be used which allows the following analytical expression for the maximum density of the two dimensional electron gas to be derived.[17]

$$n_s = [N_d^2(d_i+\Delta d)^2 + (2\varepsilon N_d/q^2)(\Delta E_c+\delta(\Delta E_c)-E_{F2})]^{1/2}-N_d(d_i+\Delta d) \quad (3)$$

where N_d is the donor density, d_i is the thickness of the undoped (Al,Ga)As layer, Δd = 80 Å is a constant related to the E_F vs. n_s curve[19], ε is the dielectric permittivity of (Al,Ga)As, q is the electronic charge, ΔE_c is the discontinuity in the conduction band,

$$\delta(\Delta E_c) = -(kT)[\ln(1+g'y) + 4/N'_d \ln(1+1/4y)] \quad (4)$$

and

$$y = [((1-1/4N'_d)^2 + 4g'N'_d)^{1/2} - (1-1/4N'_d]/2g' \quad (5)$$

where

$$N'_d = N_d/N_c, \qquad g' = g\exp(+E_d/kT) \quad (6)$$

and

$$y = \exp(-E_{F2}/kT)$$

Here E_{F2} is the energy difference between the bottom of the conduction band and the Fermi level in (Al,Ga)As, N_c is the density of states in (Al,Ga)As, g

is the donor g-factor and E_d is the donor ionization energy. Comparison of the exact solution (dotted line) with our analytical expression for n_s (solid line) in Fig. 5 illustrates the accuracy of the approximation.

IV.c. Charge Control and I-V Characteristics

So far we have related the interface charge, which is to carry the current parallel to the heterointerface, to the structural parameters of the heterojunction system. To control and modulate this charge, and therefore the current, a Schottky barrier is placed on the doped AlGaAs layer. As indicated earlier the doped AlGaAs is depleted at the heterointerface by electron diffusion into GaAs, but this is limited to about 100 Å for an AlGaAs doping level of about $10^{18}cm^{-3}$. It is also depleted from the surface by the Schottky barrier. To avoid conduction through AlGaAs which has inferior transport properties and screening of the channel by the carriers in the AlGaAs, parameters must be chosen such that the two depletion regions just overlap. Detailed description of the device modeling and analysis has been given elsewhere.[20]

In normally-on devices the depletion by the gate built-in voltage should be just enough to have the surface depletion extended to the interface depletion. For example, devices designed for 10^{12} cm^{-2} electrons in the channel can be turned off at a gate bias of -1V by the gate located 600 Å away from the interface on the AlGaAs layer. This is the structure used for discrete high speed analog applications, e.g., microwave low noise amplifiers.

In normally-off devices the thickness of the doped AlGaAs under the gate is smaller and the gate built-in voltage depletes the doped AlGaAs, overcomes the built-in potential at the heterointerface, and depletes the electron gas. No current flows through the device unless a positive gate voltage is applied

to the gate. This type of device is used as a switch in high speed integrated digital circuits because of the associated low power dissipation. The loads may be normally-on transistors with the gate shorted to the source, or an ungated "saturated resistor", which has a saturating current characteristic due to the velocity saturation of the carriers.

Away from the cut-off regime, it is quite reasonable to assume that the capacitance under the gate is constant and thus the charge at the interface is linearly proportional to the gate voltage minus the threshold voltage. As the threshold voltage is approached, the triangular potential well widens, and the Fermi-energy of the electrons is lowered. This change in surface potential substracts from the change in the applied gate bias, so that a lesser change in potential acts across the AlGaAs layer, reducing the transconductance of the device, and causing the curvature of the gate characteristic near threshold, as will be discussed later. This curvature is more pronounced at room temperature, due to the thermal distribution of the electrons, however some curvature will persist down to the lowest temperatures, due to quantum-mechanical confinement energies. This has profound implications for device operation since it preclues high speed operation at voltages less than a few tenths of a volt. This means that ultra low power-delay products, similar to those of Josephson Junction devices, which operate at a few millivolts only, would not be [illegible]lized. Near complete pinchoff (defined loosley as when the free electron [illegible]ntration drops to 10% of its maximum value) the effective position[1][illegible] the electron gas may be 200 Å away from the interface as shown in Fig. 6. This simply implies that it will require larger gate voltages to deplete the electron gas leading to a slow gradual pinch-off. In addition, the gate capacitance near pinch-off will show a decline as well.

Away from cut-off, the charge can be assumed to be linearly proportional to the gate voltage, and in the velocity saturated regime the current will then be linearly proportional to gate voltage and the transconductance will approach a constant (except when the AlGaAs starts conducting). These arguments apply to the velocity saturated MOSFET as well. For the MESFET, in contrast, the transconductance increases with increasing gate biases, since the depletion layer width narrows and modulation of the channel charge increases.

In order to calculate the current voltage characteristic, one must know the electron velocity as a function of electric field. Since the device dimensions (gate) used are about 1μm or less, high field effects such as velocity saturation must be considered.

Even though the electrons in MODFETs are located in GaAs and the electron transport in GaAs is well known, there was some confusion in the early days as to what one should expect. There were, in fact, reports, that this heterojunction structure held promise only because of the high mobilities which are measured at extremely small voltages (electric field $\leq$ 5 V/cm). In short channel devices, the electric field can reach tens of kV/cm, making it necessary to understand the high field transport.

Using 400 μm long conventional Hall bar structures the velocity field characteristics have been reassured.[21] A dc technique below 300 V/cm and a pulsed technique up to 2 kV/cm were used to measure the current vs. field characteristics. Knowing the electron concentration from the same sample by Hall measurements, the electron velocity vs. electric field characteristics were deduced on many modulation doped structures. Above 2 kV/cm the electric field was suspected to be developing non-uniformities as determined by the voltage between equally spaced voltage wings along the sample. Depending on

the low temperature low field mobility of the sample, hot electron effects even at fields as low as 5V/cm have been observed.[22] At very low fields piezo-acoustic phonons and at fields of about 100-200 V/cm, optical phonons are emitted. This leads to electron velocities smaller than predicted by simple extrapolations based on low field mobility.

The velocity vs. field characteristics below 300 V/cm for a typical modulation doped structure intended for FETs is shown in Fig. 7. Also shown are the Monte Carlo calculations performed for lightly doped and ion free bulk GaAs layers. The agreement between the modulation doped structures and undoped GaAs ($N_I \leq 10^{15} cm^{-3}$) is striking. The agreement at low temperatures is even better at high fields as determined from the heterojunction FET performance. It is clear that having electrons but not the donors in concentrations of about $10^{12} cm^{-2}$ in modulation doped structures does not degrade the velocity. The most important aspects of these results can be summarized as:

(i) A quasi-saturation of electron velocities is obtained at field of about 200 V/cm. This implies that the extrememly high electron mobilities obtained at very low electric fields have only a secondary effect on device performance.

(ii) The higher mobilities at low fields help give the device a low saturation voltage and small on-resistance and help enhance its speed during turn-on and turn-off transients.

(iii) Since the properties of the pure GaAs are maintained, electron peak velocities of over 2×10^7 and 3×10^7 cm/s at 300 and 77 K, respectively, can be obtained. These values have already been deduced using drain current vs. gate voltage characteristics of heterojunction FETs.

It can simply be concluded that modulation doped structures provide current transport which is needed to charge and discharge capacitances, without degrading the properties of pure GaAs. To get electrons in conventional structures, the donors have to be incorporated, which degrade the velocity. From the velocity considerations only, these devices offer about 20% improvement at 300 K and about 60% at 77 K. However, other factors, e.g., large current, large transconductance, and low source resistance improve the performance in a real circuit far beyond the aforementioned figures. For small signal operation, e.g. microwave small signal amplifiers, the improvement in the device performance as compared to the conventional bulk FETs may actually be very close to these figures mentioned above.

In the presence of a Schottky gate on AlGaAs the denisty of the 2DEG is approximately described by the modified charge control model.

$$n_s = (\varepsilon/q)[(V_g - V_{off})/(d+\Delta d)] \qquad (7)$$

where $d = d_d + d_i$, where d_d is the thickness of the doped (Al,Ga)As layer, $V_{off} = \phi_b - \frac{1}{q}(\Delta E_c + \Delta E_{FO}) - V_{P2}$ where ϕ_b is the Schottky barrier height, ΔE_{FO} is a temperature dependent parameter.[17,19] $V_{p2} = qN_d d_d^2/2\varepsilon$ and typically ΔE_{FO} is small (of the order of 25 meV). A similar calculation for a Si-SiO_2 interface leads to Δd = 10 Å (compared to Δd = 80 Å for GaAs). This 10 Å correction may not be very important in a typical MOSFET but should be considered when the oxide thickness becomes less than 200 Å.

In Fig. 8, the exact value of interface carrier density (dotted line) is plotted against the applied gate voltage. As can be seen from this figure, the analytical expression (dashed line) eq. (7) is quite good except near the

threshold. The solid line is plotted assuming no dependence of E_F on n_s, i.e. $\Delta d = 0$.[12] Using two-piece and three piece approximations for the velocity-on field characteristics, simple analytical expressions for I-V characteristics which include the source resistance R_s and the drain resistance were developed earlier.[17,19]

V. OPTIMIZATION

In a normally-off heterojunction FET, the type used for the switches in an integrated circuit, a positive gate voltage is applied to turn the device on. The maximum gate voltage is limited to the value above which the doped AlGaAs layer begins to conduct. If exceeded, a conduction path through the AlGaAs layer which has much inferior properties is created leading to reduced performance. This parasitic MESFET for typical parameters becomes noticeable above a gate voltage of about +0.6 V which determines the gate logic swing.[23] Using alternate methods to improve this shortcoming should be very useful.

Since the ultimate speed of a switching device is determined by the transconductance divided by the sum of the gate and interconnect capacitances, the larger the transconductance, the better the speed is. MODFETs, already exhibit larger transconductances because of higher electron velocity and in addition, since the electron gas is located only about 400 Å away from the gate metal, a large concentration of charge can be modulated by small gate voltages. The latter comes at the expense of slightly larger gate capacitance. Considering the interconnect capacitances, any increase in transconductance, even with increased gate capacitance, improves the speed.

The transconductance in these devices can be optimized by reducing the AlGaAs layer thickness. This must accompany increased doping in AlGaAs, which

in turn is limited to about $10^{18}cm^{-3}$ by the requirement for a non-leaky Schottky barrier. By decreasing the undoped setback layer thickness one can not only increase the transconductance, but also the current level (through the increased electron gas concentration). There is, of course, a limit to this process as well because thinner setback layers increase the Coulombic scattering. All things considered, a setback layer thickness of about 20-30 Å appears to be the best at the present. Setback layers less than 20 Å led to much inferior performance. Transconductances of about 225 mSmm (275 being the best) and 400 mS mm gate width have been demonstrated at 300 and 77 K respectively. The current levels of MODFETs also depend strongly on the setback layer thickness and on the doping level in AlGaAs.

For good switching and amplifier devices, a good saturation, low differential conductance in the current saturation region, and a low saturation voltage are needed. These are attained quite well, particularly at 77 K as shown in Fig. 9. The increased current level at 77 K is attributed to the enhancement of electron velocity. The rise in current would have been more if it were not for the shift in the threshold voltage, from about 0 V at 300 K to about $\geq$ 0.1 V at 77 K, which will

The maximum gate voltage $(V')_{g\ max}$ that can be applied, is the pinch off voltage of the 2DEG.

$$(V')_{g\ max} = (V_g - V_{off})_{max} = (V_{po})_{2D} = \frac{q(d+\Delta d)n_s}{\varepsilon} \qquad (8)$$

This together with the 2-piece model leads to the following expressions for the maximum "intrinsic" transconductance $(R_s=0)$[24]

$$(g_m)_{max} = (q\mu n_s Z/L)\ [1+(q\mu n_s(d+\Delta d)/\varepsilon v_s L)^2]^{-1/2} \quad (9)$$

where g_m is the intrinsic transconductance per unit gate length, μ is the low field mobility, v_s is the saturation velocity and

$$d = d_i + [2\varepsilon(V_{Bi} - V_{off})/qN_d]^{1/2} \quad (10)$$

where $V_{Bi} = \phi_b - \Delta E_c/q$ is the effective built-in voltage. One of the consequences of eqs. (9) and (10) is that higher doping of the (Al,Ga)As reduces the minimum thickness of the doped (Al,Ga)As beneath the gate given by the second term in the right side of eq. (10), leading to a higher transconductance.

The results indicate that at small gate lengths the transconductance becomes nearly independent of the gate length due to the velocity saturation. In reality, an additional enhancement of the transconductance in short gate structures is possible due to ballistic effects. For very short gate lengths when

$$q\mu n_s(d + \Delta d)/\varepsilon v_s L >> 1 \quad (11)$$

and one finds $(g_m)^{short}_{max} = \varepsilon v Z_s/(d+\Delta d)$. This expression together with eq. (10) sets an upper limit for the transconductance of short gate heterojunction FETs.

At room temperatuer when μ is only a weak function of d_i, the transconductance should increase both with a decrease in d_i (in agreement with experimental results) and with a decrease in gate length. This reduction in d_i has

two effects. First it increases both the capacitance and transconductance. Second it increases n_s, the maximum voltage swing (eq. (8)), the maximum drain saturation current and $(g_m)_{max}$ through eq. (9).

Assuming V_{Bi} = 0.7 V, Δd = 80 Å and μ = 7000 cm^2/Vs, which is independent of d_i at 300 K (Fig. 10 and reference 24), we calculate $(g_m)_{max}$ as a function of d_i for a 1 μm gate N-off device. The results are shown in Fig. 11. Also shown are the values of the highest intrinsic transconductance obtained in our laboratory[25] at 300 K and 77 K. The transconductance is considerably larger for small values of d_i especially at higher doping levels. This result is in good agreement with the experimental data reported earlier.[26] It should be noted here that the values of transconductance are somewhat overestimated for reasons not underserved yet, although it could possibly due to the uncertainities in AlGaAs thickness under the gate. To some extent the current swing is even more important than the high transconductance in logic devices designed for maximum speed because the current determines the time necessary to charge the effective input capacitance. The maximum current from 2DEG layer is given by

$$(I_{ds})_{max} = qn_{so}v_sZ \qquad (12)$$

Where Z is the width of the device. Using the theory described earlier[17] $(I_{ds})_{max}$ as a function of d_i for 10^{18} cm^{-3} can be calculated. The results of this calculation are shown in Figure 12 where they are compared with the experimental results. As can be seen from the figure the trend in $(I_{ds})_{max}$ variations with d_i seems to agree with the experimental results. However, the calculated values of the current are considerably higher than the experimental

values. One of the reasons for this is that eq. (3) slightly overestimates the measured n_s. perhaps due to an uncertainties in the electron concentrations is the AlGaAs layer some mobility and/or of this discrepancy may also be due to the reduction of the effective saturation velocity at large values of n_s due to the intersubband scattering. As can be seen from eq. (12) the maximum drain current is determined by n_s and v_s independent of the series source resistance, R_s. Thus, more detailed studies of the maximum current may yield important information about n_s and v_s.

The steps to be taken to optimize the heterojunction structure for FETs for logic and microwave applications can be summarized as follows:

(1) Increasing the Al content in the AlGaAs increases both the Schottky barrier height of the gate, and the heterojunction interface barrier. These permit higher forward gate voltages on the device, reduce any hot carrier injection from the GaAs into the AlGaAs, and permit higher electron concentrations in the channel without conduction in the AlGaAs. The concentration of the Al in the AlGaAs should therefore be as high as possible consistent with obtaining low ionization energies for the donors, good ohmic contacts and minimum traps. In present practice it varies from 25% to 30%.

(2) Maximum voltages on the gate, limited by Schottky diode leakage or by conduction in the AlGaAs, are about 0.8 V at room temperature and about 1 V at liquid nitrogen temperature. Threshold voltages should be about 0.1 V for good noise margins and tolerances.

(3) To maximize the transconductance for logic applications, (and dc current, since voltage swings are given) the AlGaAs should be as thin as possible. Thinner AlGaAs implies higher doping, to achieve the desired threshold voltage. Doping levels cannot be larger than about 1 x 10^{18} cm^{-3} because of possibly large gate leakage currents. If one goes ahead with a thin AlGaAs layer without increasing the doping level, the gate built in potential will widen up the triangular potential well and the electrons will not be confined to the heterointerface as shown in Figure 6. When this happens the transconductance near turn on will be very small and non-linear with respect to the gate voltage.

(4) The setback layer should be as narrow as possible without compromising transport properties (20-30 Å) since this gives the minimum total AlGaAs thickness and maximum transconductance consistent with the above limits. Typical parameters for a normally-off device to satisfy these criteria would be: Al concentration of about 30%, AlGaAs thickness of about 350 Å, setback thickness of 30 Å and doping level of about 1 x 10^{18} cm^{-3}.

VI. Performance in Logic Circuits

Interest in the MODFETs was aroused almost immediately after after the first working circuits were built by Fujitsu in 1980, by the (then) record-breaking delays of 17 picoseconds attained by ring oscillators) operating at liquid nitrogen temperature.[27] These results can be explained on the basis of the higher velocities and transconductance, and lower saturation voltages of the device as evidenced from the experimental characteristics.

In the logic application area, using 1μm gate technology and ring oscillators (about 25 stages), Fujitsu in 1982 reported a τ_D = 12.8 ps switching time at 77 K (power consumption not given), Thomson CSF reported 18.4 ps with a power dissipation of P_D = 0.9 mW/stage at 300 K[28] and Bell Labs reported τ_D ~ 23 ps and p ~ 4 mW/stage with 1 μm gate technology.[10] Very recently Rockwell reported a switching speed of 12.2 ps at 300K with 13.6fJ/stage power-delay product.[29] Rockwell also reported a switching speed of 27.3 ps with 3.9 fJ/stage power-speed product. Much improved results of Rockwell can be attributed to the low source resistance, ~ 0.5 Ω-mm, (1-2 Ω-mm typical) obtained.

Modulation doped FETs have recently progressed from no-function circuits, e.g., ring oscillators, to frequency dividers. AT and T Bell Laboratories using a type D flip flop divide-by-two circuit with 1 μm gate technology obtained frequency division at 3.7 GHz (with 2.4 mW/gate power dissipation and 38 ps/fate propagation delay) at 300 K and at 5.9 GHz (with 5.1 mW/gate power dissipation and 18 ps/gate propagation delay) at 77K.[30] Fujitsu has also recently reported results on their master-slave direct coupled flip flop divide-by-two circuit. At 300K and with a dc bias of 1.3 V, input signals with frequencies up to 5.5 GHz were divided by two. At 77 K, the frequency of the input signal could be increased to 8.9 GHz before the divide-by-two function was no longer possible. The dissipation per gate was 3 mW and the dc bias voltage was 0.96 V.[31]

All of the above circuits have used the simple direct-coupled logic circuit family using enhancement-mode driver and depletion-mode loads, or saturated resistor loads. The delay for such a stage is proportional to capacitances and the voltage swing inversely proportional to the current drive.

To achieve high speed we need to develop a high current to voltage ratio. This requires more than just a high transconductance, which is simply the slope of the drain current vs. gate voltage characteristics. The characteristic should also have a sharp knee so that little of the valuable swing is lost traversing the low transconductance knee region. The sharp turn-on of the device maximizes the load current of the NOR gate for a given noise margin and therefore maximizes speed. The maximum transconductance is mainly a function of the saturated carrier velocity, but the sharpness of the knee demands strongly on the lower field part of the velocity vs. field characteristic (as well as on the charge control characteristics as mentioned previously). While the device possesses good high speed characteristics at room temperature, these are enhanced at liquid nitrogen temperature considerably.

Low voltages are the key to low power operation, since the switching energy of the circuit is proportional to CV^2; however operation at low power supply voltages would require a very tight control over turn-on characteristics of the device. Good uniformity of the threshold voltage has been achieved over distances of a few cm., the best number being about a 10 mV standard deviation, achieved by Fujitsu,[31] and 14 mV over a 3" wafer achieved by Honeywell.[32] This control would be sufficient for enhance-deplete logic, if it could be obtained reproducibly.

VII. MICROWAVE PERFORMANCE.

While a great majority of heterojunction related research has so far been directed toward logic applications because of distinct advantages over conventional GaAs MESFETs, promising results in the area of low noise amplifiers have become available. Even though this device is being considered for power

applications as well, its power handling capabilities are limited by the relatively low breakdown of the gate Schottky barrier. Approaches such as the camel gate.[33] which utilizes a p^+/n^+ structure on n-AlGaAs for an increased breakdown voltage will have to be advanced before this device could be a good contender in the power FET area.

In the microwave low noise FET area, using a 0.55 μm gate technology, researches at Thomson CSF obtained noise figures of 1.26,1.7 and 2.25 dB at 10,12,and 17.5 GHz with associated gains of 12, 10.3 and 6.6 dB respectively.[34]The current gain cut-off frequency was about 30 GHz. At cryogenic temperatures, the noise performance is enhanced substantially, well below 0.5 dB. Assigning a hard figure, however, is hampered by the inaccuracy of measurements in that range. Programs are currently being initiated to carefully characterize the noise performance at cryogenic temperatures. If the state of the art source resistance were obtained, almost two-fold improvement over GaAs MESFETs could be expected. Three-stage amplifiers for satellite communications operating at 20 GHz were constructed by the Fujitsu group with a 300 K (L_g = 0.5 μm) overall noise figure of 3.9 dB and gain of 30 dB.[35] It must be pointed out that these results by no means represent the ultimate from these devices. With further improvements in the source resistance, much lower noise figures can be expected. Using very short channel MODFETs with 0.25 μm gate lengths a current cut-off frequency of 45 GHz has recently been reported.[36]

For understanding and modeling the high frequency small signal and large signal performance, an equivalent circuit for the device must be developed.[37] This can be done by, for example, performing microwave S-parameters measurements as a function of bias from which Y-parameters and thus the equivalent

circuit parameters can be calculated.[38,39] Such measurement made between 2 and 18 GHz are shown in Figure 13. One of the most commonly used equivalent circuits for high speed FETs is shown in Figure 14. Additional resistances are to be added to the input and feedback circuit to increase the accuracy in a larger range of frequencies. It should be pointed out that the Y-parameters measurements have so far been made at 300 K. Table 1 shows the values of circuit elements of Figure 14 deduced from 4 GHz measurements for a normally-on 1 μm gate device exhibiting a dc transconductance of 140 mS/mm and source resistance of 1.5 Ωmm. For comparison the results from comparable geometry MESFET are also tabulated.

Measured source and drain resistances (R_s and R_d) include contact resistance, semiconductor resistance between the gate and source or drain contact as well as part of the distributed channel resistance under the gate.[40] Due to variations in the positioning of the gate during fabrication, R_s and R_D values vary among devices but $R_s + R_d$ remains approximately constant. For the bias points listed in Table I corresponding current-gain cutoff and unilateral power-gain cut-off frequencies can be estimated[37] from the equivalent circuit by;

$$f_T = g_{mo}/2\pi C_{gs} \tag{12}$$

$$f_{max} = f_T/\{2[(R_{in} + R_g + R_s)/R_{ds} + 2\pi f_T R_g C_{dg}]^{1/2}\} \tag{13}$$

The resulting current-gain cutoff frequencies are 18 GHz and 14 GHz for the MODFET and MESFET, respectively. The unilateral gain cut-off frequency was 38 GHz for the MODFET and 30 GHz for the MESFET.

The difference in cut-off frequencies between the two devices can be attributed to the larger transconductance in the MODFET. The intrinsic transconductance, g_m, of short gate length FETs operating in the velocity saturated mode[39] is given by the short channel range of eq. (9) as:

$$g_m = \varepsilon v_s Z/W \tag{14}$$

For a MESFET, W is the depletion depth. For a heterojunction, $W = d + \Delta d$ where d is the thickness of the (Al,Ga)As beneath the gate and $\Delta d = 80Å$ is the average effective displacement of the electron gas in the GaAs from the hetero-interface.[19] Because the heterojunction channels are undoped, one expects a higher electron saturation velocity than that in doped GaAs MESFET channels. Furthermore, W in the heterojunction is smaller since the permittivity of both structures is approximately equal, $\varepsilon_r(Al_xGa_{1-x}As)/\varepsilon_0 = 13.2 - 2.8x$. Then by equation (14) all leading to higher intrinsic transconductances in MODFETs. This is evidenced in Figure 15 where small signal transconductances, g_{mo}, is plotted against the gate bias for a drain voltage of 4V.

The sharper pinch-off characteristics of the MODFET is also indicated in Figure 15. For MESFETs, W in Equation (14) increases with bias decreasing g_m. In the heterojunction $W = d + \Delta d$ is independent of bias and g_m is constant until the device is biased close to pinch-off and the approximation $\Delta d \simeq 80$ Å breaks down. The slight increase in g_{mo} at small reverse gate voltages is a result of the parasitic MESFET which arises from parallel conduction in the $Al_xGa_{1-x}As$. Figure 16 presents the input capacitance, C_{gs}, as a function of the gate and drain biases for the MODFET. Theoretically C_{gs} should be chiefly

due to the gate capacitance[41] given by:

$$C_g = \frac{\varepsilon LZ}{W} \tag{15}$$

where L is the gate length. For a MODFET W and therefore C_{gs} is independent of bias expect near pinch-off as shown in Figure 16. This variation may also indicate that C_{gs}, calculated here, merely represents an effective input capacitance. The combined capacitive effects in the input circuit is here termed and modeled as C_{gs} as shown in Figure 14. The large drop in C_{gs} as the gate voltage approaches pinch-off is explained by the widening of the potential well in the undoped GaAs channel near pinch-off as shown in Figure 16.

Combining equations (14) and (15) we obtain for the current-gain cut-off frequency.

$$f_T = v_s/2\pi L \tag{16}$$

Figure 17, which shows f_T and f_{max} versus gate bias for both devices indicates that this is true for the MESFETs. For the MODFET we would have expected f_T to remain constant if the effective input capacitance, C_{gs} were bias independent. The bias variation of C_{gs}, however, results in the bias variations of f_T and f_{max} as depicted in Figure 17.

The feedback capacitance, C_{dg} is mainly due to gate fringing capacitance between the gate and drain. As would be expected, C_{dg} is almost constant with increasing reverse gate bias since the gate fringing capacitance is invariant of gate bias[42,43]. At low drain biases, C_{dg} contains part of C_g as well. However, when the device reaches velocity saturation C_{dg} reflects only the

gate fringe capacitance. This explains the rapid decrease of C_{dg} with increasing drain bias near saturation (Fig. 18). Similar behavior has been reported for GaAs MESFETs[43-45].

Figure 19 shows the output resistance, R_{ds}, of the MODFET versus V_{ds} with gate voltage as a parameter. At low drain voltages R_{ds} fits the theory developed for GaAs FETs[46].

$$R_{ds} \propto V_{ds}(1 - I_d/I_s) \tag{17}$$

Here I_d and I_s are the drain and drain saturation currents, respectively. This dependence upon V_{ds} can be seen in Figure 19 for low drain voltage. In Figure 20 which shows R_{ds} versus I_d it is obvious that the linear dependence on the drain current does not hold over the entire operating range of the device. The nonlinearities may arise from parallel resistance in the substrate. Such behavior has been observed experimentally in MESFETs[42,44] as well. At present it appears that above 60 GHz operation even with sub micron dimensions requires careful analysis and reduction of the feedback capacitance.

VIII. ANOMOLIES IN THE CURRENT-VOLTAGE CHARACTERISTICS

As indicated earlier the devices have the potential for better performance at cryogenic temperatures, however, a peculiar behavior in the drain I-V characteristics of these devices upon cooling to 77K has been observed[47,48]. In particular, when the device is cooled to 77K without exposure to light, the drain I-V characteristics collapse at drain to source voltages less than about 0.5V, while at voltages greater than about 1.0V the characteristics look normal. In addition, a marked reduction in the drain current has been reported

in some devices for large drain biases[49] which was attributed to carrier injection over the barrier.[50]

Modulation doped FET would be of limited value for cryogenic operation if this effect could not be understood and preferably eliminated. By careful control of the fabrication process, and growth conditions it has been shown to be possible to fabricate heterojunction FETs that do not exhibit this effect at cryogenic temperature.[51]

Figure 21 shows a schematic cross section of a fabricated device and also indicates one possible mechanism by which the distortion of the drain I-V characteristics may occur. Since the collapse in the I-V characteristics of MODFETs is observed only after a drain bias greater than 1 V has been applied, it seems likely that the mechanism responsible for the collapse is related to some charge injection/trapping process. Also, since the magnitude of the electric field is largest at the drain end of the channel, the charge injection mechanism would be expected to occur near the drain. Drummond et al.[47] have suggested that the mechanism responsible for the observed effect is due to charge injection and trapping in the bulk $Al_xGa_{1-x}As$ near the drain end of the channel. A similar collapse in the drain current has also been observed in CdSe thin film transistors[52], and in insulated gate (SiO_2) FETs.[53,54]. In both cases, the collapse was attributed to electron trapping in the gate insulator. In the MODFET the depleted $Al_xGa_{1-x}As$ undoubtedly containing a very large concentration of defects can trap the injected electrons.

It is well known that $Al_xGa_{1-x}As$ contains a defect center presumably induced by donors and has quite a large barrier to electron capture and emission at cryogenic temperatures.[55] It is this center which is believed to give rise to the persistent photoconductivity effect in $Al_xGa_{1-x}As$[56] and it is

conceivable that this particular center could capture the electrons injected into the $Al_xGa_{1-x}As$ for a sufficient period of time so as to give rise to the observed phenomenon. When electrons are injected into the $Al_xGa_{1-x}As$ near the drain, the reduction of net positive space charge in the depleted $Al_xGa_{1-x}As$ calls for a smaller two dimensional electron gas (2DEG) concentration in that region. A depleted 2DEG would restrict current flow in the channel. As the drain bias increases, however, the depleted region can be punched through, resulting in the resumption of drain current.

The mechanism is supported by experimental results of Figure 22a where the typical behavior of the collapse of I-V characteristics is shown at 77K. The drain I-V characteristics are shown at room temperature, after cooling to 77K in the dark, and after exposure to light at 77K. Some traces in the I-V characteristics of these devices at low temperature are shown as dashed lines. The larger transconductances achieved at low temperatures lead to bias instabilities due to oscillations caused by parasitics of the TO 18 headers used.

Both of the devices shown in Figure 22 were fabricated from the same epitaxial layer. Once the source and drain ohmic contacts were formed, the wafer was cut in half. On one piece, 1.6 μm long gates were fabricated, while on the other, 1.0 μm gates were fabricated. The gate recess was the same length in both pieces. The characteristics shown in 22b correspond to the device having the 1.6 μm gate length while that in 22a corresponds to the device with the 1.0 μm long gate. The I-V characteristics of the device in 22b demonstrates that is is indeed possible to fabricate FETs whose performance improves substantially when cooled to 77K in the dark. Furthermore, when the characteristics of 22b are compared to those of 22a, it is obvious that at least part of the mechanism responsible for the collapse is related to the

geometry and/or particular fabrication procedures used.

The transconductance of the device in 22b was 170 mS/mm and 280 mS/mm at 300K and 77K respectively. The source resistance of this device estimated from the drain I-V characteristics was about 1.5 Ω mm at 300K and decreased to 0.36 Ω mm at 77K. The value for the source resistance measured by forward biasing the gate with respect to the source and recording the drain voltage while monitoring the gate current was slightly larger than 1 Ω mm at 300K. On the same wafer, using the transmission line method a specific contain resistivity of slightly less than $2x10^{-7}$ Ω cm^2 was measured for this particular structure. This resistivity should be treated with some caution because the sheet resistivity under the contact may be different.

The results of Figure 22 can be understood in light of the phenomenological model outlined above. It has been shown that when the distance between two electrodes is less than about 0.4μ, the surface depletion does not occur to any appreciable extent[57] which has been confirmed in camel diode gate GaAs FETs[58] as well. Since the $Al_xGa_{1-x}As$ is thinner in the gate recess, any surface depletion can extend closer to the 2DEG than in regions away from the gate recess. In addition, this results in lifting the conduction band edge in $Al_xGa_{1-x}As$ with respect to the Fermi level. The entire thickness of the $Al_xGa_{1-x}As$ could in fact be depleted, enhancing the charge trapping mechanism alluded to earlier.

Since little or no effective surface depletion was shown to occur for distances of less than about 0.4μ[57] allows some variation in the positioning of the gate metalization within the recess. As long as the gap in the recess is kept below about 0.4 μm the devices should not show any collapse. The results of Figure 22 support this observation since the only difference

between the device of 22a as opposed to that of 22b is in the size of the gap between the gate metal and edge of the recess. Figure 23 shows the drain I-V characteristics of the device of Figure 22b with the source and drain leads interchanged (inverted). For this particular device, the 1.6 μm gate was not placed in the center of the 2.2 μm long recess. The gap between the edge of the gate metal and gate recess on the drain side was about 0.1 when the device was operated in the normal configuration while that for the inverted configuration was about 0.5μ. The fact that collapse occurred for inverted operation only but not for normal operation further verifies the proposed mechanism. The results of Figure 22 also indicates that the drain I-V distortion in MODFETs is not necessarily related to problems associated with contacting the 2DEG through $Al_xGa_{1-x}As$. The devices of Figure 22 had their source and drain ohmic contacts formed at the same time, yet one exhibited collapse while the other did not.

If indeed the collapse of the drain I-V characteristics at cryogenic temperatures is related to charge trapping in the $Al_xGa_{1-x}As$, the density of defects in the $Al_xGa_{1-x}As$ should have a profound impact on this phenomenon. In order to determine the influence of defect concentration, FETs were fabricated from an epitaxial layer on which several monolayers of Ga had been deposited on half the surface of the substrate prior to the initiation of growth to achieve a varying As vacancy related defect concentration across the wafer. The characteristics shown in Figure 24a correspond to devices taken from areas of wafers with no Ga predeposition, while those of 24b are associated with the area of the wafer with predeposited Ga layer.

The characteristics of Fig. 24a show no collapse, while those of Fig. 24b do show collapse. This demonstrates that the presence of traps plays an

important role in the drain I-V collapse. The characteristics of Figure 24a demonstrate another important feature having to do with the lack of performance enhancement as it is colled to 77K. At room temperature, the transconductance and source resistance were 150 mS/mm and 1.5 Ω mm, respectively. As the device was cooled to 77K in the dark, the transconductance increased slightly to 155 mS/mm but the source resistance increased to about 2 Ω mm. Upon exposure to light, however, the transconductance increased to 315 mS/mm and the source resistance decreased to about 0.5 Ω mm. This demonstrates the importance of eliminating defects and shows that the cryogenic performance of the device is sensitive to the molecular beam epitaxial growth conditions. Since it is well known that ternary compounds such as $Al_xGa_{1-x}As$ are much more sensitive to the growth conditions used than are binaries, the defects are predominantly believed to be associated with $Al_xGa_{1-x}As$.

A further verification of this conclusion was obtained in another experiment in which the group V/III ratio used during the growth of the $Al_xGa_{1-x}As$ was varied from the optimum value (about 5:1) to a much lower value (2:1). The points to be drawn from the results of this series, are that the device performance at room temperature and 77K (dark and light) all degrade as the V/III ratio decreases. This underscores the importance of obtaining the highest possible quality $Al_xGa_{1-x}As$. Another important point is that although the device results degrade with lowering group V/III ratio (and hence AlGaAs quality), the Hall measurements do not necessarily reflect this difference. With the exception of the 77K mobility for the layer grown with the lowest V/III ratio, the Hall data do not vary appreciably from layer to layer. This demonstrates that the Hall mobility of modulation doped layers gives a rather poor indication of device performance. Again the device with the lowest (2:1)

group V/III ratio showed collapse while the others did not.

IX. ADVANCE TECHNOLOGY REQUIREMENTS

In the ultra high speed area, the technology for fabricating submicron gate devices with extremely small source and drain contact resistances must be developed. In order for the heterojunction FET to retain its speed advantages over self aligned gate GaAs FETs[59], a post growth ion implantation and annealing process (Figure 25) must be used. It is then imperative that after annealing the heterojunction structure maintain its electrical properties. Initial furnace annealing studies have revealed an extensive degradation which casts doubt on the development of this important technology.[60] Further investigation with furnace annealing showed that the interfare sheet carrier concentrations must be made very small to reduce degradation[61] (but fails to eliminate it). This is contradictory to the requirements for a fast switching device since large interface electron concentrations are needed.

Using conventional single interface modulation doped structures. Henderson et al.[62] have shown that almost no degradation occurs after flash annealing at 800°C which is sufficient to produce about 80-90% activation in GaAs. In this particular study the samples were flash annealed at T_A = 750°C, 800°C, 850°C, and 900°C in a commercially available annealing apparatus in an inert atmosphere of 3% H_2 in Ar, and in contact with an undoped GaAs wafer to minimize As desorption. A similar technique has been shown[63] to yield an activation efficiency of > 90% in Zn-implanted bulk GaAs at T_A = 800°C.

The results of Hall mobility and sheet carrier concentration measurements are presented in Figure 26. Note that while in both instances annealing at 800°C preserves over 85% of the virgin 77K mobility, n_s at 77K is reduced 25%

in layer A, but remains virtually unaffected in layer B. Layer A consisted of a 1.0 μm GaAs buffer layer beneath a 30 Å undoped AlGaAs setback layer topped with a 400 Å n-AlGaAs layer which is then capped with 200 Å n-GaAs. The thicknesses in layer B were 3.0 μm, 30 Å, 600 Å and 50 Å respectively. Diffusion of Si from the doped AlGaAs layer can be ruled out on two premises: (i) insufficient time at elevated temperature and (ii) the more heavily doped layer is less affected with the same undoped layer thickness. the remaining plausible mechanisms are As desorption, diffusion of impurities from the substrate and site transfer of the amphoteric Si dopant in the doped AlGaAs layer.

The structure of layer A is more susceptible to surface As desorption due to the thinner AlGaAs layer. While the unperturbed mobilities indicate that desorption does not reach the 2DEG, it is possible that the doped AlGaAs layer is affected. Due to the greater electronegativity of Al with respect to Ga, As is expected to desorb more readily from GaAs than AlGaAs, so if the GaAs cap layers are rapidly depleted of As, then the depth of As desorption may be greater in layer A. It is also likely that even Si with its small diffusion constant can diffuse through the 30 Å set back layer above 850°C degrading the mobility of the 2 DEG. Alternatively, if highly diffusive impurities stream from the substrate at nearly 1000 Å/s, traps could form in the channel that may reduce n_s. This explanation, however, is not consistent with the high mobilities obtained, nor is it likely that impurities could diffuse nearly one micron in several seconds at 700°C. Even at high annealing temperatures where degraded mobilities point to imperfections in the 2DEG region, surface desorption and site transfer seem the more likely mechanisms.

The photoluminescence spectra reproduced in Figures 27 and 28 exhibit trends similar to those observed in the Hall data. Both samples display an overall decrease in integrated PL intensity as T_A increases, except that the control from layer B produced weak luminescence, possibly due to misalignment during measurement. Deterioration of the GaAs buffer at higher T_A is evidenced by broadening of the exciton lines and an increase in the ratio of intensities of peaks associated with defects[64] (d,X) with respect to the free exciton (F,X) line. It should be pointed out though recent result on high purity samples indicate what previously thought to be (d,X)[64] lines may actually be associated with donor-acceptor pairs.[65]

The difference in the deterioration of the optical properties of the two layers is again one of degree. The overall similarity of PL spectra from samples annealed at $750^{o}C$ and $800^{o}C$ to their respective controls supports the conclusion that decreases in n_s stem from either As depletion or site transfer of the amphoteric Si dopant in the doped AlGaAs layer rather than deterioration of the GaAs itself. The decrease in intensity of exciton lies is due to and correlates well with the decrease in n_s: in layer A as T_A increases from $750^{o}C$ to $800^{o}C$, $\Delta n_s = 16\%$ while $\Delta(F,X) = 28\%$; in layer B as T_A increases from $750^{o}C$ to $800^{o}C$, $\Delta n_s = 1\%$ while $\Delta(F,X) = 1.5\%$.

Despite the fact that some degradation is observed in transient annealed modulation doped heterostructures at the higher end of the temperature range, the results of this experiment are quite promising and demonstrate that the modulation doped structures can withstand the annealing process that makes 90% implant activation possible in GaAs, and retain over 95% of the virgin mobility and sheet carrier concentration. The successful results reported here serve to remove a significant obstacle on the path to a new generation of

ultrafast, heterojunction FET-based circuits.

X. REMAINING PROBLEMS AND PROJECTIONS

Since the AlGaAs/GaAs heterojunction FETs are large current and small voltage devices, the saturation voltage and transconductance are very sensitive to the contact resistance. In fact, the higher the transconductance the more severe the effect of the source resistance becomes. In order to fully take advantage of the device potential it is essential that extremely low contact resistances be obtained. Not only the contact resistance but parasitic resistances such as the source and drain semiconductor access resistance must be minimized. This could be done using the gate as an ion implantation mask to increase the conductance on each side of the gate as described in section IX. In some prototype devices this technique has successfully been applied but high speed results are not yet available.[66] Currently many laboratories, both university and industrial, are looking into the degradation mechanism occurring during the annealing step. Although preliminary, the transient annealing technique looks very promising in this regard.

Modulation doped structures also suffer from the persistent photoconductivity (PPC) effect below 100 K.[67] This is believed to be the result of donor induced defects in AlGaAs which once ionized exhibit a repulsion towards capture. Recent results, however, appear to indicate that defect related processes in GaAs as well can play an important role.[68] As a result, increased carrier concentrations, which persist unless the sample is warmed up, are obtained. The electron mobility too, increases with illumination in samples with low areal carrier density. This is tentatively attributed to perhaps neutralizing some defect centers in the depleted AlGaAs near the

hetero-interface which then do not cause as much scattering. This PPC effect has been shown to decrease when the AlGaAs layer is grown at high substrate temperatures.[69] It should be pointed out that using As_2 dimeric source, modulation doped structures with minimal light sensitivity have been grown.

For the most part the hetero-interface is almost perfect in that the interface states encountered in Si MOSFET do not occur. However, the AlGaAs layer contains a large concentration of traps which can give rise to threshold voltage shifts with temperature and perhaps with time. Temperature dependence of the threshold voltage in long gate FET has been studied in detail[70] which show a positive shift as the temperature is lowered. Part of this threshold shift can be attributed to freez out of electrons to relatively deep donor level in AlGaAs. Since the AlGaAs under the gate is thicker in normally-on devices, the voltage shift as compared to normally-off devices is much larger. The emission time from the traps is dependent exponentionally on the sum of trap level and the barrier against emission. This barrier against emission may be obtained from transient gate capacitance measurements as reported earlier.[70] Highly non exponential time response of the gate capacitance to a gate voltage pulse was found to be indicative of time dependent threshold voltage resulting from the change of trap occupation. In addition, from the temperature dependence of the threshold voltage donor traps were found to be 42 meV below the conduction band edge with 30% Al mole fraction. The value of the thermal activation energy for emission from the traps is estimated to be 450 meV. The density of the native traps and donor induced traps in AlGaAs can be quite comparable to the electron concentration which makes the deep level analysis by transient capacitance somewhat difficult. Alternate studies such as the drain current transient can be used in FETs to

deduce similar information when large trap concentrations are encountered.[71] Again recent results obtained in our laboratory show that the threshold voltage shift when the device is cooled to 77K is much less than 0.1V.

The drain current response to a gate bias with varying temperature can be used to calculate the activation energies of the traps as well. With this method an activation energy of 0.47 eV was deduced for 30% Al mole fraction which is good agreement with the data obtained from transient capacitance measurements.[70] In addition, other techniques such as low frequency generation recombination noise characteristics of MODFETs can be used to characterize deep levels at the hetero-interface.[72] The generation-recombination noise is a result of fluctuations in the number of electrons,[73] in this case number of electrons at the hetero-interface trapped by defects located in the forbidden band of AlGaAs. Using the low frequency noise characteristics of FETs measured in a frequency range of 1Hz-25KHz and a temperature range of 100-400K, four deep levels at 0.4, 0.42, 0.54 and 0.6 eV below the conduction band were detected.[74] These energy levels are in a general agreement with those deduced from deep level transient spectroscopy performed in bulk AlGaAs,[75] which indicate the presence of deep levels. There are some discrepencies among the results of deep level transient spectroscopy in bulk AlGaAs performed at various laboratories as well. The details of deep level study is beyond the scope of this text and will not be covered here.

It is obvious that the defects associated with the AlGaAs must be minimized so that their influence on device performance is not noticeable. Realizing the importance of the issue, many reseachers are looking into sources and causes of the traps and electronic defects in AlGaAs. Modulation doped FETs in contrast to injection lasers, are the first devices utilizing AlGaAs where

charge and defect concentrations of about $10^{11}cm^{-2}$ can give rise to unacceptable adverse effects on the device performance. There are also efforts to explore device structures that are not very sensitive to at least some of the obstacles discussed above.

The questions of yield and reliability may, however, take a little longer to resolve. For yield, the processing philosophy with regard to GaAs must change. Instrumentation, care and environment similar to that used for Si ICs must be implemented. There is also the question of epi defects either introduced by the epi process or present on substrates. Some of these are morphological defects which not only degrade the semiconductor but also cause processing defects. The present state of the art of molecular beam epitaxy when used with average GaAs substrates is such that only MSI circuits with some success in terms of yield maybe possible. There are already encouraging results which tend to suggest that by the latter part of the decade the substrate quality, the epi morphological quality, the processing that introduces few defects and thus functional circuits with active elements in the mid to upper thousands may be possible.

Like that of MESFETs, the threshold voltage of FETs is very sensitive to the epi properties. For a normally-off device, a thickness control to about 2 monolayers (~ 5Å) and doping control and AlAs mole fraction control of about 1% are needed to control the threshold voltage within about 10 mV. Controls like this have already, though occasionally, been obtained on wafers slightly less than 3" in diameter.[32] The repeatability of this technology is one of the questions that is also being addressed. Perhaps the most difficult problem is to prepare AlGaAs of the quality with defect and trap concentration of $10^{14}cm^{-3}$ as compared to the present concentration of high $10^{15}cm^{-3}$. Again

more effort and time will undoubtedly result in substantial reductions in the defect concentration.

Finally, it is clear that this device has many of the attributes required by high speed devices particularly those of the integrated circuits. Present results with moderate devices are very encouraging and with more effort even better results are expected. In fact, the MODFETs with only 1 μm gate length and 3μm source-drain spacing have surpassed the performance of other techniques, e.g. conventional GaAs with sub 0.5μm dimensions as shown in Fig. 29. It should be kept in mind that the delay times shown in Fig. 29 would increase by a factor of about 3 in a real circuit with loaded gates. Nevertheless, the MODFET is capable of providing functional operations in a large system by at least a factor of 10 faster than the current state of the art. With more advanced fabrication technologies, even better performance can be expected.

Acknowledgments

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Figure Captions

Fig. 1. Since interface heterostructures used for heterojunction FETs. The structure with AlGaAs grown on top of GaAs, "normal modulation doped structure," is the one that is used commonly for FETs. The diagram on the right hand side shows the conduction band edge with respect to distance. When the order of growth is inverted, (bottom sketch, doped AlGaAs first), the interface quality is not sufficiently good to provide enhanced device performance. The realtively small surface mobility of Al is thought to lead to degraded interface in the inverted structure.

Fig. 2. Cross-sectional view of a MODFET commonly used. Alloyed contacts, e.g. AuGe/Ni/Au diffuse past the interface forming contacts to the two dimensional electron gas.

Fig. 3. Top view of a fabricated device intented for microwave applicatins and having a 3 μm x 290 μm. For logic circuis the gate width is reduced to 20 μm to minimize the real estate and power consumption.

Fig. 4. Variation of the electron gas density with Fermi level as measured from the bottom of the conduction band in GaAs. Since the conduction band density of states in si is very large, the Fermi level even for the largest sheet carrier concentration, 2×10^{12} cm^{-2}, is still below the conduction band and predictions are reasonably accurate when the problem is treated like three dimensinal (3D) and the quantization is neglected. For GaAs, however, the density of states is smaller (or the effective mass is smaller) and the quantization of the electron population at the hterointerface can not be

neglected. Models encompassing the two diemsional (2D), solid lines, nature of the electron population must be utlizied.

Fig. 5. Interface carrier density, n_s as a function of doping density, N_d, with various undoped (Al,Ga)As layer thicknesses. The dotted line is the exact slutin and the solid line is the analytical expression, eq. (3).

Fig. 6. Effecitve position of the two dimensional electron gas from the hetero-interface, Δd vs. gate bias.

Fig. 7. Velocity versus electric field measured in a single interface modulation doped structure at 300 and 77 K. The electron gas concentration at the heterointerface is about 7×10^{11} cm^{-3} and the unitnentional background acceptor concentration in GaAs of the modulation doped structure is about 10^{14} cm^{-3}. For comparison, calculated velocity field characteristics of bulk GaAs with zero ionized impurity density ($N_I = 0$) at 300 K and at 77 K and with $N_I = 10^{15}$ cm^{-3} at 77 K are also shown. It is clearly seen that at 300 K, transport properties of the modulation doped structure with as many electrons as needed for FETs is comparable to the pure GaAs. At 77 K it is almost comparable to pure GaAs at fields below 300 V/cm and quite comparable at 2 kV/cm and above (estimated from FET performance).

Fig. 8. Interface carrier density vs. voltage difference between gate and channel (V_{off} = 0.15 V and d = 400 Å). The slid line is the simple charge control model proposed in reference 12, the dotted line is the numerical exact solution and the dashed line is the analytical model of reference 19.

Fig. 9. Drain I-V characteristic of a MODFET with a 300 μm gate width at 300 and 77 K. As indicated, the extrinsic transconductance increases from about 225 (best 275 mS/mm) to 400 mS/mm) to 400 mS/mm as the device is colled to 77 K. The improvement in the drain current observed at 77 K could be much larger if it were not for the positive shift in the threshold voltage. This sift is attributed to defects in AlGaAs and is a subject of current research.

Fig. 10. Measured, deduced and calculated two dimensional electron mobility at 300 K vs the set back layer thickness. Extremely good agreement is obtained when the effect of parallel conduction through AlGaAs on the mobility is accounted for.

Fig. 11. Since the transconductance is inversely proportional to the gate to electron gas separation, the undoped AlGaAs layer at the heterointerface can influence the transconductance substantially. Considiering that the gate to elctron gas distance is about 300 Å, an undoped layer thickness of greater than 100 Å can have a dramatic influence on the transconductance. For best resutls an undopd layer thickness of about 20-30 Å must be used. This imposes stringent requirements on the epitaxial growth process and only molecular beam epitaxy has so far been able to produce such structures. The circles above are the experimental data points wile te solid line shows the theory. Below 20 Å, the performance degrades.

Fig. 12. Maximum drain current is also very sensitive to the undoped AlGaAs layer thickness. For desired large current levels a smaller electron-donor separation is needed to yield a large electron gas concentration. The available data otained in N-on FETs while

showing the general trends, should be augmented with more experiments. Maximum current levels of about 300 mA (per millimeter of gate width) at 300 K in N-on FETs with a 1 μm gate length is possible. Large current levels obtainable at low voltages lead to fast switching speeds with low power dissipation.

Fig. 13. Scattering parameters measured as a function of frequency (data) at V_{gs} = 0V and V_{ds} = 2.5V for a normally as FET. The outer circle correspond to 1 for S_{11} and S_{22}, 5 for S_{21} and 0.2 for S_{12} respecitvely. The calculated S parameters using the equivalent circuit of Fig. 14 are also shown (solid lines).

Fig. 14. Equivalent circuit parameters calculted from y-parameters which in turn are calculated from S-parameters.

Fig. 15. Small signal transconductance calculated from y_{21} at 4 GHz of a MODFET and conventional MESFET vs the gate bias normalized with respect to the pinch-off volage and to 1 mm of gate width. The fact that the transconductance of the heterojunction FET stays high for about half the gate bias range supports the theory presented.

Fig. 16. The variation of the gate capacitance with the gate bias in a conventional MESFET and a MODFET. Again invariance away from the pinch-off is characteristic of the MODFET.

Fig. 17. Current-gain cutoff frequency, f_t, and unilateral power-gain frequency, f_{max}, for a MODFET and MESFETs (in GHz) versus gate bias normalized to pinch-off.

Fig. 18. Feedback capacitance for a MODFET versus V_{ds} with V_{gs} as a parameter in pF per mm gate width.

Fig. 19. Output resistance for a MODFET versus V_{ds} with V_{gs} as a parameter in Ω mm.

Fig. 20. Output resistance for a MODFET as a function of drain current in Ω mm.

Fig. 21. Schematic cross section of a MODFET indicating a possible mechanism by which I-V collapse occurs.

Fig. 22. Current-Voltage chracteristics from two devices, one with 1.0 μm long gates (shown in a) and one with 1.6 μm long gates (shown in b). The gate recess was the same length in both devices. The step size was + 0.2 V for all characteristics. Some of the traces at 77 K are shown as dashed lies because of oscillations.

Fig. 23. Drain I-V characteristic from the device of Figure 22b with source and rain leads interchanged.

Fig. 24. Drain current-voltage characteristics from two device staken from a layer in which about 1 monolayer of Ga was predeposited to study the effect of traps. The characteristics shown in (a) are from a device with a smaller amount of predeposted Ga and those in (b) are from one with a larger amount.

Fig. 25. Cross-sectional view of a self aligned modulation doped MODFET where the T shaped gate is used as a self aligned n^+-implantation mask. The gate metal in contact with the semiconductor is a refractory material and the cap on it may or may not be left in place depending on whether or not it tolerates the annealing process.

Fig. 26. The sheet electron areal density and the electron mobilty at 77 K of modulation doped heterostructures flash annealed between 750 and

900°C.

Fig. 27. Low temperature photoluminescence spectra obtained from layer A after flash annealing between 750 and 900°C.

Fig. 28. Low temperature photoluminscence obtaied in layer B following flash annealing at temperatures between 750 and 900°C.

Fig. 29. Experimental performance, points, and projected performance of 1μm gate MODFET in a highly optimized inverter chain (ring oscillator). The performance of other devices are also shown.

Table I. Heterojunction FET and MESFET small signal equivalent circuit values for the circuit of Fig. 14. The values are normalized to 1 mm of gate width with the exception of gate resistance, R_g.

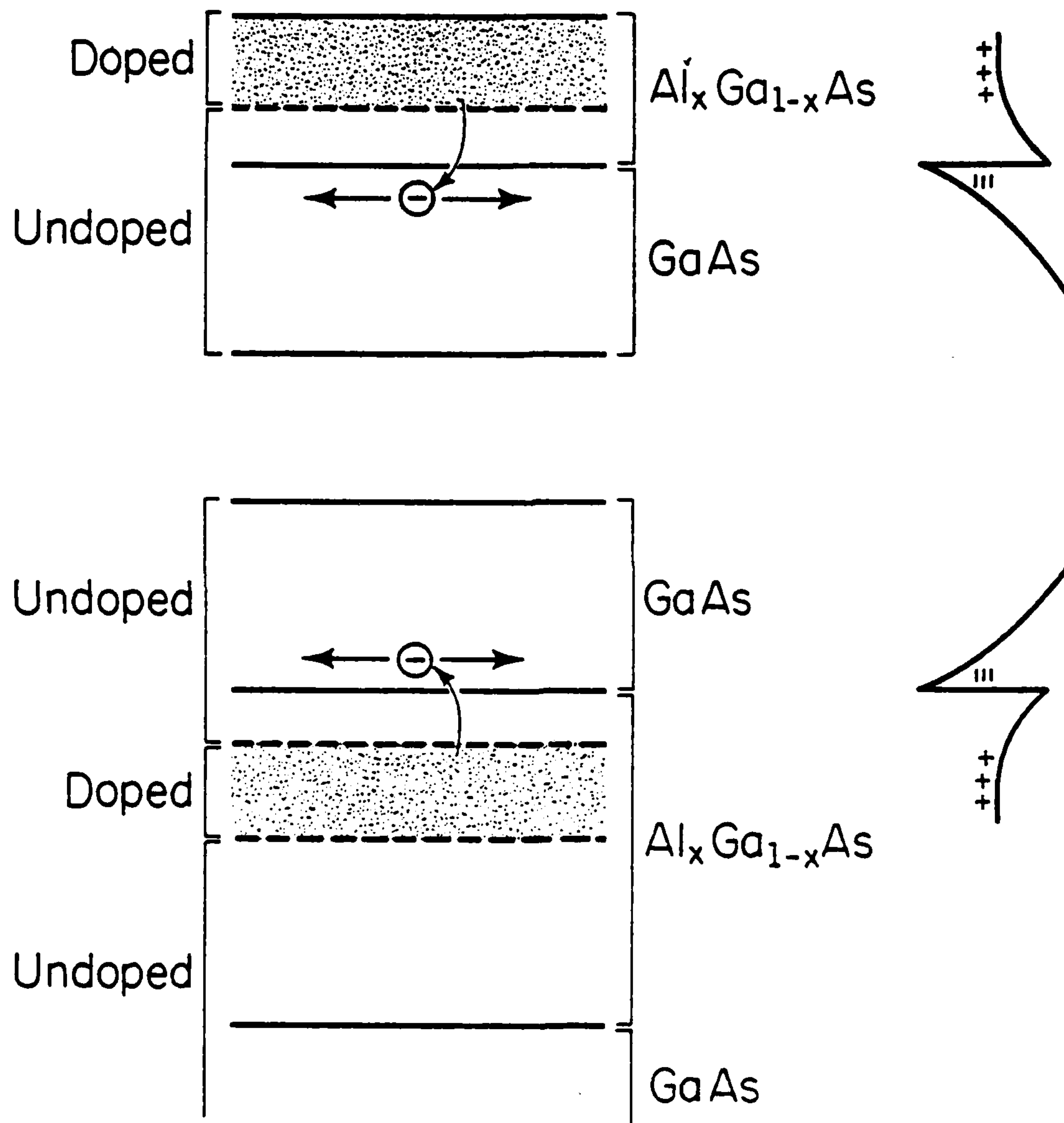


Fig. 1

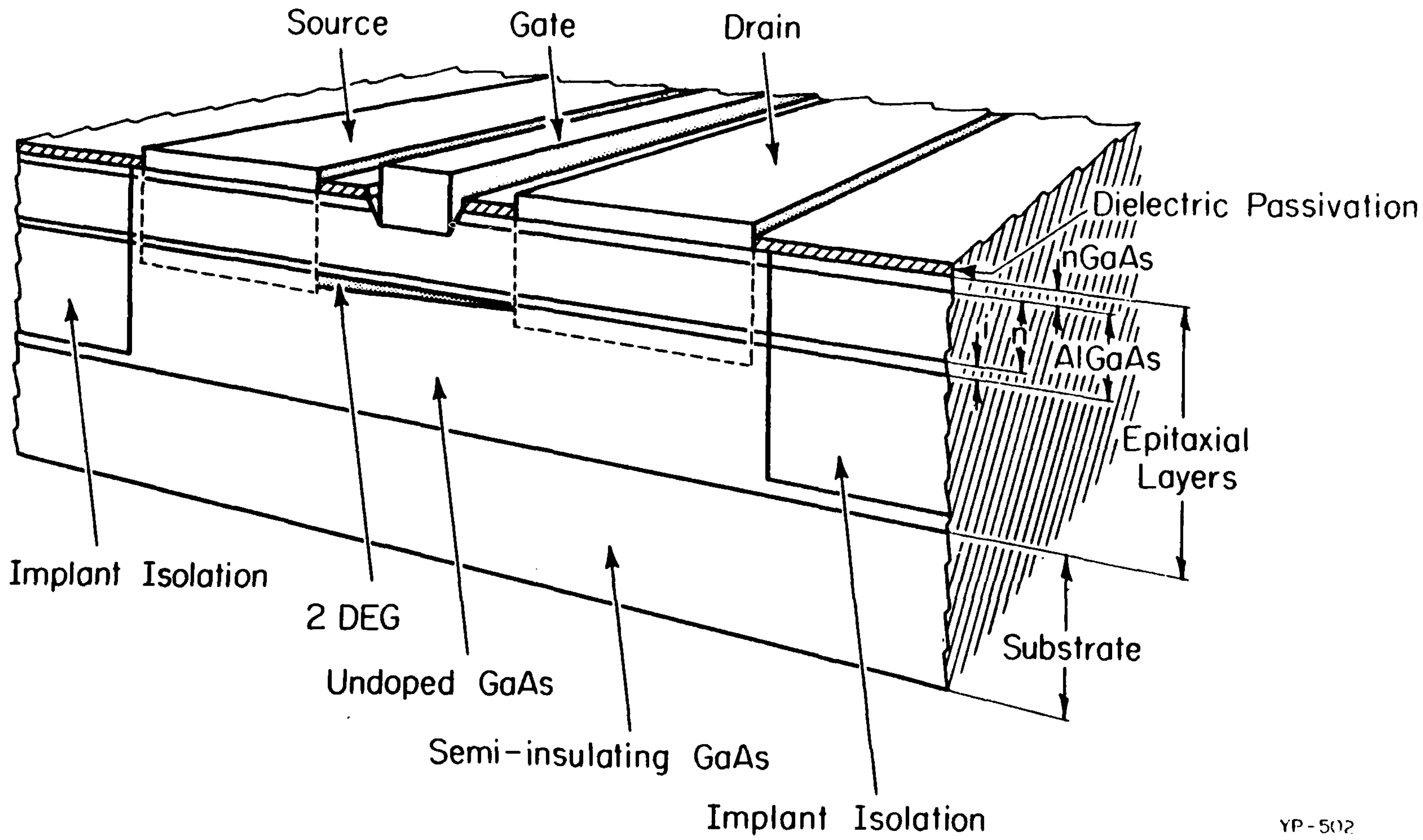
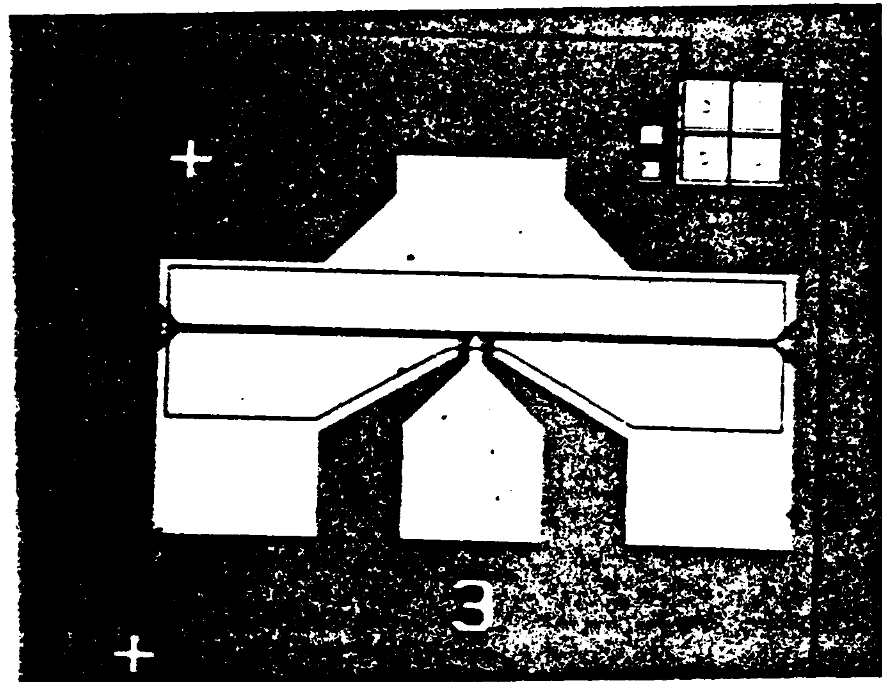


Fig. 2



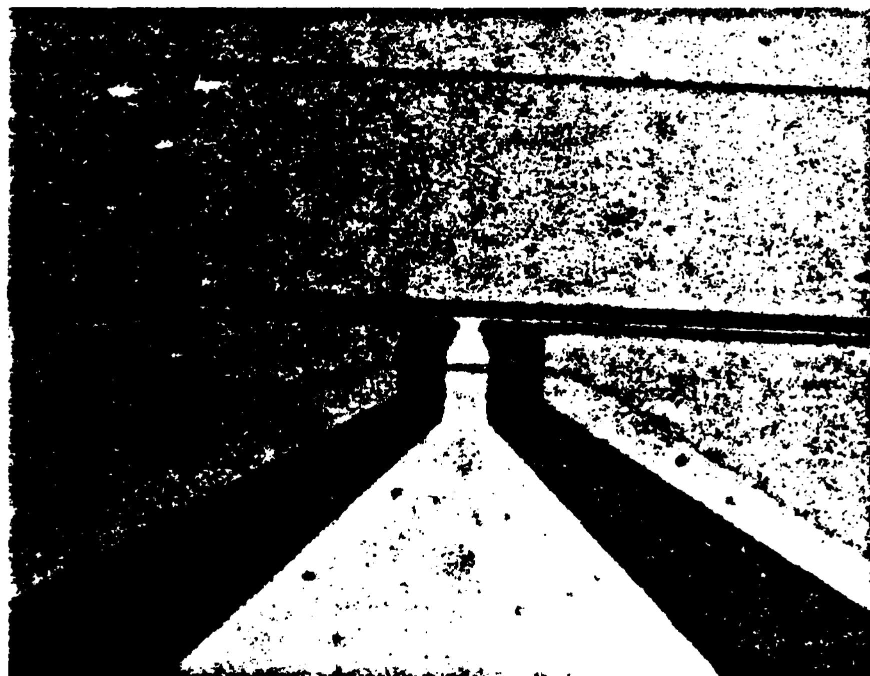


Fig. 3.

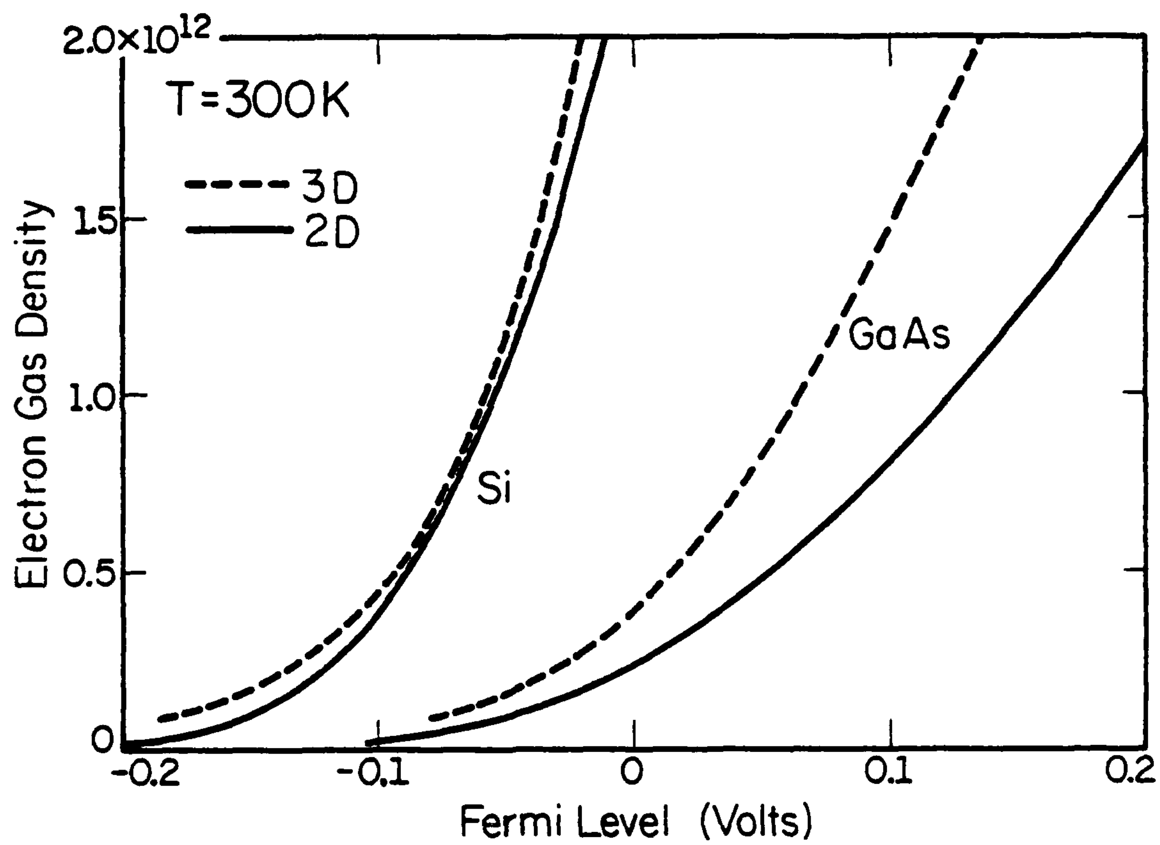


Fig. 4

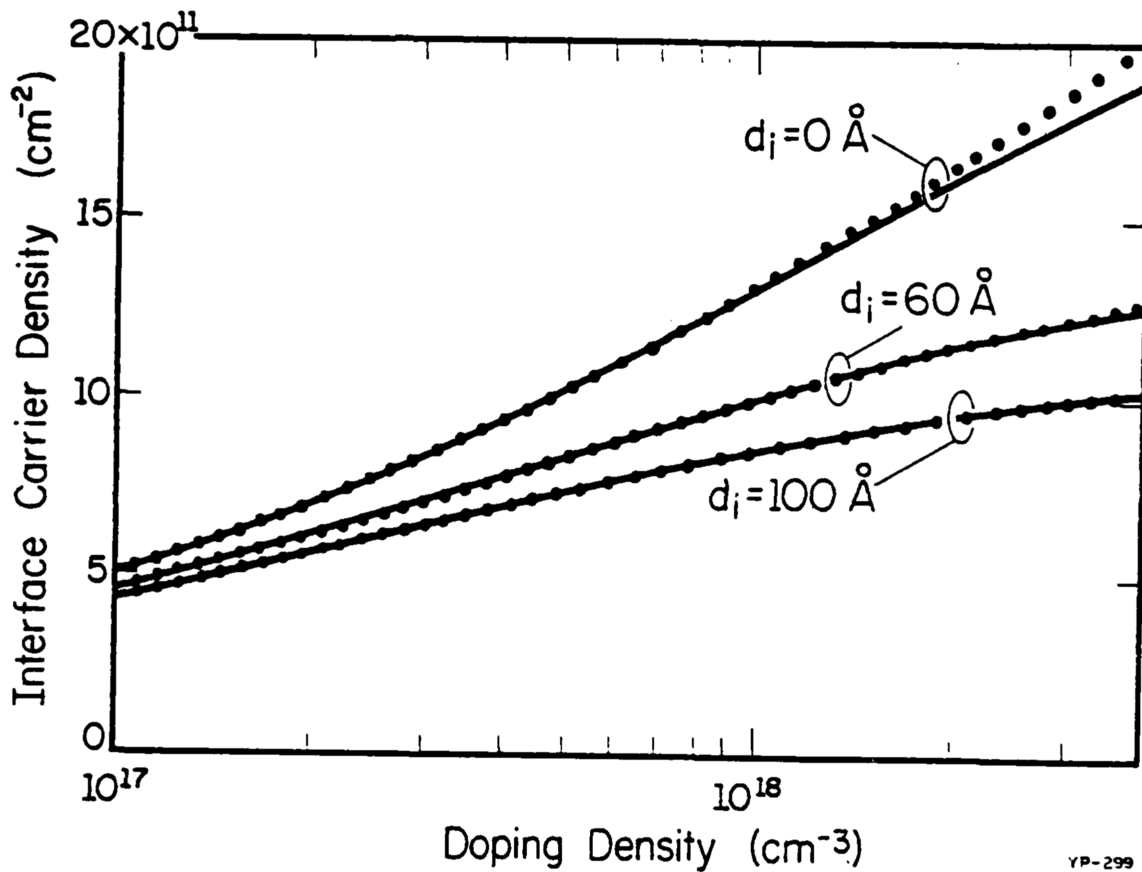


Fig 5

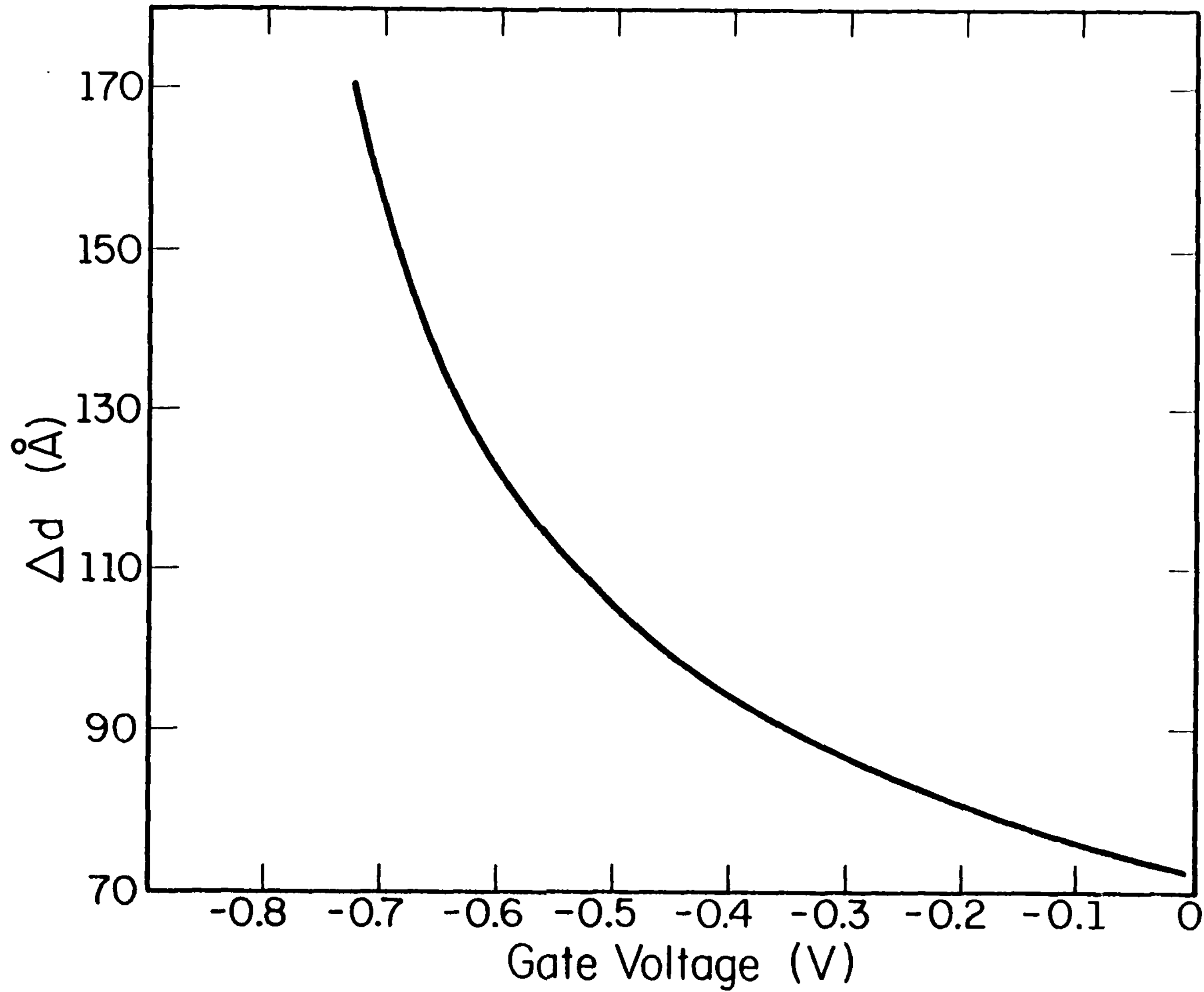
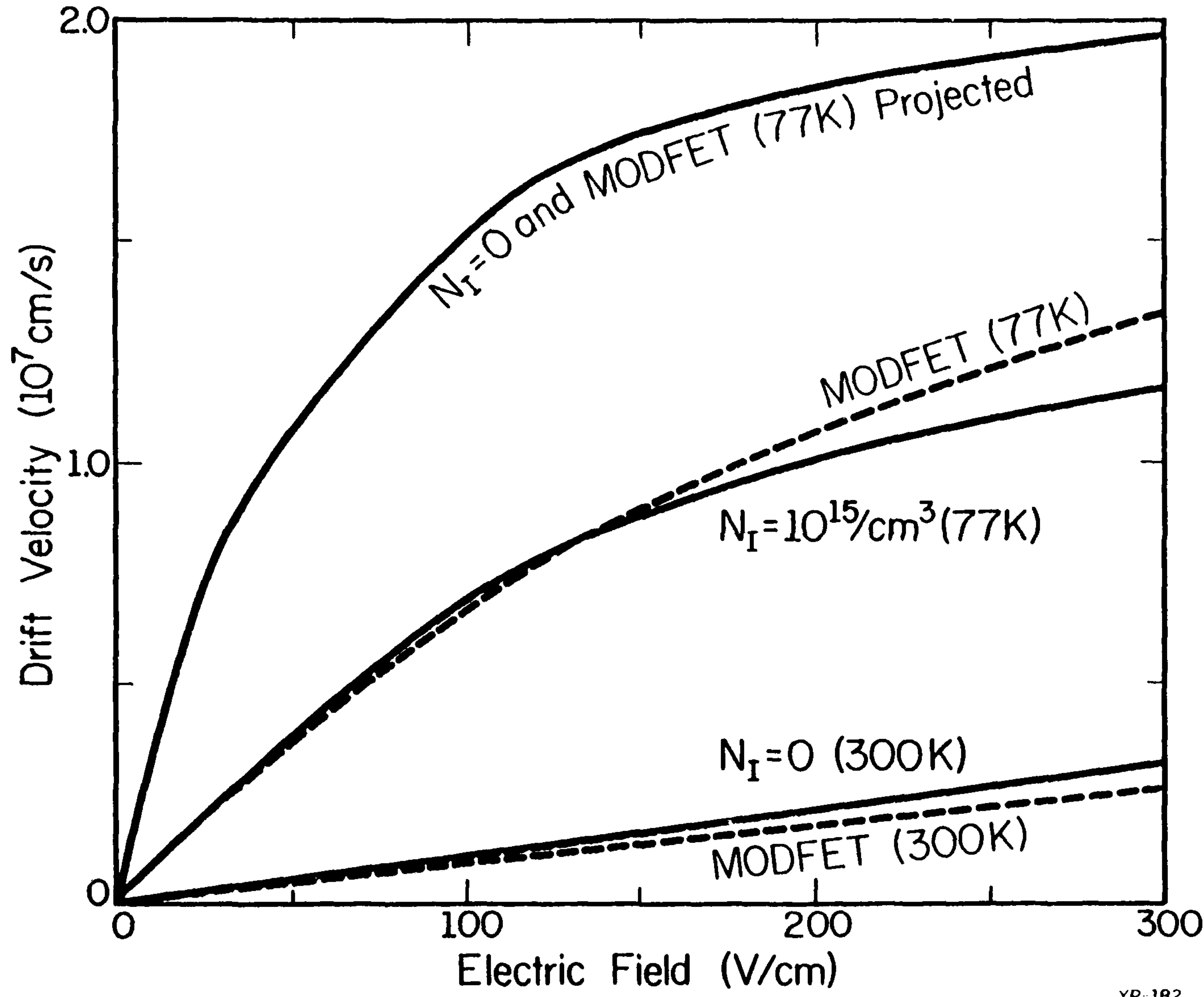


Fig. 6



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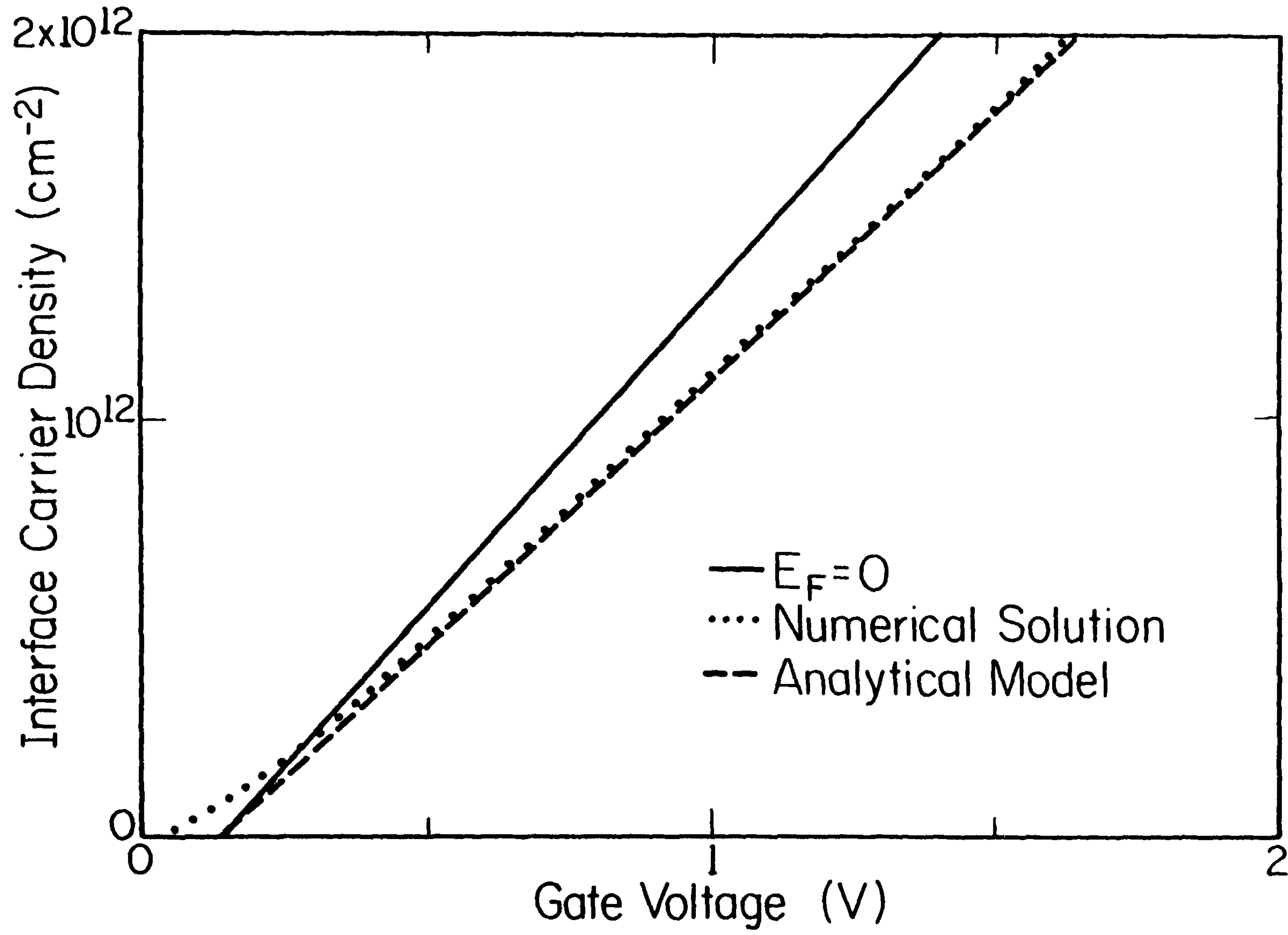

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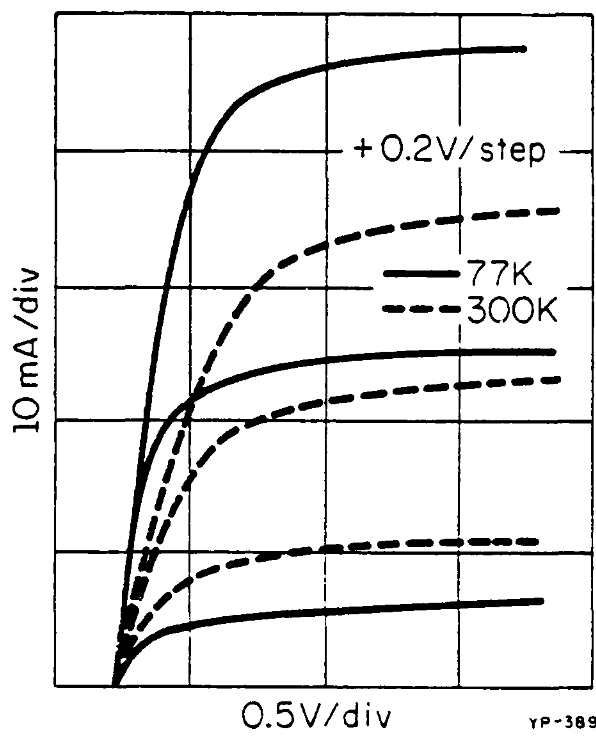

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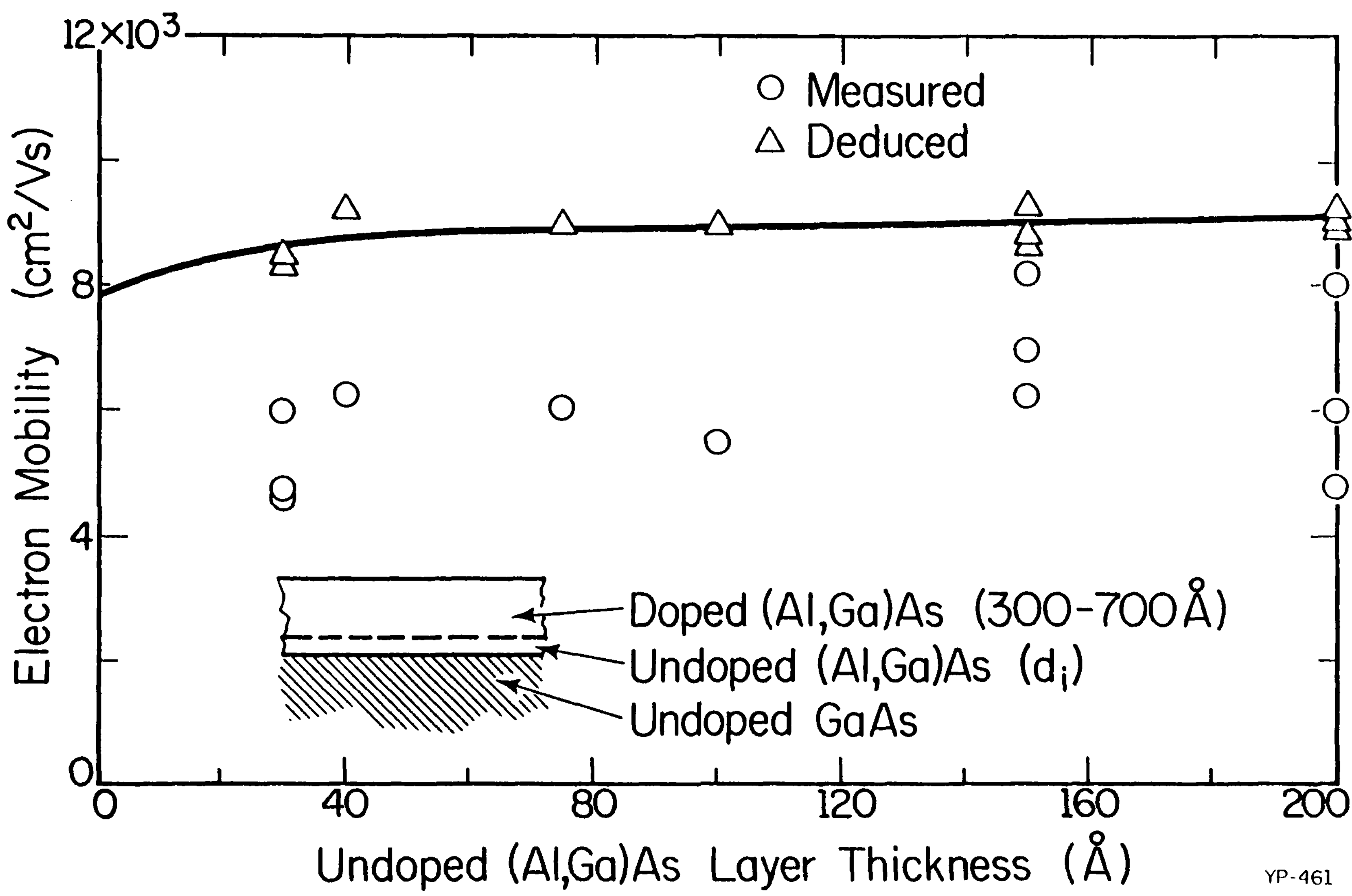

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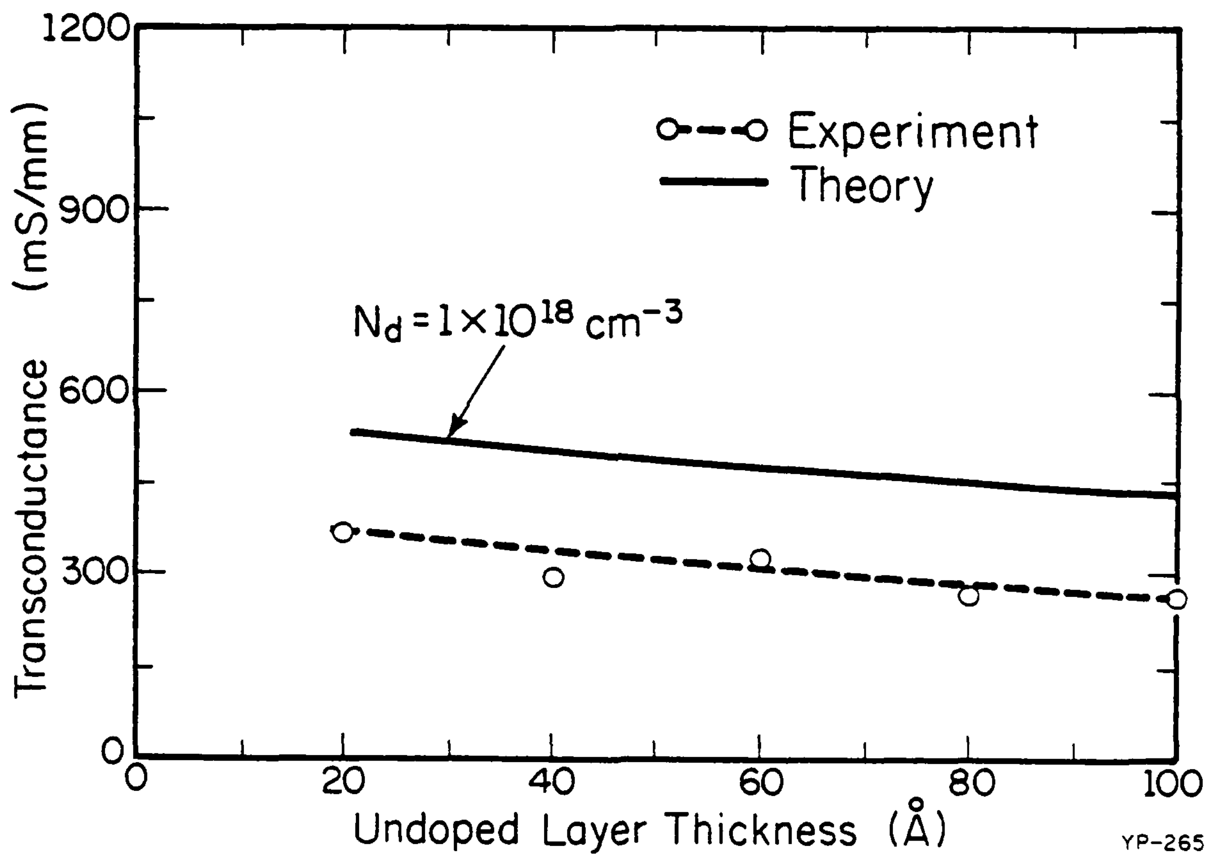

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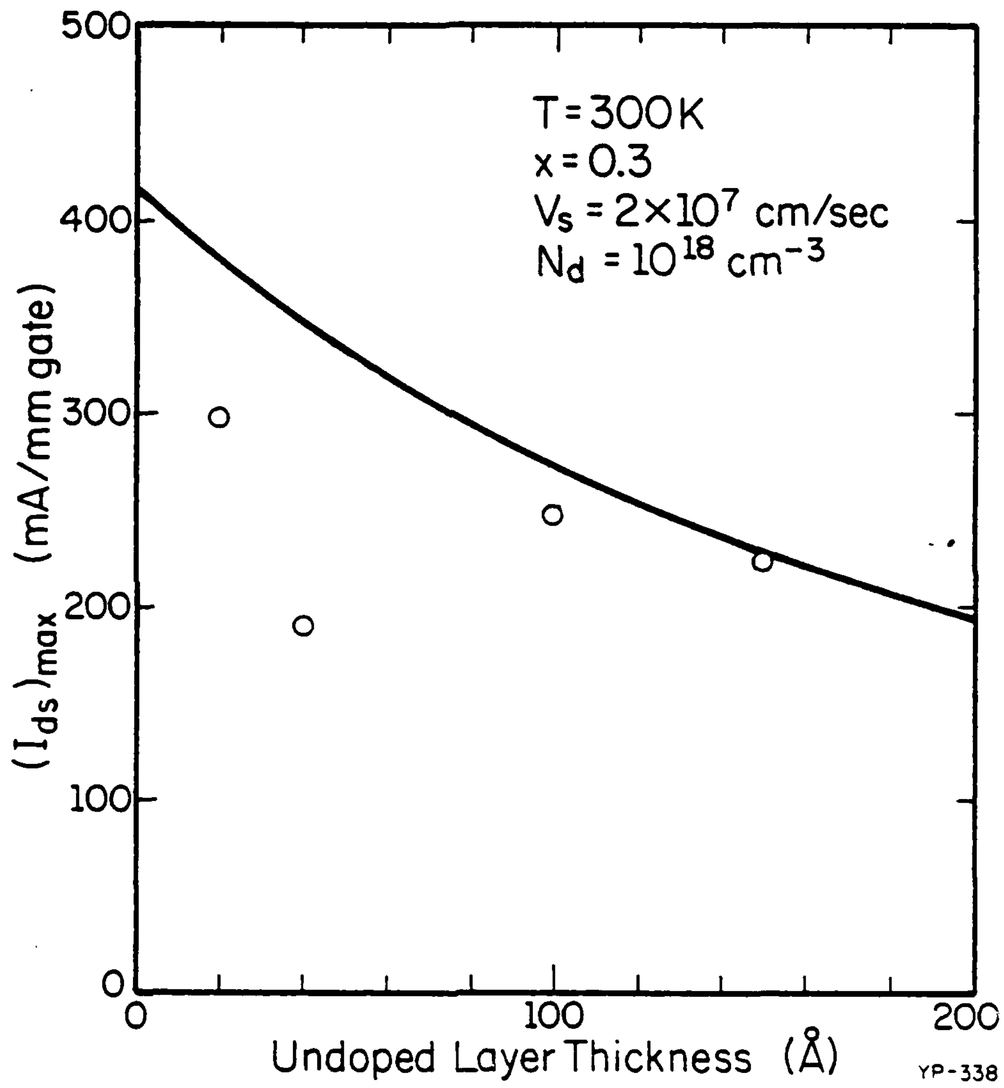

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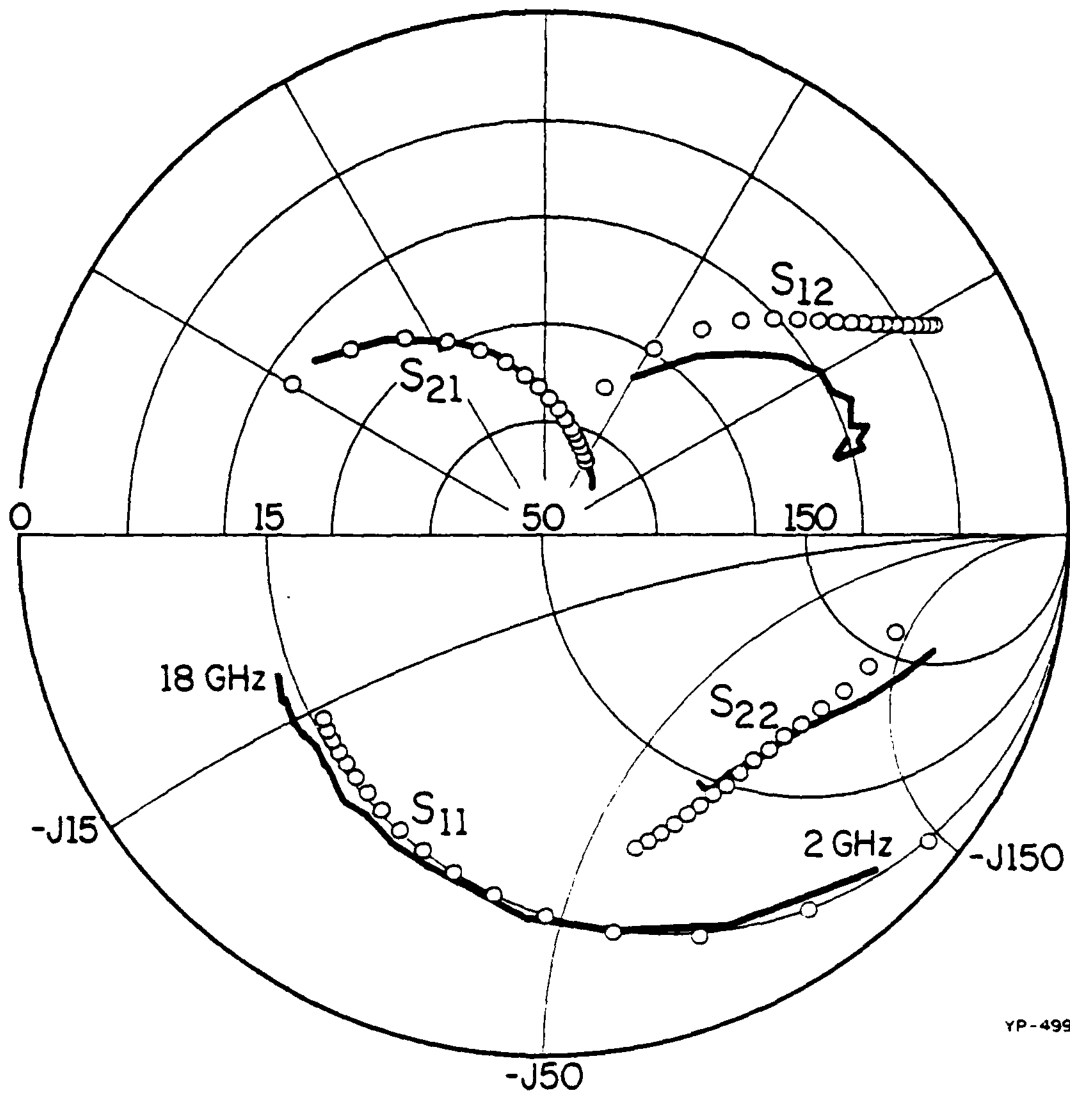

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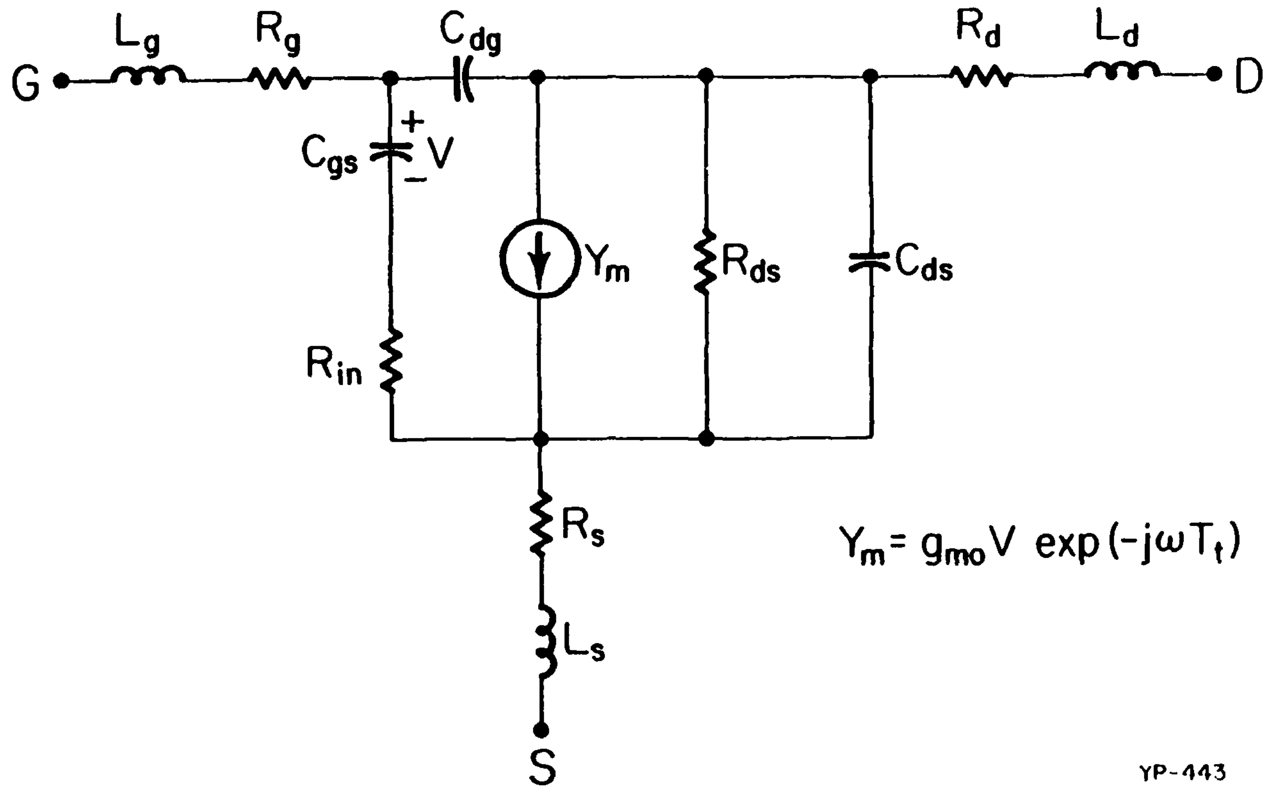

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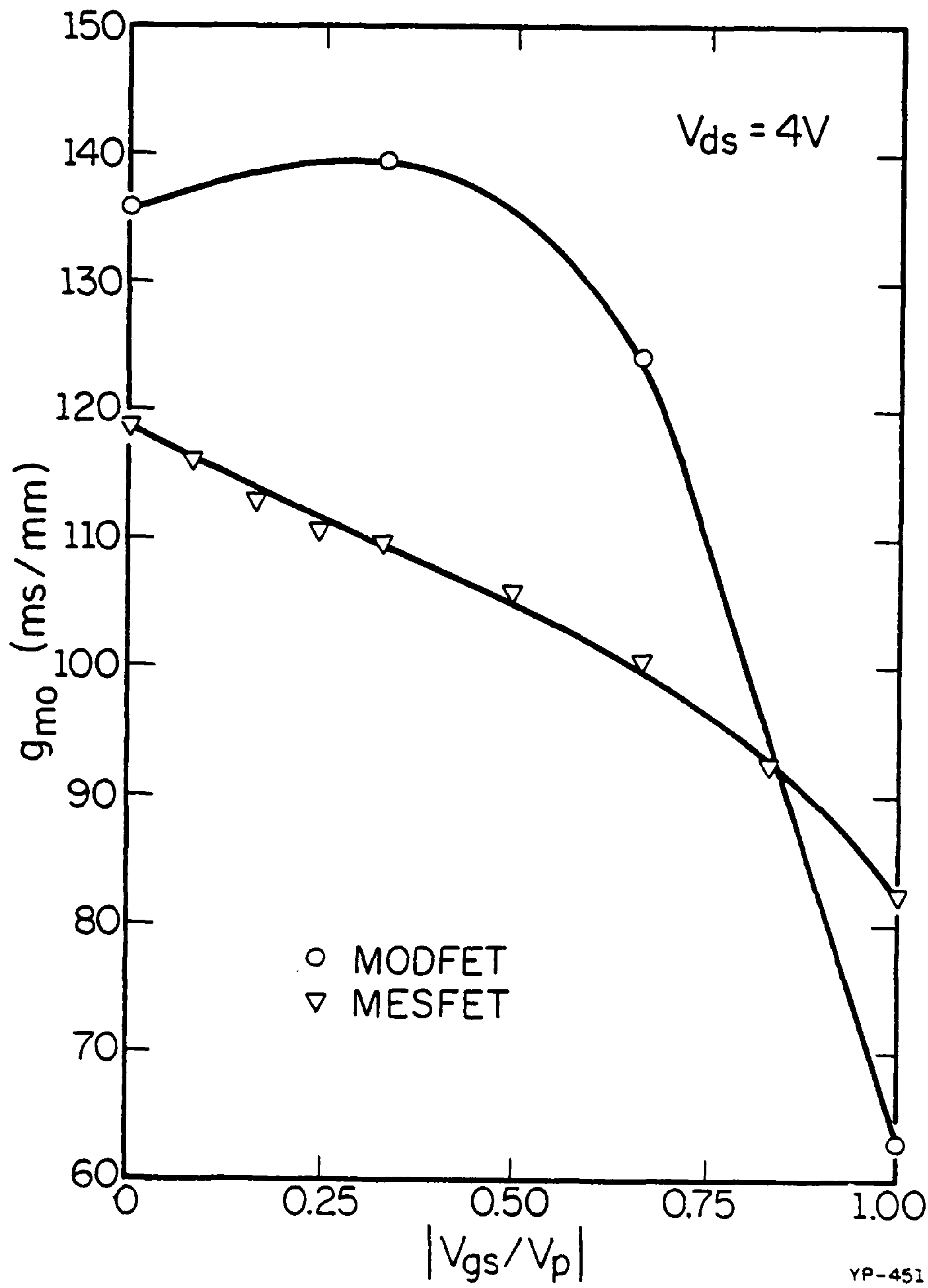

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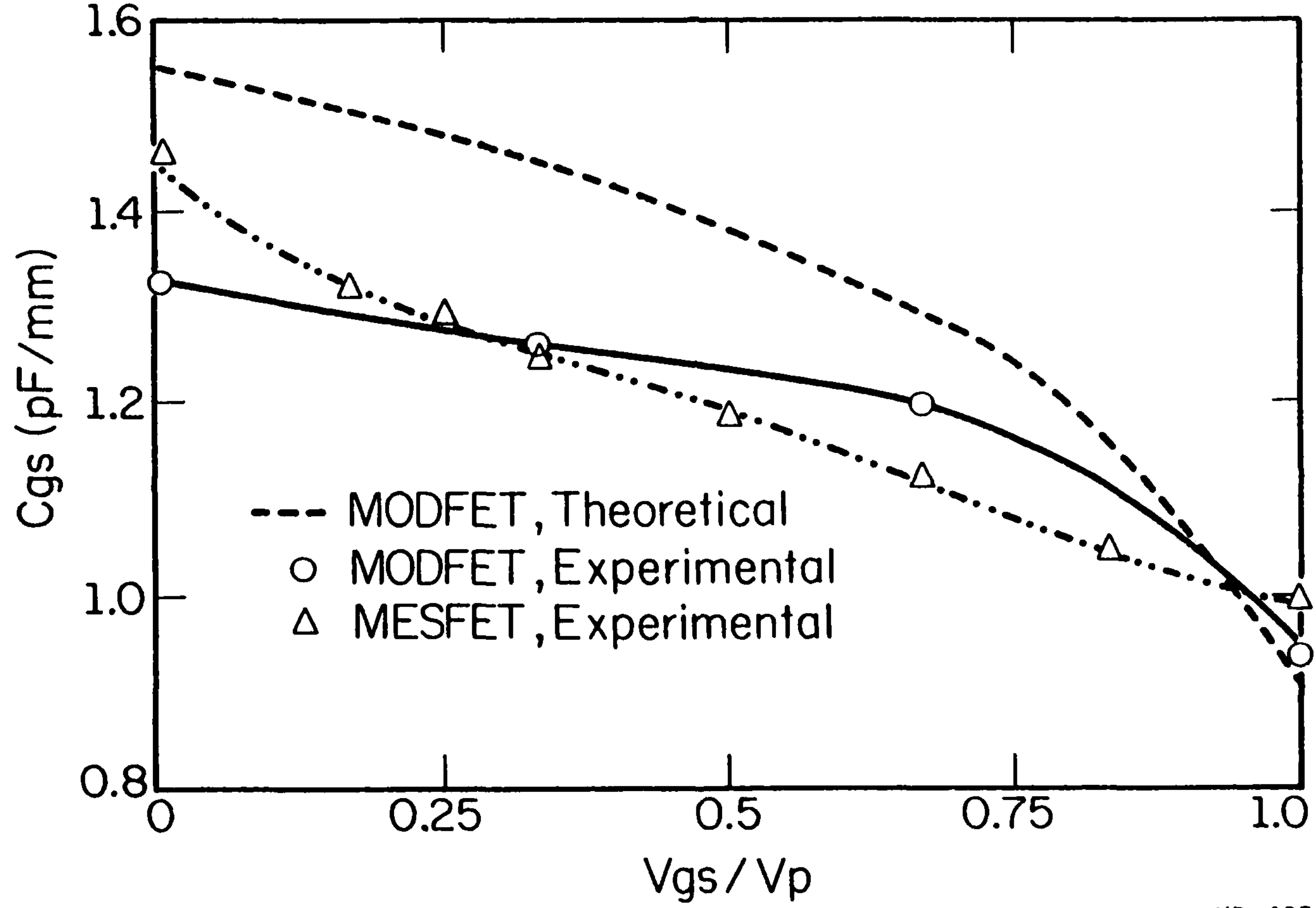

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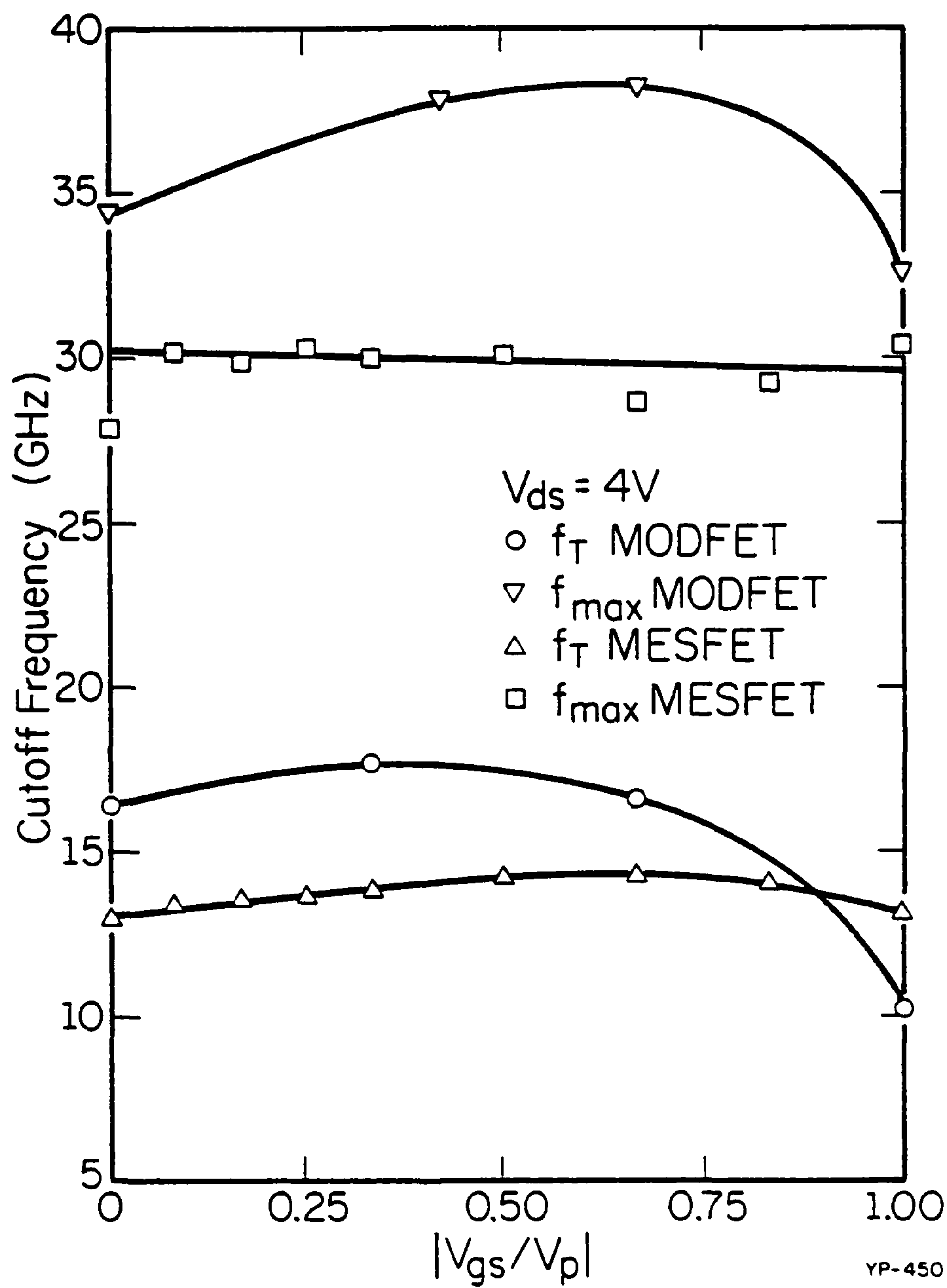

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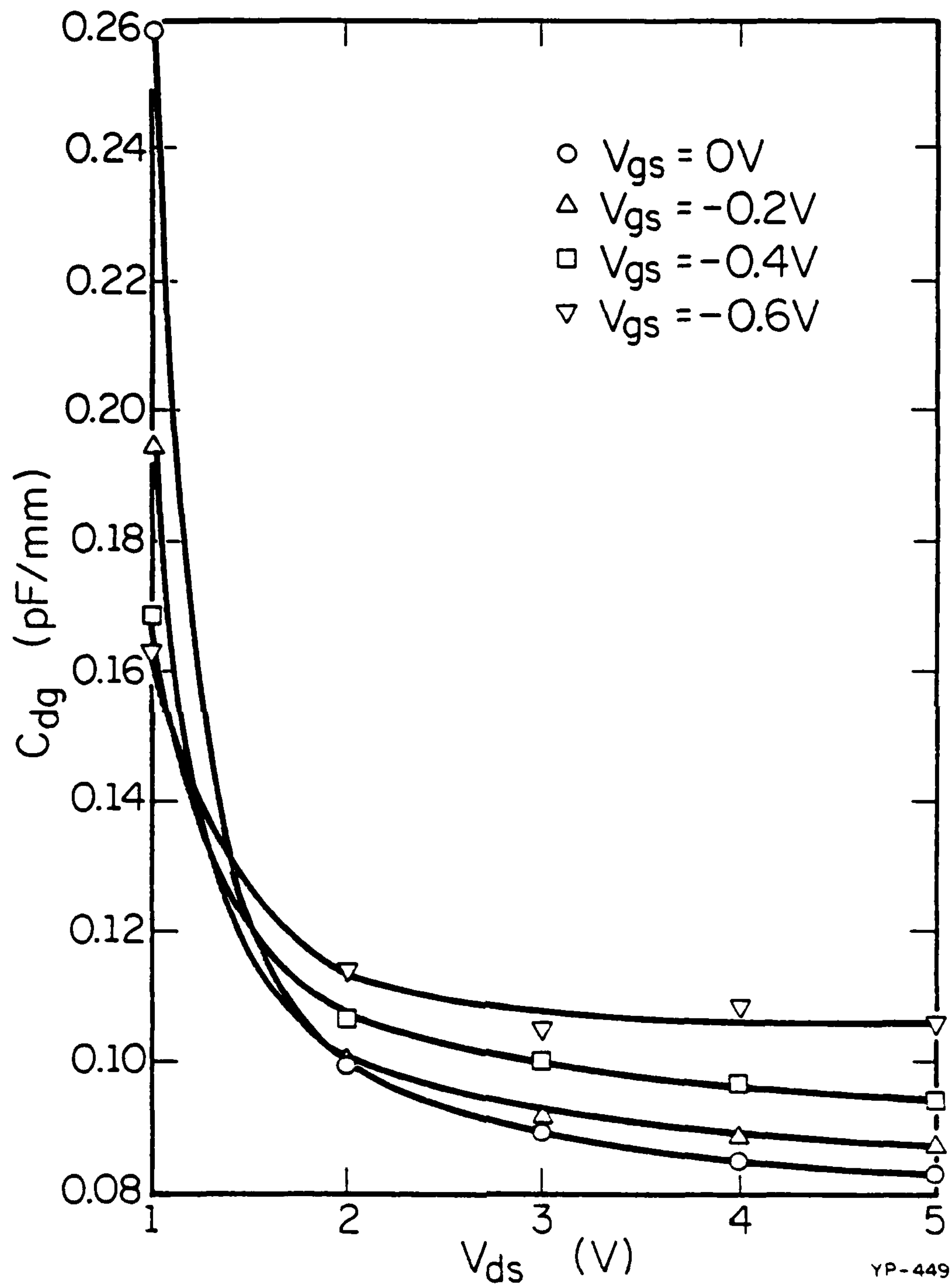

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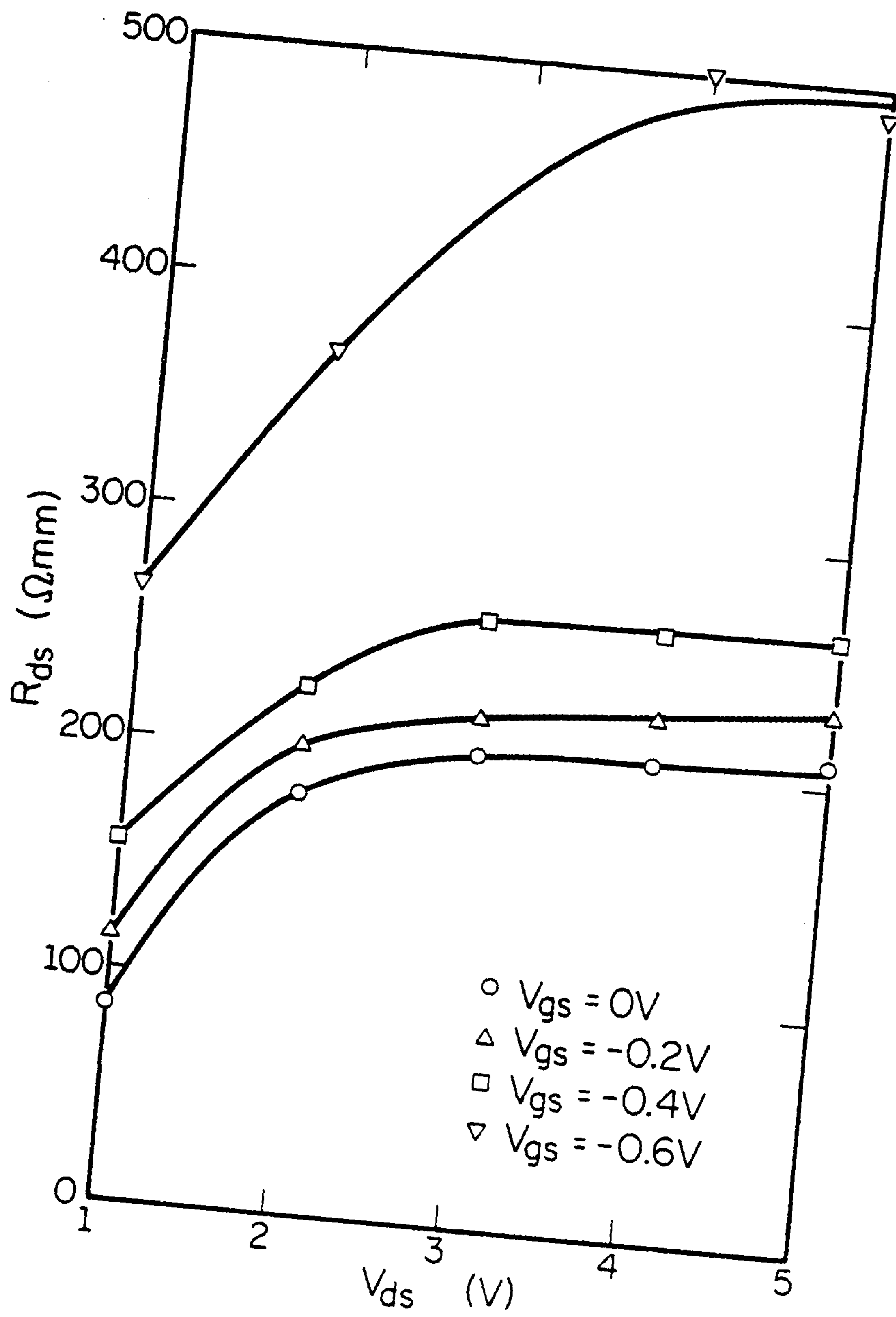

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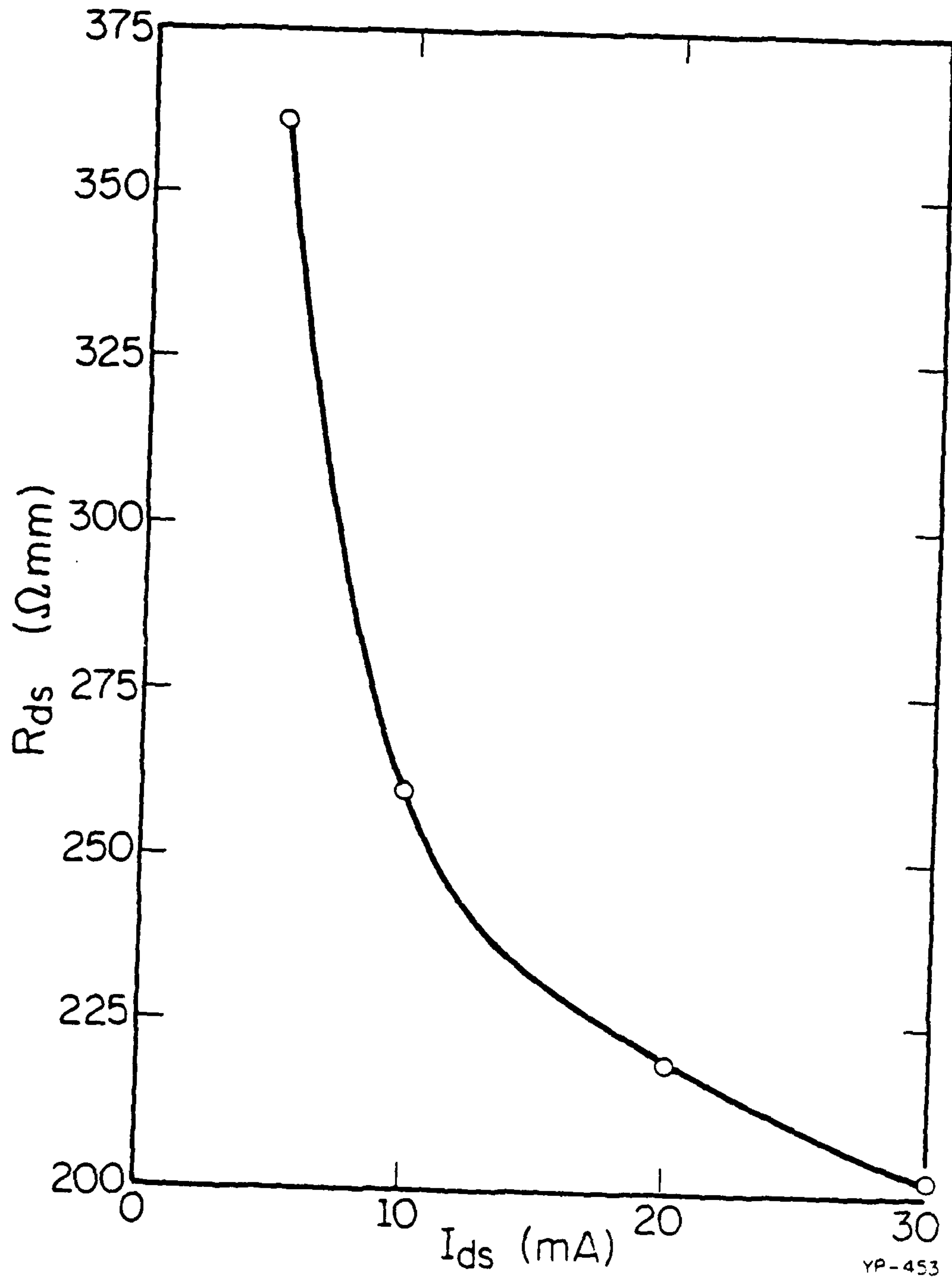

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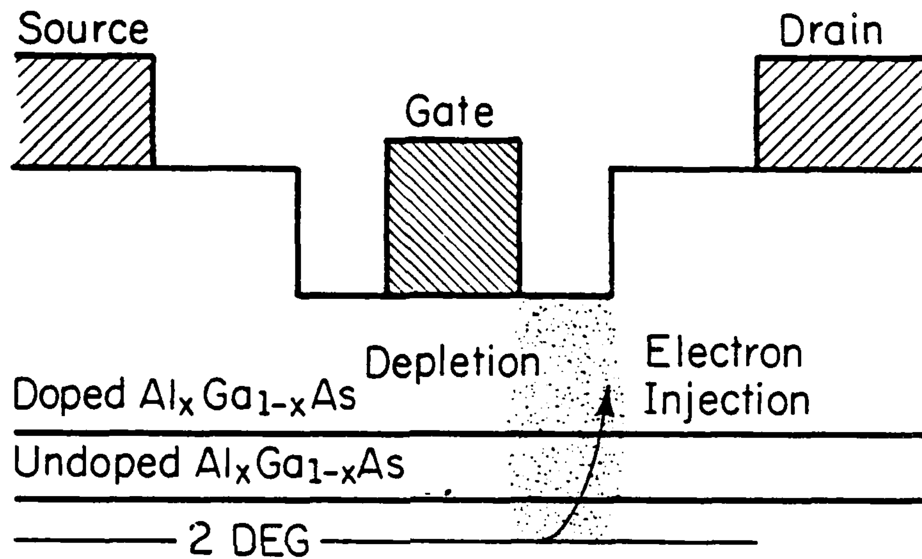

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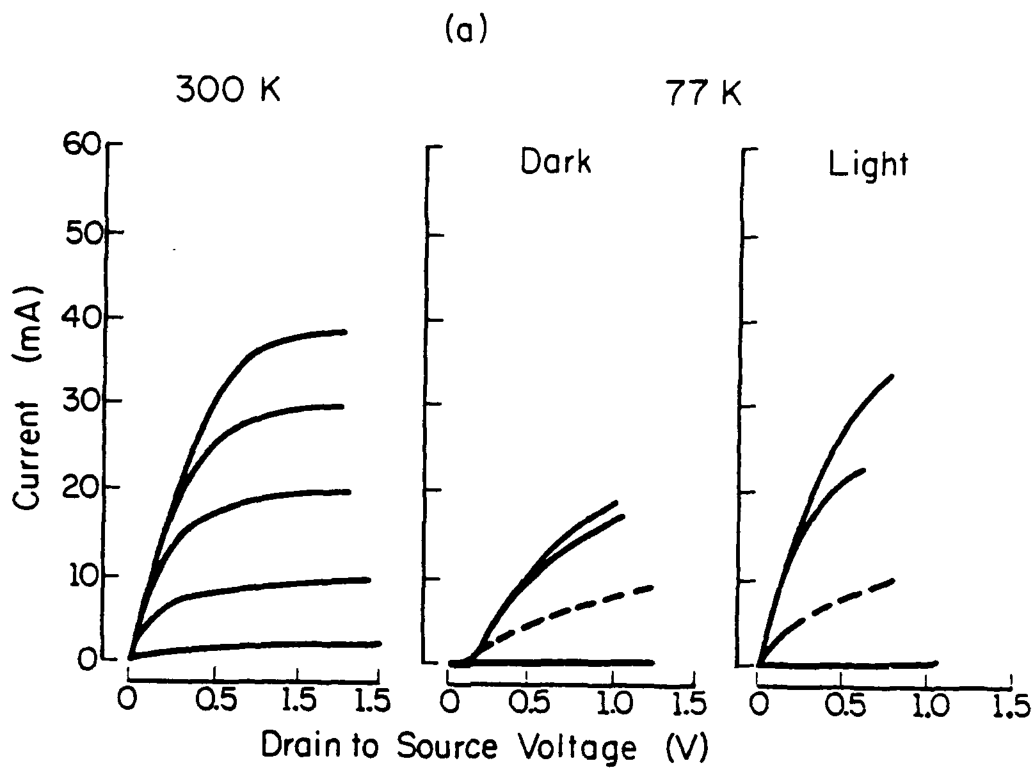

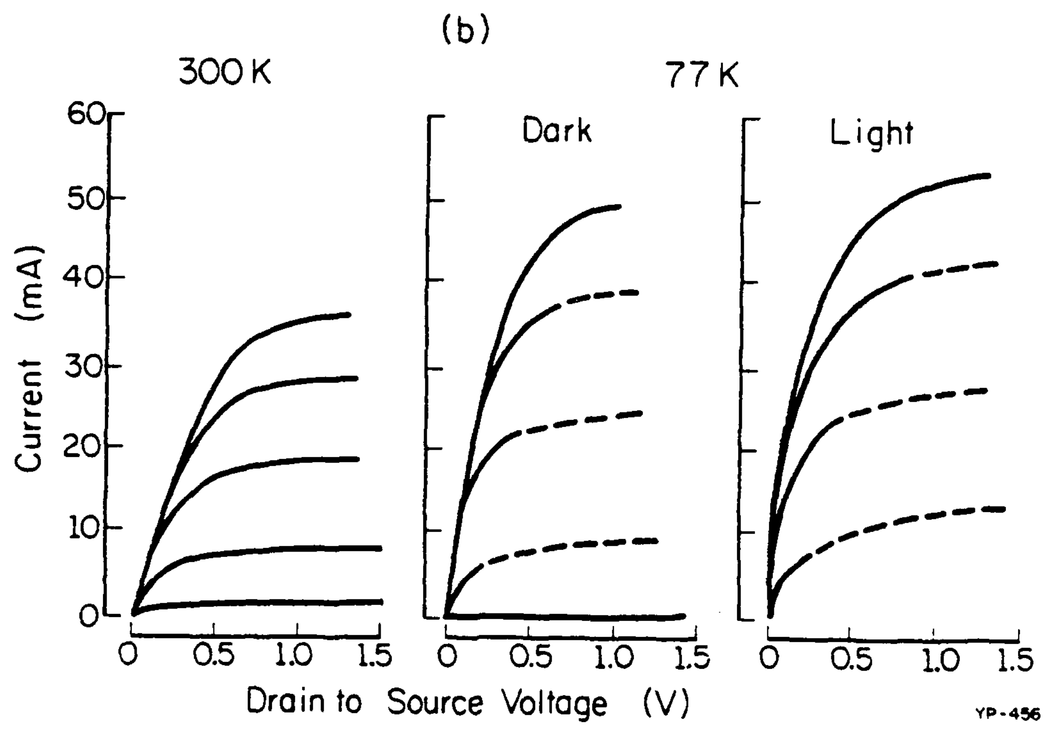

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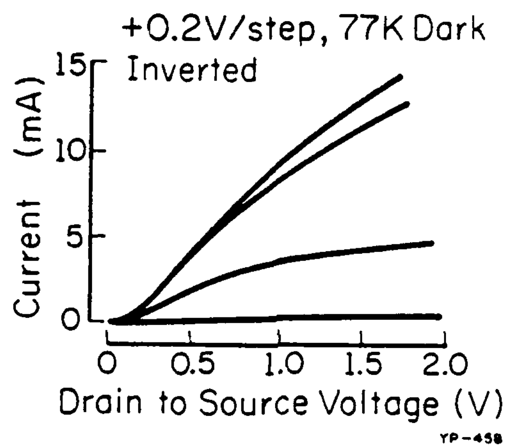

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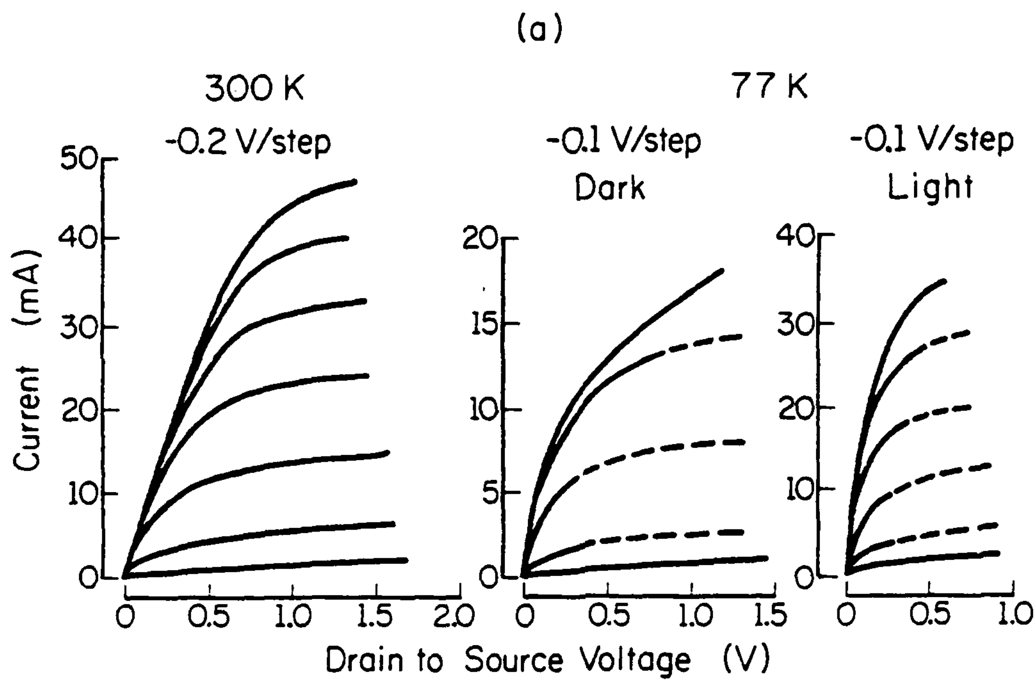

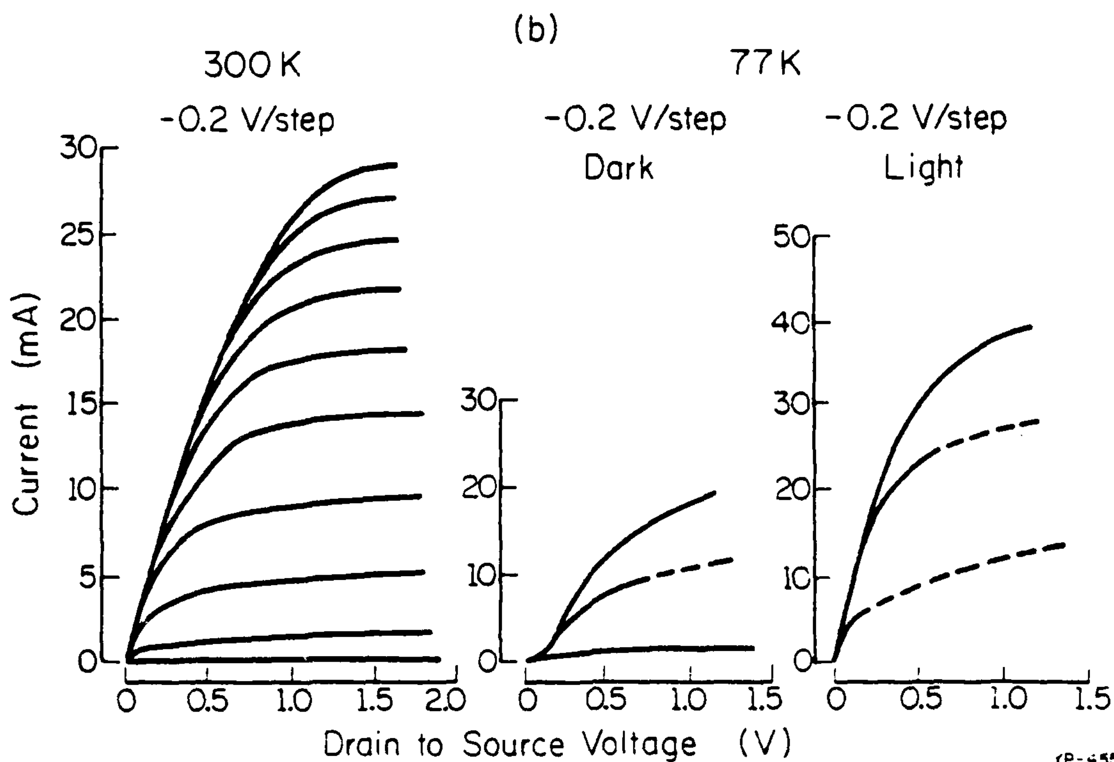

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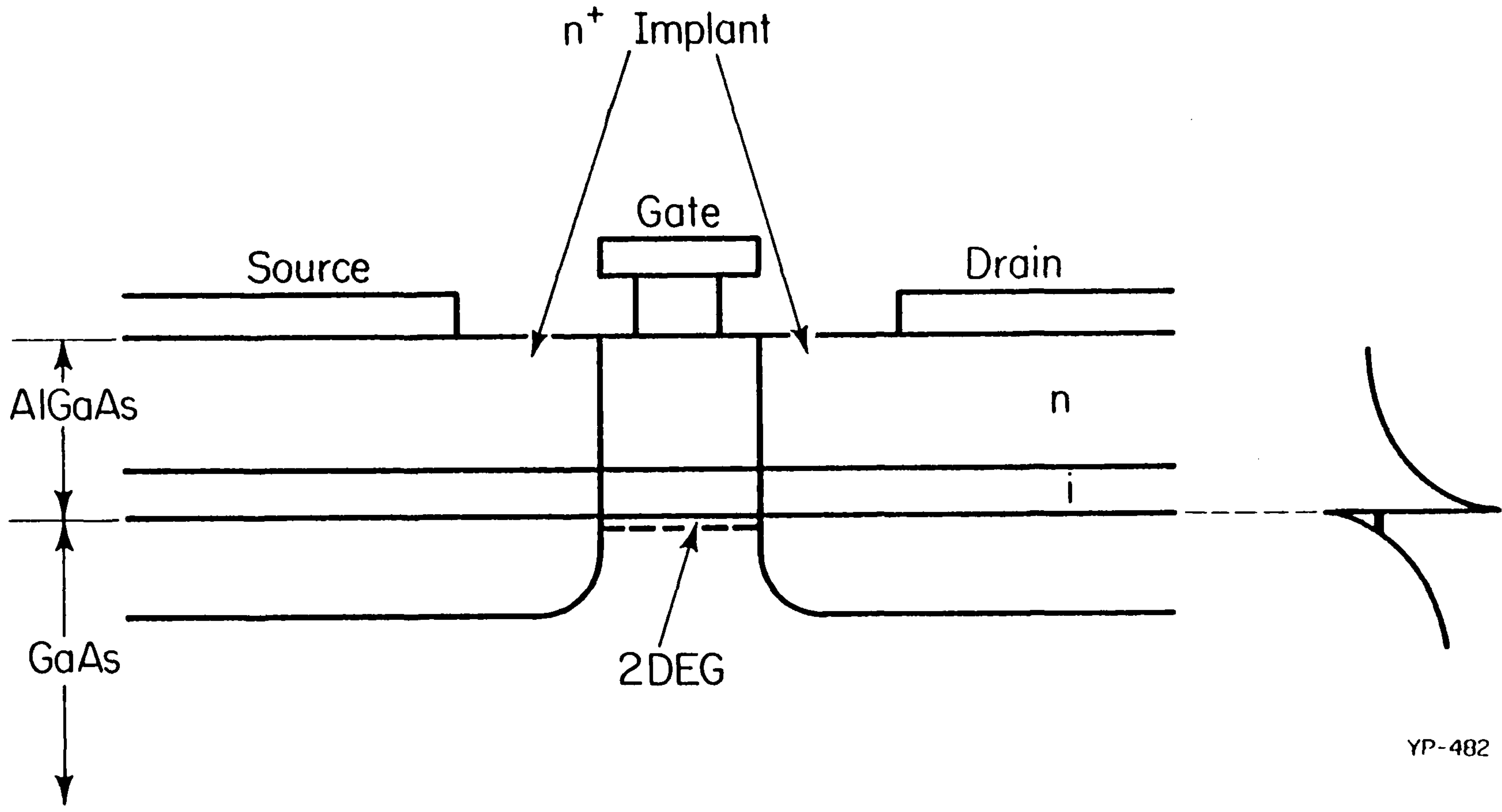

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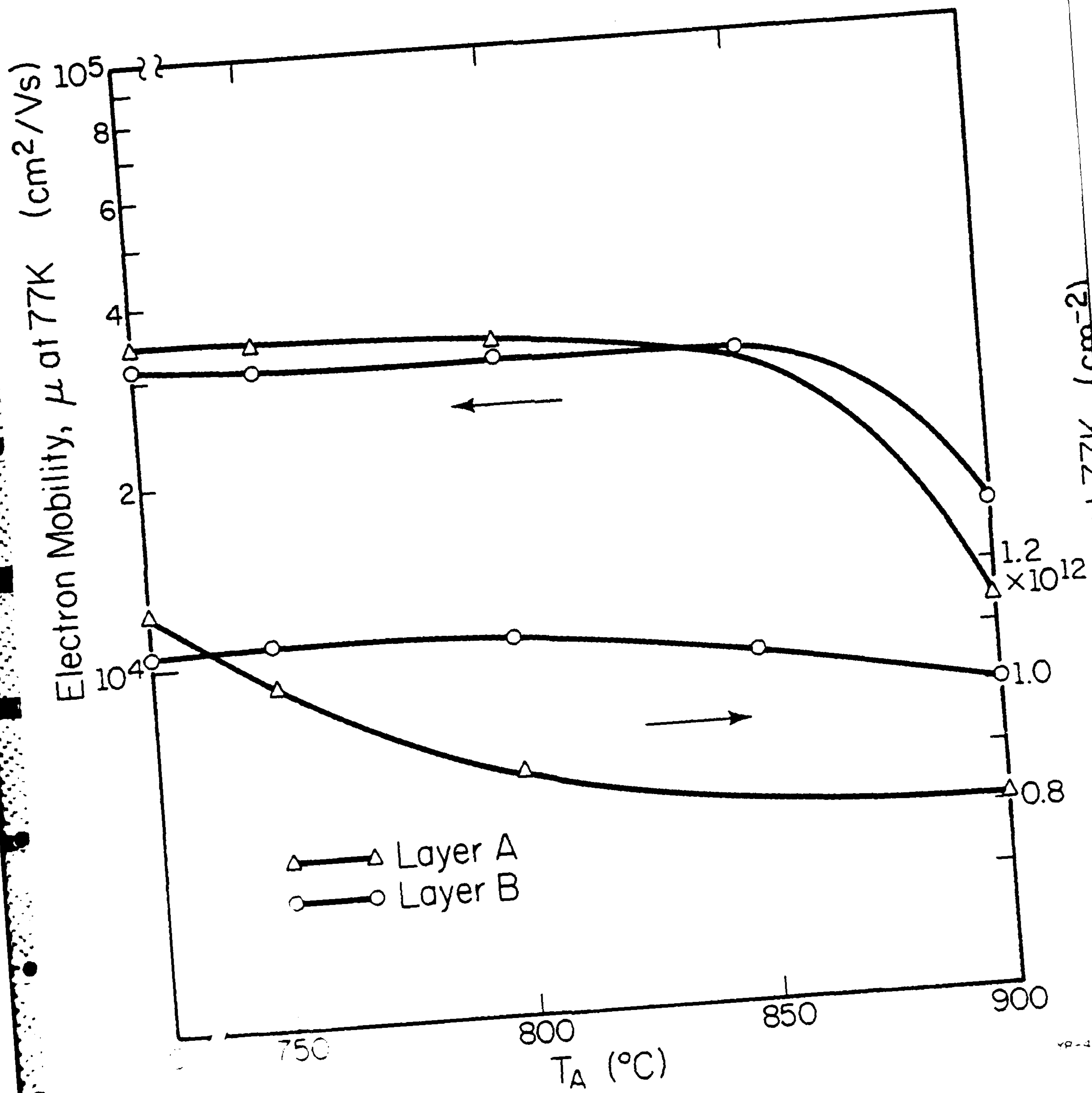


Fig. 26

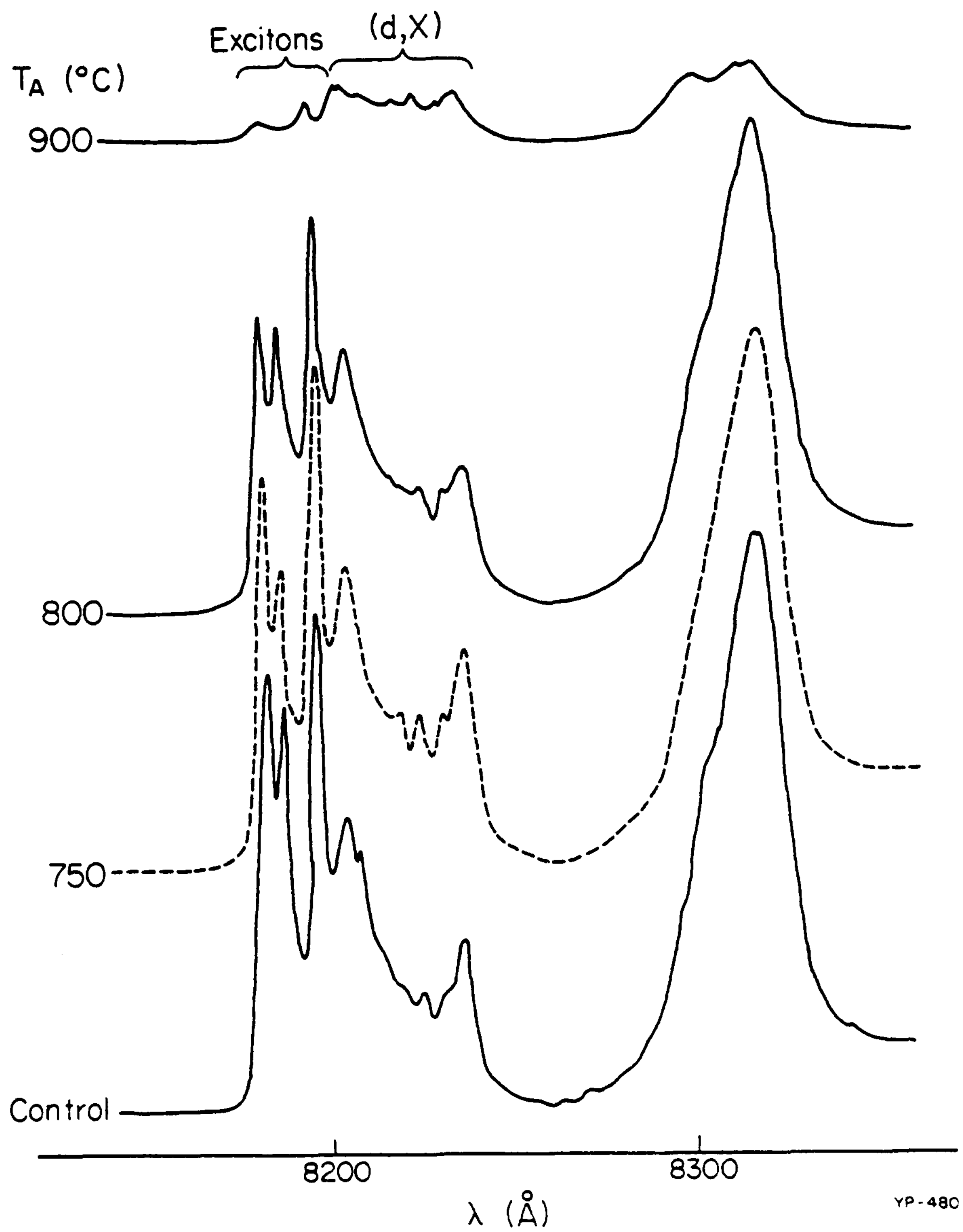
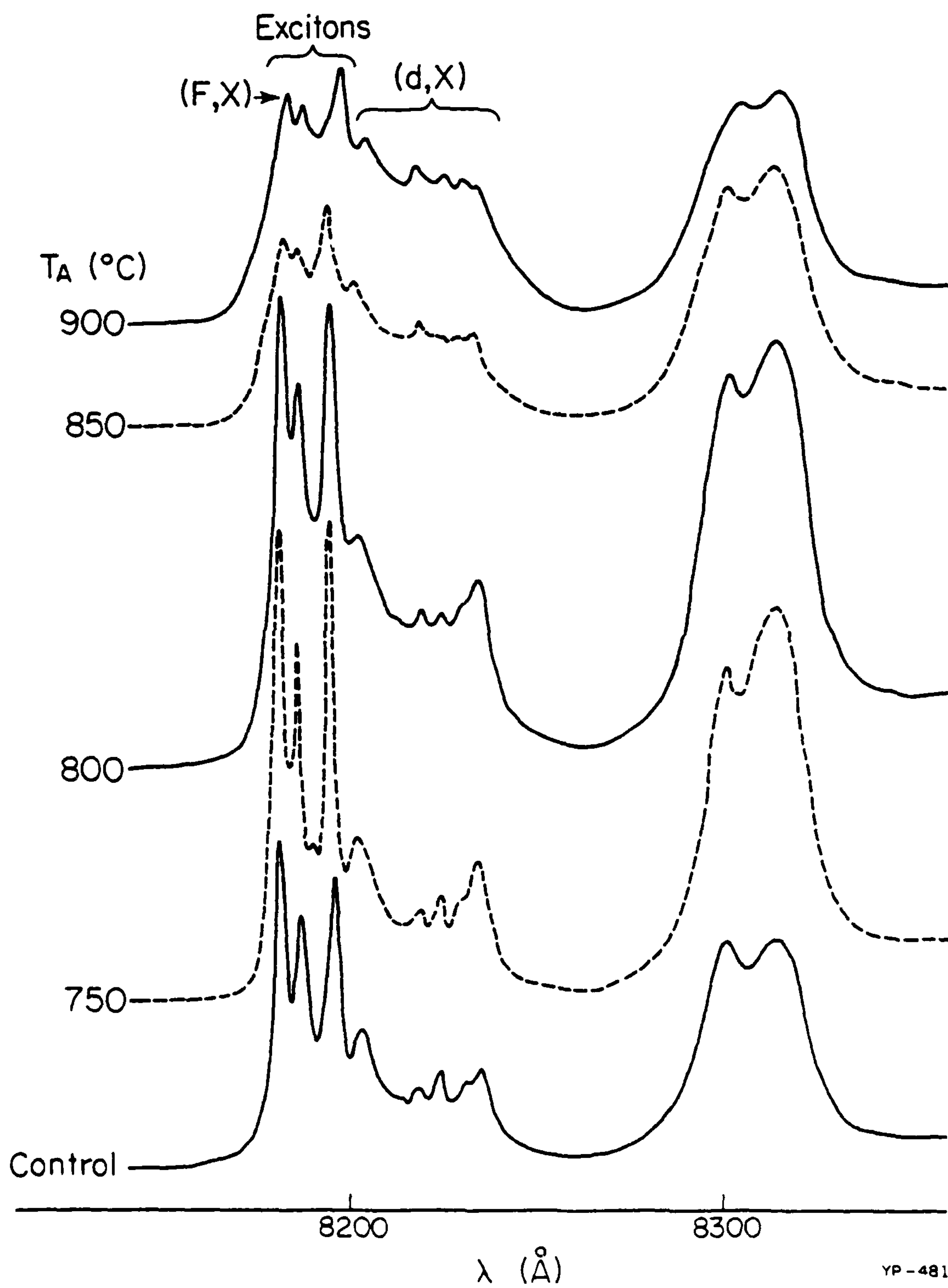


Fig 27



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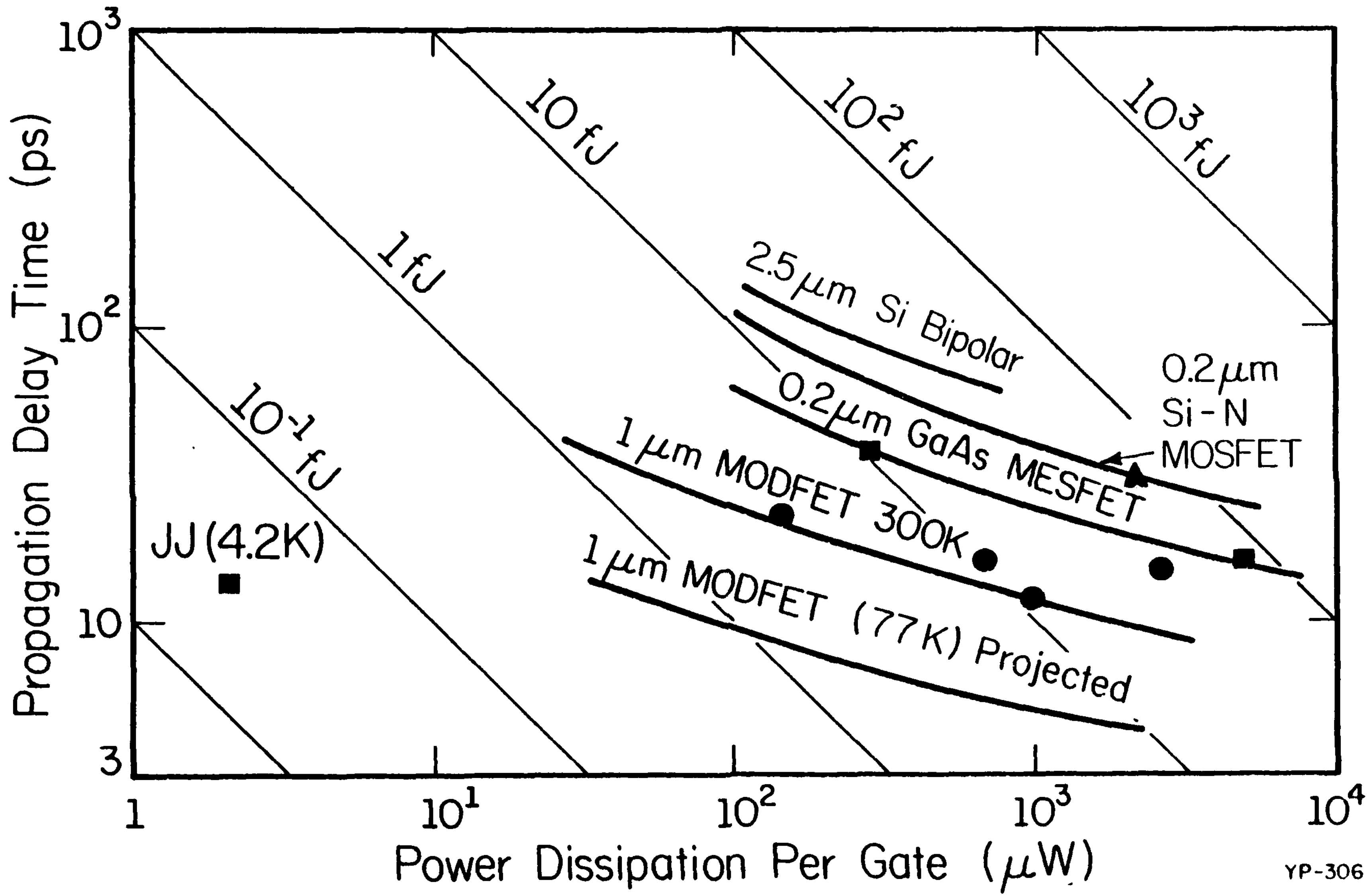

Fig. 29

XIII. APPENDIX A

Microwave Performance of GaAs MESFETs with AlGaAs Buffer Layers: Effect of Heterointerfaces

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Abstract

Field effect transistors consisting of GaAs active layers and $Al_{0.33}Ga_{0.67}As$ buffer layers with abrupt, graded bulk, and graded superlattice hetero-interfaces were fabricated and compared to GaAs buffer transistors. Microwave measurements showed that a good interface is obtained in the graded superlattice interface structure and that there is a small improvement in gain (1 to 2 dB) over the GaAs buffer structure.

Based on dc results, improved rf performance has been predicted for GaAs MESFETs when an $Al_xGa_{1-x}As$ buffer layer is incorporated between the substrate and the channel.[1,2] The higher resistivity and bandgap of $Al_xGa_{1-x}As$ is expected to reduce undesirable substrate currents and improve the sharpness of the pinch-off characteristics.[1-4] Accordingly, the microwave performance of a GaAs MESFET should be improved by the inclusion of an $Al_xGa_{1-x}As$ buffer layer. Until now no effort has been made to investigate the microwave properties of $Al_xGa_{1-x}As$ buffer GaAs MESFETs in detail.

Unfortunately, it has proven difficult to achieve a good interface between GaAs and $Al_xGa_{1-x}As$ when the GaAs is grown on top of the $Al_xGa_{1-x}As$.[5] Two possible means of improving this interface are the insertion of a graded mole fraction $Al_xGa_{1-x}As$ layer, insertion of a graded superlattice between the channel and buffer layer and replacing the $Al_xGa_{1-x}As$ layer with a superlattice altogether.[6] The graded superlattice structure has already been demonstrated to improve the electron mobilities in inverted modulation doped structures sixfold (where the ($Al_xGa_{1-x}Ga$ is on top of GaAs) which is a good indication that the superlattice has significantly improved the interface between the GaAs and the $Al_xGa_{1-x}As$.[7]. In addition, the use of this superlattice at the heterojunctions in double heterojunction lasers reduced the current threshold density by a factor of two.[8] Further, it improved the photoluminescence related to excitonic processes in GaAs/$Al_xGa_{1-x}As$ single quantum well structures by a factor of 160 over that from an abrupt interface quantum well.[8]

Since the performance of an $Al_xGa_{1-x}As$ buffer GaAs MESFET hinges on the quality of the hetero-interface, the use of the aforementioned schemes of interfacial improvement should also result in better performance of these devices. In this work, the three types of hetero-interfaces for $Al_xGa_{1-x}As$ buffer GaAs MESFETs are compared through their microwave performance for the first time. The three types of $Al_xGa_{1-x}As$ buffer MESFETs are also compared to GaAs buffer MESFETs.

Experimental

Structures studied were grown by Molecular Beam Epitaxy (MBE) on (100) oriented Cr doped GaAs substrates. The details of substrate preparation and growth procedures have been reported elsewhere.[9] The structure having a 0.5 μm GaAs buffer was first grown followed by a 0.5 μm $Al_{0.33}Ga_{0.67}As$ buffer layer and a 0.3 μm GaAs channel is shown in Figure 1. Three types of interfaces were incorporated between the buffer and the channel: An abrupt interface, a graded bulk interface, where the Al mole fraction was graded over 150 Å, and a three period 150 Å total thickness superlattice interface where the thickness of AlGaAs layers was reduced toward the GaAs channel, leading to a graded average Al mole fraction. The channel layer was 0.3 μm thick and doped with Si to 2×10^{17} cm-3.

After growth, mesa isolation patterns were photolithographically defined and etched in 1:1:3 $HF:H_2O_2:H_2O$. Source and drain metallization patterns were developed and AuGe/Ni/Au was evaporated. The contacts were alloyed at 500°C in an H_2 atmosphere for one minute. Next an Aluminum gate of length 1 μm and width 290 μm was evaporated following a

gate recess of about 0.15 μm. Finally overlay metallization was added and the devices were bonded to 50 ohm microstrip transmission lines for scattering parameter measurements using an HP 8409B automatic network analyzer controlled by a HP 9845 desktop computer. From the measured data gain and small signal circuit parameters were deduced.[10]

Results

Figure 2 shows the current-voltage characteristics of half a superlattice interface $Al_xGa_{1-x}As$ buffer device. The low frequency I-V characteristics of the other two $Al_xGa_{1-x}As$ buffer layer structures and those of devices which had only GaAs buffers displayed similar characteristics. One difference between the characteristics is pinch-off voltage of the abrupt and linear graded interface devices, which were lower than those of the superlattice interface or GaAs buffer devices because of different gate recessing.

S-parameter measurements at 2 GHz were made as a function of reverse gate bias. In Figure 3, the unilateral gain is plotted against reverse gate bias up to the pinch-off voltage of each device. The maximum available gain was not computed since the stability factor, k, was less than one for the devices. The deleterious effect of the poor interface between the $Al_xGa_{1-x}As$ buffer layer and the GaAs channel is demonstrated by the drop in microwave gain with increasing reverse gate bias for the abrupt interface device. In contrast, the graded alloy interface structure does not demonstrate this decrease until the gate bias approaches the pinch-off voltage indicating a better interface.

The superlattice interface structure demonstrates almost no degradation with gate bias implying an excellent interface between the buffer and channel. Although the reason for the positive slope of the gain versus gate bias characteristics for the superlattice interface structure at gate voltages below 0.6 volts is not clear, it is consistent among several devices taken from different wafers. It may be related to charge trapping in the superlattice. Due to the imperfect buffer/channel interfaces for the abrupt and graded alloy interface mole fraction $Al_xGa_{1-x}As$ buffer devices only the superlattice structure demonstrated a slight performance advantage over the GaAs buffer device; and this is a increase of just one to two decibels.

The small signal transconductance plotted in Figure 4 again exhibits a sharp decline for the abrupt and graded alloy interface transistors as the gate bias near pinch-off. A small improvement in high frequency transconductance is indicated for the $Al_xGa_{1-x}As$ buffer structure with superlattice interface or linear graded interface at small gate voltage over the GaAs buffer device.

A good interface in terms of rf electron transport at high fields has been achieved between an $Al_xGa_{1-x}As$ buffer layer and the GaAs channel of a GaAs MESFET by inclusion of a three period superlattice at the hetero-interface. A small improvement in microwave performance has been obtained for the $Al_xGa_{1-x}As$ buffer MESFET with the superlattice over the conventional GaAs buffer device. This improvement was demonstrated by an increase in unilateral gain and small signal transconductance at 2 GHz.

Acknowledgements

This work is supported by the Air Force Office of Scientific Research. The authors would like to acknowledge the fruitful discussions with Dr. T. J. Drummond, J. Klem, Prof. L. F. Eastman and K. R. Gleason.

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AD-A141 058 HIGH SPEED FETS FABRICATED IN GAAS/ALGAAS LAYERED STRUCTURES PREPARED BY..(U) ILLINOIS UNIV AT URBANA COORDINATED SCIENCE LAB H MORKOC JAN 84 2/2

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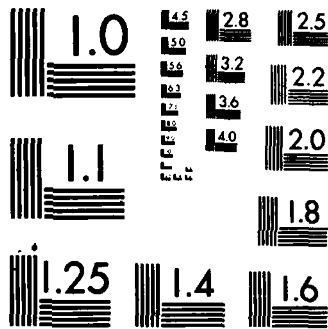

MICROCOPY RESOLUTION TEST CHART
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Figure Captions

1. Structure of $Al_xGa_{1-x}As$ MESFETs. Abrupt, 150 Å graded alloy (mole fraction graded from 0.3 to 0 from bottom to top), and graded superlattice interfaces were grown. The superlattice is indicated in the inset.

2. Current-voltage characteristics of a superlattice interface $Al_xGa_{1-x}As$ buffer MESFET. The scales are 10 mA/DIV horizontal, 0.5 V/DIV vertical and 0.5 gate bias/step. The I-V characteristics of the abrupt and graded bulk interface devices and the GaAs buffer device were similar.

3. Unilateral gain in dB at 2 GHz for the abrupt, linearly graded alloy, and graded superlattice interface $Al_xGa_{1-x}As$ buffer MESFETs and a GaAs buffer MESFET versus gate bias out to the pinch-off voltage.

4. Small signal transconductance at 2 GHz for $Al_xGa_{1-x}As$ buffer and GaAs buffer structures plotted versus reverse gate bias out to the pinch-off voltages.

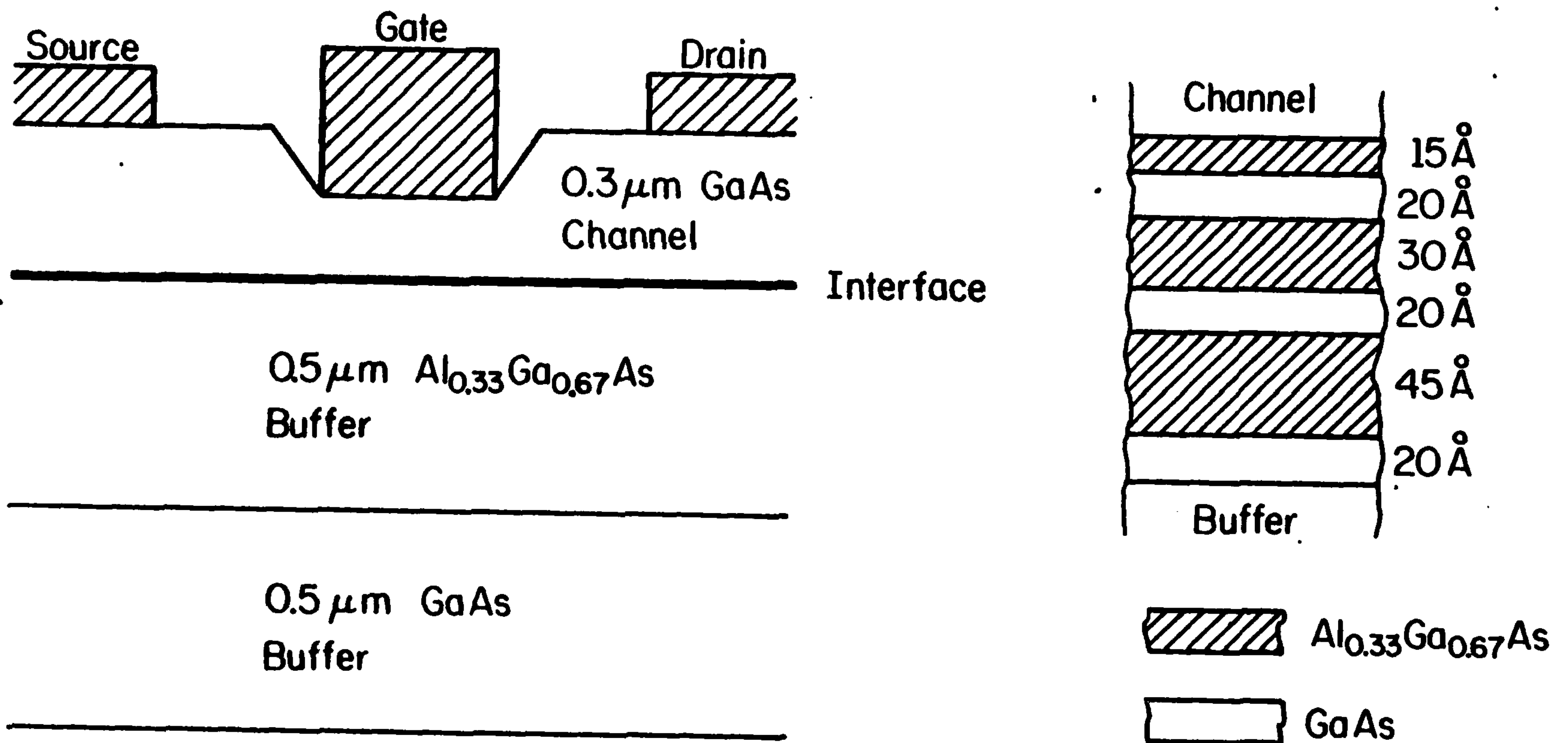

Fig 1

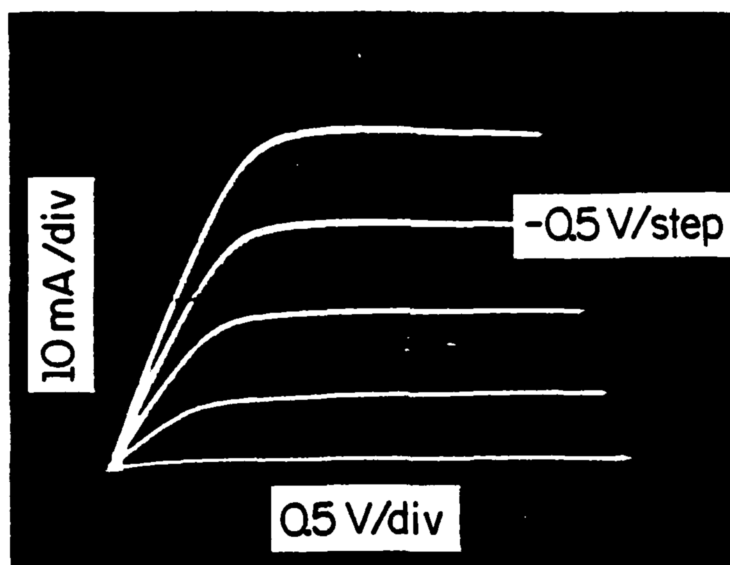

Fig 2

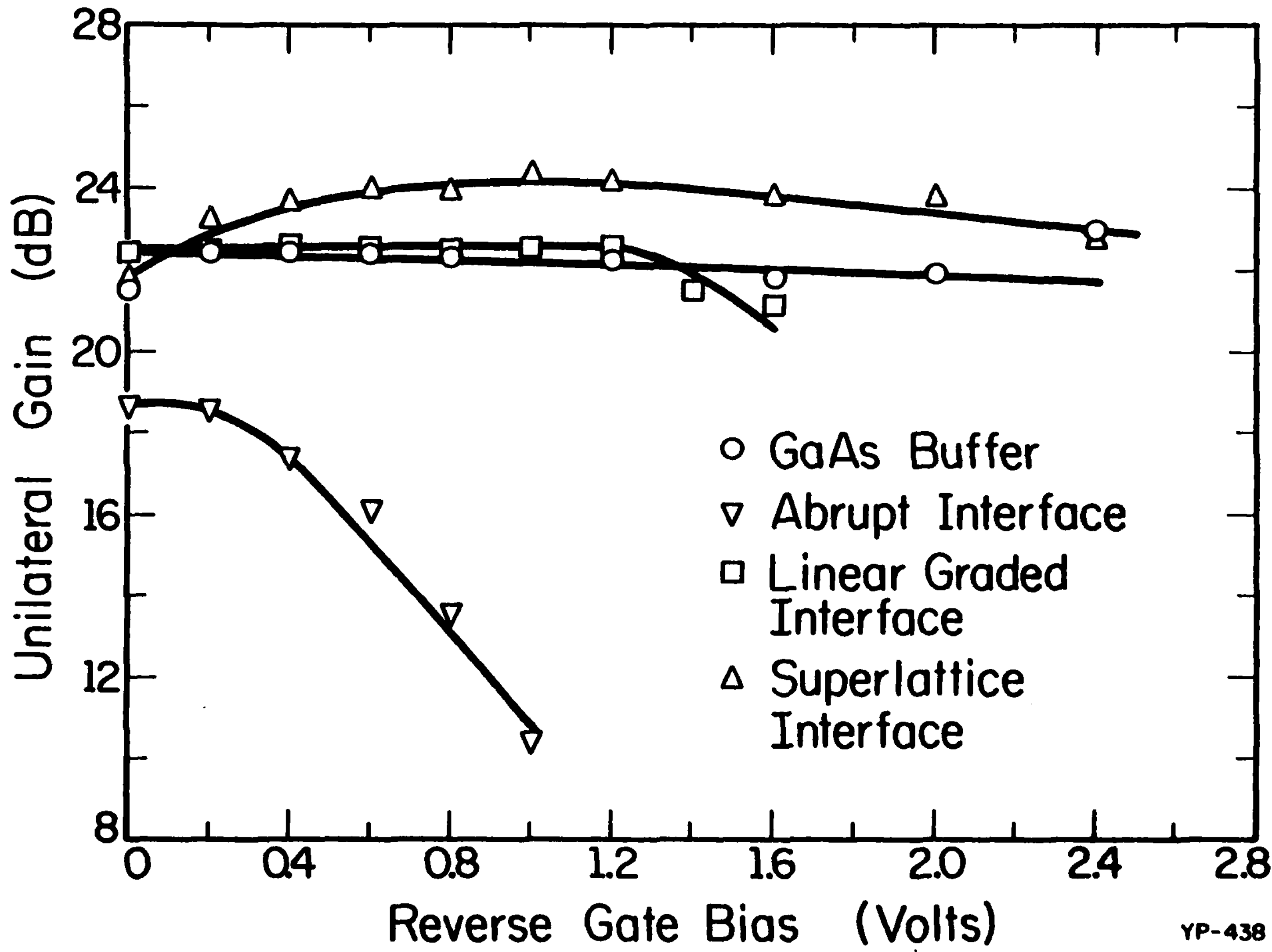

fig 3

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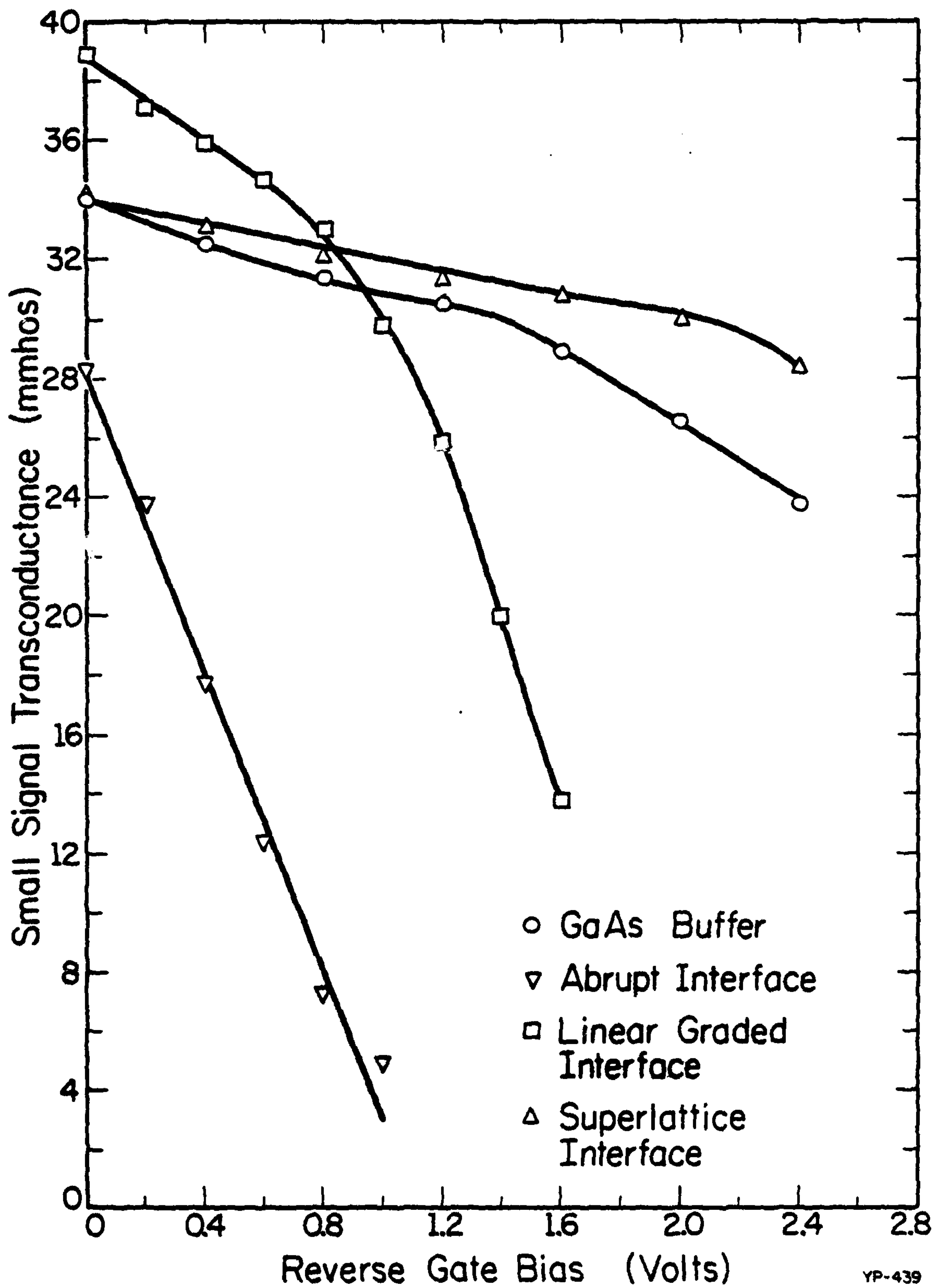

Fig 4

XIII. APPENDIX B

Reduction of Backgating in GaAs/AlGaAs MESFETs by Optimization Of the Active Layer - Buffer Layer Interface

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Abstract

Backgating measurements made on GaAs MESFETs with abrupt, graded alloy, and graded superlattice interface AlGaAs buffer layers were compared to measurements made on conventional GaAs buffer layer MESFETs. Only the superlattice interface structure showed a reduction in the backgating transconductance (by a factor of 24 compared to the GaAs buffer layer FET). The lack of reduction in the backgating transconductace for the abrupt and graded alloy interface devices is attributed to traps resulting from GaAs growth on an AlGaAs layer.

The performance of GaAs MESFETs can be adversely affected by the reduction of drain current due to backgating.[1-4] Backgating is the modulation of the channel caused by changes in the potential of the substrate arising from deep traps in the substrate.[1,3]

It has been reported that the inclusion of an AlGaAs buffer layer in GaAs MESFETs can lead to improved pinch-off characteristics.[5,6] higher output resistance,[5,9] and higher breakdown voltages[8,9] due to higher buffer layer resistivity and electron confinement at the interface. Little or no effort, however, has been devoted to the investigation of the effect of AlGaAs buffer layers on the backgating in GaAs MESFETs. In this letter we report on the backgating of GaAs MESFETs with AlGaAs buffers.

Of special interest is the interface quality because growth of GaAs on top of AlGaAs, can result in inferior electron velocity in the GaAs active layer as a consequence of the relatively small surface mobility of Al and perhaps to strain at the heterointerface, novel structural schemes for overcoming this difficulty can be employed. Their effect on backgating is also reported in this study.

The samples were grown by molecular beam epitaxy on Cr doped semi-insulating, GaAs substrates.[10] The structures, indicated in Figure 1, consist of a 0.5 μm thick undoped GaAs buffer layer, a 0.5 μm thick undoped $Al_{0.3}Ga_{0.7}As$ buffer layer, and a 0.3 μm GaAs channel doped with Si to Nd = $2x10^{17}cm^{-3}$. Three different interface structures were incorporated between the channel and the AlGaAs buffer layer: An abrupt interface, a 150 Å graded alloy interface (Al mole fraction graded from 0.3 at the buffer to zero at the channel), and a 150 Å three period graded superlattice interface.

The structure of the superlattice is indicated in the inset of Figure 1 and consists of alternating 20 Å thick undoped layers of GaAs and 45, 30, and 15 Å thick undoped $Al_{0.3}Ga_{0.7}As$ layers. This superlattice interface scheme for growing GaAs on AlGaAs has been found to substantially improve the performance of inverted modulation doped structures[11] and GaAs/AlGaAs double heterojunction lasers,[12] as well as to improve the photoluminescence properties of GaAs/AlGaAs quantum wells.[13] The superlattice structure is believed to conserve the electronic properties of bulk GaAs material in the active layer, which is grown epitaxially on top of the AlGaAs buffer layer.

After growth mesa isolation patterns were photolithographically defined and etched in 1:1:3 ($HF:H_2O_2:H_2O$). Source and drain patterns were defined after which AuGe/Ni/Au was evaporated and alloyed at 500°C in an H_2 atmosphere for 60 seconds to form ohmic contacts. Gate patterns were defined and the active layer under the gate recessed to approximately 1500 Å. Al was evaporated for gate metalization.

Devices from each of these three AlGaAs buffer layer structures as well as from a GaAs buffer FET exhibited almost the same transconductances. Transistors with a 1 µm gate length, a 145 µm gate width and a channel length of 3 µm exhibited transconductances of 160-175 mS/mm and source resistances of 1.2-0.93 Ω mm.

The test pattern for measuring the backgating effect is shown in Figure 2. The backgating contact is located 50 µm away from an FET with a 1 µm long by 50 µm wide gate and a 6 µm long channel. The backgating transconductance ($\Delta I_{dss}/ \Delta V_{BG}$) is given in Table 1 for a gate to source voltage of zero where I_{dss} is the drain saturation current and V_{BG} is the voltage on the backgating contact with respect to the source. The AlGaAs buffer layer devices showed no

improvement in the backgating effect except for the superlattice interface structure FET, which shows a 24 fold reduction in backgating transconductace compared to the conventional GaAs buffer layer device. FETs with an AlGaAs buffer layer should exhibit less backgating transconductance because the high resistivity of the AlGaAs layer impedes injection of charge into the substrate. The effect of this high resistivity layer is evident by the three fold increase in output resistace for the AlGaAs buffer layer FET over the GaAs buffer layer device.

The fact that the abrupt and graded alloy interface devices do not show less backgating effect may be due to modulation of the active layer by changes in deep traps at the buffer layer-active layer interface, a direct result of not being able to achieve a high quality heterointerface.[13] The superlattice structure reduces this effect by reducing the number of deep traps caused by lattice mismatch strain and/or vacancies resulting from the smaller surface mobility of Al as compared to Ga.[14] The active layer - AlGaAs buffer layer interface is under further investigation.

Summary

AlGaAs buffer layer FETs with a graded superlattice active layer-buffer layer interface displayed 24 times less backgating transconductance than conventional GaAs buffer layer devices because of the high resistivity of the AlGaAs. AlGaAs buffer layer structures with abrupt or graded alloy interface did not demonstrate a reduction of the backgating effect due to a large concentration of traps at the heterointerface.

Acknowledgements

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Figure Captions

1. Structure of AlGaAs MESFETs. Abrupt, 150 Å graded alloy (Al Molefraction graded from 0.3 to 0 from botton to top), and graded superlattice interfaces are grown. The superlattice is indicated in the inset.

2. Layout of the backgating test pattern on the wafer. The gate is 1 μm long by 50 μm wide with a channel length of 6 μm. The gate is grounded to the source during backgating measurements.

Device Structure	Saturation Current (mA/mm)	Transconductance (mS/mm)	Backgating Transconductance (mS/mm)	Rds (Ω)
GaAs Buffer Layer	300	175	12	500
Abrupt Interface	255	160	8	1600
Graded Alloy Interface	290	160	10	1400
Superlattice Interface	310	175	0.5	1400

Table 1. Characteristics of AlGaAs buffer layer GaAs FETs.

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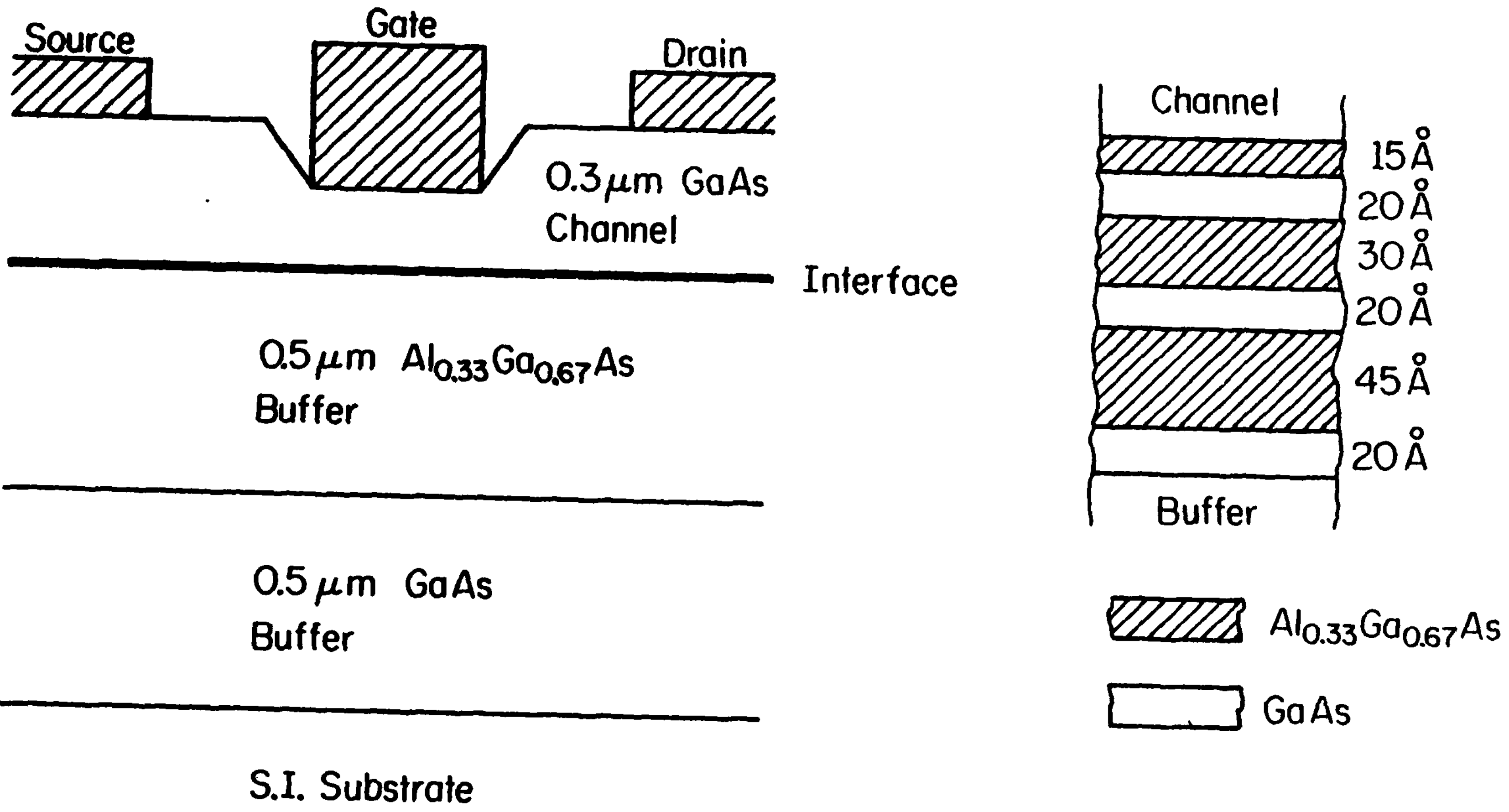

Fig 1

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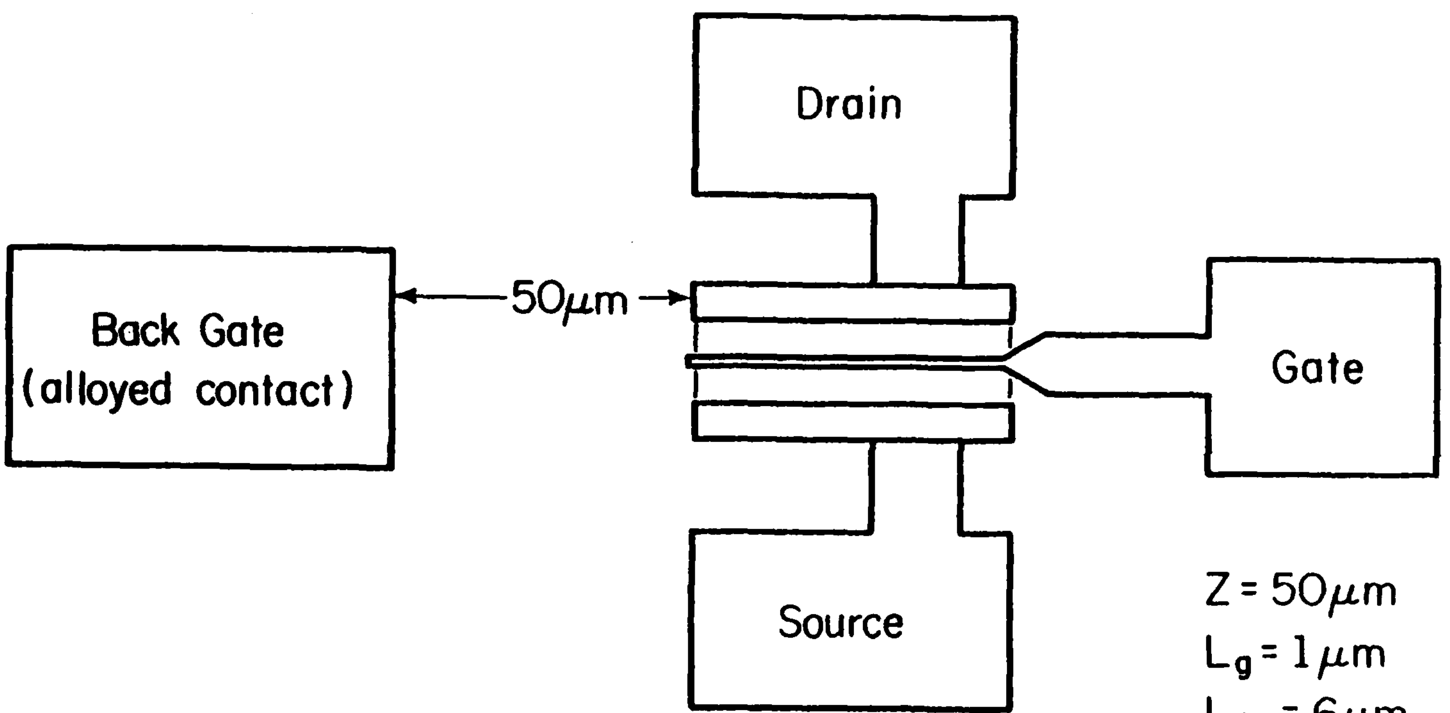

Fig. 2

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