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March, 1984 MRDC41131.6SA

# LOW POWER RADIATION HARD GaAs RAM

Semi-Annual Technical Report
For Period 6/10/82 through 12/9/83
Contract No. MDA903-83-C-0067

Effective and Expiration Dates: 12/10/82 and 11/09/84

Sponsored by:

Defense Advanced Research Projects Agency (DoD)
ARPA Order No. 4100

Under Contract No. MDA903-83-C-0067, issued by
Department of Army, Defense Supply Service -
Washington, D.C. 20310



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SECURITY CLASSIFICATION OF THIS PAGE

AD A139930

## REPORT DOCUMENTATION PAGE

| | |
|---|---|
| 1a. REPORT SECURITY CLASSIFICATION<br>Unclassified | 1b. RESTRICTIVE MARKINGS |
| 2a. SECURITY CLASSIFICATION AUTHORITY | 3. DISTRIBUTION/AVAILABILITY OF REPORT<br>Approved for public release; distribution unlimited. |
| 2b. DECLASSIFICATION/DOWNGRADING SCHEDULE | |
| 4. PERFORMING ORGANIZATION REPORT NUMBER(S)<br>MRDC41131.6SA | 5. MONITORING ORGANIZATION REPORT NUMBER(S) |
| 6a. NAME OF PERFORMING ORGANIZATION<br>Rockwell International Microelectronics Research & Development Center<br>6b. OFFICE SYMBOL (If applicable) | 7a. NAME OF MONITORING ORGANIZATION |
| 6c. ADDRESS (City, State and ZIP Code)<br>1049 Camino Dos Rios<br>Thousand Oaks, California 91360 | 7b. ADDRESS (City, State and ZIP Code) |
| 8a. NAME OF FUNDING/SPONSORING ORGANIZATION<br>Defense Advanced Research Projects Agency (DoD)<br>8b. OFFICE SYMBOL (If applicable) | 9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER<br>Contract No. MDA903-83-C-0067 |
| 8c. ADDRESS (City, State and ZIP Code)<br>Department of Army<br>Washington, D.C. 20310 | 10. SOURCE OF FUNDING NOS.<br>PROGRAM ELEMENT NO. / PROJECT NO. ARPA Order No. 4100 / TASK NO. / WORK UNIT NO. |
| 11. TITLE (Include Security Classification)<br>LOW POWER RADIATION HARD GaAs RAM (U) | |
| 12. PERSONAL AUTHOR(S)<br>Vahrenkamp, Richard; Chang, Frank; Kirkpatrick, Conilee; Eisen, Fred H. | |
| 13a. TYPE OF REPORT<br>Semi-Annual Technical Report<br>13b. TIME COVERED<br>FROM 06/10/82 TO 12/09/84 | 14. DATE OF REPORT (Yr., Mo., Day)<br>MARCH 1984<br>15. PAGE COUNT<br>34 |
| 16. SUPPLEMENTARY NOTATION | |
| 17. COSATI CODES<br>FIELD / GROUP / SUB. GR. | 18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number) |

19. ABSTRACT (Continue on reverse if necessary and identify by block number)


The scope of this program is to demonstrate a 1K GaAs static RAM having very low power dissipation, 1 μW/bit in standby, and a short access time, 10 ns, to meet the requirements of the DARPA Advanced On-Board Signal Processor (AOSP). In the six month period covered by this report the initial processing of the 1K RAM arrays was begun. Testing of several lots revealed a mask error which is currently being corrected.

The isolation studies for ultra-low power devices continued with major emphasis on isolation degradation following the Schottky metal process. A theoretical formulation for the leakage behavior of GaAs substrates was initiated, and good agreement between theory and the experimental data was obtained.

Upset measurements have been made on a number of 256 bit RAMs using an Am-241 alpha particle source. The numerical value for the failure cross section was found to be similar in magnitude to the area of the Schottky barrier speed-up capacitor, suggesting that the capacitor is primarily responsible for the magnitude of the upset cross section. Single event upset measurements have also been carried out using 40 meV protons


| | |
|---|---|
| 20. DISTRIBUTION/AVAILABILITY OF ABSTRACT<br>UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT. ☐ DTIC USERS ☐ | 21. ABSTRACT SECURITY CLASSIFICATION<br>Unclassified |
| 22a. NAME OF RESPONSIBLE INDIVIDUAL<br>Vahrenkamp, Richard | 22b. TELEPHONE NUMBER (Include Area Code)<br>(805) 498-4545<br>22c. OFFICE SYMBOL |

DD FORM 1473, 83 APR EDITION OF 1 JAN 73 IS OBSOLETE.

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SECURITY CLASSIFICATION OF THIS PAGE

at the NRL cyclotron facility. The results for this case also demonstrated a lower upset cross section for RAMs fabricated without the n⁻ layer in the speed-up capacitor.

A conceptual design of a new RAM mask set was begun in order to evaluate a wider range of RAM cell configurations. Both 256 and 1K bit arrays are being considered, and emphasis will be placed both on cell designs for enhanced yield and radiation hardness. Enhancement/depletion devices will also be incorporated into the design.

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## SUMMARY

The scope of this program is to demonstrate a 1K GaAs static RAM having very low power dissipation, 1 μW/bit in standby, and short access time, 10 ns, to meet the requirements of the DARPA Advanced On-Board Signal Process (AOSP). High radiation tolerance (total dose and transient radiation) of GaAs circuits is also important for the AOSP application, and it will be evaluated and optimized within this program. In the six month period covered by this report, the processing of 1K RAMs was begun, studies of isolation behavior continued, radiation studies were performed, and the design of a high speed RAM mask was initiated.

The initial three weeks of this semester were spent in reestablishing the process line following the accidental fire of August 1, 1983. A new 10X wafer stepper was received and brought on-line; no problems were encountered in bringing the machine up to acceptance standards. The alloy and anneal furnace tubes, which also experience considerable damage, were replaced and several conditioning runs made to insure proper functionality.

Once all processing equipment was on-line, fabrication of the new mask set RM4 containing 256/1K bit RAM circuits was begun. Four lots were processed with particular emphasis on uniformity and threshold voltage control. The dc parametric data indicated threshold uniformity improvements due primarily to better deposition techniques for the $SiO_2$ layer. However, the magnitude of the threshold voltage was lower than anticipated, and the discrepancy appears to be due either to lower activation in the new anneal furnace, or altered surface conditions following dielectric etching. All other processing parameters appeared normal and consistent with pre-accident data.

Testing of the first lots of RAM wafers yielded a very high failure rate. The problem was traced to a mask error in the peripheral circuitry in which a Schottky-ohmic metal overlay was missing. The masks are currently being modified with an approximate two week turnaround time expected.

The isolation studies for ultra-low power devices contined with major emphasis on isolation degradation following the Schottky metal process. It was found that the metalization step itself was not responsible for the reduction in breakdown voltage, and it appears that the dielectric etching steps play a primary role. A theoretical formulation for the leakage behavior of GaAs substrates was initiated, and good agreement between theory and the experimental data was obtained.

A conceptual design of a new RAM mask set was begun in order to evaluate a wider range of RAM cell configurations. Both 256 and 1K bit arrays are being considered, and emphasis will be placed both on cell designs for enhanced yield and radiation hardness. Enhancement/depletion devices will also be incorporated into the design.

Upset measurements have been made on a number of 256 bit RAMs using an Am-241 alpha particle source. The numerical value for the failure cross section was found to be similar in magnitude to the area of the Schottky barrier speed-up capacitor, suggesting that the capacitor is primarily responsible for the magnitude of the upset cross section. Eliminating the $n^-$ implant in this capacitor reduced both the hold zero and hold one upset rates. However, the cross sections were still substantially larger than the area of the FET gates. More experiments are underway in order to evaluate the charge collection of Schottky metal on semi-insulating GaAs.

Single event upset measurements have also been carried out using 40 MeV protons at the NRL cyclotron facility. The results for this case also demonstrated a lower upset cross section for RAMs fabricated without the $n^-$ layer in the speed-up capacitor. The preliminary data indicates that the susceptibility of the RAM cell to alpha particle radiation may be greatly reduced by relatively small design changes.

## 1.0 INTRODUCTION

The development of a low power radiation hard memory chip is motivated by the DARPA Advanced On-Board Signal Processor (AOSP) program. The goal of this program is to develop a flexible, multi-mission signal processor to fulfill the processing requirements of space-based missions through the 1990's. The AOSP system specification translates into memory device specifications in the following manner. Long mission lifetimes (> 5 years) and space-based environmental conditions require a radiation hardened device technology capable of surviving total doses in excess of $10^6$ rads. Power dissipations of 0.5-1 μW/bit are required due to the large memory sizes and limited power budget. The 4K memory design goals are summarized in Table 1-1.

Table 1-1
AOSP GaAs Memory Design Goals

| Memory Type | Static Random Access |
|---|---|
| Power Dissipation | 1 μW/bit |
| Speed | $\tau_{access}$ < 10 ns |
| Radiation Hardness | > $10^6$ rad total dose |
| Storage Capacity | 4096 bits/chip |

The above requirements are very demanding. They represent a "speed power" product of < 10 fJ/bit.

In the previous GaAs static RAM development program, a low power RAM cell was designed and a 256 bit RAM was demonstrated. The final phase of the previous program provided an opportunity to begin processing 3 in. GaAs wafers. The implementation of the 3 in. wafer process was very successful.

In this report, the results from the second semester of a 21-month program designed to raise the complexity of the GaAs static RAM from 256 to 1K bits with the operating characteristics listed in Table 1-1 are discussed. In

this period, the processing of the 1K RAM design was begun, as well as continued effort in the area of device isolation. The results are discussed in Section 2. Single event upset measurements using both alpha particle sources and 40 MeV protons are discussed in Section 3, while the initial design considerations for the next RAM mask set RM4 are discussed in Section 4.

## 2.0 PROCESS STATUS

The initial three weeks of the semester were spent in reestablishing the process line following the accidental fire of August 1, 1983. A new 10X wafer stepper was received and brought on-line; no problems were encountered in bringing the machine up to acceptance standards. The alloy and anneal furnace tubes and boats, which also experienced considerable damage, were replaced and several conditioning runs made to insure proper functionality. Once all processing equipment was back on-line, fabrication of the new 256/1K bit RAM circuits was begun. In addition, a detailed analytical study of substrate isolation for ultra-low current devices was initiated so that a theoretical formulation could be compared to the observed experimental data.

### 2.1 1K Bit RAM Processing

Since reestablishment of the process line, four wafer lots of the RM4 1K RAM design have been fabricated with particular emphasis on uniformity and threshold voltage. Since these lots were the first wafers to utilize the new equipment, there was uncertainty whether the old process parameters would be valid. The dc parametric data indicated threshold uniformity improvements, due primarily to better deposition techniques for the $SiO_2$ layer. However, the magnitude of the threshold voltage was somewhat lower than anticipated, and the discrepancy appears to be due either to lower activation in the new anneal furnace, or altered surface conditions following dielectric etching. All other processing parameters appeared normal and consistent with pre-accident data. The initial testing of the first lots of RM4 RAM wafers yielded a very high failure rate. The problem was traced to a mask error in the peripheral circuitry in which a Schottky ohmic metal overlay was missing. The masks are currently being modified with an approximate two week turnaround time expected.

## 2.2 Surface Leakage Studies

The semi-insulating GaAs substrate is one of the most important factors in achieving high speed and low power GaAs ICs. It has been recently found that as-grown, undoped semi-insulating GaAs wafers do not remain totally semi-insulating after processing. To understand the mechanism of the substrate leakage, an analytical pseudo two-dimensional multi-conduction path model has been developed to correlate the injection level and the threshold voltage with EL2 and carbon distributions. Good quantitative agreement between the model and isolation test results have been achieved.

### 2.2.1 Multi-Conduction Path Model

It has been known that the substrate leakage current in processed semi-insulating GaAs wafers follows nonlinear injection behavior.[1] However, the observed breakdown voltage is lower than what would be expected from the measured bulk trap concentration based on the carrier injection model.[2] Since the compensation scheme in undoped semi-insulating GaAs is controlled by the balance between EL2 and residual carbon,[3] the major electron traps are EL2 deep donors ionized by carbon acceptors. Nevertheless, EL2 can outdiffuse, dropping in density at the surface approximately two orders of magnitude after thermal annealing.[4,5] In this case, the concentration of empty EL2 (electron traps) in the close vicinity of the surface would be much lower than that in the bulk, and therefore cause a low trap-fill-limited voltage in substrate conduction. Recent experiments have indicated the correlation between the trap-fill-limited voltage and the EL2 distribution.[6,7] According to the compensation scheme in undoped semi-insulating GaAs, the trap density is the same as the carbon concentration when the total EL2 concentration exceeds the carbon level. If the EL2 concentration falls below the carbon level, EL2 would be fully ionized and the substrate converts to p-type.[8] Because of the p-type conversion, the explanation for the low voltage carrier injection through a $n^+$-p-$n^+$ structure becomes nontrivial. To explain the observed nonlinear injection behavior, a multi-conduction path structure for the GaAs substrate has been formulated.

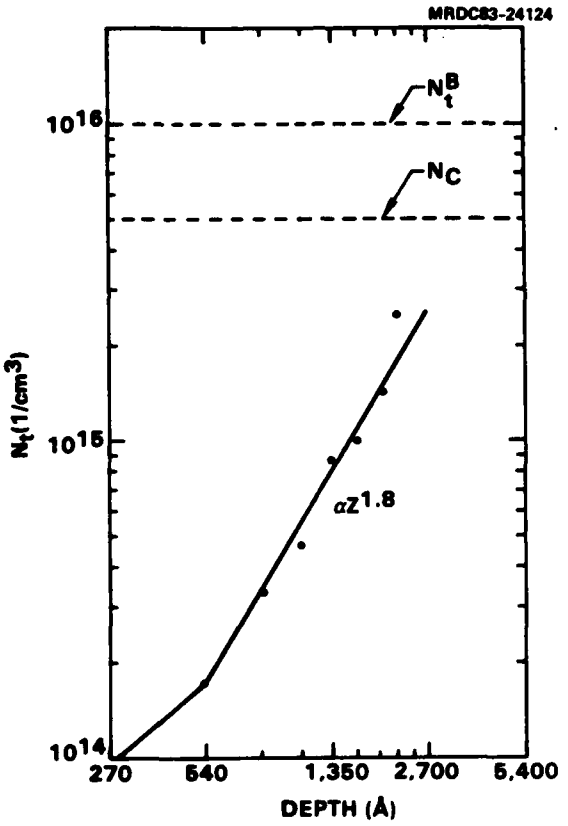


Fig. 2.2-1 Trap concentration as a function of distance from surface.

Previous work has shown that trap-fill-limited SCL injection would not take place unless breakdown of the reverse biased junction occurred. Since the hole concentration of the p-type surface layer is close to the carbon concentration (typically 5 x $10^{15}/cm^3$), the breakdown will not happen until 36 V. Under this condition, the trap-fill-limited voltage is too high to observe any SCL injection at lower voltages. Therefore, it is believed that the low threshold voltage conduction mechanism is due to the existence of a surface potential depleted space-charge region close to the surface, as shown in Fig. 2.2-1. A few thousand angstrom thick space-charge region could be easily formed by assuming a 0.5 eV band bending, which is not unusual for a p-type (100) GaAs wafer after chemical etching.[10] Because all free holes are depleted by the surface potential, the injected electrons fill empty surface traps leading to the trap-fill-limited behavior.

Based on this surface depletion model, the substrate leakage current

can be separated into three components: The space-charge limited (SCL) injection through the surface depletion region ($I_{SCL}$), the reverse saturation current through the $n^+$-p-$n^+$ transistor located underneath the surface depletion zone ($I_R$), and the ohmic leakage current through the bulk of the substrate ($I_{ohm}$). According to this conduction scheme, an analytical pseudo two-dimensional model was developed to correlate the injection level and the threshold voltage with EL2 and carbon distribution.

### 2.2.2 Pseudo Two-Dimensional Treatment on Surface Space-Charge Injection

Since the spacing between two $n^+$ electrodes is smaller than the width of electrodes, the current flowing from the cathode to the anode can be viewed as a two-dimensional boundary value problem. The boundary values for the surface space-charge injection ($I_{SCL}$) can be idealized, as shown in Fig. 2.2-2. The upper surface of the depletion zone is biased by the surface potential, $V_s$, the cathode grounded, and the anode externally biased by $V_a$. In addition, the derivative of the potential should be zero at the bottom layer because the neutral p-type region is underneath.

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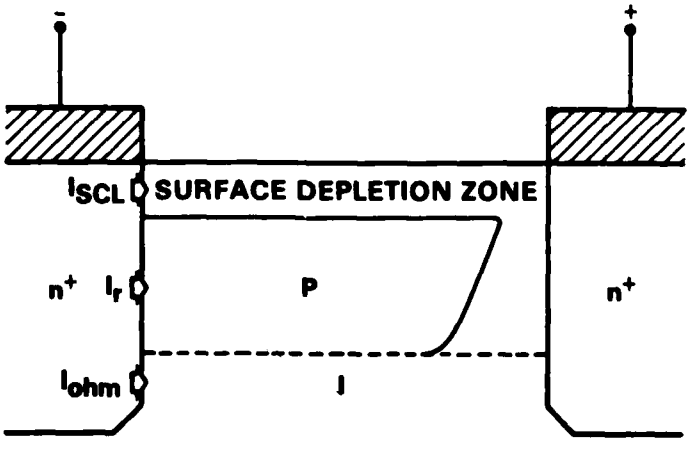



Fig. 2.2-2 Boundary model for surface space-charge injection.

The general equations which determine the injection behavior can be written as

$$\nabla \cdot E(x,y) = -\frac{q}{\varepsilon}\{n + n_t + N_A\} \tag{1}$$

$$\nabla \cdot J_{SCL}(x,y) = 0 \tag{2}$$

$$J^x_{SCL} = q\mu n E_x + qD\frac{\partial n}{\partial x} \tag{3}$$

$$J^y_{SCL} = q\mu n E_y - qD\frac{\partial n}{\partial y} \tag{4}$$

$$n_t = \frac{N_t}{1 + \frac{N}{gn}} \tag{5}$$

$$N = N_c \exp\left[\frac{E_t - E_c}{kT}\right] \tag{6}$$

where the x-direction is horizontal from the cathode to the anode, and the y-direction is vertical from the bottom to the top; $n$ and $n_t$ represent electron population at conduction band and trap levels, respectively. $N_A$ is the acceptor concentration. $J_1$ is the total current flow. $J^x_{SCL}$ and $J^y_{SCL}$ are the components of current flow in horizontal and vertical directions, respectively. $N_t$ stands for the concentration of deep level traps, $N_c$ for the density of state in the conduction band, $E_t$ and $E_c$ for the energy level of trap state and conduction band, respectively. In addition, g is a degeneracy factor for electron population. N is introduced as a matter of convenience.

Unfortunately, it is difficult to find an analytical solution for the previously mentioned equations. Instead of solving these equations numerically, simplifications were made so that the equations could be solved analytically. The simplifications are based on the following assumptions.

1. The surface depletion region is completely depleted by the surface potential.

2. There is no net current flow in the vertical direction. Besides, the horizontal current is mainly contributed by its drift component.
3. The concentration of ionized acceptors ($N_A$), the electron population over the conduction band (n) and the trap level ($n_t$) only vary with depth y.

When the externally applied voltage $V_A$ is much lower than the inter-electrode punch-through voltage, the first assumption is generally correct, except in those areas very close to the anode. Since no net current flows vertically, the cancellation between the drift and the diffusion term of current, $J^y_{SCL}$, would relate the electron population to the vertical field. As the following analysis shows, this relation gives one of the major constraints to the cross sectional area of carrier injection. For simplicity, $N_A$, n and $n_t$ are assumed to vary vertically. Neglect of the diffusion components from $J^x_{SCL}$ is due to the fact that the intereletrode space is often larger than the carrier diffusion length. All these assumptions are made to reduce original equations into a pseudo two-dimensional form and the main features of physics remain intact. The simplified equations can be rewritten as follows:

Assuming

$$\frac{\partial E_y}{\partial_y} = -\frac{q}{\varepsilon} N_A(y) \quad . \tag{7}$$

Then, for certain depth y down from the surface, Eq. (1) becomes

$$\frac{\partial E_x}{\partial_x} = -\frac{q}{\varepsilon} \{n(y) + n_t(y)\} \tag{8}$$

and the equation of continuity is reduced to

$$J^x_{SCL} = q\mu n E_x = \text{constant} \tag{9}$$

with a constraint

$$n(y) = n(o) \exp \left[ - \frac{1}{kT} \left(\frac{q^2}{\varepsilon}\right) N_A \left(dy - \frac{y^2}{2}\right)\right] \qquad (10$$

where n(o) is the electron concentration at the top surface, and d is the depth of depletion zone. Equations (7), (8) and (10) are then used to calculate the space-charge injection through a trapped depletion region.

Traps are viewed as "shallow" or "deep" based on the injection level. As the injection level increases, the Fermi level ($E_f$) moves up in the forbidden gap toward the conduction. When it moves through a trap level, the trap which used to be shallow, becomes deep. Therefore, the injection behavior of SCL current could be categorized into three limiting cases.

Case of Shallow Trapping

As long as $E_f$ lies below $E_t$ by more than kT, $1 + N/gn \approx \frac{N}{gn}$ and the traps are said to be "shallow". The ratio of free to trapped electron densities is a constant $\theta$ which is independent of n and expressed as

$$\theta = \frac{n(y)}{n_t(y)} = \frac{N}{gN_t} \quad . \qquad (11)$$

Those shallow traps are important for which $\theta << 1$, since most injected electrons are immobilized in such traps. For the case of EL2 traps, $E_t = E_c$ -0.83 eV so that

$$\theta = \frac{1.88 \times 10^3}{N_t} \quad . \qquad (12)$$

With a typical trap concentration of EL2 of $10^{14}/cm^3$ on the surface and $10^{16}/cm^3$ in the bulk, $\theta$ is insignificant. Putting Eq. (12) into the Poisson equation,

$$\frac{\partial E_x(y)}{\partial_x} = - \frac{q}{\varepsilon} \frac{n(y)}{\theta} \quad . \qquad (13)$$

Combining Eq. (13) with the current Eq. (9) and assuming $E_x = 0$ at $x = 0$, the current density of SCL injection in the shallow trap case becomes

$$J_{SCL}^{x}(y) = 2.25 \times 10^{3} \cdot \frac{\mu\varepsilon V_a^{2}}{W^{3} N_t(y)} \tag{14}$$

where W is the width of depletion region. With a reasonable estimation of EL2 distribution,[11]

$$N_t(y) = N_t^{S} + (N_t^{B} - N_t^{S}) \left(\frac{y}{y_o}\right)^{2} \tag{15}$$

where $N_t^{S}$ and $N_t^{B}$ represent EL2 concentration on the surface and in the bulk, respectively. $y_o$ is the depth of the EL2 outdiffusion zone. By integrating the injection carrier density over the whole depletion depth, the total current per unit width can be derived as

$$I_{SCL} = \int_{o}^{d} J_{SCL}^{x}(y)\, dy \tag{16}$$

$$= 2.25 \times 10^{3} \frac{\mu\varepsilon V_a^{2}}{W^{3}} \frac{y_o}{\sqrt{N_t^{S}(N_t^{B} - N_t^{S})}} \left\{\tan^{-1}\left[\left(\frac{N_t^{B} - N_t^{S}}{N_t^{S}}\right)^{1/2} \left(\frac{d}{y_o}\right)\right]\right\}$$

In the case

$$\left(\frac{N_t^{B} - N_t^{S}}{N_t^{S}}\right)^{1/2} \left(\frac{d}{y_o}\right) \ll 1 \text{ , Eq. (16) is deduced as}$$

$$I_{SCL} = 2.25 \times 10^{3} \frac{\mu\varepsilon V_a^{2} d}{W^{3} N_t^{S}} \quad . \tag{17}$$

In Eq. (15), the upper limit of current integration is determined by two constraints. The first constraint is the depth of the surface depletion zone

which, in first order, can be estimated as

$$d_1 \sqrt{\frac{2\epsilon V_S}{q(n_c - N_t^S)}} \tag{18}$$

where $n_c$ is the density of residual carbon acceptors. The second constraint comes from the psuedo two-dimensional assumption in which no net current flows vertically. This constraint confines all electron carriers into a surface conduction layer with thickness

$$d_z = d_1 - \sqrt{d_1^2 - \frac{2D\epsilon}{\mu q N_A}} \tag{19}$$

which is always smaller than $d_1$, thus $d = d_2$. In a representative case, assuming $D = 130$, $\epsilon = 1.1 \times 10^{-12}$, $\mu = 5 \times 10^3$, $q = 1.6 \times 10^{-19}$ coul., $N_A = 5 \times 10^{15}/cm^3$, the magnitude of d is around $10^2$A.

Case of Deep Trapping

If $E_f$ lies above $E_t$ by more than kT, $1 + \frac{N}{gn}$, the traps are said to be "deep", and they are filled with electrons. In this case,

$\frac{E_f - E_t}{kT} > 1$, which implies

$$n_t(y) \approx N_t(y) \tag{20}$$

and the field equation can be rewritten as

$$\frac{\partial E_x(y)}{\partial_x} = -\frac{q}{\epsilon}\{n(y) + N_t(y)\} \quad . \tag{21}$$

Manipulating Eqs. (18) and (19), the current density of SCL injection in the "deep" trap case can be found as

$$J^{x}_{SCL}(y) \approx \frac{9}{8}\frac{\mu\varepsilon V_a^2}{W^3} - q\mu N_t(y)\left(\frac{V_a}{W}\right) \quad . \tag{22}$$

After a number ($N_t$) of deep traps have been filled, all carriers would be injected into the conduction band leading to trap-fill-limited SCL current. In addition, three constraints need to be fulfilled to integrate the total injection current. The first constraint comes from the fact that $J_{SCL}$ should remain positive or zero. In other words, integration can be started from the surface down to certain depth, $d_3$, which would satisfy the condition

$$J^{x}_{SCL}(d_3) = 0 \quad . \tag{23}$$

Substituting Eq. (23) into Eqs. (22) and (15), $d_3$ can be expressed as

$$d_3 \quad y_o\sqrt{\frac{7.5 \times 10^6\left(\frac{V_a}{W^2}\right) - N_t^S}{N_t^B}} \quad . \tag{24}$$

The other two constraints are the same as the constraints in the previous case. During the integration, the upper limit, d, is determined by the smallest one among $d_1$, $d_2$ and $d_3$. The total SCL current in the deep trap case can now be represented as

$$\begin{aligned} I_{SCL} &= \int_0^d J^{x}_{SCL}(y)\, dy \\ &= \frac{9}{8}\frac{\mu\varepsilon V_a^2}{W^3}\, d - \frac{q\mu Va}{W}\, d\left[N_t^S + \frac{N_t^B - N_t^S}{3}\left(\frac{d}{y_o}\right)^2\right] \quad . \end{aligned} \tag{25}$$

Case of "Shallow" to "Deep" Transition

During the transition, once the injection level changes so rapidly, no simple form could be addressed for current injection. In the present case, the Fermi level moves across the trap level when the injection increases. From the classical trap-fill-limited law of Lampert,[12] the transition would take place at $V_{TFL}$, which is

$$V_{TFL} = \frac{qN_t^S}{C} \tag{26}$$

where C is the capacitance per unit area seen between cathode and anode. As illustrated in Fig. 2.2-3, the SCL flow switches suddenly from one limiting case (shallow trap or low injection) to another limiting case (deep trap or high injection). At $V_{TFL}$, the ratio between the deep trap injection and shallow trap injection is as much as the magnitude of $\frac{1}{\theta}$.

## 2.2.3 Reverse Saturation Current Through $n^+$-p-$n^+$

For a nearly floating base transistor, the major current is contributed by the collector reverse saturation current due to the bias voltage drop across the collector space-charge region. Therefore, the current can be expressed by

$$J_r = \left(\frac{qD_nD_p}{L_n} + \frac{qD_pP_n}{L_p}\right) \quad \left(e^{-\frac{qVa}{kT}} - 1\right) \quad . \tag{27}$$

In case $V_a$ >> 26 mV, $J_r$ becomes

$$J_r = \frac{qD_nN_p}{L_n} + \frac{qD_pP_n}{L_p} \tag{28}$$

where $D_n$ and $D_p$ are diffusion constants for electrons and holes, respectively. $L_n$ represents minority carrier diffusion length for the electron and $L_p$ for holes. $N_p$ is the concentration in the base region, and $P_n$ the hole concentration in the collection region. In case of room temperature, $n_i^2 = 10^{14}/cm^6$,

$P \approx 5 \times 10^{15}/cm^3$, $L_n \approx 5 \times 10^{-4}$ cm, $L_p \approx 3 \times 10^{-4}$ cm, $D_n = 130$, $D_p \approx 10$, $N_p \frac{n_i^2}{p}$, $P_n = \frac{n_i^2}{n}$, and the magnitude of $J_r$ is approximately equal to $8 \times 10^{-16}/cm^2$. As shown in Fig. 2.2-3, $J_r$ is too small to be responsible for the substrate leakage.

### 2.2.4 Bulk Leakage Current

Although EL2 outdiffusion can cause surface leakage, the concentration remains high in the bulk ($5 \times 10^{15}/cm^3$, typically). Since the trap-fill-limited voltage ($V_{TFL}$) is linearly proportional to deep level trap density, the bulk $V_{TFL}$ should be much higher than its surface counterpart. Therefore,

$$V_{TFL}^{(bulk)} = \left(\frac{N_t^B}{N_t^S}\right) \cdot V_{TFL}^{(surface)} \quad . \tag{29}$$

Previous work has demonstrated $\frac{N_t^B}{N_t^S} \approx 10^2$ after thermal annealing. Under such circumstances, the bulk leakage current does not initiate trap-fill-limited SCL injection for substrate leakage. However, the existence of unintentionally doped Si shallow donors would deliver free electrons to the conduction band to contribute to the ohmic current,

$$J_{ohm} = qn\mu E_x \quad . \tag{30}$$

For a typical undoped semi-insulating GaAs wafer ($10^8$ Ω-cm resistivity), the residual donor concentration is about $10^7/cm^3$. The calculated current densities are illustrated in Fig. 2.2-3. It is interesting to find that for $V < V_{TFL}$, ohmic current through the bulk dominates, while for voltages higher than $V_{TFL}$, the injection through the surface depletion zone dominates.

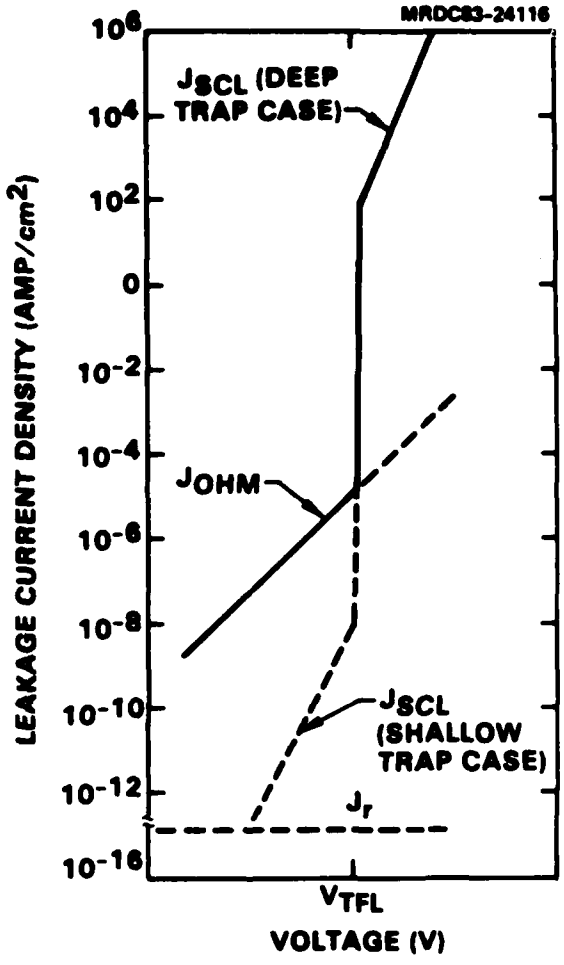



Fig. 2.2-3 Surface conduction mechanism in SI GaAs.

## 2.2.5 Experiments

Two experiments were carried out to check the accuracy of the multi-conduction path model. The purpose of the first experiment was to determine if EL2 or carbon correlated with $V_{TFL}$. Four wafers were processed for the isolation measurements. As shown in Table 2.2-1, the EL2 concentrations were varied from $4.8 \times 10^{15}/cm^3$ to $2.3 \times 10^{16}/cm^3$, and the carbon concentrations were varied from $7 \times 10^{15}/cm^3$ to $4.6 \times 10^{16}/cm^3$. These wafers were checked as semi-insulating before processing. After processing, three possible situations were expected: 1) the $V_{TFL}$ correlates with carbon concentration, but not EL2 concentration, 2) the $V_{TFL}$ correlates with EL2 concentration, but not carbon concentration, and 3) the $V_{TFL}$ does not correlate with either EL2 or carbon concentrations.

Table 2.2-1

$V_{TFL}$ Voltage vs EL2 and Carbon

| Wafer No. | Carbon | EL2 | $V_{TFL}$ |
|---|---|---|---|
| 1 | $4.6 \times 10^{16}$ | $1.6 \times 10^{16}$ | 4 ~ 6 V |
| 2 | $5.4 \times 10^{15}$ | $2.3 \times 10^{16}$ | 6.5 ~ 7.5 V |
| 3* | $5.4 \times 10^{15}$ | $2.3 \times 10^{16}$ | 6.5 ~ 7 V |
| 4 | $7 \times 10^{15}$ | $4.8 \times 10^{15}$ | 1.6 ~ 3 V |

* Surface treated with hot $H_3PO_4$ before $Si_3N_4$ cap.

The results showed that there was no correlation between $V_{TFL}$ and carbon concentration, but that the correlation between $V_{TFL}$ and EL2 concentrations was very strong. Thus, the higher the EL2 level, the higher the $V_{TFL}$. The experiment also rules out the prospect of exterior contamination, and favors the scenario for reduced surface EL2 concentration.

The second experiment quantitatively checked the injection level with 3 μm spaced isolation devices. Results are shown in Fig. 2.2-4; the solid line shows experimental data, and the dashed line shows calculated results based on measured $V_{TFL}$ and the conduction model. Very close agreement was achieved; for $V < V_{TFL}$ bulk ohmic current dominates, while $V > V_{TFL}$ surface SCL dominates.

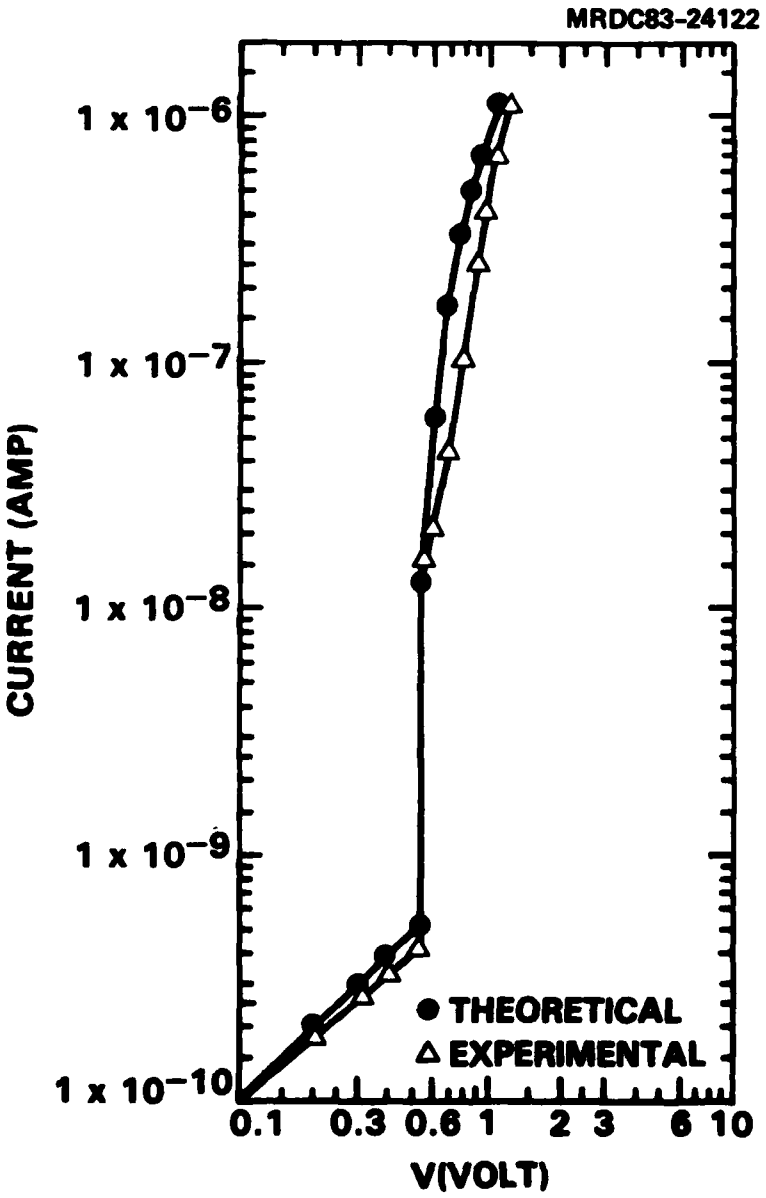



Fig. 2.2-4 Comparison of isolation model to experimental data.

# 3.0 SINGLE EVENT UPSET MEASUREMENTS

Single event upsets can occur in a RAM when sufficient charge from the path of an incident ion is collected at a critical node of a RAM cell such that the cell switches state from a zero to a one or vice versa. The critical charge, $Q_C$, required to produce such a change is related to the voltage change at the node, $V_C$, and the node capacitance, C, by the following relation:

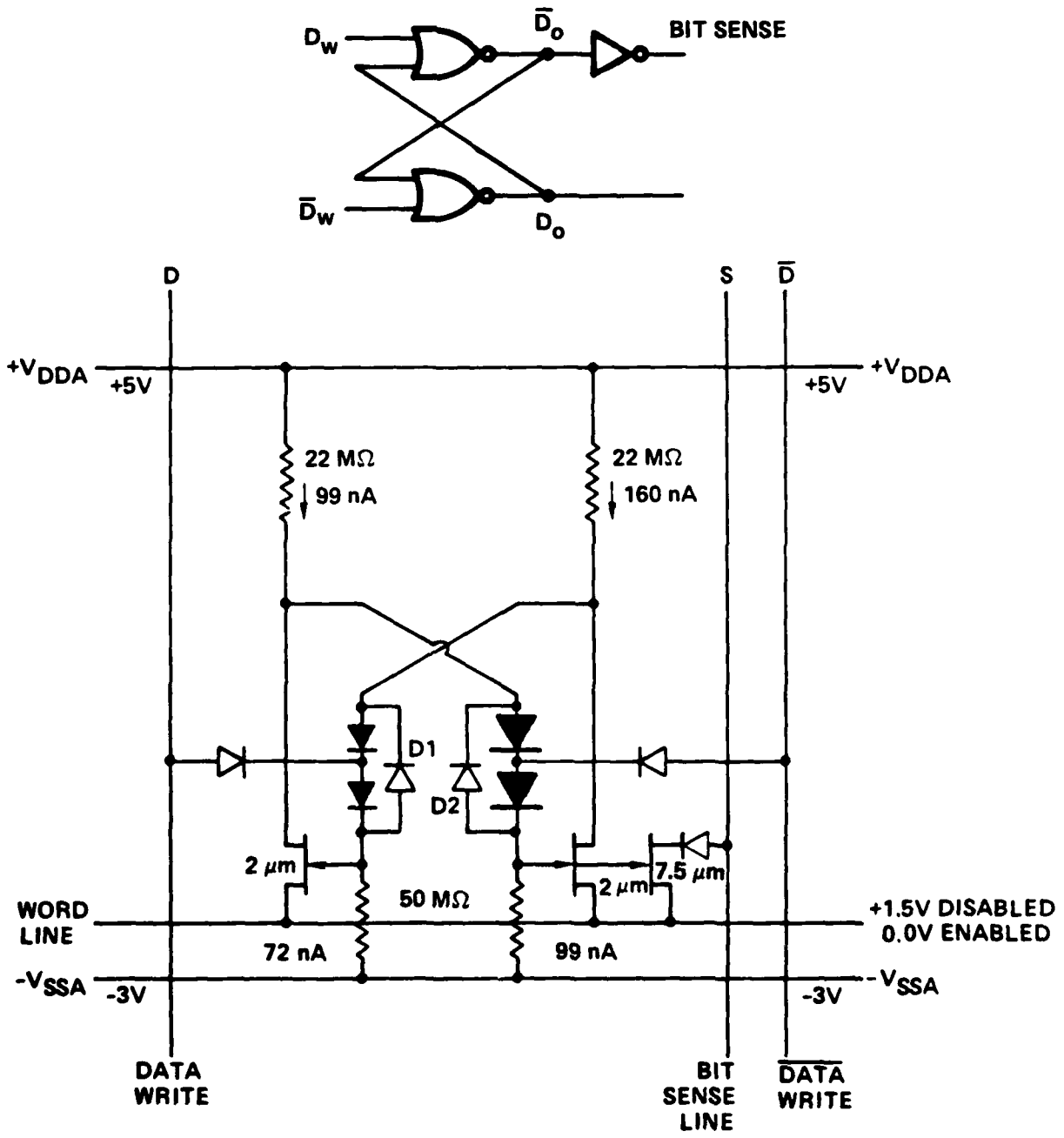
$$Q_C = C\ V_C \quad .$$

The kinds of particles which have been observed to produce single event upsets include alpha particles and heavier high energy ions, which produce a high charge density along their track in a semiconductor material. High energy protons produce nuclear reactions in the semiconductor, yielding high energy alpha particles and recoil ions, both of which may be capable of causing single event upsets.

The critical node in the 256 bit RAM is believed to be the gate of the FET in the flip-flop of the RAM cell which is biased off. Ionizing particles which pass through the gate region of this FET may produce upsets if sufficient charge is collected by the gate. From the schematic of the RAM cell shown in Fig. 3.0-1, it can be seen that there is a Schottky diode connected to the gate of each of the transistors. This diode serves as a speed-up capacitor. The area of the diode is much larger than the area of the FET gate so that the cross section for upset would be expected to be determined primarily by the area of the speed-up capacitor diode rather than the FET gate area.

## 3.1 Alpha Particle Measurements

Upset measurements have been made on a number of 256 bit RAMs using an Am-241 alpha particle source. The measurement consisted of storing either all zeros or all ones in the cells of the RAM, exposing it to alpha particle radiation for a given period of time, and then reading each cell to determine




**POWER/BIT = (+5) (529) + (-3) (-171) = 1.81 μW/BIT**
**MEMORY ARRAY STATIC POWER = 4096 x 1.81 x $10^{-6}$ = 7.4 mW/4K CHIP**

Fig. 3.0-1 Cell for 256 bit GaAs static RAM.

the number of cells which had changed state as a result of the alpha particle irradiation. Data for several RAMs are presented in Table 3.1-1 in terms of the cross sections for failure to hold a zero or failure to hold a one. The numerical value of these cross sections is similar in magnitude to the area of the Schottky barrier speed-up capacitor, suggesting that this capacitor is primarily responsible for the magnitude of the upset cross section. In an attempt to confirm this hypothesis, an experiment was carried out in which RAMs were processed without the implant for the Schottky diode speed-up capacitor. However, the metalization for this capacitor was deposited during the processing so that the Schottky barrier metal in these devices lies on semi-insulating GaAs rather than on GaAs which has been doped n-type by ion implantation. Alpha particle upset cross sections for these devices are listed in Table 3.1-2. Both the hold zero and hold one cross sections were reduced as a result of this change. However, these cross sections are still substantially larger than the area of the FET gate. It is believed that is is associated with the fact that reduction of the capacitor connected to the FET gate decreases the critical charge, and makes it possible for upsets to occur as a result of collection of substantially smaller charge then when the speed-up capacitor is present. Such charge may be collected, for example, by the Schottky barrier metal of the unimplanted diode which lies on semi-insulating GaAs. Charge collection experiments of the type described below indicate that some charge collection will occur in such a structure.

Table 3.1-1
Upset Cross Sections for Alpha Particles

| With Diode Implant | Hold 0 | Hold 1 |
|---|---|---|
| 62-53-22-2 | 155 $\mu m^2$ | 141 $\mu m^2$ |
| 101-65-33-1 | 181 $\mu m^2$ | 165 $\mu m^2$ |
| 152-55-31-2<br>152-54-33-2 | 143 $\mu m^2$ | 143 $\mu m^2$ |
| 143-64-33-1 | 195 $\mu m^2$ | 168 $\mu m^2$ |

Table 3.1-2

Upset Cross Sections for Alpha Particles

| With Diode Implant | Hold 0 | Hold 1 |
|---|---|---|
| 152-55-21-2<br>152-54-23-2 | 19 $\mu m^2$ | 75 $\mu m^2$ |
| 143-45-22-1 | 27 $\mu m^2$ | 114 $\mu m^2$ |

It is of interest to know the magnitude of charge which may be collected from an alpha particle track in the GaAs RAMs. In order to investigate this, experiments were carried out in which a fat FET connected as a diode was irradiated with alpha particles. The device was connected to a charge sensitive amplifier and the output of the amplifier fed to a pulse height analyzer, as illustrated in Fig. 3.1-1. Typical data are shown in Fig. 3.1-2 where the spectrum represented by the filled dots was obtained from the Am-241 source.

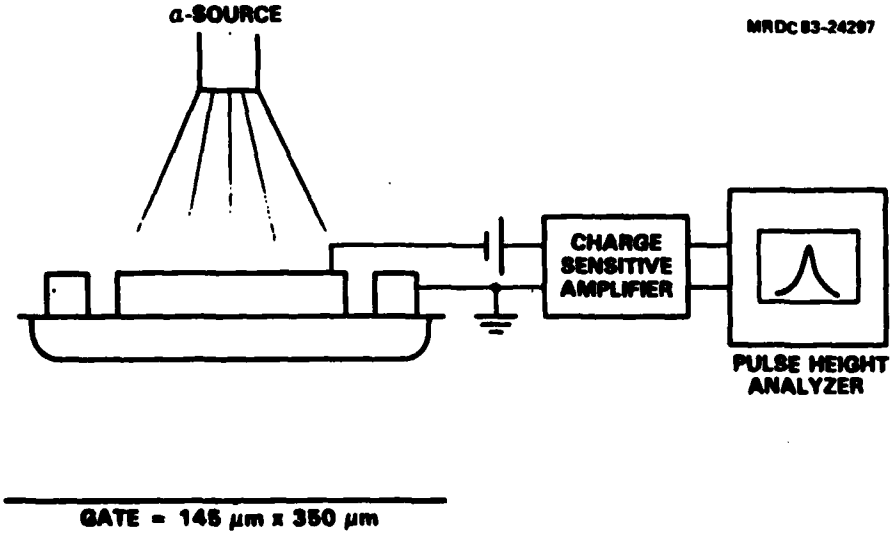



Fig. 3.1-1 Illustration of charge collection experiment.

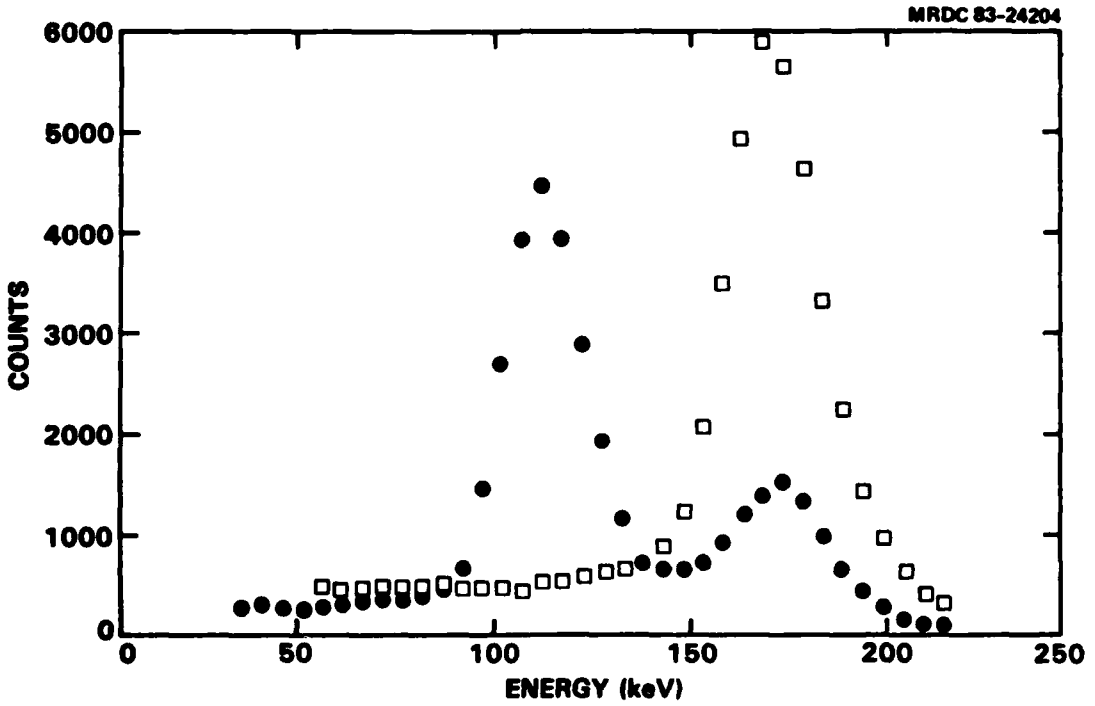



Fig. 3.1-2 Charge collection spectra for fat FETs irradiated with alpha particles. Solid circles are for alphas from the Am-241 source and open squares are for the Cm-244 source covered with a 1 mil mylar absorber.

The two peaks seen in this spectrum are thought to be a result of the shape of the energy spectrum of the alpha particles from the Am-241 source, shown in Fig. 3.1-3. The alphas in the high energy peak have lower energy loss in the GaAs and produce the lower energy peak in the charge collection spectrum, whereas those in the low energy tail which have a higher energy loss rate in the GaAs produce the peak at the higher energy. This hypothesis has been checked by irradiating fat FETs with a Cm-244 source covered with a 1 mil thick mylar absorber. The spectrum from this source with the absorber is also shown in Fig. 3.1-3. It can be seen that only alphas with energies below about 1 MeV would be incident upon the fat FET test device. The resulting

MRDC83-24174

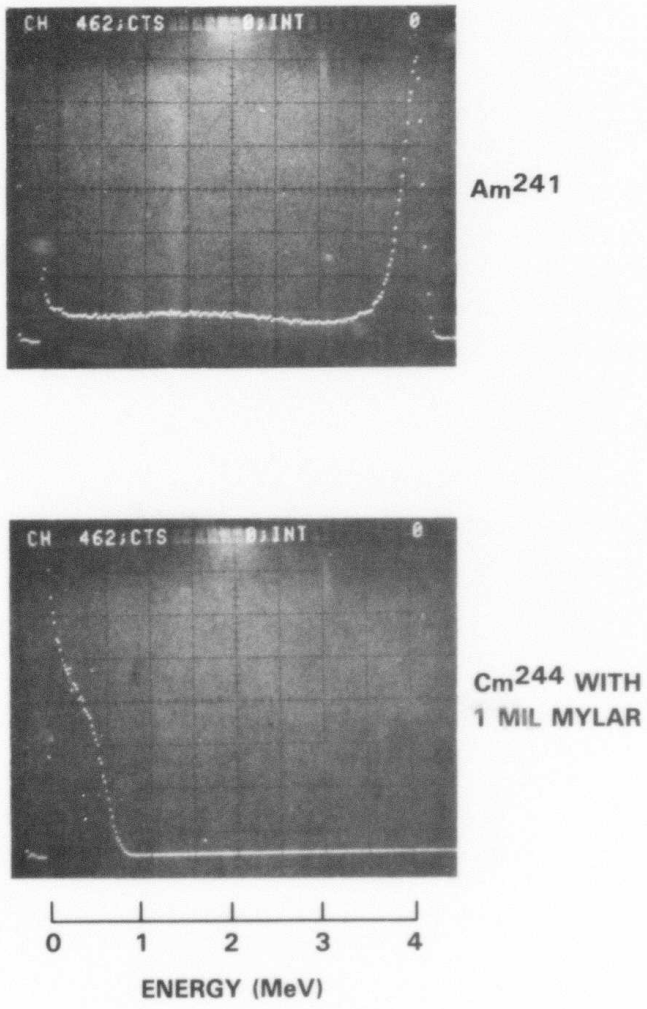



Fig. 3.1-3 Alpha particle energy spectra for the sources as labeled.

spectrum is the one shown by the open squares in Fig. 3.1-2, which consists primarily of a peak at the same energy as the higher energy peak produced by the Am-241 source. It is therefore believed that the two peaks in the Am-produced spectrum result from the energy spectrum of the incident alphas rather than being an artifact of the geometry of the test device. The magnitude of the charge collected (about 7.5 fC maximum) is consistent with collection from an effective depth of about 0.5 μm.

## 3.2 40 MeV Proton Measurements

Single event upset measurements have also been carried out using 40 MeV protons from the NRL cyclotron. The data from these measurements are shown in Table 3.2-1, where results both with and without the diode implant are presented. In this case also, the cross sections are smaller for the RAMs which did not have the diode implant. However, the asymmetry between hold zero and hold one failures is opposite to that exhibited in the alpha particle irradiation. This observation is not understood at present. The asymmetry in the alpha particle case seemed consistent with asymmetries in geometry present in the RAM cell.

Table 3.2-1

Upset Cross Sections for 40 MeV Protons ($cm^2$/proton-bit)

| With Diode Implant | Hold 0 | Hold 1 |
|---|---|---|
| 62-43-22-2 | $2.5 \times 10^{-10}$ | $2.3 \times 10^{-10}$ |
| 62-43-21-1 | $1.5 \times 10^{-10}$ | $2.5 \times 10^{-10}$ |
| 62-53-22-2 | $4.5 \times 10^{-10}$ | $2.8 \times 10^{-10}$ |
| 101-55-21-1 | $7.9 \times 10^{-10}$ | $7.9 \times 10^{-10}$ |
| **Without Diode Implant** | | |
| 152-56-21-2 | $4.8 \times 10^{-11}$ | $1.4 \times 10^{-10}$ |
| 152-55-21-1 | $2.3 \times 10^{-11}$ | $7.7 \times 10^{-11}$ |

The upset cross sections measured in the 40 MeV proton experiments are higher than for most other RAM circuits which have been measured with such irradiation. However, it is encouraging to note that a rough estimate of the critical charge gives a result of about 6.5 fC. This value is only slightly smaller than the maximum charge collected in the charge collection experiment on the fat FETs. This result may indicate that the susceptibility of the RAM to alpha particle radiation can be greatly decreased by relatively small design changes, i.e., doubling voltage swing. A significant decrease in alpha particle susceptibility would be expected to result in a decrease in the cross section for upset by 40 MeV protons, since alpha particles from the nuclear reactions in the GaAs are responsible for a significant fraction of the upsets resulting from the proton irradiation.

## 4.0 RM5 MASK DESIGN

In order to provide RAM circuits with higher fabrication yields and improved radiation resistance, the next RAM mask, RM5, incorporates new call approaches. Several 256 bit circuits will be included to evaulate the impact of both design and processing parameters. An optimized 1K circuit will also be placed on RM5.

In a move which is anticipated to significantly improve RAM device yields, a new cell approach utilizing a transmission gate concept will be explored. This is envisioned to be a conservative step, with two transmission gates in a symmetrical design. This symmetry is expected to improve cell radiation hardness. The cell utilizes all transistor loads and is designed for a 1 V threshold voltage. Although it is estimated that this approach will result in 16% more complexity per cell, the use of active loads and higher threshold voltage are anticipated to result in very significant yield improvements. The deletion of the additional fabrication steps related to cermet resistor formation alone would improve the yield prognosis. The speed performance of this cell is expected to be excellent with predicted read or write times ~ 2 nsec. Although the penalty in power for this approach is significant, the desired goal of this study, the determination of the importance of selected design/fabrication parameters on yield, is expected to result.

In a different direction, a second cell approach will be included on RM5 which utilizes an enhancement/depletion (E/D) approach. In this design, an enhancement approach is used for the memory cell, and a depletion approach for the peripherals. This results in a very compact device (30 x 35 $\mu$) occupying only 60% of the area of 256 bit RAMs of previous designs. The small area of this device is expected to result in significant yield improvements. Simulation indicate that a 1K design with this E/D approach will offer advantages in power as well, with ~ 10-20 $\mu$W/bit projected dissipation. The goal of this design is 2 nsec access time.

The enhancement approach will be accomplished by recessing, most likely by reactive ion etching. Experience has already been gained in dry recessing technique development in IR&D activities. Resistors will be formed with the cermet process, with 200-500K Ω values required. The enhancement model memory cell has a voltage swing of only 0.7 V the depletion model peripherals with a swing of 1.5 V, providing larger charging capability.

In a third approach, as shown in Fig. 4.0-1, a transmission gate design also employs cermet resistors. With this lower power, lower speed (> 10 nsec) circuit, the threshold voltages will be 0.5 V, with resistors < 4 M-Ω. This approach shows promise as a low power, rad hard design.

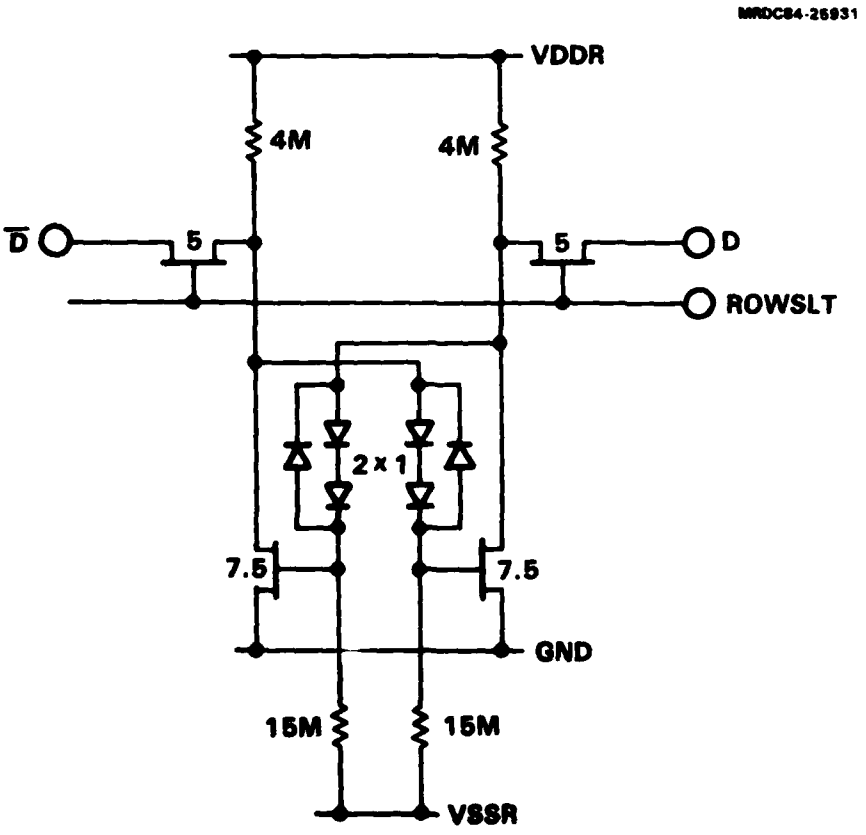



Fig. 4.0-1 Low power transmission gate cell approach.

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