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## APPENDIX B

# LSI/VLSI ION IMPLANTED GaAs IC PROCESSING

**FINAL REPORT FOR THE PERIOD**
**July 25, 1980 through September 30, 1982**



Prepared for
Defense Advanced Research Projects Agency (DoD)
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Arlington, VA 22209

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Rockwell International

**APPENDIX B**

# FINAL REPORT

# ON

# TWO-DIMENSIONAL MODELING OF GaAs MESFET DEVICES FOR INTEGRATED HIGH-SPEED LOGIC CIRCUITS

**Submitted to Rockwell International**
**Microelectronics Research and Development Center**

**in connection with Rockwell International Program on**
**"LSI-VLSI Ion Implanted Planar GaAs IC Processing"**

**Period: January 1, 1981 - September 30, 1982**

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# 1.0 INTRODUCTION

This report summarizes the research carried out at North Carolina State University in support of the Rockwell International Program on "LSI-VLSI Ion Implanted Planar GaAs IC Processing." The major thrust of the program at NCSU was to develop accurate computer models for analyzing the performance of short-channel GaAs MESFET devices as used in the Rockwell VLSI circuits.

The modeling research is divided into three parts:

1. Two-dimensional finite difference simulation,
2. Two-dimensional Monte Carlo analysis,
3. Analytical modeling.

The intent was to use the two-dimensional analyses to give exact solutions to the device operation and to serve as a guide for developing a simpler, and less expensive, analytical model of sufficient accuracy to be valuable as a design aid and to study effects of parameter changes.

In addition, work has been carried out in the characterization of material and device properties using C-V and DLTS techniques.

In general, significant results have been obtained in all phases of the program. The following sections of the report describe the research program in detail and summarize the main conclusions resulting from the investigations.



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# 2.0 TWO-DIMENSIONAL NUMERICAL MODELING

This phase of the research has been devoted to two-dimensional modeling of ion implanted FETs using a conventional finite difference approach and a static velocity-field relationship. The basic device structure considered is shown in Figure 2.1. It consists of a semi-insulating GaAs substrate in which a thin ion implanted channel is formed near the surface. Source and drain contacts are heavily doped regions symmetrically placed about the gate region and extending below the implanted channel. The device structure and typical dimensions shown in Figure 2.1 are based upon the device structure used by Rockwell International on the "LSI-VLSI Ion Implanted Planar GaAs IC Processing" research program. Variations to the basic structure have been considered and are reported in more detail in the following discussion.

## 2.1 Fundamental Device Equations

The fundamental device equations used in modeling the MESFETs are given by:

$$\frac{\partial^2\phi}{\partial x^2} + \frac{\partial^2\phi}{\partial y^2} = -\frac{q}{\varepsilon_o\varepsilon_s}(N_d(y) - n), \tag{2.1}$$

$$\vec{E} = -\nabla\phi, \tag{2.2}$$

$$\tau = \frac{m}{q}\mu, \tag{2.3}$$

$$\frac{d\vec{J}}{dt} + \frac{\vec{J}}{\tau} = -\frac{\mu}{\tau}\left[n\vec{E} + \frac{kT}{q}\nabla r \cdot n\right], \tag{2.4}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \vec{J}, \tag{2.5}$$

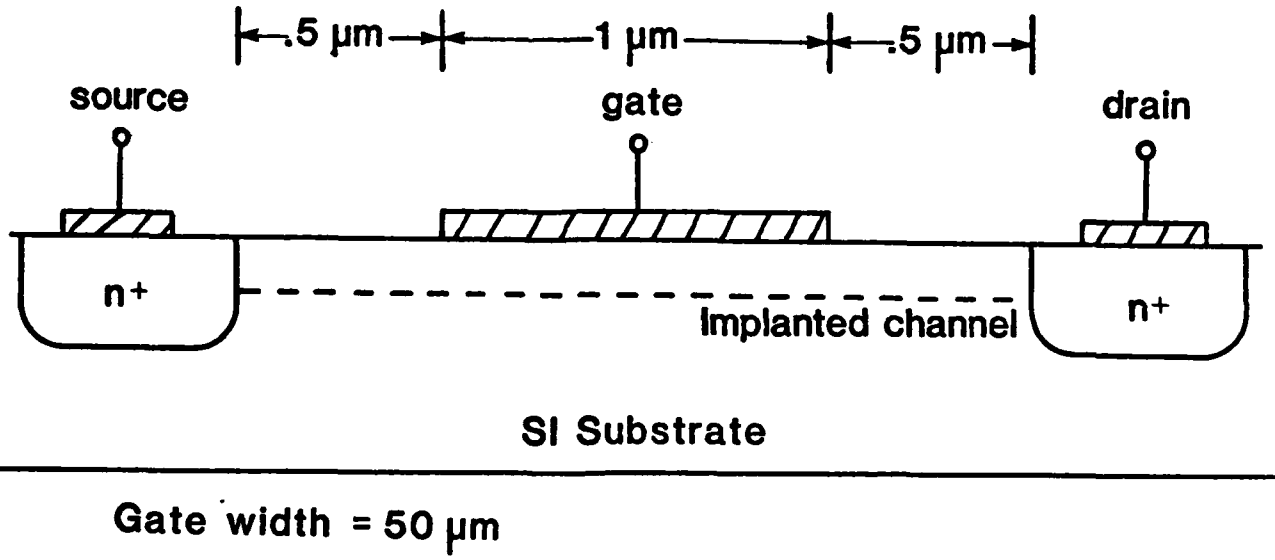


Figure 2.1 MESFET device structure. Dimensions shown are those used in calculations unless otherwise noted in text.

$\phi$ = electric potential

$q$ = electronic charge

$\varepsilon_o$ = permittivity of free space

$\varepsilon_o$ = relative premittivity of semiconductor material

$N_d$ = impurity profile

$n$ = electron density

$E$ = total electric field

$\mu$ = mobility

$J$ = current density

$k$ = Boltzman's constant

$T$ = room temperature

$\tau$ = average collision time

In these equations, holes have been neglected as the GaAs MESFET is basically an electron majority carrier device. Equation (2.1) is Poisson's equation relating potential to charge density. In some of the calculations, the effects of electron traps were considered. In this case, n on the right hand side of Equation (2.1) was replaced by $n + n_t$ where $n_t$ can be expressed as a function of n as

$$n_t = N_t\left(\frac{n}{n+n_1}\right) , \tag{2.6}$$

where $N_t$ is the trap density and $n_1$ is a constant depending on the location of the trap ($E_t$) within the energy band, i.e.

$$n_1 = N_c \exp(-E_c-E_t)/kT) . \tag{2.7}$$

As long as n is large, compared with $n_1$, essentially all of the traps will be occupied.

Equation (2.4) is a time dependent current-density equation which is derived from Boltzman's transport equation considering time-dependent effects. In steady state it is seen that Equation (2.4) becomes independent of $\tau$ and reduces to the more familiar expression relating current density to electric field and electron density gradient. In Equation (2.4), $\tau$ is a time constant related to the transient effects and as given by Equation (2.3) is the mobility relaxation time. Finally, Equation (2.5) is the continuity equation for current density in the time-dependent case.

The mobility in Equation (2.4) is both doping and field dependent. In this work various empirical relationships have been used to model this parameter. The parameter usually modeled is drift velocity ($v=\mu E$) expressed as a function of electric field and doping density. Figure 2.2 shows several velocity-field relationships. Curves a and b are for an empirical relationship of the form

$$v = \frac{\mu_o E + v_s (E/E_o)^4}{1 + (E/E_o)^4} \quad , \qquad 2.8$$

with the following parameters

curve a: $\mu_o = 8000\ cm^2/v \cdot sec$

$v_s = 8.5 \times 10^6\ cm/sec$

$E_o = 4\ kV/cm$

curve b: $\mu_o = 4500\ cm^2/v \cdot sec$

$v_s = 8.5 \times 10^6\ cm/sec$

$E_o = 4kV/cm$

There two curves approach the same high-field saturation velocity but have considerably different low-field mobilities and peak velocities.

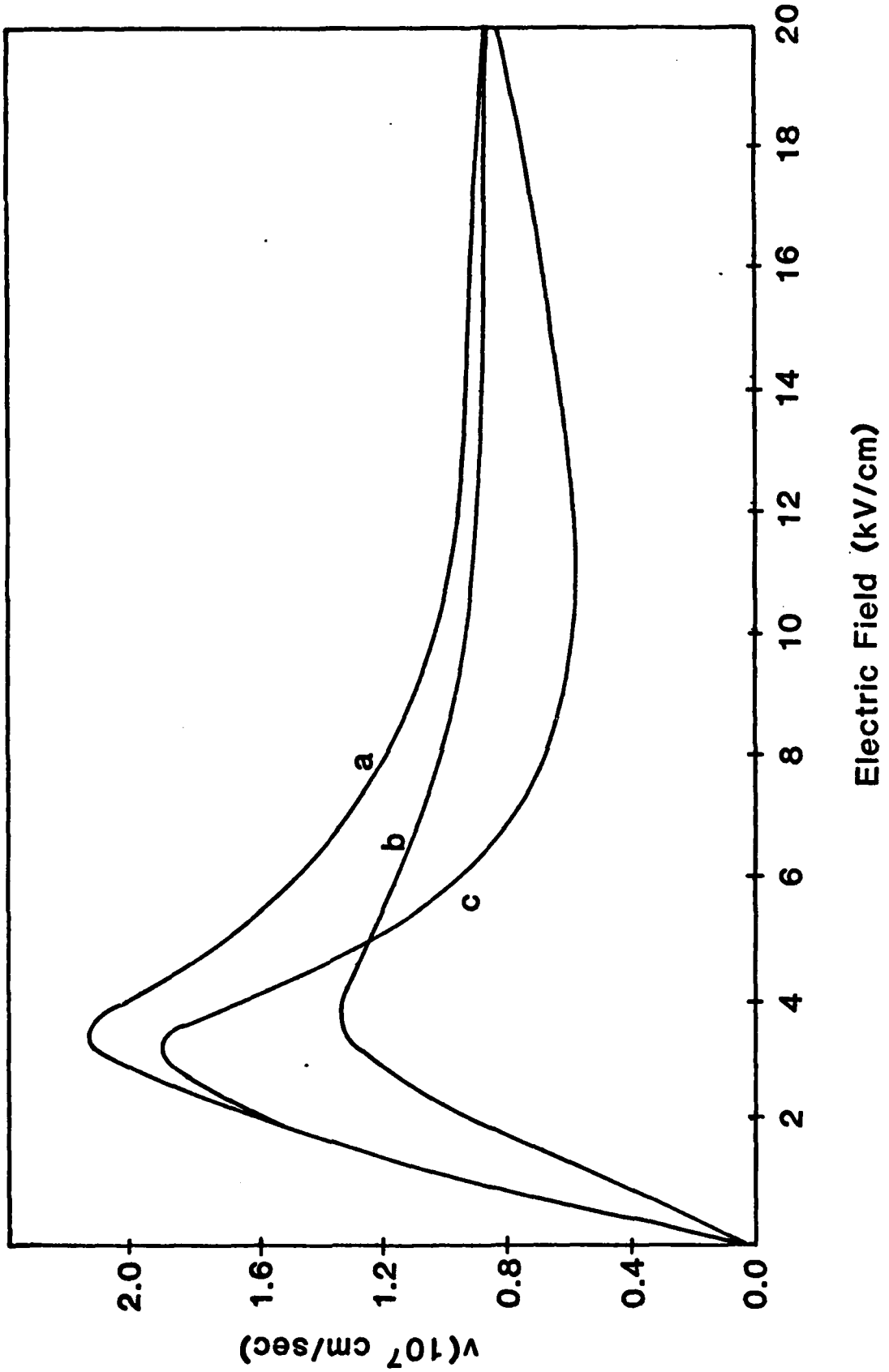


Figure 2.2 Different velocity-field models.

Curve c is given by an empirical equation of the form

$$v = \frac{\mu_o E(1 + B(E/E_o)^4)}{1 + (E/E_o)^4} , \qquad (2.9)$$

with parameters (curve c): $\mu_o = 8000\ cm^2/v \cdot sec$,

$B = .05$, and

$E_o = 4kV/cm$.

This relationship is seen to be close to curve a at low fields, drops below both curve a and curve b at intermediate fields (6 - 20kV/cm) and gives a larger velocity at very high field (> 20 kV/cm).

The relationship expressed by Equation (2.8) has been used in most of the device calculations. With this equation the low-field mobility $\mu_o$ can be made a function of doping density to account for doping effects. Ionized impurity scattering is known to have little effect on the saturated drift velocity so this parameter has not been varied with doping. Figure 2.3 shows the low-field mobility variation used in this work. The solid curve is a plot of the empirical equation

$$\mu_o = \frac{A}{1 + (\frac{\ln N_D}{B})^n} \qquad (2.10)$$

where

$A = 8{,}380\ cm^2/V \cdot sec$,

$n = 23$, and

$B = 23.255$

The points in Figure 2.3 are results calculated by a Monte Carlo transport program. Curves a and b in Figure 2.2 are seen to cover the expected velocity-field relationships of MESFETS with doping densities over the range of $10^{15}/cm^3$ to $10^{17}/cm^3$.

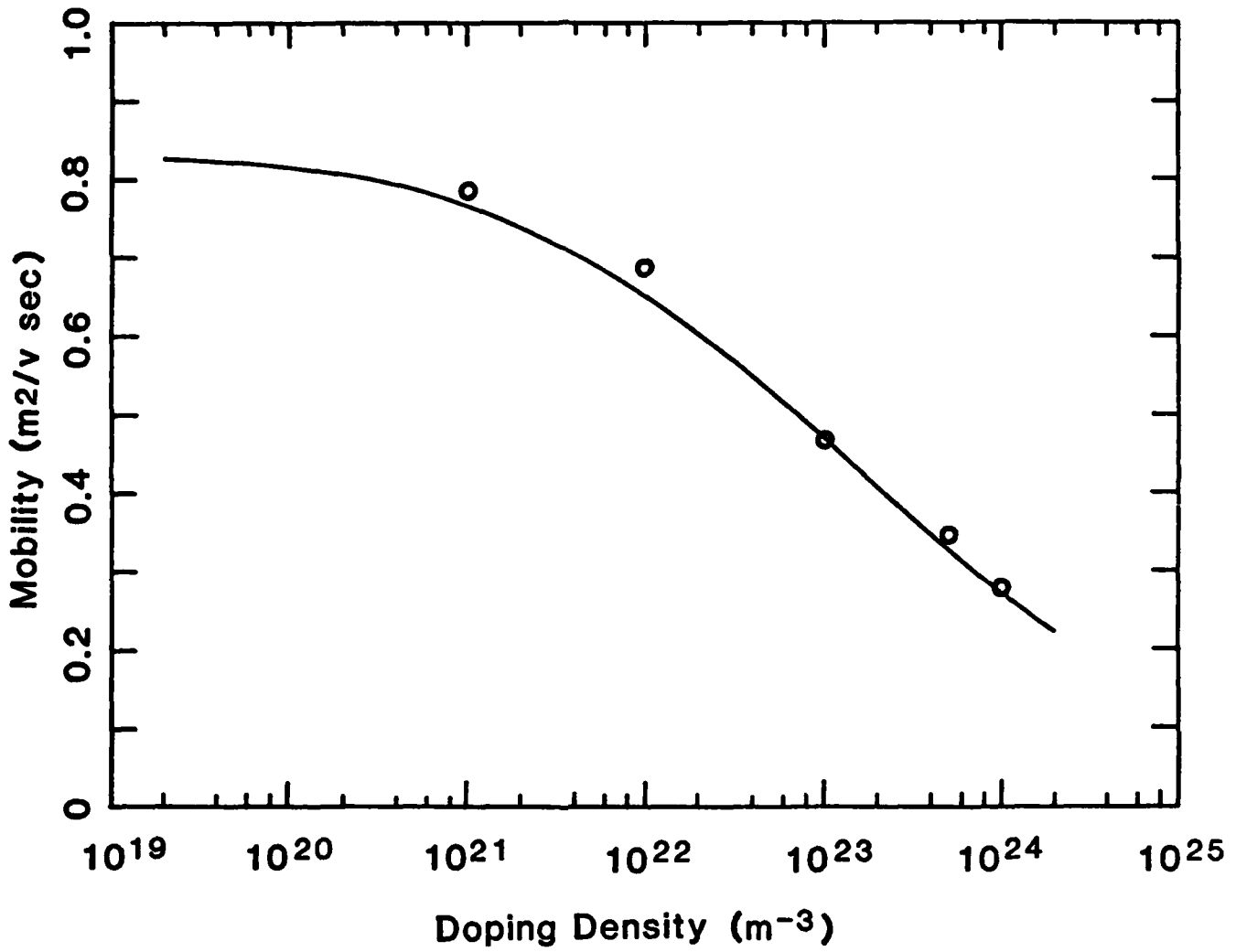


Figure 2.3 Variation of low-field mobility with doping density. Circles are calculated points from Monte Carlo analysis.

## 2.2 Solution Techniques for Equations

In solving Equations (2.1)-(2.5) a numerical technique based on the finite difference method has been used to solve Poisson's equation. The two-dimensional grid structure for the numerical model assumes a device in which the gate is centered midway between the source and the drain contacts. The device is divided into a uniform rectangular mesh of length $\Delta x$ and width $\Delta y$. A typical grid size is 60 x 15 points in the x and y directions respectively so that the resolution is about 0.033 μm along the channel direction and 0.02 μm perpendicular to the channel. These values are less than a Debye length [2] and meet the mesh size criterion in the simulation of uniformly doped devices as recommended by others [3].

By expanding the electrostatic potential function using a Taylor's series expansion about the point (x,y) a series of difference equations results which are of the five- point type. The boundary conditions of this problem are such that the exposed semiconductor surfaces are assumed to be ideal electrical insulators, with no current flowing normal to these surfaces. This implies that all normal gradients at the free surface are zero. The end contacts are approximated by equipotential surfaces with neutral charge. In order to obtain a physical picture for the model, the quantities such as potential $\phi$, electron density n, and impurity donor density $N_d$ are defined at the node points.

With the aid of the boundary conditions as stated above and Poisson's relation in difference form, an equation can be written at each interior point, resulting in a set of I x J linear system of equations in I x J unknowns and its matrix form is written as,

$$[A][\phi] = [C], \qquad (2.11)$$

where

[A] is the banded square matrix of order IxJ,

[$\phi$] is the column matrix of length IxJ, and

[C] is the column matrix of length IxJ.

Matrix [C] is composed of two columns, one of which contains the potential along the boundaries while the other contains the potential due to electronic charge density. I and J are the number of interior points in the x- and y-direction respectively.

The properties of the matrix [A] that results from such a linear system of equations has been studied [4,6] and efficient solution methods are available.

In this work three different techniques have been used to solve the matrix equation:

1. L-U Decomposition

In this technique, the L-U decomposition technique operating on a non-singular square-banded matrix is used from the standard IMSL subroutine package.

2. Cholesky Factorization

This factorization is for a symmetric, positive, definite, banded matrix and was obtained using Linpack subroutines. This technique uses less storage than the previous one.

3. SPARSPAK

The matrix [A] is a sparce matrix and techniques which make use of this sparsity can save storage. The attractive feature of this package is that it effectively reduces the storage requirement and saves computer time [6].

Once the solution of Poisson's equation has been obtained, the x-and y-directed fields can be immediately obtained by applying the difference method

to the potential. The total field is the resultant of the two components. The mobility is then evaluated by relating the instantaneous velocity to the field through the empirical relationships as previously described.

The x- and y-components of current density in the device are calculated through the spatial difference form of the transient solution to the electron transport equation. The continuity equation that relates the current density to the electron density is computed using the difference method for both time and spatial variation.

Initially, charge neutrality is assumed at each point. Poisson's equation is solved for the electric potential, followed by the electric field and the current density in both directions. The electron density is computed from the continuity equation (Equation (2.5)). The updated electron density is then used in Equation (2.4) to update the current density. Equations (2.4) and (2.5) are then iterated until there is a negligible change in $\vec{J}$ or n. This is the period for one time step. The process is repeated for the next time step by returning the updated values of electron density to Poisson's equation and solving again for the next time period. The process is continued until any further change in the variables is negligible and a steady-state solution is achieved.

To solve Equations (2.4) and (2.5), a time increment $\Delta t$ must be selected. The improper choice of this time increment may cause the solution of the equation to diverge. This can be avoided by adjusting $\Delta t$ using the approximate inequality [5] $\Delta\tau < \varepsilon\varepsilon_o/q\mu N_d$. As a final check for the convergence of the equations, and the validity of the above numerical calculation, the current should be approximately constant at every point in the device.

## 2.3 Impurity Profiles

The MESFETs studied have impurity profiles typical of the devices being used at Rockwell on the Ion Implanted Planar GaAs IC Program.* Three slightly different impurity profiles have been modeled. The original data obtained from Rockwell is shown in Figures 2.4, 2.5 and 2.6. These have been replotted in Figure 2.7 using a linear horizontal scale. As can be seen in the figure, the original data based upon C-V measurements does not provide any information about the impurity profile in the region from the surface to a depth of about 0.08 μm. This information is of course needed in the numerical calculations and has been obtained by extrapolating the actual data about the peak in the impurity profile. The data has been assumed to be symmetrical about the implantation peak to obtain the missing data. This may introduce some error into the results but is the best approximation we have based upon the available experimental data.

As can be seen from Figure 2.7 the three impurity profiles are very similar in general features. One profile (referred to as profile I) peaks at slightly less than $10^{17}/cm^3$ while the other two profiles (profile II and III) peak at slightly above $10^{17}/cm^3$. All three profiles have about the same value at 0.3 μm but profile II has a significantly larger value at 0.2 μm than the other two profiles.

## 2.4 General Results

The model discussed in the previous sections has been used to study a variety of GaAs ion implanted MESFET structures. The structures have been selected to be as close as possible to experimental devices being fabricated at Rockwell. Calculations have been made for all three impurity profiles previously discussed.

*Data on the profiles was kindly supplied by Ricardo Zucca.

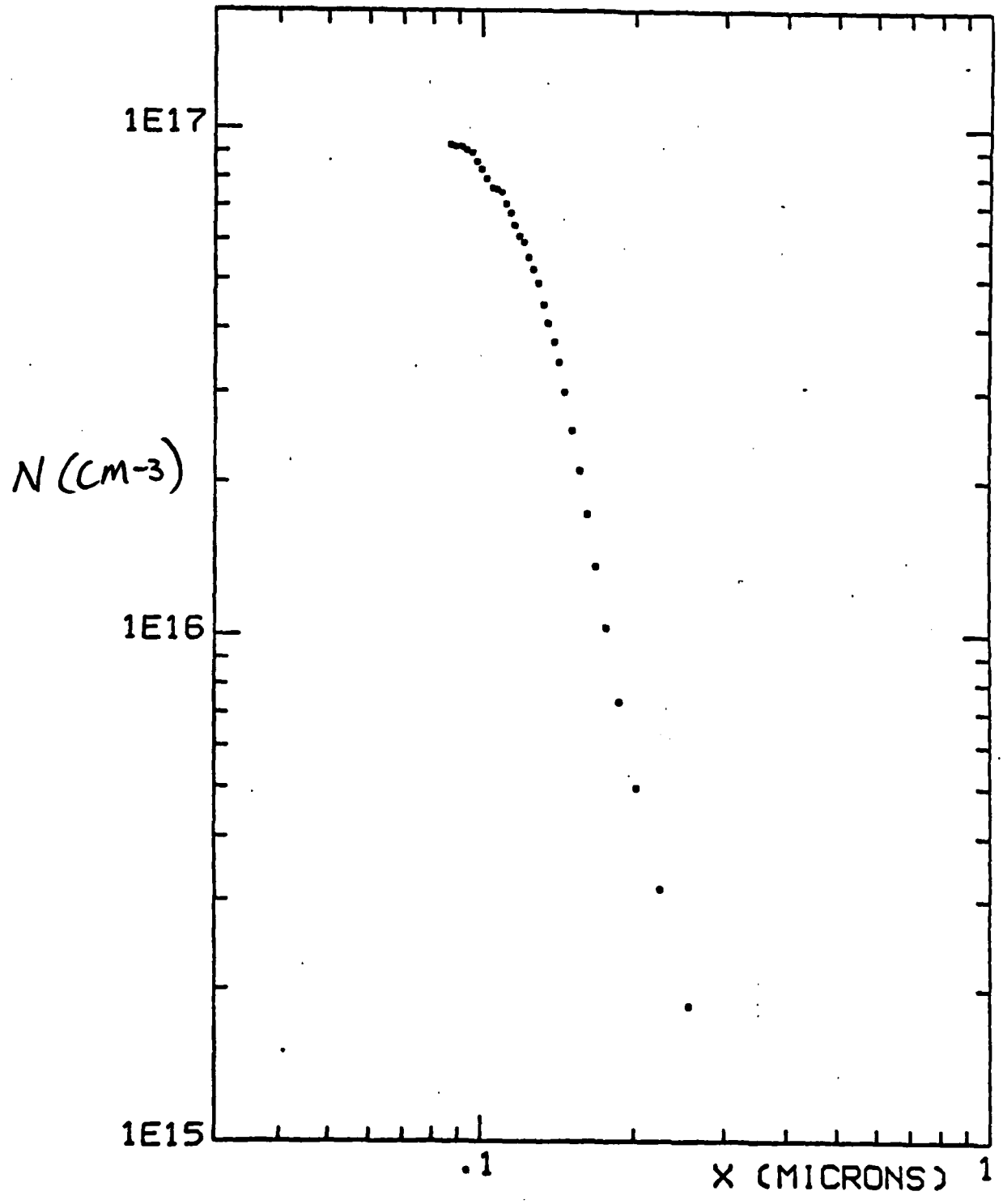


Figure 2.4 Measured doping profile of a type I device. Data provided by Rockwell.

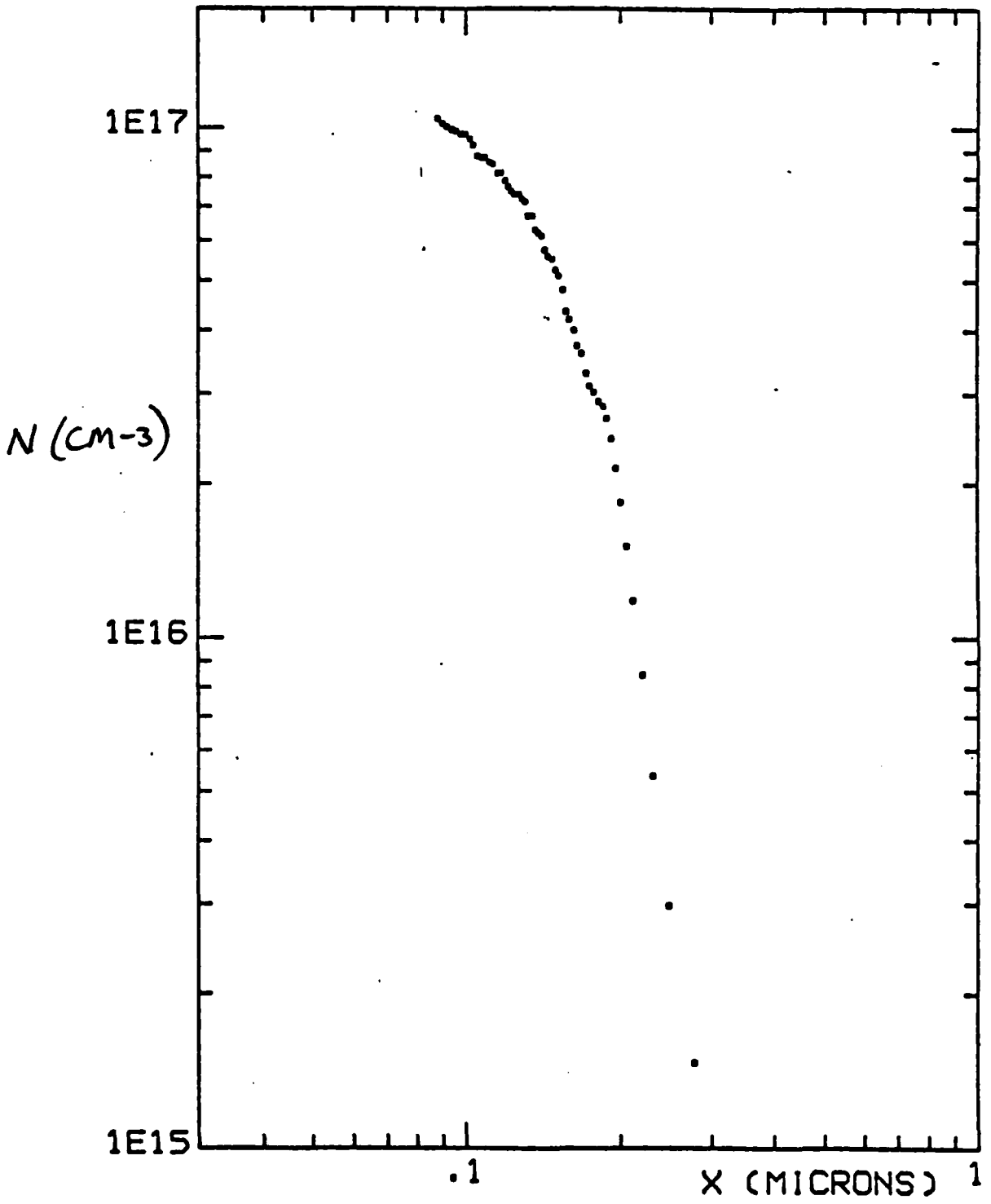


Figure 2.5 Doping profile of a type II device. Data provided by Rockwell.

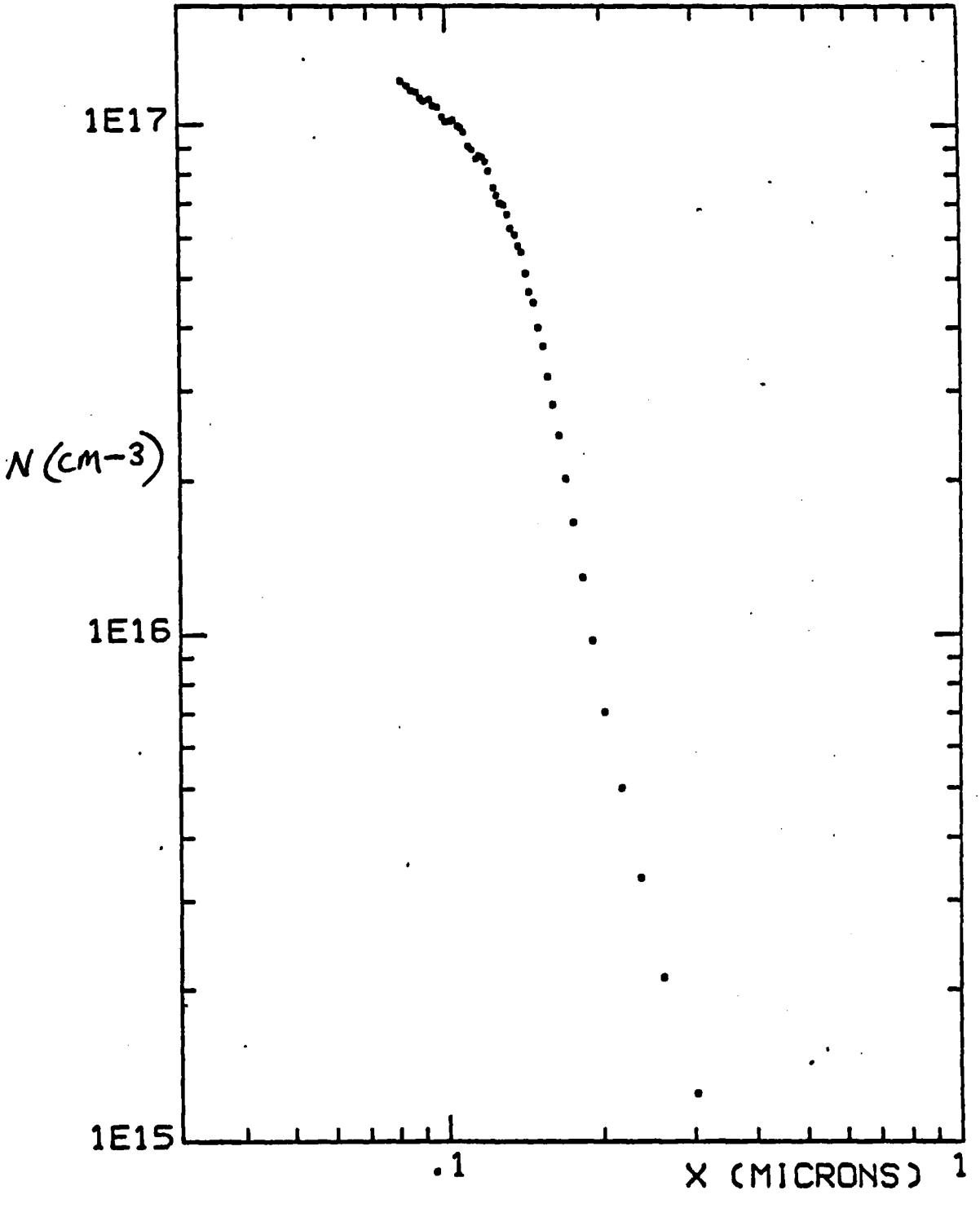


Figure 2.6 Doping profile of a type III device. Rockwell data.

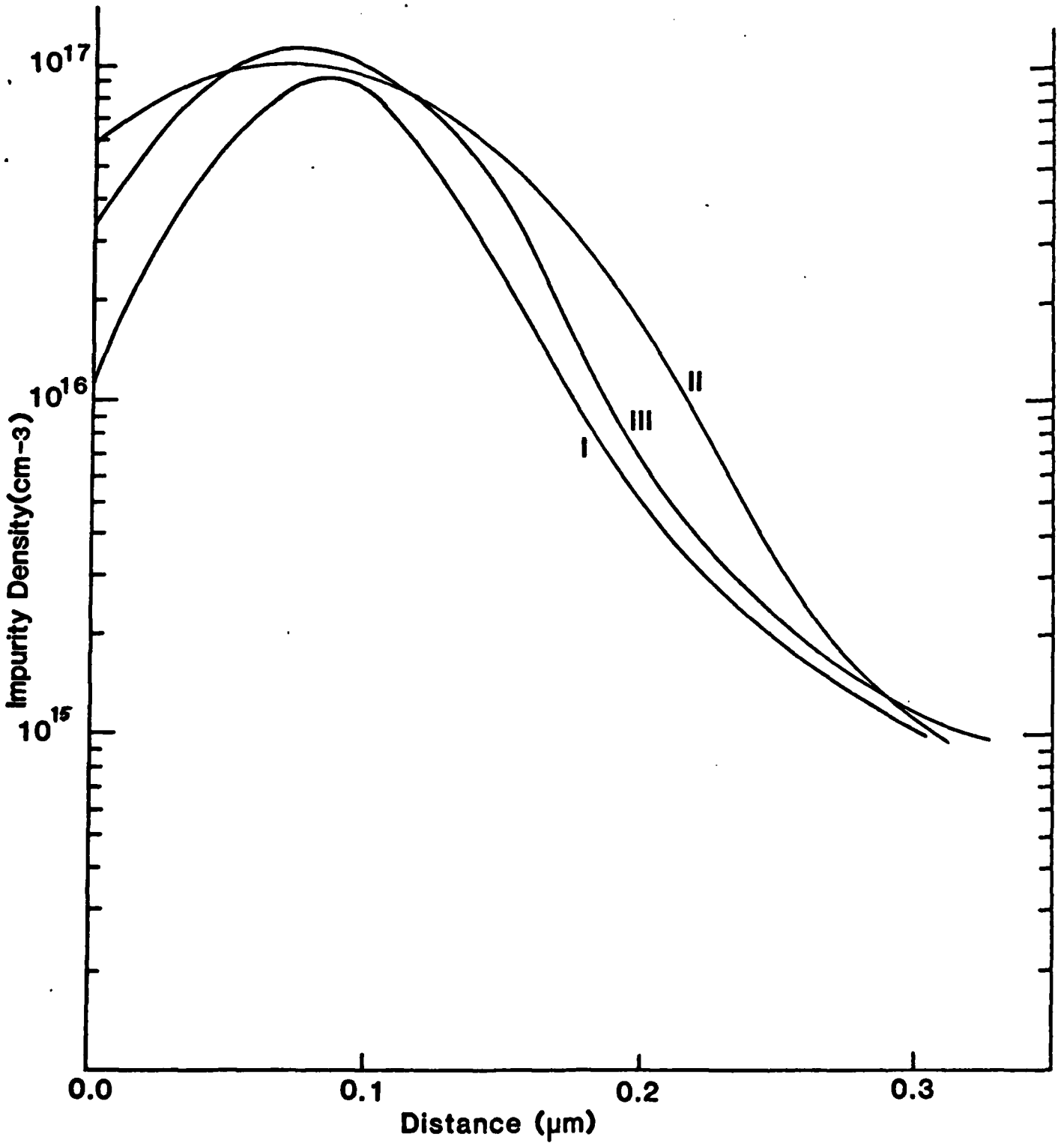


Figure 2.7 Comparison of the three different doping profiles.

The general approach to the numerical calculations can be summarized as follows. First a particular geometrical configuration is selected specifying device dimensions such as gate-to-source, gate-to-drain, etc. spacings. The doping profile and velocity-field model to be used is specified. For a selected set of bias voltages on the gate and drain the transient numerical solution is obtained to the device equations. The solution is allowed to develop in time until a steady state is reached. At this point the internal device parameters such as carrier densities, current densities and potential are known throughout the device as well as knowing the terminal currents. These results are then plotted if desired. The process is then repeated for any desired gate and drain voltages to model device operation under a set of operating conditions.

Results have typically been made using either a 40 x 25 grid of points or a 60 x 15 grid. No significant differences have been observed with these grid sizes or with other reasonable variations in grid size. Typical device dimensions have been a gate length of 1 μm and source-to-gate and gate-to-drain spacings of 0.5 μm. The gate width has been taken as 50 μm. Since the device has an implanted channel there is no unique depth into the device at which point to terminate the calculations. Typically the calculations have modeled the device to a depth of about 0.3 μm at which point the implanted profile is around $10^{15}/cm^3$ or about two orders of magnitude below the peak doping density. Unless otherwise stated, all the results reported here are for the conditions discussed above.

Typical results for the internal electron concentration are shown in Figures 2.8-2.11 for a device (profile I) with a drain voltage of 2.5 volts and gate voltages of +0.5, +0.25, 0 and -0.5 volts, respectively. In each figure the source is on the left side, the drain on the right side and the

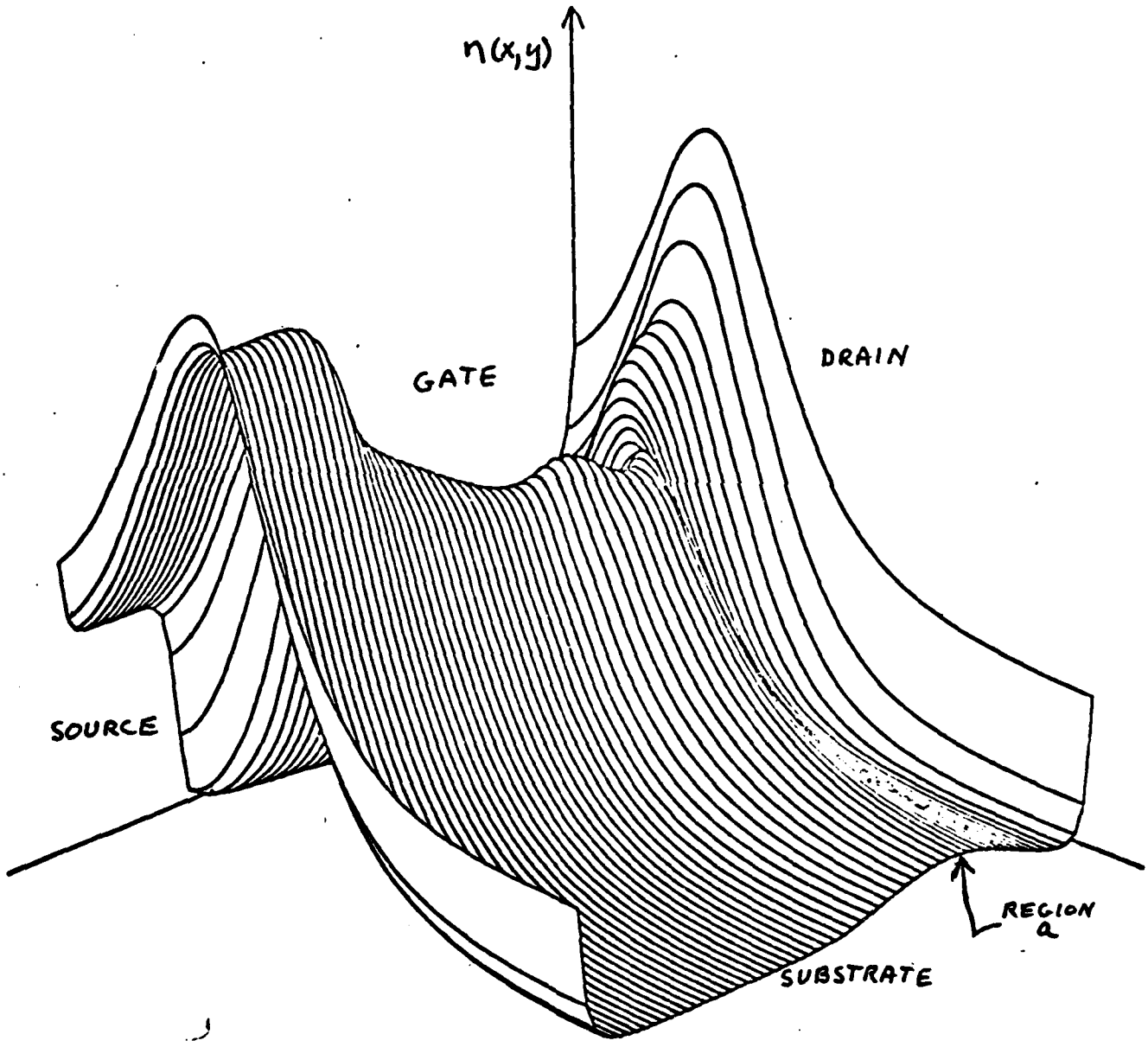


Figure 2.8 Internal electron density for a type I device at $V_{ds}$=2.5V and $V_{gs}$ = 0.5V.

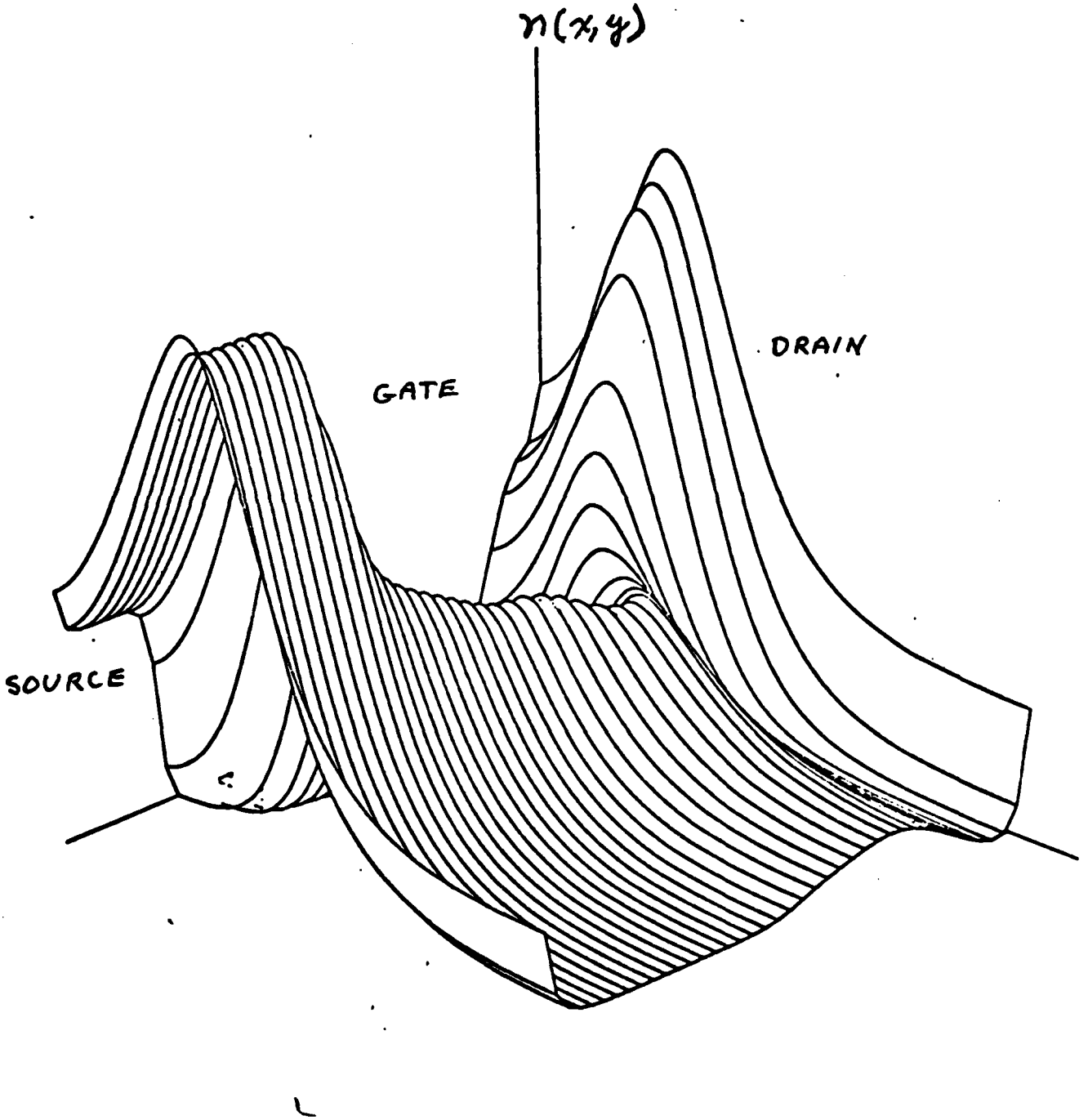


Figure 2.9 Internal electron density for a type I device at $V_{ds}$ = 2.5V and $V_{gs}$ = 0.25V.

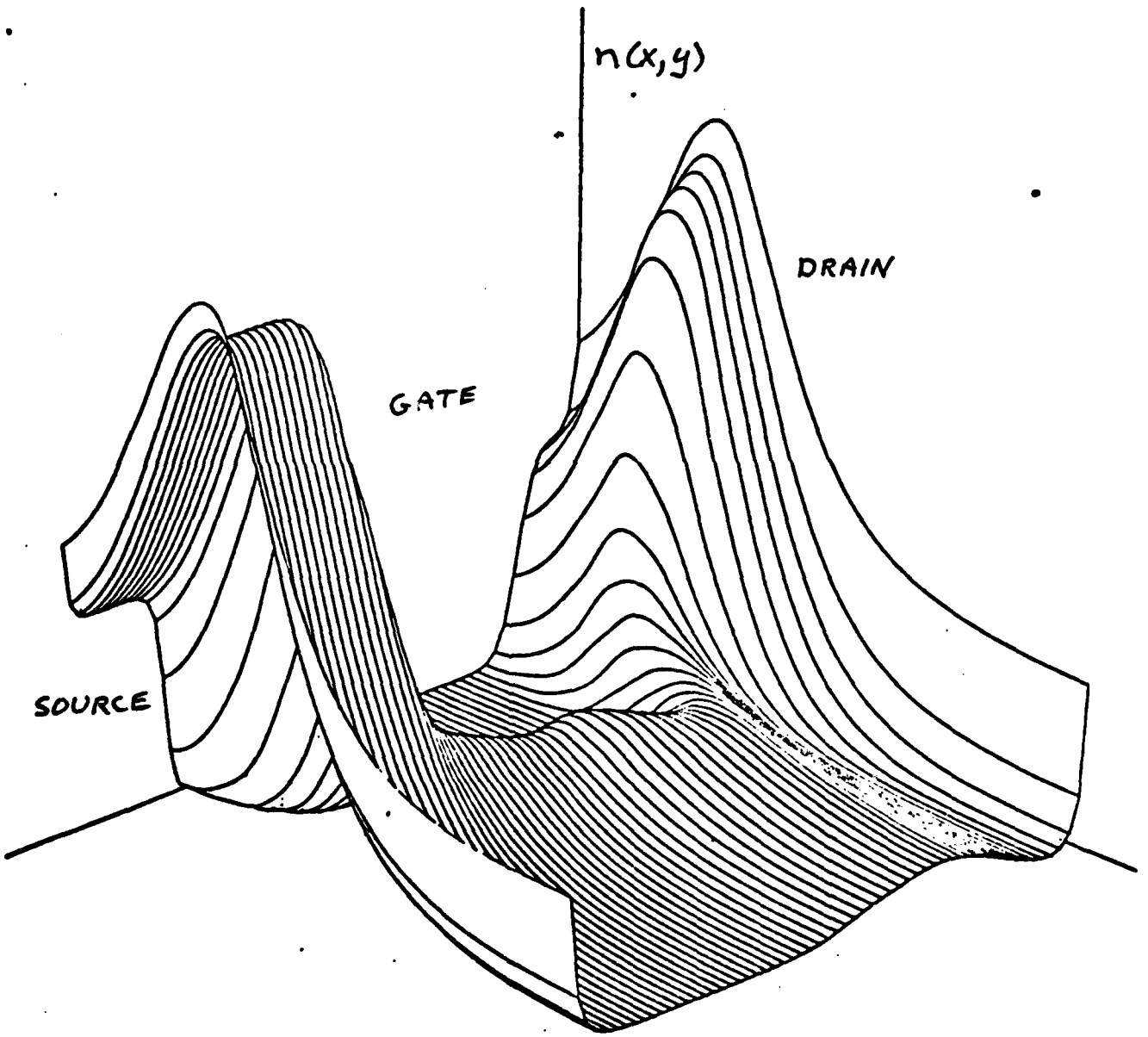


Figure 2.10 Internal electron density for a type I device at $V_{ds}$ = 2.5V and $V_{gs}$ = 0V.

gate along the rear of the view presented. Near the source and drain contacts the electron profile follows closely the impurity profile and has a Gaussian like shape. Various degrees of channel depletion can be seen in the figures with Figure 2.11 at a reverse bias of -0.5 volts showing almost complete depletion of the channel.

An interesting feature of the calculations appears in region a of Figure 2.8. This is deep within the device almost directly under the drain end of the gate region. This is also the high-field region of the channel. The calculations indicate a carrier enhancement region which extends deep within the device. Although the carrier density within this region is still small compared with the peak in the profile, the density in this high-field region has increased about an order of magnitude over the background doping density of about $10^{15}/cm^3$. This carrier enhancement is seen in all the profiles except that of Figure 2.11 where the depletion region extends completely throughout the channel.

It should be noted that no dipole layer is observed in these calculations as have been reported by some investigators for uniformly doped channel devices. Whether this is due to the implanted profile or to the small device dimensions is not known at the present time. However, no dipole layers or negative resistance effects have been observed in any of the calculations.

A comparison of the internal carrier densities for the three doping profiles under similar bias conditions is shown in Figures 2.1-2.14. Profile I (shown in Figure 2.12), which has the lowest value of doping density, has the deepest depletion layer as expected, with profile II as shown in Figure 2.14 showing the largest undepleted channel. It is also seen in Figure 2.12 that the depletion region between the drain and gate extends almost to the drain contact. The other profiles show a short undepleted region near the drain

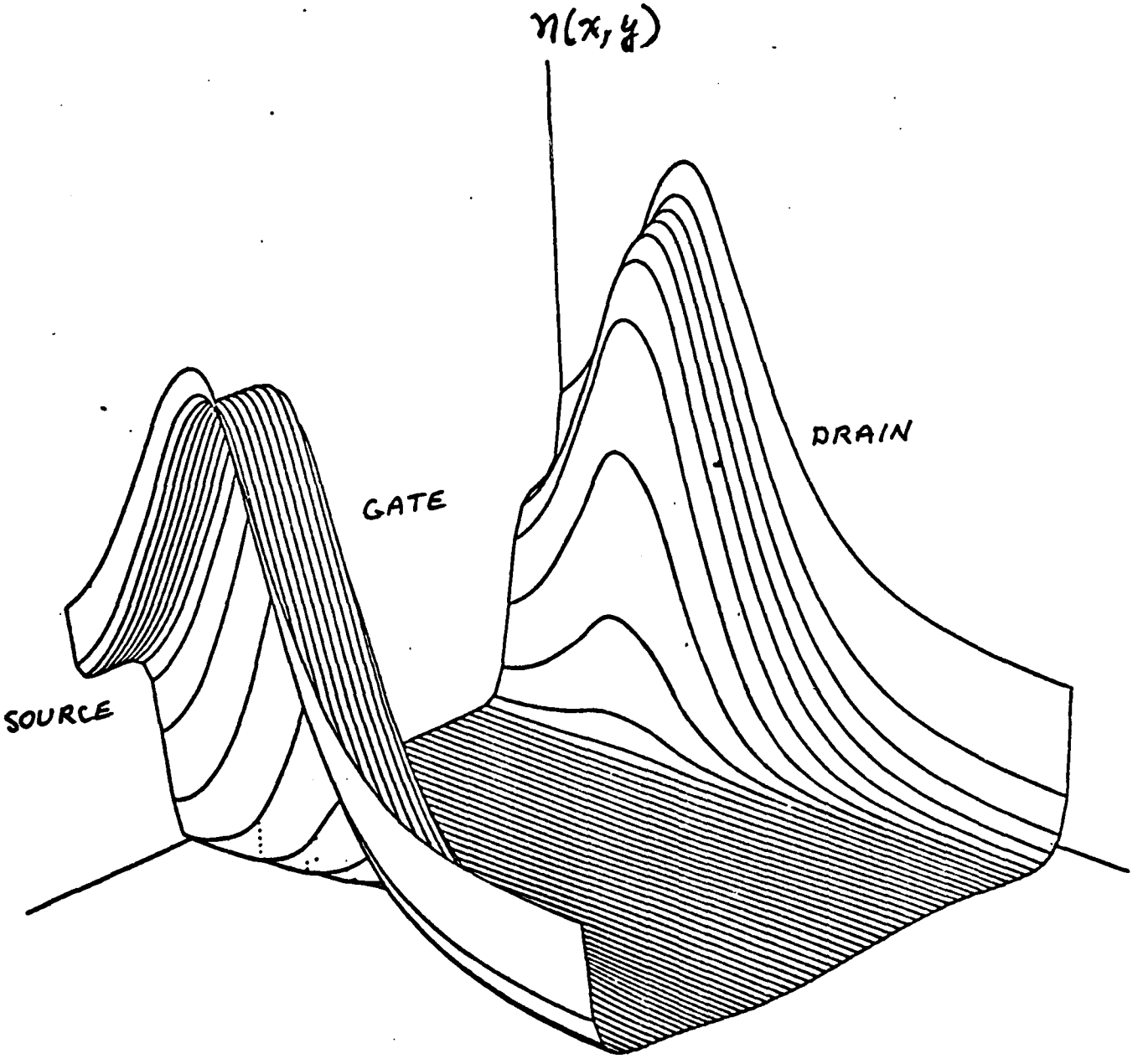


Figure 2.11 Internal electron density for a type I device at $V_{ds}$ = 2.5V and $V_{gs}$ = -0.5V.

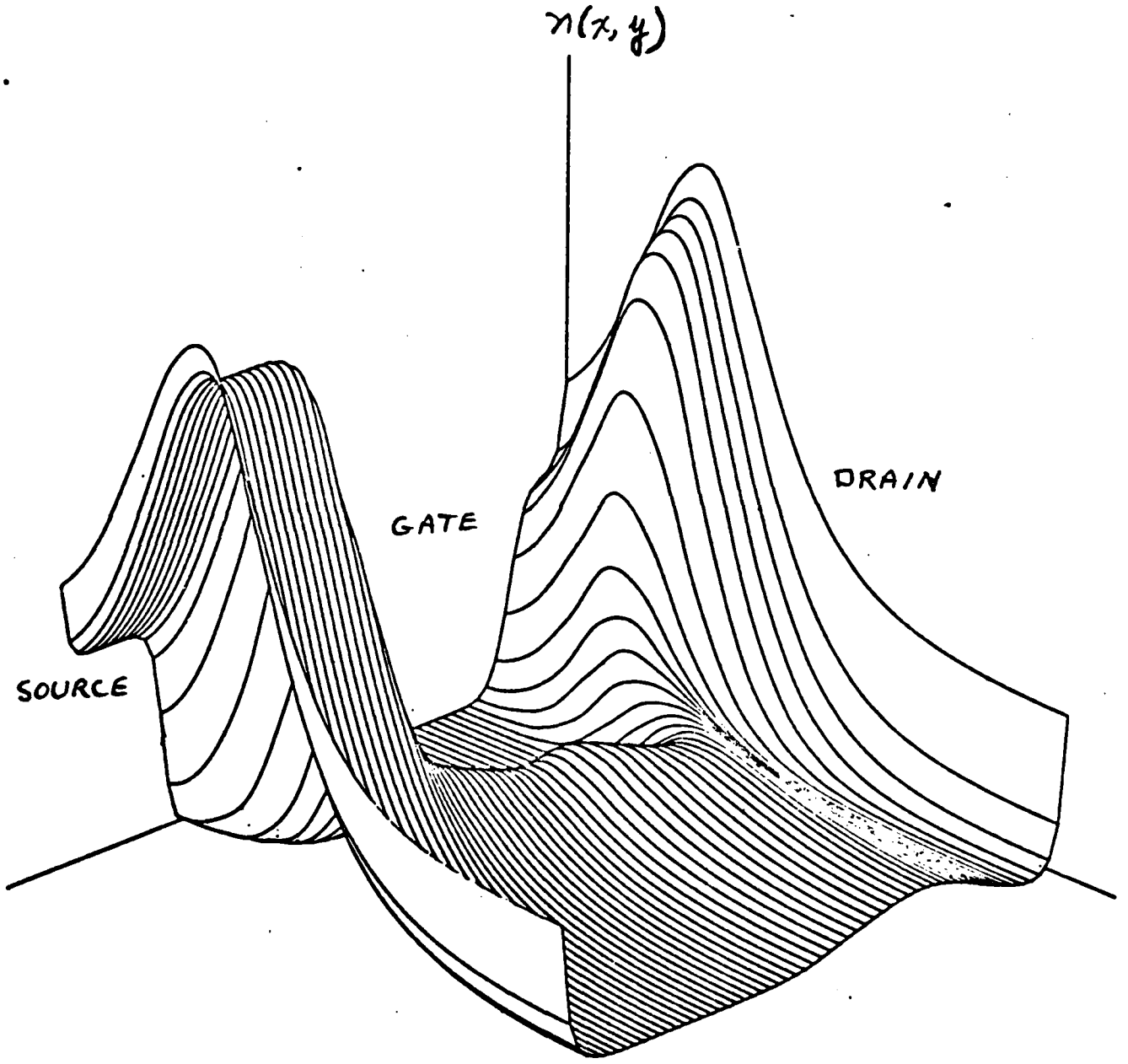


Figure 2.12 Internal electron density for a type I device at $V_{ds}$ = 2.5V and $V_{gs}$ = 0V.

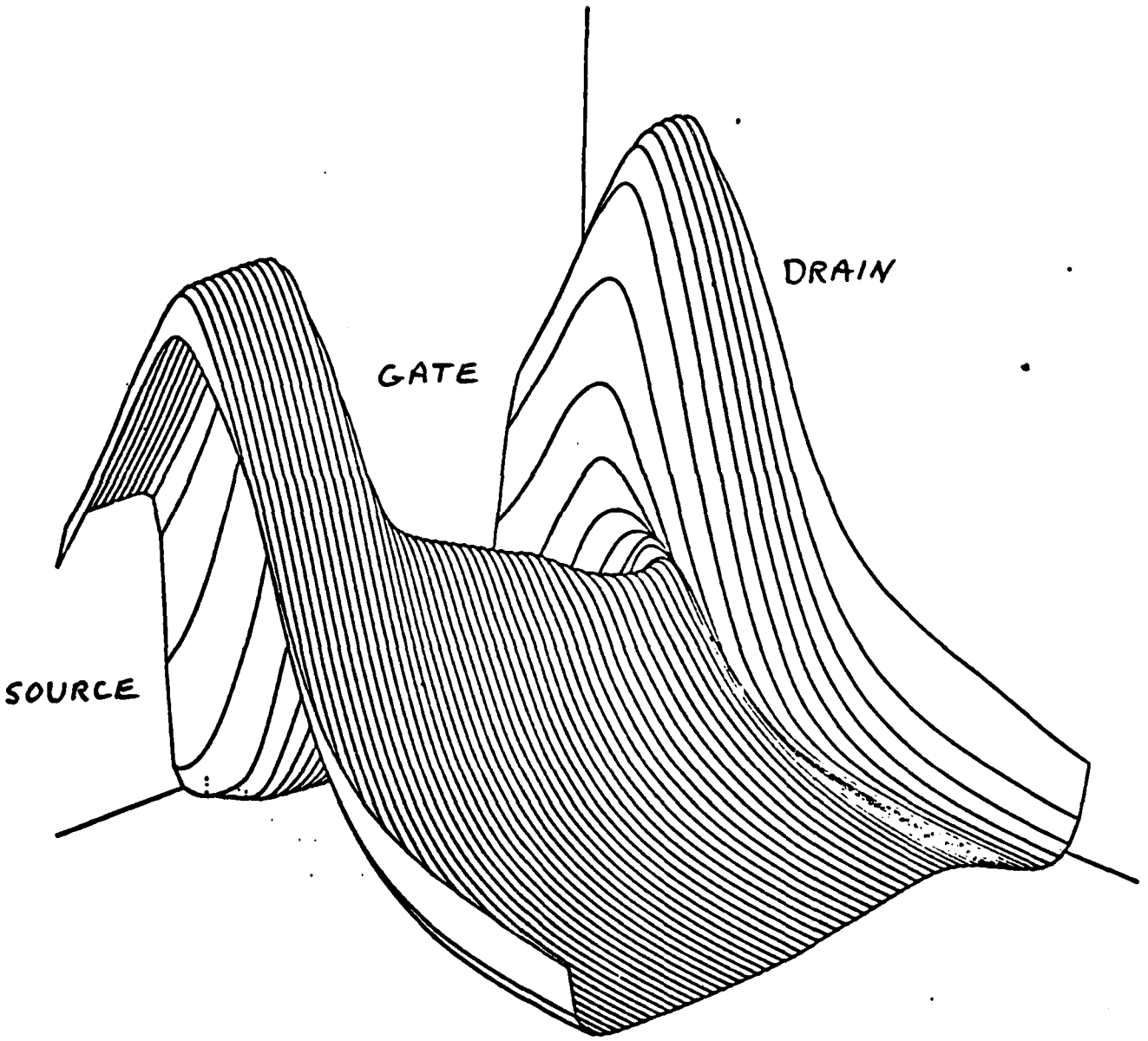


Figure 2.13 Internal electron density for a type III device at $V_{ds}$ = 2.5V and $V_{gs}$ = 0V.

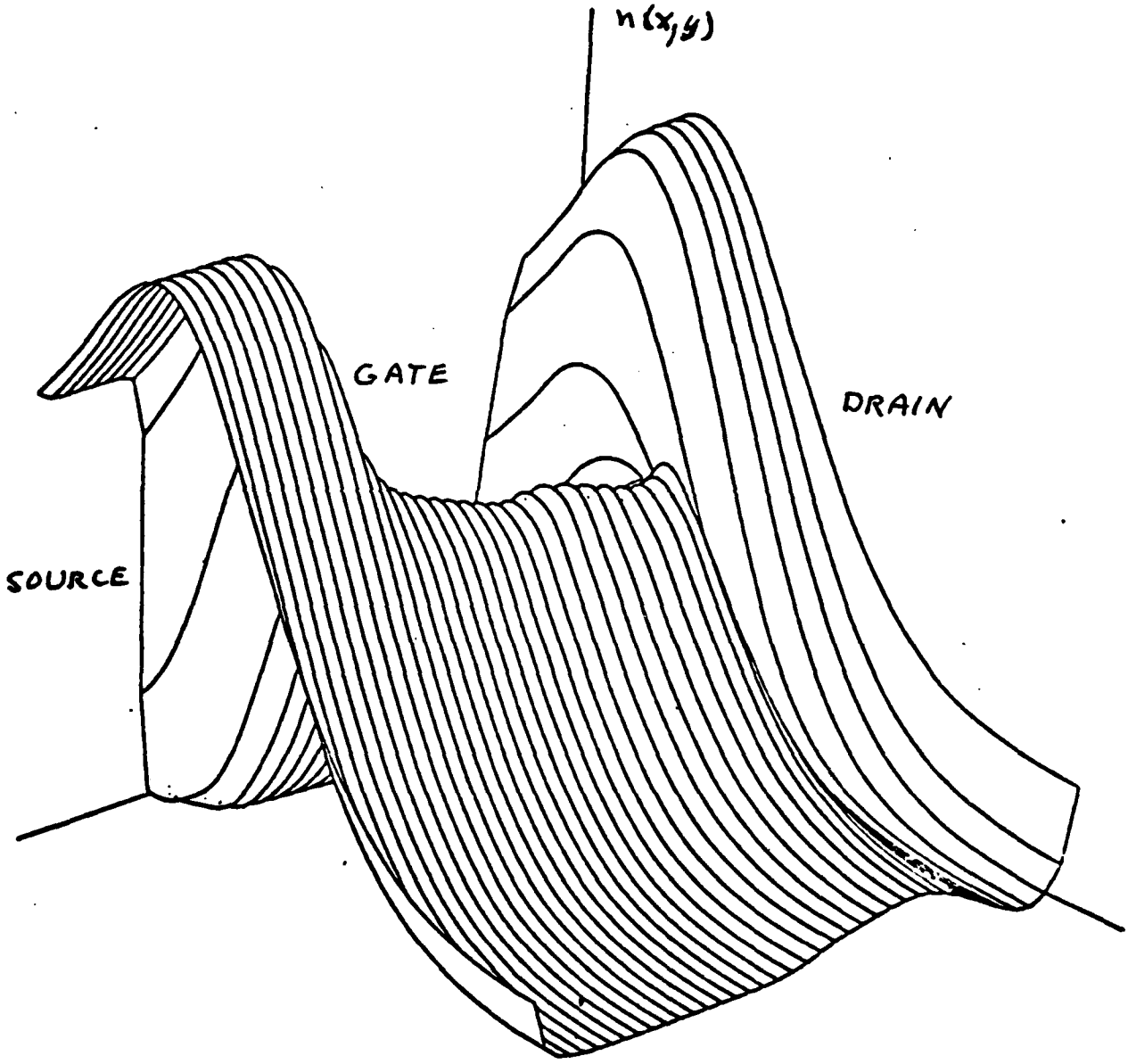


Figure 2.14 Internal electron density for a type II device at $V_{ds}$ = 2.5V and $V_{gs}$ = 0V.

contacts. These calculations illustrate that the zero bias condition is very sensitive to the doping profile and small changes in peak doping density can result in large changes in the active channel charge density, which subsequently show up as variations in current density.

A typical $I_{ds}$ vs $V_{ds}$ characteristic is shown in Figure 2.15 for a type I profile. The calculated characteristic shows good current saturation with a low pinch-off voltage. As mentioned previously there is no evidence of any negative resistance effects in any of the calculated curves.

A typical plot of the magnitude of the electric field as a function of position is shown in Figure 2.16. In this case the gate is to the front of the view instead of the back as in previous figures. The electric field is essentially what would be expected with the field peaking sharply near the drain end of the gate. The peak field is in the range of 3809 kv/m.

A plot of the x-component of current density, $J_x(x,y)$, within the device is shown in Figure 2.17. The general shape of the current-density is as expected but the curve shows some interesting second-order effects as the carriers move from source to drain. Near the source, the current-density profile follows closely that of the implanted channel. Moving under the source end of the gate region, the current-density must peak deeper into the device because of the depletion effect under the gate. Also the width of the conductive channel decreases so the peak value of the current-density profile must increase as seen by the large values of current-density under the gate at the source end of the device. Moving further along under the gate, the current-density profile is seen to broaden and reduce in peak value. This is related to the deeper penetration of the electrons into the device as discussed in connection with Figure 2.8. As the carriers heat up in the large field, the carrier-density profile and the current-density profile both broaden.

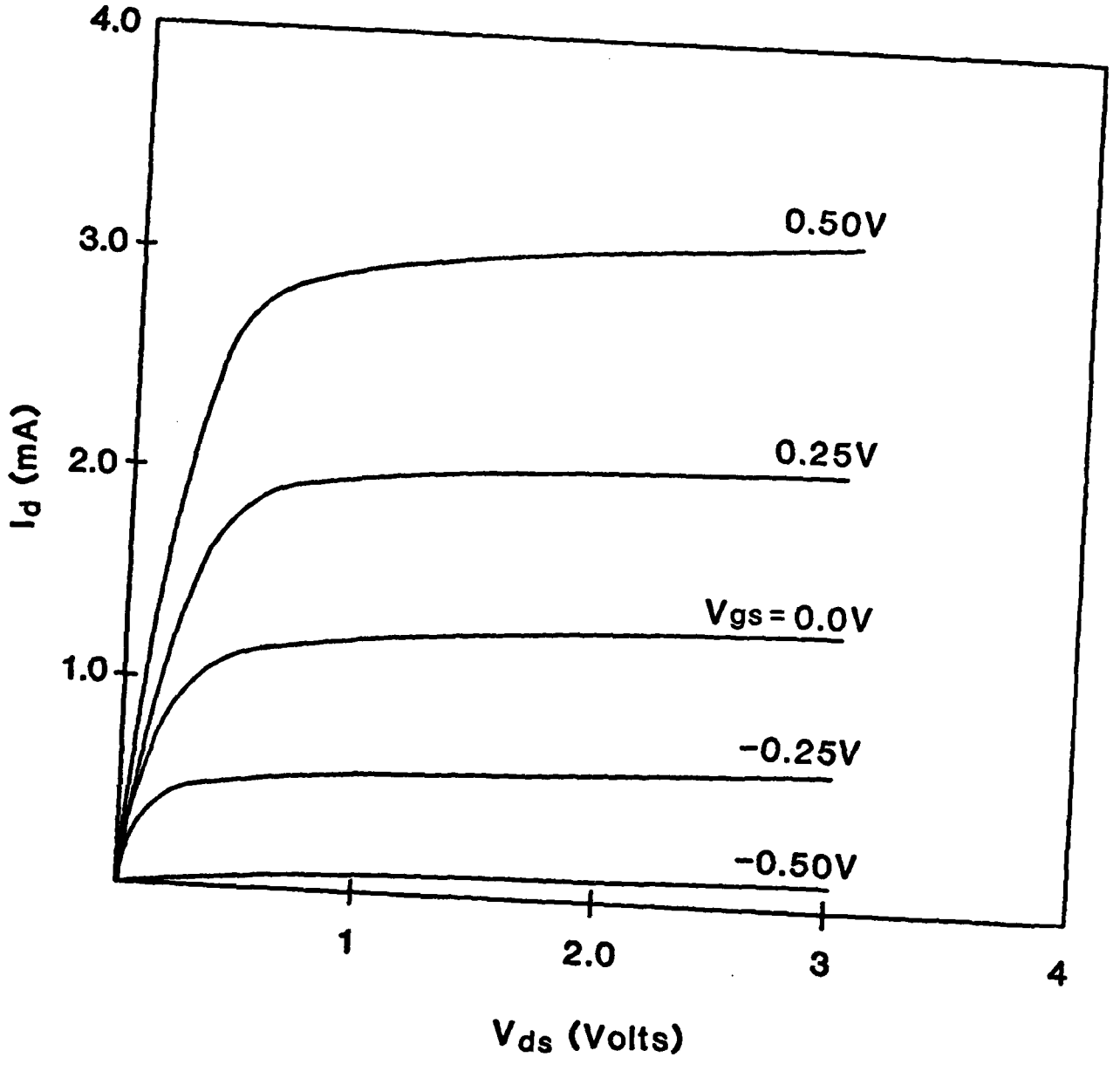


Figure 2.15 Typical calculated $I_d$ - $V_{ds}$ characteristics. (Type I device).

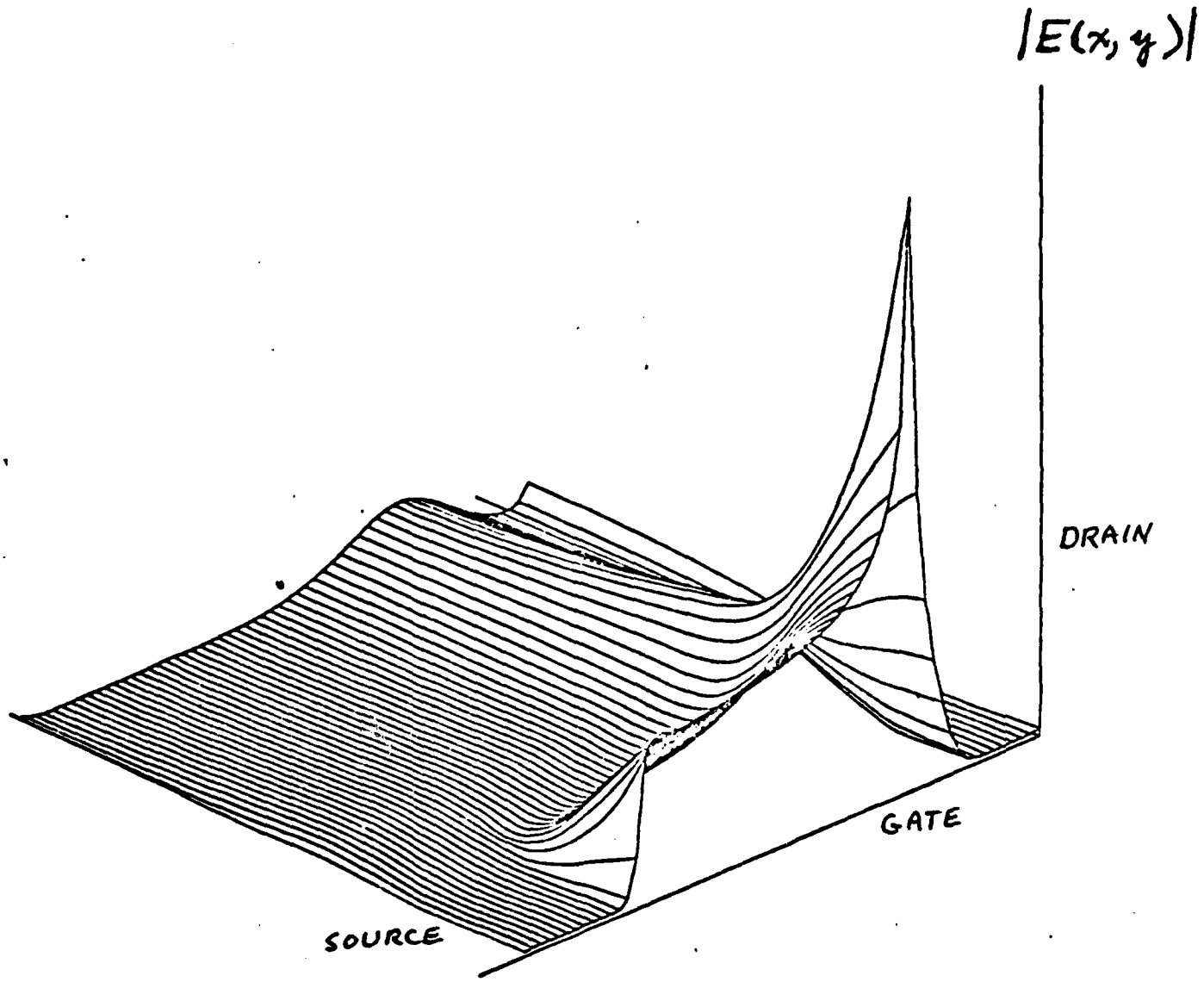


Figure 2.16 Internal electric field magnitude for a type I device at $V_{ds}$ = 2.5V and $V_{gs}$ = 0V.

Finally, near the drain contact the current-density profile again becomes similar in shape to the doping profile. The total current, which is the integral of each of the profile curves in Figure 2.17, is constant at each point along the device. This was verified for each calculation which was performed.

Three final views of internal variables are shown in Figure 2.18-2.20. Figure 2.18 shows a vector plot of the two-dimensional current-density within the device. At each grid point the direction of the arrow is the actual direction of the current density while the length of the vector is proportional to the magnitude of the current density. On this figure one can follow the major paths of the carriers between the source and drain.

Figures 2.19 and 2.20 show contour plots of the potential and carrier densities for a typical device with zero applied gate voltage and 2.5 volts on the drain. The values on the curves in Figure 2.20 are values of $\log_{10}(n)$. Figure 2.20 also illustrates the enhanced electron density under the gate at the drain end of the channel. These figures can be used in combination with previous figures to obtain a clearer picture of the internal MESFET operation.

## 2.5 Effects of Different Velocity-Field Models

The effects of using different velocity-field relationships on calculated device properties has been investigated. The saturated drain current vs gate voltage provides a convenient measure of the influence of different expressions on the overall I-V characteristics. Figure 2.21 shows the results of calculations of drain current at a drain voltage of 2.5 volts using four different velocity-field expressions. The equations and parameters used are summarized below:

a. Equation 2.8 with $\mu_o$ varied according to Figure 2.3
b. Equation 2.8 with $\mu_o = 4500\ cm^2/V \cdot sec$
c. Equation 2.8 with $\mu_o = 8000\ cm^2/V \cdot sec$
d. Equation 2.9 with the same parameters as used for Figure 2.2

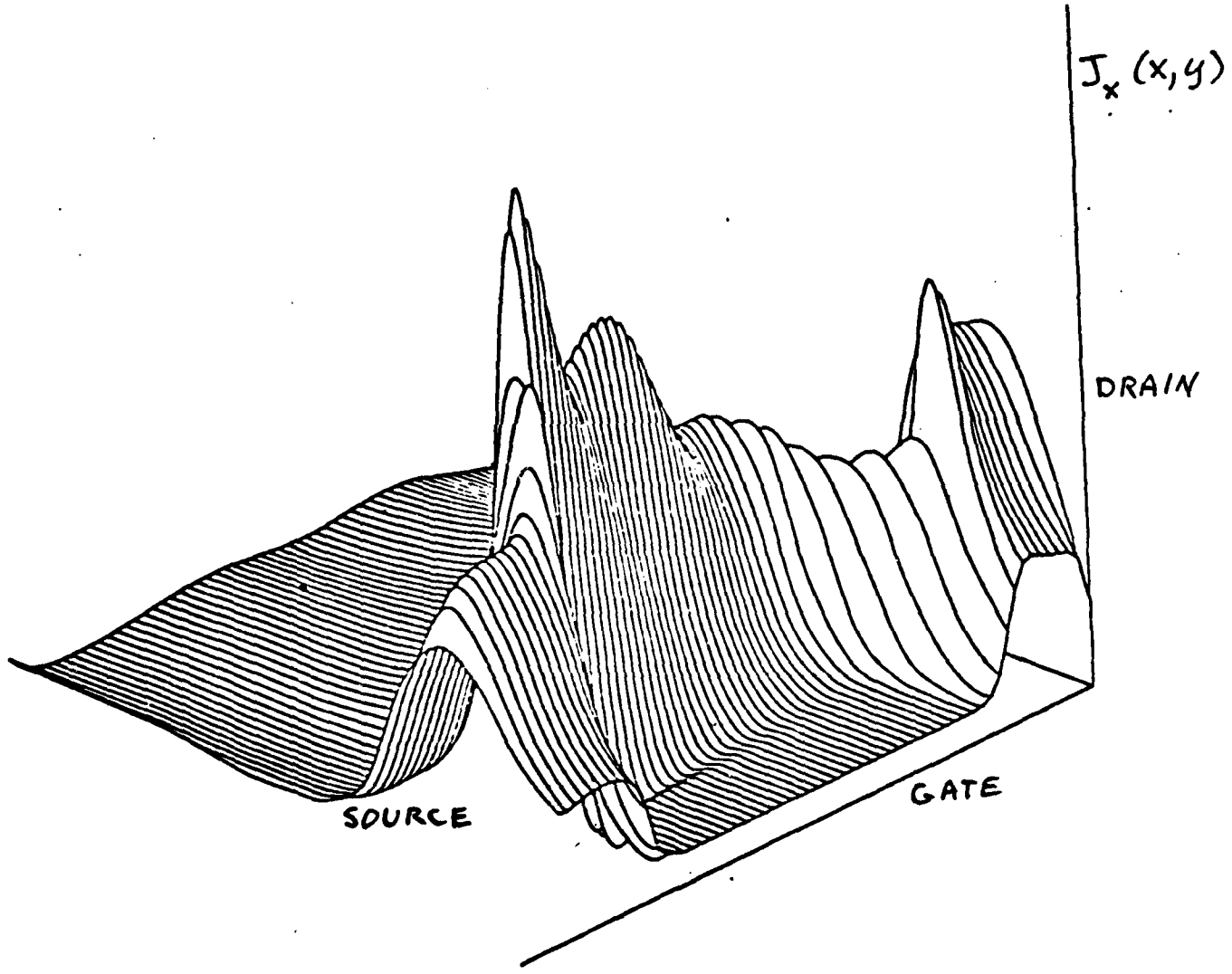


Figure 2.17 Typical $J_x$ current density profile for a type I device at $V_{ds}$ = 2.5V and $V_{gs}$ = 0V.

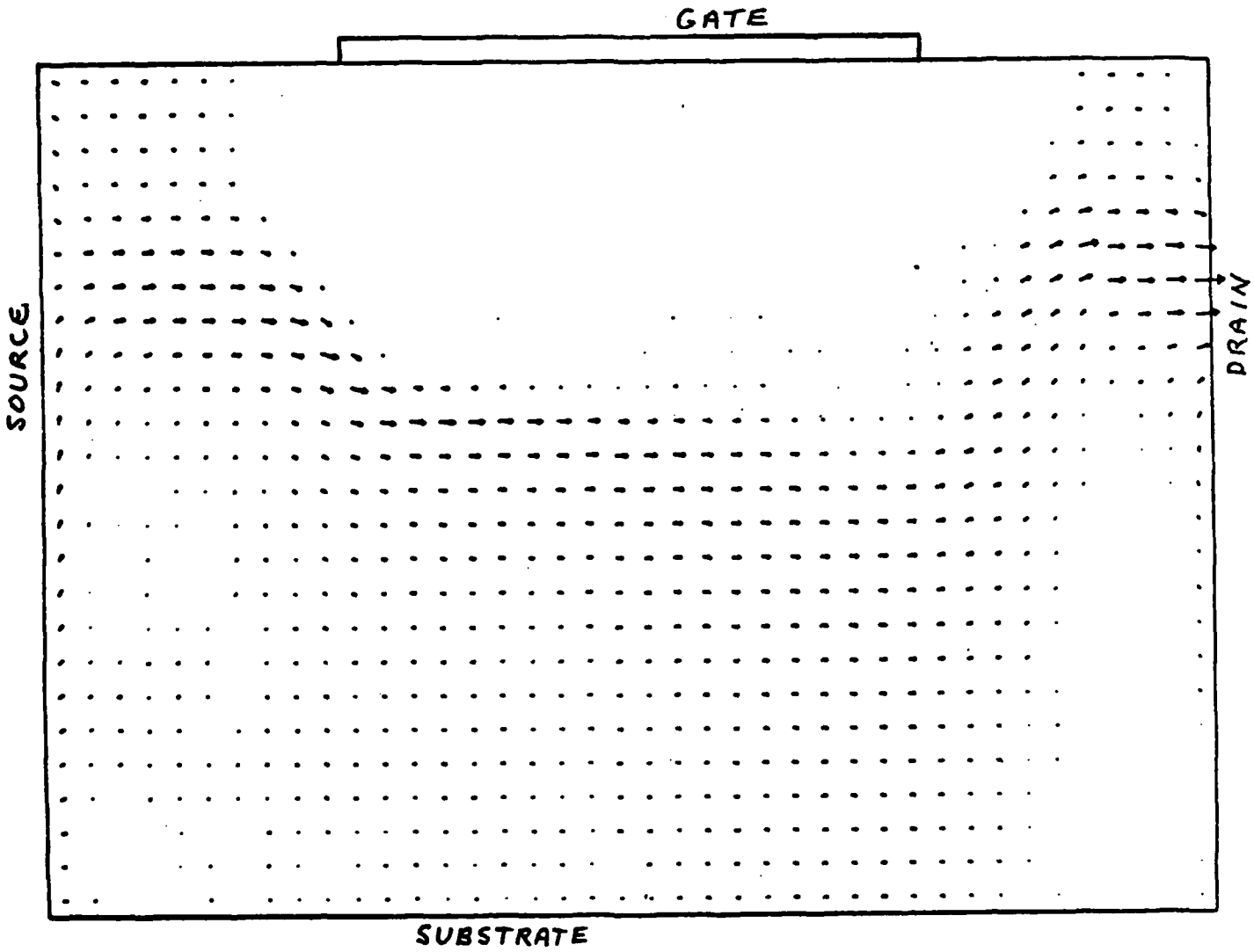


Figure 2.18 Vector plot of internal current density for a type I device at $V_{ds}$ = 2.5V and $V_{gs}$ = 0V.

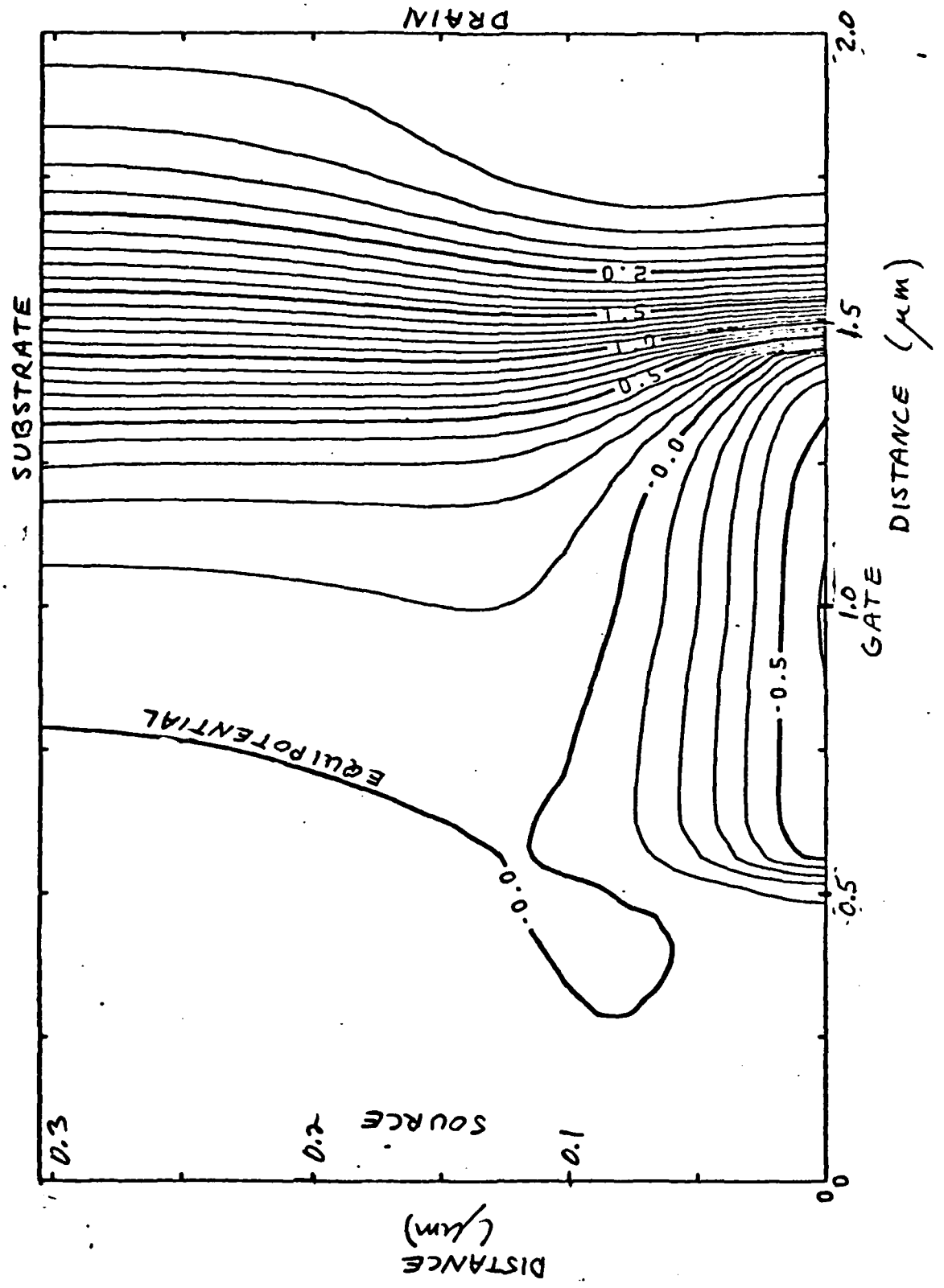


Figure 2.19 Typical equipotential contours for a type I device at $V_{ds}$ = 2.5V and $V_{gs}$ = 0V.

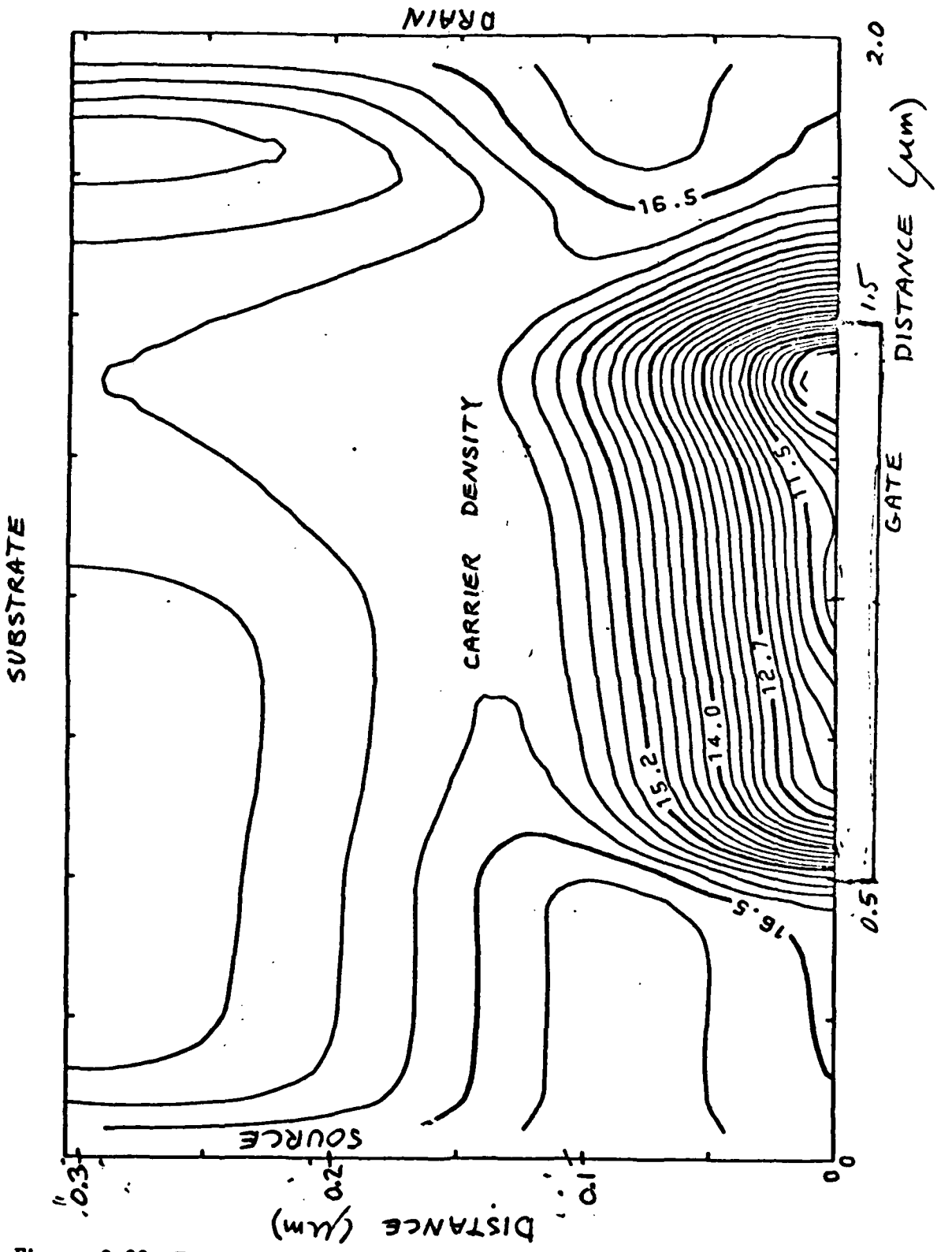


Figure 2.20 Typical carrier density profiles for a type I device at $V_{ds}$ = 2.5V and $V_{gs}$ = 0V. $n=10^K$ where K represents the numbers shown on the curves.

Several general conclusions can be drawn from the results in Figure 2.21. First, all of the calculations predict approximately the same values of current. The largest current (curve c) as expected is obtained from using Equation (2.8) with a low-field mobility of 8000 $cm^2/V \cdot sec$. Second, one can observe that the current is definitely not proportional to low-field mobility and that changes in low-field mobility have a much smaller effect than would be expected from first-order device models. The velocity in the 4-20kV/cm field range appears to be important since curve d has the lowest velocity in this region and also predicts the lowest value of current density.

Also shown in Figure 2.21 are experimental points for a typical MESFET with the doping profile used in the calculations. It is seen that there is reasonable agreement in the magnitude of the current between the theoretical calculations and the experimental results. There is one disturbing difference, however, between the calculated results and the experimental results. This is the observation that the theoretical calculations do not pinch-off as rapidly as the experimental data indicates. This general trend has been observed in calculations for all three doping profiles and the use of different velocity-field models above does not appear to give better agreement as Figure 2.21 indicates.

One can postulate several possible physical mechanisms which might be responsible for the discrepancy seen in Figure 2.21 between theory and experiment. Basically one needs a mechanism which causes the current to be lower than that predicted when the channel nears the pinch-off condition. Several possible explanations are:

1. The carrier saturation velocity may be doping dependent.
2. The doping profile may drop more abruptly than the C-V data indicates.

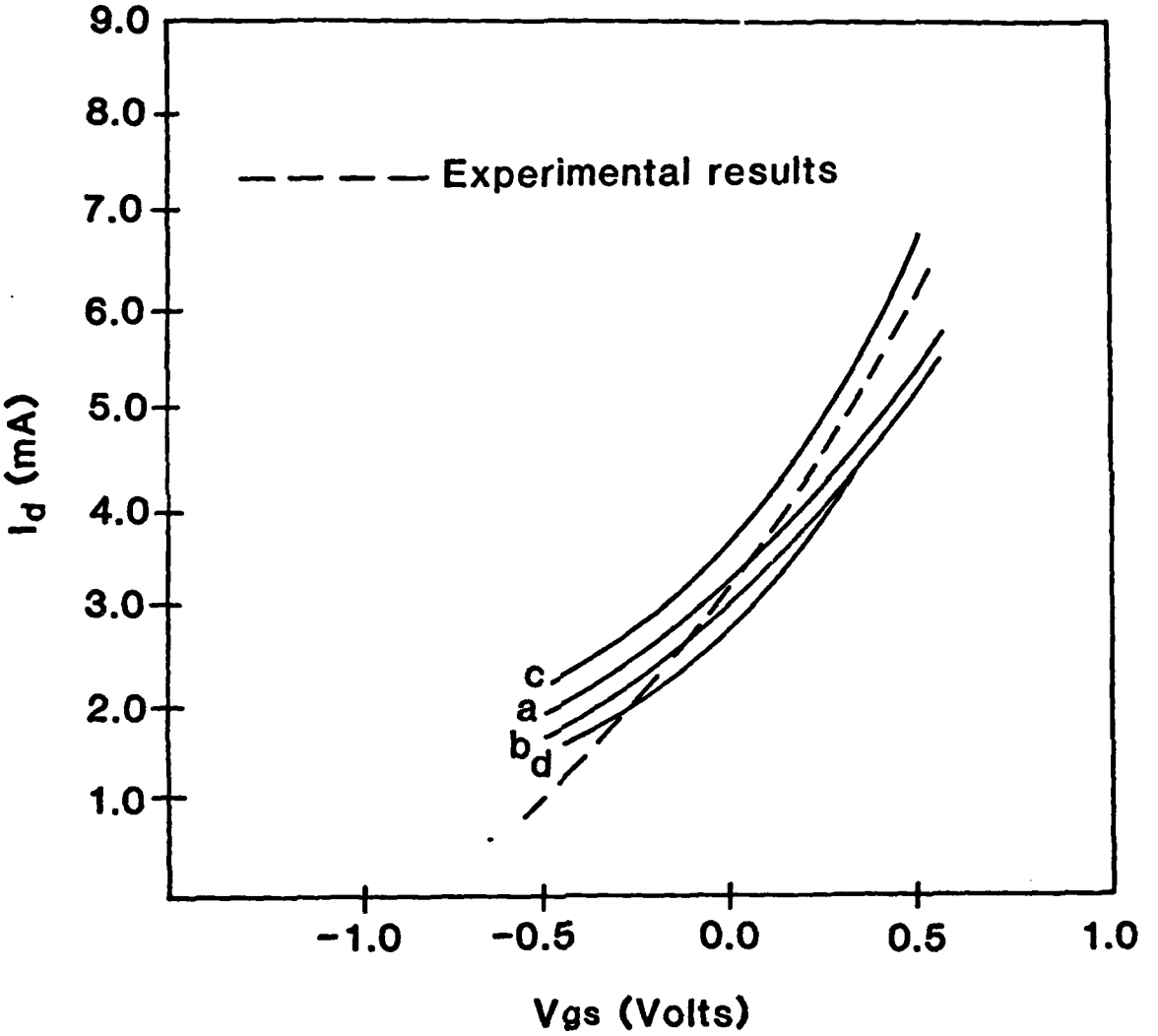


Figure 2.21 Comparison of calculated $I_d$ - $V_{ds}$ characteristics for different velocity-field models.

3. The carrier mobility may be lower than expected in the tail of the implanted profile.

4. The carrier density may be lower than expected due to carrier trapping.

5. The transport is not adequately modeled by a static velocity-field relationship.

These possibilities can now be examined in turn. Explanation 1 would require that the high-field saturation velocity be lower in lightly-doped regions than in heavily-doped regions and this is opposite to what one would expect theoretically. Explanation 2 is a real possibility. However, some initial calculations with somewhat arbitrary changes in the doping profile did not appear to improve the agreement. Explanation 3 would require that the mobility in lightly-doped material be lower than that in heavily-doped material and this is opposite to what would be expected from theory. Explanation 5 cannot be ruled out with the present calculations but can only be studied with the aid of a Monte Carlo technique such as that discussed elsewhere in this report. Finally possibility 4 appears to have considerable merit since traps are known to exist in GaAs and additional trapping states are introduced by the ion implantation process. The effect of traps is also of considerable theoretical interest and thus considerable effort has been expended to study the effects of including traps on the results as reported in the next section.

## 2.6 Effects of Electron Traps

Electron traps were included in the theoretical model as discussed in Section 2.1. In these initial calculations a uniform trap density has been assumed located somewhere near the center of the bandgap such that $n_1 \ll 10^{15}/cm^3$ (see equation (2.7)). Trap densities in the range of $1 - 5 \times 10^{15}/cm^3$ have been studied.

Figure 2.22 shows a comparison of experimental and calculated saturation current vs drain voltage (type I device) when a trap density of 3 x 1015/cm3

is included in the calculation. As can be seen from the results, the agreement between theory and experiment has improved considerably. Similar improvements were also found for the other doping profiles. Even with the traps as seen in Figure 2.22 the current still does not turn off quite as fast as the experimental device. This may be due to the inadequacy of the static velocity-field relationship or may be due to a non-uniform density of electron traps. What is needed to achieve better agreement is a trap density which increases on the tail of the implantation profile. This is in the direction that one expects from theoretical arguments since it is harder to anneal out the implantation damage on the tail of the profile than near the peak of the profile. Although the calculations have not been made, it appears that reasonably good agreement could be obtained with the turn-off characteristics if the experimental devices had electron traps in the range of $10^{15}$ /cm$^3$ near the peak of the prpfile, increasing to around 5 x $10^{15}$/cm$^3$ around the tails of the implanted profiles. These appear to be reasonable values but have not been independently verified.

Figures 2.23 and 2.24 illustrate the effects of the electron traps on the free-carrier density for a device near pinch-off. Figure 2.23 is for no traps and shows the deep hump in carrier density as previously described. Figure 2.24 with 3 x $10^{15}$/cm$^3$ traps, however, shows a considerably reduced free-electron density deep within the device resulting in a smaller drain current.

## 2.7 Calculations of Small Signal Parameters

The first order small-signal parameters have been calculated for several of the devices. These parameters are calculated by making small changes in either the gate or drain voltage and observing changes in the external and

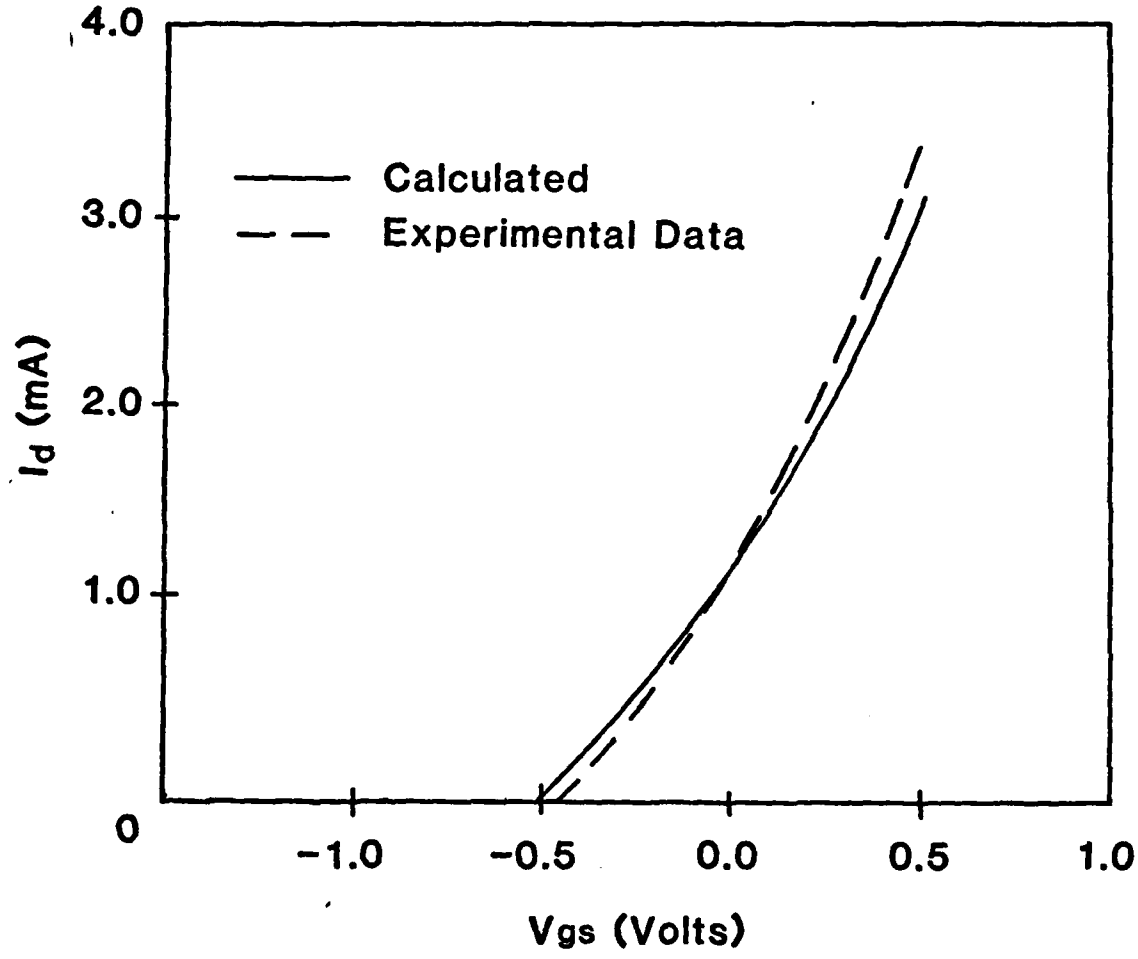


Figure 2.22 Comparison of calculated and experimental $I_d - V_{ds}$ characteristics for a constant low-field model with $3 \times 10^{15}$ $cm^{-3}$ electron traps.

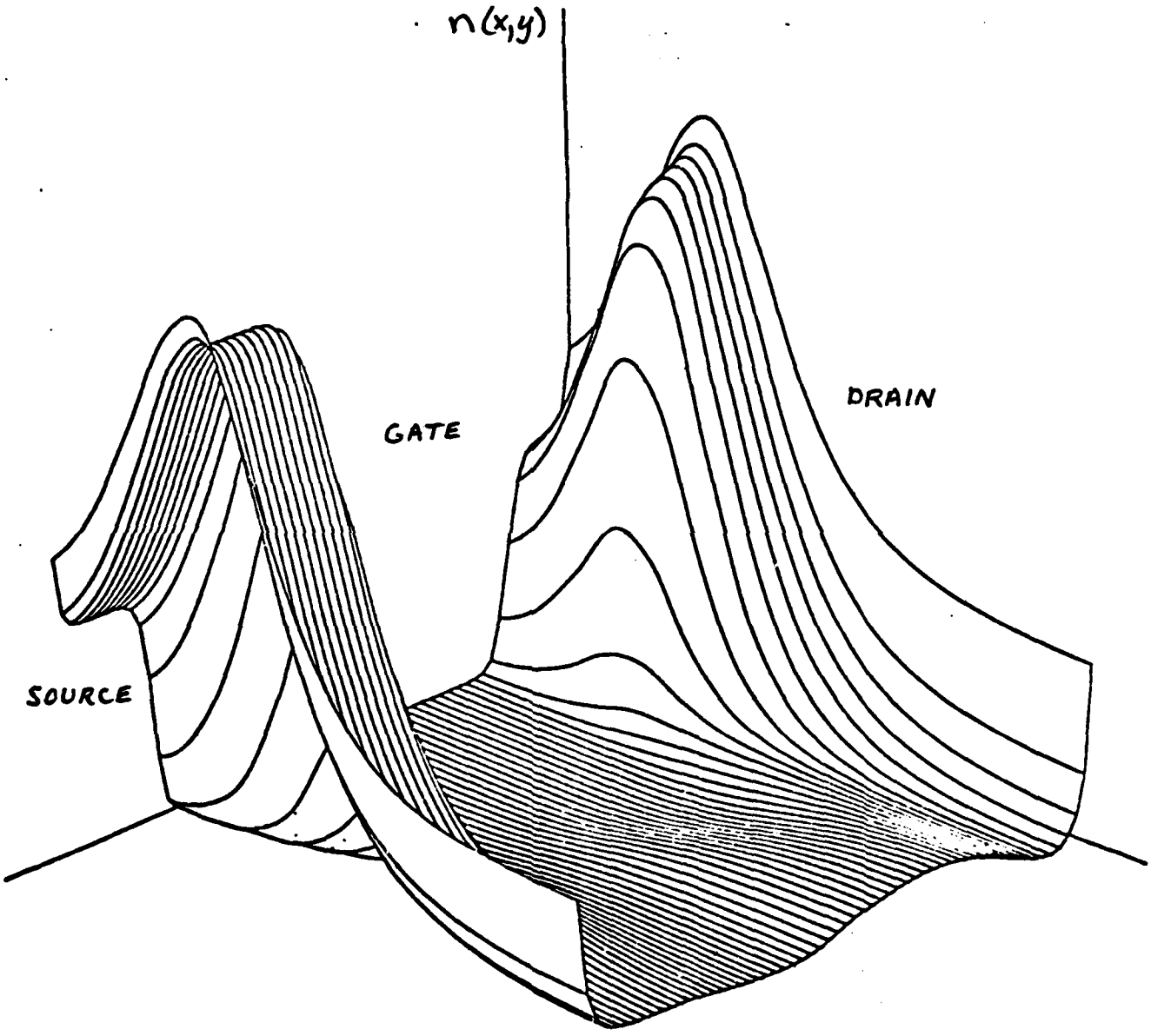


Figure 2.23 Electron density near pinch-off for a type I device at $V_{ds}$ = 2.5V and $V_{gs}$ = -0.5V without electron traps.

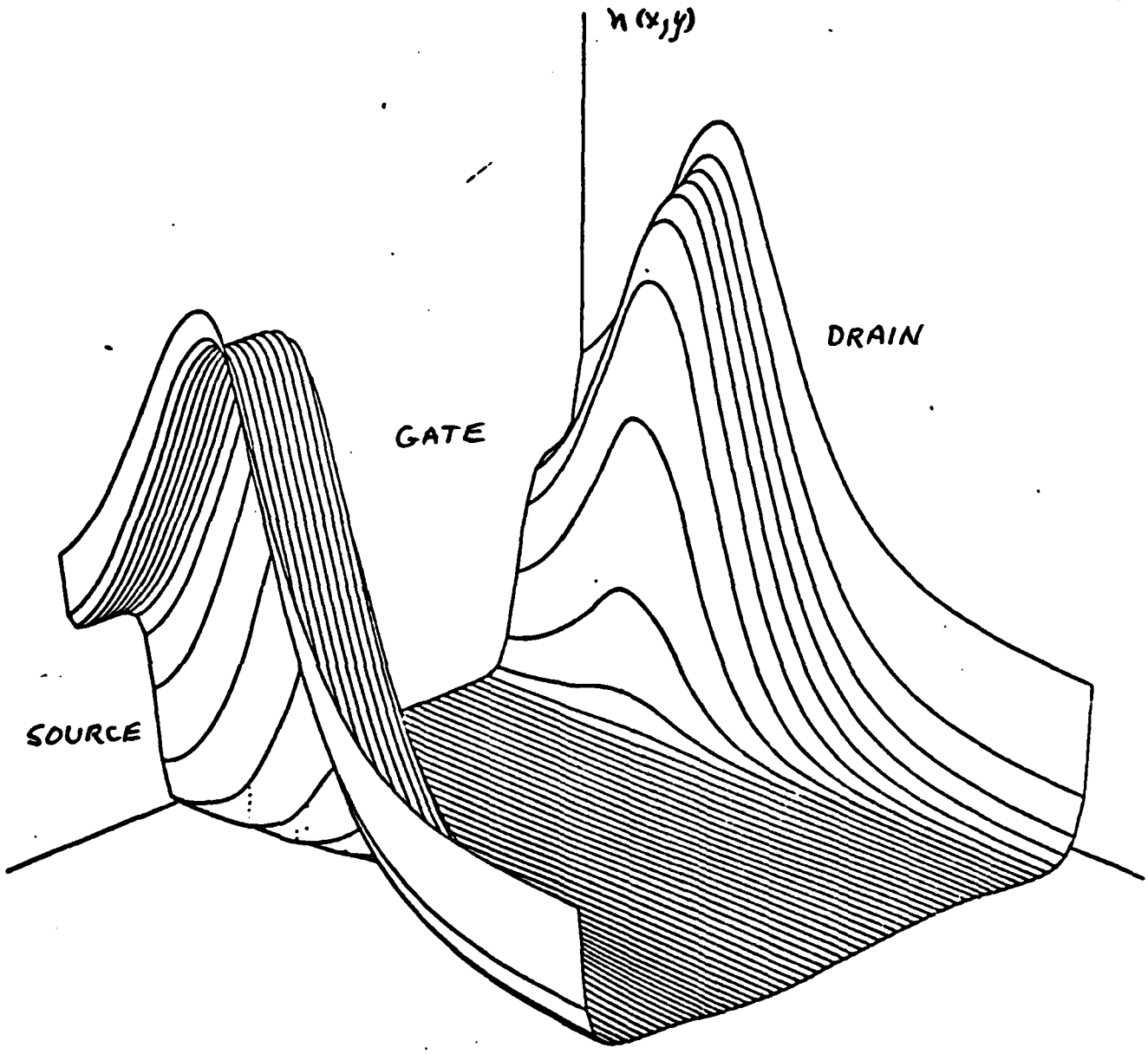


Figure 2.24 Electron density near pinch-off for a type I device at $V_{ds}$ = 2.5V, $V_{gs}$ = -0.5V with 3 x $10^{15}$ $cm^{-3}$ electron traps.

internal device parameters. The typical change in drain voltage was 0.1 volt and that of gate voltage was 0.01 volt. The small-signal parameters were calculated as

$$g_m = \frac{\Delta I_d}{\Delta V_{gs}} , \tag{2.12}$$

$$g_d = \frac{\Delta I_d}{\Delta V_{ds}} , \tag{2.13}$$

$$C_{gs} + C_{gd} = \frac{\Delta Q_g}{\Delta V_{gs}} , \tag{2.14}$$

$$C_{gd} = \frac{\Delta Q_g}{\Delta V_{ds}} . \tag{2.15}$$

In the case of the capacitance values, the gate charge was obtained by integrating the normal component of the electric field immediately under the gate over the gate area and using the relationship $\sigma = \varepsilon E$ where $\sigma$ is the surface charge density. By comparing the gate charge at two drain voltages, the capacitance values were obtained.

Additional information on device operation can be obtained by looking at the internal changes in the charge density when the terminal voltages change by small amounts. Figure 2.25 shows the change in free electron concentration when the drain voltage changes. This charge change occurs mainly in the region between the gate and drain contact as the depletion region widens around the gate toward the drain. A smaller change is seen under the gate near the drain end of the device. This represents the charge distribution which must flow into and out of the device as the drain voltage changes.

A similar plot is shown in Figure 2.26 of the internal change in electron concentration when the gate voltage changes. The major change in charge occurs under the gate and the distribution extends throughout the entire device

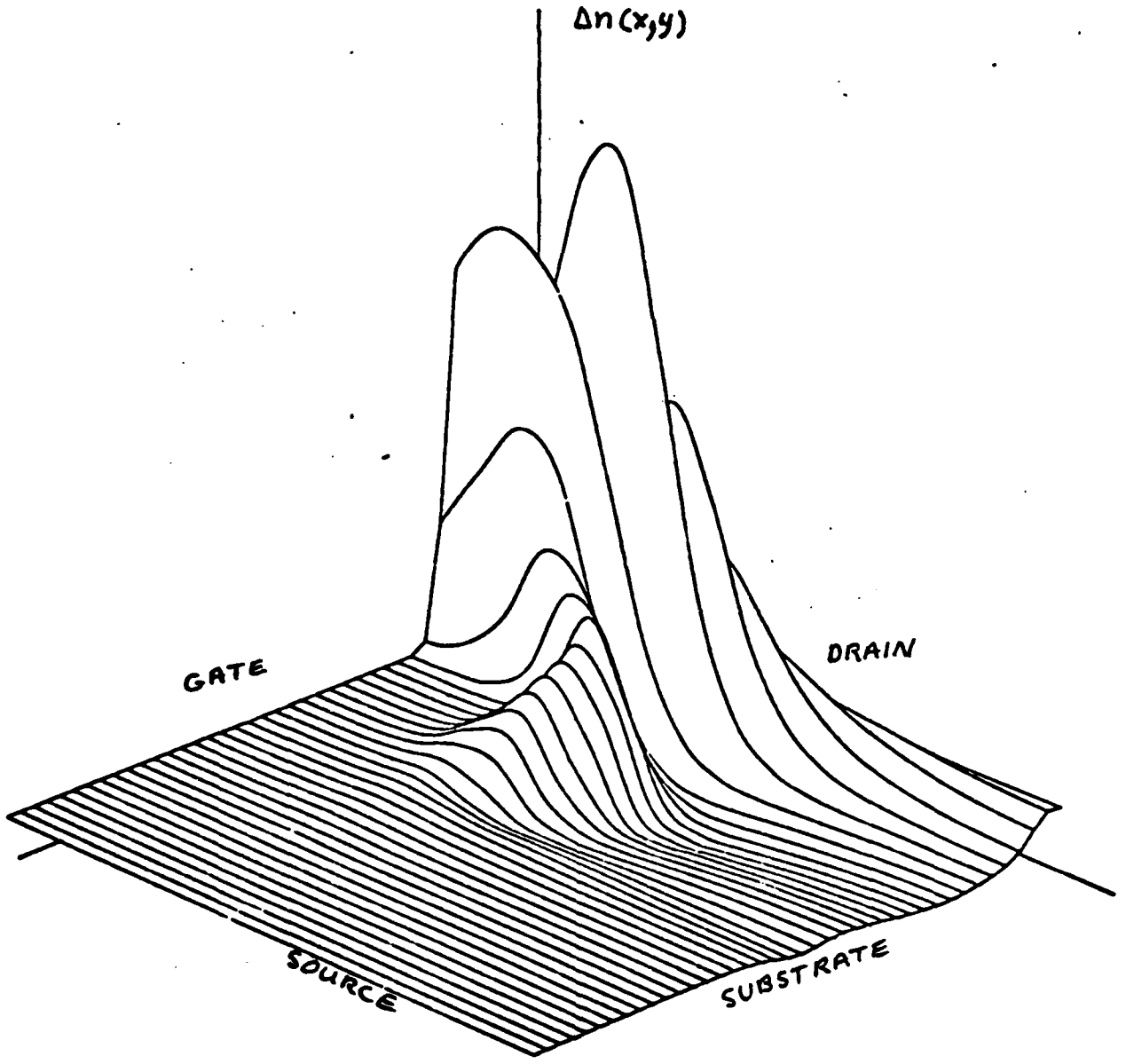


Figure 2.25 Typical change in electron density for a 0.1V change in drain voltage at $V_{ds}$ = 2.5V and $V_{gs}$ = 0V.

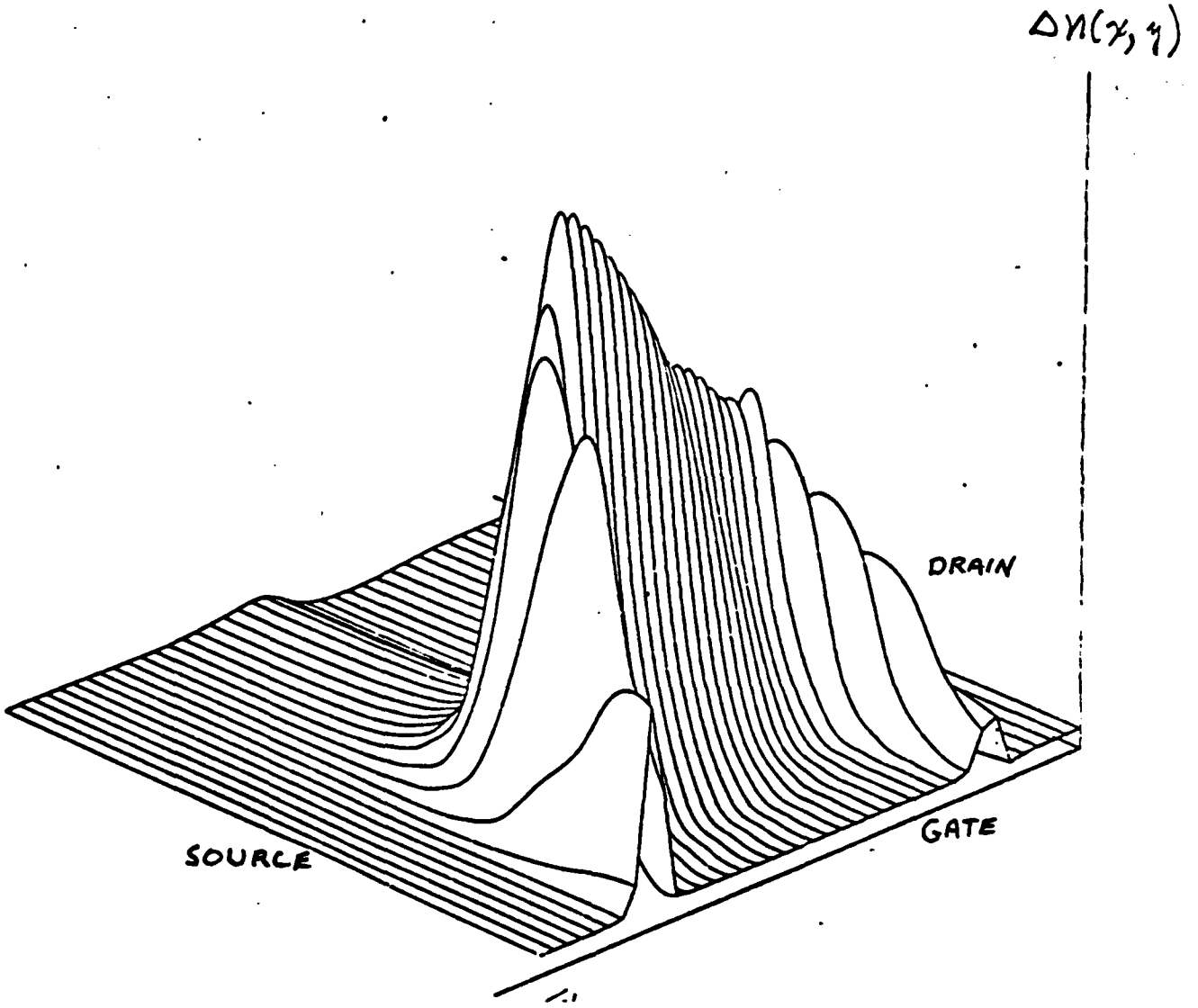


Figure 2.26 Typical change in electron density for a 0.01V change in gate voltage at $V_{ds}$ = 2.5V and $V_{gs}$ = 0V.

dimenison. The total charge change is about an order of magnitude larger for a given change in gate voltage than for the same change in drain voltage.

Complete calculations for terminal $I_d$ - $V_{ds}$ and small-signal parameters for two doping profiles and two velocity-field models are shown in Figures 2.27-2.46. The conditions used in the various calculations are summarized below:

A. Type I impurity profile

   a. Varying low-field mobility and no traps — Figures 2.27-2.31.

   b. Constant low-field mobility and 3 x $10^{15}/cm^3$ traps — Figures 2.32-2.36.

B. Type III impurity profile

   a. Varying low-field mobility and no traps — Figures 2.37-2.41.

   b. Constant low-field mobility and 3 x $10^{15}/cm^3$ traps — Figures 2.42-2.46.

In case a above the low-field mobility was varied according to Figure 2.3. In case b the low-field mobility was held fixed at 8000 $cm^2/V \cdot sec$. The best agreement with experimental $I_d$ - $V_{ds}$ characteristics was obtained for the case of constant low-field mobility plus traps. Thus one would expect that the corresponding small-signal parameters would agree more closely with experimental values although such values were not available for comparison.

In each case the $I_d$ - $V_{ds}$ characteristic are about as one would expect for low pinch-off MESFET devices and no negative resistance values were observed in any of the calculations. The transconductance values, $g_m$, are essentially independent of drain voltage in the current-saturation region and increase somewhat in all cases for higher turn-on voltages.

The gate-to-source capacitance values are essentially independent of drain voltage as one would expect, but change with gate-to-source voltage again approximately as expected from first-order device models. The

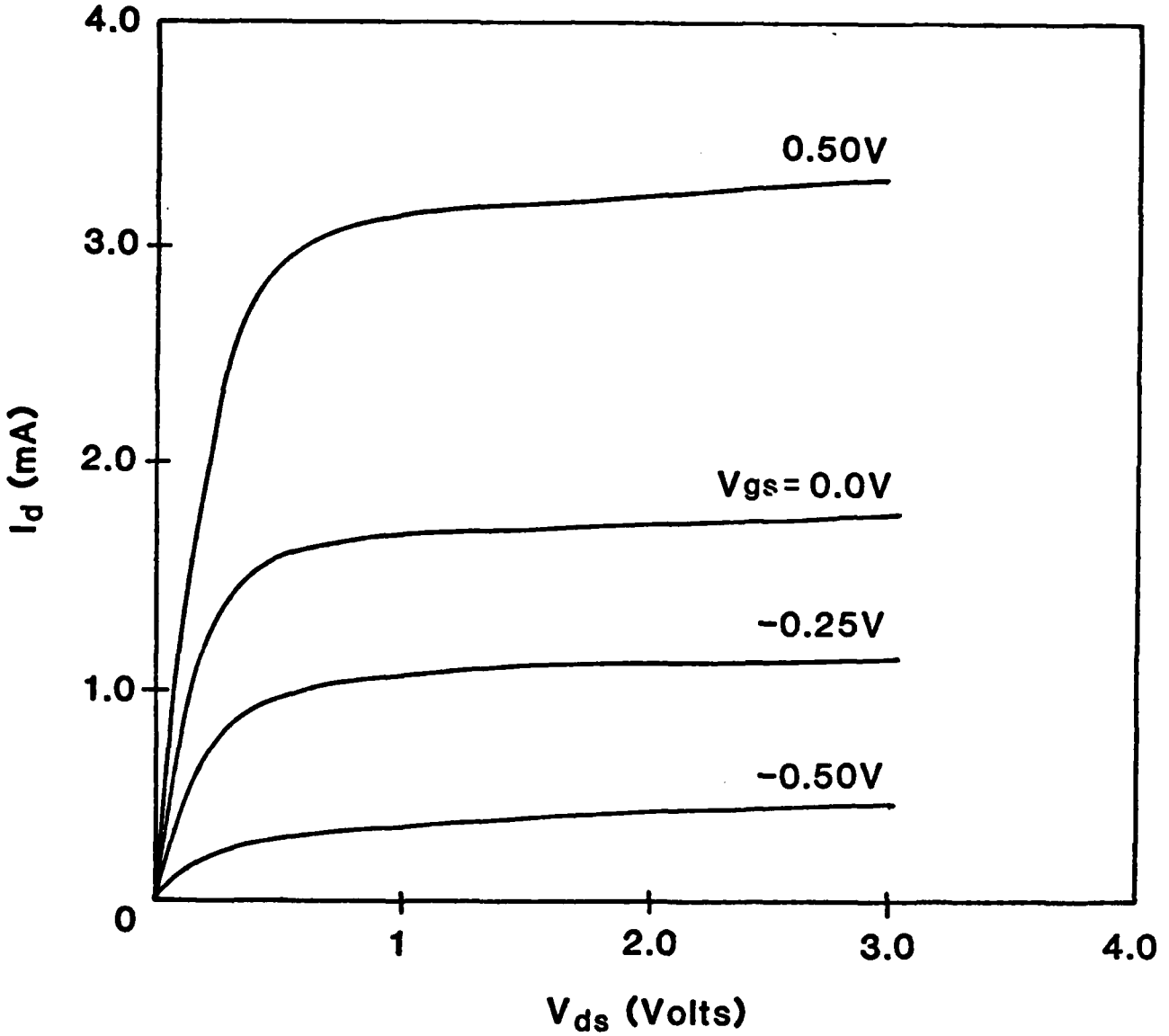


Figure 2.27 Calculated drain current characteristics for a type I device using a varying low-field mobility but with no electron traps.

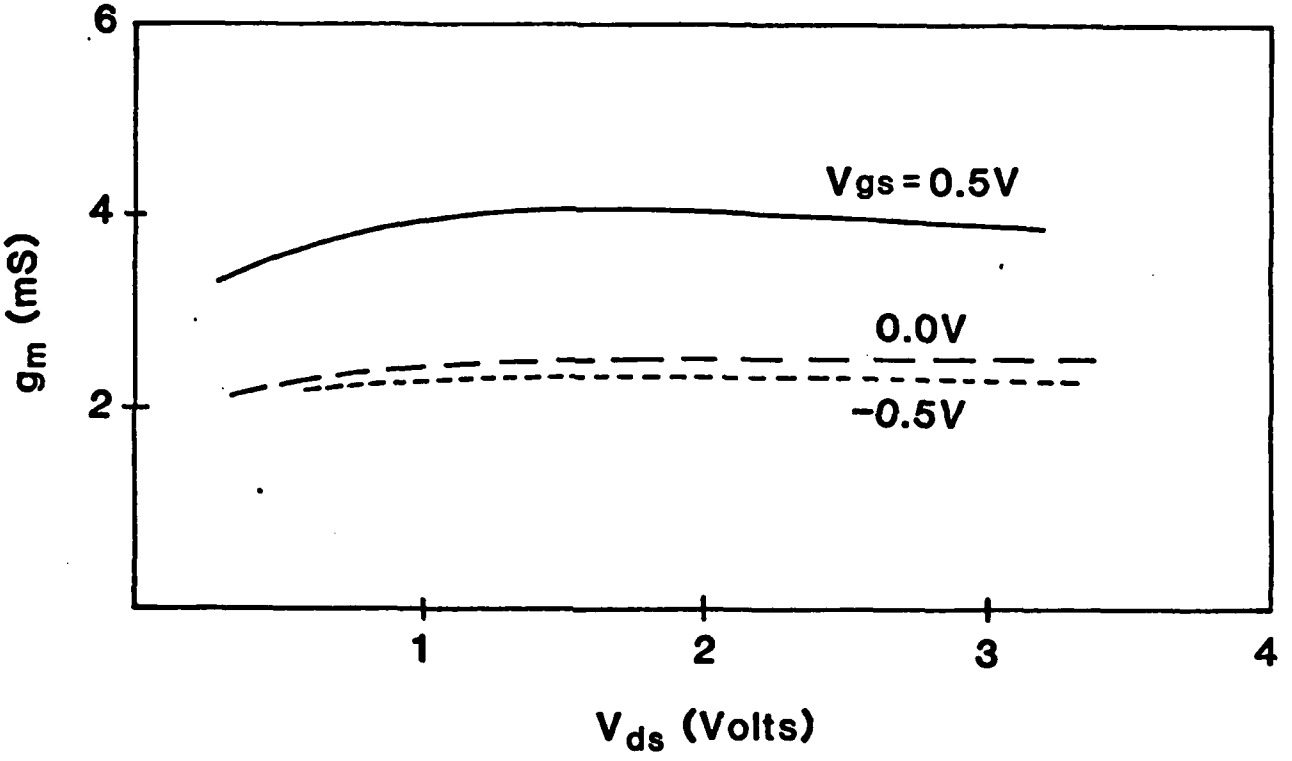


Figure 2.28 Calculated small-signal transconductance for same conditions as Fig. 2.27.

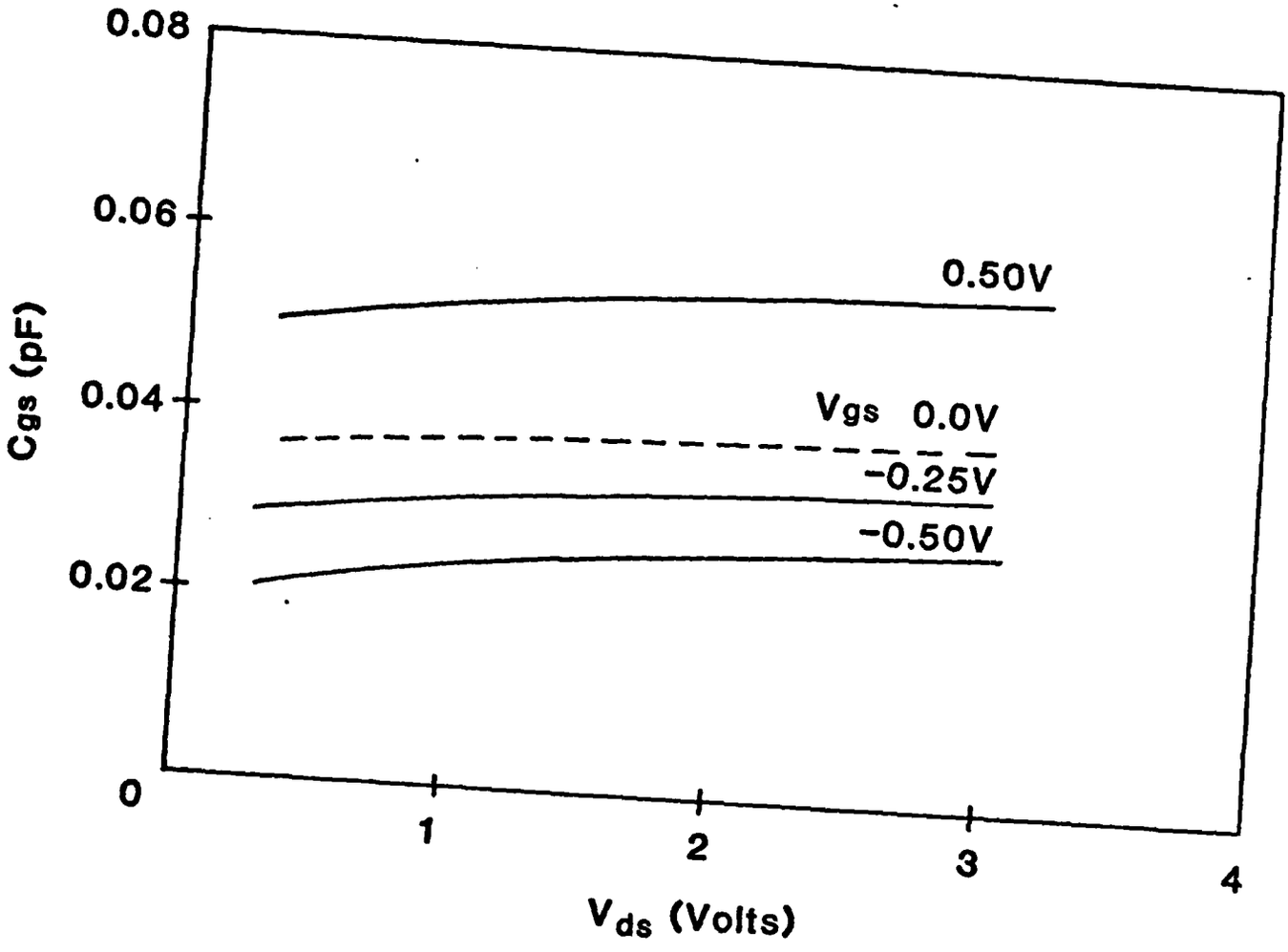


Figure 2.29 Calculated gate-to-source capacitance for same conditions as Fig. 2.27.

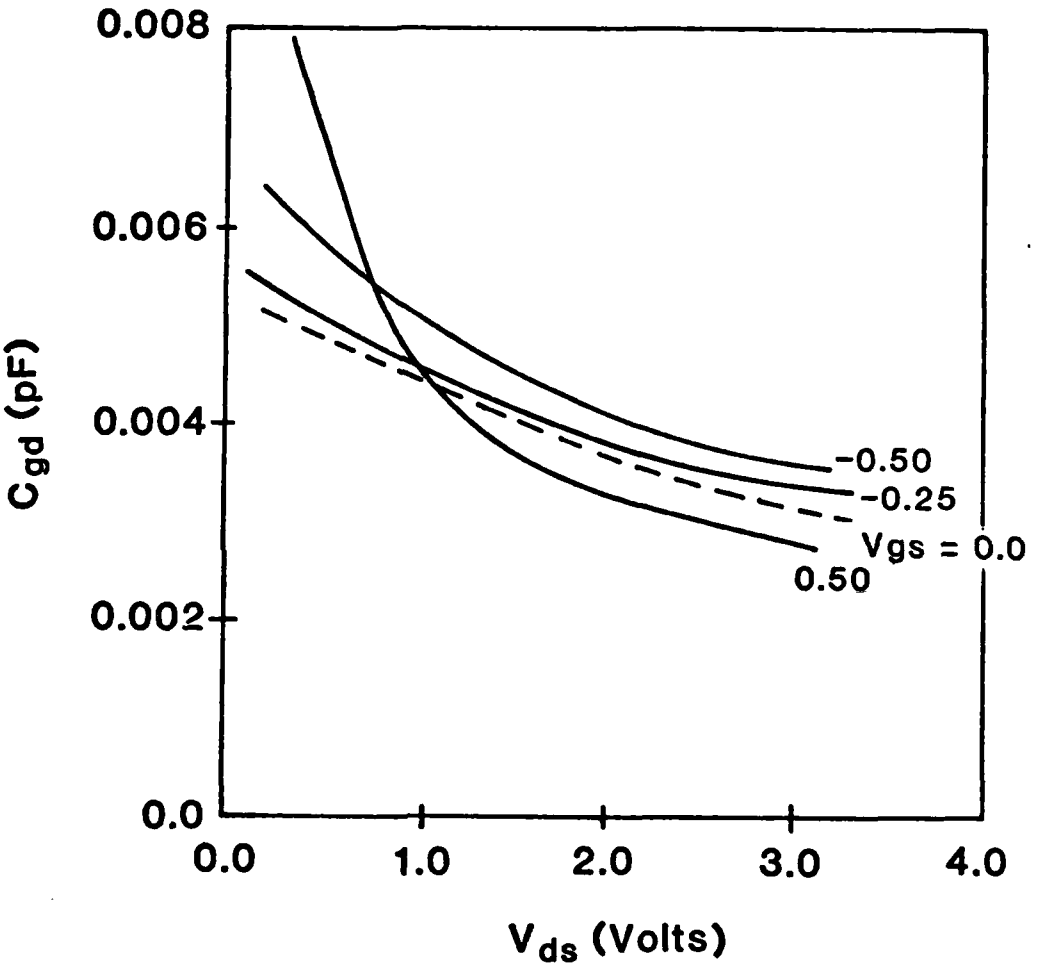


Figure 2.30 Calculated gate-to-drain capacitance for same conditions as Fig. 2.27.

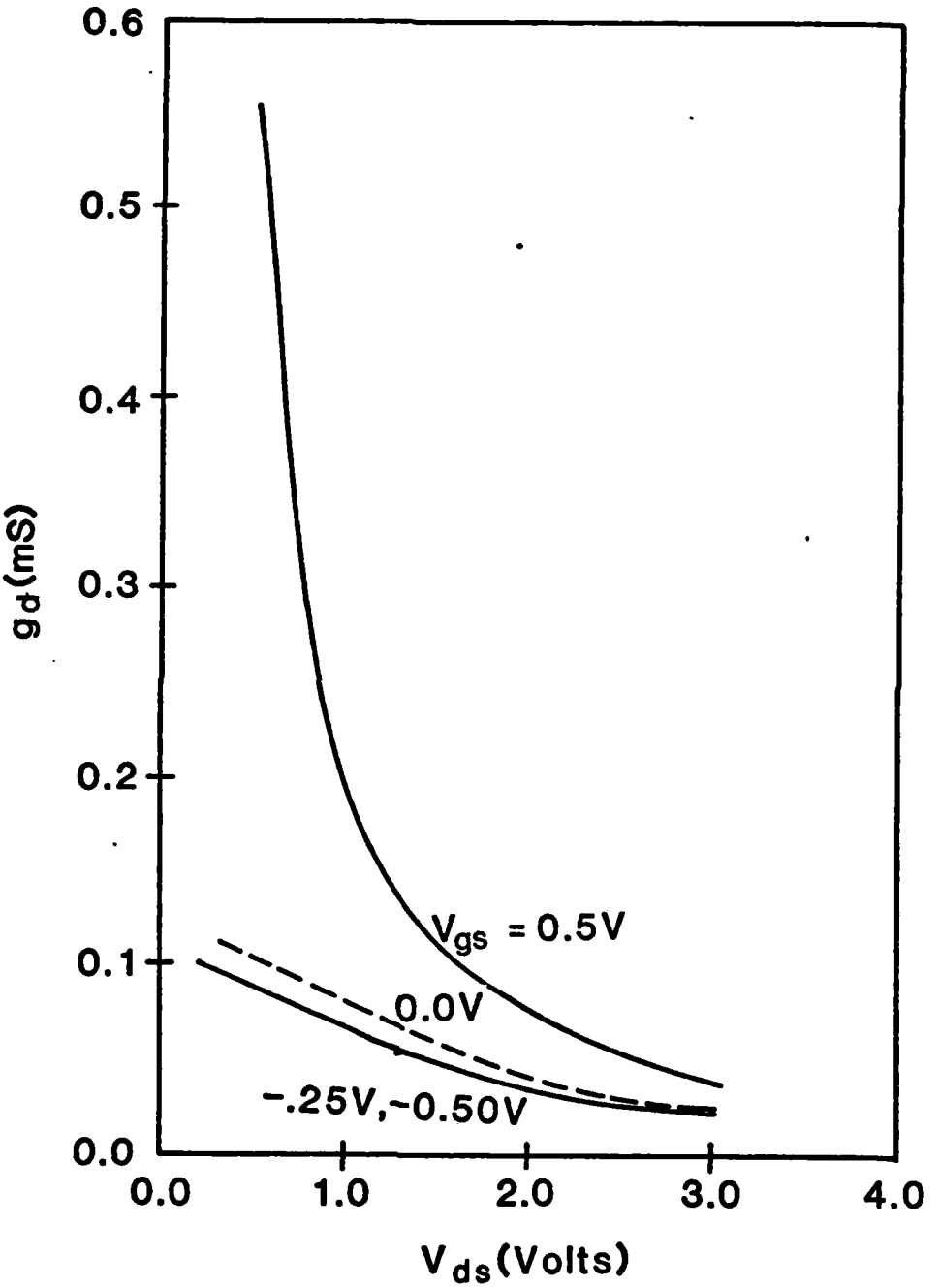


Figure 2.31 Calculated small-signal drain conductance for same conditions as Fig. 2.27.

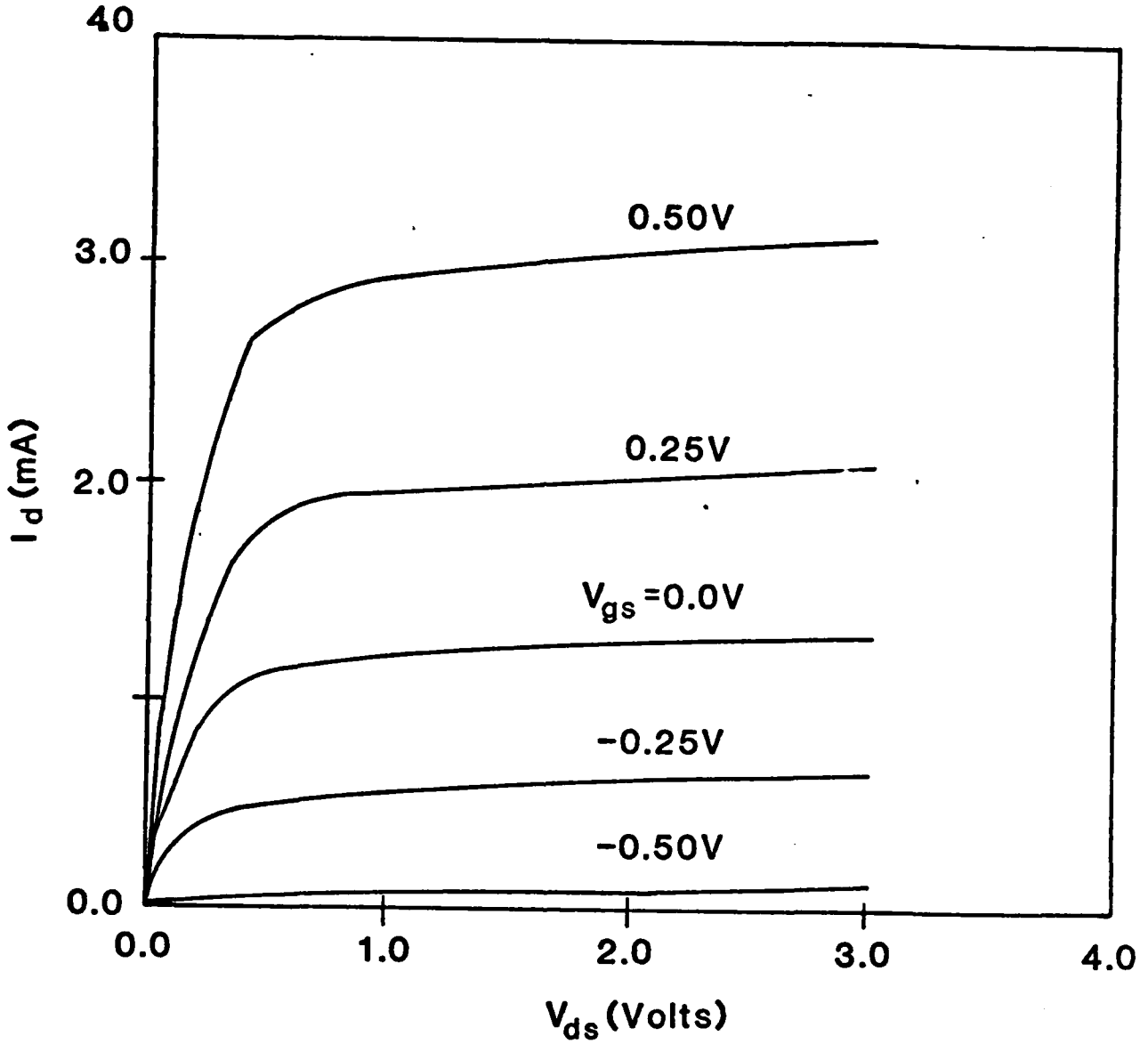


Figure 2.32 Calculated drain current characteristics for a type I device using a constant low-field mobility (8000 $cm^2$/v-sec) and with $3x10^{15}$ $cm^{-3}$ electron traps.

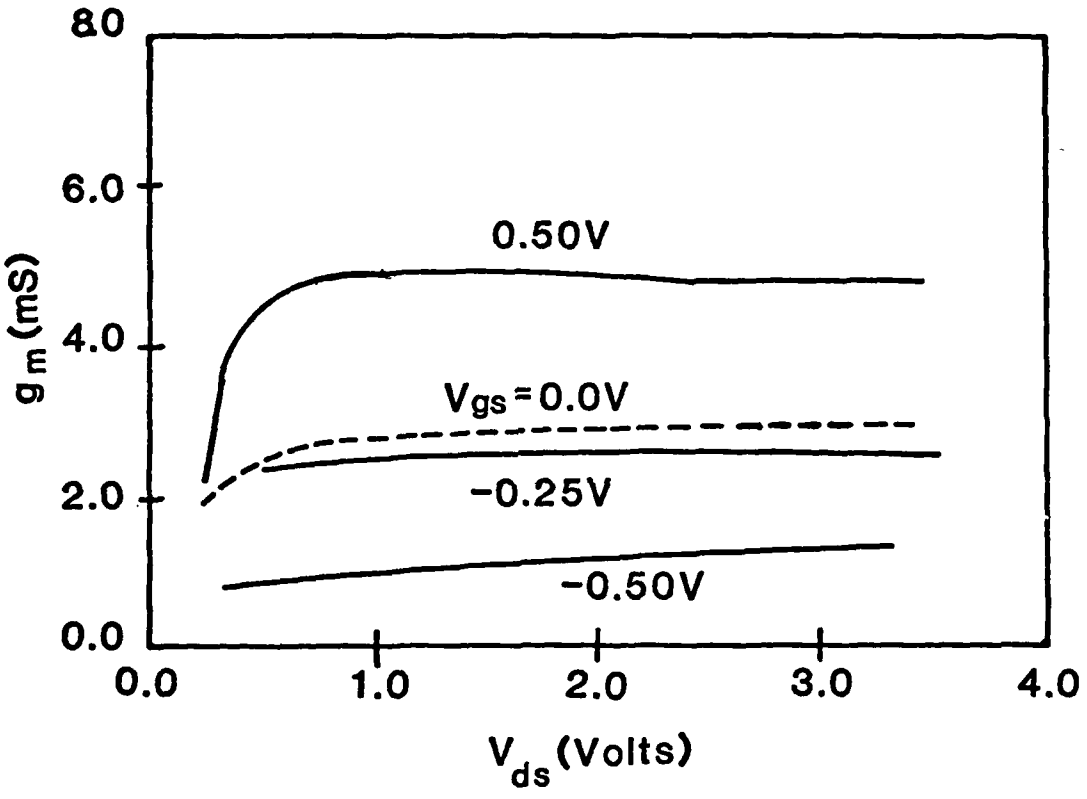


Figure 2.3. Calculated small-signal transconductance for Fig. 2.32 conditions.

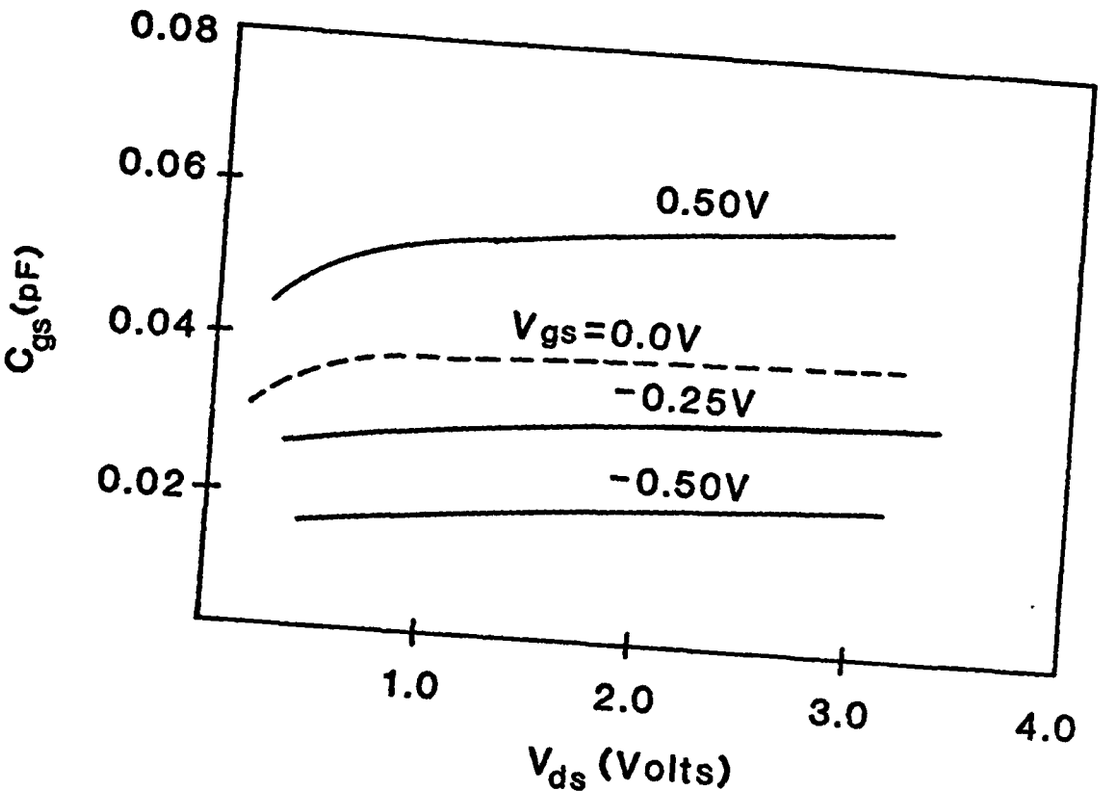


Figure 2.34 Calculated gate-to-source capacitance for Fig. 2.32 conditions.

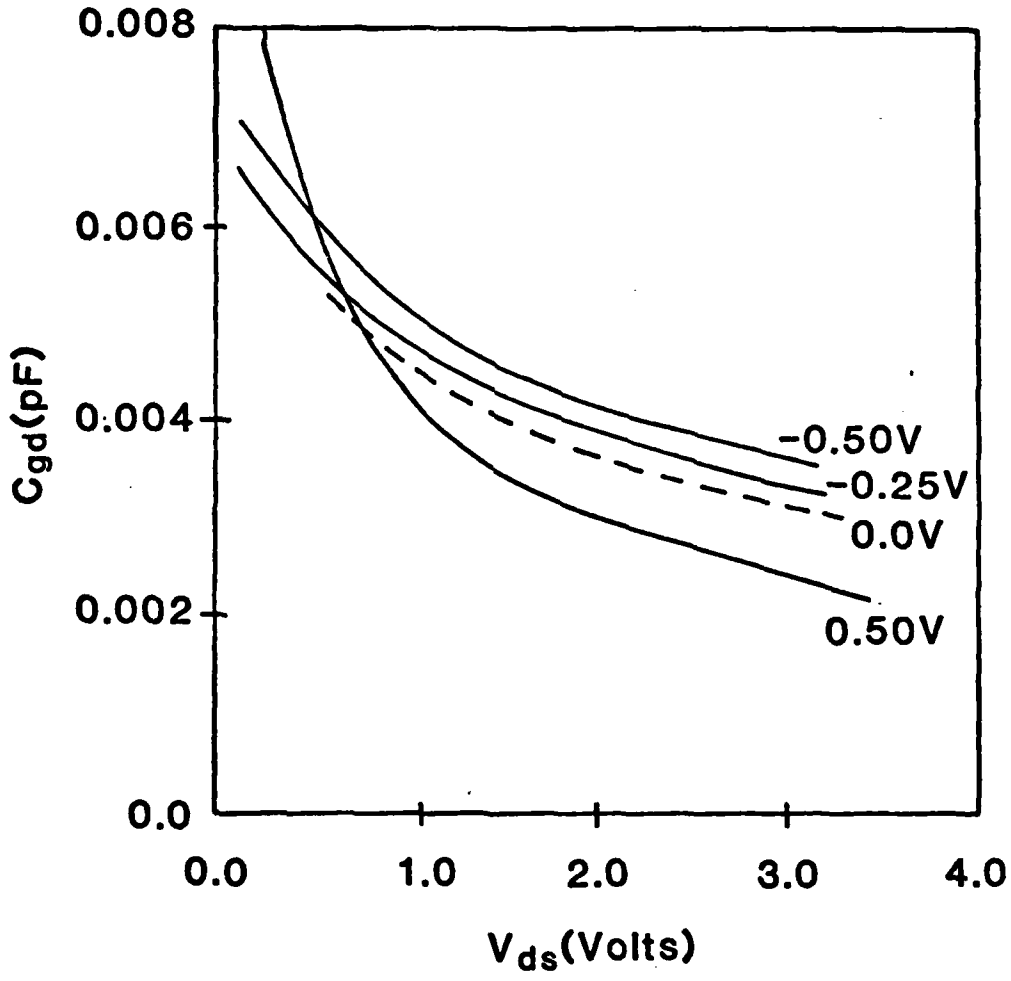


Figure 2.35 Calculated gate-to-drain capacitance for Fig. 2.32 conditions.

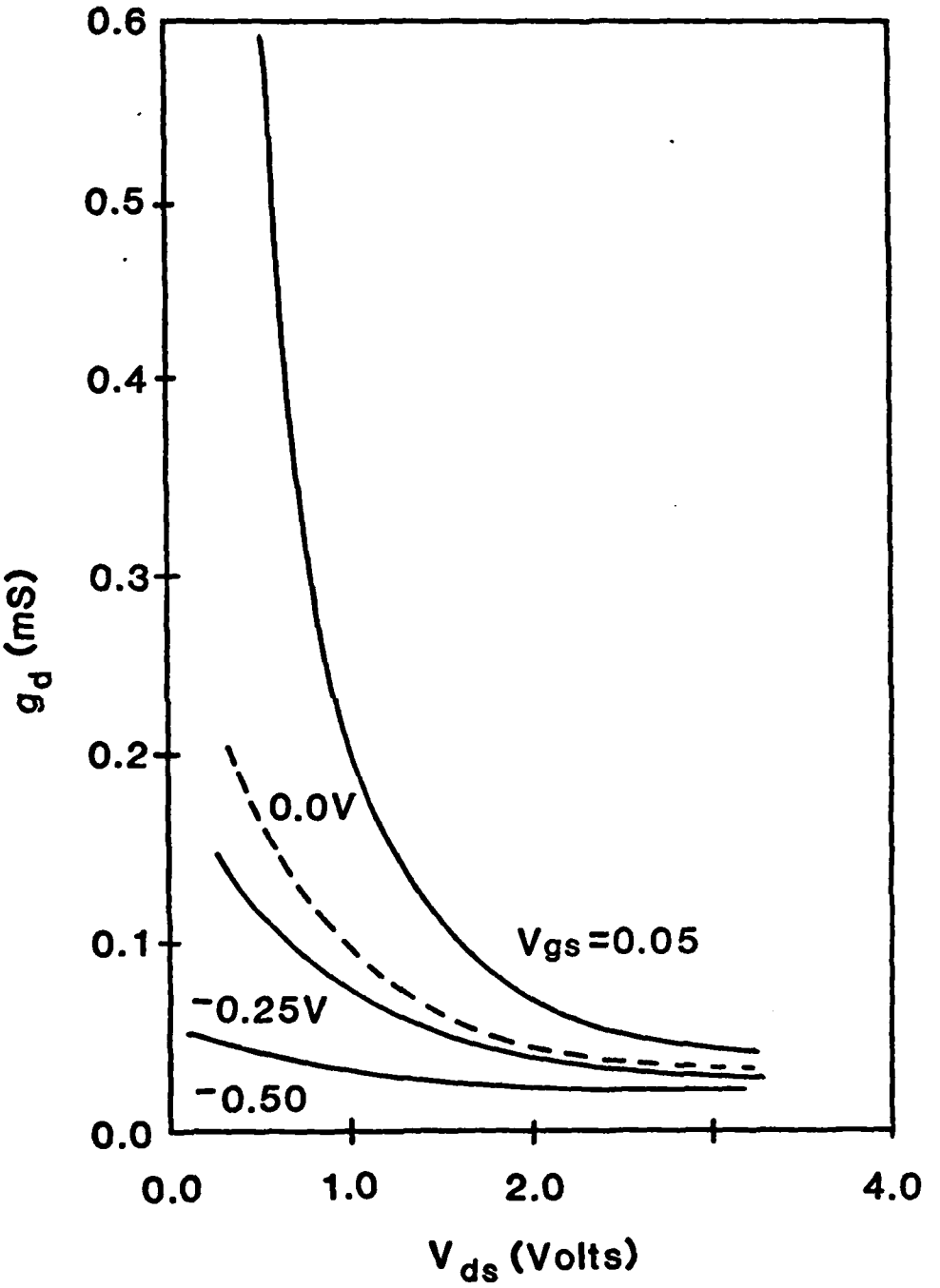


Figure 2.36 Calculated small-signal drain conductance for Figure 2.32 conditions.

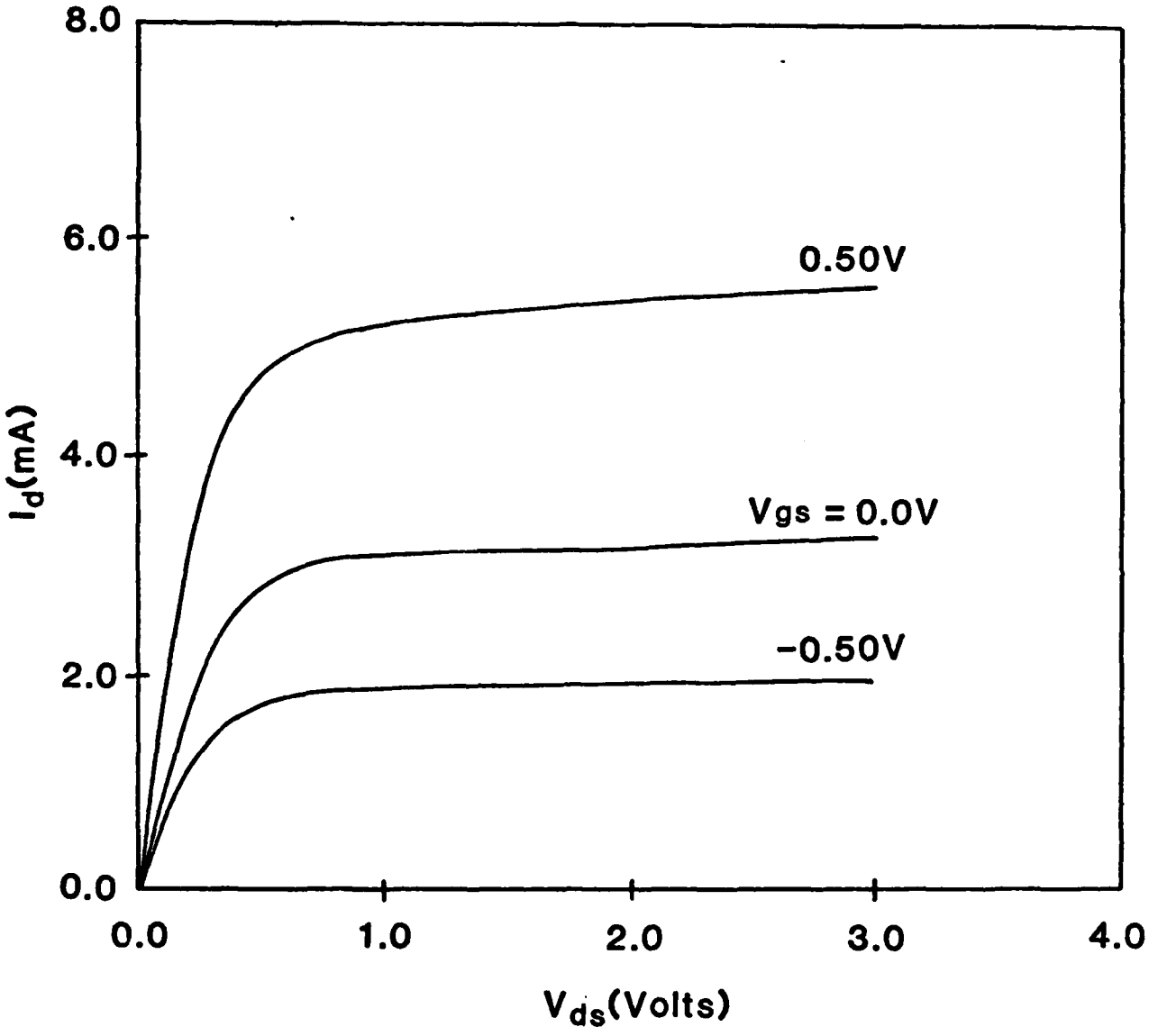


Figure 2.37 Calculated drain current characteristics for a Type III device using a varying low-field mobility but with no electron traps.

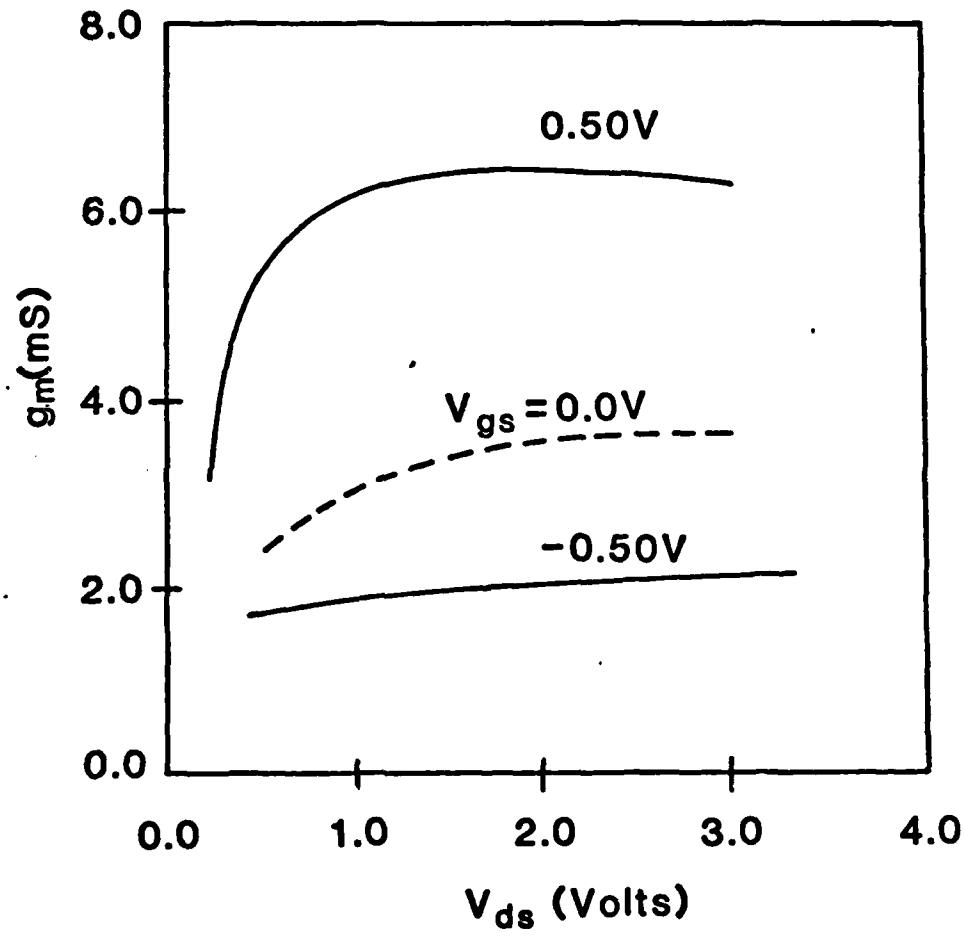


Figure 2.38 Calculated small-signal transconductance for Figure 2.37 conditions.

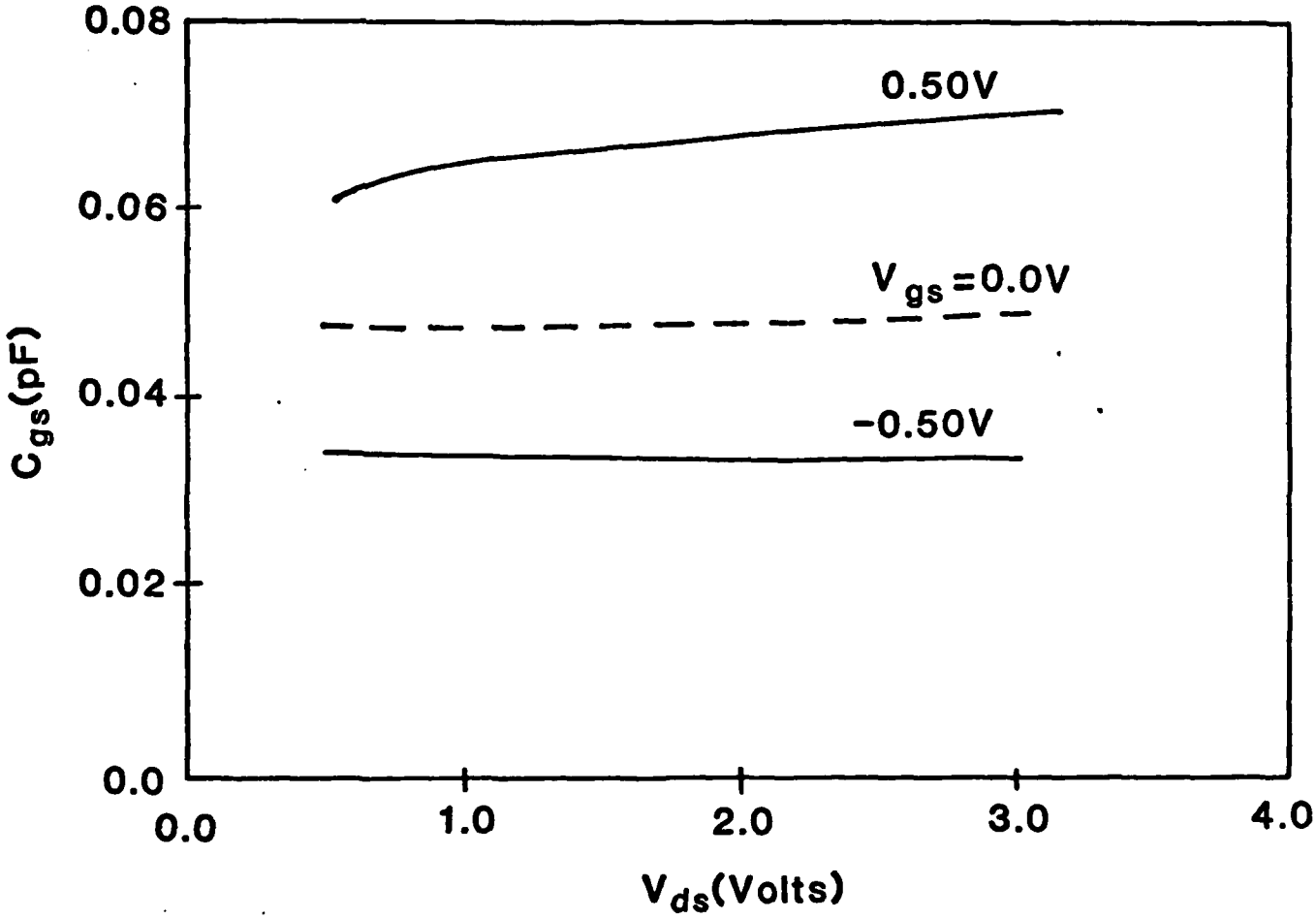


Figure 2.39 Calculated gate-to-source capacitance for Figure 2.37 conditions.

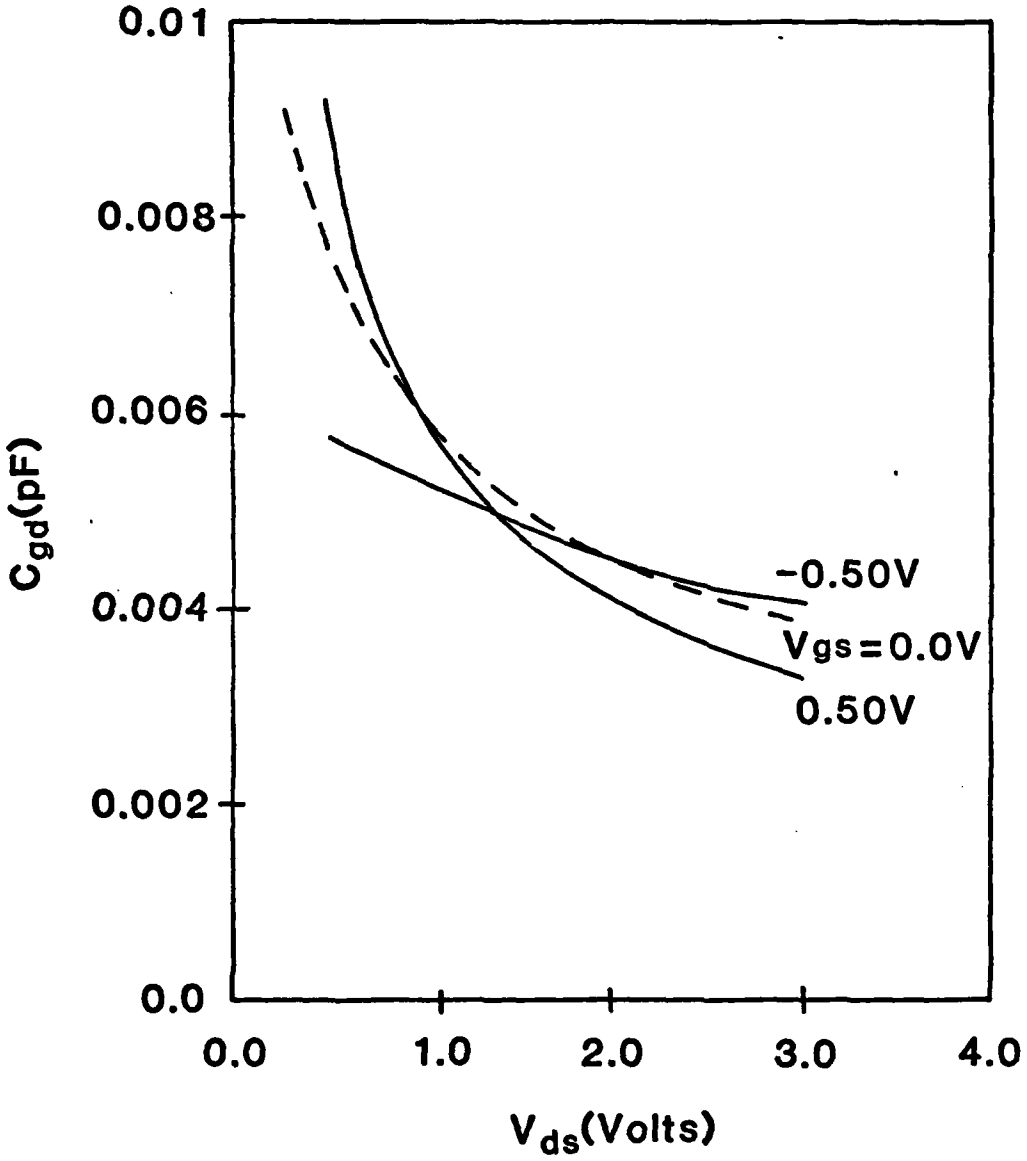


Figure 2.40 Calculated gate-to-drain capacitance for Figure 2.37 conditions.

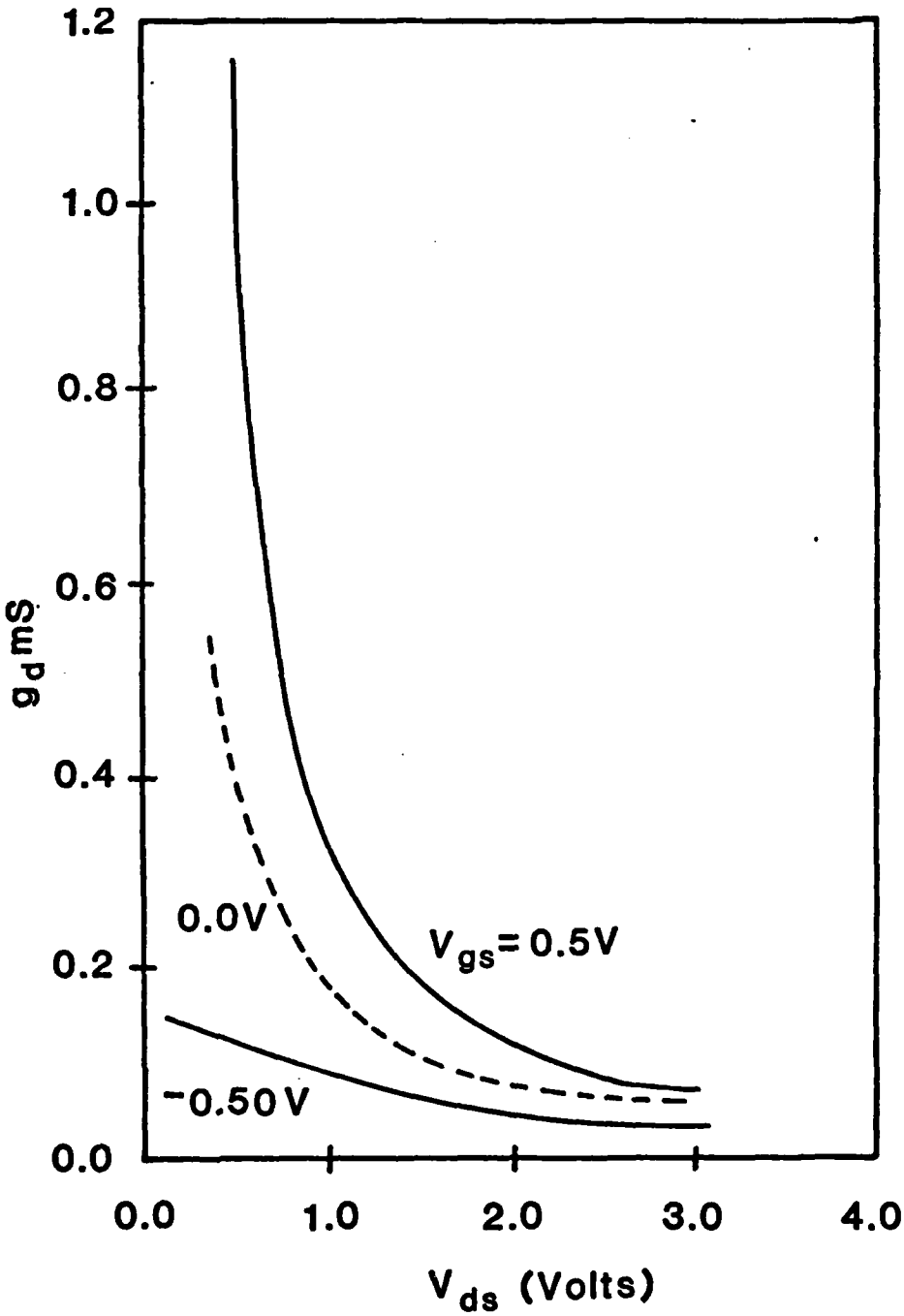


Figure 2.41 Calculated small-signal drain conductance for Figure 2.37 conditions.

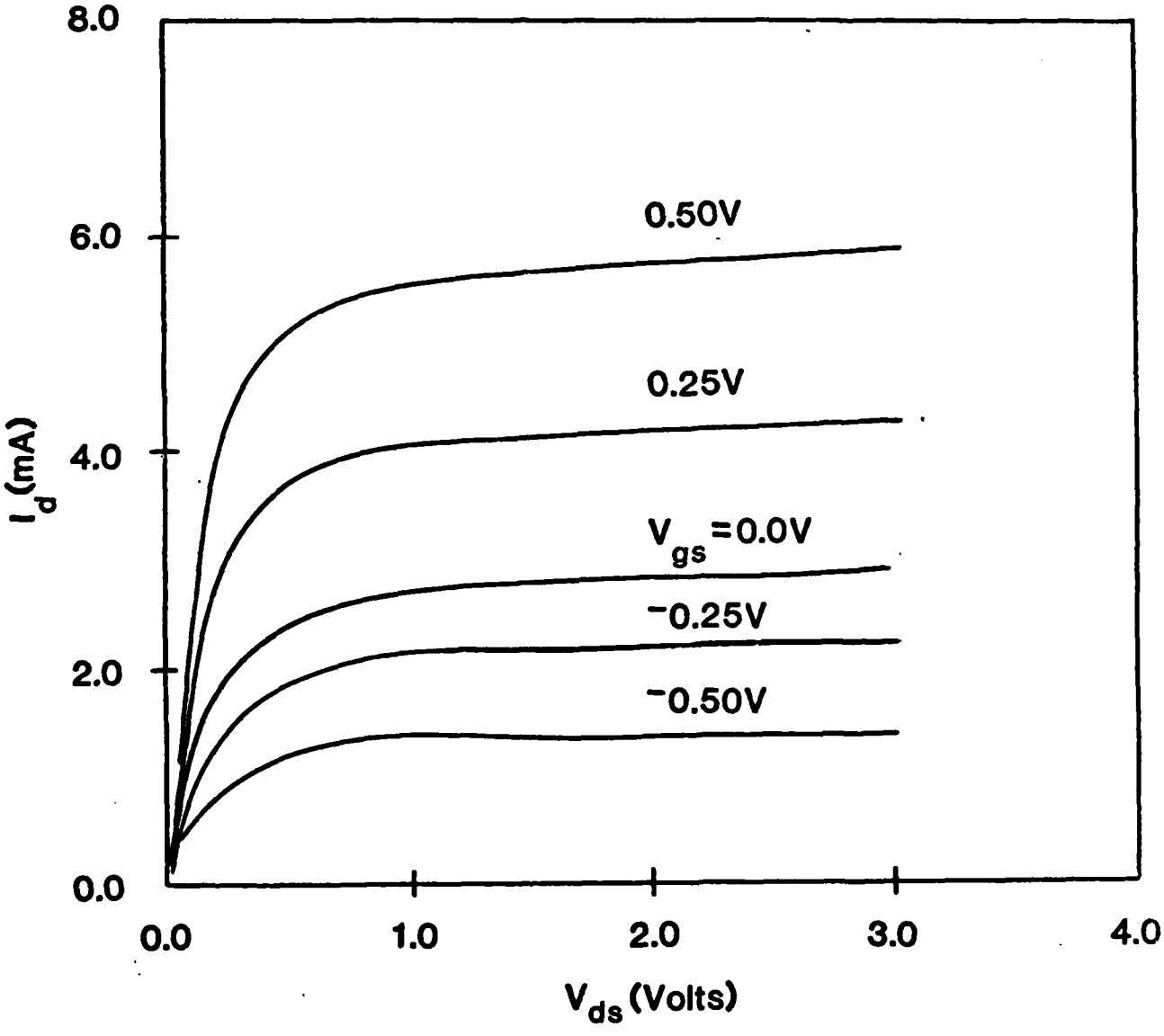


Figure 2.42 Calculated drain current characteristics for a type III device using a constant low-field mobility (8000 $cm^2$/v-sec) and with $3x10^{15}cm^{-3}$ electron traps.

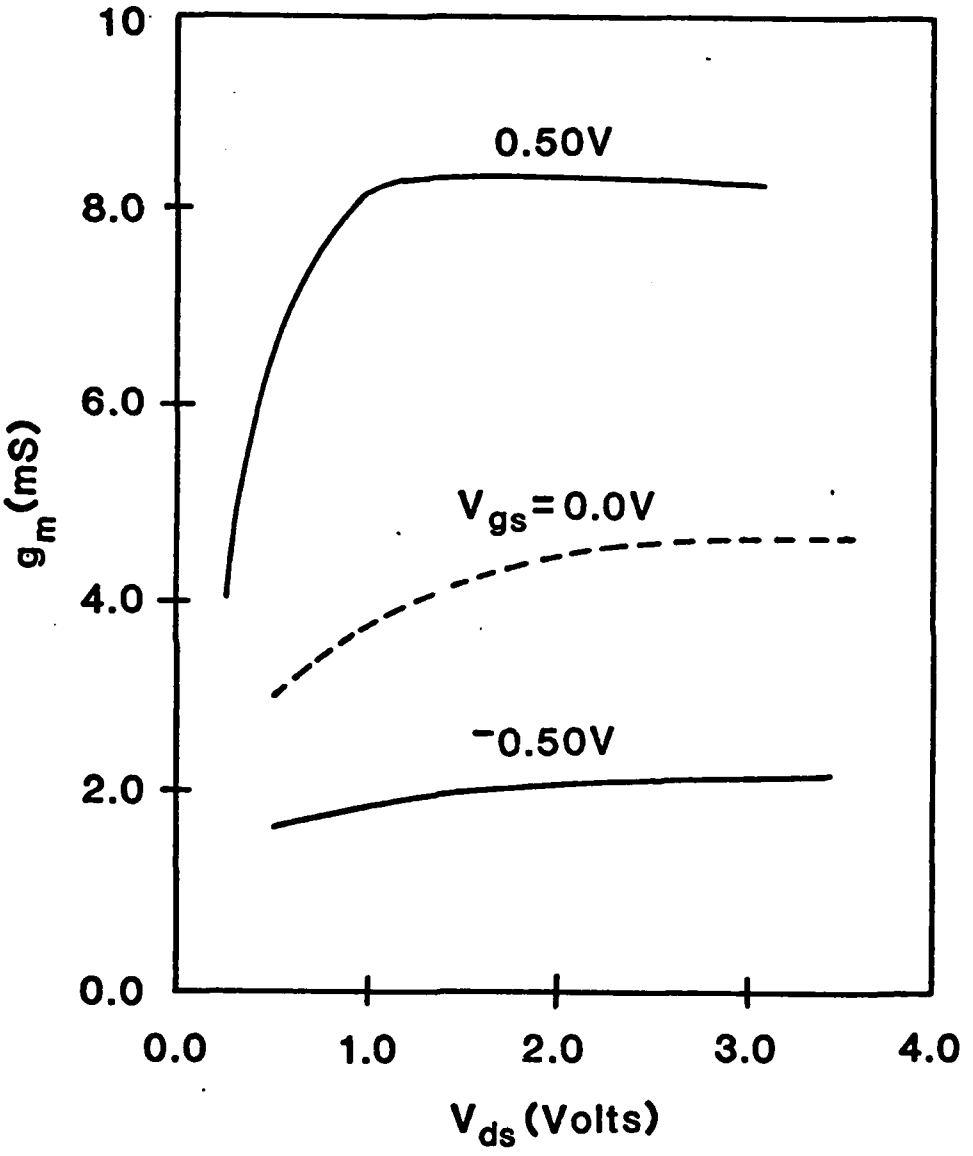


Figure 2.43 Calculated small-signal transconductance for Figure 2.42 conditions.

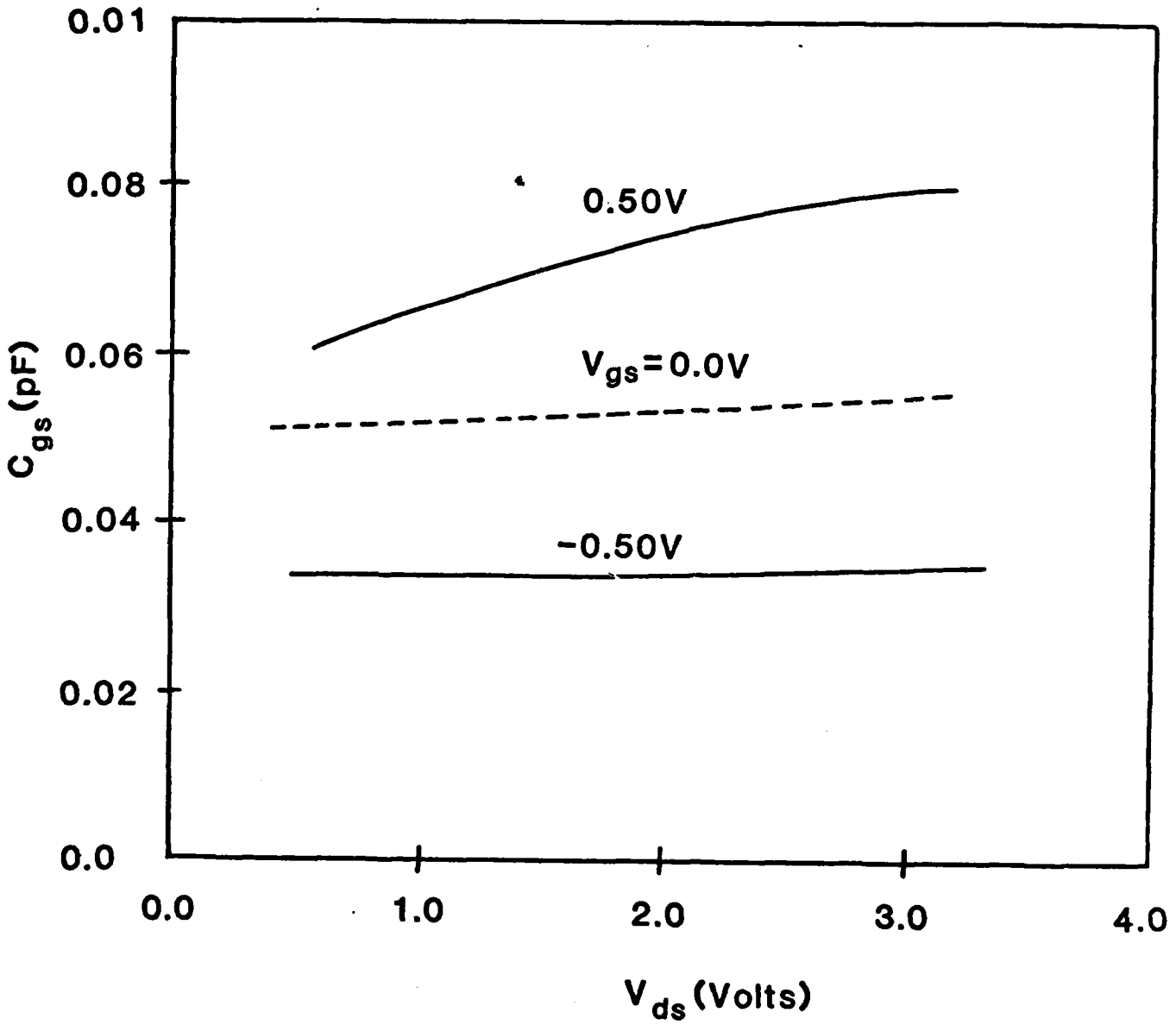


Figure 2.44 Calculated gate-to-source capacitance for Figure 2.42 conditions.

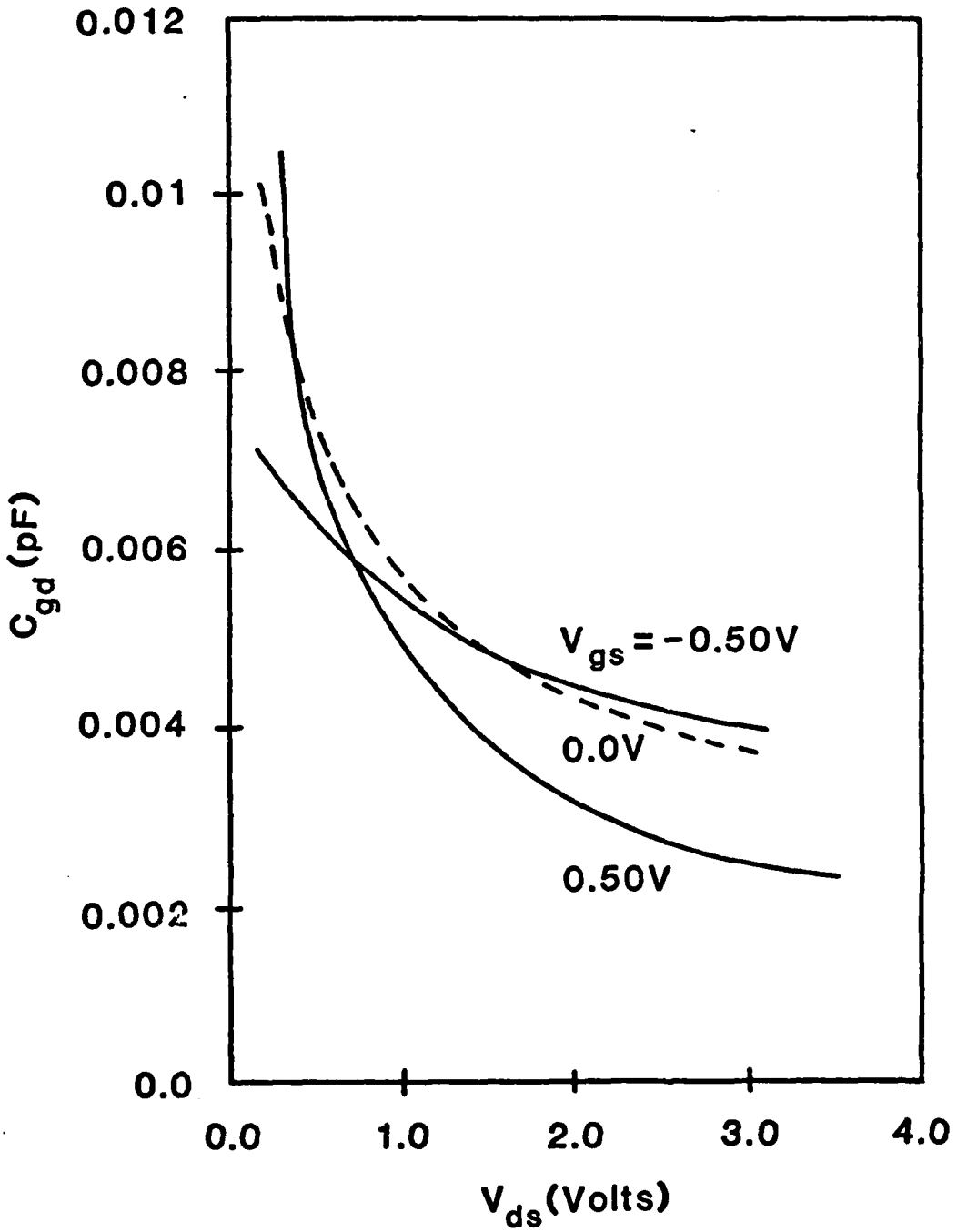


Figure 2.45 Calculated gate-to-drain capacitance for Figure 2.42 conditions.

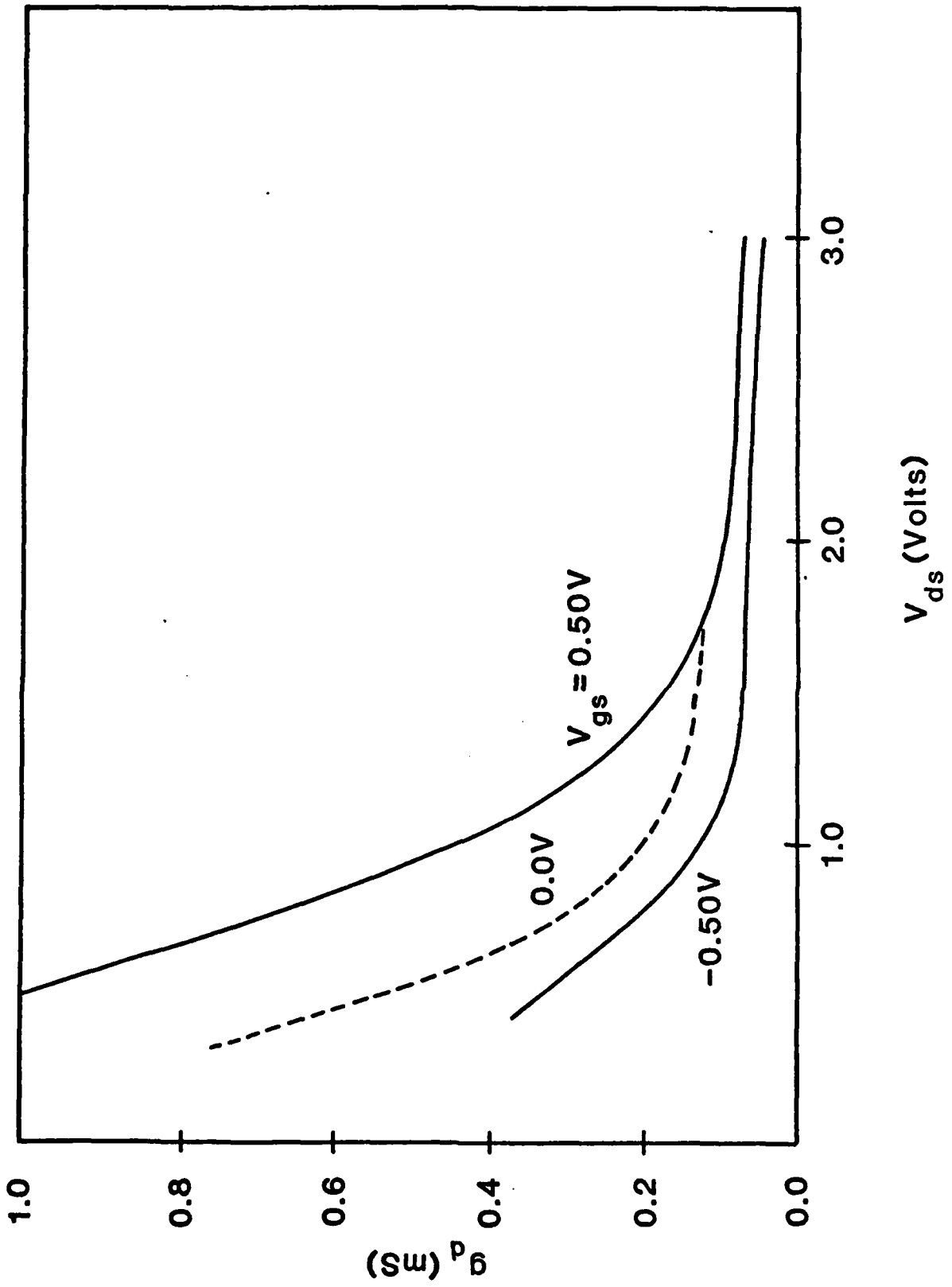


Figure 2.46 Calculated small-signal drain conductance for Figure 2.42 conditions.

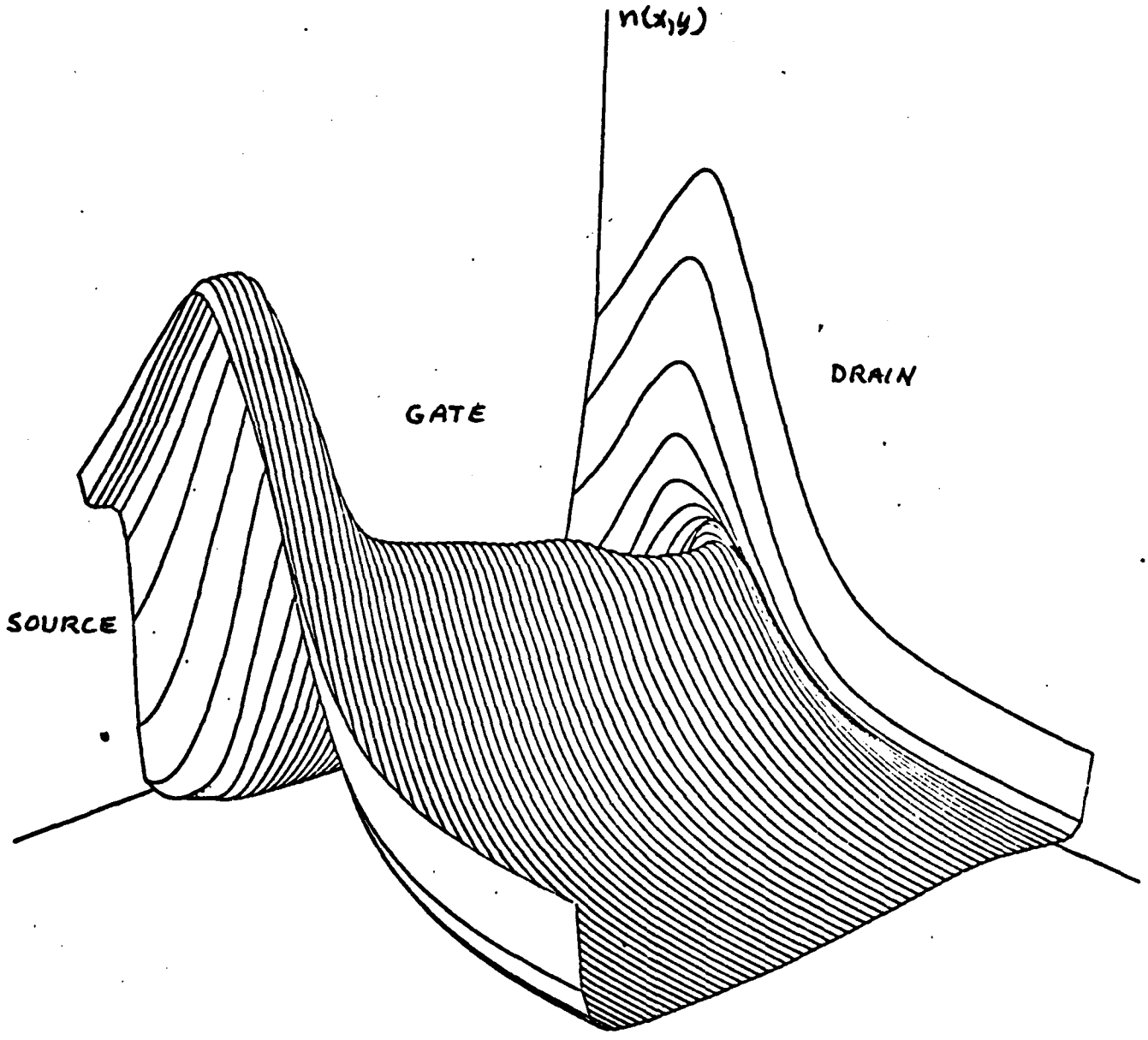


Figure 2.47 Electron density for a type III device with reduced gate-source and gate-drain spacings.

capacitance curves for a positive gate bias of 0.5 volts shows in all cases an anomalously large capacitance at low-drain voltages where the calculated values exceed the values for the reverse-biased gate cases. The physical origin of this anomalously large capacitance is not known at this time. Finally, the drain conductance shows a decreasing value with increasing drain voltage and gate reverse bias as expected.

While there are small differences in magnitudes of the small-signal parameters between the two devices and the different velocity-field relationships, the calculations are remarkably similar in general features. The major features of the calculations appear to be in good agreement with experimental devices fabricated at Rockwell. The small-signal parameters are related to $f_T$ values in the next section.

## 2.8 Varying of Source-Gate and Gate-Drain Spacing

In order to assess the effects of various source-gate and gate-drain spacings on the MESFET characteristics, calculations were made for several devices with a spacing of 0.25 μm instead of the usual 0.5 μm while retaining the 1 μm gate length. This was observed to produce only small changes in the calculated device characteristics. The most significant change in the internal properties can be seen in the free-carrier density profile of Figure 2.47. As can be seen here, the depletion region at the drain end of the gate now extends all the way to the drain contact.

A comparison of the small-signal parameters of the 0.25 μm spacing with the standard 0.5 μm device is shown in Figures 2.48-2.51, for operation at zero gate bias and for the type III doping profile. The major differences in the small-signal parameters are in $g_m$ and in $C_{gd}$. The transcoductance is larger for the 0.25 μm spacing because of the smaller voltage drop between source and active gate region. The gate-to-drain capacitance shows a

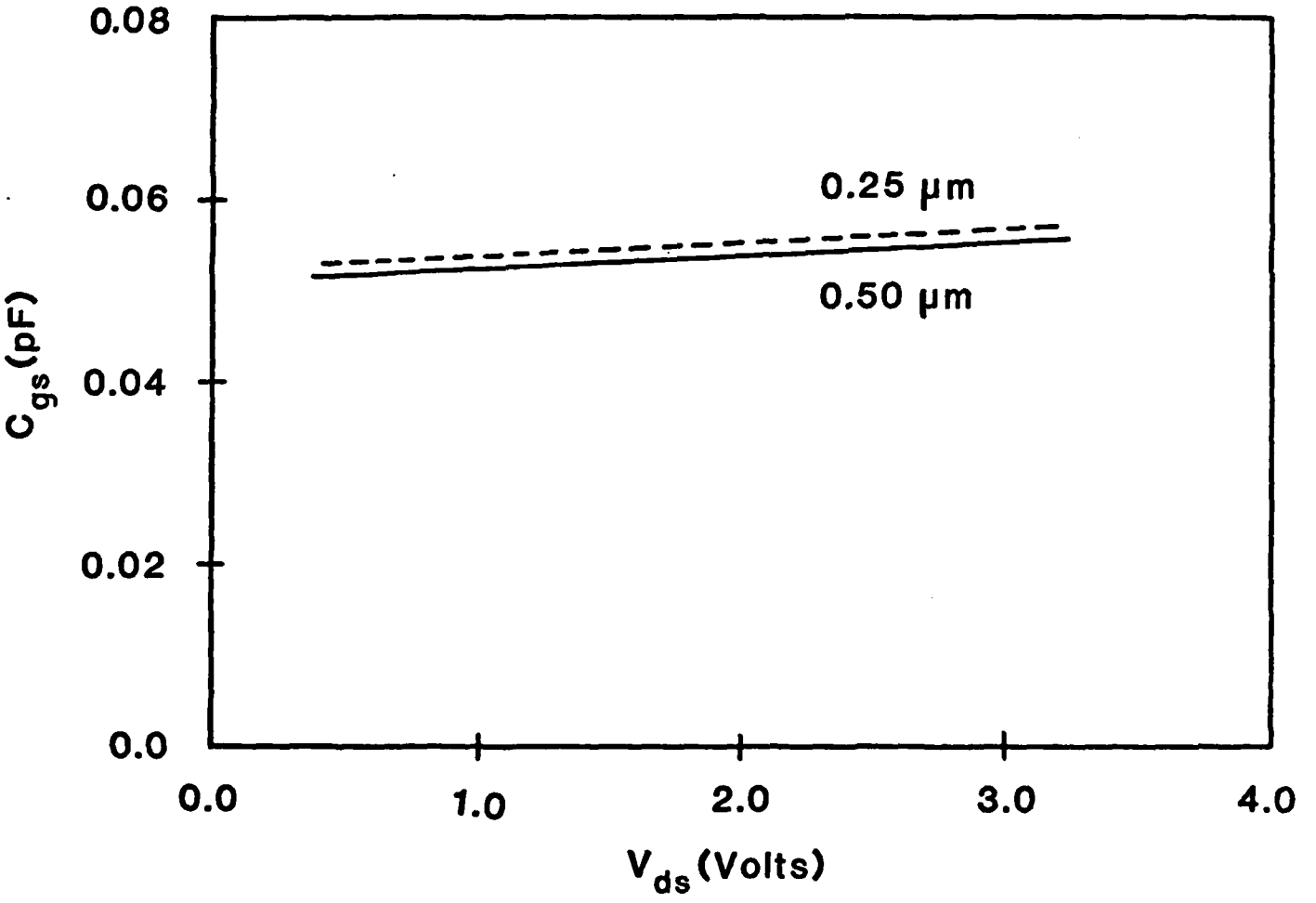


Figure 2.48 Comparison of gate-to-source capacitance for reduced spacing device and standard device at $V_{gs}$ = 0V.

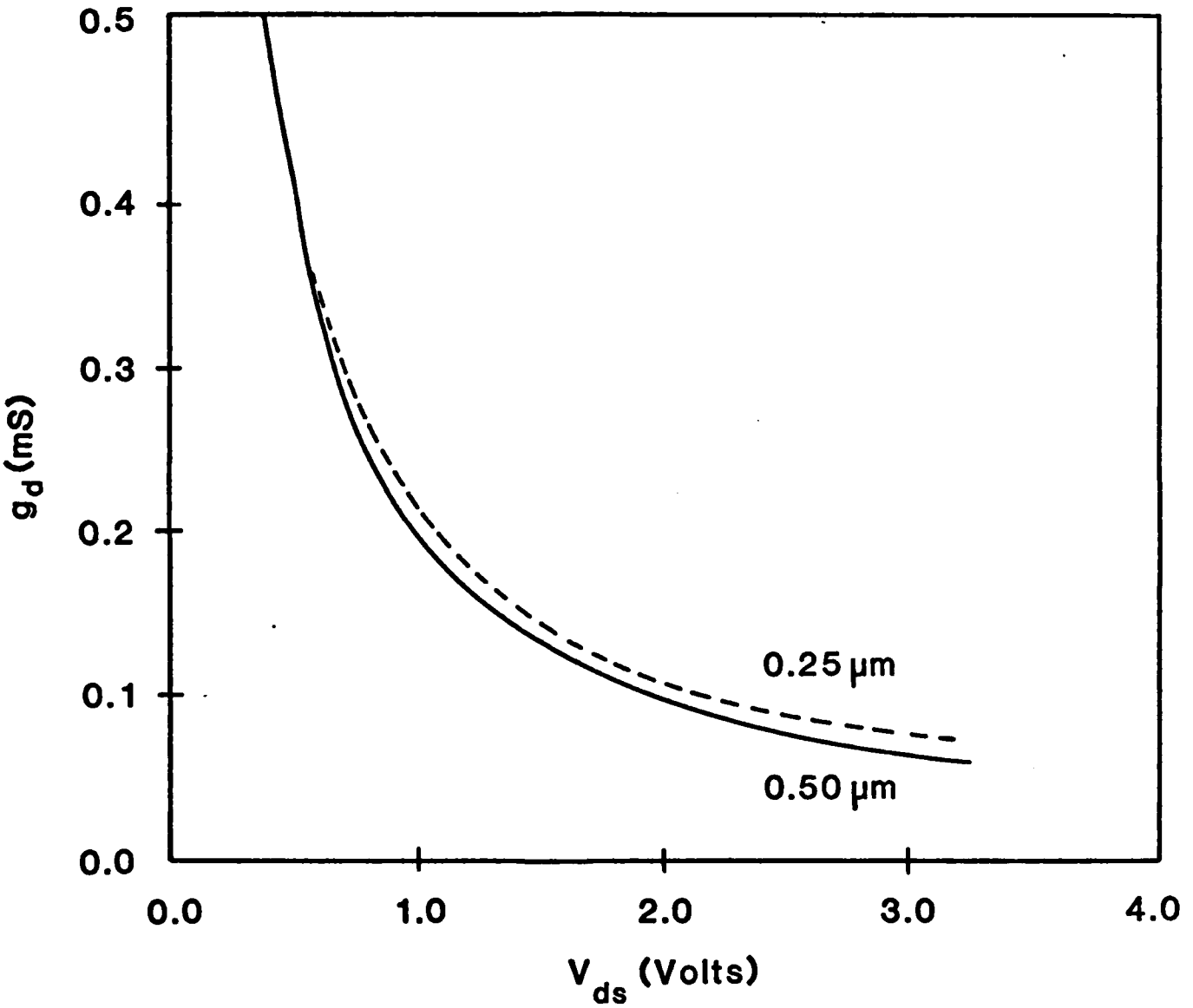


Figure 2.49 Comparison of small-signal drain conductance for reduced spacing device and standard device at $V_{gs}$ = 0V.

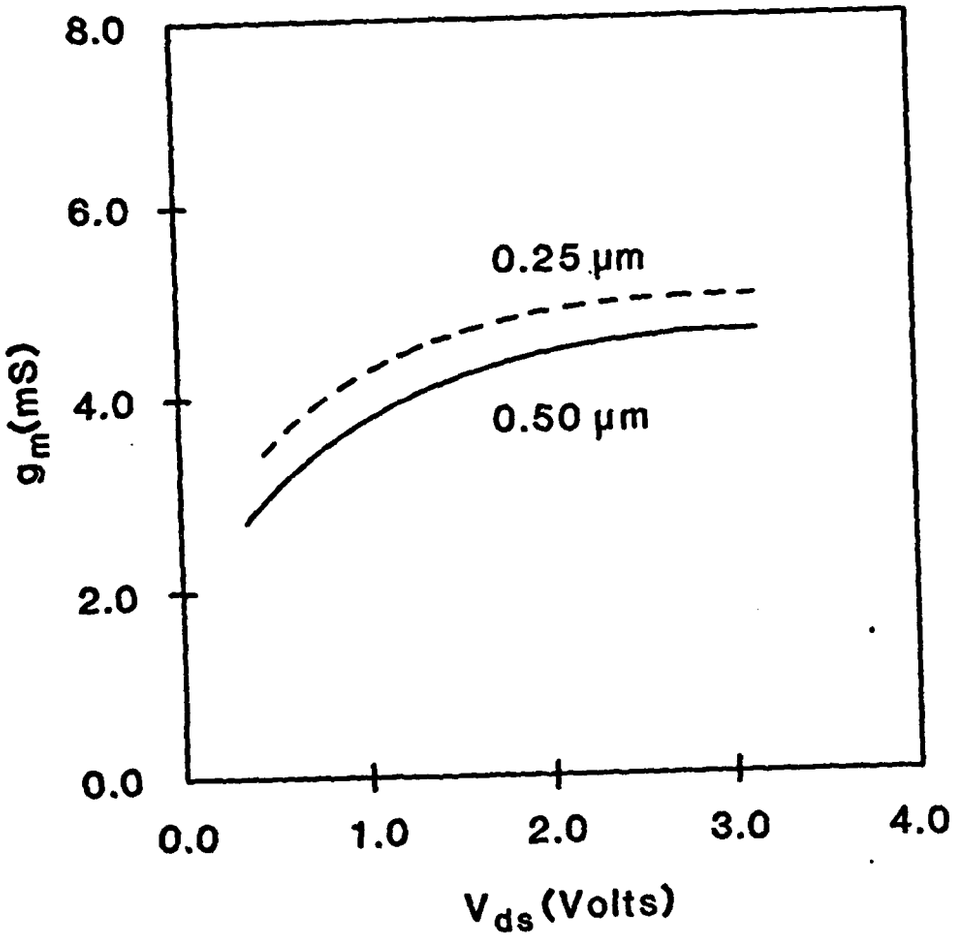


Figure 2.50 Comparison of small-signal transconductance for reduced spacing device and standard device at $V_{gs}$ = 0V.

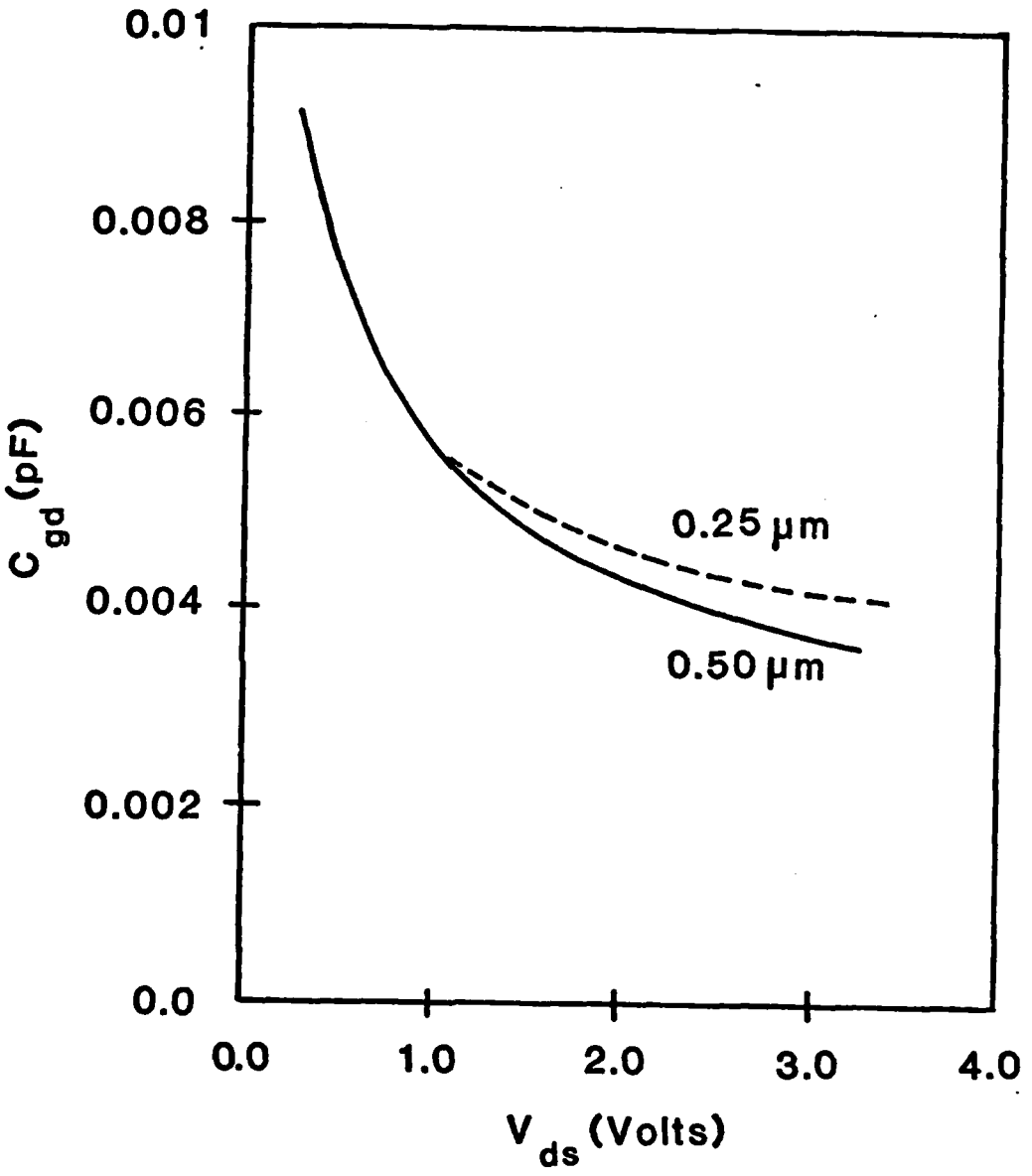


Figure 2.51 Comparison of gate-to-drain capacitance for reduced spacing device and standard device at $V_{gs}$ = 0V.

saturation effect at large drain voltages where the depletion layer extends completely to the drain contact.

A comparison of the small-signal parameters is contained in Tables 2.1-2.3 for two doping profiles and two different velocity-field models. Tables 2.1 and 2.2 are for type I and III profiles with a varying low-field mobility while Table 2.3 is for a type III profile with traps and a constant low-field mobility. Reducing the gate-source and gate-drain spacing is seen to increase the $f_T$ values by 4.6 - 7.6%. The actual calculated $f_T$ values are seen to range from 10.6 to 13.3 GHz for the 0.5 μm devices, to 11.0 to 14.1 GHz for the 0.25 μm devices. Thus it is seen that reducing the gate-source spacing is useful in increasing $f_T$ with most of the increase due to an increase in the transconductance $g_m$.

## 2.9 Scaled MESFET Calculations

The performance of GaAs MESFET devices scaled to smaller dimensions is of interest from both a theoretical and experimental view. To explore a scaled device, calculations were made for an implanted device for which the physical dimensions were reduced by a factor of 5 from the standard device discussed so far. This means that the gate length was 0.2 μm while the gate-source and gate-drain spacing was 0.1 μm. In order to keep the gate depletion region from extending to the source and drain contacts, it is necessary to increase the doping density. Ideal scaling theory would take $N \alpha f^2$ where f is the scaling factor. Thus the doping profile was taken to be that of a type III profile increased by a factor of 25. A more complete description of the device and doping profile is contained in the section on the two-dimensional Monte Carlo calculations.

Calculated internal free-electron density at a drain voltage of 2.5 volts and a gate voltage of 0 is shown in Figure 2.52. This can be compared with

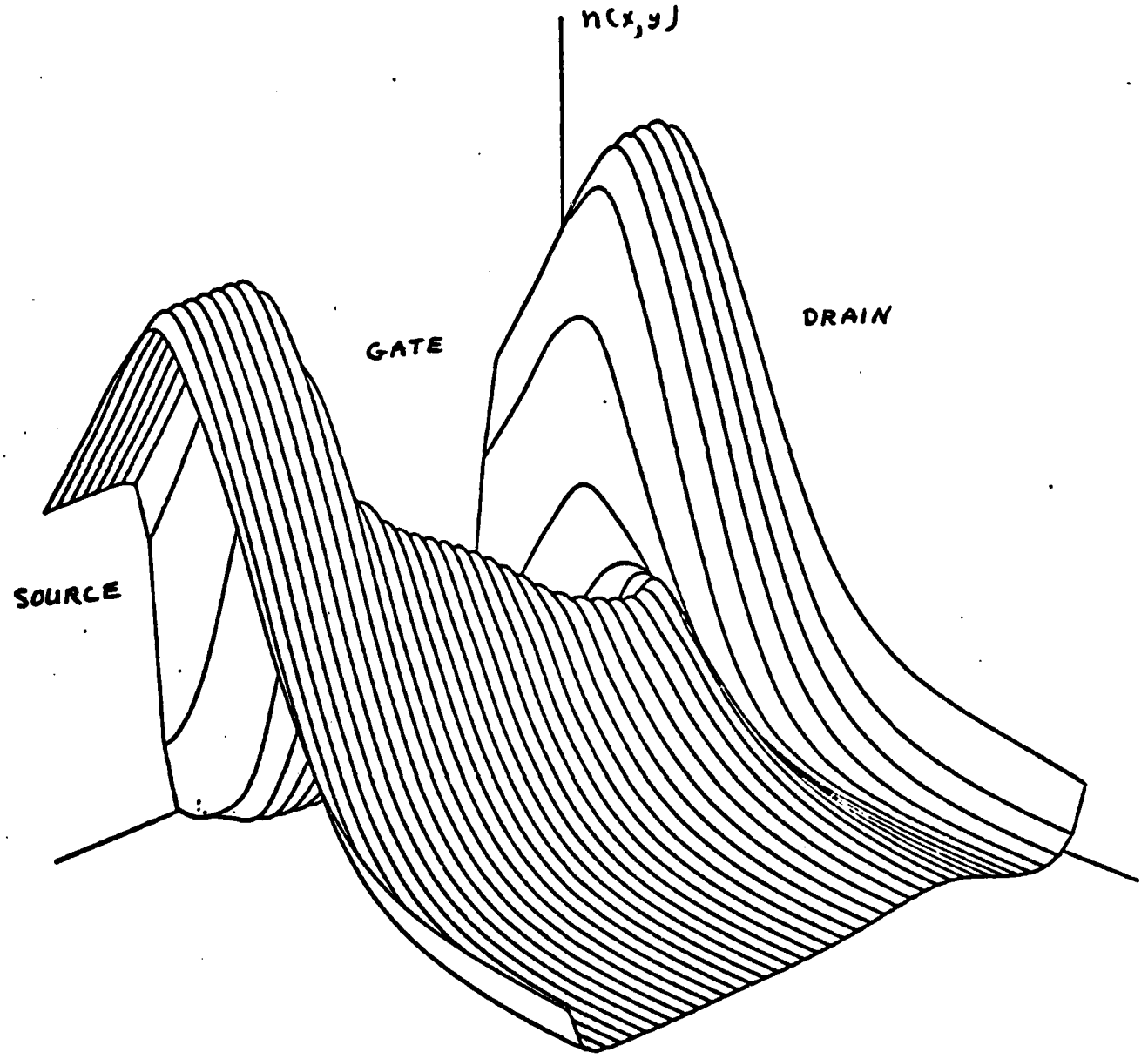


Figure 2.52 Electron density for a scaled MESFET with a gate length of 0.2 μm.

Figure 2.14 for the standard device. As can be seen, the carrier-density profiles are very similar. However, it should be noted that the dimensions are a factor of 5 smaller in Figure 2.52 and the carrier densities a factor of 25 larger. Figure 2.52 illustrates that the scaling theory applies to a good approximation to these calculations.

The I-V characteristics of the scaled devices are shown in Figure 2.53. Again the characteristics are very similar to the non-scaled device except for the larger values of drain current. In fact, the drain current has been increased by about a factor of 5 as first-order device models would indicate. It should be noted that with a peak doping density of about $3 \times 10^{18}/cm^3$, the gate-drain breakdown voltage would be about 3 volts and consequently the large voltages (up to 4 volts) in Figure 2.53 are somewhat unrealistic. Breakdown voltage obviously does not scale with the ideal scale factor and represents a limit on how far the ideal scaling theory can be pushed.

The calculated small-signal parameters for the scaled device at $V_{ds} = 2.5$ volts, $V_{gs} = 0.0$ volts are

$$C_{gs} = 0.041 \text{ pf} \qquad C_{gd} = 0.0045 \text{ pf}$$

$$g_m = 15.76 \text{ mA/V} \qquad g_d = 0.58 \text{ mA/V}$$

From these values an $f_T$ of 61.0 GHz is calculated. This is a considerably higher value of $f_T$ than has ever been experimentally obtained with GaAs MESFET devices, and it indicates that there is a considerable range for improvement in future devices. The capacitance values given above are comparable to those of an unscaled device. This is to be expected, since the gate area decreases by f while the depletion layer width decreases by the same factor f keeping the capacitance values relatively constant. The gain in $f_T$ comes from the enhanced value of $g_m$ in the scaled device.

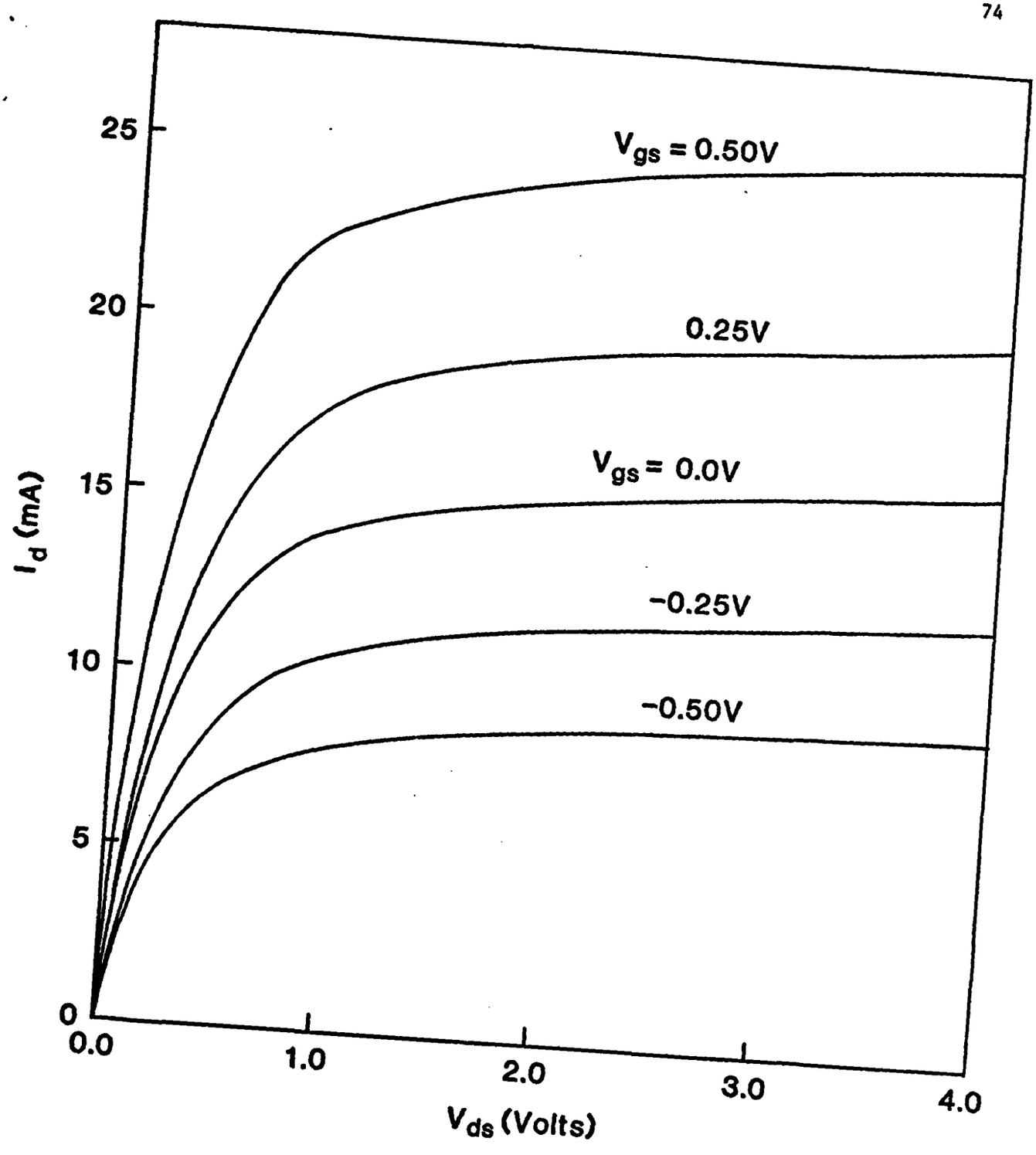


Figure 2.53 Calculated terminal $I_d$-$V_{ds}$ characteristics for a scaled MESFET with a gate length of 0.2 μm.

The results of a Monte Carlo simulation of the same MESFET (discussed elsewhere in this report) indicate that the present calculations underestimate the current and consequently transconductance of such short-channel devices by a factor of about 3. This would indicate that the potential $f_T$ for a 0.2 μm gate GaAs MESFET is about 120 GHz. Achieving performance of 100 Ghz or above will remain a goal of GaAs MESFET development for several years but appears from a theoretical viewpoint to be an achievable goal.

## 2.10 Conclusions

This section has presented a discussion of the two-dimensional model used in this work for studying ion implanted GaAs MESFET devices along with results obtained from this numerical modeling. The analysis has been based on a static velocity-field relationship and does not include high-field velocity overshoot effects which should not be too important for 1 μm gate length devices. The results indicate that the major features of the ion implanted MESFETs appear to be reasonably well predicted by such a conventional two-dimensional analysis.

| $V_{DS}$ = 2.5<br>$V_D$ = 0 | 0.5 μm spacing | 0.25 μm spacing | Change<br>% |
|---|---|---|---|
| $I_{DS}$ | 1.7453 mA | 1.7973 mA | 2.97% |
| $g_m$ | 2.51 mmho | 2.659 mmho | 5.94% |
| $C_{gs}$ | 0.0380121 pf | 0.038503 pf | 1.29% |
| $C_{gd}$ | 0.0332 mmho | 0.0039677 pf | 14.88% |
| $g_d$ | 0.0332 mmho | 0.084 mmho | 15.6% |
| $f_T = \frac{g_m}{2\pi C_{gs}}$ | 10.509 Ghz | 10.9919 GHz | 4.64% |

Table 2.1 Comparison of small-signal parameters of reduced contact spacing device and standard device using a doping-dependent, low-field mobility, zero trap density, and a type I doping profile ($V_{ds}$ = 2.5V, $V_{gs}$ = 0.0V).

| $V_{DS}$ = 2.5V<br>$V_{gs}$ = 0.0 | 0.5 μm spacing | 0.25 μm spacing | Change<br>% |
|---|---|---|---|
| $I_{DS}$ | 3.1771 mA | 3.24082 mA | 2.2% |
| $g_m$ | 3.323 mmho | 3.706 mmho | 11.5% |
| $C_{gs}$ | 0.0477228 pf | 0.049499 pf | 3.72% |
| $C_{gd}$ | 0.00425 pf | 0.0046081 pf | 8.4% |
| $g_d$ | 0.07 mmho | 0.0779 mmho | 10% |
| $f_T = \frac{g_m}{2\pi C_{gs}}$ | 11.08216 Ghz | 11.92779 GHz | 7.63% |

Table 2.2 Comparison of small-signal parameters of reduced contact spacing device and standard device using a doping-dependent, low-field mobility, zero trap density, and a type II doping profile ($V_{ds}$ = 2.5V, $V_{gs}$ = 0.0V).

| $V_{DS}$ = 2.5<br>$V_{gs}$ = 0.0 | 0.5 μm spacing | 0.25 μm spacing | Change<br>% |
|---|---|---|---|
| $I_{DS}$ | 2.86151 mA | 2.92670 mA | 2.27% |
| $g_m$ | 4.578 mmho | 5.029 mmho | 9.85% |
| $C_{gs}$ | 0.05495 pf | 0.05658 pf | 2.96% |
| $C_{gd}$ | 0.0040659 pf | 0.004441 pf | 9.22% |
| $g_d$ | 0.0793 mmho | 0.0869 mmho | 9.58 |
| $f_T$ | 13.259 Ghz | 14.14 GHz | 6.68% |

Table 2.3 Comparison of small-signal parameters of reduced contact spacing device and standard device using a constant, low-field mobility, (8000 $cm^2/V \cdot sec$), a trap density of $3x10^{15}/cm^3$ and a type III doping profile ($V_{ds}$ = 2.5V, $V_{gs}$ = 0.0V).

# 3.0 ANALYTICAL STUDIES

## 3.1 One-Dimensional Model

Two different analytical one-dimensional models have been used to examine important properties of GaAs MESFETs. One model allows only homogeneously doped channels to be studied. This model has been used to study the effects various material properties have on device performance figure such as available gain and minimum noise figure. The other model allows arbitrary doping profiles to be studied. Novel features of this model include channel-depth-dependent velocity and mobility expressions and the effects of deep-level trips.

Following the work of Pucel et al. [7] there models assume that the electron transport characteristics can be approximated by a two-piece velocity-field relationship. The two-piece approximation (Figure 3.1) is defined from theoretical velocity-field characteristics determined by Monte Carlo techniques.

For electric fields less than an appropriate saturation field, $E_m$, the electron velocity is described by a linear expression,

$$v = \mu_o E. \tag{3.1}$$

For electric fields above $E_m$ the electrons move at a constant, saturated velocity, $v_m$. Using this information, a small-signal equivalent circuit can be determined and analyzed to obtain RF performance predictions, including power gain and noise figure.

The low-field mobility for materials of interest is obtained directly from Monte-Carlo data. The importance of developing a systematic, well-justified technique for determining $v_m$ has been discussed in earlier work [8] and in this study, such a method has been developed. The method involves numerical determination of the carrier transit time under the gate using an

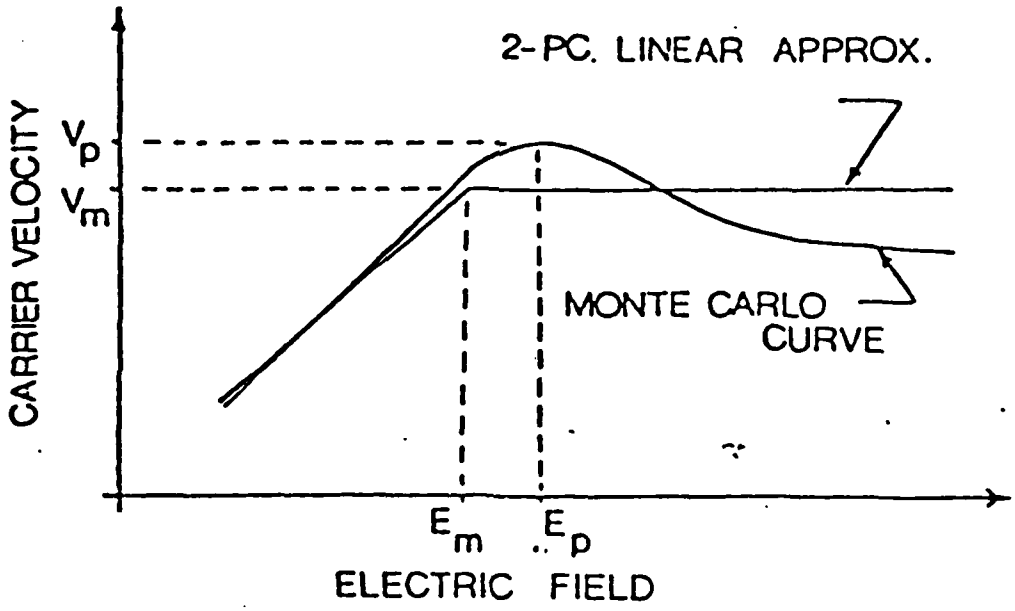


Figure 3.1 Carrier velocity as a function of electric field for GaAs doped to $N_D = 10^{17}$ cm$^{-3}$

exact velocity-field relationship. Then, it is required that the transit time calculated assuming a two-piece approximated velocity-field relationship be equal to the exact analysis. The method yields a $v_m$ for GaAs (doped $N_D = 10^{17}cm^{-3}$) in excellent agreement with the value obtained by Pucel [7].

In the profile model, the effect which deep-level trips have on the velocity-field characteristics is also accounted for as described in another section of this report.

## 3.2 Material Parameter Study

The homogeneous model was used to study the effects of low-field mobility and peak velocity on minimum noise figure and the associated gain of the device. This was done by keeping either $v_m$, or $\mu_o$ constant while varying the other in the model. The results shown in Figure 3.2 indicate that for a fixed value of $v_m$, increasing $\mu_o$ value has been reached. The effect of changing peak velocity, $v_m$, with the mobility constant (Figure 3.3), however, indicates that no such point of diminishing returns exists in the device gain.

This information is expected to be valuable in determining the semiconductor materials which are most likely to result in optimum-performance of devices for particular applications. Table 3.1 gives values for low-field mobility and peak velocity of several materials of current interest.

The effect of lower mobility and velocity on device performance as a result of traps due to ion implantation can also be understood from this information.

## 3.3 Profile Study

The profile dependent characteristics of ion-implanted GaAs MESFETs were studied through the use of a model which considers channel-depth-dependent carrier velocity and mobility and the effects of deep-level traps.

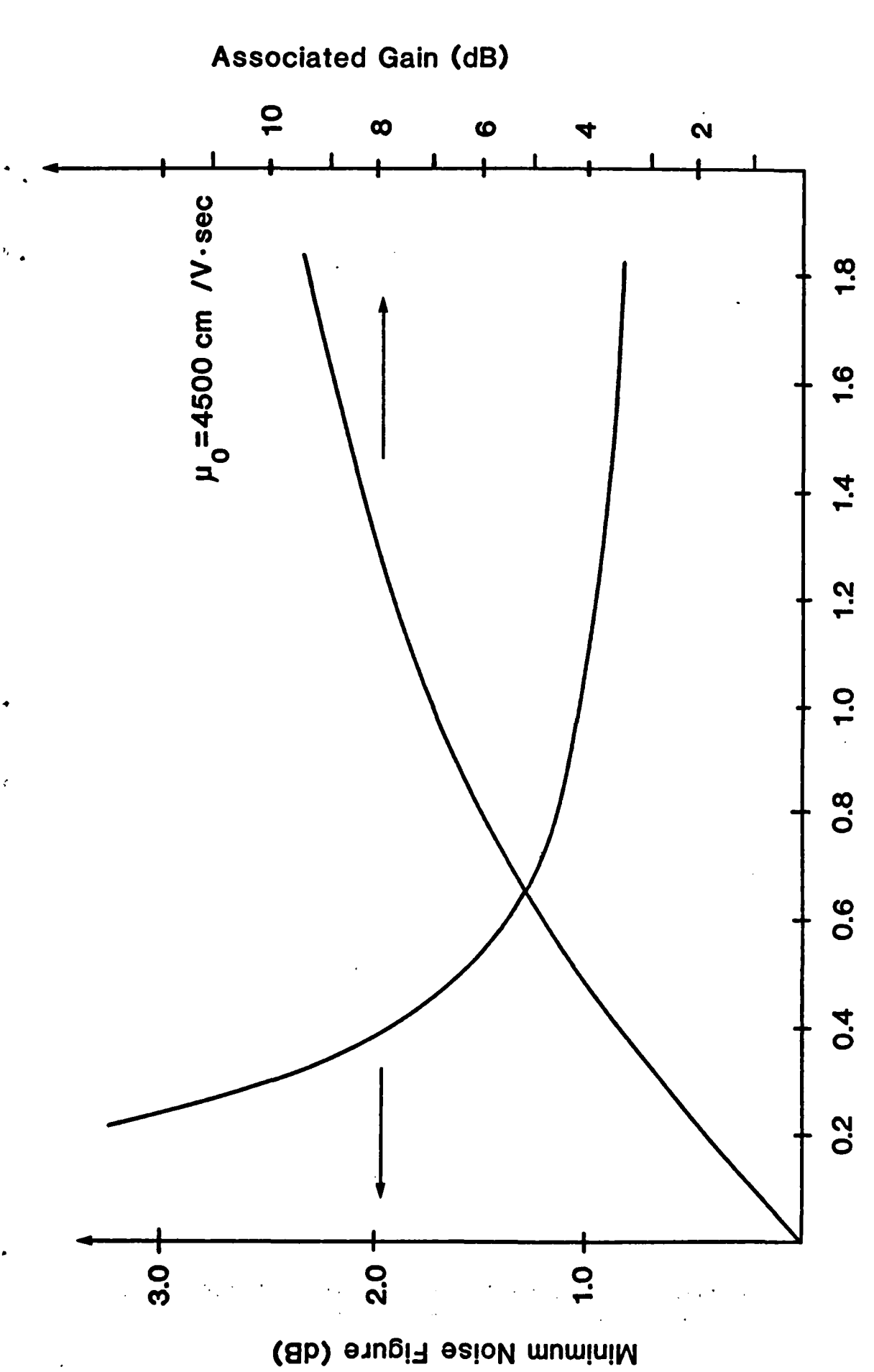


Figure 3.2 Predicted minimum noise figure and associated gain at 10 GHz as a function of low-field mobility.

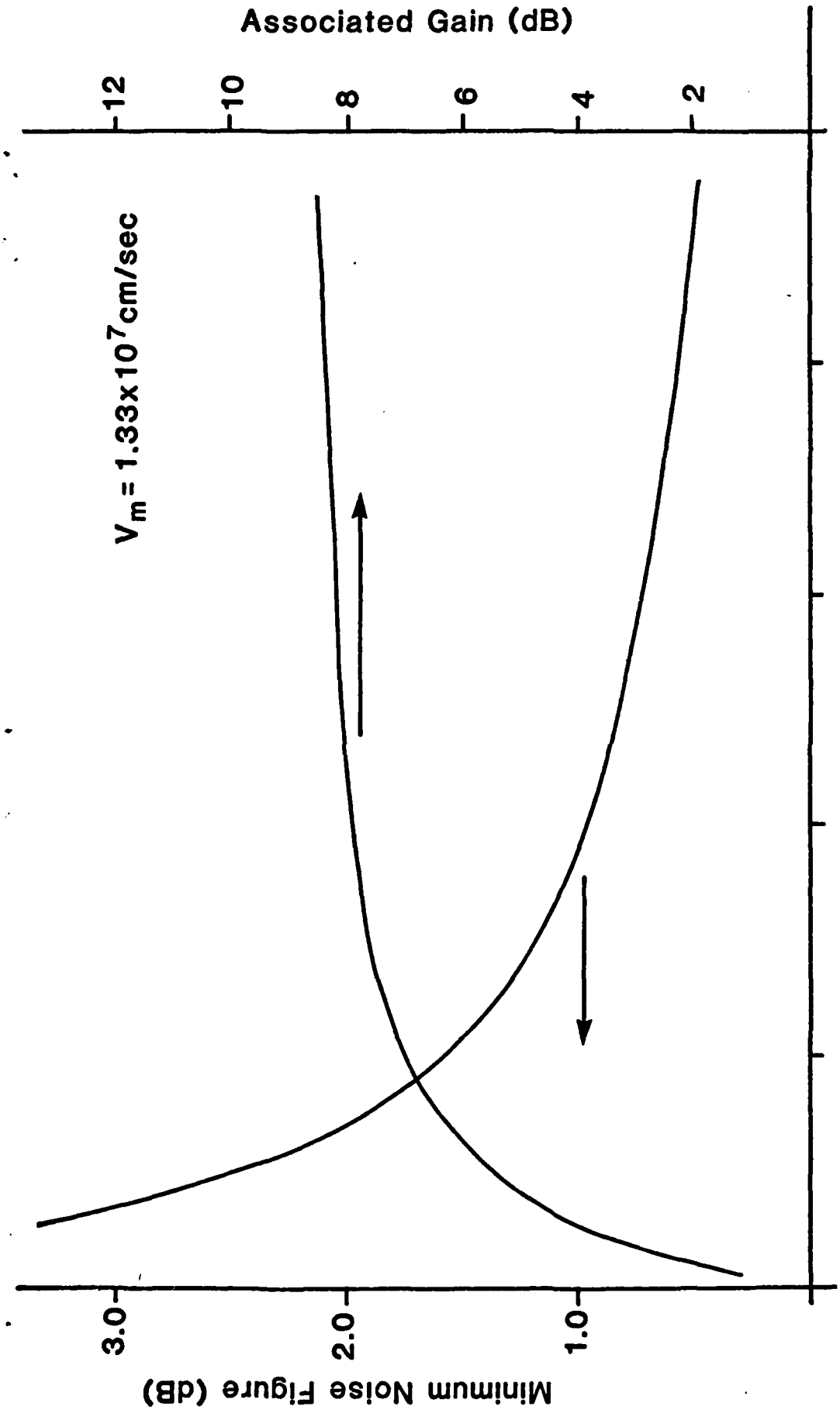


Figure 3.3 Predicted minimum noise figure and associated gain at 10 GHz as a function of maximum velocity.

| Material | $_{o}$(cm$_2$/v•sec) | vm($10^7$cm/sec) |
|---|---|---|
| Si | 500 | 1.00 |
| GaAs | 4660 | 1.30 |
| InP | 3490 | 1.84 |
| $Ga_{.47}In_{.53}As$ | 8900 | 1.31 |
| $Al_{.47}In_{.53}As$ | 5050 | 0.99 |

Table 3.1 Low-field mobility, $\mu_o$, and saturation velocity, $v_m$, for several materials. Values are appropriate for 1 μm devices doped to a level $N_D = 10^{17}cm^{-3}$.

Figure 3.4 shows the computed peak-velocity and low-field mobility versus channel depth for one device which was characterized. The I-V characteristics predicted by the model for this device are in excellent agreement with actual measured I-V characteristics as shown in Figure 3.5.

Once the validity of the model was verified a profile study was begun. From LSS theory for Silicon implanted Gatts [9], shallow-level donor concentrations were determined for various implantation energies and fluences. Background trap concentrations were estimated from profiling studies of actual devices using the technique outlined in other sections of this report. The actual free-carrier concentration could then be determined from device equations. This information was then used in the profile model to predict device performance. The results of the 70, 100, and 140 KeV implant study are tabulated in Table 3.2 Note that the 140 KeV profile is assumed to have been etched back 0.05 μm from the surface.

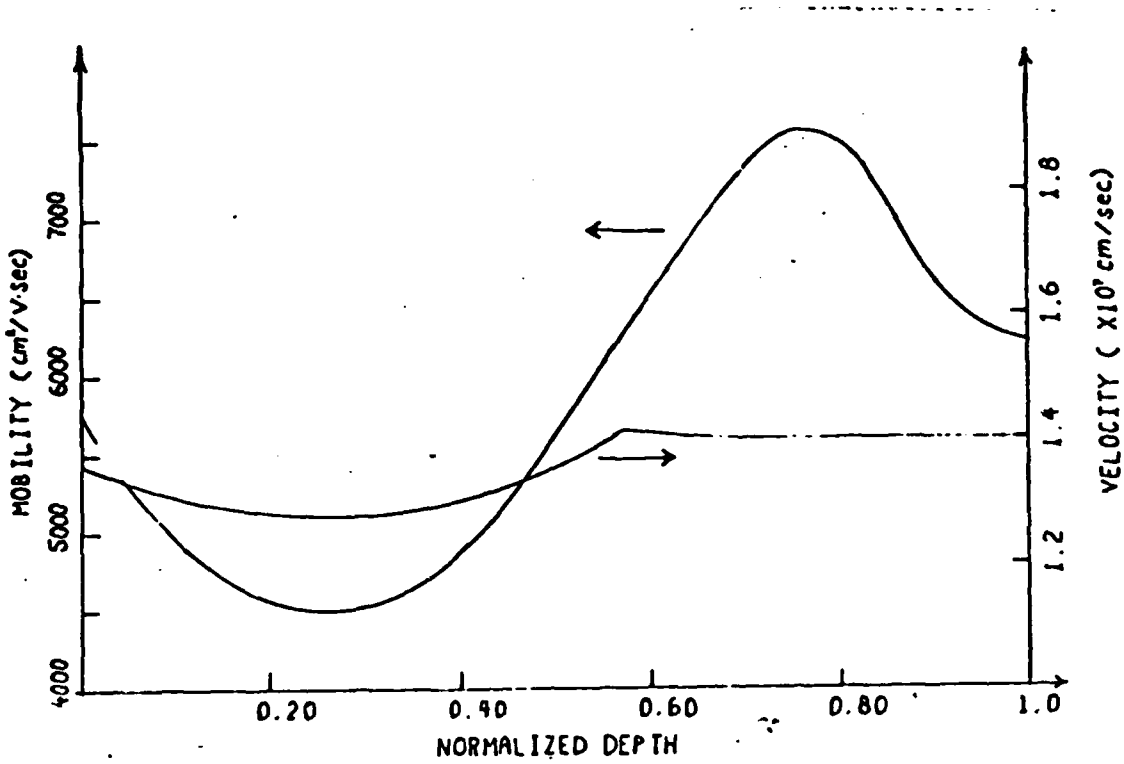


Figure 3.4 Electron saturation velocity and low-field mobility versus channel depth.

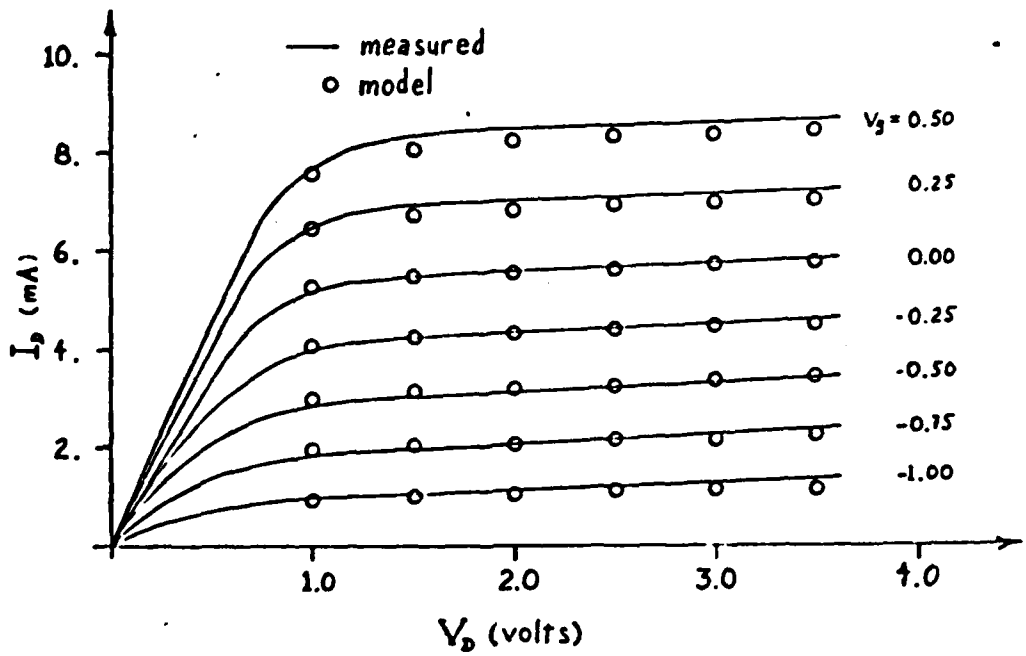


Figure 3.5 Comparison between measured and calculated I-V characteristics for an ion-implanted GaAs MESFET.

| Implant Energy (KeV) | Doping Peak ($cm^{-3}$) | $I_{DSS}$ (mA) | $C_{gso}$ (pF) | $G_{mo}$(mv) | G@10GHz (dB) | $I_D$ (mA) | $C_{gs}$(pF) | $G_m$(mv) | $G_a$@10GHz (dB) |
|---|---|---|---|---|---|---|---|---|---|
| 70 | $1.95x10^{17}$ | 26.8 | 0.414 | 44.4 | 8.61 | 26.8 | 0.414 | 44.4 | 8.61 |
| 70 | $3.90x10^{17}$ | 93.0 | 0.519 | 56.4 | 8.61 | 32.9 | 0.422 | 38.4 | 7.96 |
| 100 | $2.22x10^{17}$ | 79.8 | 0.410 | 44.1 | 8.43 | 28.6 | 0.317 | 29.6 | 7.68 |
| 100 | $3.70x10^{17}$ | 154.0 | 0.459 | 49.2 | 8.28 | 27.5 | 0.343 | 26.3 | 7.00 |
| 140* | $1.74x10^{17}$ | 60.9 | 0.392 | 42.4 | 8.45 | 28.9 | 0.310 | 30.6 | 7.86 |
| 140* | $3.50x10^{17}$ | 158.0 | 0.472 | 50.9 | 8.32 | 31.0 | 0.320 | 25.6 | 7.06 |

*Surface lapped 0.05 μm

Table 2. Predicted device performance parameters as a function of implant energy and fluence.

# 4.0 DEVICE CHARACTERIZATION

An attractive technology for the development of GaAs integrated circuits for microwave, millimeter-wave and high-speed logic applications involves ion-implantation of conductive regions directly into high-resistivity, bulk grown semiconductor substrates [10,11]. The performance of FET's fabricated in this way depends greatly on carrier concentrations and velocity-field characteristics as a function of depth into the active device layers. The characterization of these quantities, however, is complicated by the presence of impurity compensation in the form of chromium or other deep-level traps within the channel. In this section, we present a method of determining free-carrier, shallow-level donor, deep-level trap, and low-field mobility profiles from differential capacitance and conductance DLTS measurements.

## 4.1 General Device Equations

Figure 4.1 shows typical free-carrier, background donor, and deep-level trap profiles for a sample of ion-implanted semiconductor material. Deep-level trap centers and free-carrier diffusion from highly-doped to more-lowly doped regions will cause the free-carrier profile to differ from that of the ionized donors. Our studies show that as much as an order of magnitude difference can exist between these two profiles for ion-implanted materials typically used in the fabrication of GaAs MESFET's.

The relationship between the free-carrier, donor, and trap profiles can be obtained by combining the current density equation for electrons with Poisson's equation in the direction into the channel. The appropriate form for the current density equation is

$$J_n = 0 = q\{\mu_o\, n(x)\, E(x) + D_n \frac{dn}{dx}\} \qquad (4.1)$$

where

$q$ = electronic charge,

$\mu_o$ = the electron mobility,

$n(x)$ = free-carrier concentration,

$E(x)$ = electric field within the channel,

$D_n$ = electron diffusion coefficient,

and

$J_n$ = electron current density in the x-direction.

While Poisson's equation for this case is written as:

$$\frac{dE}{dx} = \frac{q}{\varepsilon_R \varepsilon_o} \{N_D(x) - n(x) - N_T(x)\} \tag{4.2}$$

where

$\varepsilon_R$ = relative dielectric constant of the material,

$\varepsilon_o$ = permittivity of free-space,

$N_D(x)$ = shallow-level ionized donor concentration,

and

$N_T(x)$ = deep-level donor concentration.

Equations (4.1) and (4.2) can be combined to express one of the profiles in terms of the other two. In this case, the background donor concentration can be written as:

$$N_D(x) = n(x) + N_T(x) - \frac{kT}{q^2} \frac{d}{dx} \left(\frac{1}{n(x)} \frac{dn}{dx}\right) \tag{4.3}$$

where the Einstein relation has been used and where

$k$ = Boltzman's constant

and

$T$ = material temperature.

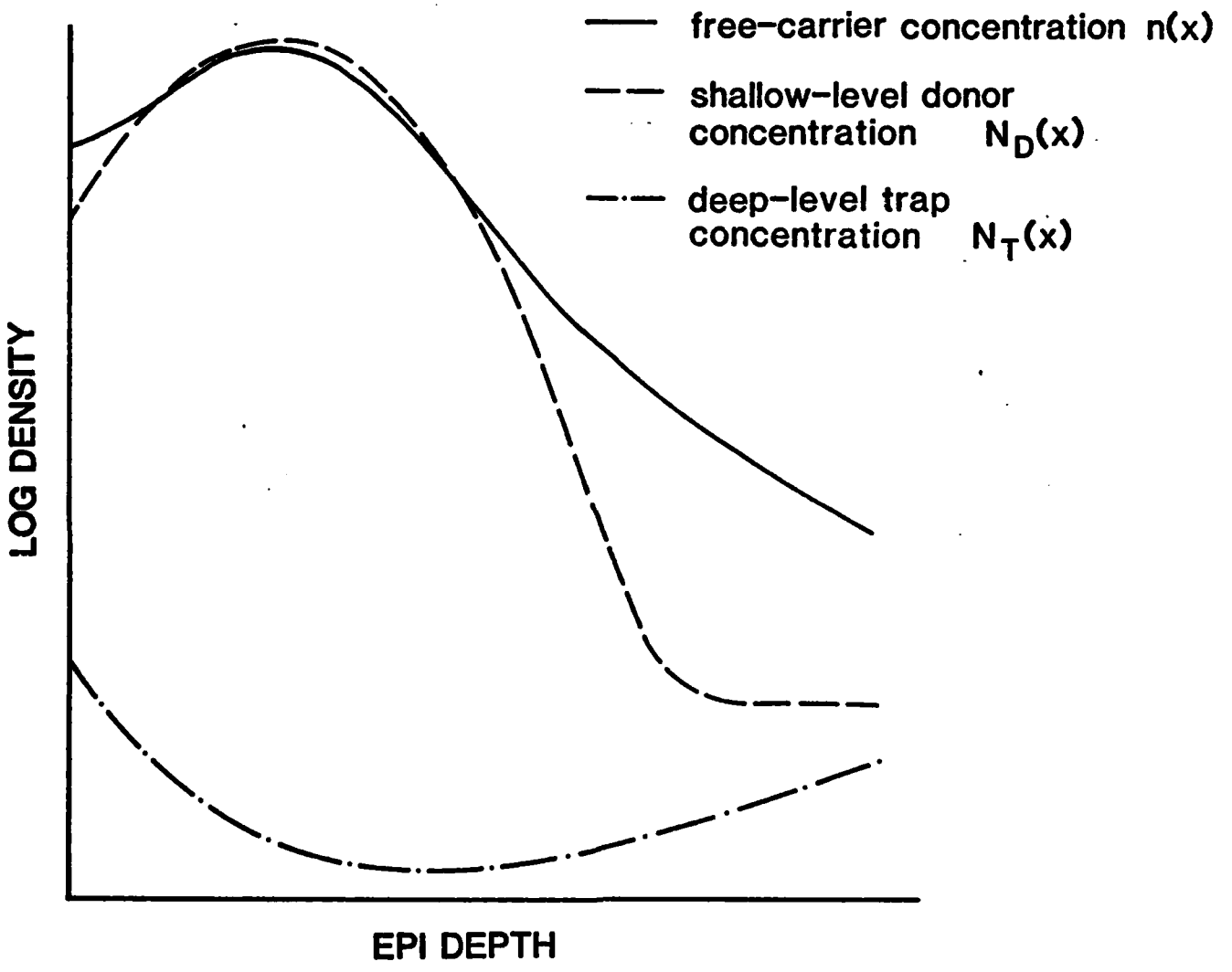


Figure 4.1 Typical concentration profiles for ion-implanted material.

The relationship (4.3) is identical to that derived by Kennedy and O'Brien [12] if trap centers were not present. The last term in (4.3) represents a local charge imbalance which will, in general, exist within the material. Thus, a potential gradient will be created within the semiconductor even without contact or bias disturbance. The importance of this local steady-state charge imbalance in terms of the device measurements will be discussed in more detail in the following sections.

## 4.2 Differential Capacitance Measurement (C-V)

The differential capacitance (C-V) measurement can be considered as a parallel-plate capacitor problem and examined by analyzing the structure shown in Figure 4.2. The capacitance, C, is normally measured with a small oscillating voltage, $\Delta V$, superimposed over a fixed applied bias, $V_a$,. The oscillating voltage induces a current due to an incremental charge, $\Delta Q$, being alternately covered and uncovered near the depletion region edge, $x_w$. Kennedy et al. [13] have shown that in the absence of deep states, traditional C-V analysis estimates the free-carrier concentration rather than the background donor density. Since only the free-carriers can participate in the differential change in the device charge $\Delta Q$, it is the free-carrier concentration which is measured.

If deep-level trapping states are present, then the incremental charge, $\Delta Q$, can come not only from free-carriers in the conduction band, but also from electrons trapped in the deep-level sites. The interpretation of C-V data under these conditions is dependent on the relationship between the frequency of the oscillating voltage, $\omega(\Delta V)$, the electron emission rate associated with the deep-energy site, $e_n$, and the rate of change of the dc bias, $\omega(\Delta V_a)$; as well as on the type of trap site present. Both deep-level donors and acceptors modulated at various speeds with respect to e have been examined by

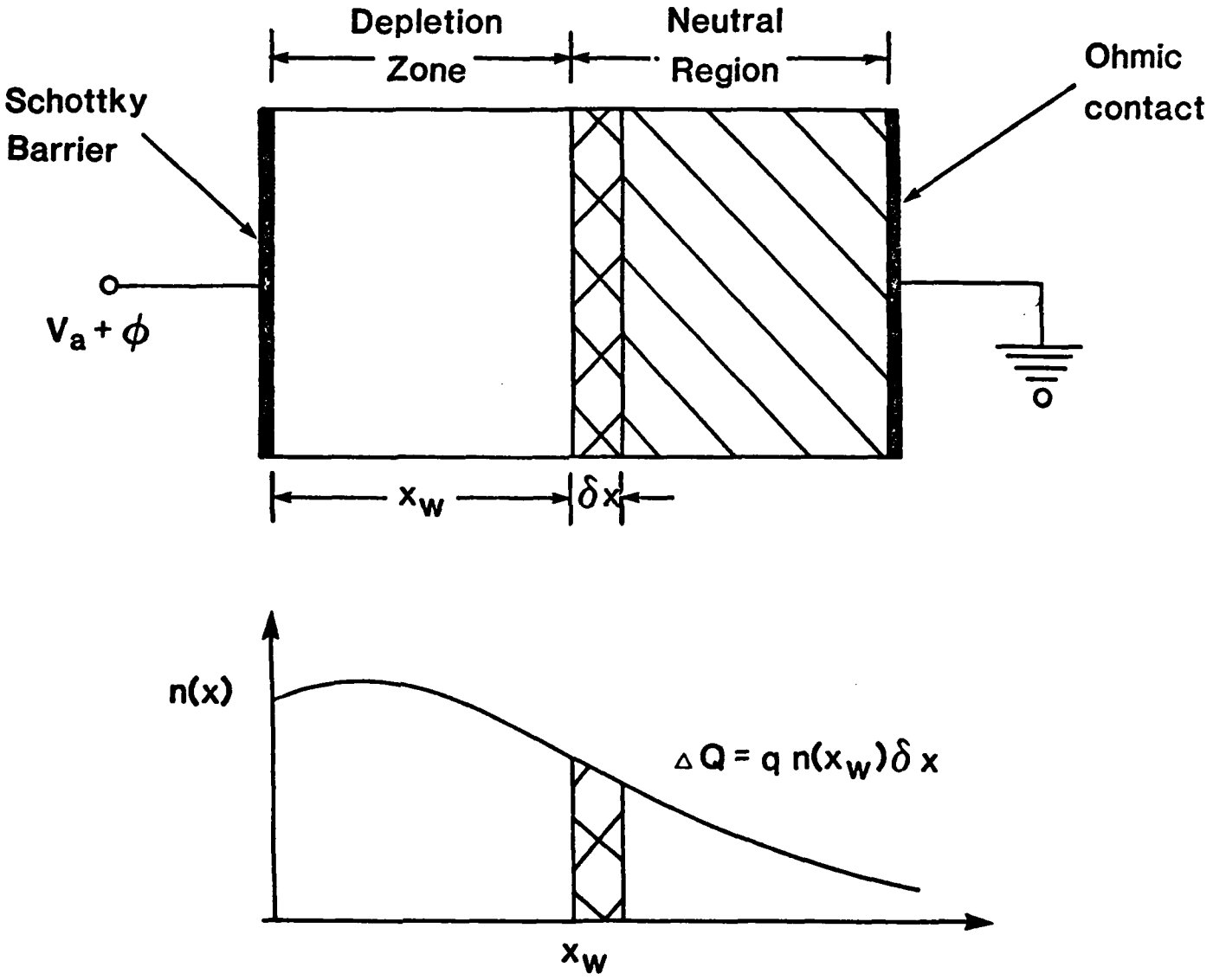


Figure 4.2 Parallel-plate capacitance model of a reverse-biased Schottky contact used to simulate the differential capacitance measurement.

a number of workers [14-16]. For simplicity, however, we will examine only the case where

$$\omega(\Delta V) \gg e_n \gg \omega(\Delta V_a)$$

and only deep-level donors as shown in Figure 4.3. These conditions are chosen since they would commonly hold for C-V measurements on Cr-doped GaAs substrates ion-implanted with n-type dopants.

Kimmerling [16] has shown that the free-carrier concentration under the previously stated assumptions is given by

$$n(x) = n_{C-V}\ (x_\omega) - N_T\ (y_\omega)\ \frac{y_\omega}{x_\omega}\ \frac{\Delta y}{\Delta x}\ , \tag{4.4}$$

where

$$n_{C-V}(x) = -\frac{C^3}{q\,\epsilon_R\,\epsilon_o}\ \left(\frac{dC}{dV}\right)^{-1} \tag{4.5}$$

is the traditional C-V expression and where

$N_T(y_\omega)$ = trap concentration at the point $y_\omega$.

$\Delta y$ = change in the position of the Fermi level cross point $y_\omega$.

and

$\Delta x$ = change in the depletion region extent $x_\omega$.

The Fermi level cross-point $y_\omega$ can be derived from the band bending if the background donor concentration is known. Referring to Figure 4.3a and applying Poisson's equation gives

$$E_f - E_T = \frac{q^2}{\epsilon_R\,\epsilon_o}\ \{\int_{y\omega}^{x\omega}\int_{o}^{x} N_D(z)\ dz\ dx - (x_\omega - y_\omega)\int_{o}^{x\omega} N_D(z)\ dz\} \tag{4.6}$$

Knowledge of the value $(E_f-E_T)$ is also required for equation (4.6) to be used to compute $y_\omega$. Normally, the value $E_C-E_T$ is determined through independent measurement [17-20]. The relation

$$E_C - E_f = kT\ \ln\ (N_C/n(x)) \tag{4.7}$$

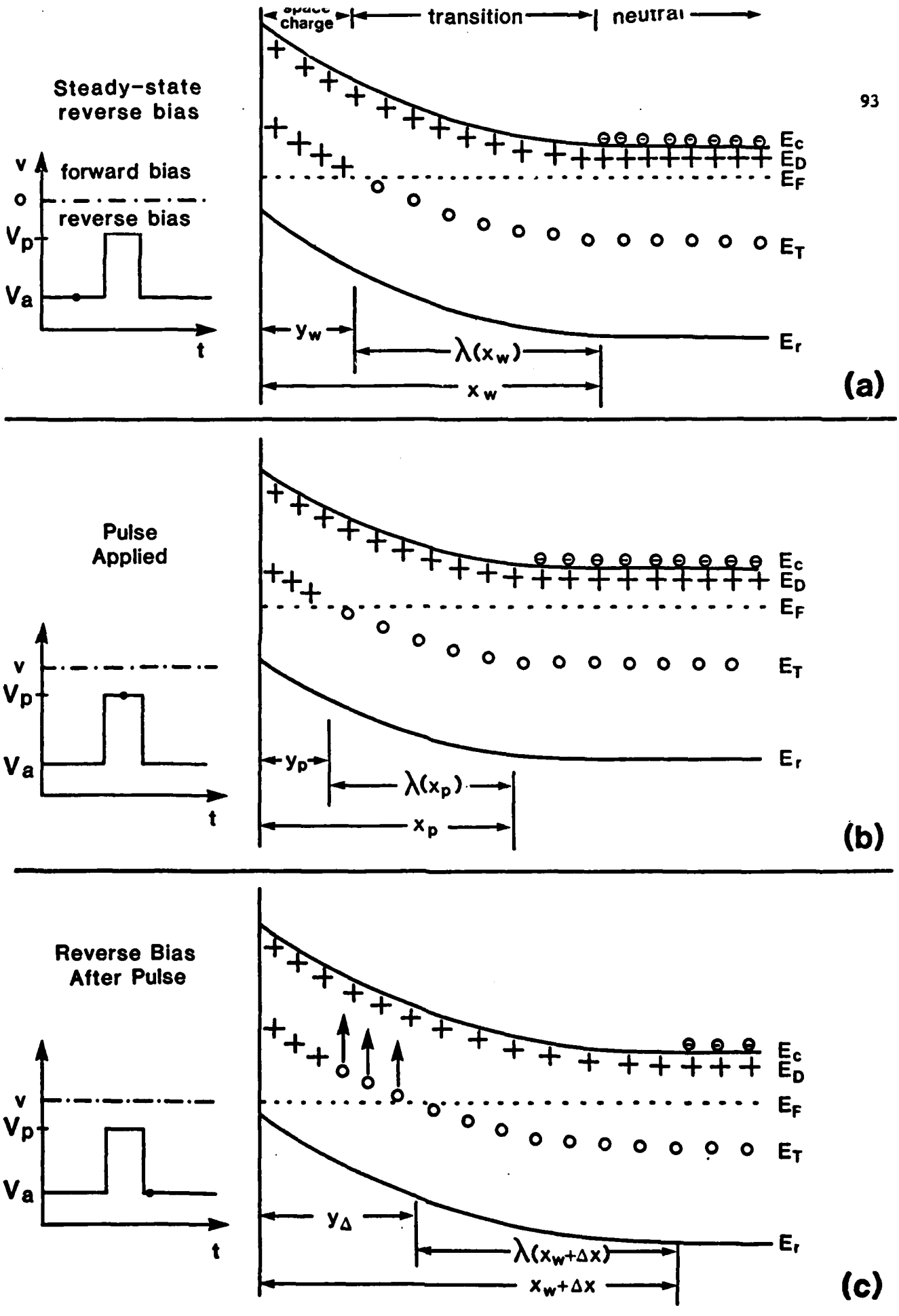


Figure 4.3 Band-diagrams for reverse-biased Schottky structure with one deep trap. a) before forward pulse. b) during pulse. c) immediately following pulse.

where

$N_C$ = conduction band density of states,

is then used with this information to determine $E_f$-$E_T$.

Equations (4.4) and (4.6) can also be written in terms of the quantity $\lambda(x_\omega)$ through the relationship

$$\lambda(x_\omega) = x_\omega - y_\omega \quad . \tag{4.8}$$

When this is done and $\Delta y$ is written as a truncated Taylor's Series in $x_\omega$, equation (4.4) becomes

$$n(x_\omega) = n_{C-V}(x_\omega) - N_T(y_\omega)\frac{[x_\omega-\lambda(x_\omega)][1 - \frac{d\lambda}{dx_\omega}]}{x_\omega} \quad . \tag{4.9}$$

Figure 4.4 shows a profile obtained from traditiona C-V analysis along with the corresponding actual free-carrier profile according to equation (4.9) for various constant trap densities.

## 4.3 Conductance DLTS

Capacitance deep-level transient spectroscopy (DLTS) was originally proposed by Lang [17] and described in various forms by others [18,19] as a technique to characterize traps in semiconductors. Similar information can also be obtained from conductance DLTS [20] and it is this method that has been utilized in this work. The technique involves monitoring the source-drain conductance of an FET structure while a repetitive gate voltage pulse is applied. The band diagrams corresponding to times before, during and after the gate pulse are illustrated in Figure 4.3. Before the pulse, a reverse bias $V_a$ has the channel nearly pinched off so that only a small steady-state conductance, $g_o$, is measured. The pulse acts to decrease the depletion region extent and causes empty electron traps formerly in the depletion zone to be

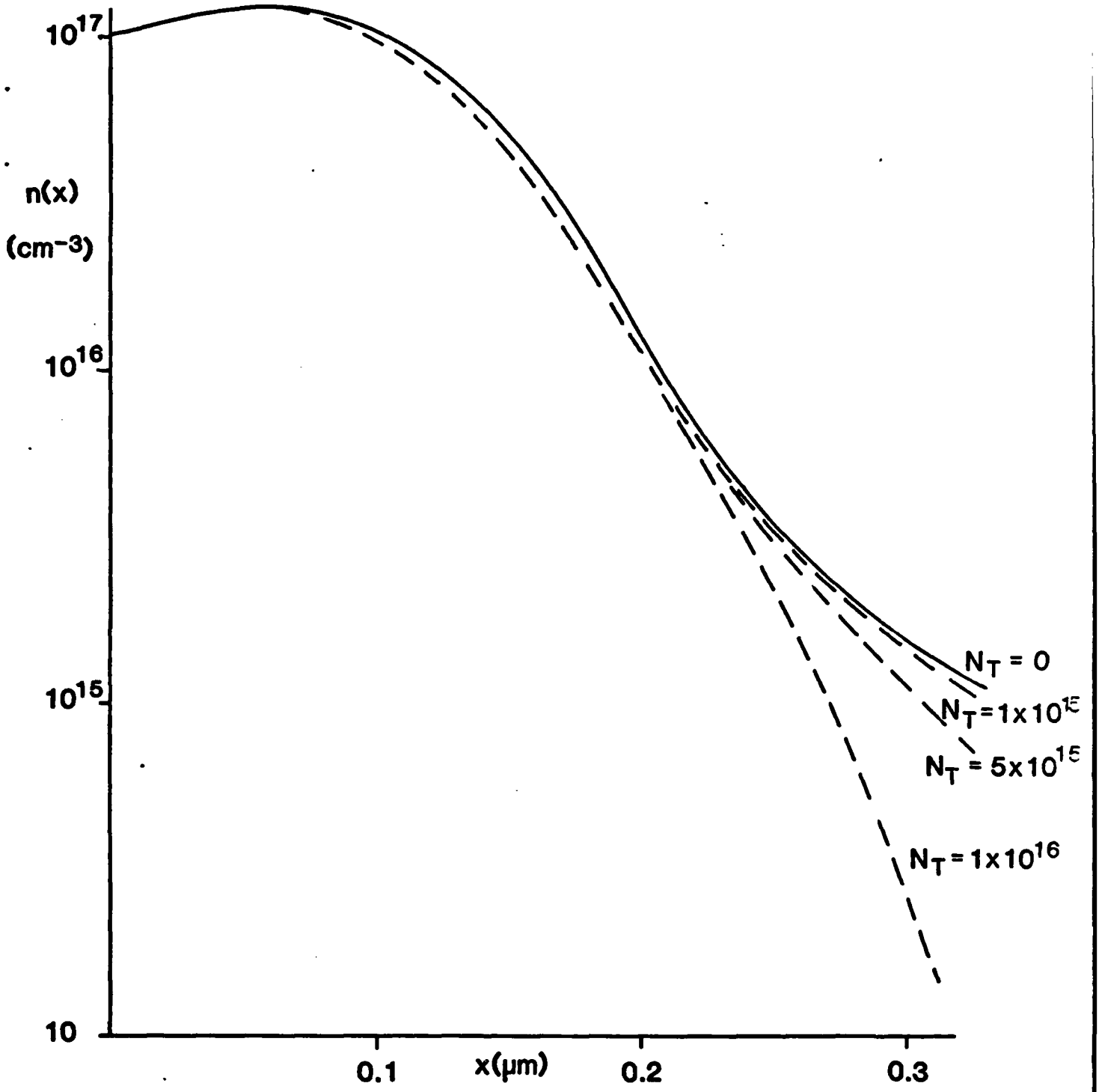


Figure 4.4 Effect of deep-level traps on C-V interpretation of free-carrier profile. The solid line represents the computed free-carrier profile if no traps are present. The dashed lines are the resulting concentrations for various constant trap profile levels.

filled (see Figure 4.3b). Immediately after the pulse, the depletion region is deeper than before the pulse since the filled traps are no longer positively charged. This increase in depletion width — signified as $\Delta x$ in Figure 4.3c — causes a decrease in the source-drain conductance $\Delta g$. A decay of this non-equilibrium change in conductance will occur as the filled traps emit electrons back into the conduction band. The decay process is very slow compared to gate capacitance time constants, however, so that $\Delta g$ due to filled traps immediately after the pulse is not difficult to determine. It is this quantity — the change in conductance from the steady-state value immediately after the pulse — which is of interest here. The actual rate of decay as a function of temperature which characterizes more traditional DLTS analysis [17-20], is used only independently to determine the trapping state energy level. Finally, by using several gate pulses of different magnitudes, information about the deep energy levels as a function of depth can be obtained.

Under the steady-state condition of Figure 4.3a, the conductance $g_o$ can be computed from

$$g_o = \frac{qZ}{L} \int_{x\omega}^{a} \mu_o(x)\, n(x)\, dx \qquad (4.10)$$

where

$a$ = the maximum epi-layer depth,

$Z$ = device gate width,

$L$ = device gate length,

and

$\mu_o$ = the low-field electron mobility.

Likewise, the change in conductance immediately after the pulse can be written from Figure 4.3c as

$$\Delta g = -\frac{qZ}{L} \int_{x_\omega}^{x_\omega+\Delta x} \mu_o(x)\, n(x)\, dx \qquad (4.11)$$

Equations (4.10) and (4.11) require that mobility be known as a function of donor density and background compensation. This is done using the theoretical results of Walukiewicz et al. [21] in conjunction with Monte Carlo velocity-field predictions. Our own Monte Carlo results [22] were used to determine the mobility as a function of background donor density with no traps present, and the Walukiewicz values were then normalized to the Monte Carlo numbers. The normalized data was finally curve fit to obtain an empirical expression for mobility as a function of background donor density and compensation ratio. The resulting expression is

$$\mu_o = \frac{\mu_{max}}{1 + (\frac{\log N_D}{N_D})^c} \cdot (1 - \Theta)^b \qquad (4.12)$$

where

$$\mu_{max} = 8380 \ (cm^2/V*sec),$$

$$N_o = 23.2553,$$

$$c = 23.0,$$

$$\Theta = N_T/N_D.$$

$$b = \begin{cases} 0.025*(\log N_D) - 0.817278*(\log N_D) + 6.252838 \\ \qquad \text{for } N_D > 10^{21} \ (m^{-3}) . \\ \\ 0.114992 \\ \qquad \text{for } N_D < 10^{21} \ (m^{-3}). \end{cases}$$

and where $N_D$ is given in ($m^{-3}$). Expression (4.11) is plotted against the normalized Walukiewicz values in Figure 4.5. As can be seen from the plot, the agreement is quite good.

Another restriction which applies to the situations illustrated in Figure 4.3 is that Poisson's equation must hold. As noted above, however, a non-zero charge density which gives rise to a potential gradient exists within the channel independent of bias. This potential is not the quantity of interest for this analysis. Rather, it is the relationship of the change in applied potential to the extent of the depletion width which must be described. These quantities are related through the charge which can be moved — n(x) and $N_T(x)$ — and are therefore independent of $N_D(x)$. Thus, the appropriate form of Poisson's equation to describe Figure 4.3a is $x_\omega - \lambda(x_\omega)$

$$V_a = \frac{q}{\varepsilon_R \varepsilon_o} \left\{ \int_o^{x_\omega} \int_o^{x} n(z)dzdx + \int_o^{x_\omega - \lambda_\omega(x_\omega)} \int_o^{x} N_T(z)dzdx - X_\omega \int_o^{x_\omega} n(z)dz \right.$$
$$\left. - (x_\omega - \lambda(x_\omega)) \int_o^{x_\omega - \lambda(x_\omega)} N_T(z)dz \right\} - \phi \qquad (4.13)$$

where

$\phi$ = built-in potential.

The applicable equation for Figure 4.3b is obtained by simply changing $V_a$ to $V_p$, $x_\omega$ to $x_p$ and $\lambda(x\omega)$ to $\lambda(x_p)$ in equation (4.13). Similarly, for Figure 4.3c

$$V_a = \frac{q}{\varepsilon_R \varepsilon_o} \left\{ \int_o^{x_\omega + \Delta x} \int_o^{x} n(z)dzdx + \int_o^{x_p - \lambda(x_p)} \int_o^{x} N_T(z)dzdx - (x_\omega + \Delta x) \int_o^{x_\omega + \Delta x} n(z)dz \right.$$
$$\left. - (x_p - \lambda(x_p)) \int_o^{x_p - \lambda(x_p)} N_T(z)dz \right\} - \phi \qquad (4.14)$$

It can be noted from Figure 4.3 that only the trap sites within a distance of $x_\omega - \lambda(x_\omega)$ from the surface can be alternately filled and emptied by the pulse $V_p$. For the case studied here, this corresponds to a depth of about 0.1 μm. For distances into the device greater than this, the trap concentration still enters into the computations through the free-carrier concentration as specified by equation (4.9), and through carrier mobility as expressed in equation (4.12).

## 4.4 Method of Solution

The differential capacitance data, conductance DLTS data, and measurement of the trapping state energy level when coupled with the equations of the preceding sections provide sufficient information for determining the profiles of interest. Certain problems exist, however, in utilizing the data and equations together.

Equation (4.10) requires that a value for the maximum epi-layer depth be known. With ion-implanted profiles, however, this is a difficult quantity to determine. For the low-energy (70-140 keV) Si implants studied here, it was found that a good value for epi-thickness was on the order of 0.3 to 0.35 μm. This corresponds to a free-carrier density a little more than two orders of magnitude below the peak free-carrier density in the device.

The limitation of the C-V measurement technique itself to obtain data near the surface of the sample creates another difficulty in the analysis. Equations (4.3), (4.9), (4.13) and (4.14) all require knowledge of the free-carrier concentration throughout the active layer. This difficulty is overcome, however, by requiring that equations (4.10) and (4.13) hold simultaneously. In fact, if the C-V data were available throughout the active layer, then either equation (4.10) or (4.13) would be redundant and the problem would be overspecified. In collecting conductance DLTS data, both the reverse

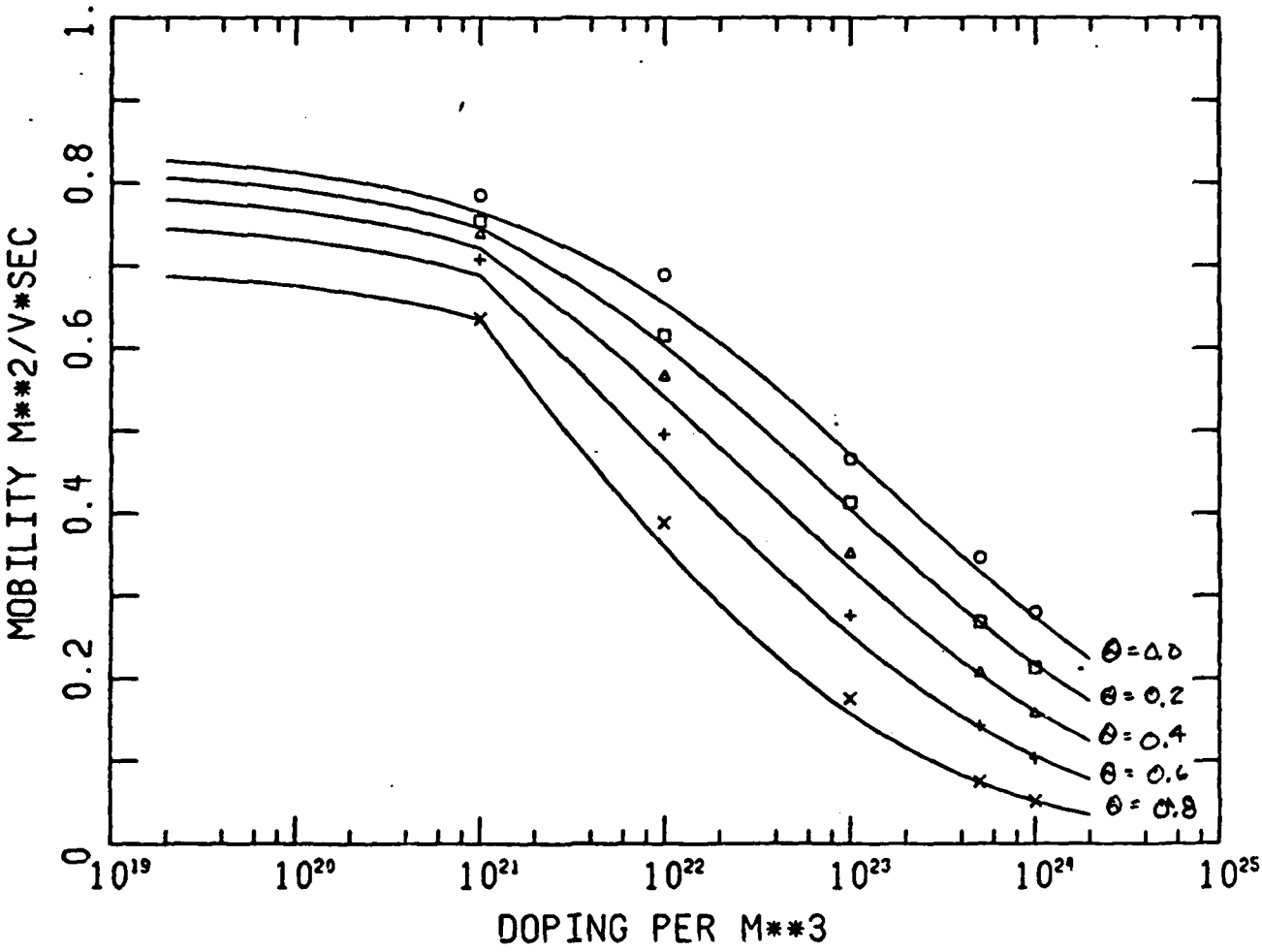


Figure 4.5 Low-field mobility as a function of doping and deep-level compensation. The solid lines are computed from eq. (12) for $\Theta$=0, 0.2, 0.4, 0.6 and 0.8. The data points are from normalized theoretical computations [12].

bias, $V_a$, and the steady-state conductance, $g_o$, are measured. Also, from C-V analysis and equation (4.4), a value for free-carrier concentration is obtained from some minimum obtainable depletion width, $x_{min}$, to the maximum epilayer extent, a. For values of x between the material surface and $x_{min}$, the free-carrier profile can only be estimated. The initial estimate of the free-carrier concentration near the surface can be made by assuming that the profile should be approximately gaussian in this region with the slope of the profile flat at the surface. Once a profile has been established over the entire active region, equation (4.14) can be used to calculate the depletion width, $x_\omega$, corresponding to applied bias, $V_a$. Likewise, equation (4.10) can be used to compute $x_w$ for a steady-state conductance, $g_o$. Any discrepancy between the two values for $x_w$ obtained by these equations must be due to inaccuracies in the built-in potential used or in the free-carrier concentration estimate between the surface and $x_{min}$. Adjustments can then be made to either of these quantities until the two values for depletion width agree.

Notice that this method produces only an equivalent built-in potential — free-carrier profile pair near the surface. However, since under normal device operation of an ion-implanted MESFET this region would always be depleted, this information is usually adequate.

To solve the equations of the preceding sections simultaneously in a rigorous fashion is still non-trivial. Equations (4.11) and (4.14) must hold for each pulse used in the conductance DLTS measurement. Thus, if twenty different pulse heights were used, there would be over forty integral and differential equations that must be solved simultaneously.

An alternative to this method is to assume that the background trap profile is known, and to compute the resulting conductance DLTS data. The actual DLTS measurement data can then be compared to the predictions for the assumed

trap profile. By making modifications on the assumed trap profile good agreement between the change in conductance predicted and that which is measured can be obtained.

This latter method was chosen for the work presented here. The system of equations was solved iteratively: each equation being solved individually to update only one quantity at a time. To begin, the trap concentration was assumed equal to some constant value throughout the device. The depletion width, $x_w$, corresponding to the steady-state bias, $V_a$. was determined using equations (4.10) and (4.13) as outlined above. Equation (4.3) was used to update the shallow-level donor profile. The function $\lambda(x_w)$ was then obtained from equation (4.6) and the free-carrier profile was determined through the use of equation (4.9). Normally, three to six iterations through the equations were required before convergence was achieved.

Once the free-carrier and shallow-level donor profiles were determined, equation (4.14) was used to compute the depletion width change, $\Delta x$, as a function of pulse bias, $v_p$. this information was then easily utilized with equation (4.11) to predict conductance DLTS data. Finally, the results were compared to the DLTS data actually measured on the device. At this point, adjustments could be made to the trap profile originally assumed, and the process repeated until good agreement was obtained.

## 4.5 Results

A 1 μm gate length MESFET along with a differential capacitance test pattern were fabricated on Silicon implanted Cr-doped GaAs substrate. Conductance DLTS and C-V measurements were performed on these devices and a dominant deep-level trap state was identified 0.736 eV below the conduction band. The measurements were used as input data to a computer simulation which computes the desired profiles as outlined in the preceding sections.

As a first guess, the trap concentration was assumed constant. The solid lines of Figure (4.6) give the resulting conductance DLTS predictions for various trap densities along with the measured data. Notice that small values of $V_a-V_p$ represent areas deep in the device while larger values represent areas close to the surface. Using simple step function approximations for the trap profile results in considerable improvement in the obtained agreement. A step-profile defined by

$$N_T = \begin{cases} 3.0\text{x}10^{15}\ (\text{cm}^{-3}),\ 0.0 < x < 0.040\ \mu\text{m} \\ 2.5\text{x}10^{15}\ (\text{cm}^{-3}),\ 0.04 < x < 0.055\ \mu\text{m} \\ 2.0\text{x}10^{15}\ (\text{cm}^{-3}),\ 0.055 < x < a \end{cases}$$

was used to obtain the results shown by the dashed line of Figure 4.6. Here the agreement between model predictions and measurements is excellent.

The final resulting free-carrier, shallow-level donor, and deep-level trap concentrations as a function of depth into the material are shown in Figure 4.7. Notice that deep into the channel there is some scatter of the shallow-level donor data. This begins to occur when the trap concentration and the shallow-level donor concentration are of the same order of magnitude. The uncertainties in the exact shallow-level concentration at this depth into the channel are not critical to the profile predictions. This is true since the magnitude of all the profiles of interest are small at this depth when compared to their magnitudes near the implantation peak.

The low-field mobility profile obtained from this analysis is also shown in Figure 4.7. The curve can be compared to the results of Das and Kim [23], and seems to be in good qualitative agreement.

## 4.6 Conclusion

A measurement technique for determining free-carrier, shallow-level donor, trap and mobility profiles of ion-implanted devices has been illustra-

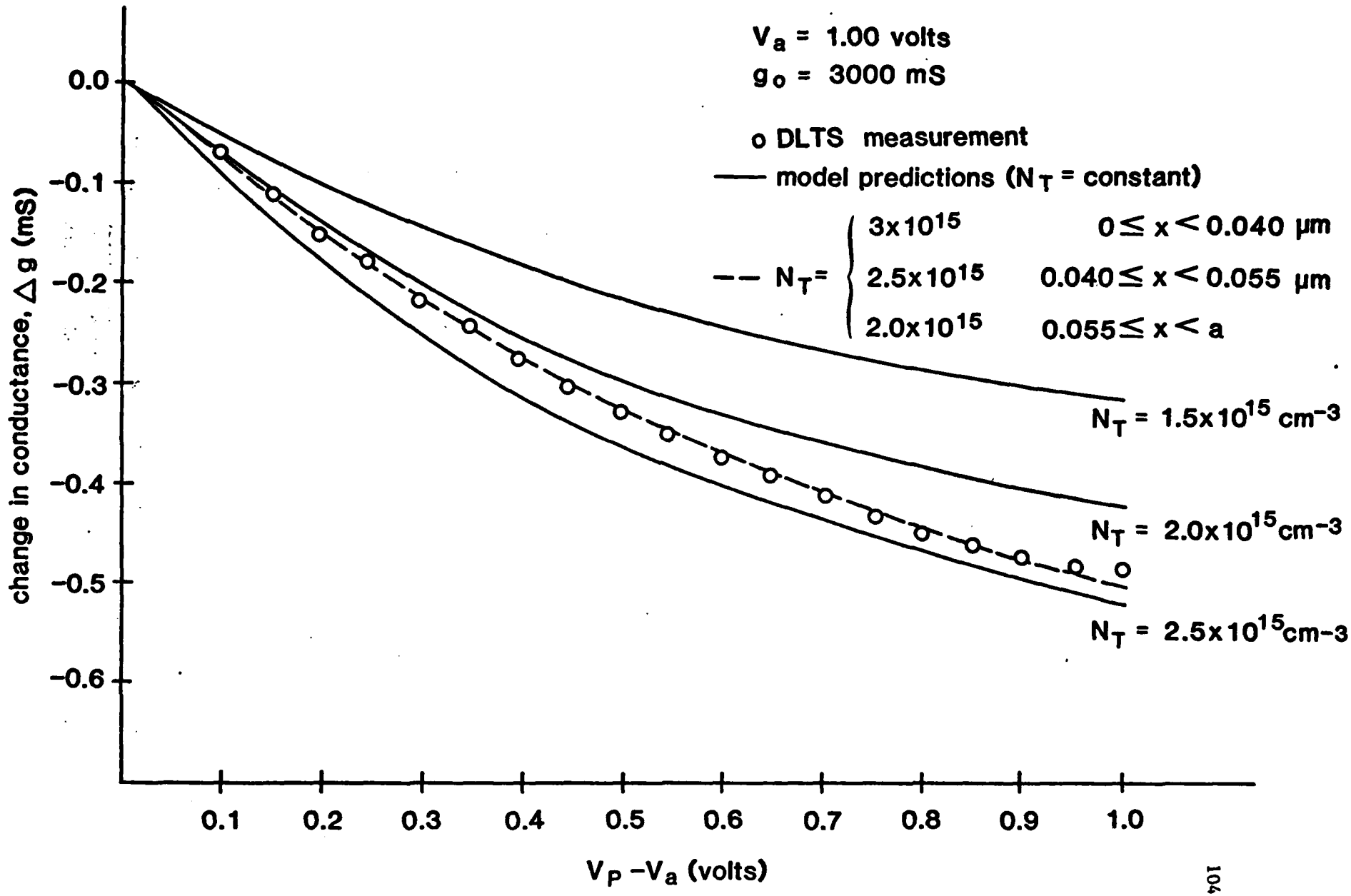


Figure 4.6 Conductance DLTS results. The data points are from actual measurements. The solid lines represent predicted data for constant trap concentration background. The dashed line is the predicted data for the step profile defined in the figure.

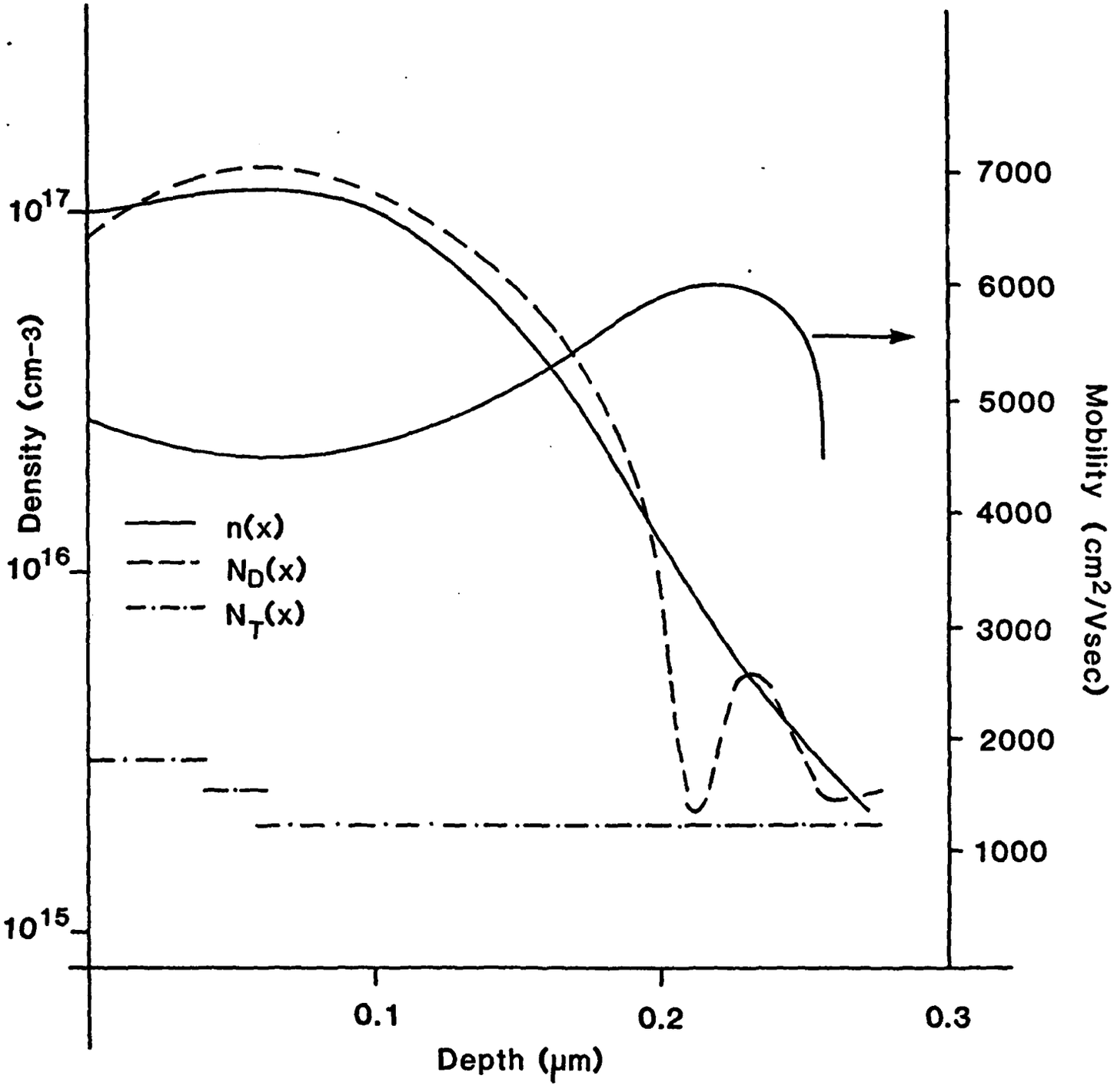


Figure 4.7 Resulting concentration profiles and low-field mobility profile for the case examined.

ted. The technique involves non-destructive electrical measurements coupled with the solution of applicable device equations. The appropriate equations have been developed and a method of solution examined. Finally, the technique has been applied to a sample case, and the results presented.

It should be noted that these results are subject to the limitations of the abrupt depletion approximation which has been assumed for the equations that have been presented. This limitation can become severe in the lower-doped regions of the device where the Debye length is relatively large [24]. However, it should be noted that most one-dimensional FET models also make use of the abrupt depletion approximation. For applications involving the use of one-dimensional models, therefore, the consistency of the profiling and modeling techniques is a desirable quality.

# 5.0 TWO-DIMENSIONAL MONTE CARLO MESFET SIMULATION

An important application of solid state theory is predicting performance of a semiconductor device from a knowledge of the structure of the device and of parameters describing the material of which the device is made. In this chapter, we describe a simulation of a submicron GaAs metal-semiconductor field-effect transistor (MESFET), using a two-dimensional ensemble Monte Carlo simulation coupled with a program for solving Poisson's equation. Currents given by the Monte Carlo simulation are much larger than those given by a conventional calculation. This difference can be attributed to the fact that the Monte Carlo simulation accurately accounts for transient transport, whereas the conventional calculation assumes that steady-state conditions prevail throughout the device.

## 5.1 Device Structure

Figure 5.1 shows the device used in this work. The MESFET is built on a semi-insulating substrate. The length of the gate is 0.2 μm with 0.1 μm spaces between the gate and the heavily-doped source and drain regions. The device is formed by multiple ion implantations to produce the impurity profiles shown in Fig. 5.2. The source and drain contacts are ohmic and the gate contact is a Schottky barrier diode.

## 5.2 Description of the Simulation

The simulation uses a time-step method described by Hockney and Eastwood [25]. The channel of the MESFET is mapped onto a two-dimensional grid and approximately 8000 carriers are distributed among the cells of the grid. The carriers are allowed to drift and scatter under the influence of the electric fields in the channel for a short time, called a time step, using a two-dimensional ensemble Monte Carlo simulation. At the end of the time step, the

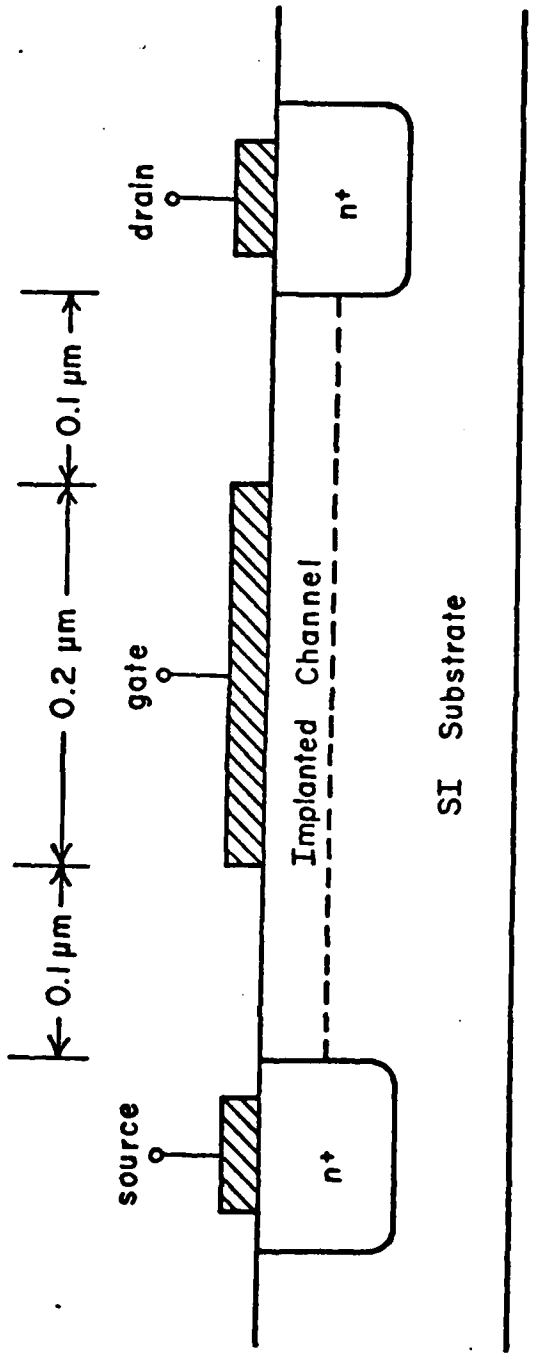


Figure 5.1 MESFET structure.

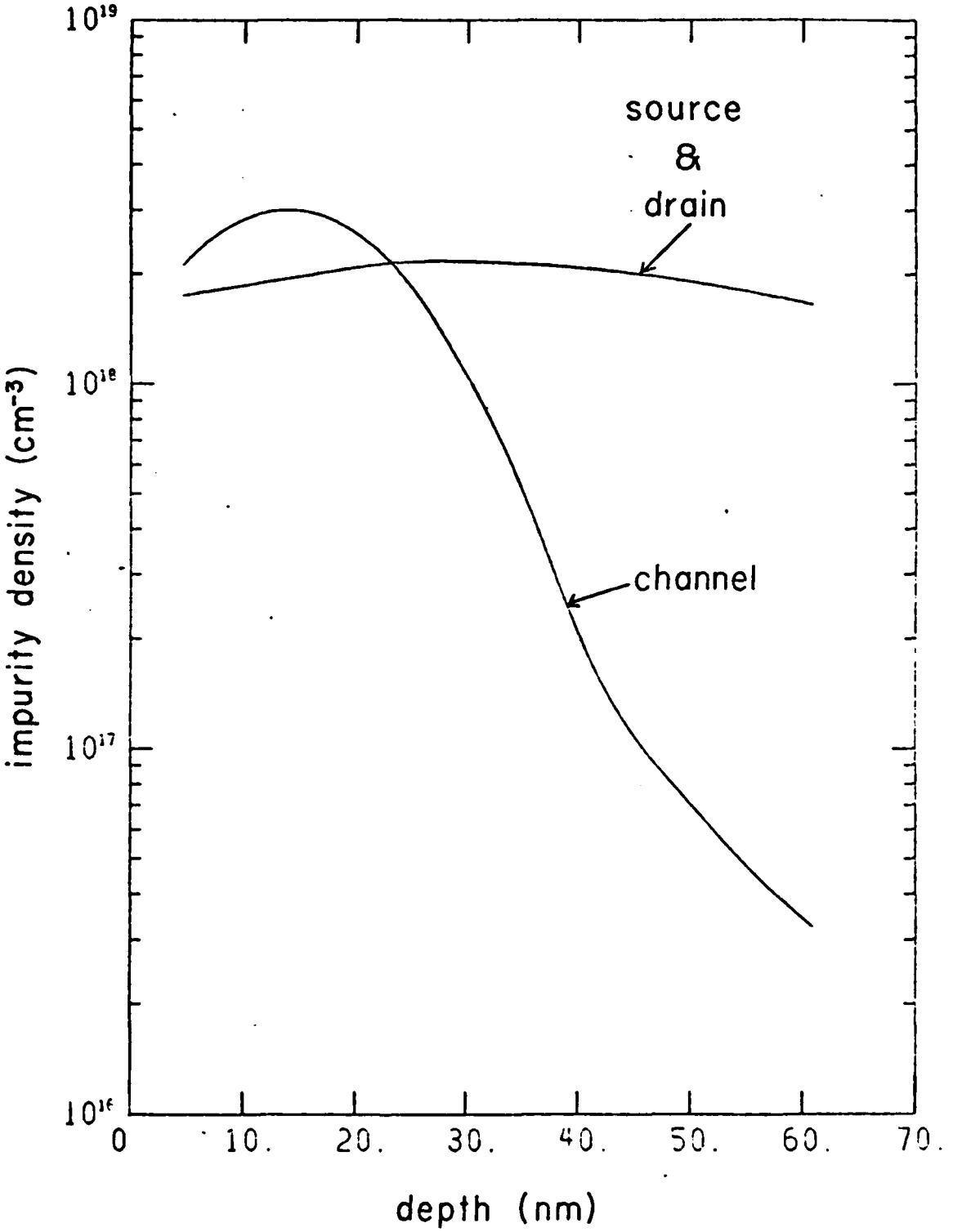


Figure 5.2 Doping profiles for the MESFET of Fig. 5.1.

charge density at each grid point is determined and the electric field at each grid point is calculated by solving Poisson's equation. The carriers then drift and scatter for another time step, after which the electric fields are calculated again. This process is repeated until a steady-state solution is obtained.

### 5.2.1 Grid Details

The grid points form a uniform rectangular mesh, with the first and last columns located in the heavily-doped source and drain regions, as shown in Fig. 5.3. Each grid point is the center of a rectangular cell in which the electric field and carrier density are considered to be constant.

The first and last columns of cells (extending into the heavily-doped source and drain regions) are treated as ohmic contacts. The charge density is forced to be equal to the background charge density (impurity density) and the potential is equal to the applied potential.

After a time step, the charge associated with each simulated carrier is prorated over four nearest-neighbor grid points as illustrated in Fig. 5.4. Each simulated carrier is treated as a uniform rectangular cloud of charge having the dimensions of one cell of the grid and the charge is divided among the four neighboring grid points in proportion to the area of overlap of the cloud with the cells containing the grid points. This scheme for assigning charge to the grid points is called "cloud-in-cell" (CIC) or area-weighting [25]. The charge assigned to a grid point is given by

$$w(x,y) = AV(x/\Delta x)\ V(y/\Delta y), \tag{5.1}$$

where

$$v(\alpha) = \begin{cases} 1-|\alpha|, & |\alpha| \leq 1 \\ 0, & |\alpha| > 1 \end{cases}, \tag{5.2}$$

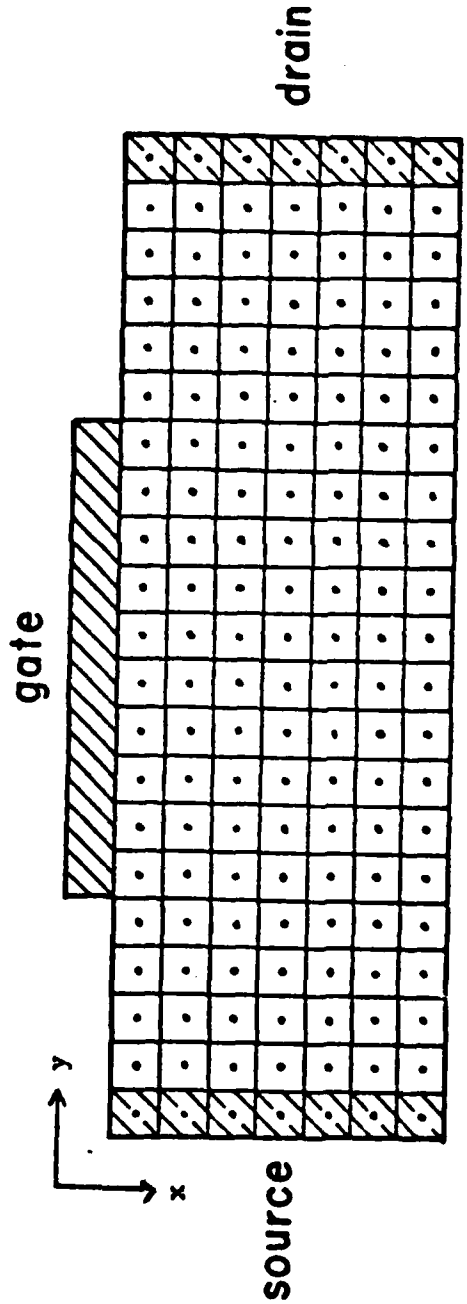


Figure 5.3 Grid point assignment.

and A is the charge of a simulated carrier given by

$$A = e\ N_f/N_s\ , \tag{5.3}$$

where $N_f$ is the number of free carriers in the device for charge neutrality and $N_s$ is the number of simulated carriers. Here, x and y are the coordinates of the grid point (using the position of the carrier as the origin), and $\Delta x$ and $\Delta y$ are the dimensions of the grid.

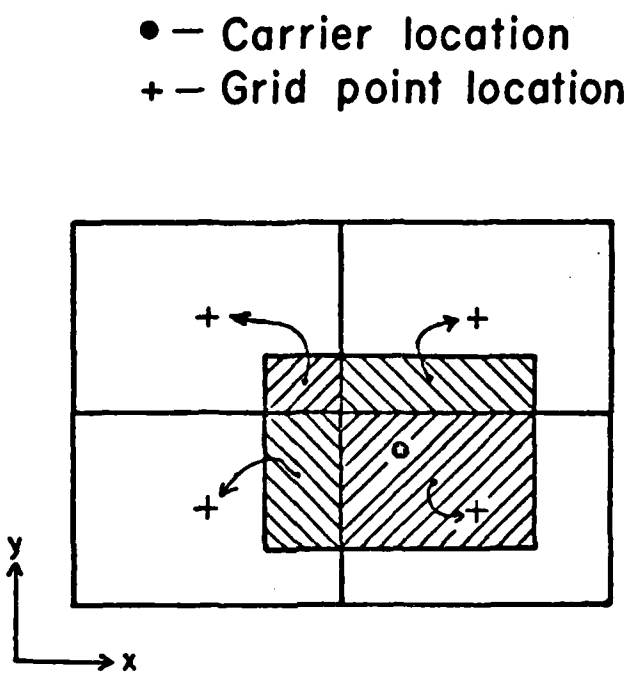


Figure 5.4 Cloud-in-cell method of assigning charge to grid points.

### 5.2.2 Monte Carlo Program

The Monte Carlo program used to simulate the motion of electrons in the MESFET is a modified version of the ensemble Monte Carlo program described elsewhere [26]. The modifications involve tracking each carrier on the two-dimensional grid described above the including a position-dependent electric field $\vec{E}(x,y)$.

The top and bottom of the grid are treated as reflecting boundaries and the left and right boundaries (source and drain regions) are treated as ohmic contacts (absorbing boundaries). Strictly, the portion of the top boundary under the gate should be treated as an absorbing boundary; however, under normal operating conditions (negative gate bias) very few carriers reach the gate contact. Consequently, the error in calculated drain current introduced by using a reflecting boundary at the gate is negligible. One disadvantage of using the approximation is that the actual gate current cannot be calculated.

Before the simulation is started, the scattering rates are tabulated. In the MESFET, the scattering rates are functions of position and time because both impurity concentration ($n_i$) and free carrier concentration ($n_f$) are functions of position and time. For computational reasons, it is currently impractical to use time-and position-dependent scattering rates. It is necessary to assume that $n_i$ and $n_f$ are constant insofar as the scattering rates are concerned. The value used for both $n_i$ and $n_f$ is the average impurity density in the channel of the MESFET.

At the start of a simulation, each carrier is given an initial position and an initial momentum. The positions are selected to give charge neutrality. Each component of momentum is selected from a gaussian distribution having mean zero and standard deviation $\sqrt{m^* k_B T}$ corresponding to the average

energy $\langle\varepsilon\rangle = 3k_BT/2$ (in a parabolic band). All carriers are started in the lowest-lying conduction band.

After each time step, enough carriers are added to each cell in the heavily-doped source and drain regions to make each cell charge neutral, as is consistent with treating those regions as ohmic contacts. Here, the components of momentum are selected from "half-gaussian" distributions such that each carrier selected is entering the device.

5.2.3 Solution of Poisson's Equation

Poisson's equation is solved using a general subroutine for solving a single partial differential equation on a plane [27]. Boundary conditions are imposed as shown in Fig. 5.5. At the source and drain, the potentials are the applied potentials. Under the gate, the potential is equal to the difference $V_{gs}-V_{SB}$ between the applied potential $V_{gs}$ and the built-in potential $V_{SB}$=0.8 V associated with the Schottky barrier. On all other boundaries, the electric field normal to the boundary is zero.

5.2.4 Effect of Device Size

The computing time required for a simulation increases with the size of the device for two reasons: 1) more carriers must be used to obtain an accurate estimate of charge density, and 2) more time steps are needed to obtain a steady-state solution. A pessimistic estimate of the number of iterations needed is obtained by dividing the mean time required for a carrier to travel from source to drain by the time step. For a 0.4 μm GaAs MESFET, the number of 0.05 psec time-steps required for an "average carrier" ($v \approx 10^7$ cm/sec) is approximately 80. At present, our simulation procedure is impractical for devices larger than about 1 μm.

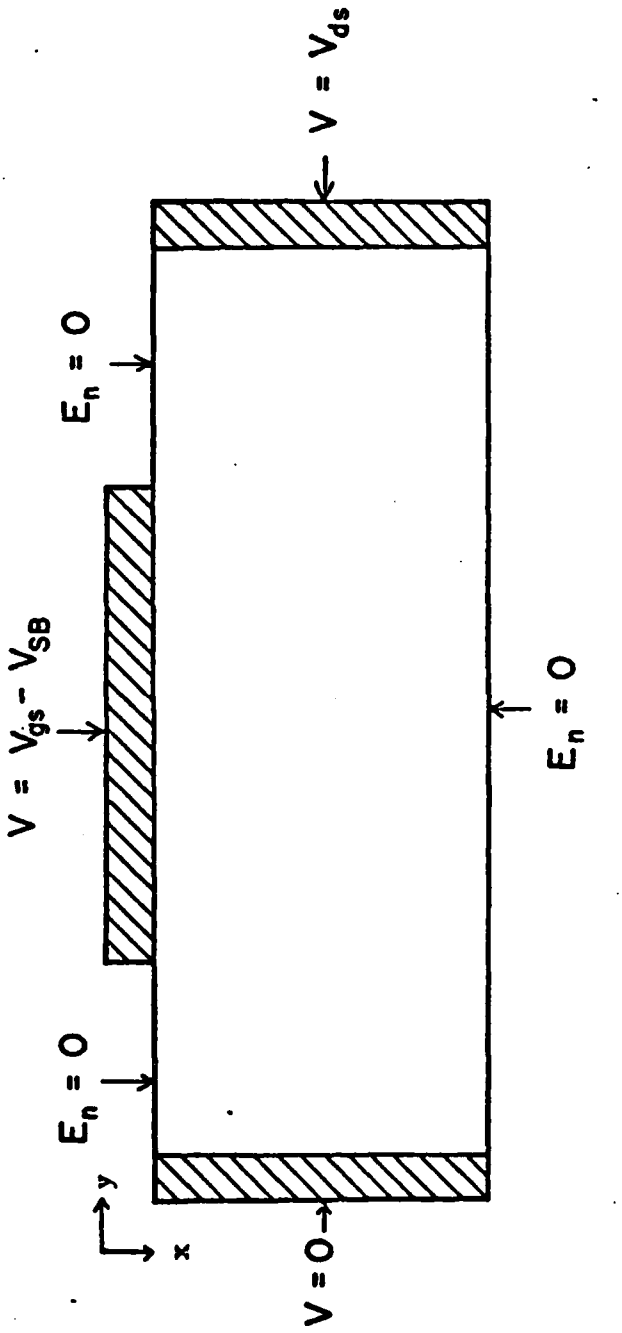


Figure 5.5 Boundary Conditions.

## 5.3. Charge Density, Velocity, and Current Density Calculations

Charge density is calculated by assigning the charge associated with each simulated carrier to grid points as described in Sec. 5.2.1. This gives large statistical fluctuations from one time step to the next because the number of carriers is relatively small. To reduce this fluctuation, we use a smoothed charge density given by

$$\rho_i(x,y) = 0.9\ \rho_{i-1}(x,y) + 0.1\ \rho_u(x,y)\ (i=1,2,3,\ldots)\ , \qquad (5.4)$$

where $\rho_i$ is charge density after the i'th time step, $\rho_o$ is initial charge density, and $\rho_u$ is charge density obtained using the cloud-in-cell assignment scheme described above (Sec. 5.2.1).

Current density in the y direction (from source to drain) is given by

$$J_y(x,y) = \rho(x,y)\ \bar{v}_y(x,y)\ , \qquad (5.5)$$

where $\rho$ is charge density and $\bar{v}_y$ is average velocity in the y direction. The average velocity in the y direction is calculated using the same smoothing procedure used for calculating the charge density. Average velocity $\bar{v}_y$ is calculated using

$$\bar{v}_{yi}(x,y) = 0.9\ \bar{v}_{yi-1}(x,y) + 0.1\ \bar{v}_{yu}(x,y)\ (i=1,2,3,\ldots), \qquad (5.6)$$

where $\bar{v}_{yi}$ is average velocity after the i'th time-step, $\bar{v}_{yo} = 0$, and $\bar{v}_{yn}$ is the average velocity obtained using a cloud-in-cell scheme for assigning velocities to grid points [see 4.1].

## 5.4 Results for a GaAs MESFET

This section gives results of a two-dimensional Monte Carlo simulation of a GaAs MESFET and compares these results with those obtained using a conventional two-dimensional device analysis program.

Figure 5.6 shows an I-V characteristic obtained from a Monte Carlo simulation for a GaAs MESFET having gate width 50 μm. Figure 5.7 shows the I-V characteristics given by a conventional 2D device analysis program for the

same device. The currents given by the Monte Carlo simulation are almost 3 times those given by the conventional device analysis program. The larger currents given by the Monte Carlo simulation arise from velocity overshoot in the channel of the MESFET. The Monte Carlo simulation accounts for transient effects (e.g., velocity overshoot), whereas the conventional device analysis program uses a static v-E characteristic. The velocity-field relationship used in the conventional device analysis program is

$$v(E) = \frac{\mu_o E + v_s (E/E_o)^4}{1 + (E/Eo)^4} \tag{5.7}$$

where the saturation velocity $v_s = 0.85 \times 10^7$ cm/sec, $E_o = 4$ kV/cm, and the low-field mobility $\mu_o$ given by

$$\mu_o(n_i) = \mu_s \{1 + [\log (n_i)/n_o]^{25}\}^{-1} \tag{5.8}$$

where $n_i$ is impurity concentration, $n_o = 22.9294$, and $\mu_s = 10^4$ cm$^2$/V-sec. The maximum velocity given by (5.7) for the channel profile of Fig. 5.2 is $v_m \simeq 1.67 \times 10^7$ cm/sec. This maximum velocity corresponds to $E \simeq 3.63$ kV/cm. For a 0.4 μm device with $V_{ds} = 2$ V, the average electric field in the channel is 50 kV/cm. Therefore, the velocities of the carriers in the conventional device analysis program are nearer the saturation velocity than the peak velocity.

Figure 5.8 shows average velocity from the Monte Carlo simulation versus distance from the source for $V_{gs} = 0$ and $V_{ds} = 2$V. The average velocity under the gate is approximately $3 \times 10^7$ cm/sec. This is almost twice the maximum velocity given by (5.7) and is more than 3 times the saturation velocity. The average carrier velocity under the gate is about $3 \times 10^7$ cm/sec for each bias condition simulated. This explains much of the difference between the I-V characteristics of Figs. 5.6 and 5.7.

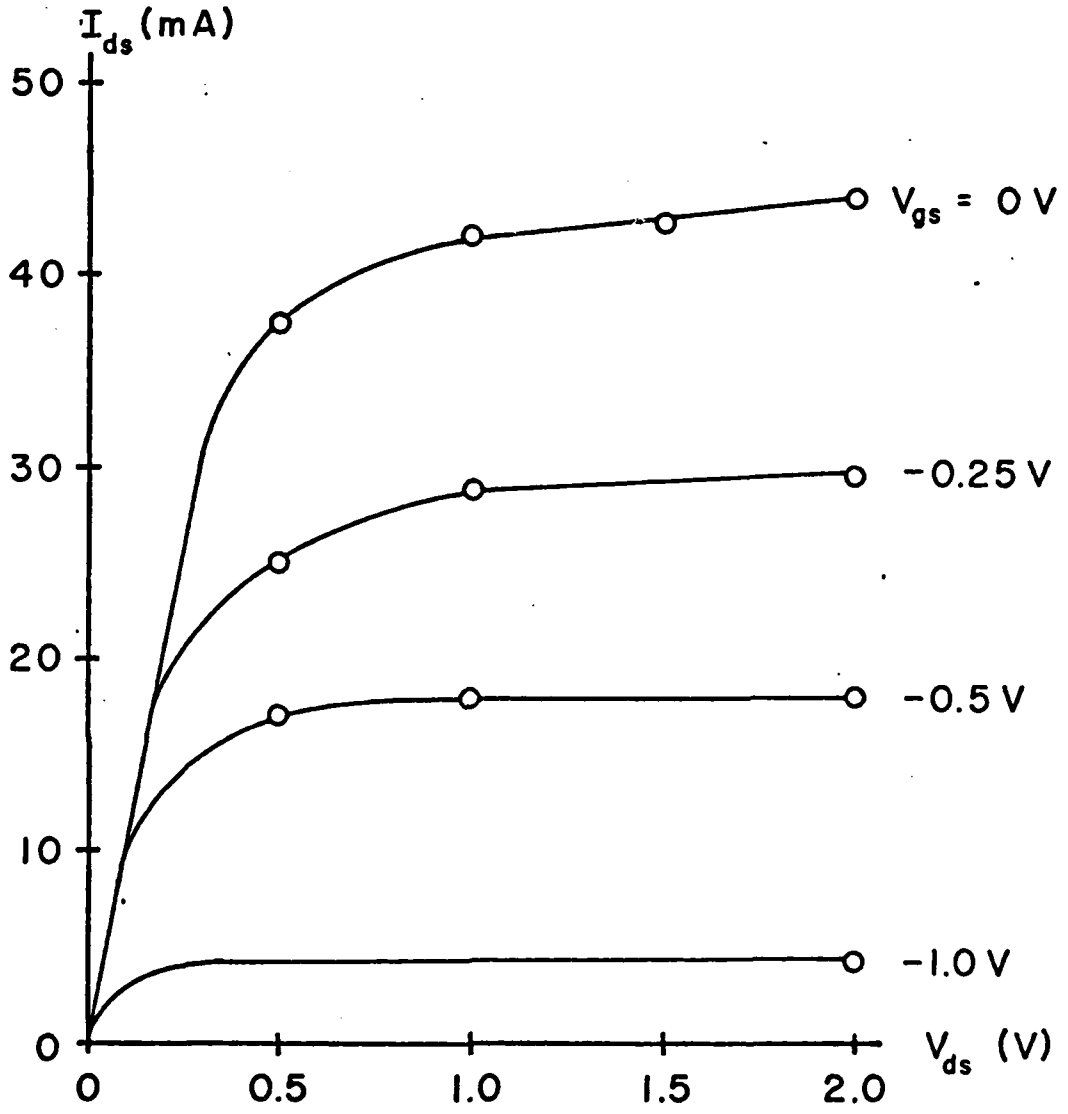


Figure 5.6 I-V characteristic obtained from a two-dimensional ensemble Monte Carlo simulation for a GaAs MESFET having a gate width 50 μm.

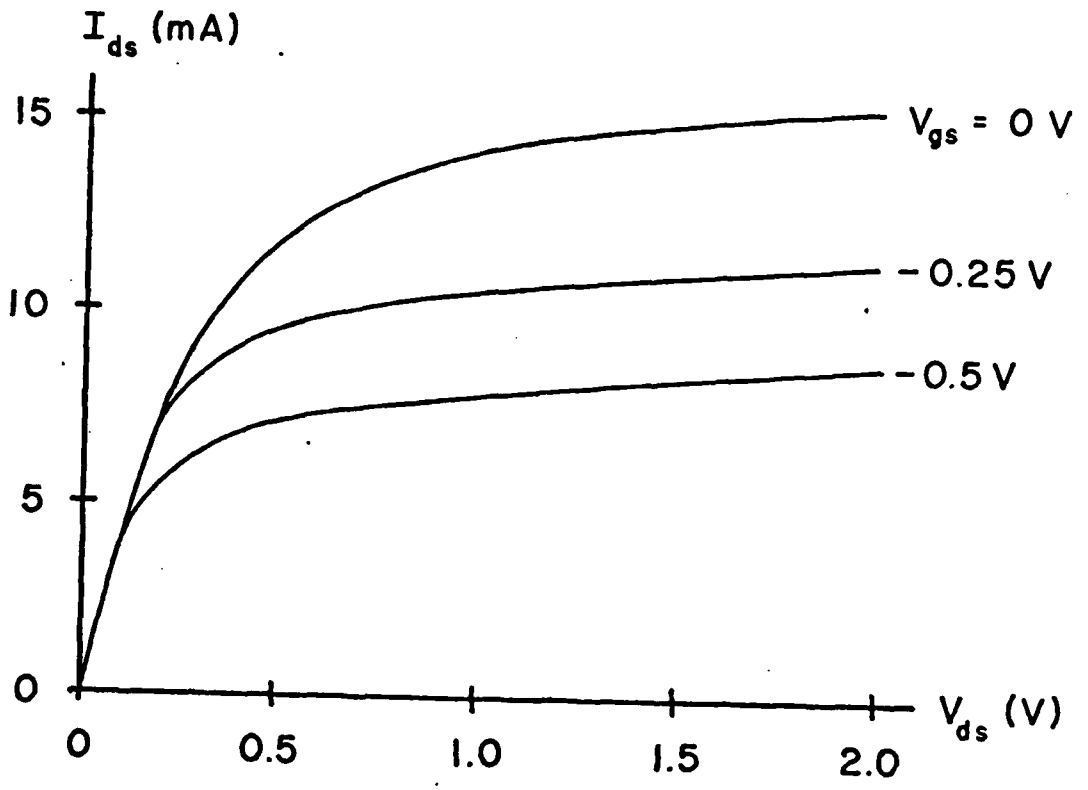


Figure 5.7 I-V characteristic given by a conventional 2D device analysis program for a GaAs MESFET with gate width 50 μm.

Figure 5.9 shows equipotential contours in the MESFET for $V_{gs} = 0$ and $V_{ds} = 2$ V. Most of the voltage drop occurs between the gate and drain. This gives rise to very high fields near the drain; however, this does not mean that the fields in other regions of the device can be considered small. For example, under the gate the potential drop is about 0.4V. The corresponding field is approximately 20 kV/cm. For this field strength, velocity overshoot persists for about 0.5 psec [26], in which time an average carrier travels about 0.2 μm. From Fig. 5.8, the distance over which an average carrier in the channel exhibits velocity overshoot is about 0.2 μm. This is in excellent agreement with the results given in [26].

Figure 5.10 shows net charge density (carriers and impurities) for the MESFET with $V_{gs} = 0$ and $V_{ds} = 2$ V. The net charge density is obtained using

$$\rho_n(x,y) = \rho(x,y) + q\, N_D(x,y), \tag{5.9}$$

where $N_D$ is background impurity (donor) concentration and $\rho$ is charge density for the carriers alone. The depletion region under the gate and the accumulation region near the drain are apparent in Fig. 5.10.

## 5.5 Summary and Conclusions

A Monte Carlo simulation of a submicron ion-implanted GaAs MESFET is described. The simulation uses a two-dimensional ensemble Monte Carlo simulation coupled with a program for solving Poisson's equation (to obtain a self-consistent solution). Currents calculated using the Monte Carlo simulation are almost 3 times those given by a conventional 2D device analysis program. The large difference in the currents results from velocity overshoot (Velocity overshoot and other transient phenomena are not accounted for in conventional 2D device analysis programs). This result suggests that conventional 2D device analysis programs are inadequate for analysis and modeling of very small devices.

The 2D ensemble Monte Carlo simulation method for MESFETs could be useful in predicting performance of submicron devices; however, there are several problems that need more study, including accurate modeling of contacts and injection mechanisms, electron-electron scattering, position-dependent scattering rates, and modeling surface trapping in ion implanted devices (where most of the current is near the surface).

Another problem that warrants investigation is developing phenomenological models that describe transient transport in III-V semiconductor materials. If such models can be developed, considerable time and money could be saved by using a modified conventional analysis program instead of a 2D ensemble Monte Carlo simulation for device analysis. Such models may also provide a much better understanding of transient transport.

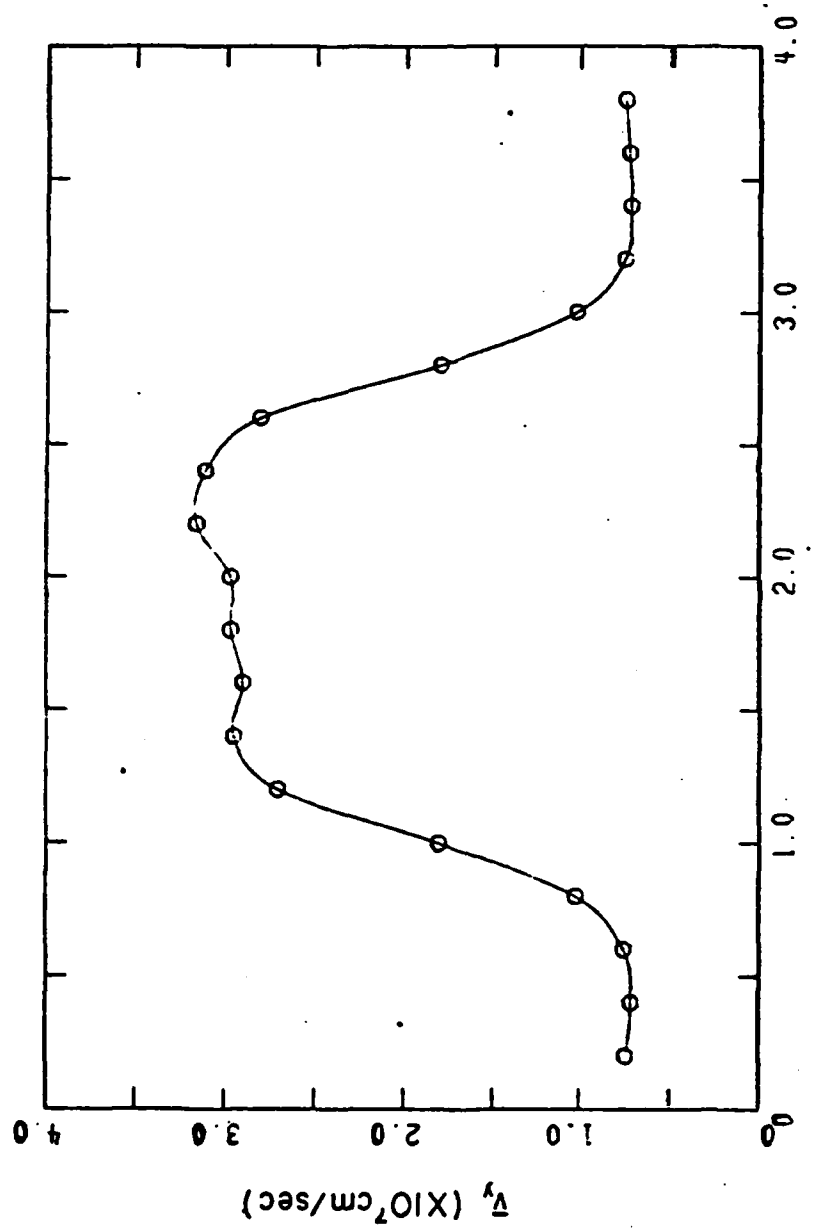


Figure 5.8 Average velocity versus distance from the source for $V_{gs}$ = 0 and $V_{ds}$ = 2 V.

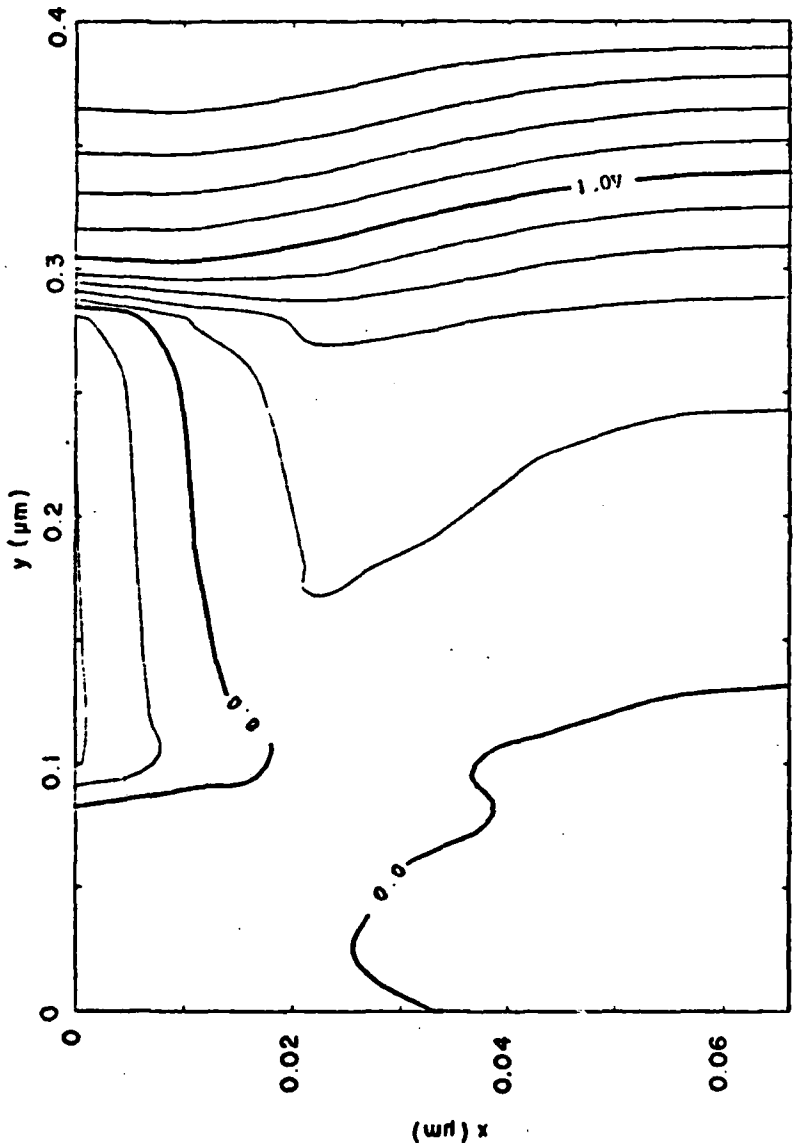


Figure 5.9 Equipotential contours in the MESFET for $V_{gs}$ = 0 and $V_{ds}$ = 2 V.

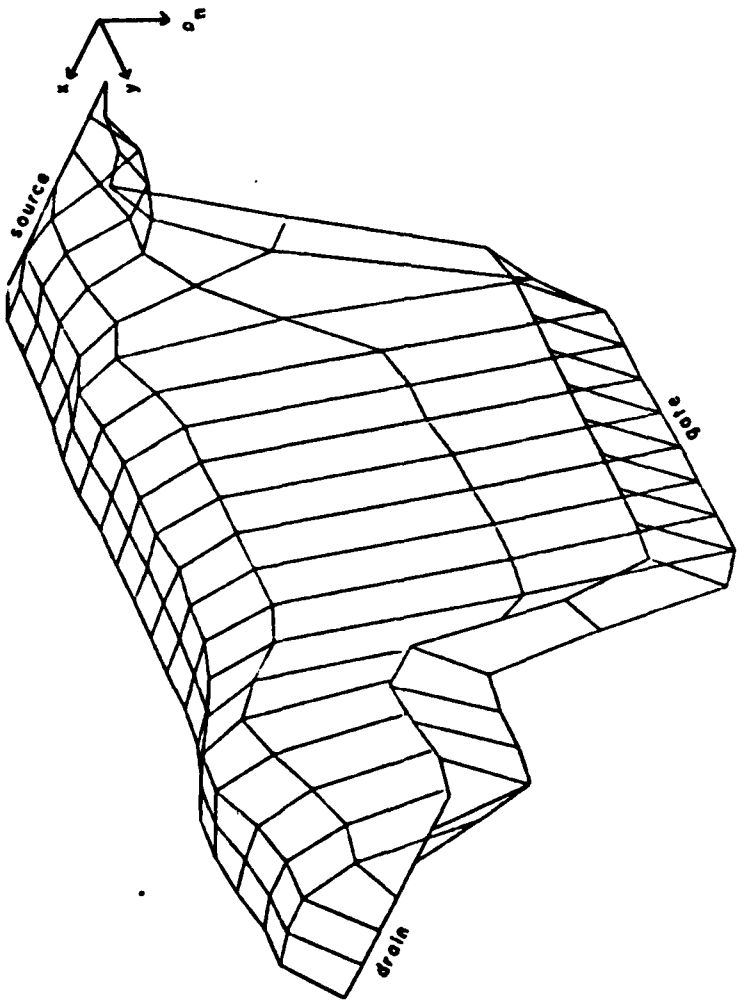


Figure 5.10 Net charge density in the MESFET for $V_{gs}$ = 0 and $V_{ds}$ = 2 V.

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