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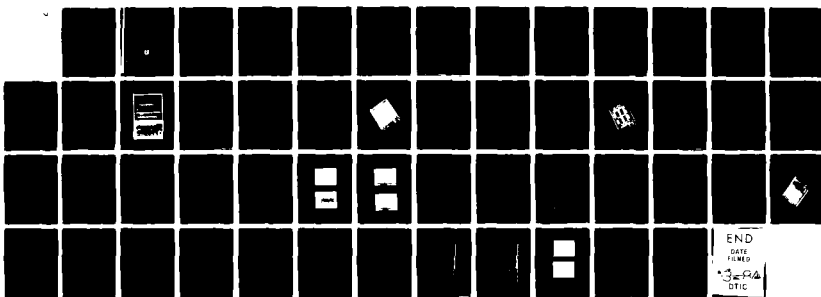
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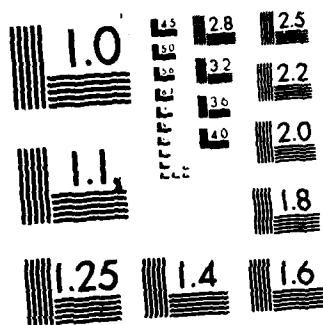
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VOICE PREPROCESSING SYSTEM
INCORPORATING A REAL-TIME SPECTRUM ANALYZER
WITH PROGRAMMABLE SWITCHED-CAPACITOR FILTERS

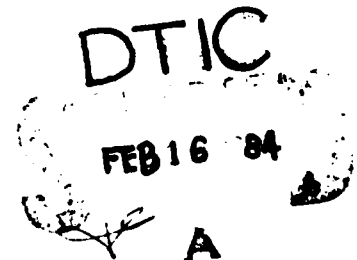
By
G. KNAPP

JANUARY 1984

Prepared for
DEPUTY FOR MISSION SYSTEMS
ELECTRONIC SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
Hanscom Air Force Base, Massachusetts

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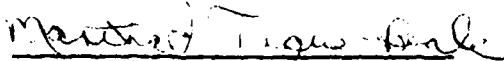
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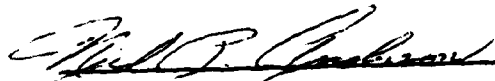
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SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE				
1a. REPORT SECURITY CLASSIFICATION Unclassified		1b. RESTRICTIVE MARKINGS		
2a. SECURITY CLASSIFICATION AUTHORITY		3. DISTRIBUTION/AVAILABILITY OF REPORT		
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE		Approved for public release; distribution unlimited.		
4. PERFORMING ORGANIZATION REPORT NUMBER(S) MTR-8677 ESD-TR-83-253		5. MONITORING ORGANIZATION REPORT NUMBER(S)		
6a. NAME OF PERFORMING ORGANIZATION The MITRE Corporation	6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION		
6c. ADDRESS (City, State and ZIP Code) Burlington Road Bedford, MA 01730		7b. ADDRESS (City, State and ZIP Code)		
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Deputy for Mission Systems	8b. OFFICE SYMBOL (If applicable) OCBE	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER		
8c. ADDRESS (City, State and ZIP Code) Electronic Systems Division, AFSC Hanscom AFB, MA 01731		10. SOURCE OF FUNDING NOS.		
11. TITLE (Include Security Classification) VOICE PREPROCESSING SYSTEM (cont.)		PROGRAM ELEMENT NO.	PROJECT NO. 4130	TASK NO.
				WORK UNIT NO.
12. PERSONAL AUTHOR(S) G. Knapp				
13a. TYPE OF REPORT Final Report	13b. TIME COVERED FROM _____ TO _____	14. DATE OF REPORT (Yr., Mo., Day) 1984 January	15. PAGE COUNT 52	
16. SUPPLEMENTARY NOTATION				
17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)	
FIELD	GROUP	SUB. GR.	ANALYZER SWITCHED-CAPACITOR	
			FILTER BANK VOICE SPECTRUM	
			SPEAKER IDENTIFICATION	
19. ABSTRACT (Continue on reverse if necessary and identify by block number)				
<p>→ As part of a speaker verification program for BISS (Base Installation Security System), a test system is being designed with a flexible preprocessing system for the evaluation of voice spectrum/verification algorithm related problems.</p> <p>The main part of this report covers the design, construction, and testing of a voice analyzer with 16 integrating real-time frequency channels ranging from 300 Hz to 3 KHz. The bandpass filter response of each channel is programmable by NMOS switched-capacitor quad filter arrays.</p> <p>Presently, the accuracy of these units is limited to a moderate precision by the finite steps of programming. However, repeatability of characteristics between filter units and sections seems to be excellent for the implemented fourth-order Butterworth bandpass responses.</p>				
20. DISTRIBUTION/AVAILABILITY OF ABSTRACT UNCLASSIFIED/UNLIMITED <input type="checkbox"/> SAME AS RPT. <input checked="" type="checkbox"/> DTIC USERS <input type="checkbox"/>		21. ABSTRACT SECURITY CLASSIFICATION Unclassified		
22a. NAME OF RESPONSIBLE INDIVIDUAL Susan R. Gilbert		22b. TELEPHONE NUMBER (Include Area Code) (617) 271-8088	22c. OFFICE SYMBOL	

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INCORPORATING A REAL-TIME SPECTRUM ANALYZER WITH PROGRAMMABLE SWITCHED-CAPACITOR FILTERS

19. (Concluded)

We obtained a 0.1 dB linearity error of signal detection and measured a signal-to-noise ratio of approximately 70 Db.

The preprocessing system discussed includes preemphasis filter design, gain normalizer design, and data acquisition system design as well as test results.

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ACKNOWLEDGEMENTS

The author wishes to thank P.A. Odierno for detailed design and construction of the data acquisition system and G.H. Monty for printed circuit lay-out and construction of the modules. Also appreciated is the assistance by W.A. Karlsen, J.A. Harper, and P.J. Alexander.

The author would like to thank in particular S.M. Jolly for his enthusiastic support of the program.

This document has been prepared by The MITRE Corporation under Project 4130, Contract No. F19628-82-C-0001. The contract is sponsored by the Electronic Systems Division, Air Force Systems Command, Hanscom Air Force Base, Massachusetts.



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SECTION 1

INTRODUCTION

Speech and speaker identification systems require preprocessing systems to extract precise voice parameters, or vectors. When utilized in suitable processing algorithms, machine recognition of words, or machine identification and verification of speakers can be accomplished. In this paper we shall discuss the design, implementation, and some test results of an integrating real-time spectrum analyzer voice preprocessing system. We designed this system primarily for experimental use with an algorithm developed by Texas Instruments for an Air Force speaker verification system.

The design approach for the preprocessor discussed here simplifies real-time spectrum analysis, thereby reducing costs and lowering the requirement for replacement parts and software. Simplification has been accomplished by a system design utilizing programmable switched-capacitor filter arrays and improved operational amplifiers.

BACKGROUND

In its basic form the BISS (Base Installation Security System) speaker verification system will consist of an entry control pedestrian booth, a voice preprocessor, and a microcomputer for data storage and voice print verification. As an individual passes through the pedestrian booth, he or she must repeat a random computer-prompted four-word phrase into a microphone. The individual's speech is first filtered into up to sixteen frequency bands by a bank of bandpass filter channels and is then digitized by a data acquisition system for processing by a recognition algorithm implemented in software. This algorithm compares the temporal pattern of the energy content in each of the frequency bands with the individual's previously recorded templates that are stored in the computer's memory.

Our voice preprocessing system will identify weaknesses and deficiencies in the current voice verification algorithm and test improvements developed at MITRE or elsewhere.

The MITRE development system consists of an acoustic isolation booth for data collection, a programmable switched-capacitor real time spectrum analyzer preprocessor, and a Zilog Z8000-based microcomputer system that can process the data or store them for analysis on a larger computer. In future efforts to reduce errors and increase

throughput rate, we will be studying the algorithm's sensitivity to a noisy environment, changes in the specifications of the preprocessor and improvements to the initial data-compression of the preprocessor, and algorithm.

MOTIVATION

Test results of an earlier experimental speaker verification system developed at MITRE and an analysis of the system by the MITRE project team revealed certain difficulties in the areas of uniformity, noise, and accuracy, which required additional development efforts. These problem areas prompted the work described in this paper.

The earlier dual point entry system was comprised of two digital preprocessors (one for each entry point) and a common minicomputer. Good results with error rates of 2% for rejection of valid voice patterns and 3% for acceptance of random cross matching of invalid voice patterns were achieved with this system; however, these results were obtained only if individuals used the same enrollment entry point for all subsequent verifications. In the proposed Air Force entry control system this would be impractical, since individuals will enroll at a central location and then verify at multiple sites at which they are authorized. In addition, the entry points at the sites may have multiple terminals to accommodate the real traffic loads.

The inability to match the enrolled voice pattern with the verification patterns at different locations, which we have called the "uniformity problem," is caused by non-uniformity of preprocessors and non-uniform, individual acoustic characteristics such as sound absorption, reflections and room resonance of the entry points and enrollment center.

The second problem area, the "noise problem," concerns system performance deterioration from internally and externally generated noises. Tests at RADC showed that throughput rates – the number of people who are able to pass through an entry control point in a given time – dropped by approximately one half when the random ambient noise of ≈ 80 dB (equivalent to a noisy office) was increased by 10 dB to a noise level equivalent to heavy traffic. At this noise level, too many phrases (up to four) had to be repeated before the system was able to match the voice pattern successfully.

Also, an improvement of the system's stated verification precision, which we have called the "accuracy problem," would permit higher throughput rates, and possibly, achievement of higher security levels.

All three problems – uniformity, noise and accuracy – stem from limitations in the verification system's original design. In terms of equipment uniformity, frequency

alignment provisions for the electronics of the two preprocessors were not provided, nor did the system include compensation for room acoustics. Preemphasis for the audio pass band is specified with a tolerance of ± 2 dB, equivalent to a maximum amplitude misalignment of 52% from one preprocessor to the next.

The noise problem is more complex. The signal-to-noise (S/N) ratio for the preprocessors is given as 36 dB, which would appear quite low, since the system also specifies a high-resolution, 12 bit analog-to-digital (A/D) conversion which has a theoretical S/N ratio of 83 dB.

This low S/N ratio of the original experimental verification system we believe is caused mainly by quantization noise from truncation and rounding errors inherent to digital processing (filter) systems with many multiplications. Also 6 dB signal is lost simply because of the front-end digital encoding of the bipolar audio signal. Furthermore, the system's S/N ratio has to include the external noise present at the preprocessor's microphone. We consider the upper noise level at certain air base locations to be 95 dB, a value based on measurements obtained at future entry point locations.

The accuracy problem is not as critical, because we believe that with improvements in uniformity and signal-to-noise ratio, an operational system with reasonable throughput rates can be obtained. The accuracy problem is related to the system's uniformity and noise; accuracy will increase with improvements to these areas as long as the algorithm's fundamental error limitation has not been reached.

Except for the RADC noise test, there are no experimental data or simulated data available providing conclusive proof that by improving preprocessor accuracy and uniformity, the throughput rate will increase. If we assume that improvements are possible, to what degree are accuracy and uniformity required at the hardware level?

There are two known hardware specifications that have an effect on the accuracy and uniformity problems:

- (1) the ± 2 dB tolerance of the preemphasis function;
- (2) the 12-bit A/D conversion of the preprocessor data.

For (1) we have a $\pm 26\%$ tolerance in accuracy and for (2) we obtain approximately $\pm 0.1\%$ accuracy of data conversion when two bits are deducted as overhead.

The ± 2 dB accuracy for the preemphasis can be easily improved by a good design, while an increase of the $\pm 0.1\%$ accuracy for the data conversion – to, let us say, $\pm 0.01\%$ – would very likely not improve the performance. This is because the instability of

the analog circuits will dominate the system accuracy if they are not designed with an overall tolerance of approximately $\pm 0.1\%$, a difficult and expensive approach. Nevertheless, there is considerable room for system improvement needed in order to justify the accuracy of a 12-bit A/D converter. Actually, the commercial equipment incorporated here for analog preamplification and equalization provides system uniformity adjustment to approximately ± 0.4 dB, with accuracies of ≤ 0.2 dB under laboratory conditions. This should be sufficient for experimental evaluations of throughput rates and hardware trade-offs.

SECTION 2

VOICE PREPROCESSOR SYSTEM

The entire voice preprocessor system, as mounted in its equipment rack, is shown in Figure 1. The system contains four 480 mm wide units: a 16-channel switched-capacitor filter bank with a threshold detector module, program control module, data acquisition system (top), a graphic equalizer (second), a microphone preamplifier with preemphasis filter (third), and the system's power supply (bottom).

The block diagram (Figure 2) depicts in more detail the specific functions of the four units. The audio signal from the microphone is first amplified by the preamplifier; then, signal alteration by acoustics in the booth is compensated for by the graphic equalizer, in the same way as sound is improved in recording studios. The natural roll-off (lowering) of the higher frequency contents of human speech is then raised to approximately the same average level for the entire voice audio band by a preemphasis filter. A sufficient sound level over the ambient noise is maintained by a predetermined setting (manual preset) of the acceptable speech threshold. A green LED mounted on the microphone serves as a volume indicator for the speaker.

Programmable switched-capacitor (SC) LSI filters are programmed as bandpass (BP) filters, to select up to 16 spectral components from the voice spectrum in accordance with filter specifications. The specifications are stored in memories that can be called up by manual or computer command through the memory program control; the memory system is decentralized. Each SC filter chip has its own auxiliary, 1/4 K memory carrying data for four different BP filters. Since the SC filters are sampled data systems, an anti-aliasing filter is required to eliminate folding frequencies. The sampling nature of the BP filters also requires post-filtering for removal of switching noise. After detection (rectification), each of the 16 signals is integrated by lowpass (LP) filters.

Data acquisition of the 16 analog signals is usually accomplished by multiplexing, sample and hold, and subsequent digitizing by an analog to digital (A/D) converter. However, in order to equalize all BP filter gains, a gain-normalizing circuit has been included between the multiplexing section and the A/D section of the data acquisition system. The A/D converter output registers are connected via a data bus with a microcomputer. The microcomputer performs speaker verification by comparing the obtained and processed temporal voice spectra with stored spectral data.

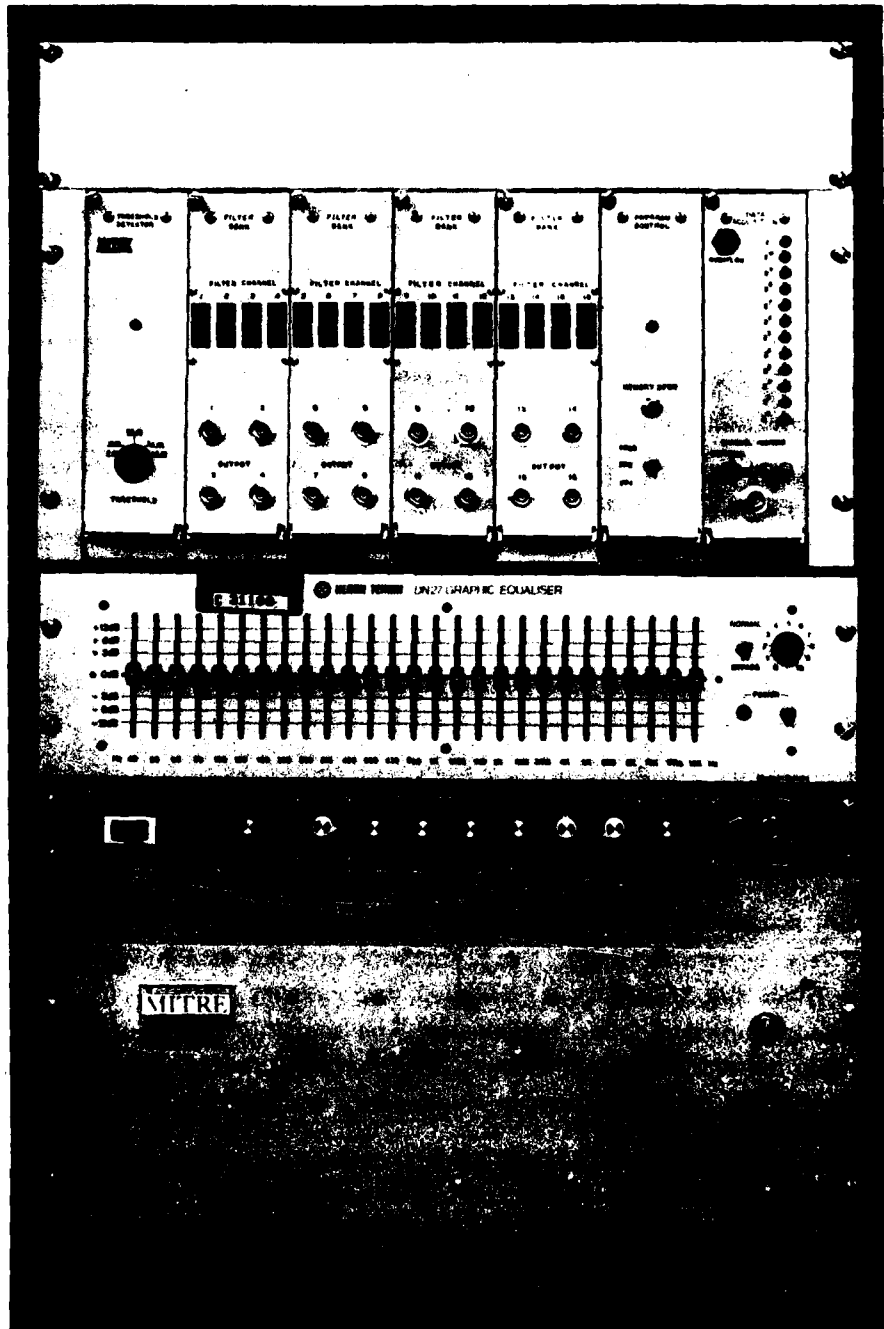


Figure 1. Front View of Voice Preprocessor System

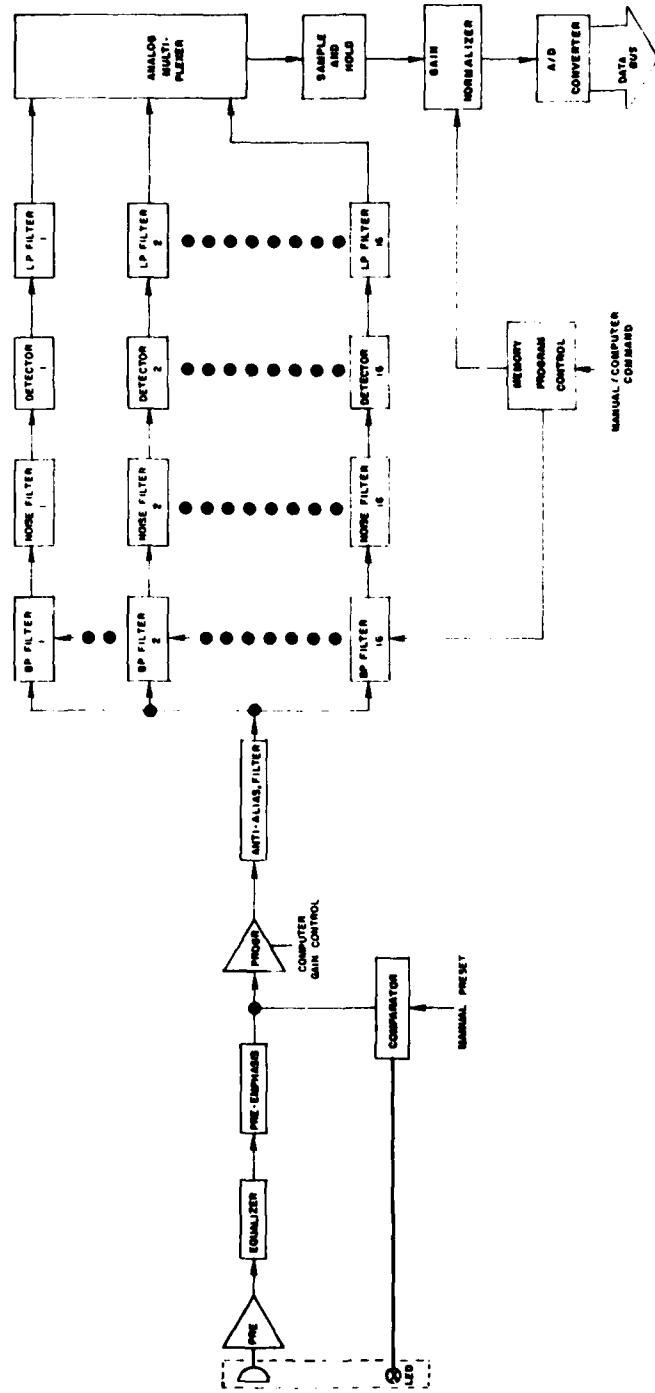


Figure 2. Block Diagram of Voice Preprocessor System

PREAMPLIFICATION

The relatively low output power of microphones requires preamplification before further processing of the signal can take place. A dynamic microphone is the best choice in terms of cost, output level, and accuracy over the limited frequency range of 300 Hz to 3 KHz. It is considered here as the input to the preamplifier.

Preamplifier

An Ashley instrument preamplifier Type SC-40 (shown in Figure 1) was selected for the following features: inputs for microphone and tape, a built-in equalizer with three variable filters, interface connections to external in-line equipment, and an over-drive indicator effective at all amplification stages.

Preemphasis Filter

Preemphasis of the speech spectrum is commonly applied in speech processors. A dynamic range reduction of approximately 20 dB can be achieved by normalizing the average power spectrum of speech. The fairly complex average power spectrum^[1] needs only to be equalized by simple highpass (HP) filters in most applications. Ideally, the resulting response by the preemphasis function is

$$H(f) = [G(f)]^{-1}, \quad (1)$$

with $G(f)$ the average spectrum of speech. Then we will obtain

$$G(f)H(f) = G(f)[G(f)]^{-1} = 1, \quad (2)$$

a unity response throughout the frequency range.

We implemented a preemphasis function published by Texas Instruments, Inc.^[2] since their speaker verification algorithm, originally developed by Doddington, utilizes this particular preemphasis. If required, the preemphasis function can be modified by non-zero settings of the preamplifier's equalizer (EQ) controls.

A simple active HP filter was synthesized as shown in Figure 3, containing a switch for frequency-independent unity gain when opened. With the switch in closed position the dashed curve is obtained. The solid line represents TI's preemphasis response.

The preemphasis circuit has been integrated with the instrument preamplifier at its output stage.

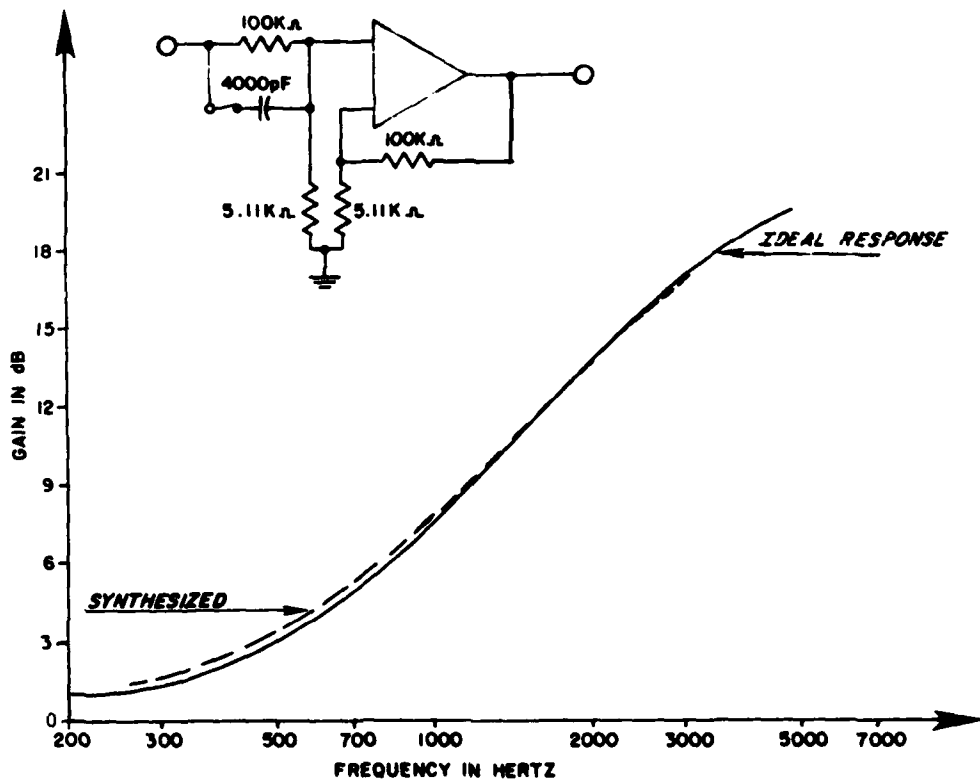


Figure 3. Preemphasis Response and Filter Circuit

EQUALIZER

Some acoustic problems can be reduced or eliminated by equalizers. Small rooms can exhibit resonance points within the speech band and also tend to emphasize higher audio frequencies. Both of these acoustic problems are best reduced by fractional octave equalizers. Division of the audio band into one-third octave ranges is the highest resolution available in commercial equalizers. The N27 graphic equalizer made by Klark-Teknik Research, Ltd., has 27 slide potentiometers for boost or attenuation of 27 filter outputs from 40 Hz to 16 KHz. The wide range provides flexibility to weigh the frequency spectrum both inside and outside the processing band.

THRESHOLD DETECTOR MODULE

The module consists of a comparator circuit and anti-aliasing filter. A photograph of the module is shown in Figure 4; a schematic diagram is presented in Figure 5.



Figure 4. Photograph of Threshold Detector Module

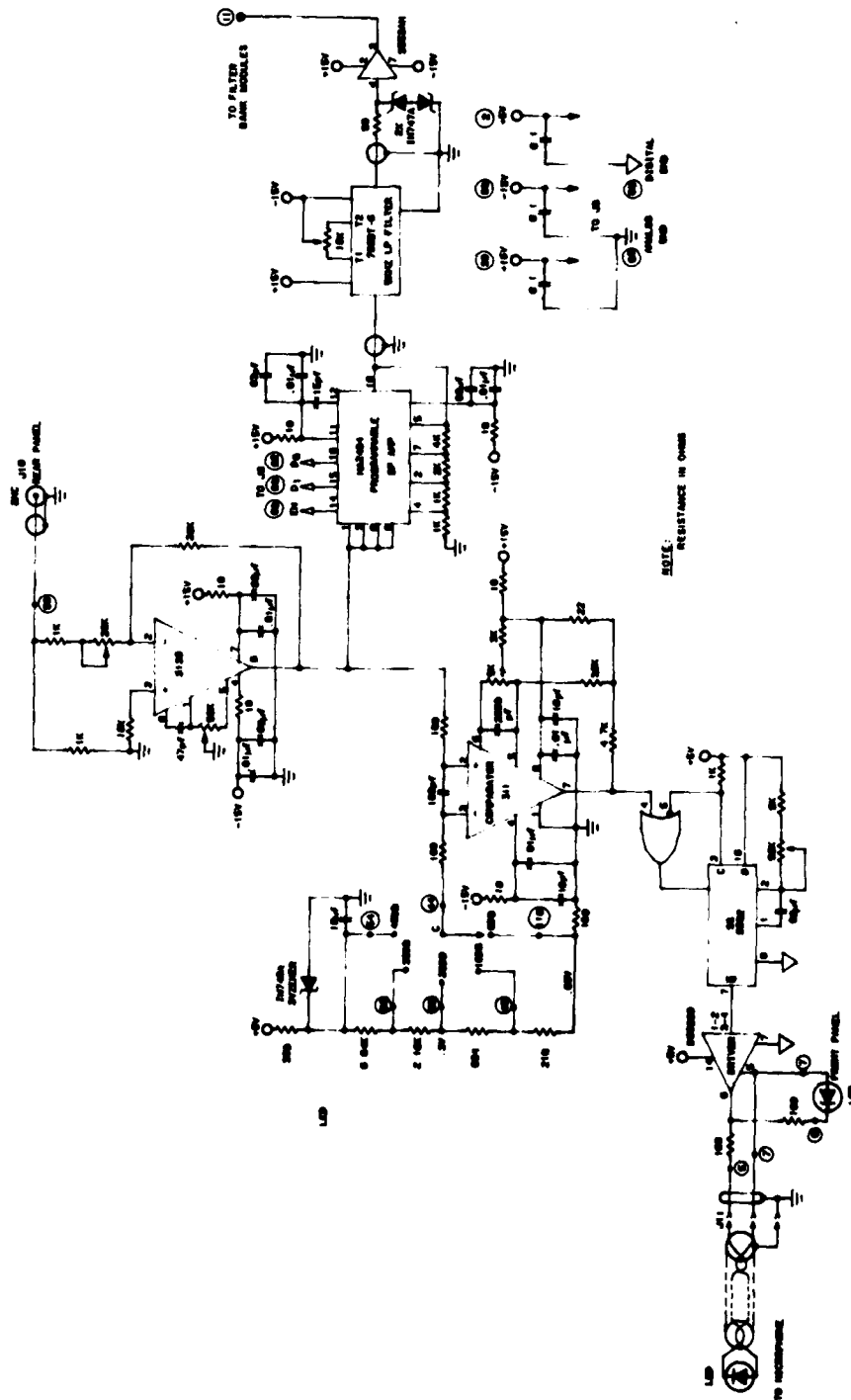


Figure 5. Schematic of Threshold Detector Module

The module has been included into the filter bank bin to improve the signal-to-noise ratio of live voices, since they are accompanied by ambient noises of varying degrees as they enter the microphone.

The idea is to prompt the individual to raise his voice above a predetermined threshold. In order to obtain the speaker's required voice minimum amplitude (signal-to-noise ratio), a green LED lamp is turned on whenever his speech exceeds the threshold. This prompting occurs immediately and does not depend on the algorithm's computed error rates or energy levels registered. On the other hand, the signal level to the filter bank can be adjusted independent of the threshold detector by a computer-controlled programmable op amp; this assures that the signal of each filter channel will stay within a given range (above a minimum level without overflow). Usually, one complete phrase of speech is required before the computer's decision process can be completed and the gain adjustment executed.

Comparator Circuit

Indoor acoustic noise levels typically do not exceed 85 dB (SPL reference 0.0002 dynes/cm²), while the acoustic level of conversation is approximately 45 dB. These levels are the basis for the adjustable voltage reference range of the threshold detector module's comparator. A reference voltage is divided into four 10 dB attenuation steps forming a 0 to 40 dB threshold range by a stepping switch, (see Figure 5). Depending on the noise environment, the operator selects one of the four threshold settings on the front panel.

A single-shot circuit provides the LED on-time, adjustable by a 50 K Ω potentiometer.

Anti-Aliasing Filter

Like CCD filters or digital filters, switched-capacitor (SC) filters are sampled data systems and require low-pass filtering for removal of folding frequencies. Since the ratio of sampling frequency to the upper signal frequency for the SC filter is in general much higher than for any other sampled data systems, the anti-aliasing filter for an SC system is less critical in design.

The Butterworth filter configuration was chosen for its flat passband, reasonably steep transition regions and modest overshoot. It can be shown that an eighth-order filter with a 3 dB bandwidth of 5 KHz has attenuations of ≥ 55 dB for the closest alias frequencies. The required filter was purchased from Frequency Devices, Inc. as Type 790 BT-8-5,000 Hz.

The anti-aliasing filter is followed by a driver for 16 parallel-connected SC band-pass filters which are located in the filter bank modules.

FILTER BANK MODULE

The filter bank module consists of two programmable switched-capacitor filter ICs, four noise filters, four detectors, four lowpass filters and four output LED bargraph displays, as shown in Figure 6.

Programmable Switched-Capacitor Bandpass Filters

Before we proceed, a word about the basics of SC filters. The concept is relatively new; chips actually designed for specific applications first appeared about two years ago. The design and production of programmable switched-capacitor filters by Reticon (EG&G)^[3] marks the entry of a new building block for the filter designer and systems engineer.

The design of SC filters requires the generation of a "resistive" circuit element, a biquadratic system, and orthogonal tuning of poles and Q's. The design of the resistive circuit element employs the switched-capacitor concept (Figure 7). At the time $t = 0$ the capacitor C is charged up to $q(0)$ and at the time $t = t_s$, the charge on the capacitor is $q(t_s)$. Dependent on the value of V_1 and V_2 , a different charge Δq will be added or subtracted with each switching cycle, generating a current $i = \Delta q/t_s$ during the sampling period t_s , or

$$i = C_s(V_1 - V_2)/t_s = C_s\Delta Vf_s \quad (3)$$

and

$$R = \Delta V/i = \frac{1}{C_s f_s} \quad (4)$$

is the "resistor" for a given sampling frequency f_s . The result is a first-order approximation^[4]. This simple fact permits the design of MOS "resistors" for RC products with a minimum of chip real estate and high precision for active filter implementations.

Without trimming, 0.1% accuracy for RC products can be obtained for monolithic ICs due to the capacitance ratio

$$RC = \frac{C}{C_s f_s}, \quad (5)$$

where voltage dependence and temperature coefficients are cancelling.

The use of a biquadratic transfer function in the design of an SC filter is a design convenience. Biquadratic forms have been well investigated for their utility as active

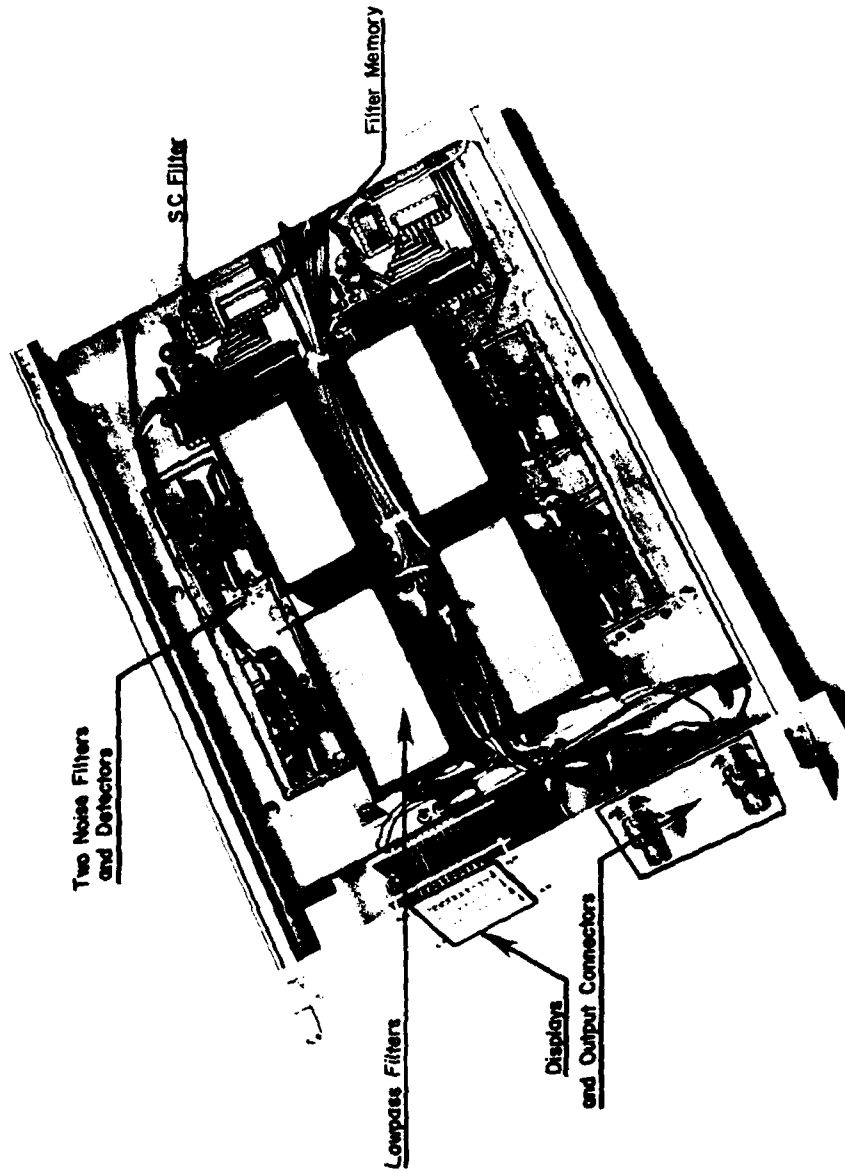


Figure 6. Four-Channel Switched-Capacitor Filter Bank Module

filters and lead to practical filter sections that can be cascaded for higher-order implementations. The universal filter by James Tow^[5] is the most commonly produced (National Semiconductor, Burr-Brown) active filter building block today. It is a three op amp leap-frog approach that is inherently low in sensitivity and permits orthogonal tuning of poles and Q's. Orthogonal tuning is an important requirement for the practicality of the design because only without interdependence of pole frequencies and Q values can multisection filters be aligned without tedious trimming. Orthogonality is mandatory for digitally controlled filters where new filter functions are required on command (real-time).

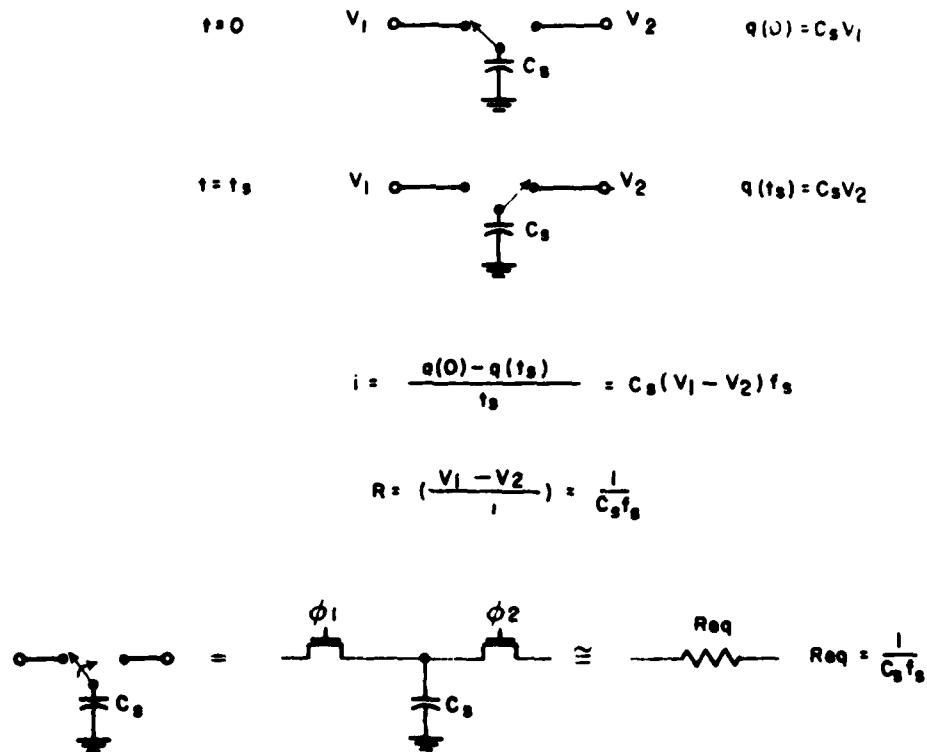


Figure 7. "Resistors" Using Switched Capacitors

Experimental, programmable switched-capacitor filters were chosen as the band-pass filters. Reticon's new VLS integrated circuit R5610 is being fabricated with an NMOS process in limited quantities. This device is able to provide eight poles or pole pairs over the audio frequency range with its associated Q's on a single monolithic chip. It is organized in four filter sections, with one programming logic and a clock divider system, as shown in Figure 8. Serial connection of sections (hard wire) permits the design of filters with even-numbered poles. The poles can be programmed within $\pm 1.1\%$ of their ideal values over seven octaves in frequency. The normalized pole frequency f_o within each octave can be set by command to one of 32 values. It can be shown that

$$f_o = 0.5 \times 1.0226^{(n-1)} \quad (6)$$

with n the "fine tuning" step which can be set to any integer values from one through 32. The octaves are programmed by sampling rate f_s multiplying R commands. If N is the octave, then the value of R is determined by $R = 2^{(N-1)}$. The maximum pole frequency for each octave is $0.0436f_s$. The internally generated sampling rate is actually changed by a binary divider with a maximum division ratio of 256 ($R = 1$) for the lowest octave of operation.

With the external clock frequency f_c given, we can calculate the sampling frequency f_s as

$$f_s = f_c R / 256 \quad (7)$$

The actual pole location f_p can now be derived as

$$f_p = 85.16 \times 10^{-6} f_c R \times 1.0226^{(n-1)}, \quad (8)$$

when operating the R5610 with the recommended clock frequency $f_c = 3.58$ MHz. By setting $R = 1$, we obtain $f_{\min} = 312$ Hz, the lowest pole frequency, and with $R = 128$ and $n = 32$, we obtain 78,020 Hz, the highest pole frequency attainable. Since the frequency range of interest is approximately from 300 Hz to 3 KHz, the R5610 is suitable for the application.

In contrast to the pole locations, we cannot conveniently equate the choice of Q's. Here, the designer has to resort to the published Q table in Reticon's preliminary data sheet[6]. Q's from 0.577 to 50 can be obtained by 32 binary addresses.

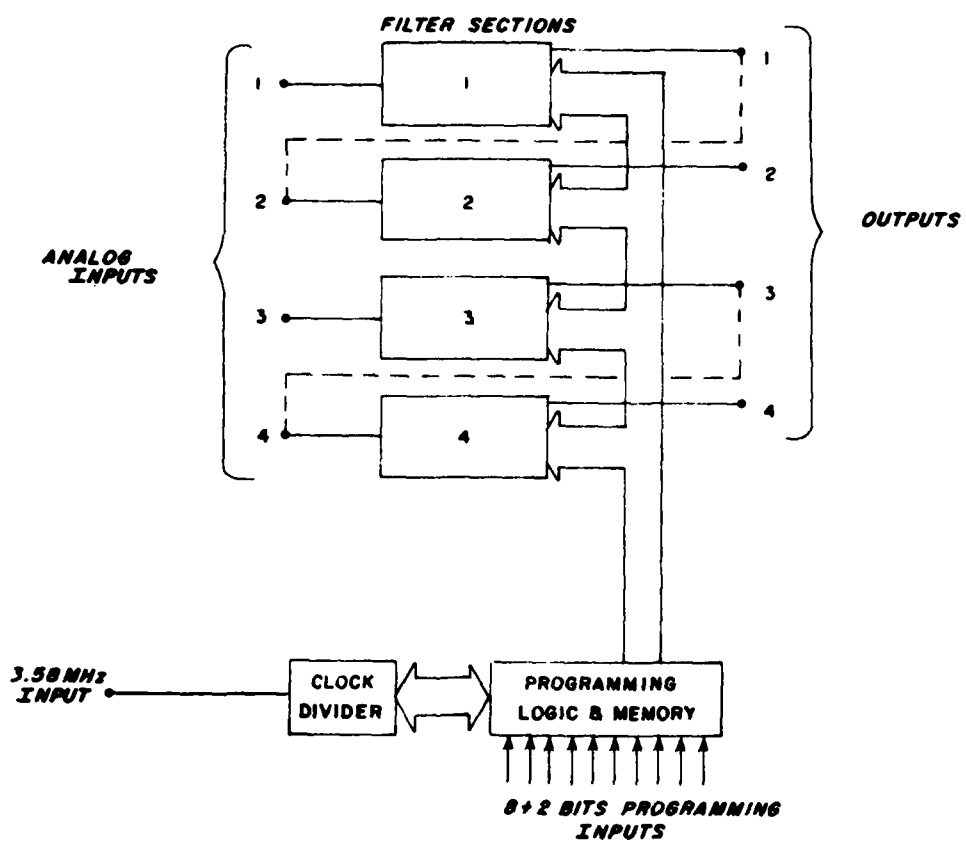


Figure 8. Block Diagram of Real-Time Programmable Switched-Capacitor Filter

The R5610 circuit configuration, Figure 9, is similar to the "universal" active RC-filter topology of a state-variable filter. Here, lowpass and bandpass filters can be implemented, but highpass (HP) filters cannot. There is no reason, however, why future programmable SC filters cannot incorporate HP realizations[4,7].

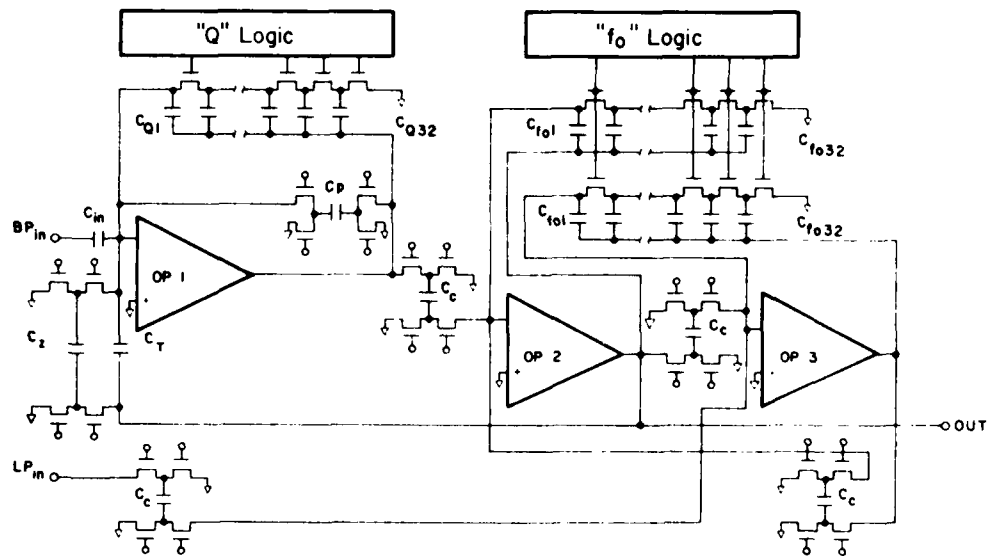


Figure 9. Schematic of One Programmable Switched-Capacitor Filter Section (Source: Reference 3.)

For the design of the fourth-order Butterworth BP filters we wrote a CAD (Computer Aided Design) program incorporating a lowpass-bandpass transformation, Figure 10, using center frequency f_c and bandwidth BW as inputs for the computation of the ideal bandpass pole locations and Q's. With the exact pole locations and Q's printed out, the program asks the operator for pole locations and Q's. Figure 11, which are found in the R5610 data sheet look-up tables closest to the ideal values. In addition, the operator will be asked for sampling rate multiplication factor R. This factor has to be estimated. If this estimation is incorrect, pole locations appear on the printout that are not within $0.5 \leq f_p \leq 1$ and the operator has to repeat the calculations with a better estimate for R. A printout of the f_c gain and the ideal 3 dB points is then provided. If the obtained BW is satisfactory, a simulated filter response plot can be obtained on command after declaration of frequency range and resolution of the requested graph.

```

1.00: SWITCHED-CAPACITOR BP FILTER DESIGN, 4TH-ORDER BUTTERWORTH, BY GUENTHER KNAPP
1.001 TYPE "COMPUTATION OF UPPER AND LOWER 3DB POINT FP AND FS FROM FC."
1.002 TYPE #
1.01 DEMAND FC,BW,R
1.02  $FP=BW/2+SQRT(BW^2/4+FC^2)$ 
1.03  $FS=FP-BW$ 
1.04  $QC=FC+FP/(FP^2-FC^2)$ 
1.05  $A=SQRT(2)/2$ 
1.06  $D=2*A/QC$ 
1.07  $Q=1/D+SQRT(1/2*(4+D^2/2+SQRT((4+D^2/2)^2-4*D^2)))$ 
1.08  $K=A*Q/QC$ 
1.09  $W=K+SQRT(K^2-1)$ 
1.10 TYPE #
1.11  $FOC=FC/(612.18*R)$ 
1.12  $F01=FOC*W,F02=FOC/W,Q=Q$ 
1.13 DO STEP 1.12
1.14 TYPE F01, F02, Q, W
1.15 DEMAND F01F,F02F,QF
1.16 TO PART 2

2.00 TYPE #
2.01 DO PART 5 FOR F=FP
2.02 TYPE "UPPER 3DB(?) GAIN", HF,FP
2.03 DO PART 5 FOR F=FC
2.04 TYPE "CENTER FREQUENCY GAIN IN DB", HF,FC
2.05 DO PART 5 FOR F=FS
2.06 TYPE "LOWER 3DB(?) GAIN", HF,FS, #
2.07 TYPE "DO YOU WANT ME TO PLOT DBPL AS PART 3 ?"

3.00 TYPE #
3.01 DEMAND FMIN, FMAX, INC
3.02 TYPE #, #
3.03 TYPE FORM 1
3.04 TYPE FORM 2
3.05 DO PART 4 FOR F=FMIN:INC:FMAX
3.06 TYPE FORM 2
3.07 TYPE FORM 1

4.00 DO PART 5
4.01  $MN=-22, MX=0$ 
4.02  $DBPL=((HF-MN)/(MX-MN))*2-1$ 
4.03 PLOT -0.909, -0.636, -0.364, -0.091, 0.182, 0.456, 0.727, 1, W, DBPL ON F

5.01  $FP1=FC+F01F/F0C, FP2=FC+F02F/F0C$ 
5.02  $HP1=(FP1+F/QF)/SQRT((FP1^2-F^2)^2+(FP1+F/QF)^2)$ 
5.03  $HP2=(FP2+F/QF)/SQRT((FP2^2-F^2)^2+(FP2+F/QF)^2)$ 
5.04  $HF=20*LOG(HP1*HP2)$ 

```

```

FORM 1
-21DB -18DB -15DB -12DB -9DB -6DB -3DB 0DB

```

```

FORM 2
.....

```

Figure 10. Computer Aided Switched-Capacitor Filter Design Program

```

; FILTER 3, RUN 2
>DO PARTS
PARTS HAS NO VALUE
>DO PART 3

```

```

; FILTER 3, RUN 2
>DO PART 1
COMPUTATION OF UPPER AND LOWER 3DB POINT FP AND FS FROM FC.

```

```

FC=741
BW=220
R=2

```

```

F01= .672453283
F02= -.544698316
Q= 4.78978619

```

```

F01F=.669
F02F=.548
BF=4

```

```

UPPER 3DB(?) GAIN -7.57346952
HF=
FP= 859.120151
CENTER FREQUENCY GAIN IN DB
HF= -4.29146376
FC= 741
LOWER 3DB(?) GAIN
HF= -7.61997208
FS= 439.120151

```

```

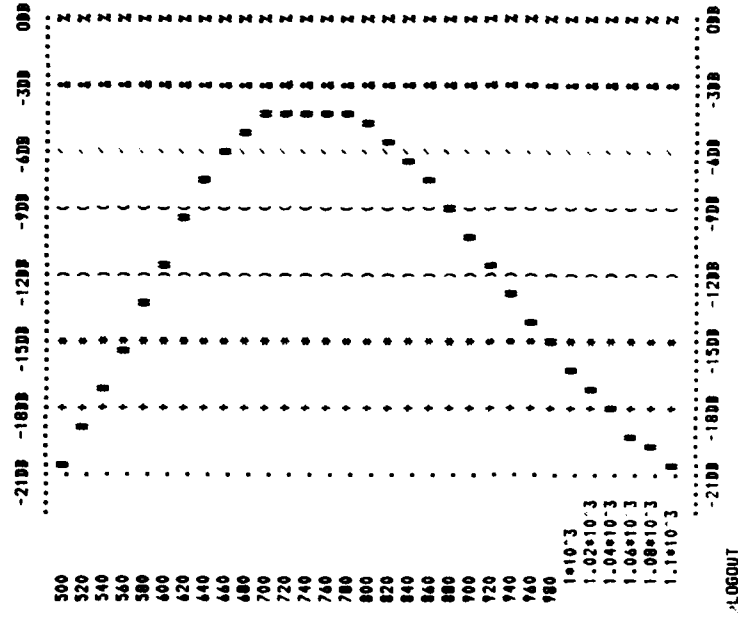
DO YOU WANT ME TO PLOT DBPL AS PART 3 ?

```

```

FRIN=500
FRAX=1100
INC=20

```



CP units: 55.1

Figure 11. Computer Printout of Switched-Capacitor Filter Design Program

After satisfactory simulation of the filter response, the sampling rate, pole locations, and Q 's have to be documented in logic and machine language, Figure 12, for subsequent programming of a filter memory. The compact address structure of the R5610 permits the storage of four fourth-order BP filter responses on one small 32 x 8 PROM, thereby permitting the command execution of two filter programs for each of the two different filters (hardware connected dual sections) in the same unit.

Figure 13 shows the output waveform of a 1 KHz signal in passband of an SC filter. Considerable noise is generated by the sampling process. At low input levels this switching noise buries the signal completely, Figure 14. With $R = 1$, the sampling spectrum contains harmonic frequencies of the 14 KHz sampling frequency, Figure 15. As indicated by (7), the sampling frequency goes up with R , the octave of operation, and therefore (hopefully) the associated sampling spectrum (noise). This is unfortunately not the case: at high sampling rates, noise components far below the fundamental sampling frequencies occur. Figure 16 shows an example for a 2.9 KHz SC filter where a sampling frequency of 112 KHz is required, while output noise components down to 28 KHz are present. The largest noise component, the 3.58 MHz clock frequency, is 10 dB higher than the 14 KHz or 28 KHz peak and is not shown on the photographs.

Noise Filters

Signal recovery can be improved simply by lowpass filtering of the SC filter output. A fourth-order Butterworth LP filter with a 3 dB point at 5.6 KHz was designed at MITRE for this task. This filter has an attenuation of approximately 30 dB at 14 KHz and ≤ 0.05 dB at ≤ 3 KHz. The step recovery is within 0.1 dB in 1 ms. The Sallen-Key unity gain circuit^[8] was selected for its simplicity and its superior low sensitivity to passive element tolerances^[9]. The BP filter was designed in two biquad sections with standard component values for the resistors and capacitors, Figure 17.

Detectors

Detection is accomplished by rectification of the SC filter output waveforms.

Nearly ideal rectification at audio frequencies can be obtained by improving the switching functions of diodes with operational amplifiers as shown in Figure 18.

SWITCHED-CAPACITOR FILTER PROGRAMMING MATRIX

SC Filter No.: 3, 4 Center Frequencies: 741 Hz, 906 Hz

S1	S0	COL2F0/I		Filter P1/P2		Address	Analog Filter Data		D0	D1	D2	D3	D4	S0	S1	F0/I	HEX Data	Remarks
		A2	A1	A0	A0		B7	B6										
0	0	0	1	0	0	2	F01	0.669	0	1	0	0	1	0	0	1		Filter 3 Progr. 1
0	0	0	0	0	0	0	0	4.0	0	1	0	1	0	0	0	0		
0	1	0	1	0	0	10	F02	0.548	1	1	0	1	1	1	0	1		
0	1	0	0	0	0	8	0	4.0	0	1	0	1	0	1	0	0		
1	0	0	1	0	0	18	F03	0.800	0	1	0	1	0	0	1	1		Filter 4 Progr. 1
1	0	0	0	0	0	16	0	5.5	1	0	1	1	0	0	1	0		
1	1	0	1	0	0	26	F04	0.669	0	1	0	0	1	1	1	1		
1	1	0	0	0	0	24	0	5.5	1	0	1	1	0	1	1	0		
1	1	1	0	0	0	28	R	2	1	0	0	0	0	0	0	0		Sampling Rate
0	0	0	1	1	1	3	F01	0.645	1	1	0	0	1	0	0	1		Filter 3 Progr. 2
0	0	0	0	1	1	1	0	4.0	0	1	0	1	0	0	0	0		
0	1	0	1	1	1	11	F02	0.563	0	0	1	1	1	1	0	1		
0	1	0	0	1	1	9	0	4.0	0	1	0	1	0	1	0	0		
1	0	0	1	1	1	19	F03	0.782	1	1	0	1	0	0	1	1		Filter 4 Progr. 2
1	0	0	0	1	1	17	0	5.5	1	0	1	1	0	0	1	0		
1	1	0	1	1	1	27	F04	0.654	1	1	0	0	1	1	1	1		
1	1	0	0	1	1	25	0	5.5	1	0	1	1	0	1	1	0		
1	1	1	0	1	1	29	R	2	1	0	0	0	0	0	0	0		Sampling Rate

32 x 8 PROM #: 3, 4 SERIES: B DATE: 1/23/81 NAME: S.K.

Figure 12. Example of Programming Matrix for Fourth-Order Butterworth Bandpass Filter

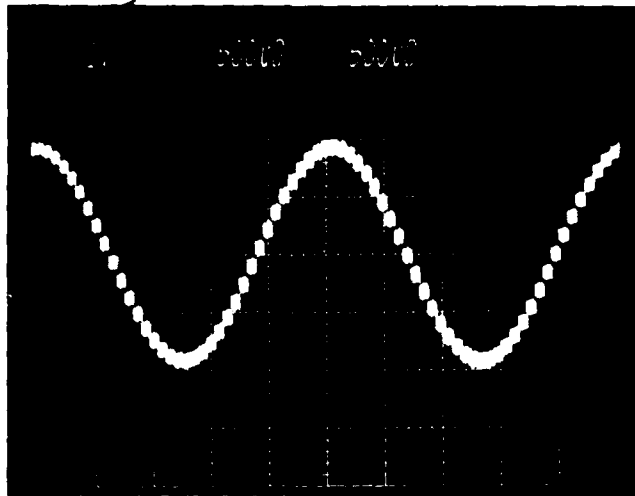


Figure 13. Sampled Data Output Waveform of Switched Capacitor Filter

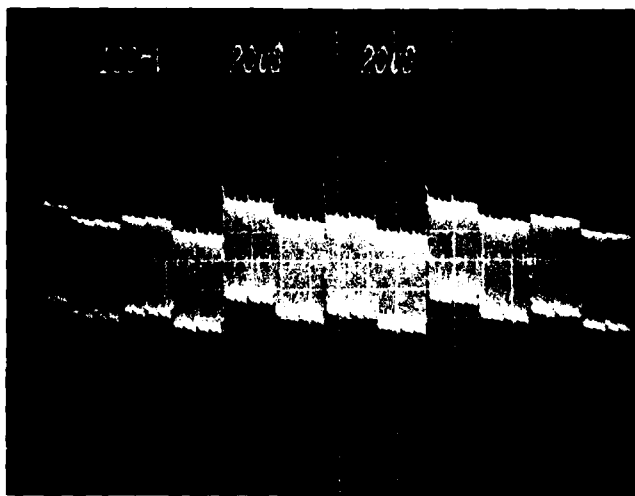


Figure 14. Sampling Noise at Output of Switched-Capacitor Filter

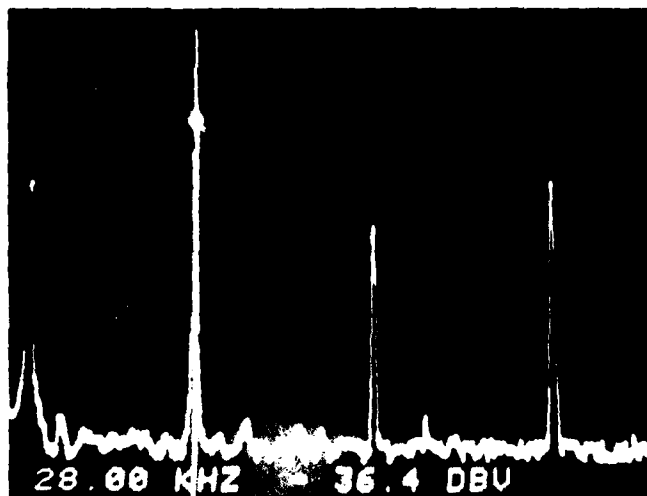


Figure 15. Sampling Spectrum of 410 Hz Switched-Capacitor Filter

Horizontal Scale: 10 KHz/Division

Vertical Scale: 20 dB/Division

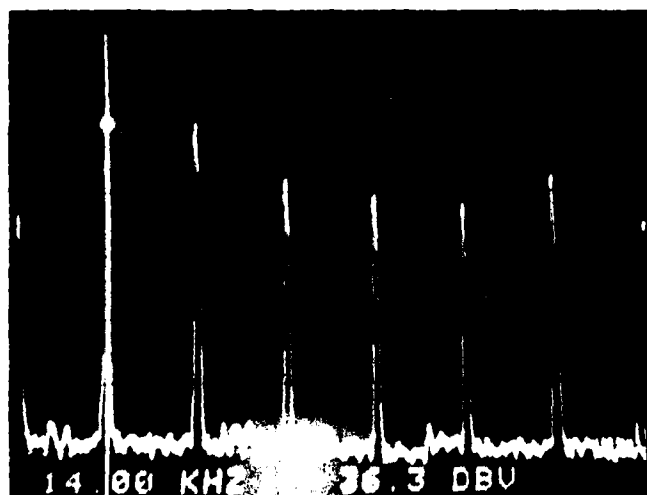


Figure 16. Sampling Spectrum of 2,900 Hz Switched-Capacitor Filter

Horizontal Scale: 10 KHz/Division

Vertical Scale: 20 dB/Division

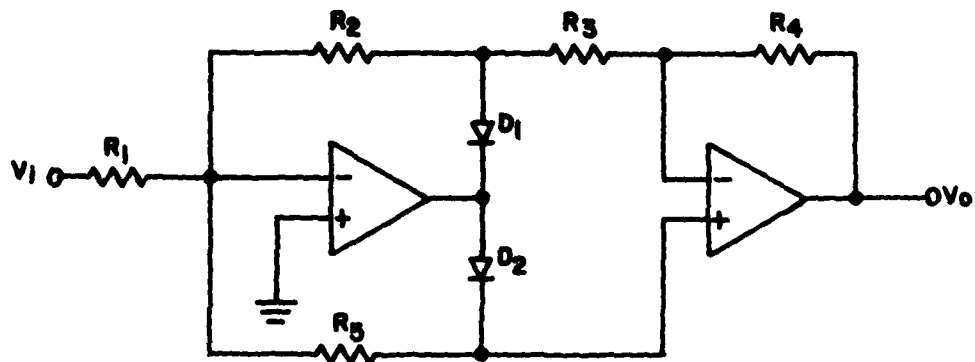


Figure 18. Absolute Value Detector Circuit

With ideal op amps in the circuit we can state, for input voltages $V_i(t) \geq 0$ with diode D_1 conducting, the gain of the circuit as

$$g_1(t) = \frac{R_2 R_4}{R_1 R_3} \quad (9)$$

For $V_i(t) < 0$ with diode D_2 conducting the gain is

$$g_2(t) = \frac{R_5(R_2 + R_3 + R_4)}{R_1(R_2 + R_3 + R_5)} \quad (10)$$

For equal gains of negative and positive input voltages we set $R_2 = R_3 = R_4 = R_5 = R$ and obtain for (9) and (10)

$$G(t) = R/R_1 \quad (11)$$

In a practical circuit the gains can be equalized conveniently by adjustment of R_5 .

Low-noise and low-offset voltage operational amplifiers are needed for a large dynamic range. We measured a dynamic range of 70 dB with LF 347A op amps in the circuit. The linearity error over a range of 60 dB was found to be within ± 0.1 dB, including the noise filter we designed.

Lowpass Filters

It is well known that most of the speech power spectrum lies below 20 Hz. For the removal of spectral components above 20 Hz, a fourth-order Bessel lowpass filter

was selected for its phase linearity and flat step response. Since no programmable low-frequency SC filters were commercially available, tunable active filters, Type 740 LT-1 from Frequency Devices, Inc., were purchased. (These rather large units can be identified on Figure 6.) The bandwidth of the filters are adjustable from 0.1 to 50 Hz by four fixed resistors for each filter. For the filter bank modules the LP filters were adjusted to a 20 Hz, 3 dB bandwidth.

Displays

The output of each filter channel is monitored by a bar graph display with ten LED segments. The control and drive system is available as a commercial part in a single IC from a number of manufacturers. The control system was adjusted with external resistors for a full-scale reading of 30 dB in 3 dB steps. On the front panel, close spacing of the 16 displays provides a rough pictorial presentation of the real-time voice spectrum.

PROGRAM CONTROL MODULE

The program control module contains the address generator and the clock system, Figure 19. The module serves as a controller for the execution of filter program selections, Filter Program 1 (FP1) or Filter Program 2 (FP2), either by computer (PROGRAM) or manually by switch.

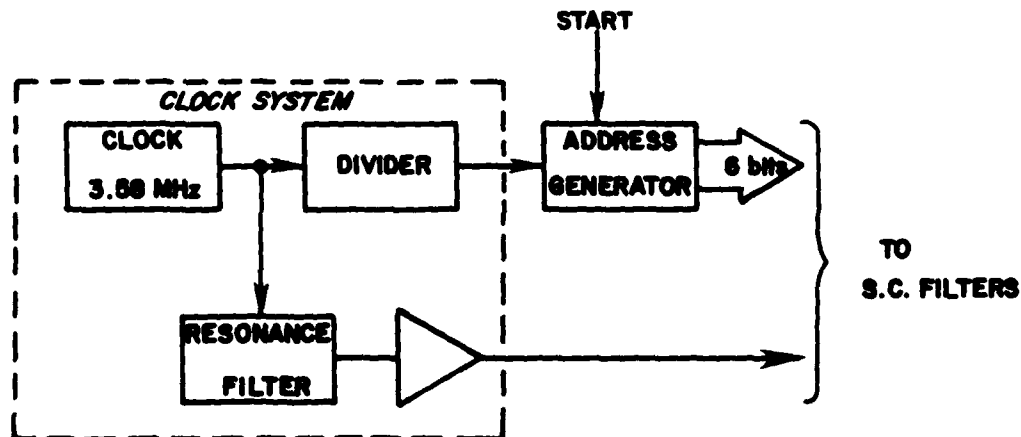


Figure 19. Block Diagram of Programming Control System

Clock System

For operating and programming the SC filters, a clock system is required. The timing signal for the address generator is derived from a 3.58 MHz, 5 V clock by binary division.

The SC filters (R5610) require a sinusoidal clock signal of 3.58 MHz for generation of sampling frequencies. A high Q tuned tank serves as a filter for the fundamental frequency and as a voltage step-up transformer. An output voltage of 6 V peak-to-peak is obtained by impedance transformation with a capacitive divider. The output amplifier drives four cables of 93 Ω impedance, one for each filter bank module.

Address Generator

Programming of the SC filters is accomplished by addressing their PROMs in parallel. The addressing format is a sequence of six parallel bits, as shown in Figure 20. Three bits carry specific categories of filter information and three bits are responsible for the execution of the information transfer (loading) of the filters. Figure 21 shows the circuit diagram of the programming control system. The sequence is stored in two 256 x 4 PROMs that are addressed by two binary counters for 41 counts. Sequence initiation takes place by a pushbutton on the front panel and the sequence is completed with the 41st count, which turns the LED on as indication for the completion of the sequence and memory transfer from filter PROMs to the SC filters. At the same time, the start FF and binary counters have been reset and the clock input is disconnected from the counters.

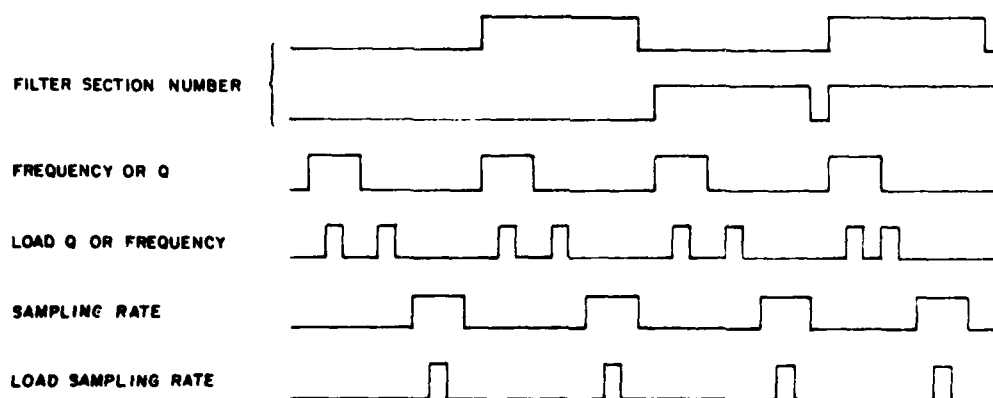


Figure 20. Filter PROM Address Sequence

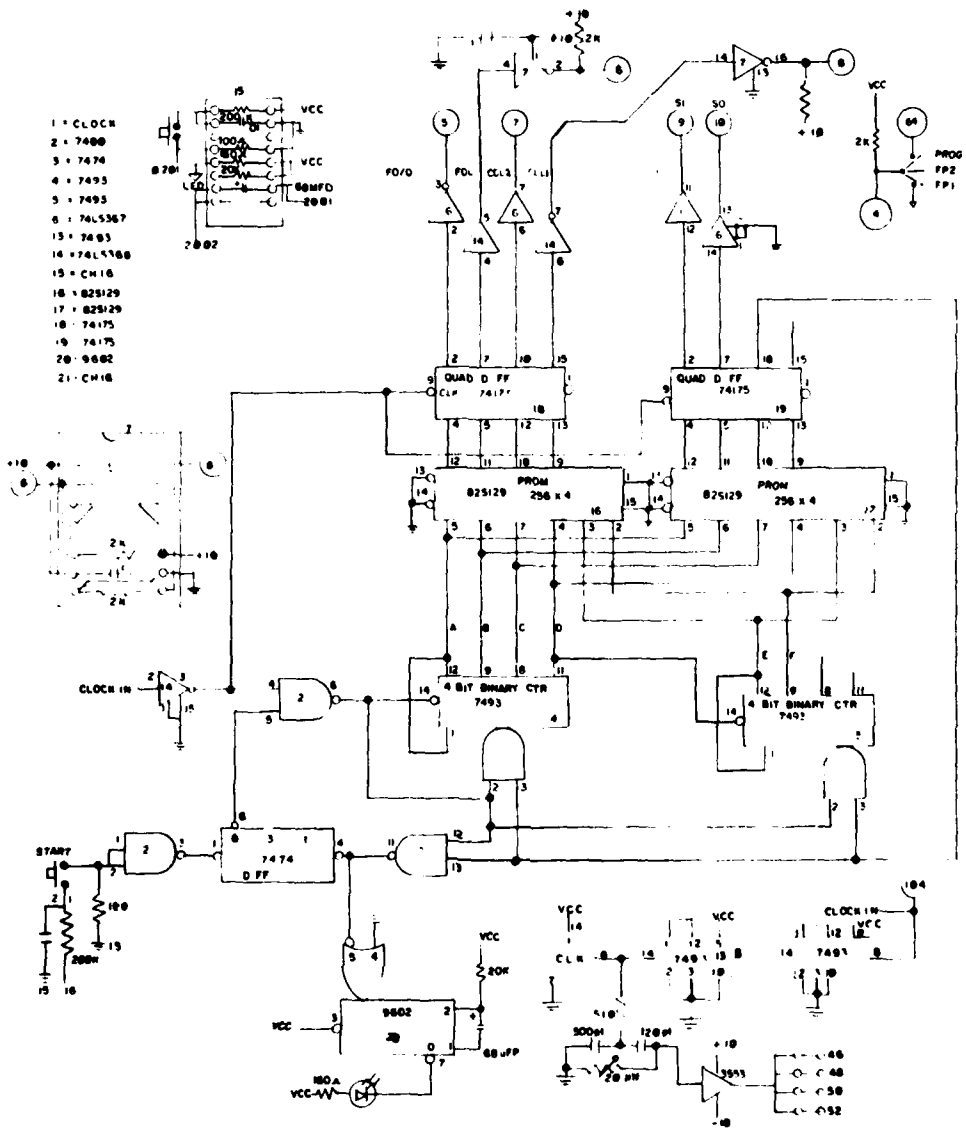


Figure 21. Programming Control Schematic

DATA ACQUISITION MODULE

For data processing of the 16 analog channels, multiplexing, gain normalization and analog-to-digital conversion is required. The block diagram of this data acquisition system is shown in Figure 22 and the completed module in Figure 23.

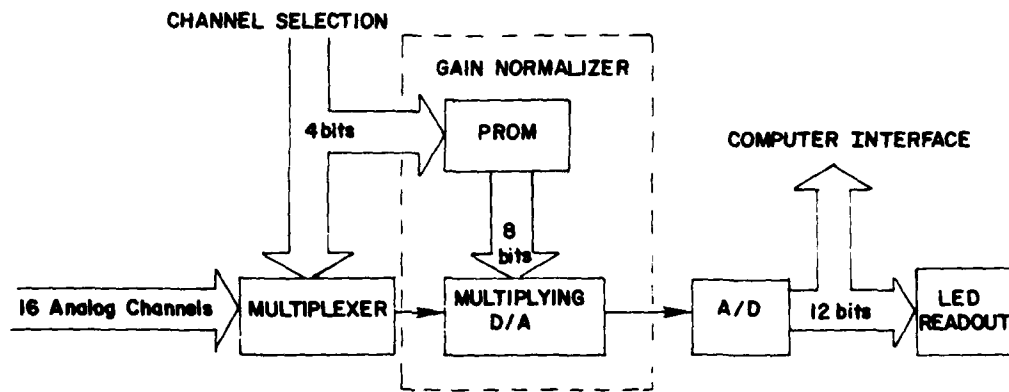


Figure 22. Block Diagram of Data Acquisition System

Multiplexer and Analog-to-Digital Converter

An integrated hybrid system manufactured by Analog Devices, Inc., Type AD363, fulfills the basic functions for data acquisition: multiplexing with sample and hold in the AIS (Analog Input Section) and parallel analog-to-digital conversion by the ADC (Analog-to-Digital Converter) section. The AD363 is a complete 16 channel, 12-bit data acquisition system in integrated circuit form. By applying large-scale linear and digital integrated circuitry, thick and thin film hybrid technology and active laser trimming, the AD363 equals or exceeds the performance and versatility of previous modular designs. The two units require a minimum of external circuitry for their operation. Figures 24 and 25.

Each analog input (channel) has a lowpass filter for reduction of noise pick-up. Channel selection is executed by computer or manually by four switches on the front panel of the module. Their upper "program" position, Figure 23, engages the computer control. For test purposes, the lower two switch positions permit the selection of binary addresses for operation of single channels.

The analog-to-digital converter section of the AD363 contains a complete 12-bit successive approximation analog-to-digital converter, including internal clock, precision 10 volt reference, comparator, buffer amplifier and a proprietary-design 12-bit D/A

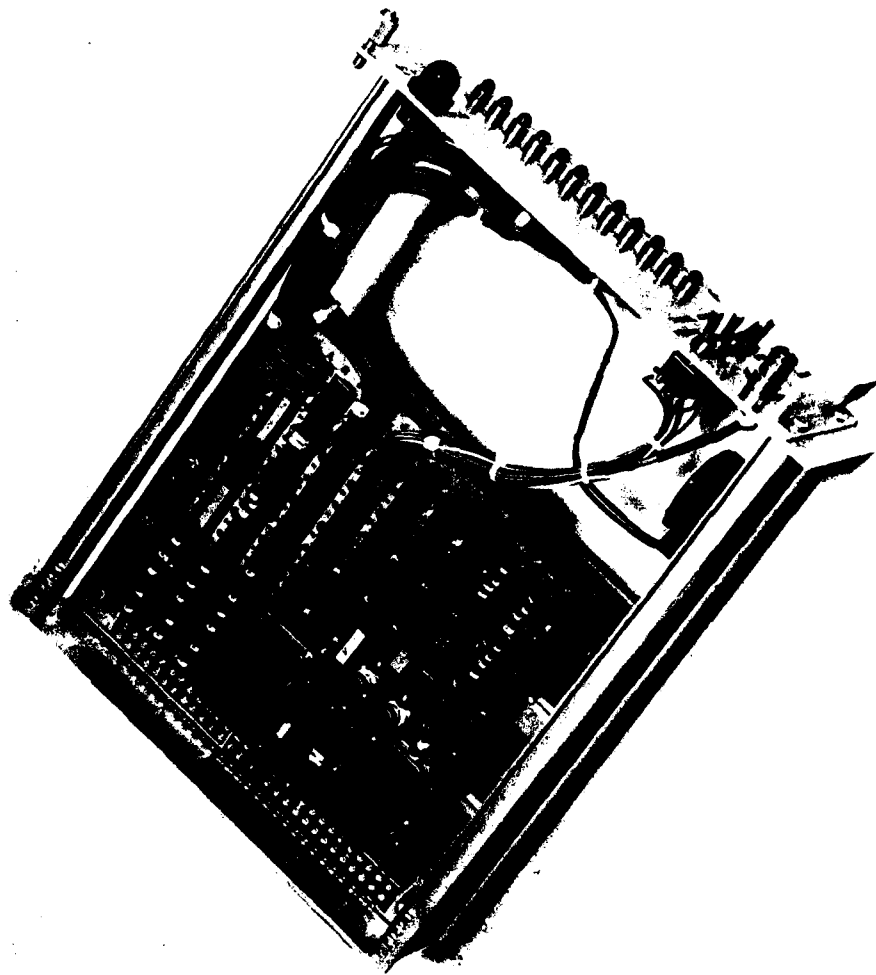


Figure 23. Data Acquisition Module

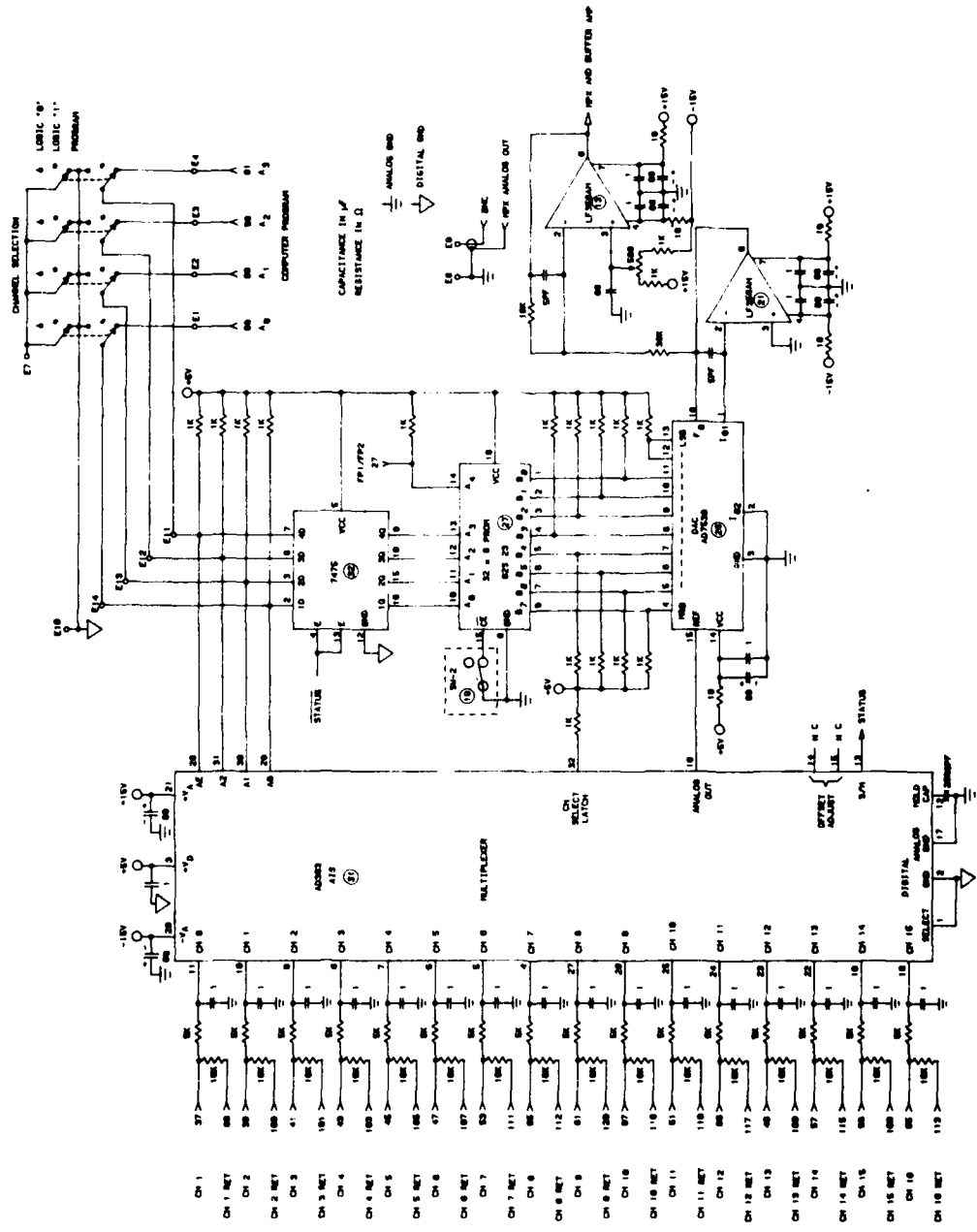


Figure 24. Multiplexer and Gain Normalizer of Data Acquisition System

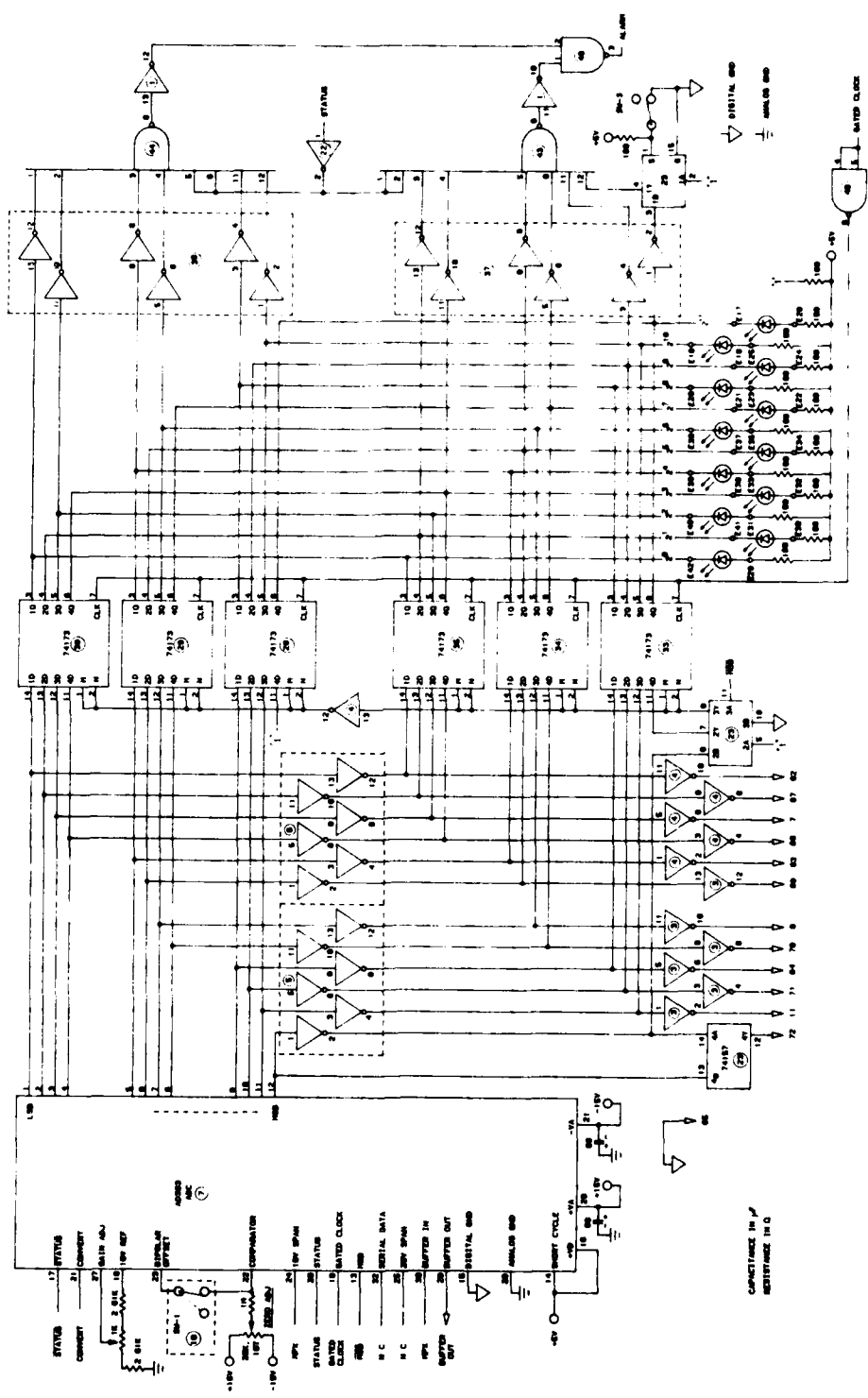


Figure 25. Analog-to-Digital Converter Section of Data Acquisition System

converter. Active laser trimming of the reference and D/A converter results in maximum linearity errors of $\pm 0.012\%$ while performing a 12 bit conversion in 25 microseconds. The combined maximum processing time of multiplexer section, gain normalizer and A/D converter section is approximately 600 microseconds. This processing speed leaves an adequate safety margin for the expected ≥ 10 ms/frame (one frame equals the processing time of 16 channels) average interrogation speed of the computer.

Gain Normalizer

The multiplexer and A/D converter are interconnected by an amplification normalizing circuit for the adjustment of unequal channel gains. This gain variation from channel to channel occurs due to the finite programming steps of the SC BP filters and gain tolerances in each channel. For certain SC BP filters, a further variation of pole and Q values was required in order to obtain a reasonable overall filter bank response without gaps or excessive overlap of the filter characteristics. In other words, a perfect Butterworth response could not be maintained for all SC BP filters in the bank.

Moreover, filter transfer functions in general do not have unity gains; insertion losses increase with the order of the filter.

The gain normalizer provides centralized gain adjustments for all channels by a 32 x 8 PROM and an 8-bit multiplying digital-to-analog converter, Figure 24. Gain information is stored in the PROM which is addressed by a 4-bit channel address and a 1-bit filter program (FP1/FP2) address. The 8-bit range of gain control provides an 0.05 dB resolution of adjustment, since less than 10 dB of interchannel gain differences need to be corrected.

SECTION 3

TEST RESULTS

The filter bank channels were tested with an audio sweep generator. The obtained LP filter outputs were plotted by an x-y recorder. Figure 26 shows two fourth-order Butterworth BP filter responses programmed on the same chip and operating at two different amplitude levels. The four filter sections of the SC chip are: 0, 1, 2 and 3. Very close tracking of both filters is evident. Even the non-linearity at maximum amplitude levels (≈ 1.4 V) is identical. This measurement was repeated with separate chips, Figure 27, and the result, except for an 0.05 dB passband change, was the same. Repeating this measurement with the other filter section yielded the same results. Only two R5610s were tested in this way which is not sufficient to draw the conclusion that these devices can be fabricated with such remarkable uniformity.

Frequency responses of the filter bank, Figures 28 and 29, show the uncorrected and normalized filter responses. Data for two filters have been stored in the memories. Both responses are fourth-order Butterworth with an approximate 3 dB bandwidth of 220 Hz. The lines identified as FPI are the original filter responses with center frequencies as shown in Table 1, beginning at 410 Hz and ending at 2559 Hz with frequency spacings of 165.33 Hz between each center frequency^[10].

Table 1
Center Frequencies of Switched-Capacitor Filter Bank

Filter Number	Center Frequency (Hz)
1	410
2	575
3	741
4	906
5	1071
6	1237
7	1402
8	1567
9	1733
10	1890
11	2063
12	2228
13	2394
14	2559

In the plots on Figures 28 and 29 generated by FP2, the poles of the filters are shifted by one programming step, reducing each pole frequency by 2.2%. (Due to the end of the pole programming range only one pole in each filter section was shifted for filter 14.) All other parameters are the same. For the normalized plots of Figure 29, all FP2 filters were reduced in amplitude by 1 dB by the normalizer for calibration purposes.

For good signal resolution, much care was taken during the design phase in avoiding ground loop problems and power supply hum. With the 12-bit A/D converter calibrated for 1 V full scale and a sampling rate of 100 Hz, we found the maximum peak-to-peak noise superimposed on the uncorrupted signal in the two least significant bits (LSBs) at the output of the data acquisition system. We can express the maximum signal-to-noise ratio in dB by

$$S/N = 20 \log_2^{(B-b)} + 20 \log(12)^{1/2}, \quad (12)$$

where $B = 12$ is the range of the A/D converter and $b = 2$, the peak-to-peak noise.

Equation (12) can be simplified and the maximum S/N ratio be calculated.

$$S/N = 6.02(B-b) + 10.8 = 71 \text{ dB}. \quad (13)$$

Since the processed speech is subject to statistical variations, headroom must be left to prevent clipping on peaks larger than the average rms amplitudes of each channel. Considering a 50% head room as satisfactory, 6 dB has to be deducted from the result of Eq. (13), reducing the S/N ratio to 65 dB.

Testing with voices was limited. Only two voice samples, a female and a male, were taken. The results, ten milliseconds of the sound ə as in ago, were displayed on a memory oscilloscope and photographed, Figure 30. Each white square represents a preprocessor channel output. For both speakers three format frequencies (channels) are clearly identified.

R5610 PROGRAMMED FOR BUTTERWORTH RESPONSE
FILTER 1

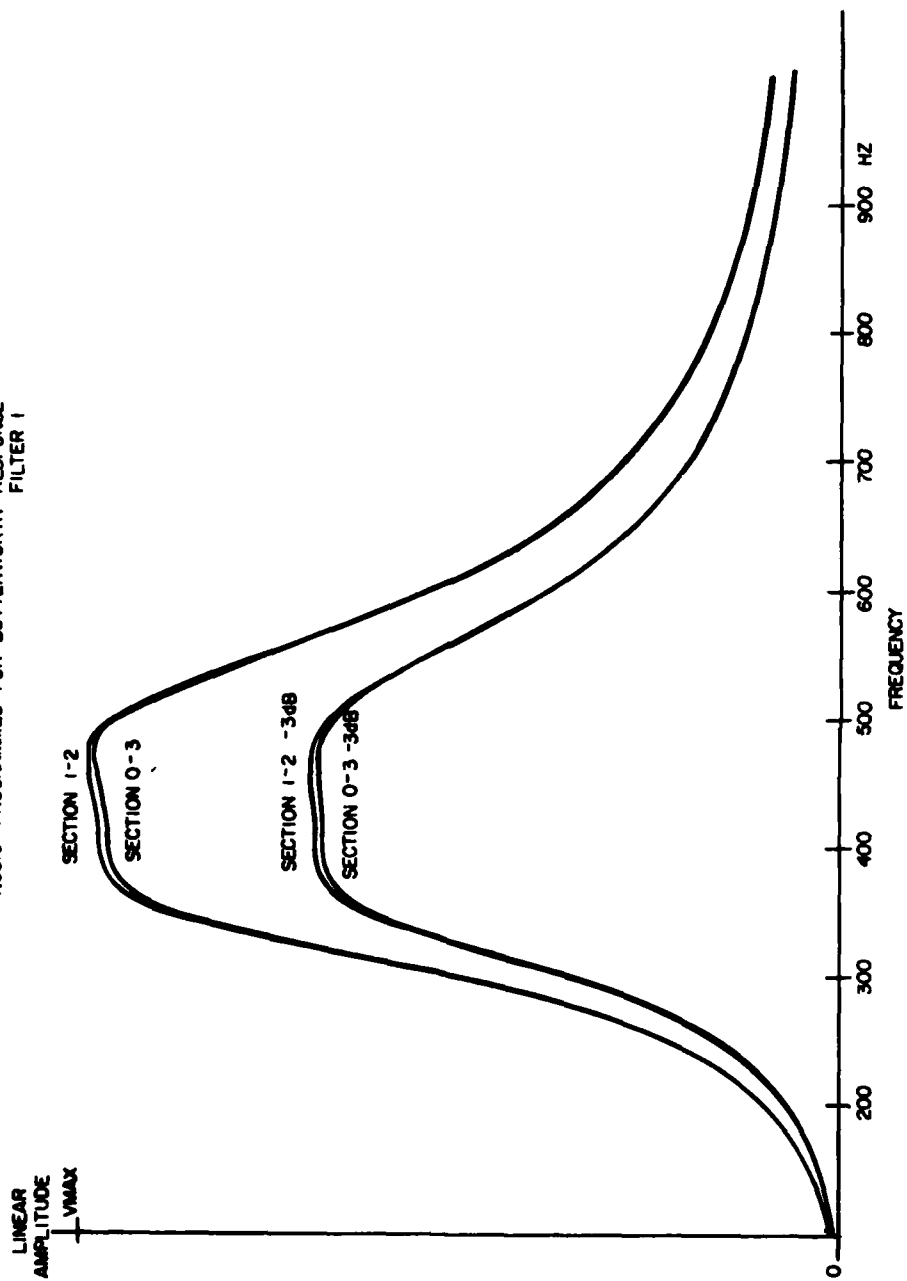


Figure 26. SC Filter Sections of the Same Chip Programmed for Two Identical BP Filters

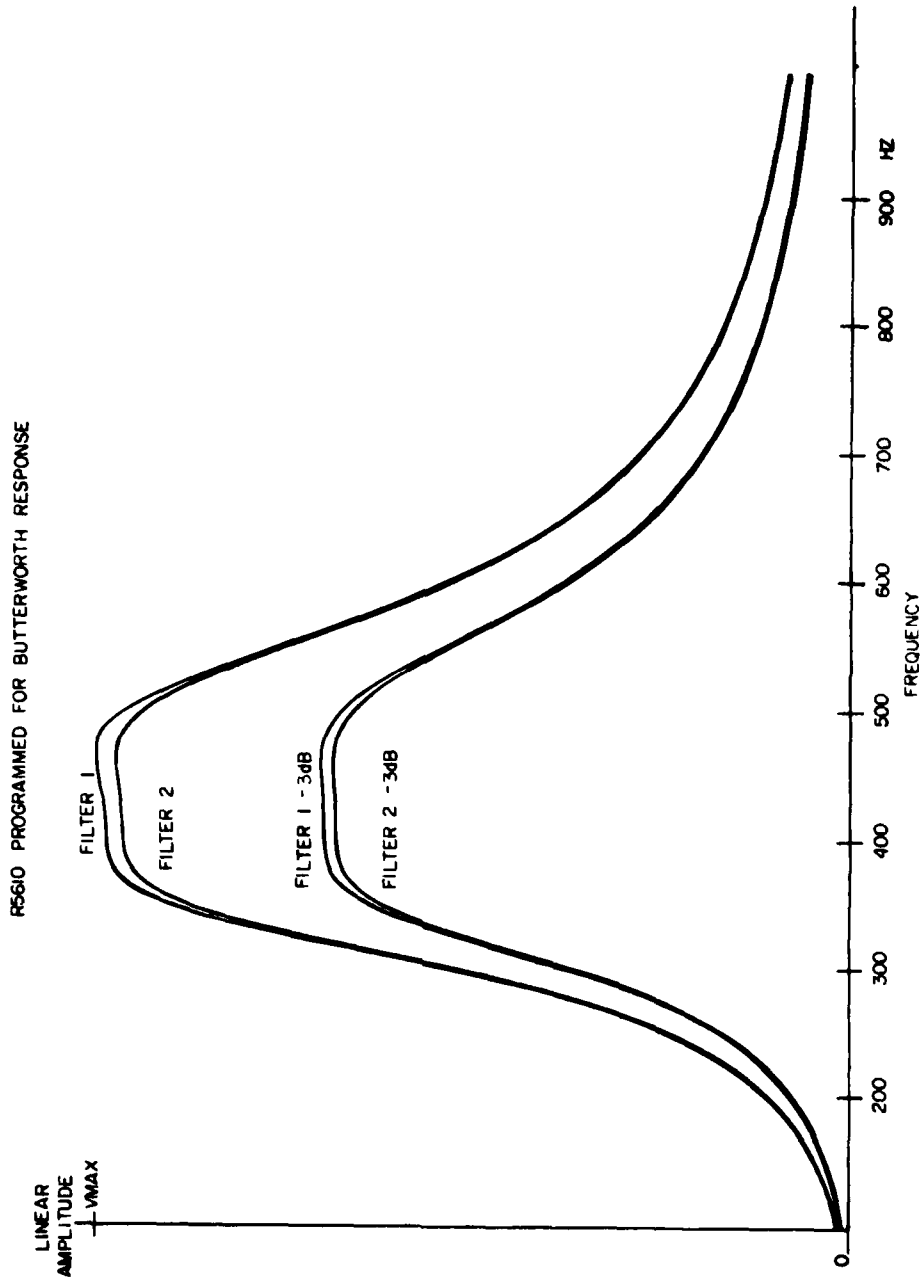


Figure 27. Two Separate SC Filter Chips Programmed for Two Identical BP Filters

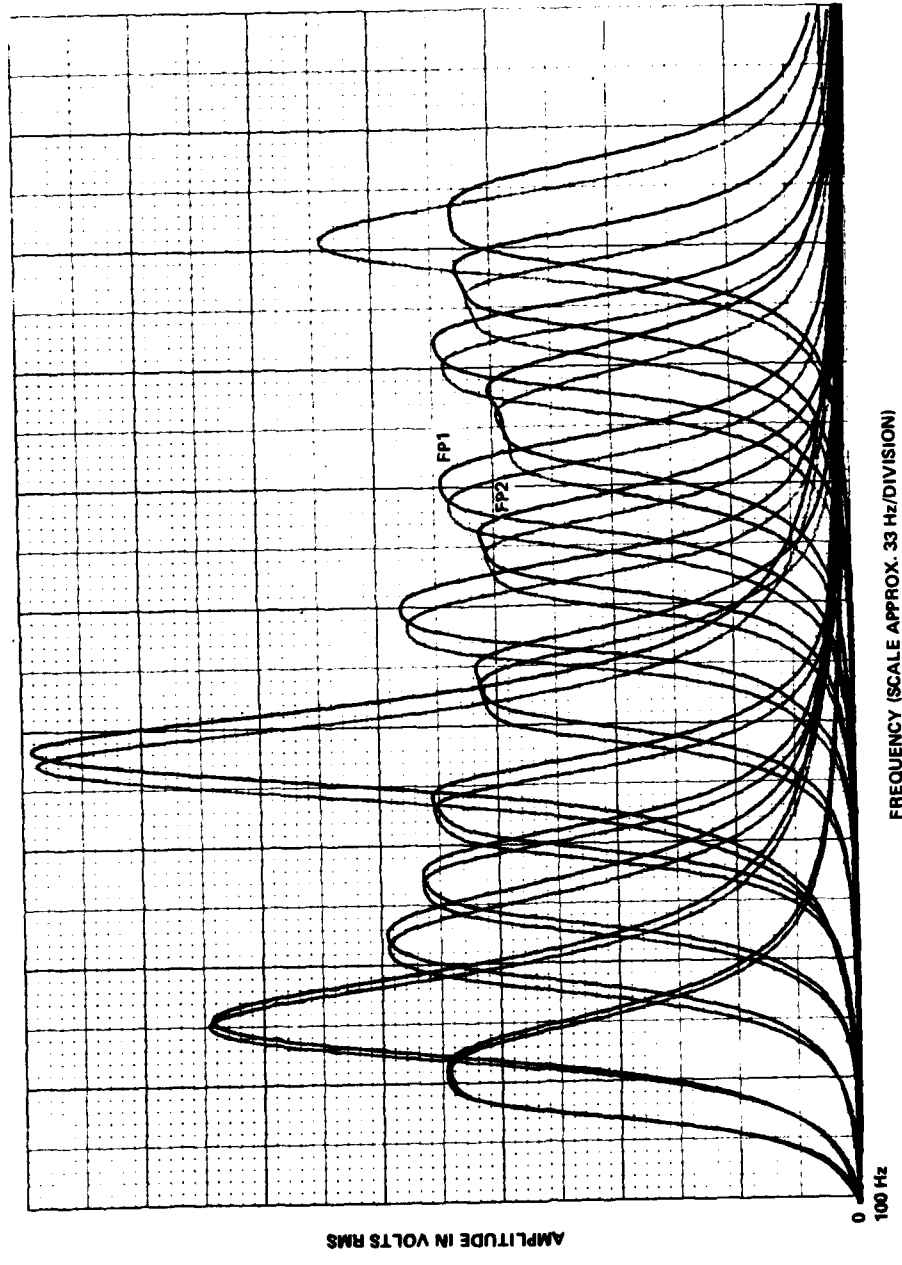


Figure 28. Frequency Response of Switched-Capacitor Filter Bank

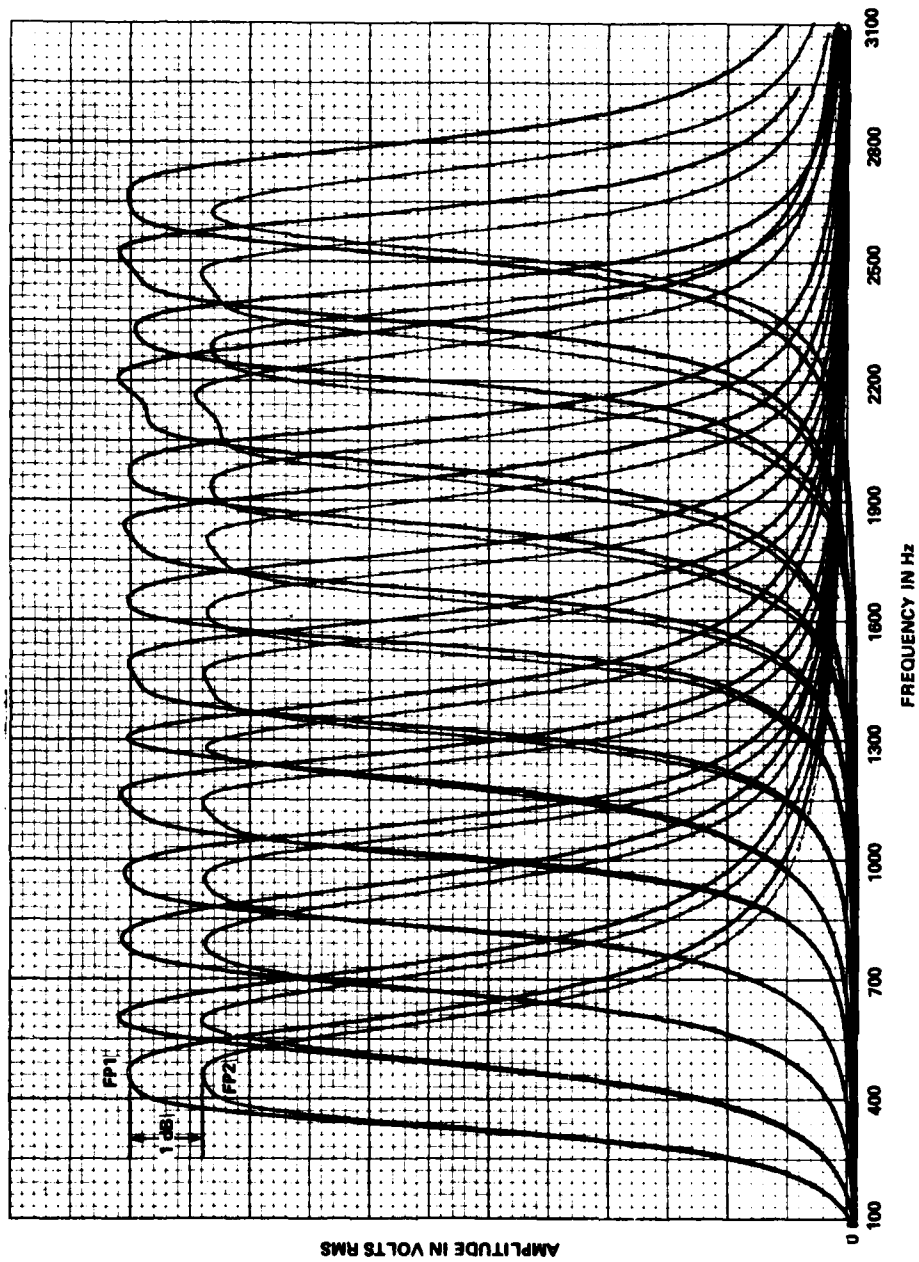


Figure 29. Normalized Frequency Response of Switched-Capacitor Filter Bank

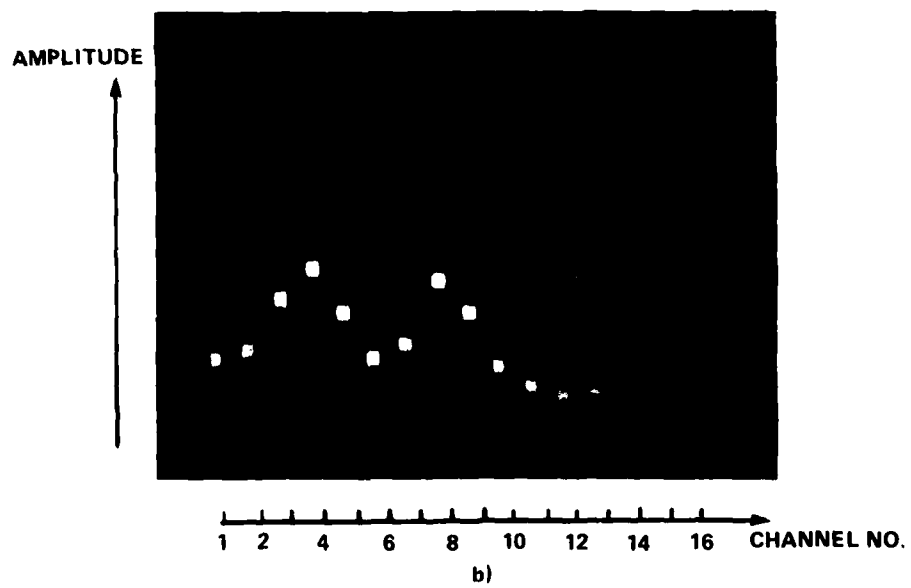
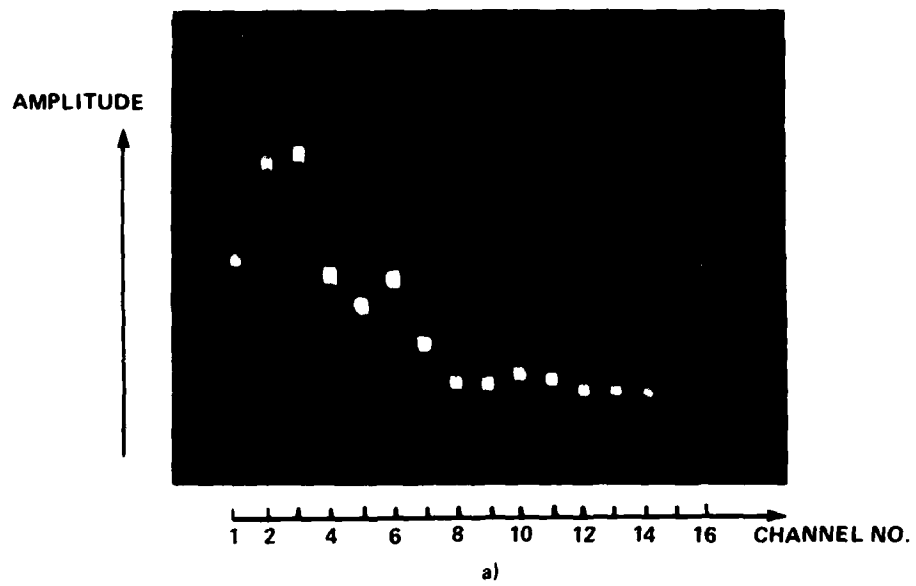


Figure 30. Ten Millisecond Segment of the Sound \Rightarrow Spoken by a Male, a), and Female, b)

SECTION 4

SUMMARY AND CONCLUSION

We designed, implemented and partially tested a speech preprocessing system utilizing programmable, monolithic switched-capacitor filters for spectrum analysis. This approach simplifies real-time analysis systems where many filters of different responses are parallel connected (filter banks). Filter channels can be exchanged and altered since software or PROM data alone specifies the individual filter. Although the filter characteristics are required in logic code, *signal filtering does not require analog to digital and digital to analog conversion.*

Presently, the accuracy of the units is limited to a moderate precision by the finite steps of programming. However, repeatability of characteristics between filter units and sections seems to be excellent for the implemented fourth-order Butterworth bandpass responses.

The processing system includes a 16-channel, 12-bit data acquisition system for serial processing and serves as computer interface.

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