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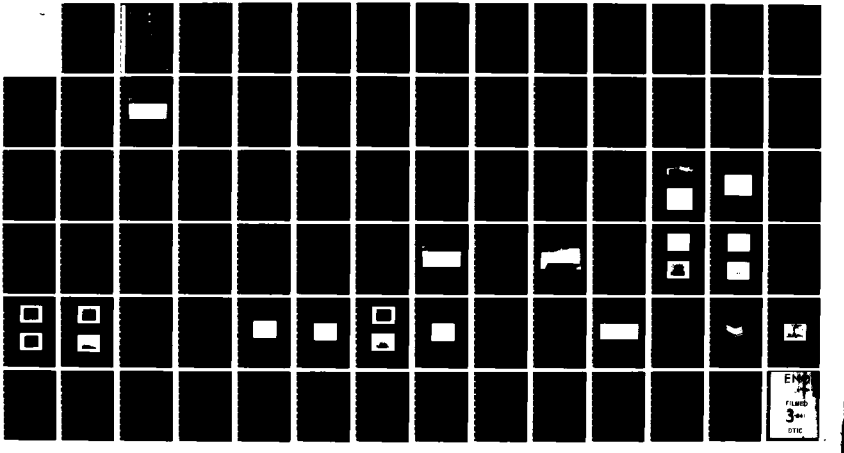

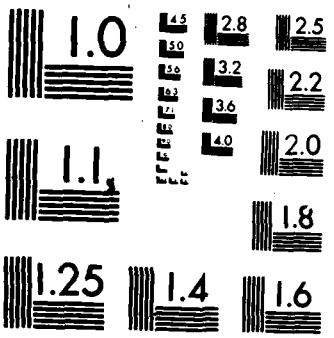

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DEFENCE RESEARCH ESTABLISHMENT OTTAWA

THE SAMPLING AMPLIFIER (U)

DREO REPORT NO. 863

by

L.J. Conway and S.L. Bouchard

JUNE 1982
OTTAWA
P.N. 310

Canada

RESEARCH AND DEVELOPMENT BRANCH

DEPARTMENT OF NATIONAL DEFENCE
CANADA

DEFENCE RESEARCH ESTABLISHMENT OTTAWA

DREO REPORT NO. 863

THE SAMPLING AMPLIFIER (U)

by

L.J. Conway and S.L. Bouchard

Radar Countermeasures Section
Electronic Warfare Division

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ABSTRACT

The current trend to higher and higher signal processing speeds in radar, communication and EW systems is well known. The flexibility offered by sampling techniques for carrying out these processing functions is also widely recognized. To provide high effective sampling rates, a novel distributed parallel sampling approach using relatively narrow-band parallel channels has been developed at DREO. This unique integration of delay lines, sampling gates and amplifiers allows for amplification of wideband r.f. signals at frequencies far above the cut-off frequencies of the amplifying devices used.

A discussion of the distributed sampling concept, the design of a prototype circuit and a comparison of theoretical and experimental results, demonstrating successful signal amplification approaching the gigahertz regime, are presented in this report. Other potential application areas which are well matched to this type of processing are also mentioned.

RESUME

La tendance actuelle d'utiliser des vitesses de traitement de signaux de plus en plus élevées dans les systèmes radar, de communications et d'alerte avancée est bien connue. On reconnaît également largement la souplesse offerte par les techniques d'échantillonnage pour le traitement de ces signaux. Afin d'obtenir un taux d'échantillonnage très élevé, le CRDO a mis au point une nouvelle méthode d'échantillonnage distribué en parallèle, utilisant des voies parallèles de largeur de bande relativement faible. Cette intégration unique de lignes de retard, de portes d'échantillonnage et d'amplificateurs permet l'amplification de signaux RF à large bande à des fréquences bien supérieures aux fréquences de coupure des dispositifs amplificateurs utilisés.

Le rapport présente une discussion du principe de l'échantillonnage distribué, la conception d'un prototype de circuit et une comparaison des résultats théoriques et expérimentaux démontrant la réussite de cette méthode d'amplification de signaux proches des gigahertz. Il mentionne également d'autres domaines possibles d'application correspondant bien à ce genre de traitement.

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LIST OF SYMBOLS

B	bandwidth
c	speed of light (3×10^{10} cm/sec)
C	input intrinsic capacitance of the amplifier
C_o	output intrinsic capacitance of the amplifier
D.U.T.	device under test
G	overall system gain
G_o	final output filter gain
G_n	amplifier-filter network gain
h	microstrip dielectric substrate thickness
N	number of parallel channels
R_{si}	resistance of the input sampling gate under a forward bias (ON) condition
R_{in}	input resistance of the amplifier
R_m	termination resistance
R_o	series source resistance in the amplifier's output model network
R_l	output load resistance
R_{so}	resistance of the output sampling gate under a foward bias (ON) condition
R_l'	parallel combination of the output load resistance (R_l) and $R_m/2$
R_s	diode's forward bias resistance
R_b	sampling gate's bias resistance
R_L	effective load resistance which the sampling gate sees

LIST OF SYMBOLS (CONT'D)

S^*	input sensitivity level
t	microstrip conductor thickness
T_s	meander line propagation delay time between adjacent channels
T'	total meander line propagation delay time between the 1st and Nth channel
T_{se}	effective meander line propagation delay time between adjacent channels
t_p	pulse line propagation delay time between adjacent channels
t_λ	propagation delay time per unit length in microstrip
$\tan\delta$	dielectric loss tangent
V_b	sampling gate bias voltage
V_s	input r.f. voltage
V_o	output r.f. voltage
W	microstrip strip conductor width
W_e	effective microstrip strip conductor width
Z_o	characteristic impedance of the meander line
ε_r	dielectric constant
ε_{eff}	effective dielectric constant
τ_1, τ_2	input and output sampling pulse widths
τ_{eff}	effective output signal pulse width
α	total dissipative losses in microstrip
α_d	substrate dielectric loss
α_c	microstrip conductor loss

LIST OF SYMBOLS (CONT'D)

α_L	pulse desensitization factor
Ω	ohms
σ	conductivity of the material
μ_o	free space permeability
υ	mhos
λ_o	free space wavelength

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1.0 INTRODUCTION

1.1 Introduction

The development of the sampling amplifier based on a distributed sampling technique is described. This is a new concept for wideband microwave amplification in which microstrip meander delay lines, picosecond sampling gates and video amplifiers are the key components. Using this scheme, voltage samples of a wave distributed along a delay line are taken at a number of points on the line. These voltages are subsequently amplified by low frequency (video) amplifiers and then resampled onto an output delay line, reconstructing the input signal at an amplified level.

The attractive aspects of the distributed sampling concept include the following potential characteristics:

(a) very wideband amplification

(b) electrically linear input, hence no intermodulation products with simultaneous signals

(c) parallel construction for redundancy and gradual degradation, and

(d) solid state low frequency components for low cost and ruggedness.

Potential applications include:

(a) wideband microwave amplification

(b) microwave signal storage

(c) signal analysis, and

(d) frequency conversion.

To prove the feasibility of the distributed sampling concept the prototype device of Fig. 1.1 was developed, thereby successfully demonstrating

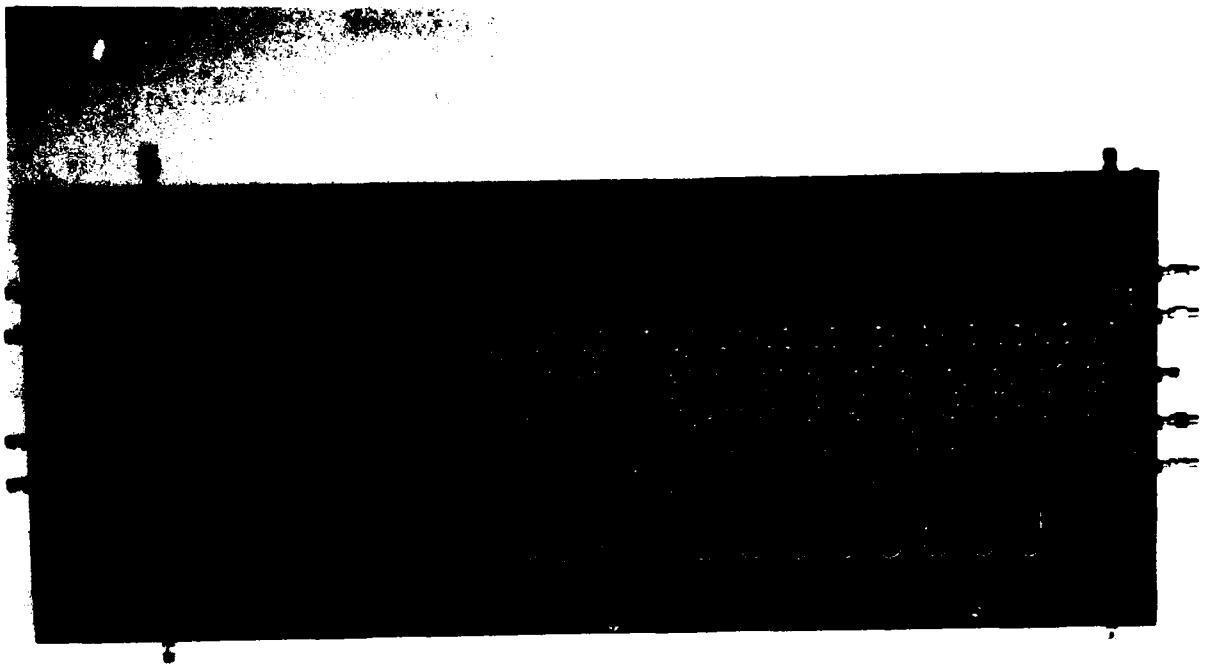


FIGURE 1.1 - TWENTY CHANNEL PROTOTYPE SAMPLING AMPLIFIER

the concept of wideband amplification by providing 11 dB of gain over the band from dc to 840 MHz.

1.2 Background and Objective

Sampling techniques which permit amplification of wideband signals using lowpass narrowband amplifiers were first reported by Lathi [1] and subsequently by Tucker, Conway and Bouchard [2]. These techniques allow the acquisition, amplification and reconstruction of wideband signals.

With present r.f. amplifiers limited to octave bandwidths (with some covering up to two octaves) the wideband characteristic of the sampling amplifier was found to be a very desirable feature for a number of applications, since large portions of the frequency spectrum may be covered with a single device. Moreover, its multi-signal handling capability is in itself very attractive as a multitude of signals are able to be reproduced exactly without the generation of intermodulation products.

Overall long term goals of 0-16 GHz bandwidths with 40 dB of gain, -30 dBm of sensitivity and output power levels of 1 watt CW are envisioned using this technology.

The remainder of this report describes the sampling amplification process in greater detail and reports on the results obtained from an experimental device.

2.0 SYSTEM DESCRIPTION

2.1 Introduction

The basic operation of the sampling amplifier is presented in this section. The theory which models the distributed sampling approach has been previously described in reference [3]. The primary equations defining the

theoretical overall system gain, frequency response and maximum output power are summarized enabling a comparison of theoretical and experimental values.

2.2 Basic Operation

A block diagram of the sampling amplifier is shown in Fig. 2.1. An r.f. signal is received at the input to the sampling amplifier and is distributed in time along the input meander delay line. At this point a signal is initiated by the control unit to activate the input pulse generator. The pulse generator in turn activates each of the samplers thereby obtaining samples of the signal at the various points along the line. These sampled voltages (which are video signals at this point) are then stored on the capacitor elements which act as analog memories. The stored samples are subsequently amplified by the video amplifier units producing amplified signal samples at their outputs. The amplifiers having responded, enable the control unit to initiate a signal activating the output pulse generator which subsequently "turn on" each of the output samplers. This allows each of the amplified input signal samples to be reconstructed on an output delay line. The output sampled waveforms then propagate in both directions on the output delay line where they are terminated at one end and transmitted at the other. The output low pass (passive) filter element eliminates any of the high frequency components which result from the sampling process. Total reconstruction of the input signal requires that the control unit initiate a signal at a rate equal to the inverse of the delay time of the meander delay line.

This unique integration of delay lines, sampling circuitry and video amplifiers provides the capability to receive, store, amplify and retransmit complex wideband radio frequency signals at frequencies far above the frequency cut-off characteristics of the amplifying devices used.

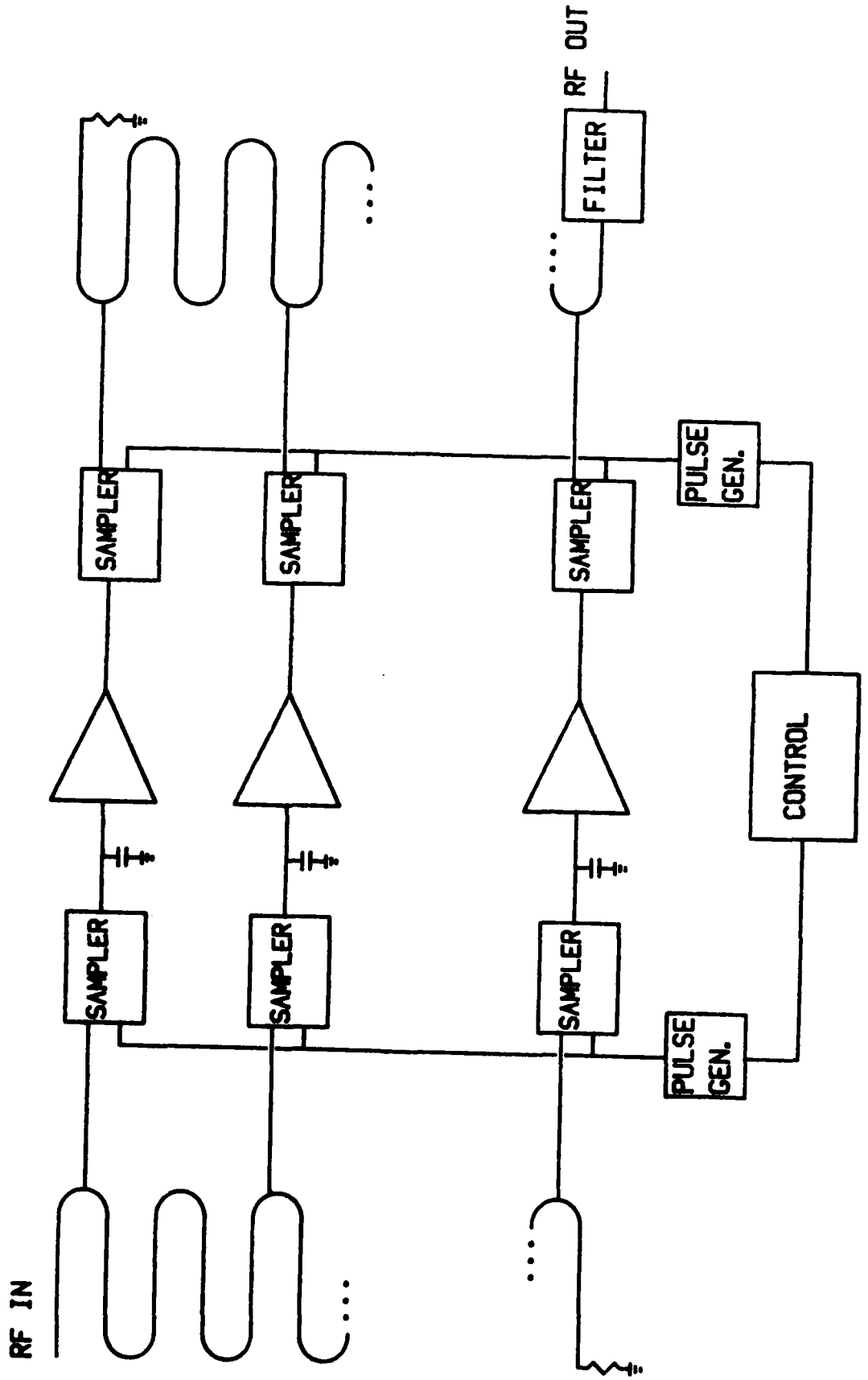


FIGURE 2.1 - BLOCK DIAGRAM OF THE SAMPLING AMPLIFIER

2.3 Mathematical Description

The basic equations defining the overall system gain, frequency response and maximum output power, which were developed in reference [3], are summarized, thereby affording verification of theoretical values with those obtained from an experimental circuit.

A single channel of the sampling amplifier system may be modelled as in Fig. 2.2, where v represents the applied open circuit voltage, R_i is the series source resistance and is equal to R_m, R_m is the termination resistance, z_o is the characteristic impedance of the delay line and is equal to R_m, R_{si} is the equivalent series resistance of the input sampling network, v_{ji} is the voltage appearing at the input to the amplifier network, C and R_{in} are the intrinsic capacitance and input resistance of the amplifier circuit, G_n is the open circuit gain of the amplifier, R_o is the output series source resistance, C_o is the intrinsic output shunt capacitance, R_l is the output load resistance (R_l is necessary to ensure stability of the amplifier when the output sampling gate is reverse biased), R_{so} is the equivalent series resistance of the output sampling network and G_o is the gain of the output passive filter. In this case, the intrinsic capacitance of the amplifier serves as the analog memory.

The overall system gain for the sampling amplifier can be expressed as [3]

$$G = G_n(2B/N)G_o(2B)\tau_1\tau_2[2K_1[1 - e^{-K_2\tau_1}]K_3[(K_4 - K_5)e^{-K_6\tau_2} + K_5]] \quad (2.1)$$

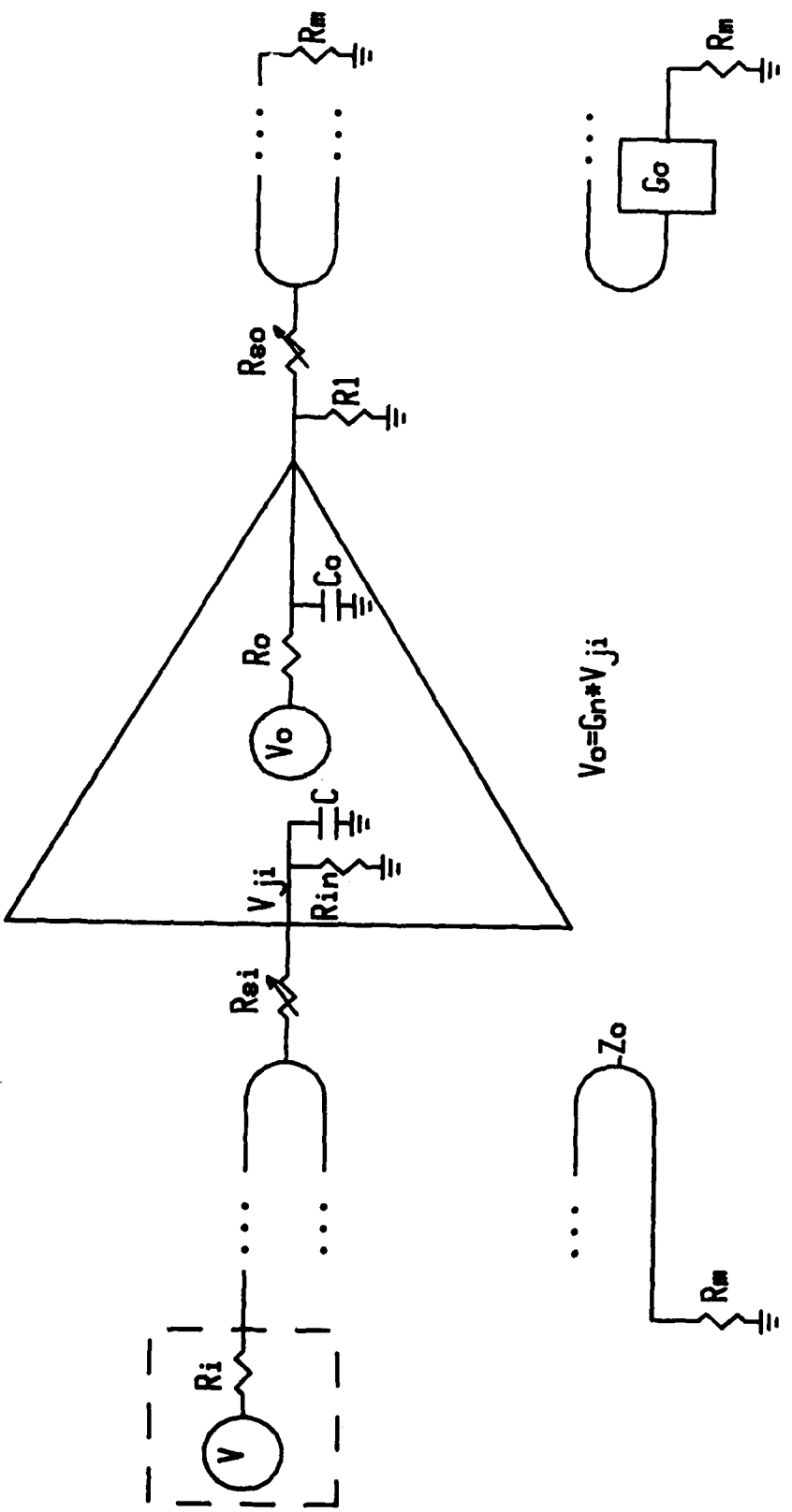


FIGURE 2.2 - MODEL OF A SINGLE CHANNEL OF THE SAMPLING AMPLIFIER SYSTEM

where

$$K_1 = \frac{R_{in}}{2R_{si} + 2R_{in} + R_m}$$

$$K_2 = \frac{1}{K_1(2R_{si} + R_m)C}$$

$$K_3 = \frac{R_m}{2R_{so} + R_m}$$

$$K_4 = \frac{R_1}{R_o + R_1}$$

$$K_5 = \frac{R_1'}{R_o + R_1'}$$

$$K_6 = \frac{R_1' + R_o}{R_1' R_o C_o}$$

$$R_1' = R_1 \| [R_{so} + (R_m/2)]$$

and where τ_1 and τ_2 are the input and output sampling pulse widths, respectively.

The upper limit on the bandwidth (B_{max}) that can be amplified by the sampling amplifier is determined by the pulse width of the output sampling pulse and is given by [3]

$$B_{max} = 1/2\tau_2. \tag{2.2}$$

The maximum output power $(P_o)_{max}$ is dependent on the sampling network. For the sampling gate of Fig. 2.3 the maximum power is expressed in terms of the bias voltage, V_b, the bias resistance, R_b, the load resistance which the sampling gate sees, R_L, and the equivalent series resistance of the sampling gate, R_s. This maximum output power is given by

$$(P_o)_{max} = \frac{R_L}{2} \cdot \left[\frac{2R_s R_b V_b}{(2R_b + R_s)[(R_s + 2R_1)(R_s + R_b) - 2R_L R_b]}\right]^2 \tag{2.3}$$

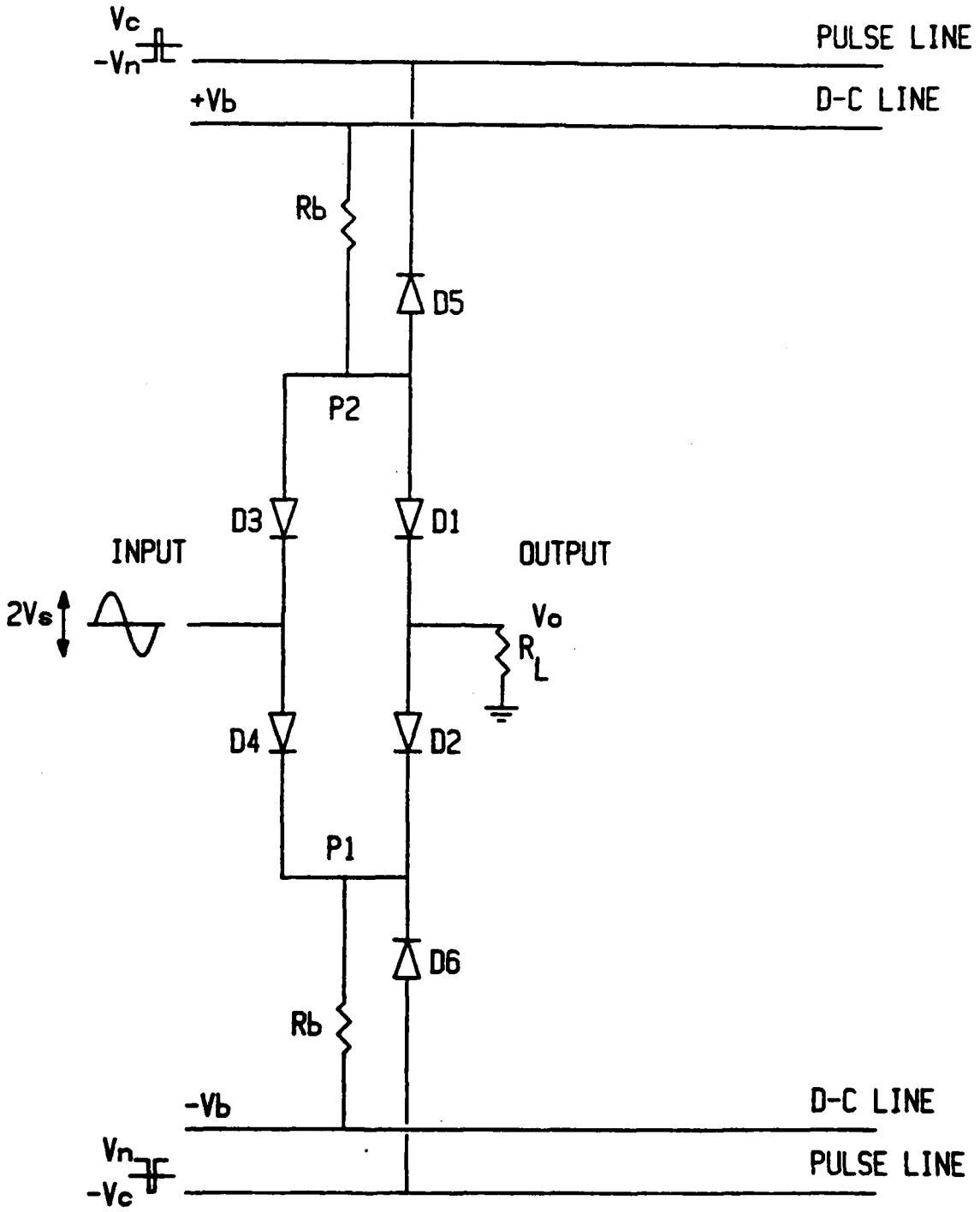


FIGURE 2.3 - DIODE SAMPLING GATE

3.0 DESIGN OF A PROTOTYPE SAMPLING AMPLIFIER

3.1 Introduction

To demonstrate the concept of wideband r.f. amplification using the distributed sampling technique, an experimental prototype device was developed. The physical characteristics of the proposed system, its design goals and the design of the meander delay line are described. The selection of suitable sampling gate, amplifier and pulse generation units are also examined.

3.2 Experimental Circuit

The physical characteristics of the prototype circuit are shown in Fig. 3.1. Regions (1), (4)-(7), (12)-(15) and (18) are constructed in microstrip using RT/duroid 5880 material. Again, line (1) carries the input signal to be sampled and element (2) serves to terminate the input meander delay line. When a sampling pulse is generated at the input to transformer (10) complementary pulses are produced at the output of the transformer. These complementary pulses travel down line (4) and (5) to "turn-on" the sampling gates (3) for a brief period of time. The inductors (8) and capacitors (9) serve to d.c. shift the output sampling pulses to aid in voltage biasing the sampling gates. Lines (6) and (7) also provide voltage bias for proper operation of the sampling gates. Once the input signal is sampled, the sampled waveforms are amplified by the amplifier circuits (11). These amplified waveforms are subsequently applied to the output delay line (18) through the output diode switch (16) at predetermined positions which are similar to the input tap positions. This reconstructed wave then propagates down the delay line (18) to its output. Element (17) is a termination resistor for the output delay line. Lines (12) and (13) correspond to the output pulse lines and lines (14) and (15) provide the voltage bias lines for the output sampler units. The transformer (21) provides the complementary output sampling pulses when triggered by a sample pulse.

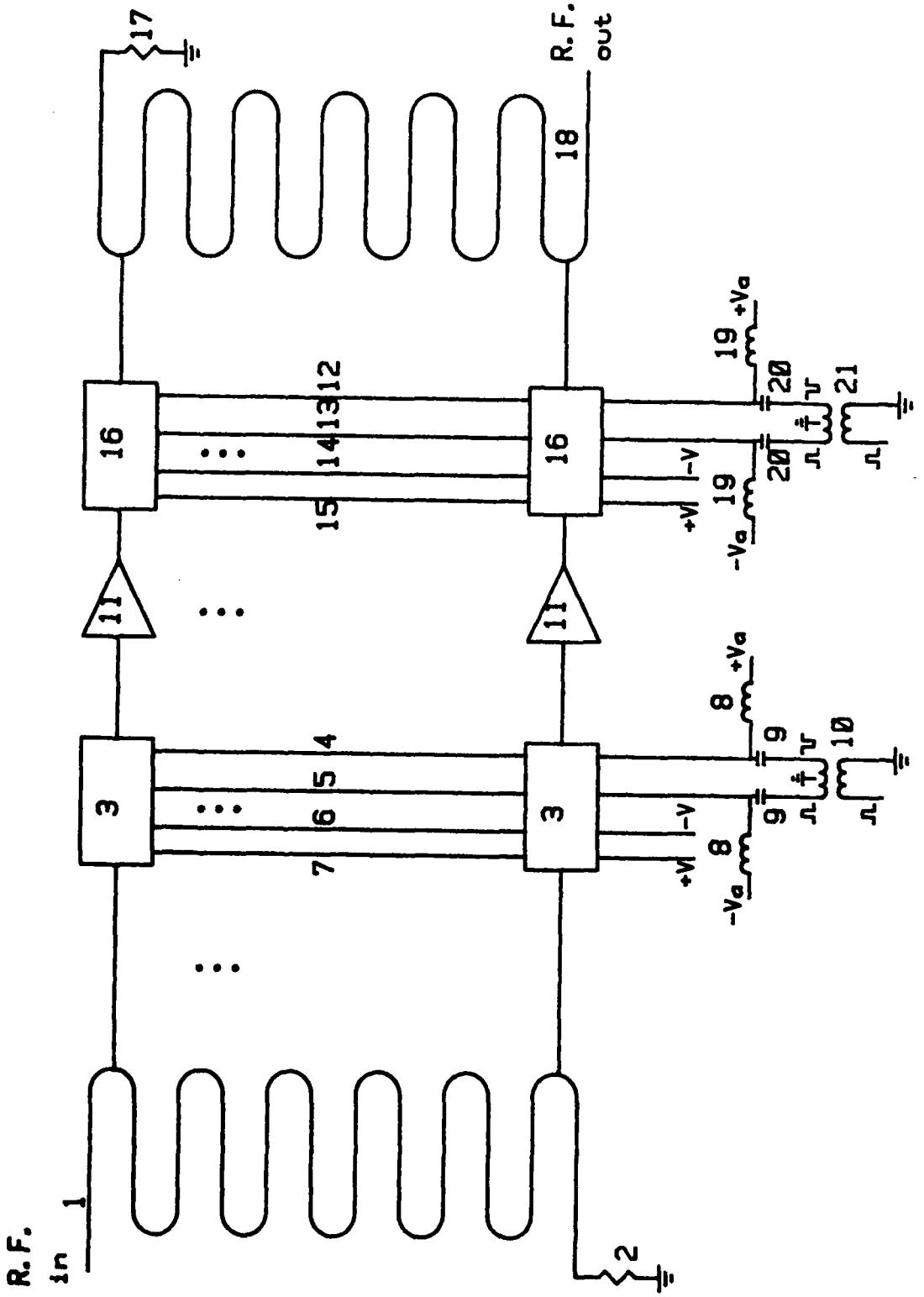


FIGURE 3.1 - PROTOTYPE SAMPLING AMPLIFIER SYSTEM

The design goals for the prototype circuit were selected on the basis of availability of pulse generation devices, the size of the prototype circuit and the standard impedance for microwave circuits. Design goals satisfying these requirements are given as follows:

Input bandwidth	0-2 GHz
Input impedance	50Ω
Sampling rate	10 MHz
Output impedance	50Ω
Number of parallel channels	20

A 20 channel prototype device was selected in order to verify the concept experimentally. This represents reconstruction and amplification of about 10% of the signal. In most applications full reconstruction and amplification would be carried out.

3.3 Delay Line Design

3.3.1 Introduction

The delay lines were fabricated of microstrip using RT/duroid 5880 material. The ease in implementing circuits in microstrip and the superior characteristics of the RT/duroid material (i.e. constant ε_r and low loss tangent) were the primary reasons for its selection. Determination of both the strip conductor width of microstrip lines and the required sampling interval (T_s) between adjacent channel (and its corresponding microstrip length) are outlined in this section. In addition, a calculation of transmission line losses and their effects on the operation of the circuit is addressed.

3.3.2 Strip Conductor Width for a 50Ω Line

Hammerstad [4] has characterized the microstrip geometry of Fig. 3.2 for given characteristic impedances. His expressions include useful relationships which define both characteristic impedance (Z_0) and effective dielectric constant (ε_{eff}). The equations are expressed in terms of the dielectric constant of the material (ε_r), the substrate thickness (h), the strip conductor thickness (t) and the strip conductor width (W). These expressions are outlined in Appendix A. A computer program, also given in Appendix A, determines the value of Z_0 for specified W/h values. For h = 20 mils, t = 1.5 mils and ε_r = 2.2, a strip conductor width (W) of about 60 mils is required for the 50Ω delay lines (printout in Appendix A).

3.3.3 Sampling Interval (T_s)

The propagation of the meander line between adjacent channels, T_s, completely defines the upper frequency for which a Nyquist sample set exists. An extension of the general Nyquist sampling theorem states that any 2BT' unique (independent) uniformly distributed pieces of information are needed to completely specify a signal over an interval T' seconds long [5]. Thus for the meander delay line of Fig. 3.3,

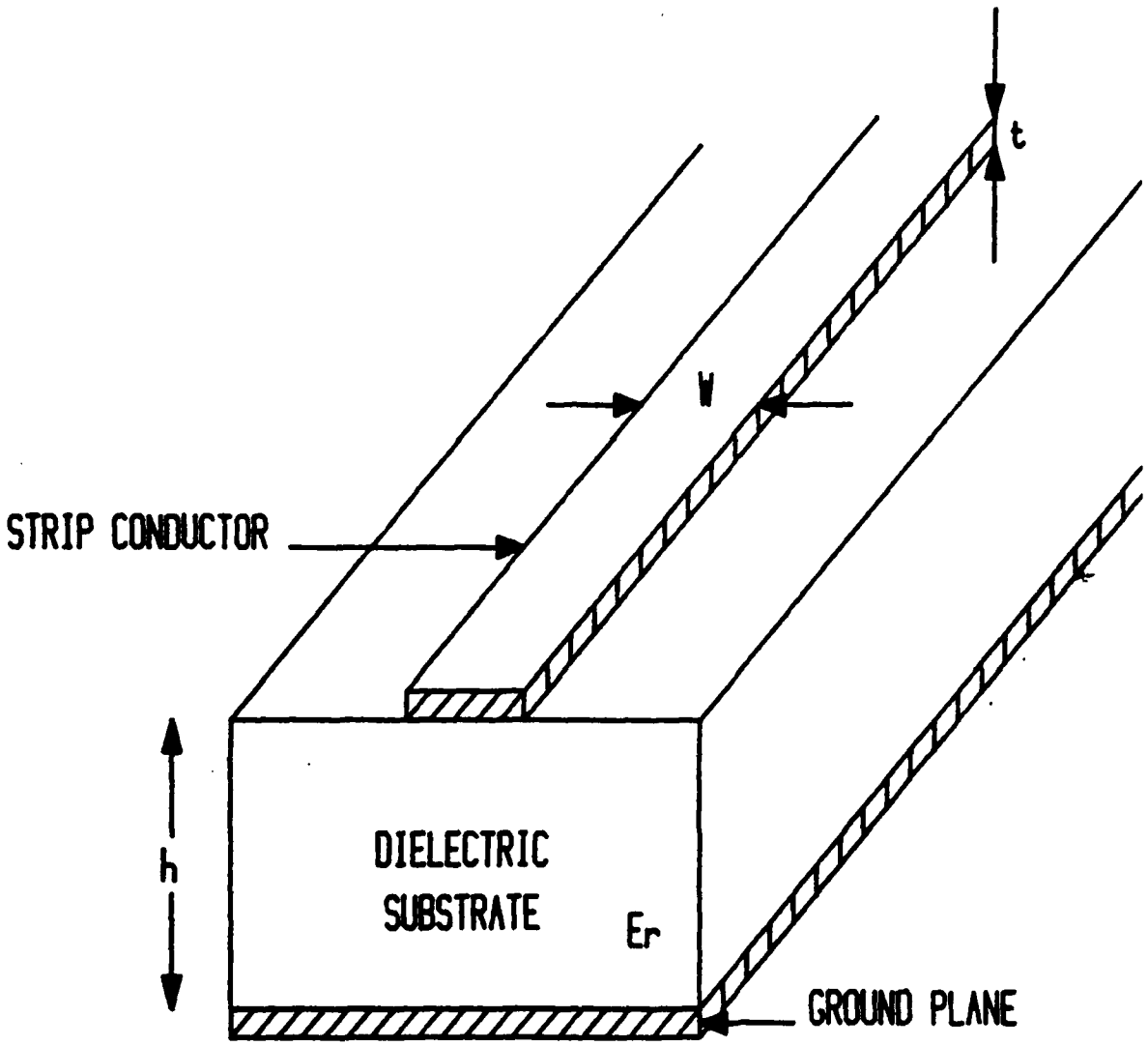
$$N = 2BT' = 2BNT_s$$

and

$$B = 1/2T_s \tag{3.1}$$

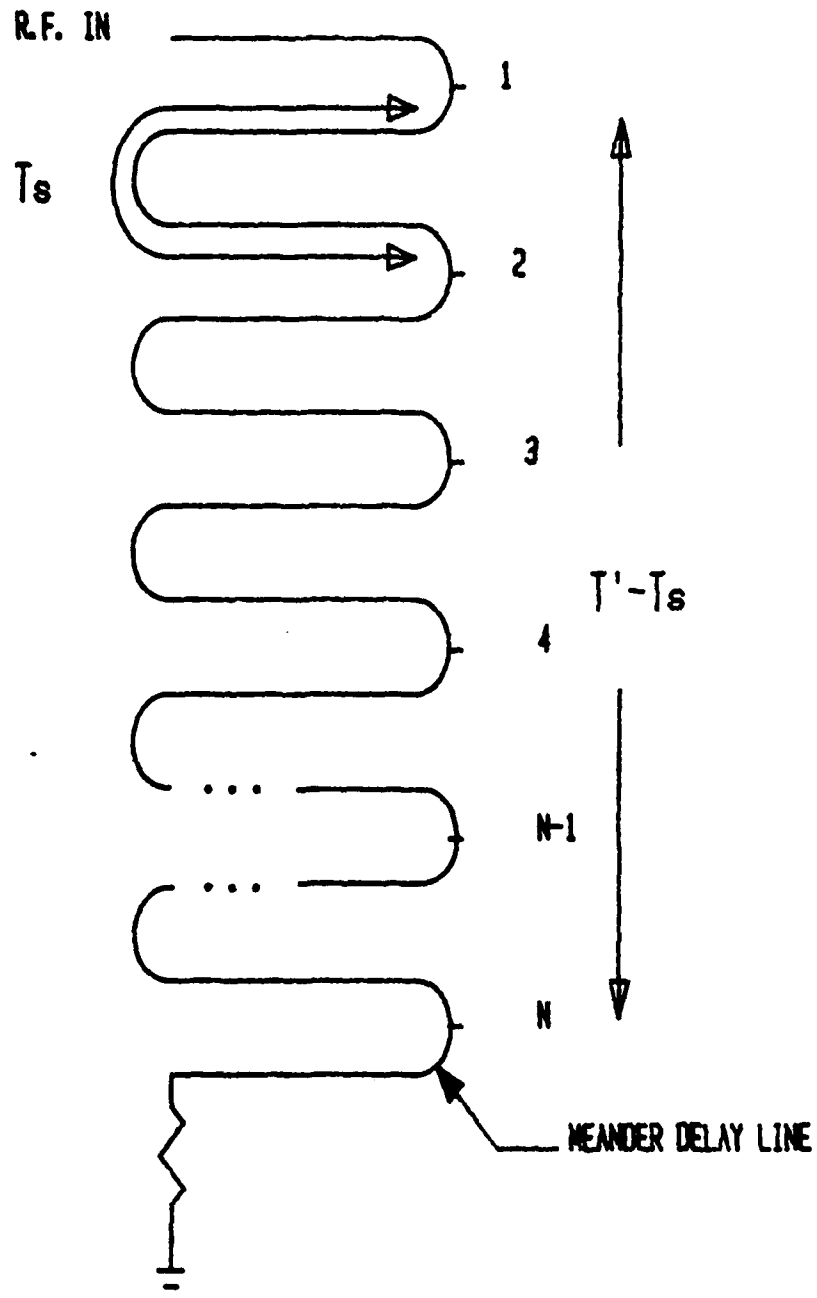
where B is the upper frequency, N is the number of independent samples and T_s is the sampling interval between adjacent channels.

The above statement is true if all samples are activated simultaneously, however, in the prototype device there is some finite delay between activation of each of the samplers. This results from the propagation delay of the sampling pulse as it travels along the pulse line. Consequently,



h: SUBSTRATE THICKNESS
t: STRIP CONDUCTOR TICKNESS
W: STRIP CONDUCTOR WIDTH
Er: DIELECTRIC CONSTANT

FIGURE 3.2 - MICROSTRIP TRANSMISSION LINE



$$T' = (N-1)T_s + T_s = NT_s$$

FIGURE 3.3 - MEANDER DELAY LINE OF DELAY TIME T' SECONDS

the propagation delay of the meander line between adjacent channels, T_s, will be modified to reflect the effective time delay (T_{se}) between adjacent channels.

The physical layout of the input side of the prototype sampling amplifier circuit is illustrated in Fig. 3.4. The spacing between adjacent channels (ℓ_1) was set to .8 inches allowing for easy assembly of components. The input signal and sampling pulses were chosen to propagate in the same direction. Thus, the effective time delay, T_{se}, is given by [3]

$$T_{se} = T_s - t_p,$$

where t_p is the propagation delay between adjacent channels along the pulse line. For an upper frequency limit of 2 GHz

$$T_{se} = \frac{1}{2B} \text{ 250 psec.}$$

Assuming the quasi-TEM mode of propagation, the propagation delay in microstrip is given by [6]

$$t_\lambda = \frac{1}{v_p} = \frac{\sqrt{\varepsilon_{eff}}}{c}.$$

From the computer printout in Appendix A

$$\varepsilon_{eff} \simeq 1.872.$$

Thus,

$$t_\lambda = 45.61 \text{ psec/cm} = 115.84 \text{ psec/in.}$$

Given

$$\ell_1 = .8 \text{ inches},$$

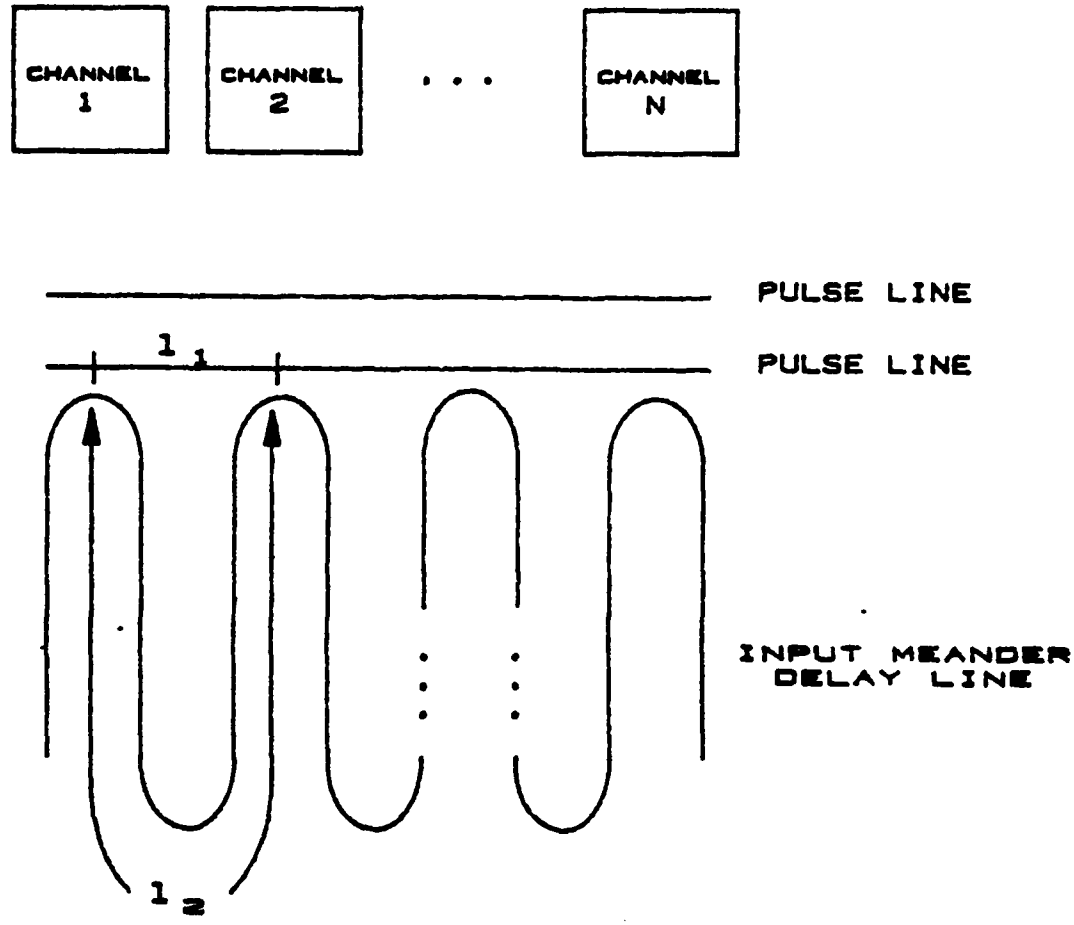
$$t_p = t_\lambda \cdot \ell_1 = 92.7 \text{ psec.}$$

Therefore,

$$T_s = T_{se} + t_p = 342.7 \text{ psec}$$

and

$$\ell_2 = \frac{T_s}{+} = 2.958 \text{ inches.}$$



l_1 - PHYSICAL LENGTH OF THE PULSE LINE BETWEEN ADJACENT CHANNELS

l_2 - PHYSICAL LENGTH OF THE MEANDER LINE BETWEEN ADJACENT CHANNELS

FIGURE 3.4 - PHYSICAL LAYOUT OF THE INPUT SIDE OF THE PROTOTYPE CIRCUIT

Hence, a maximum delay line of 2.958 inches is required between adjacent taps in order to reconstruct and amplify input signals to 2 GHz. In the prototype circuit ℓ_2 was set to 3.160 inches, allowing for the acquisition of Nyquist sample set up to a maximum input frequency of 1.8 GHz.

This derivation assumes that no capacitive effects (loading) exist along the delay line. In the case of the prototype circuit this is valid at low frequencies but may not apply at higher frequencies as a result of the diode sampling gates being tapped along the line.

3.3.4 Transmission Line Losses

Conductor loss (α_c) and substrate dielectric loss (α_d) account for the two sources of dissipative losses in microstrip. The total loss may be expressed as

$$\alpha = \alpha_c + \alpha_d \text{ dB/unit length.} \qquad (3.2)$$

Expressions describing these two sources of dissipative losses are outlined in Appendix B. For the prototype sampling amplifier circuit, the total loss is given by

$$\alpha = 1.417 \times 10^{-11} \sqrt{f} + 7.43 \times 10^{-6} f \text{ dB/cm.}$$

A plot of the total loss as a function of frequency for the meander delay line having a total length (ℓ) of 63.2 inches is given in Fig. 3.5. Clearly, the total loss of the meander line will have little effect on the overall performance of the sampling amplifier within the design region.

3.4 Sampling Gate

3.4.1 Introduction

Basic considerations in the selection of a sampler unit are input-to-output offset, input-to-output feedthrough in the "off" state and sample pulse feedthrough onto the output line. In a conventional discrete circuit, the commonest configuration uses a ring of Schottky diodes driven by a transformer

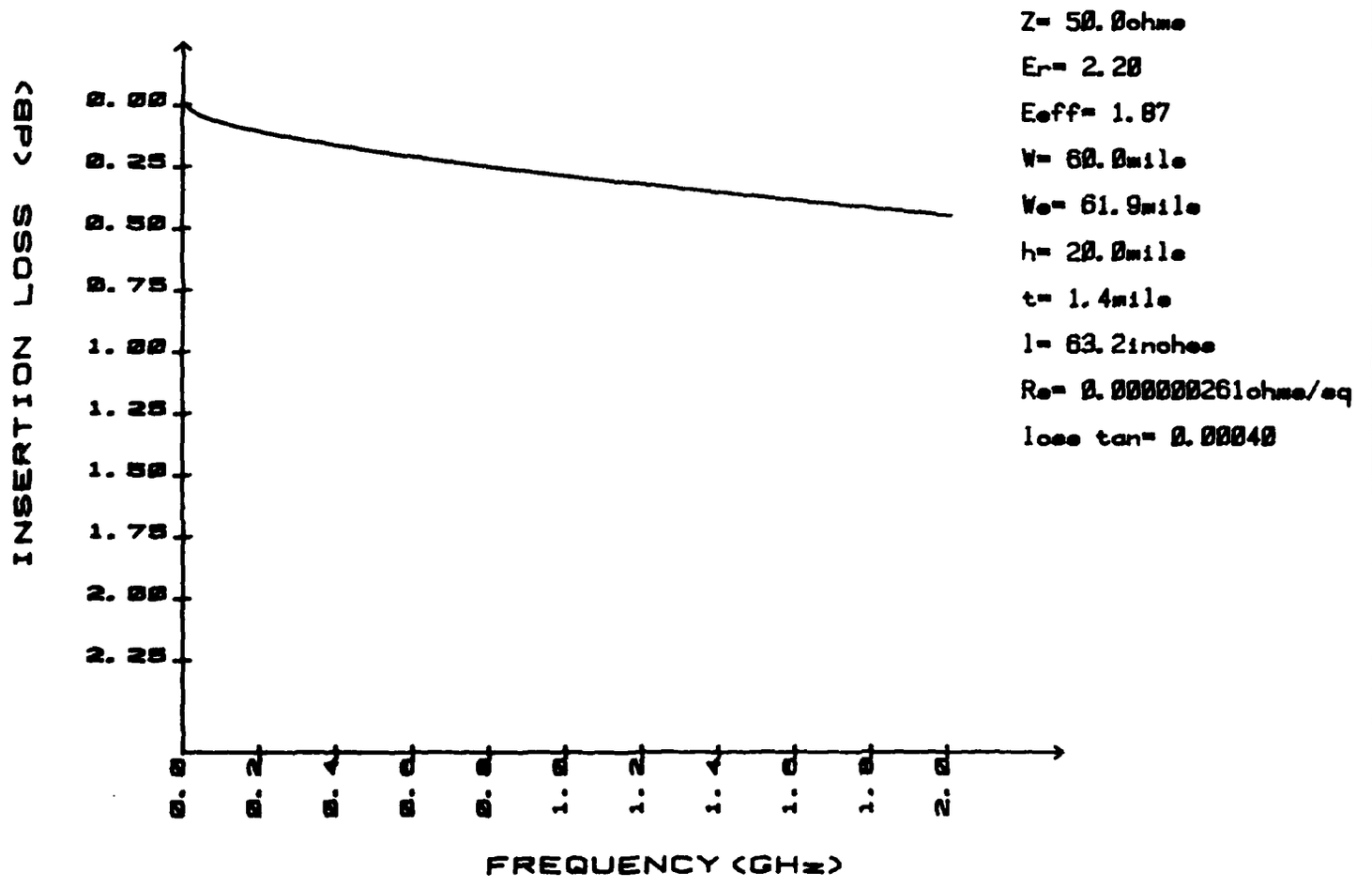


FIGURE 3.5 - CALCULATED INSERTION LOSS OF THE MEANDER DELAY LINE

which has the advantages of high "on" to "off" ratio, reasonably low offset with selected devices and a degree of sample pulse feedthrough cancellation due to the balanced drive to the circuit [10]. A six-Schottky-barrier-diode arrangement was thus selected and is shown in Fig. 3.6. Each of the sampler units in the experimental device is formed of six HP 5082-2815 Schottky barrier diodes having picosecond switching times [11].

3.4.2 Six-diode Sampling Gate

When the gate of Fig. 2.7 transmits no signal, diodes D5 and D6 are conducting and acting as clamps while all other diodes are open. During signal transmission, diodes D5 and D6 are reverse biased while diodes D1 through D4 conduct.

If the points P_1 and P_2 are clamped at a voltage $V_n - V_d$ and $-V_n + V_d$ respectively, where V_d is the forward diode drop, then none of the transmission diodes (D1-D4) will conduct until V_s exceeds V_n. Therefore,

$$(V_n)_{min} = V_s$$

Conversely, if the clamping diodes D5 and D6 are to remain reverse-biased for a signal amplitude V_s, then

$$(V_c)_{min} = V_s$$

Furthermore, the required voltages V_b and $-V_b$ depend on the amplitude of the input signal V_s and are determined by the condition that the current conduction be in the forward direction for all four diodes D1 and D4. The derivation of the d.c. bias voltages is carried out in reference [3] and is given by

$$(V_b)_{min} = \frac{2R_b + R_s}{R_s}\left[1 - \frac{R_b(R_s + 2R_L)}{(R_s + 2R_L)(R_s + 2R_b) - 2R_L R_b}\right]V_s,$$

where R_s is the forward diode resistance. The above equations assume that the forward diode resistance R_s in all four conducting diodes are approximately equal.

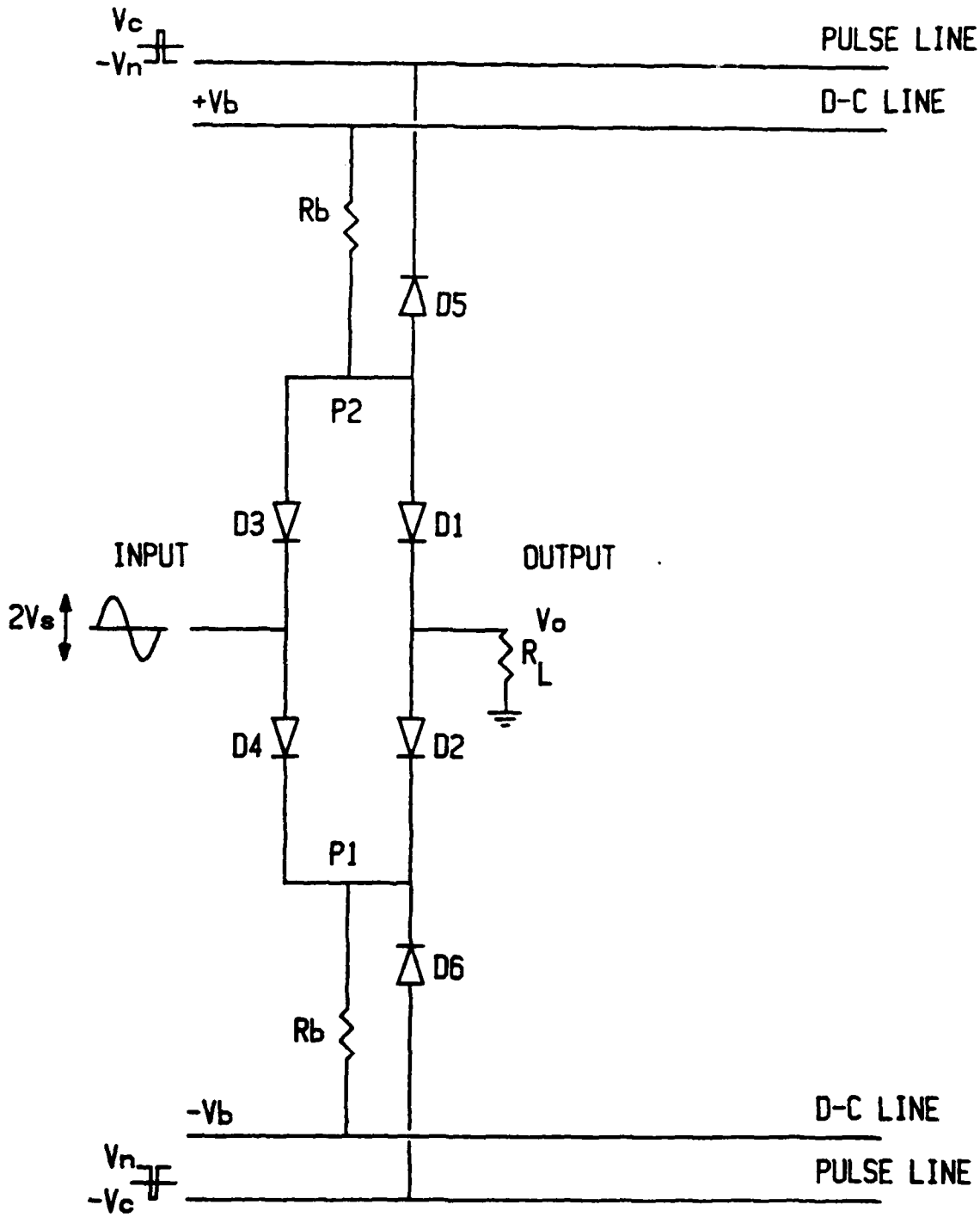


FIGURE 3.6 - DIODE SAMPLING GATE

3.4.3 Drawbacks of the Six-diode Sampling Gate

The six-diode switch configuration, although providing picosecond sampling capability, requires a low impedance driving source. Since the diode sampling gate is largely current dependent, sufficient pulse drive is necessary to enable sampling of large signal amplitudes. When 20 samples are driven in parallel the situation is even more critical. To ease the drive requirements a relatively large resistance R_b was necessary. Consequently, the experimental device is limited to relatively small output power levels.

A second difficulty occurs when the diodes (D1-D4) are reverse-biased in that their associated shunt and junction capacitances and lead inductances begin to limit the "on" to "off" ratio of the sampling gate at higher frequencies [12]. This will limit the frequency of operation for the device.

For a maximum sampling pulse amplitude of approximately 4 volts the following design values were found suitable for the input and output sampler units in the experimental device.

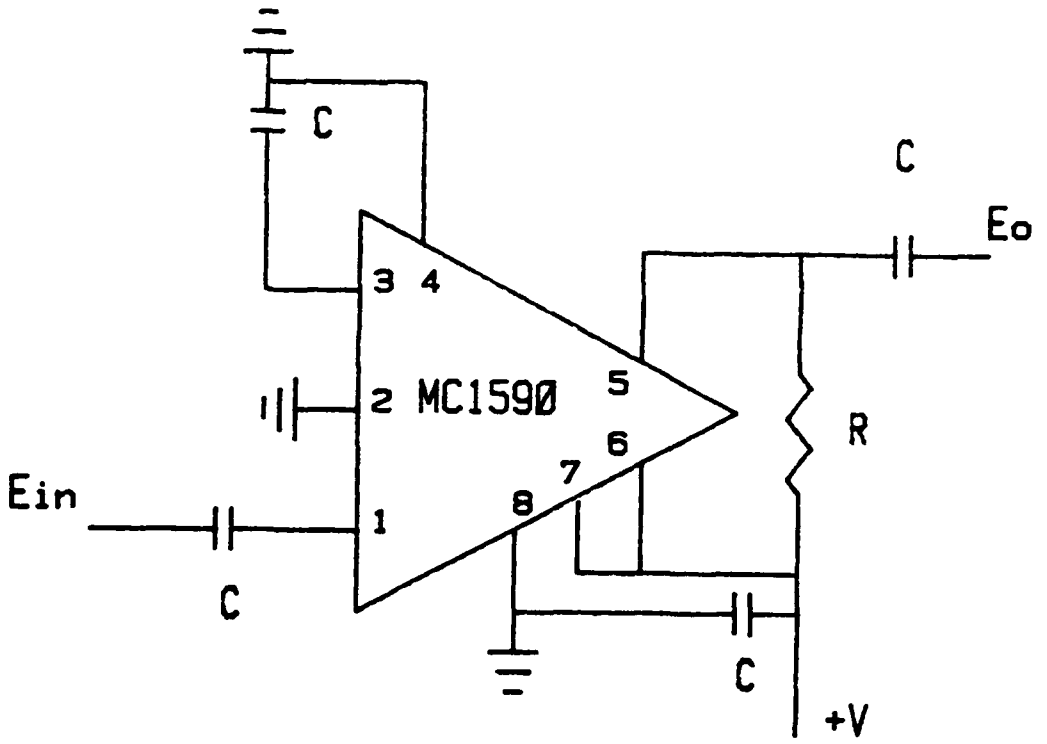
$$V_n \simeq V_c \simeq 2V$$

$$\pm V_b = 12V$$

$$R_b = 4.7k\Omega$$

3.5 Amplifier Selection

The bandwidth of the amplifier is a function of the sampling rate. The minimum bandwidth required must be slightly in excess of one-half the sampling rate as was shown in reference [3]. Thus, for a sampling rate of 10 MHz an amplifier bandwidth of about 5-10 MHz is required. The Motorola MC 1590G satisfies this requirement and was chosen as a result of its high gain characteristic. The layout for the amplifier network as recommended by the manufacturer [13] is shown in Fig. 3.7. From the specifications outlined in reference [13] the following parameter values are obtained:



R-1.0k
C-1.0uF

FIGURE 3.7 - VIDEO AMPLIFIER CIRCUIT

$$C = 6.4 \text{ pf},$$

$$R_{in} = 2500 \ \Omega,$$

$$C_o = 2.7 \text{ pf},$$

$$R_o = 20 k\Omega,$$

$$G_n = 3328.$$

In addition to the bandwidth requirement, the amplifier's input RC time constant when the sampler is reverse biased must be small in comparison to the time between samples. This is necessary in order to avoid interference from sample to sample in individual channels. The amplifier's input RC time constant when the gate is "OFF" is given by $R_{in}C$ = 16 nsec. Thus for a 10 MHz sampling rate, the input capacitor is fully discharged before the next sample is acquired and no interference from successive samples will occur.

Moreover, the gain equation given in Chapter 2 assumes that the output capacitor is fully charged when the sample waveform is sampled out onto the output delay line. The amplifier's output RC time constant when the switch is "OFF" is given by $\frac{R_L R_o C_o}{R_L + R_o}$ = 2.6 nsec. Consequently, for a 10 MHz sampling rate, the output capacitor is fully charged and the gain equation may therefore be used to compute the overall gain for the system.

3.6 Pulse Generation Devices

To provide suitable sampling pulses having picosecond pulse widths, specialized pulse generators and power splitters have been developed by Avtech Electrosystems Limited under the sponsorship of DREO. The larger units in Fig. 3.8 are impulse generators which provide 200 psec - 2 nsec pulse widths, 0-25 MHz pulse repetition rates and output pulse amplitudes to 15 volts (Fig. 3.9). The smaller units in Fig. 3.8 are special wideband power splitters which divide the input pulse into complementary positive and negative pulses (Fig. 3.10). These devices have exhibited risetimes of less than 60 picoseconds.

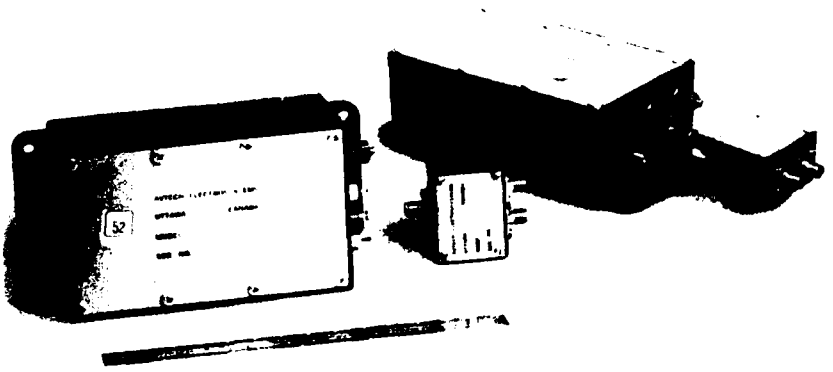


FIGURE 3.8 - PICOSECOND PULSE DEVICES

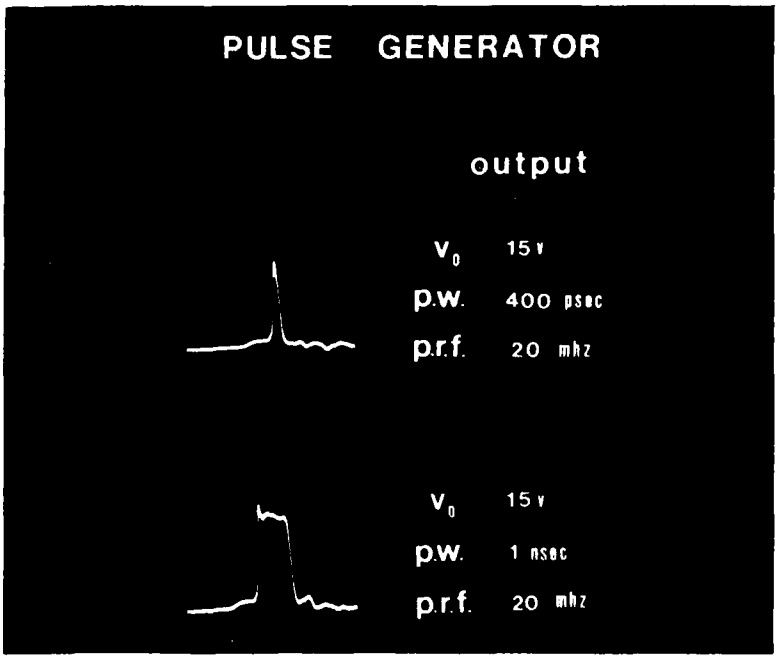


FIGURE 3.9 - TYPICAL PULSE GENERATOR OUTPUT WAVEFORMS

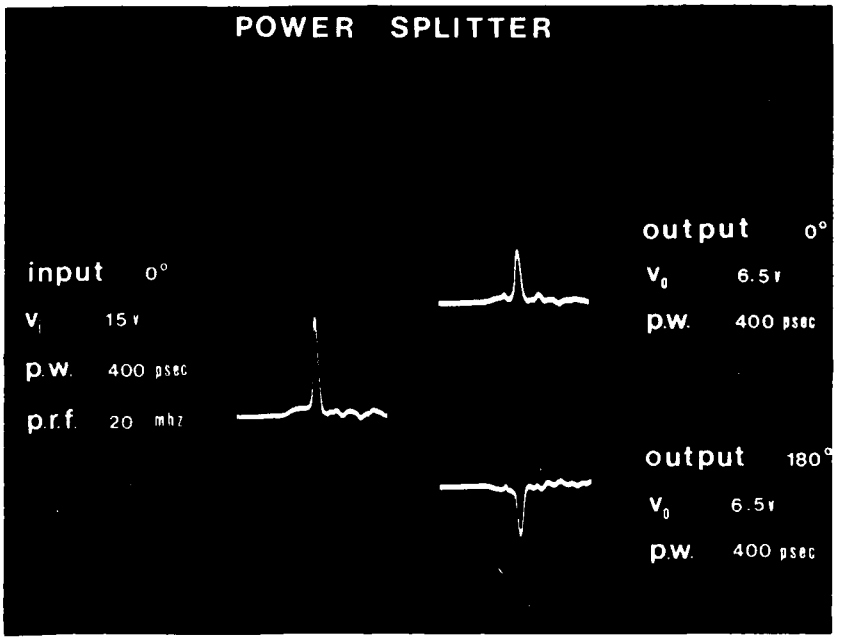


FIGURE 3.10 - COMPLEMENTARY OUTPUTS PRODUCED BY A POWER SPLITTER

4.0 EXPERIMENTAL RESULTS

4.1 Introduction

The results of the overall system performance are reported in this section. Basic subsystem parameter measurements are initially introduced in order to identify some of the system parameters and limitations. Overall system parameter measurements such as gain, frequency response and maximum output power are subsequently described and compared with theoretical values.

4.2 Subsystem Parameter Measurements

4.2.1 Introduction

This section discusses a number of subsystem parameters including the insertion loss of the input and output meander delay lines for both the unassembled and assembled circuit board and the insertion loss, input-to-output feedthrough and "on" resistance of the sampling gate. The effect of the sampler units on the meander delay lines is also described.

4.2.2 Meander Delay Line Insertion Loss

An automated set-up was used to obtain the insertion loss and return loss of the meander delay lines. The system set-up and programming are reported in reference [3]. The insertion loss and return loss for the unassembled circuit board is shown in Fig. 4.1. The measured meander delay line insertion loss is essentially the same as the calculated insertion loss given in the previous section. There is, however, a band-reject filter characteristic within the expected range of operation. The center frequency of this filter characteristic corresponds to approximately one wavelength between adjacent channels (T_s).

A second set of measurements were conducted on the assembled experimental circuit. These measurements were carried out with the sampler units reverse-biased to 2 volts. Fig. 4.2 and Fig. 4.3 show the insertion loss

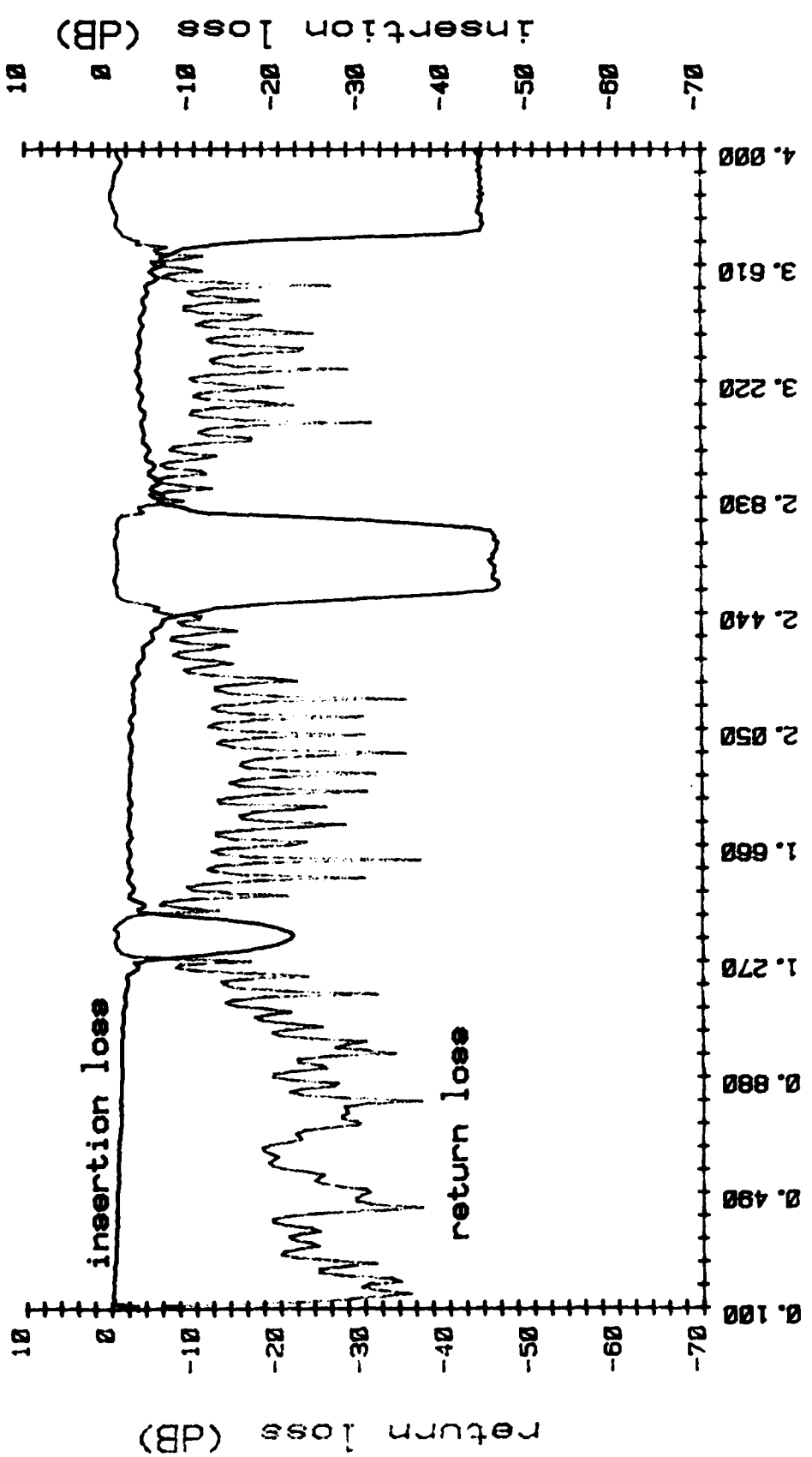


FIGURE 4.1 - INSERTION LOSS AND RETURN LOSS MEASUREMENTS OF THE MEANDER DELAY LINE FOR THE UNASSEMBLED BOARD

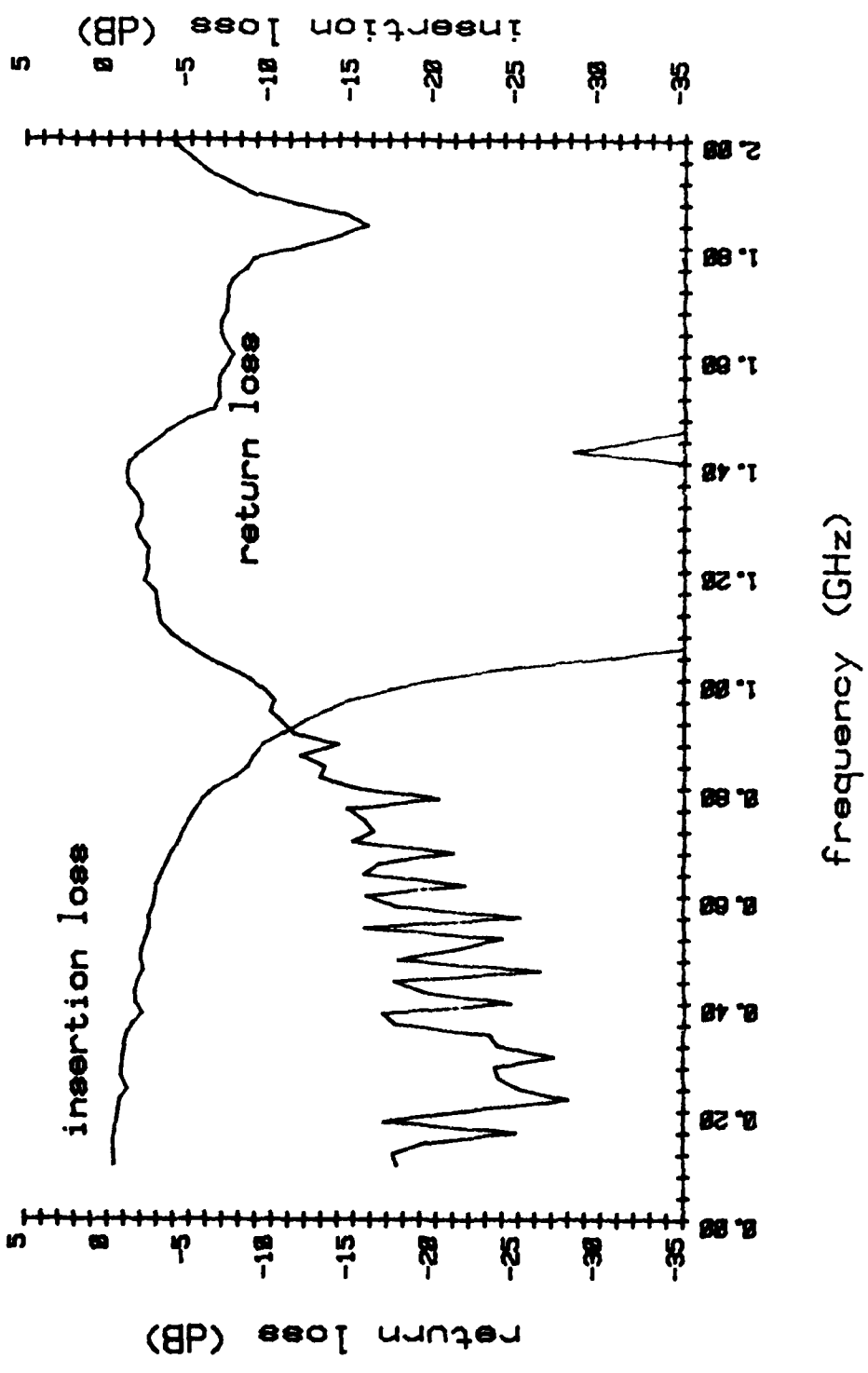


FIGURE 4.2 - INSERTION LOSS AND RETURN LOSS MEASUREMENTS OF THE INPUT MEANDER DELAY LINE FOR THE ASSEMBLED UNIT

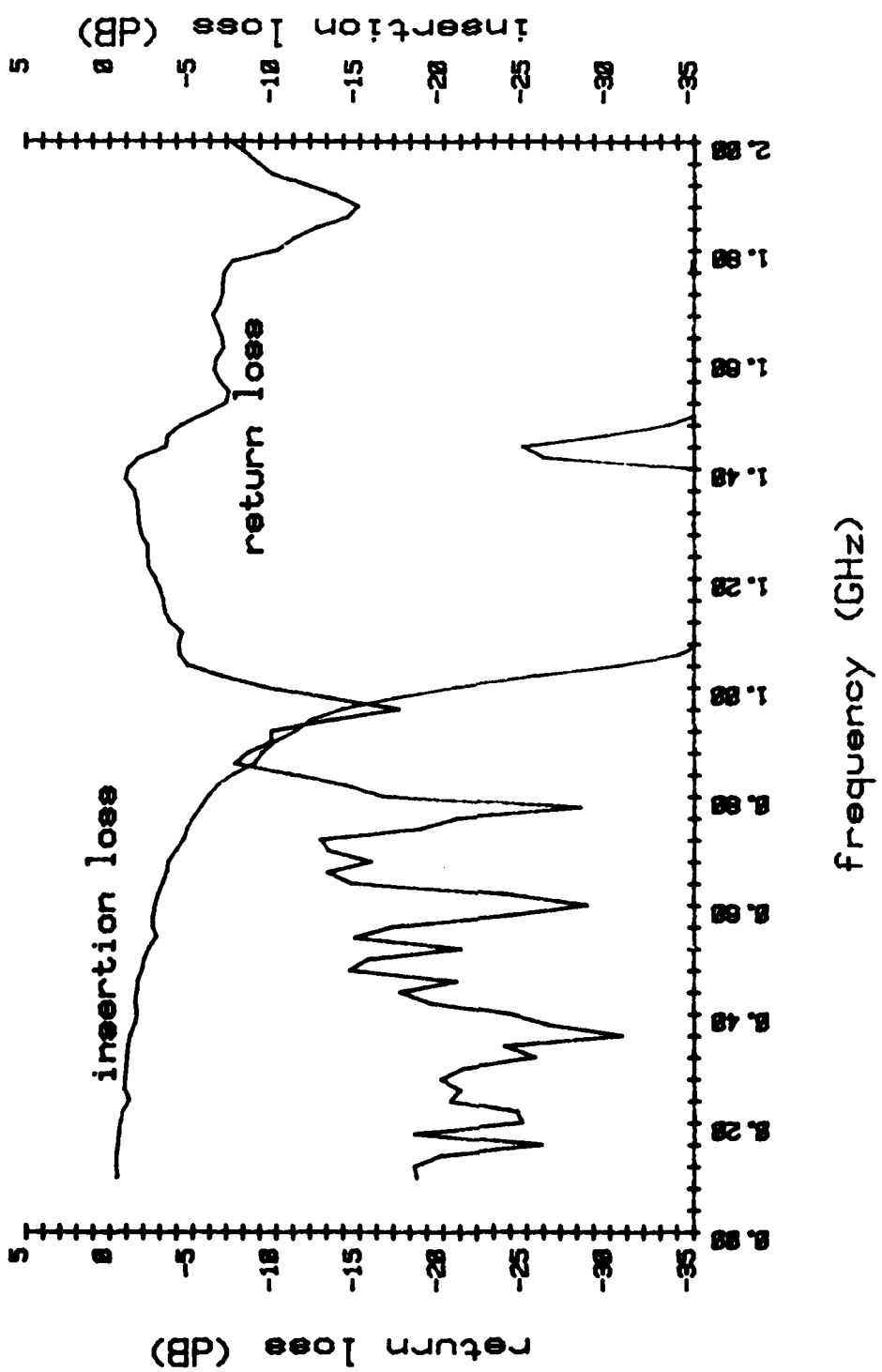


FIGURE 4.3 - INSERTION LOSS AND RETURN LOSS MEASUREMENTS OF THE OUTPUT MEANDER DELAY LINE FOR THE ASSEMBLED UNIT

and return loss of the input and output meander delay lines, respectively. These measurements indicate a low pass filter response within the expected range of operation. It will be shown that the sampler units contribute to the increase in insertion loss about the input frequency of 900 MHz. As a result of the frequency response of the meander delay lines, the sampling amplifier will be limited in bandwidth. It should be noted that even though losses in the meander delay lines are present, the overall system will remain substantially linear. This results from the fact that the signal sample which is attenuated the most at the input is attenuated the least at the output and vice-versa.

4.2.3 Sampler Characteristics

Measurements of insertion loss, input-to-output feedthrough and switch resistance were carried out on the sampling gate. Fig. 4.4 illustrates the insertion loss of the sampler under the forward bias ("on") condition. The response is reasonably flat over the 0-2 GHz range. The input-to-output feedthrough in the "off" state may be obtained by subtracting the sampler's "off" state insertion loss of Fig. 4.5 from the "on" state insertion loss of Fig. 4.4. The feedthrough component is less than -25 dB up to 800 MHz. It rises linearly from this point to 1 GHz where it reaches a maximum of -7 dB. This explains the increased insertion loss of the meander delay lines above 900 MHz.

The sampler's "on" resistance (R_s) when pulsed is different from the continuous biased "on" condition. The experimental set-up of Fig. 4.6 was used to conduct a measurement for obtaining the sampler's resistance. For a pulse width of 850 psec a switch resistance of 49Ω was obtained.

4.3 System Measurements

4.3.1 Basic Experimental Set-up

The experimental sampling amplifier circuit is shown in Fig. 4.7. The input meander delay line, output meander delay line and input and output pulse

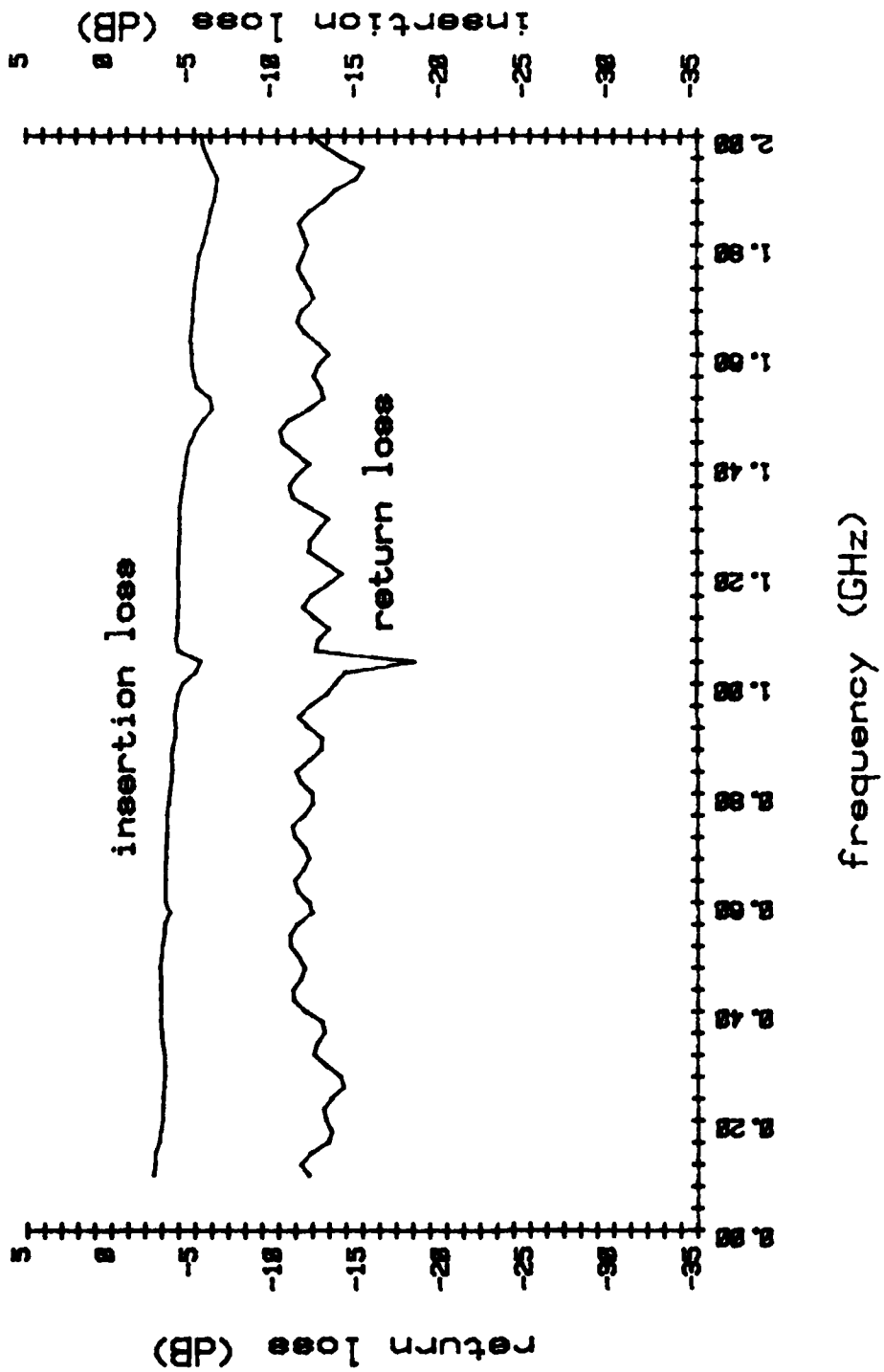


FIGURE 4.4 - INSERTION LOSS AND RETURN LOSS MEASUREMENTS OF THE SAMPLER UNIT UNDER FORWARD BIAS

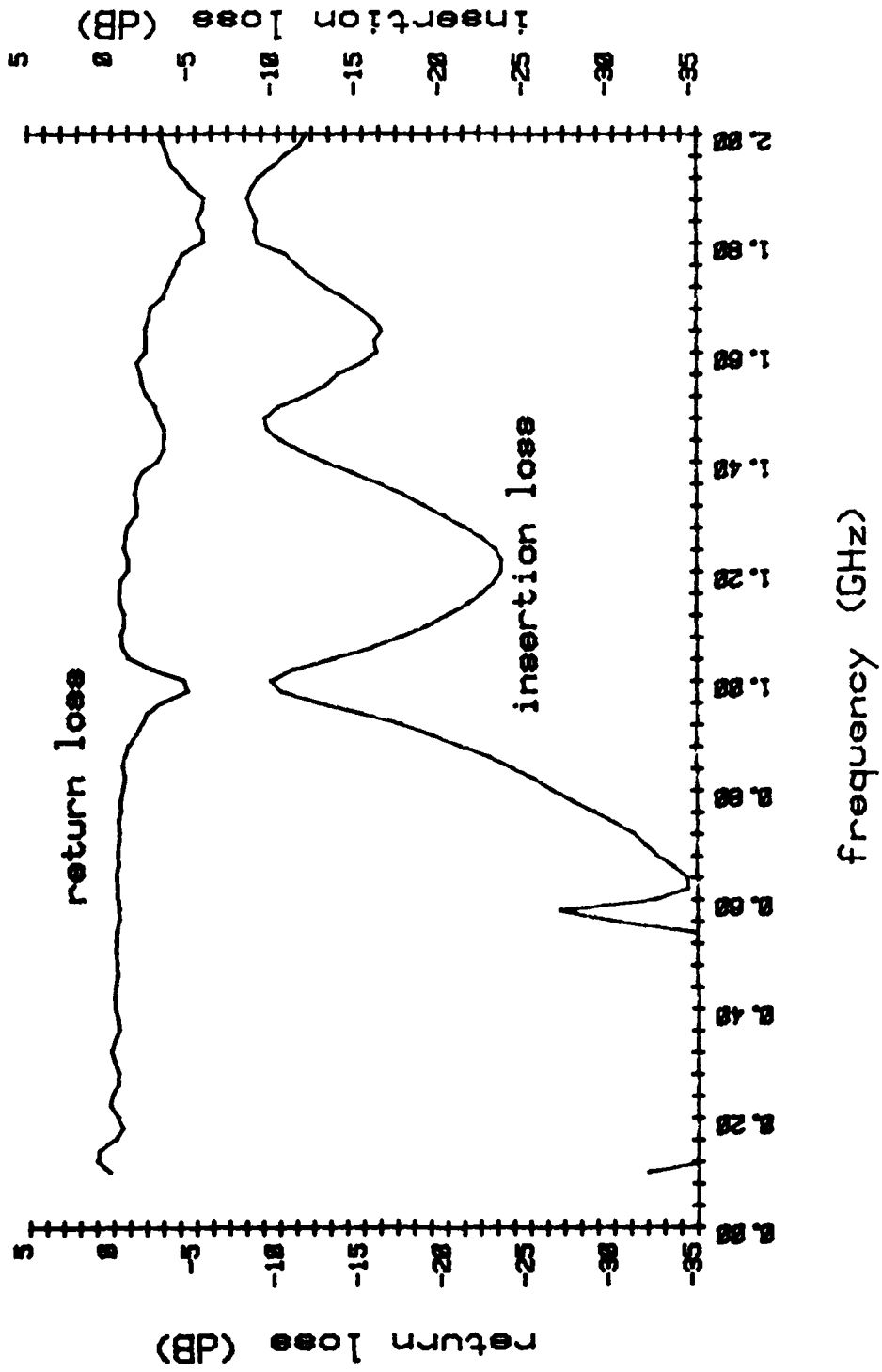
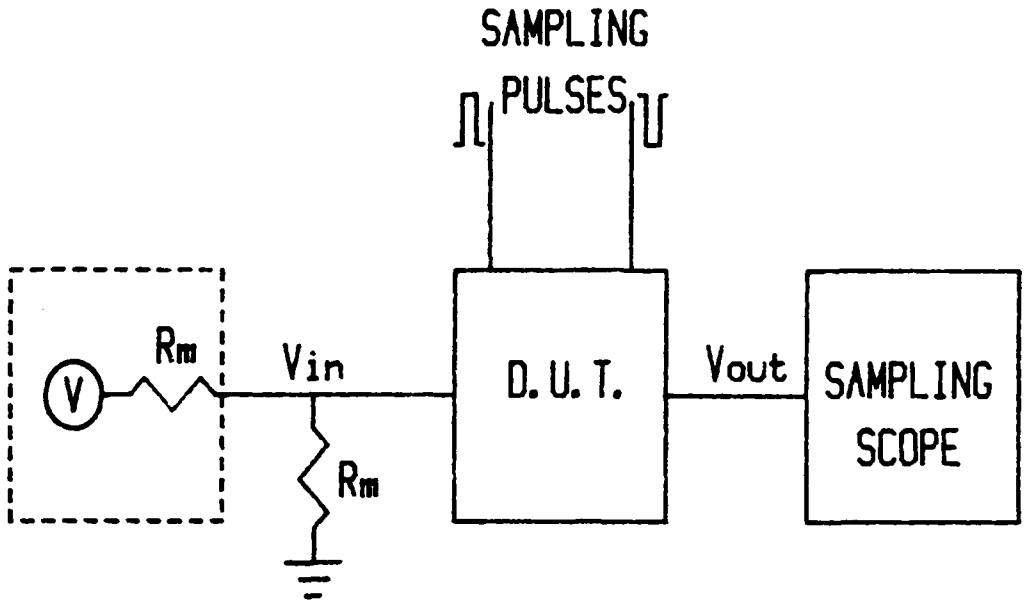
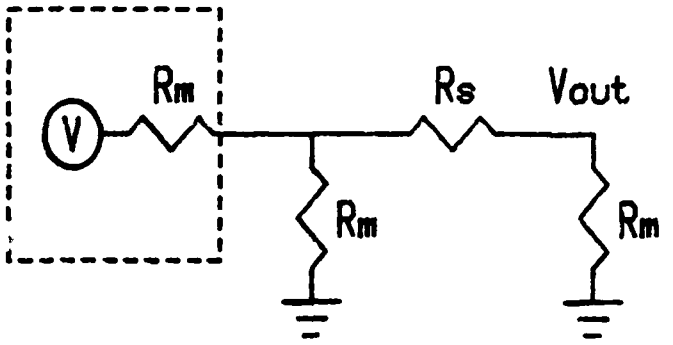


FIGURE 4.5 - INSERTION LOSS AND RETURN LOSS MEASUREMENTS OF THE SAMPLER UNIT UNDER REVERSE BIAS



(a)



$R_s = (R_m/2)(V/V_{out} - 3)$

(b)

FIGURE 4.6 - EXPERIMENTAL SET-UP FOR MEASURING THE SAMPLER'S ON RESISTANCE IN THE PULSED MODE

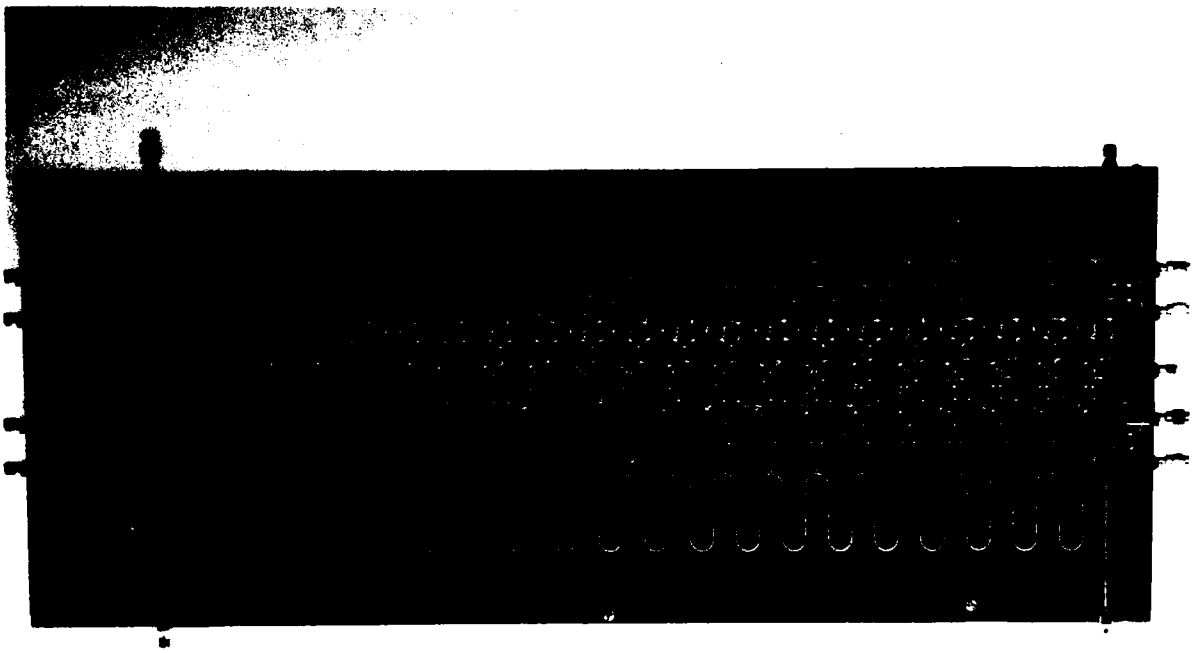


FIGURE 4.7 - EXPERIMENTAL SAMPLING AMPLIFIER CIRCUIT

lines are shown. The components (diodes, amplifiers, etc.) are situated on the back side of the board (Fig. 4.8).

Fig. 4.9 illustrates the basic experimental set-up used to measure the system parameters. A frequency synthesizer served as the input signal source to the prototype sampling amplifier. A second synthesizer activated general purpose synchronized pulse generators which in turn triggered custom picosecond pulse generators thereby producing the required sampling pulses. Both input and output sampling pulse lines contained phase shifters. These devices aligned the sampling pulses thus insuring that their respective sampling gates were being activated by both pulses simultaneously. A 18 GHz sampling scope, a 1 GHz real-time oscilloscope and a spectrum analyzer were used for conducting various measurements.

4.3.2 Time Domain and Frequency Domain Responses

Fig. 4.10 (a) shows the input and output time domain waveforms of the 20 channel sampling amplifier circuit. A 496 MHz synthesized input CW signal of 21 mv_{p-p} translates into an output pulse signal of approximately 6 nsec at 100 mv_{p-p}. Clearly, this illustrates that the use of the distributed sampling technique to carry out amplification of r.f. signals using low frequency video amplifiers is possible. The time domain and frequency domain waveforms of the output signal are shown in Fig. 4.10 (b). The (sin x)/x frequency response for the pulse signal is clearly shown in this figure. As a result of the frequency response of the meander delay lines, the (sin x)/x response is limited to the low pass region of the delay line.

Fig. 4.11 illustrates the frequency spectra of an amplitude modulated signal. In Fig. 4.11 (a), the input CW signal has 1 KHz 50% amplitude modulation. The output as produced by the sampling amplifier is shown in Fig. 4.11 (b). The peak to sidelobe level as well as the frequency content is shown

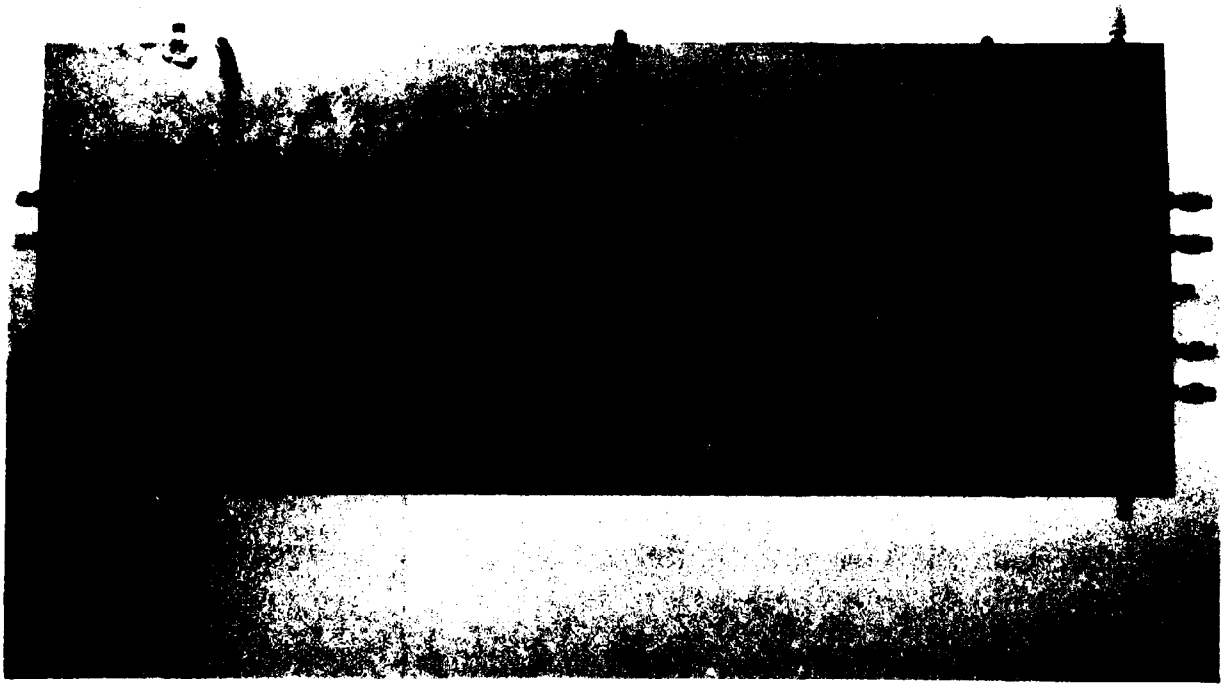


FIGURE 4.8 - COMPONENT SIDE OF THE EXPERIMENTAL SAMPLING AMPLIFIER CIRCUIT

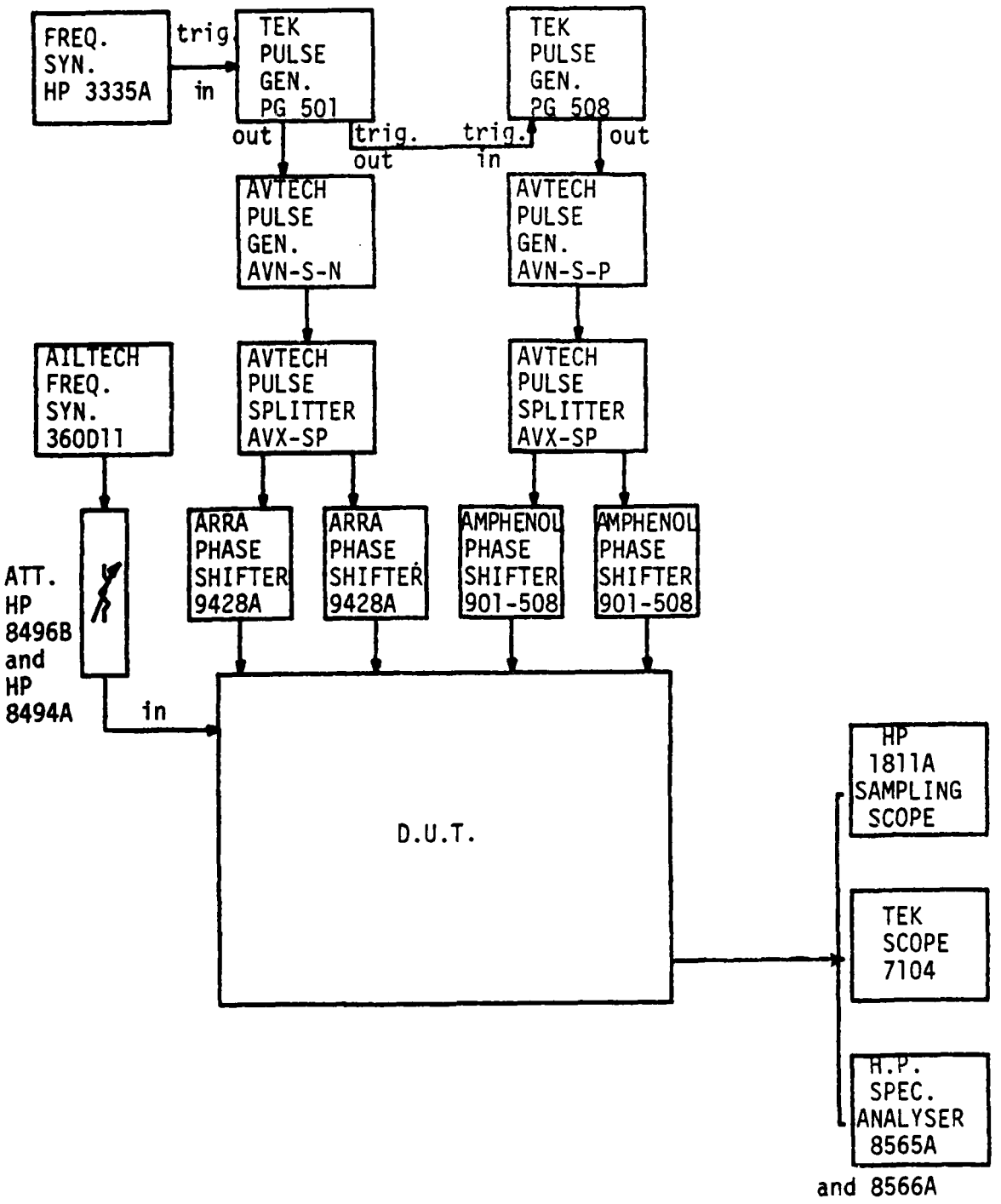
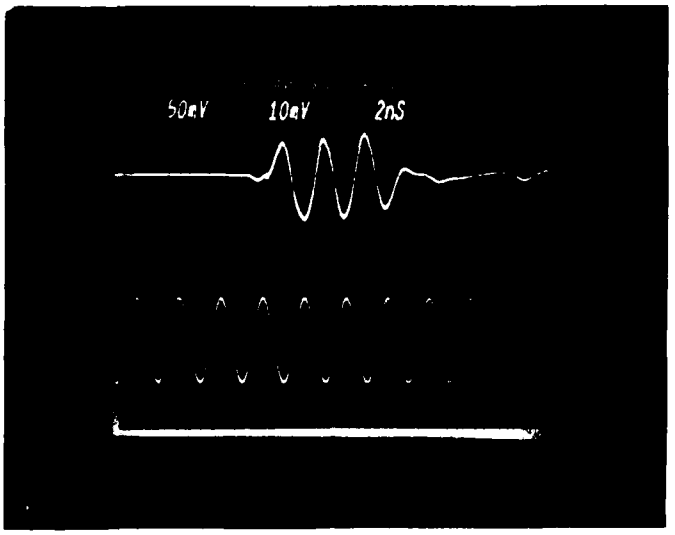
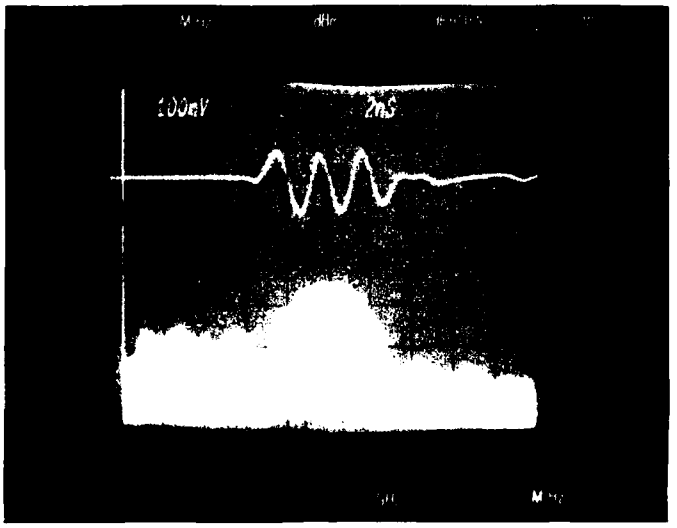


FIGURE 4.9 - BASIC EXPERIMENTAL SET-UP

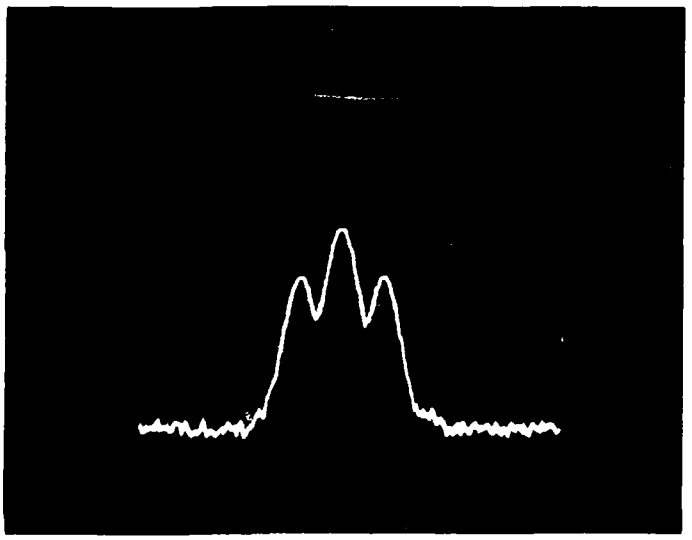


(a)

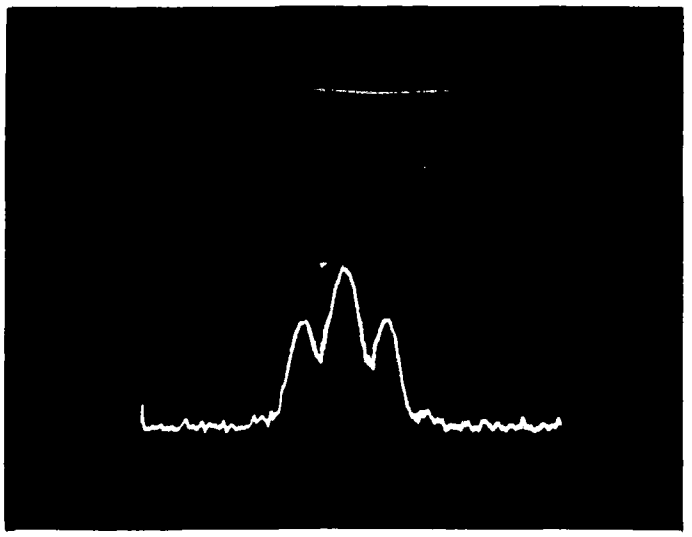


(b)

FIGURE 4.10 - (A) OUTPUT AND INPUT TIME DOMAIN WAVEFORMS
(B) OUTPUT TIME DOMAIN AND FREQUENCY DOMAIN WAVEFORMS



(a)



(b)

FIGURE 4.11 (A) INPUT CW SIGNAL WITH 1 KHz 50% AM MODULATION
(B) OUTPUT PULSE SIGNAL WITH 1 KHz 50% AM MODULATION

to be maintained through the sampling amplification process. Fig. 4.12 illustrates the input and output frequency spectra of an FM signal, again illustrating that frequency information is preserved throughout the processing.

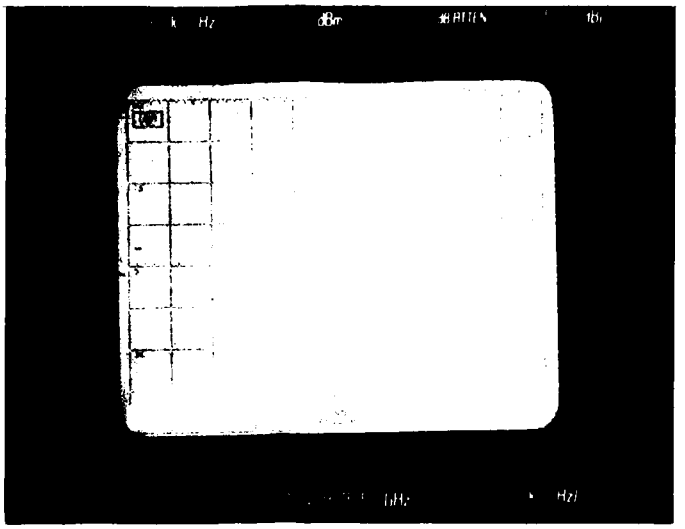
4.3.3 System Peformance Measurements

Various measurements were conducted to determine the sensitivity, 1 dB compression point, dynamic range, gain and frequency response of the experimental circuit. Fig. 4.13 (a) illustrates the output frequency spectrum of the device when an input CW signal of -27 dBm is applied. When no signal is applied, as in Fig. 4.13 (b), a noise spectrum is evident. These noise components result from a slight misalignment of the sampling diodes. Phase shifters were inserted to align the sampling pulses to avoid any pulse feedthrough, however, since the diodes are not accurately positioned some degree of noise is expected. Thus, the sensitivity S* of the experimental circuit will be defined as the input signal level for which its corresponding output reaches the self induced noise level. An input signal level -40 dBm at 496 MHz was measured for the sensitivity S*. Accurate alignment of individual diodes would substantially decrease the self induced noise level thereby improving the sensitivity.

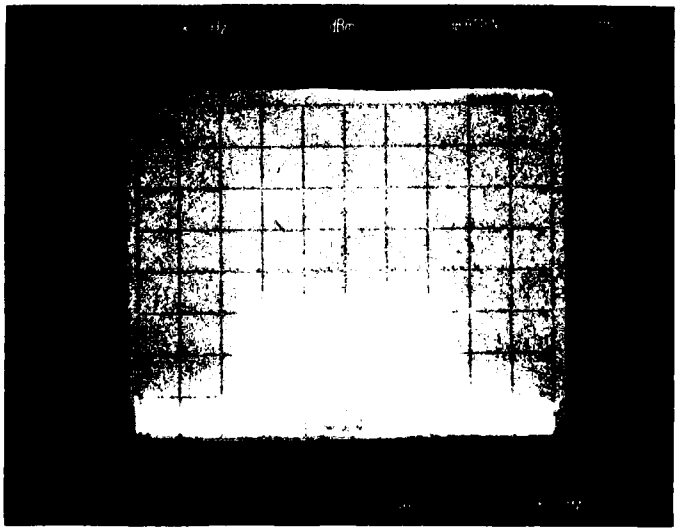
The 1 dB compression point was measured using precision attenuators at the input to the circuit. The output was monitored on a spectrum analyzer as the input level was increased in 1 dB steps. An input of -27 dBm at 496 MHz was obtained for the 1 dB compression point.

The dynamic range defined as the difference between the 1 dB compression point and the sensitivity level S* is therefore 13 dB.

The gain G given by equation 2.1 assumes the input signal is completely sampled. Since the input is a CW signal the gain of the system may

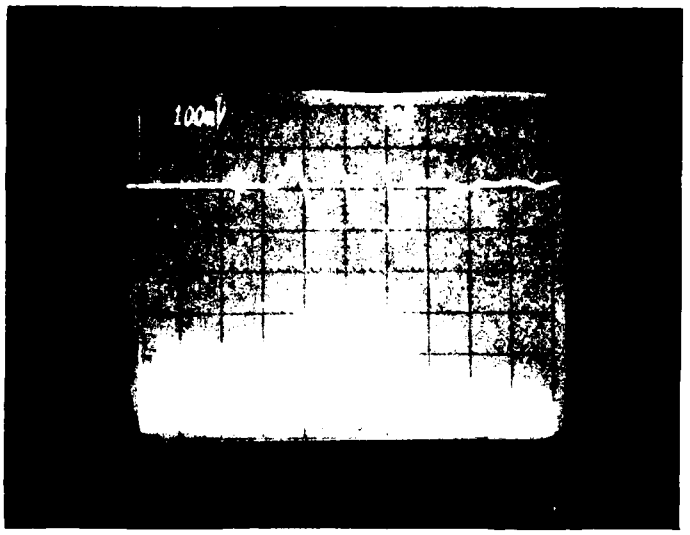


(a)

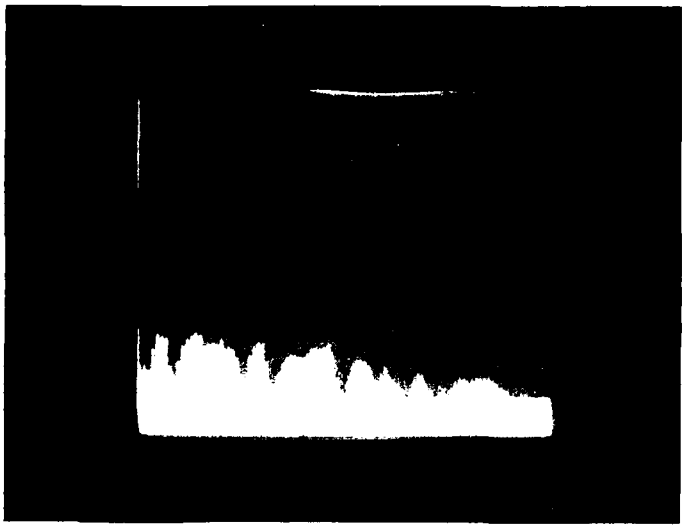


(b)

FIGURE 4.12 - (A) INPUT CW FM MODULATED SIGNAL
(B) OUTPUT PULSE FM MODULATED SIGNAL



(a)



(b)

FIGURE 4.13 - (A) OUTPUT PULSE SIGNAL
(B) OUTPUT NOISE FREQUENCY SPECTRUM

be obtained by subtracting a representative "output CW" signal level from the input CW signal level. Hence, for an input CW signal of -23 dBm at 371 MHz an output pulse signal of -40 dBm is obtained. Taking the pulse desensitization α_L [14] into account, a representative "output CW" signal level is given by

$$-40 \text{ dBm} - 20 \log (\tau_{eff} \cdot \text{PRF})$$

where τ_{eff} is the effective pulse width of the output [14]. The effective pulse width τ_{eff} was calculated from the main frequency lobe width and has a value of

$$\tau_{eff} \simeq \frac{2}{3.1 \times 100 \text{ MHz}} = 6.45 \text{ nsec.}$$

Consequently for τ_{eff} = 6.45 nsec and PRF = 10 MHz, the representative "output CW" signal level is -16.2 dBm, resulting in a gain (G) of $|-16.2 \text{ dBm} - (28 \text{ dBm})| \simeq 11.8$ dB. De-embedding the delay line insertion loss at the input frequency of 371 MHz produces a gain (G) of approximately 13 dB.

The theoretical gain (G) for G_n = 3328, $(2B/N) \cdot \tau_1 = 1$, $2B \cdot \tau_2 = 1$, $G_o = 1$, $R_m = 50\Omega$, $R_{si} = 49\Omega$, $R_{in} = 2500\Omega$, C = 6.4 pf, τ_1 = 850 psec, $R_o = 20K\Omega$, C_o = 2.7 pf, $R_1 = 1000\Omega$, $R_{so} = 49\Omega$ and τ_2 = 850 psec is 11.1 dB. It should be noted that the gain equation given in Section 2.0 was derived assuming the sampling pulse width was less than or equal to the propagation delay time between adjacent channels [3]. Since the pulse width is larger than the propagation delay time between adjacent channels, the slight difference in the theoretical and experimental values is believed to be a result of this.

The maximum output power level is

$$-27 \text{ dBm} + G = 15.2 \text{ dBm}$$

or -14.0 dBm for the de-embedded microstrip line. With the aid of equation 2.3, the theoretical maximum output power level for V_b = 12V, $R_s = 49\Omega$, $R_L = 25\Omega$ and $R_b = 4.7$ KΩ is -14.1 dBm.

The (output) frequency response of the system, for a sampling pulse width of 850 psec, is given in Fig. 4.14. The 3 dB cutoff frequency of 840 MHz in this case is governed by the band-reject filter characteristic of the meander delay lines. Consequently, the theoretical cutoff frequency cannot be compared for a sampling pulse width of 850 psec. However, by increasing the output pulse width the cutoff frequency can be lowered enabling verification of the theoretical expression. For an output pulse width of 1.25 nsec, a theoretical cutoff frequency of ($1/2\tau_2$ = B) 400 MHz is predicted. The experimentally determined cutoff frequency for a 1.25 nsec pulse width as shown in Fig. 4.15 is 615 MHz. It appears from this result that the empirical formula used to predict the cutoff frequency considerably underestimates the actual cutoff frequency. Given present minimum pulse widths of 100 picoseconds amplification of signals to 5-8 GHz appears feasible using the techniques outlined in this report.

4.3.4 Multiple Signal Reconstruction

The ability to reproduce complex multiple signals simultaneously is important in many applications. This capability has been found to exist in the sampling amplifier as is illustrated in Fig. 4.16. In Fig. 4.16 (a) a single output signal centred about 372 MHz is shown. When a second signal is applied at 633 MHz no additional frequency spectra, besides the primary ones, are evident, indicating that the prototype sampling amplifier is a linear device. It should be noted that the maximum input (and output) amplitude of individual signals in this case is further limited since the 1 dB compression point is a function of the combined signal levels.

4.3.5 Frequency Conversion

Another important feature of the sampling amplifier is illustrated in Fig. 4.17. The top trace represents a properly terminated sampling amplifier. The lower trace illustrates what is created by having an open-circuit at one end of the output meander line. A primary output pulse as well as a reflected

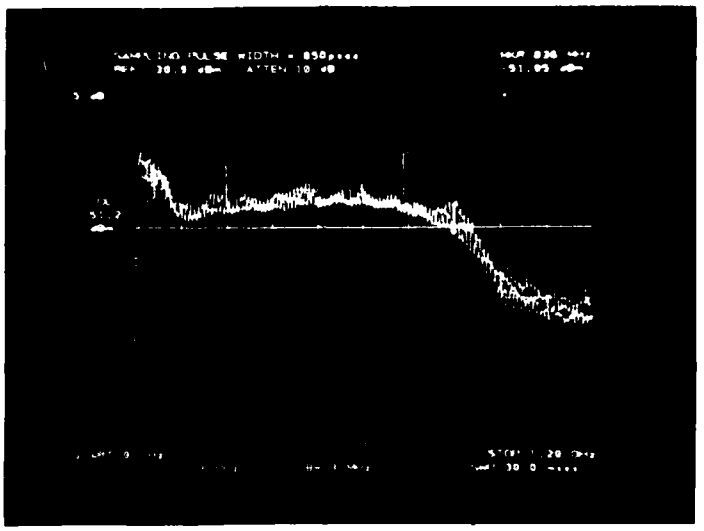


FIGURE 4.14 - OUTPUT FREQUENCY RESPONSE FOR AN OUTPUT SAMPLING PULSE WIDTH OF 850 psec

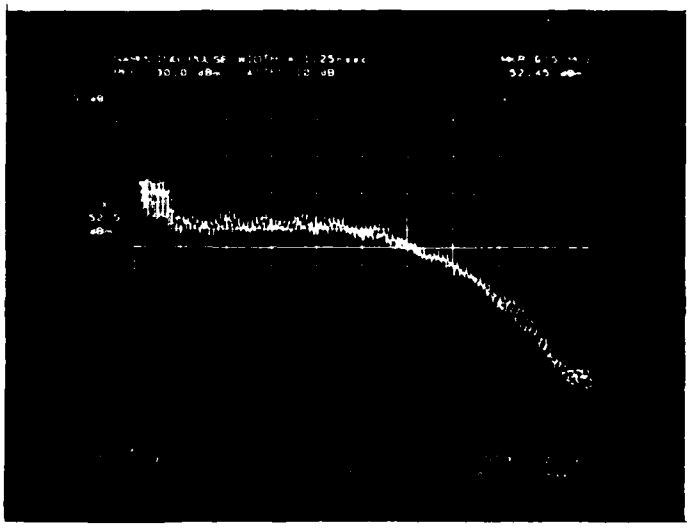
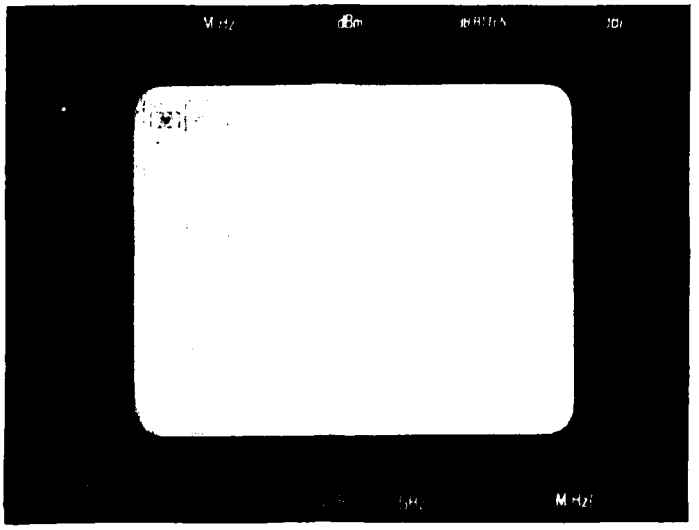
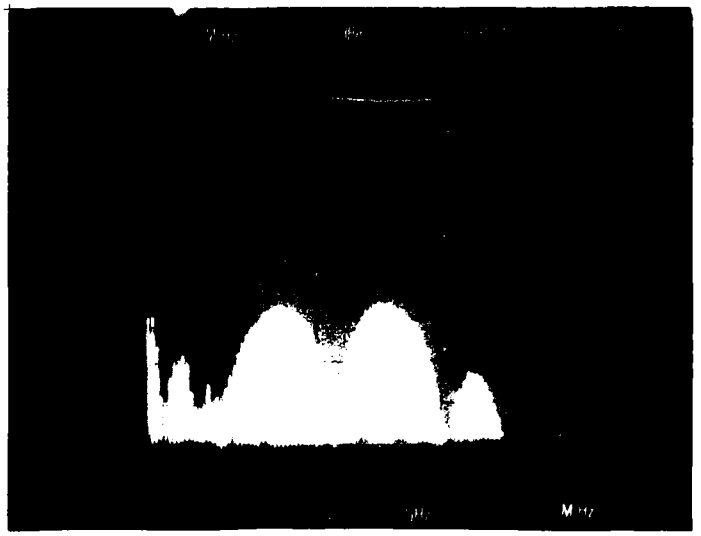


FIGURE 4.15 - OUTPUT FREQUENCY RESPONSE FOR AN OUTPUT SAMPLING PULSE WIDTH OF 1.25 nsec



(a)



(b)

FIGURE 4.16 - (A) UNFILTERED OUTPUT FOR A SINGLE INPUT SIGNAL
(B) UNFILTERED OUTPUT FOR TWO INPUT SIGNALS

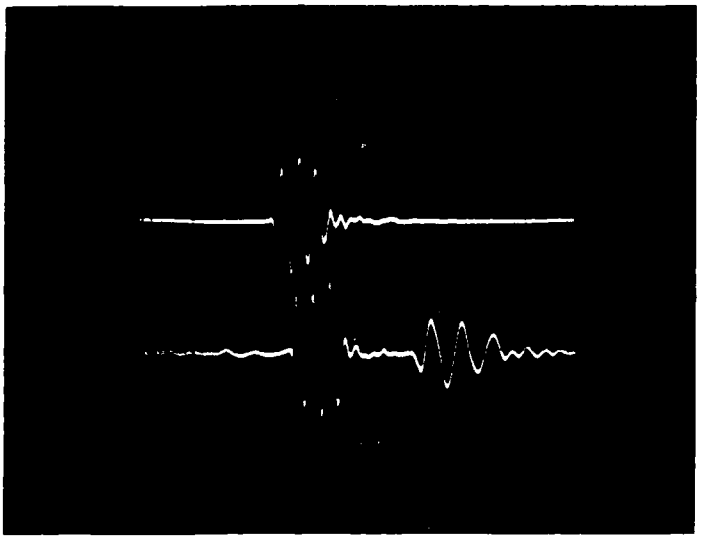


FIGURE 4.17 - OUTPUTS OF THE SAMPLING AMPLIFIER FOR THE TERMINATED AND UNTERMINATED CASES

waveform, as a result of the open circuit, are produced. The delay between the primary and reflected pulse was created by inserting an extra length of cable at the open circuit end. It is evident that the reflected pulse is of a differenct fundamental frequency. This difference in the reflected pulse frequency from the input frequency is a result of the sampling method undertaken. The delay introduced in the pulse line (Fig. 4.18) as the sampling pulse travels from the first channel to the second channel and so on, results in the first channel being sampled before the second and the second before the third and so on. Proper reconstruction of the input frequency will be maintained if the method of sampling at the output is identical to that of the input. However, the waveform which travels towards the open circuit end has a greater delay between sampled waveforms changing its fundamental frequency component to a lower value. This frequency conversion in the prototype sampling amplifier reduces the sampled input frequency by a factor of approximately 1.7.

Other methods are possible to obtain frequency conversion of this nature. Particularly, lengthening the output meander line with respect to the input meander line will down-convert the input frequency, while shortening the output meander line with respect to the input meander line will up-convert the input frequency [3]. This conversion process may have application in a communication type of repeater where isolation between the receive channel and transmit channel is necessary.

4.3.6 Summary of Results

A summary of the results is given in Table 4.1. Both experimental and de-embedded experimental values are shown. Theoretical values which exclude the meander delay line's insertion loss are also given.

TABLE 4.1

SUMMARY OF RESULTS

	SENSITIVITY S* (1) dBm	1 dB COMPRESSION POINT (INPUT) dBm	MAX. PEAK OUTPUT POWER LEVEL dBm	DYNAMIC RANGE dB	GAIN G dB	MAXIMUM FREQUENCY OF OPERATION (2) MHz	
						P.W. nsec	
						0.85	1.25
EXPERIMENTAL VALUES	-40	-27	-15.2	13	11.8	-	-
DE-EMBEDDED EXPERIMENTAL VALUES	-38.5	-25.5	-14.0	13	13.0	840	840
THEORETICAL VALUES	-	-	-14.1	-	11.1	588	400

(1) The sensitivity level is reduced for the de-embedded values since the noise level increases in this case.

(2) The maximum operating frequency of 840 MHz was limited as a result of the filter-like characteristic of the input meander delay line. The value given for the increased input pulse of 1.25 nsec allows verification of the theoretical cutoff frequency.

FIGURE 4.18 - PROTOTYPE 20 CHANNEL SAMPLING AMPLIFIER

5.0 FUTURE WORK AREAS

5.1 Introduction

The development of another sampling amplifier is planned. This prototype would incorporate improvements to alleviate some of the problems associated with the sampling gate. In particular, the development of a high PRF pulse generator/driver, reduction of the sampling gate signal feedthrough, investigation of suitable amplifiers in recognition of a high sampling rate and further development of the sampling feed structure should be undertaken.

5.2 Impulse Generator Development

The requirement for a high PRF impulse generator is desirable since the number of channels for complete reconstruction would be lower reducing the size and cost of the sampling amplifier. Avtech Electrosystems Ltd. of Ottawa, under the sponsorship of DREO, have developed a high pulse repetition rate impulse generator (Fig. 5.1). The unit provides complementing positive and negative matched outputs. The impulse waveform illustrated in Fig. 5.2 shows an output impulse of 11 volts having a pulse width of 100 psec measured at half amplitude for a PRF of 250 MHz.

5.3 Multi-channel Parallel Feed Structure

In the present prototype sampling amplifier design, the pulses which activate the sampling gates as they travel down the line are attenuated and may be broadened somewhat in width as a result of impedance loading of the sampling gates. The resulting difference from gate to gate in the sampling pulses degrades the fidelity of the voltage samples from channel to channel and hence degrades the fidelity of the reconstructed signal.

A multi-channel parallel feed structure as illustrated in Fig. 5.3 would have N parallel feed lines connected to individual sampling gates. All

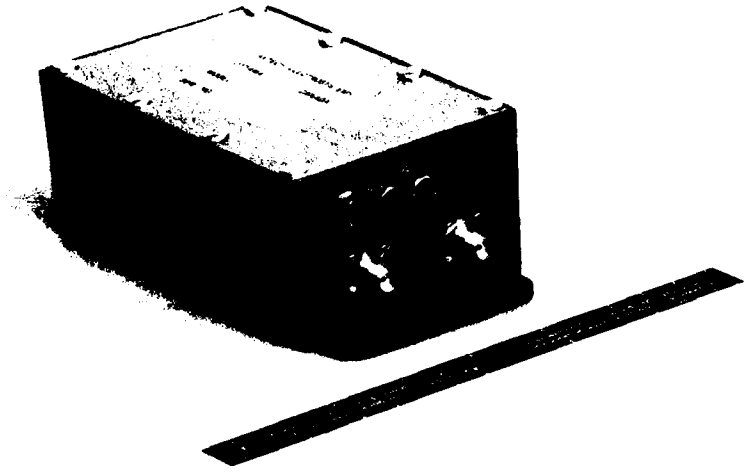


FIGURE 5.1 - HIGH PULSE REPETITION RATE IMPULSE GENERATOR

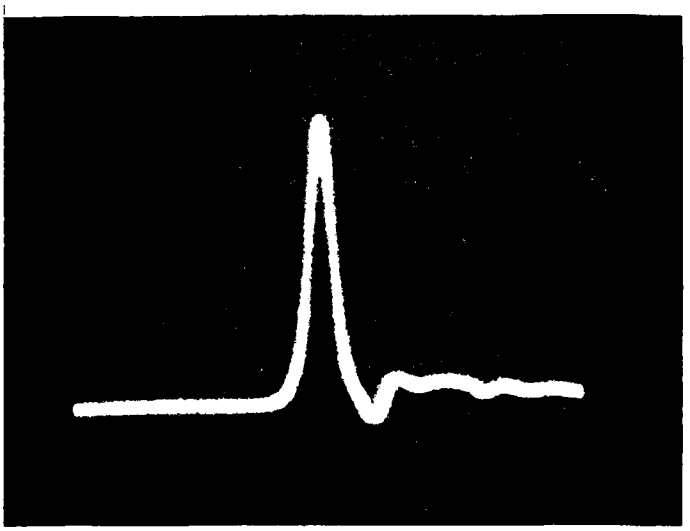


FIGURE 5.2 - OUTPUT IMPULSE WAVEFORM

lines would be driven by one pulse generator/driver. Each line would be of equal length and characteristic impedance thus making simultaneous sampling possible.

The property of sampling the parallel channels simultaneously has the additional advantage of being able to stretch the output r.f. pulse by a factor of 2. Fig. 5.3 illustrates this concept. A current waveform I_0 is sampled onto the output meander line where it divides into two equal portions at node 1. I_2 travels down the meander line to the output (2) where it is transmitted. I_1 travels towards the load end where a short has replaced the previously used termination resistor. Once I_1 reaches 3 the waveform is reflected causing it to travel towards the output (2) where it is transmitted. Applying this concept to all the waveforms of the other parallel channels one will recognize that an r.f. pulse will be created with twice the pulse width at the same r.f. frequency.

This property is extremely useful as the number of parallel channels may be reduced by a factor of 2 which leads to increased efficiency $(\frac{\text{rf power out}}{\text{prime power in}})$ and cost reduction.

This approach should minimize the serial loading effects due to the diode gates. Hence, the waveshape and amplitude of the sampling pulses would be the same at each of the parallel sampling gates, insuring that each channel operates in the same manner. This in turn leads to high fidelity reconstruction of the r.f. signal. There may be a need for impedance matching between generator and parallel lines for optimum performance.

6.0 CONCLUSIONS

6.1 Summary and Conclusions

In this report a distributed sampling technique for carrying out wideband signal amplification has been proposed. This new concept for microwave

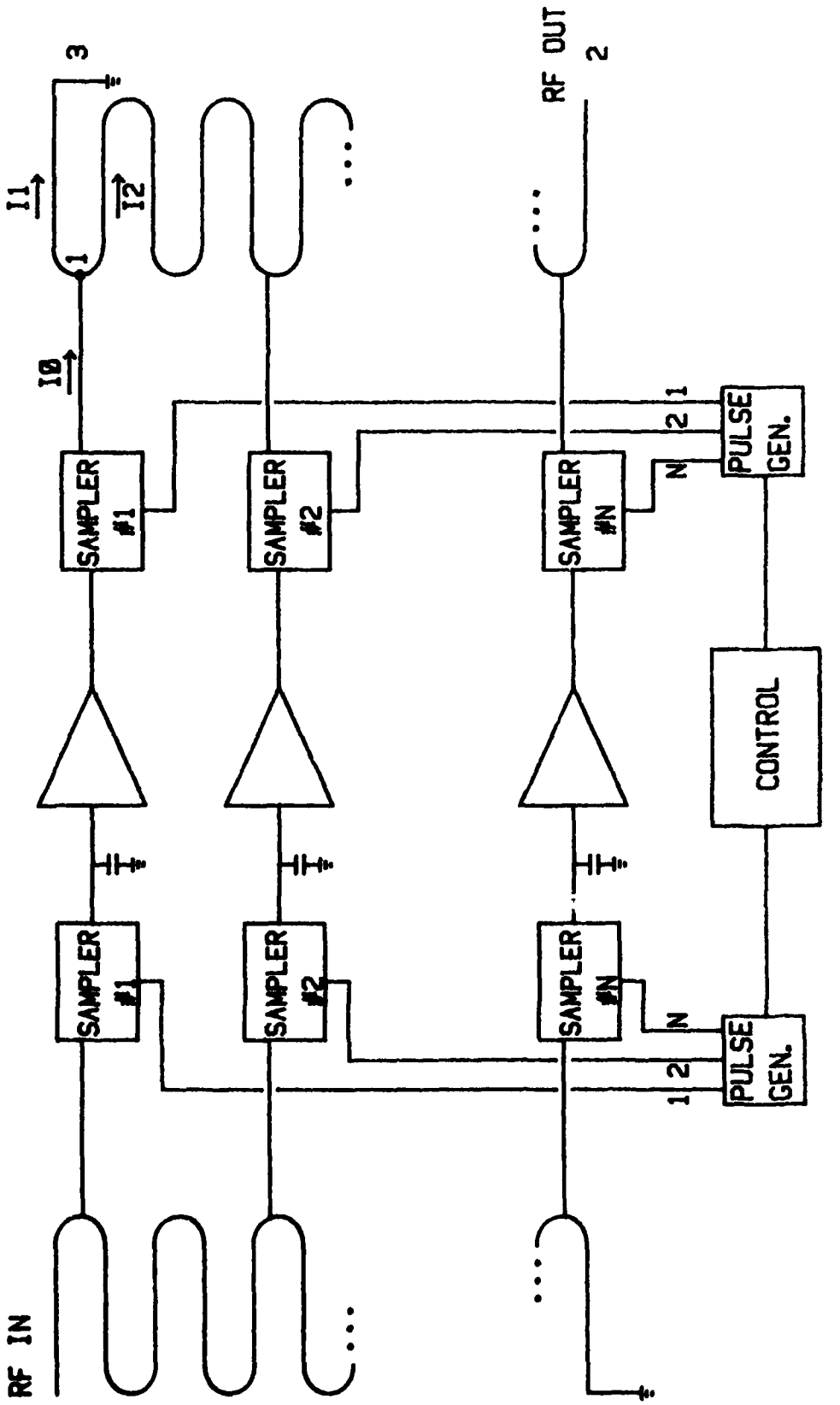


FIGURE 5.3 - MULTI-CHANNEL PARALLEL FEED STRUCTURE

amplification shows attractive features of very wideband operation and multiple signal handling capability.

Sampling techniques permit wideband signal amplification using delay lines and low pass narrowband amplifiers. The scheme allows amplification of signals at frequencies far above the cutoff frequencies of the amplifying devices used.

From the experimental results, it was concluded that it was possible to achieve amplification of signals to 840 MHz with a gain of 11 dB. The system overall performance was essentially as predicted. Output power level and frequency response limitations observed in the prototype circuit were primarily a result of the sampler characteristics. Additionally, sensitivity and dynamic range limitations were due to the electrical mismatch of individual diodes in the sampler units. The maximum frequency of operation is directly dependent on the minimum pulse width achievable. Consequently, wideband amplification of r.f. signals to 8 GHz is believed possible using the techniques outlined in this report. Other circuit techniques may allow even greater bandwidths.

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APPENDIX A

MICROSTRIP DESIGN EQUATIONS, PROGRAM LISTING AND DESIGN TABLE

Hammerstad's expressions [4] include useful relationships defining both characteristic impedance and effective dielectric constant:

For $W/h < 1$,

$$Z_o = \frac{60}{\sqrt{\varepsilon_{eff}}} \ln(8h/W + 0.25\ W/h)$$

where

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left[(1 + 12h/W)^{-\frac{1}{2}} + 0.04(1 - W/h)^2\right]$$

For $W/h > 1$,

$$Z_o = \frac{120\pi\ \sqrt{\varepsilon_{eff}}}{W/h + 1.393 + 0.667\ \ln(W/h + 1.444)}$$

where

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} (1 + 12h/W)^{-\frac{1}{2}}.$$

Hammerstad notes that the maximum relative error in ε_{eff} and Z_o is less than ±0.5 percent and 0.8 percent, respectively, for $0.05 < W/h < 20$ and $\varepsilon_r < 16$.

If the conductor thickness is taken into account the strip width, W, is replaced by an effective strip width W_e. Expressions for W_e are:

For $W/h > 1/2\pi$,

$$\frac{W_e}{h} = \frac{W}{h} + \frac{t}{\pi h} \left(1 + \ln \frac{2h}{t}\right).$$

For $W/h < 1/2\pi$,

$$\frac{W_e}{h} = \frac{W}{h} + \frac{t}{\pi h} \left(1 + \ln \frac{4\pi W}{t}\right).$$

Additional restrictions for applying the above are $t < h$ and $t < W/2$.

PROGRAM LISTING

```
"MICROSTRIP PARAMETERS":
"We/H→S, W/H→M, eff. dielectric→Q ":
"":
"MATHEMATICAL FORMULAS WERE OBTAINED FROM ":
"MICROWAVES MAY 1977 P-174 ":
"ALL CALCULATIONS INCLUDE THE EFFECTIVE WIDTH DUE TO THE ":
" LINE THICKNESS ":
"FURTHER INFO MAY BE OBTAINED FROM MICROWAVES MAY 1977 ":
"THE SOFTWARE LANGUAGE IS HPL":
"FURTHER INFO ON SOFTWARE PROGRAMMING MAY BE OBTAINED FROM REF. [15]":
: fxd 4
 "":
: ent "dielectric constant",E
: ent "line thickness",T
: ent "dielectric thickness",H
: ent "start W/H at ?",M
: ent "stop W/H at ?",P
: ent "SET PRINTER 4 LINES BELOW TOP OF FORM ",K
 M-.01→M
 "start":0→N
 wtb 6,27,84
 wtb 6,27,76,int(928/64),int(928)
 fmt 1,20x,"MICROSTRIP PARAMETERS",4b,8x,"permittivity=",f5.2
 wrt 6.1,13,10,10,10,E
 fmt 2,8x,"line thickness=",f5.2,"mils",9x,"board thickness=",f5.2,"mils"
 wrt 6.2,T,H
 fmt 1,2b,10x,"W/H",10x,"Zo",10x,"Eeff",10x,"W",10x,"We"
 wrt 6.1,13,10
 fmt 1,1b
 wrt 6.1,13
 "one":M+.01→M
 H*M→W
 if M<1/2π;gto "first"
 M+T/πH*(1+ln(2H/T))→S
 S*H→C
 gto "try"
 "first":M+(T/πH)(1+ln(4πW/T))→S
 S*H→C
 "try":if S>1;gto "second"
 (E+1)/2+(E-1)/2*((1+12/S)^(-.5)+.04(1-S)^2)→Q
 (60/√Q)ln(8/S+.25S)→Z
 gto "prin"
 "second":(E+1)/2+((E-1)/2)(1+12/S)^(-.5)→Q
 120π/√Q/(S+1.393+.667*ln(S+1.444))→Z
 "prin":N+1→N
 fmt 2,10x,f4.2,f13.2,f13.3,f12.2,f11.3
 wrt 6.2,M,Z,Q,W,C
 if M=P;gto "out"
 if N>49;gto "start"
 gto "one"
 "out":end
```

MICROSTRIP DESIGN TABLE

MICROSTRIP PARAMETERS

permittivity = 2.20
line thickness = 1.50 mils board thickness = 20.00 mils

W/h	Z_o	ε_{eff}	W	W_e
2.80	52.33	1.865	56.00	58.045
2.81	52.21	1.865	56.20	58.245
2.82	52.09	1.866	56.40	58.445
2.83	51.98	1.866	56.60	58.645
2.84	51.86	1.866	56.80	58.845
2.85	51.74	1.867	57.00	59.045
2.86	51.63	1.867	57.20	59.245
2.87	51.51	1.867	57.40	59.445
2.88	51.39	1.868	57.60	59.645
2.89	51.28	1.868	57.80	59.845
2.90	51.16	1.868	58.00	60.045
2.91	51.05	1.869	58.20	60.245
2.92	50.94	1.869	58.40	60.445
2.93	50.82	1.869	58.60	60.645
2.94	50.71	1.870	58.80	60.845
2.95	50.60	1.870	59.00	61.045
2.96	50.49	1.871	59.20	61.245
2.97	50.38	1.871	59.40	61.445
2.98	50.27	1.871	59.60	61.645
2.99	50.16	1.872	59.80	61.845
3.00	50.05	1.872	60.00	62.045
3.01	49.94	1.872	60.20	62.245
3.02	49.83	1.873	60.40	62.445
3.03	49.73	1.873	60.60	62.645
3.04	49.62	1.873	60.80	62.845
3.05	49.51	1.874	61.00	63.045
3.06	49.41	1.874	61.20	63.245
3.07	49.30	1.874	61.40	63.445
3.08	49.19	1.875	61.60	63.645
3.09	49.09	1.875	61.80	63.845
3.10	48.99	1.875	62.00	64.045

APPENDIX B

EXPRESSIONS FOR MICROSTRIP CONDUCTOR AND DIELECTRIC LOSSES

Expressions for the conductor loss derived by Pucel [7] account for the nonuniform current distribution on the conductor. These relationships are expressed in terms of the characteristic impedance Z_o, the dielectric substrate thickness h, the conductor and effective conductor strip width W and W_e, the conductor strip thickness t, the free space permeability μ_o, the conductivity of the material σ and the frequency f. For a fixed characteristic impedance, conductor loss decreases inversely with substrate thickness and increases with the square root of the frequency.

In the prototype circuit, where $W/h \simeq 3.0$ (Appendix A), the conductor loss is given by [7]

$$\alpha_c = \frac{8.68\ R}{Z_o h\{\frac{W_e}{h} + \frac{2}{\pi}\ln[2\pi e(\frac{W_e}{2h} + 0.94)]\}^2}\ (\frac{W_e/\pi h}{\frac{W_e}{2h} + 0.94} + \frac{W_e}{h})$$

$$\cdot\ \{1 + (\frac{h}{W_e} + \frac{h}{\pi W_e}[\ln(\frac{2h}{t} + \frac{t}{h})]\}\text{dB/cm},$$

where R is the surface resistivity for the conductor and is given by

$$R = \sqrt{\frac{\pi f \mu_o}{\sigma}}\ .$$

Thus, for $Z_o = 50\Omega$, h = .0508 cm, $W_e/h = 3.097$ (Appendix A), t = .0038 cm, $\mu_o = 4\pi \times 10^{-7}$ H/m, $\sigma = 5.80 \times 10^7$ υ/m (copper conductor)

$$\alpha_c = 1.417 \times 10^{-11}\sqrt{f}\ \text{dB/cm}.$$

Welch and Pratt [8] and Schneider [9] have derived the expression for the attenuation constant for a dielectric. The equation given by

$$\alpha_d = 27.3\ \frac{\varepsilon_r}{(\varepsilon_{eff})^{\frac{1}{2}}} \cdot \frac{\varepsilon_{eff-1}}{\varepsilon_{r-1}} \cdot \frac{\tan\delta}{\lambda_o}\ \text{dB/cm}$$

is expressed in terms of the dielectric constant ε_r, the effective dielectric constant ε_{eff}, the loss tangent (or dissipation factor) tan δ, and the free

space wavelength λ_o. Thus, for $\varepsilon_r = 2.2$ $\varepsilon_{eff} = 1.872$ (Appendix A), and tanδ = .0004 (manufacturer's specification)

$$\alpha_d = \frac{2.227 \times 10^3}{\lambda_o} = 74.23 \times 10^{-15} \text{ f dB/cm.}$$

Consequently, the total loss is

$$\alpha = \alpha_c + \alpha_d = 1.417 \times 10^{-11} \cdot \sqrt{f} + 7.423 \times 10^{-16} \cdot f \text{ dB/cm.}$$

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The current trend to higher and higher signal processing speeds in radar, communication and EW systems is well known. The flexibility offered by sampling techniques for carrying out these processing functions is also widely recognized. To provide high effective sampling rates, a novel distributed parallel sampling approach using relatively narrow-band parallel channels has been developed at DREO. This unique integration of delay lines, sampling gates and amplifiers allows for amplification of wideband r.f. signals at frequencies far above the cut-off frequencies of the amplifying devices used.

A discussion of the distributed sampling concept, the design of a prototype circuit and a comparison of theoretical and experimental results, demonstrating successful signal amplification approaching the gigahertz regime, are presented in this report. Other potential application areas which are well matched to this type of processing are also mentioned.

DSIS

KEY WORDS

Distributed Sampling
Picosecond Sampling
Wideband Amplification
Microwave
Device Technology
Microwave Processing

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